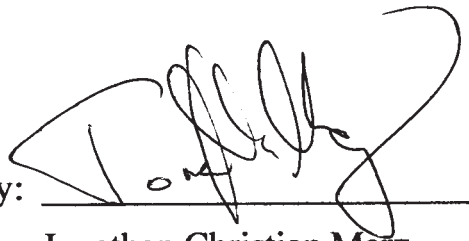


I, Jonathan Christian Merz, declare as follows:

1. I am over 21 years of age and am competent to make this declaration.
2. I am a native speaker of English.
3. I am fluent in Japanese.
4. I have 15 years of experience translating Japanese to English.
5. I translated the attached patent document "JP3141621B2" from Japanese to English.
6. I certify that the translation of the document "JP3141621B2" is, to the best of my knowledge, a true and accurate translation from Japanese to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed: August 28, 2024

By: 
Jonathan Christian Merz

(19) Japan Patent Office (JP)

(12) Japanese Patent Gazette (B2)

(11) Patent No.: 3141621 (P3141621)

(24) Registration Date: December 22, 2000 (2000.12.22)

(45) Issuance Date: March 5, 2001 (2001.3.5)

(51) Int. Cl. ⁷ ID		FI		
H01L	21/762	H01L	21/76	D
	27/12		27/12	B
Number of Claims:				1
Total Number of Pages:				4

(21) Patent Application No.: H5-124568		(73) Patent owner: 000005234
(22) Filing Date: May 27, 1993 (1993.5.27)		FUJI ELECTRIC CO., LTD. 1-1 Tanabe Shinden, Kawasaki-ku, Kawasaki-shi, Kanagawa Prefecture
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(43) Publication date: December 2, 1994 (1994.12.2)		c/o Fuji Electric Co., Ltd. 1-1 Tanabe Shinden, Kawasaki-ku, Kawasaki-shi, Kanagawa Prefecture
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(54) Title of Invention

SEMICONDUCTOR SUBSTRATE COMPRISING DIELECTRIC-ISOLATION STRUCTURE

(57) Claims

1. A semiconductor substrate comprising a dielectric-isolation structure, in which: two silicon substrates are bonded sandwiching a silicon oxide film; an isolation groove that reaches the silicon oxide film and has a rectangular cross-sectional shape is formed surrounding the perimeter of an element region on one side thereof; an oxide film is formed on a groove-interior side surface of the isolation groove, whereupon polysilicon is deposited by a CVD method so as to fill the groove interior; and planarization is performed by removing the polysilicon deposited on the substrate front surface; wherein:

the isolation groove is formed at the same groove width around the entire perimeter region thereof, a corner portion of the isolation groove is formed in an arc-shaped groove pattern such that the inner perimeter and the outer perimeter of the groove become concentric circles, the isolation groove is independently formed in each element region, and a dummy region is formed between element regions divided by the isolation groove.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

FIELD OF INDUSTRIAL APPLICABILITY

The present invention relates to a semiconductor substrate comprising a dielectric-isolation structure that is applied to a monolithic IC circuit or the like.

[0002]

RELATED ART

In monolithic IC circuits, in which a plurality of active elements and a plurality of passive elements are integrally formed on a single semiconductor substrate, various isolation methods, such as P-N junction isolation methods as well as groove-filling isolation methods and dielectric isolation methods, are known as techniques for isolating element regions (islands) from each other; in particular, dielectric isolation methods are often used because they yield extremely small isolation capacitance and large isolation withstand voltage, latch-up prevention effects, and higher integration density compared to P-N junction isolation methods.

[0003]

In addition, as a semiconductor substrate

comprising a dielectric-isolation structure (referred to hereinafter as a "dielectric-isolation substrate"), there is known a configuration wherein: two silicon substrates are bonded sandwiching a silicon oxide film, whereupon an isolation groove that reaches the silicon oxide film and has a rectangular cross-sectional shape is formed, by trench etching, surrounding the perimeter of an element region on one side thereof; an oxide film is formed on a groove-interior side surface of the isolation groove, after which polysilicon (polycrystalline silicon) is embedded in the isolation groove interior by a CVD method; and planarization is performed by removing the polysilicon deposited on the substrate front surface by etch-back, polishing, or the like.

[0004]

Next, a general method of manufacturing the dielectric isolation substrate will be described with reference to FIG. 3. In FIG. 3(a), 1 is a single-crystal silicon substrate on which a semiconductor element is to be fabricated, 2 is a silicon substrate serving as a support substrate, and 3 is a silicon oxide film (SiO_2) embedded between the silicon substrates 1 and 2. First, the silicon oxide film 3 is formed on the rear-surface side of the silicon substrate 1 by thermal oxidation. Next, the silicon substrate 2 serving as a support substrate is laid over the silicon substrate 1 with the silicon oxide film 3 interposed therebetween; thermal treatment is performed to form a silicon-on-insulator (SOI) wafer 4, after which an etch mask layer (e.g., silicon dioxide, silicon nitride) 5 is formed on the front surface of the silicon substrate 1; and an isolation groove formation region patterned to surround the perimeter of an element region is opened in the mask layer.

[0005]

Next, as shown in FIG. 3(b), trench etching is performed from the opening in the etch mask layer 5 by reactive ion etching or the like to form isolation grooves 6 having rectangular cross-sectional shapes that reach the silicon oxide film 3; next, thermal oxidation is performed to form silicon oxide films 7 on groove-interior sidewalls of the isolation grooves 6, as shown in FIG. 3(c). Next, as shown in FIG. 3(d), a polysilicon layer 8 is deposited on the SOI wafer 4 from the front-surface side of the silicon substrate 1 by a reduced-pressure CVD method or the like to fill in the isolation grooves 6, after which etch-back is performed on the front-surface side of the silicon substrate 1 to remove the polysilicon layer 8 on the substrate front surface, and the silicon oxide film on the substrate front surface is removed by hydrofluoric acid washing. Thereby, as shown in FIG. 3(e), element regions (islands) 9, which are isolated by the silicon oxide films 3, 7 and the polysilicon layer 8, are formed on the silicon substrate 1. Note that elements, such as transistors and diodes, are fabricated on the dielectric-isolation substrate in each element region 8, and the elements are connected to each other to constitute a monolithic IC circuit.

[0006]

PROBLEMS TO BE SOLVED BY THE INVENTION

Incidentally, when manufacturing the dielectric-isolation substrate, there is a problem in that, when embedding the polysilicon layer 8 in the isolation grooves 6 in existing configurations, more polysilicon than expected must be deposited to completely fill the entire perimeter regions thereof. Next, this will be described with reference to FIG. 4 and FIG. 5. That is, when the polysilicon layer 8 is filled into the isolation grooves 6 formed in the silicon substrate 1 of the SOI wafer 4 in FIG. 4 by a reduced-pressure CVD method, the polysilicon layer 8 is deposited, at a uniform growth rate, on the front surface of the silicon substrate 1 and the sidewall surfaces of the isolation grooves 6. Note that w1-w4 in the drawings schematically represent

the growth of the polysilicon layer 8 over time. Here, if the groove width of the isolation grooves 6 is defined as W and the groove depth is defined as D, ideally, when the deposition thickness of the polysilicon layer 8 has become W/2, the isolation grooves 6 are completely filled up and the deposited layer on the substrate front-surface side becomes planar.

[0007]

In practice, however, an excess deposition thickness greater than W/2 is required to make the polysilicon layer 8 planar across the entirety of the substrate front surface; the reasons for this are as follows. That is, in existing dielectric-isolation substrates, the isolation grooves 6 surrounding the perimeters of the element regions 9 are formed in a rectangular pattern combining the rectilinear grooves as shown in FIG. 5(a), (b); in the corner portions of the isolation grooves 6 in (a) and the intersection portions of the grooves in (b), the diagonal groove width W_c of the isolation grooves 6 is approximately 1.4 times the groove width W of the other rectilinear portions. For this reason, in the process of progressively depositing the polysilicon layer 8 by a CVD method, the corner portions and intersection portions of the isolation grooves 6 cannot be completely filled in simply by making the deposited layer thickness be W/2, and it is therefore necessary to deposit additional excess polysilicon beyond the deposition thickness of W/2 to completely fill in the entire perimeter regions of the isolation grooves 6. Moreover, such excessive deposition of polysilicon not only increases the amount of material used, but also affects the etch-back process performed as post-processing, making it difficult to planarize the substrate and, by extension, also becoming a factor leading to increased manufacturing costs.

[0008]

The present invention was conceived in view of the points described above and has an object of providing a dielectric-isolation substrate that, by improving the formation pattern of the isolation grooves, makes it possible, when embedding the polysilicon in the isolation grooves by a CVD method, to fill in the isolation grooves to the minimum required deposition thickness without deficiency or excess.

[0009]

MEANS FOR SOLVING THE PROBLEMS

To achieve the object described above, isolation grooves formed between element regions are formed at the same groove width around the entire perimeter regions thereof in a dielectric-isolation substrate of the present invention. Furthermore, as a specific configuration thereof, a corner portion of each isolation groove is formed in an arc-shaped groove pattern in which the inner perimeter and the outer perimeter of the groove become concentric circles.

[0010]

In addition, in the aforementioned configuration, implementation is performed by independently forming an isolation groove for each element region and forming a dummy region between the element regions isolated by the isolation groove.

[0011]

EFFECTS

According to the configuration described above, in the process of depositing polysilicon in the isolation grooves by a CVD method to fill the grooves, the entire perimeter regions of the isolation grooves, including the corner portions, are completely filled in by the polysilicon layer when the deposition thickness reaches 1/2 of the groove width; in addition, the polysilicon layer deposited on the front surface of the silicon substrate is also planarized, and the filling of the isolation grooves with polysilicon is performed without deficiency or excess. In addition, intersection of the isolation grooves with each other can be

(3) SEMICONDUCTOR SUBSTRATE COMPRISING DIELECTRIC-ISOLATION STRUCTURE

avoided by, in particular, independently forming an isolation groove for each element region and forming a dummy region between the element regions isolated by the isolation groove.

[0012]

Working Examples

Working examples of the present invention will be described below on the basis of the drawings. Note that the dielectric-isolation substrates in the illustrated examples were fabricated via the manufacturing method described in FIG. 3. First, in FIG. 1, an isolation groove 6 trench-etched in a silicon substrate of an SOI wafer 4 surrounding the perimeter of an element region 8 was formed by connecting rectilinear groove portions and a corner groove portion exhibiting an arc-shaped pattern, and the groove widths thereof were designed so as to have the same groove width W along the entire perimeter region. That is, in the corner portion of the isolation groove 6, the groove inner perimeter (radius of curvature $r1$) and the groove outer perimeter (radius of curvature $r2$) were concentric circles as seen from the inner side of the element region 9, and the difference $r2 - r1$ between the radii of curvature $r1$ and $r2$ was set so as to become the same groove width W as in the rectilinear portions.

[0013]

As a result of such a configuration, in the process of depositing the polysilicon layer 8 by a CVD method and embedding it in the isolation grooves 6 as described in FIG. 3, when the deposition thickness of the polysilicon layer 8 reached $W/2$ with respect to the groove width W , as described in FIG. 4, the isolation grooves 6 were completely filled in, without deficiency or excess, and the polysilicon layer deposited on the front surface of the silicon substrate was also planarized.

[0014]

In addition, FIG. 2 illustrates an applied working example that is a development of the aforementioned example; in instances in which the element regions 9 are formed on the SOI wafer 4 arranged in a grid shape, an isolation groove 6 is independently formed for each of the element regions 9, and a dummy region 10 partitioned off by the isolation grooves 6 is formed between the element regions 9. According to this isolation groove pattern, intersection of the isolation grooves can be avoided, and the occurrence of the disadvantage described in FIG. 5(b) can be avoided.

[0015]

EFFECTS OF THE INVENTION

According to the present invention, as described above, when filling, with polysilicon by a CVD method, the groove interiors of the inter-element isolation grooves formed in the dielectric-isolation substrate, the entire perimeter regions of the isolation grooves can be planarly filled in to the minimum required deposition thickness without deficiency or excess. Accordingly, it is possible to provide a semiconductor substrate comprising a dielectric-isolation structure that, in addition to streamlining the isolation groove embedding process, has high practical value such as achieving a reduction in manufacturing costs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a partial plan view of a dielectric-isolation substrate according to a working example of the present invention.

FIG. 2 is a partial plan view of a dielectric-isolation substrate according to an applied working example of the present invention.

FIG. 3 is an explanatory illustration of a general method of manufacturing a dielectric-isolation substrate, wherein (a)–(e) are cross-sectional views of the dielectric-isolation substrate depicted in manufacturing process order.

FIG. 4 is an illustration schematically representing growth in deposition thickness over time when filling, with polysilicon by a CVD method, isolation grooves in a dielectric-isolation substrate.

FIG. 5 is an illustration depicting a pattern of isolation grooves formed in an existing dielectric-isolation substrate, wherein (a) is a plan view of an isolation groove corner portion, and (b) is a partial plan view of an isolation groove intersection portion.

EXPLANATION OF THE REFERENCE NUMBERS

- | | |
|----|--|
| 1 | Silicon substrate |
| 2 | Silicon substrate (support substrate) |
| 3 | Silicon oxide film |
| 4 | SOI wafer |
| 6 | Isolation groove |
| 7 | Silicon oxide film on groove-interior sidewall |
| 8 | Polysilicon |
| 9 | Element region |
| 10 | Dummy region |

FIG. 1

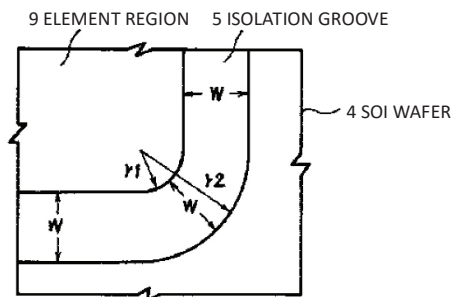


FIG. 2

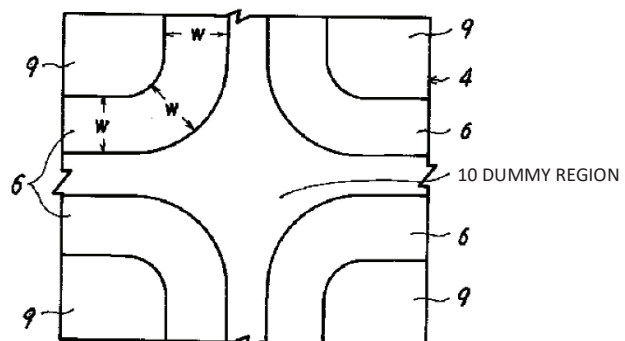


FIG. 3

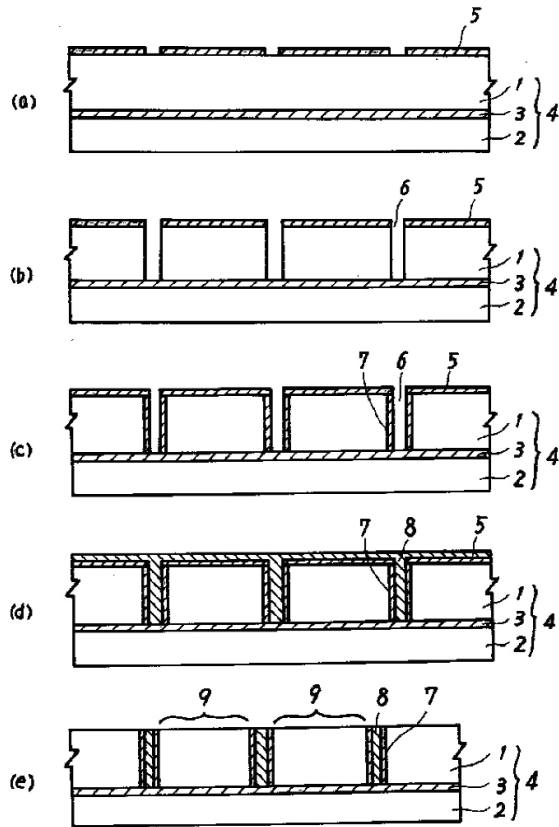


FIG. 4

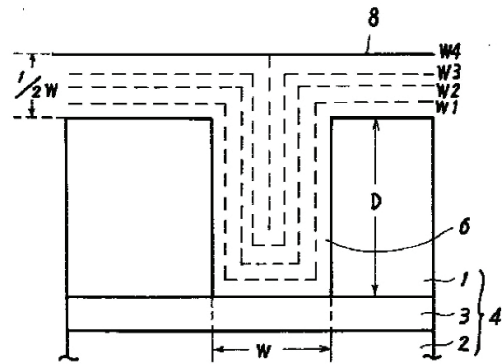
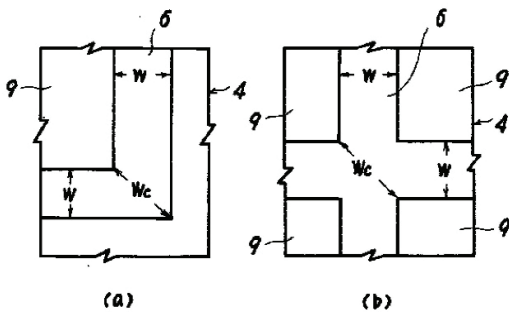


FIG. 5



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(56) Reference documents
H4-330765 (JP, A)
H4-127148 (JP, A)
H1-187944 (JP, A)
H3-62946 (JP, A)

(58) Fields searched (Int. Cl.⁷, database name)

H01L 21/762
H01L 27/12