

RELIABILITY ASSESSMENT OF DEEP TRENCH ISOLATION STRUCTURES

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ABSTRACT

An extensive investigation of the reliability of deep trench isolation structures upon reverse bias stress is performed. By using the variable base level charge pumping technique, it is shown that the degradation of the trench is primarily originating from N_h formation at the inner trench corners. The reliability is improved by introducing cut corners.

[Keywords : trench isolation, smart power, interface states, charge pumping, cut corners]

INTRODUCTION

In many smart power applications, high voltage drivers (20-80V) have to be combined on one chip with sub-micron CMOS logic for μ controllers, medium density Flash or EEPROM for data storage and even MEMS sensors. Typical applications range from industrial (printer head drivers), automotive (motor control) and medical (pace makers) [1,2]. The electrical isolation between two high voltage transistors, and between such devices and the low voltage CMOS and analogue blocks is usually achieved by standard junction isolation schemes. In this case, both the lateral (component-to-component) as well as the vertical isolation (towards the substrate) is realized by a reverse-biased junction. The lateral out-diffusion of the isolation structure is determined by the required reverse breakdown voltage, but is typically in the range of 10-20 μ m for 60-80V applications. Moreover, as these isolation junctions are typically large in area, they have a substantial leakage current which is undesirable for high temperature and low power applications [3].

The most effective way to achieve good electrical isolation is by using SOI [4-7]. However, SOI is still expensive and has an additional drawback that the buried oxide is a bad thermal conductor. As a result, integrated power devices will have less cooling via the bottom silicon and thus their application range will be limited [7,8]. An elegant alternative is the use of deep trenches as isolation structures. These trenches will substantially reduce the isolation area down to 3-5 μ m [9-12] while maintaining a good lateral isolation. The vertical isolation is still to be guaranteed by a standard reverse biased junction. The introduction of highly doped buried layers will kill the parasitic vertical substrate bipolar [11]. Hence also a good vertical isolation can be achieved. The leakage at high temperature can be solved by substrate engineering [12]. Upon reverse biasing of trench isolation structures, several mechanisms can take place : avalanche of the BLN/p-substrate junction at the trench sidewall, and the possibility of the turn-on of a parasitic MOS transistor [13].

In this paper the long-term reliability of deep trench structures upon reverse bias stress is investigated. The variable base level charge pumping technique is applied to monitor and locate the degradation [14]. The effect of cut corners on the trench reliability is investigated in detail.

TRENCH ISOLATION STRUCTURE

Trench isolation structures are processed in a 0.35 μ m based smart power technology. The technology is characterized by a non-masked low resistive BLN, on top of which a lowly doped n-epi is grown. The contact to the BLN is achieved by Nsinker which are self-aligned to the isolation trench structure. Hence every n-epi pocket is isolated from the p-substrate by the BLN. The thickness and the concentration of the n-epi determine the maximum off-state breakdown voltage of the n-type devices. The lowly-doped p-substrate is contacted at the backside. The extra process steps for both the BLN module as well as the trench module do not affect the standard CMOS process flow. An overview of the process flow is given in [11].

Fig. 1(a) shows a cross-section of the trench isolation structure, separating two n-epi pockets. The BLN and Nsinker are clearly visible. The trench is approximately 10 μ m deep, has a thick liner oxide and is filled with undoped poly silicon. A stopper implant is implanted at the bottom of the trench in order to kill the parasitic MOS. This parasitic MOS exists between the Nsinker-BLN (source)/p-substrate (bulk)/Nsinker-BLN (drain) and with liner oxide as gate oxide and the trench poly as gate electrode. The p-stop implant locally increases the doping level of the parasitic MOS and hence the threshold voltage V_{th} . Structures with encapsulated and hence electrically floating poly are processed, in addition to trenches with contacted poly. The latter are very useful as they allow to precisely bias the poly. Test structures with straight corners (Fig. 1(b)) as well as 45° cut corners (Fig. 1(c), but not drawn to scale) are investigated. For both the straight corners and cut corner structures,

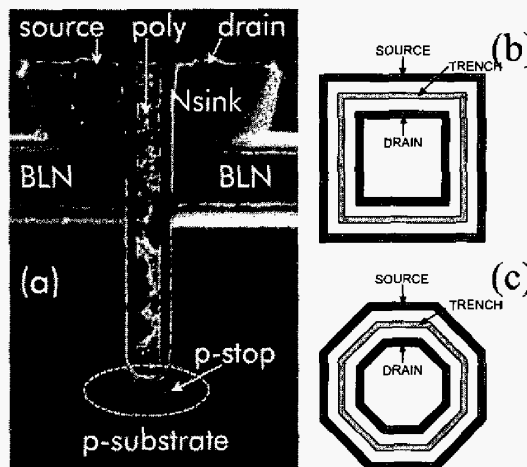


FIGURE 1. : (A) CROSS SECTION OF THE DEEP TRENCH ISOLATION STRUCTURE. (B) : TEST STRUCTURE WITH STRAIGHT CORNERS, (C) TEST STRUCTURE WITH 45° CUT CORNERS (NOT TO SCALE)

the total trench perimeter length L is equal. Typically, $L=80\text{ }\mu\text{m}$, but structures with $L=160\text{ }\mu\text{m}$ are also available. Figs 2(a) and 2(b) show top-view SEM pictures after de-layering of the straight corners and cut corners respectively. The drain contact is defined as the contact inside the trench structure. The source contact is defined as the contact outside the trench structure. A second trench is put around the complete structure in order to isolate the structures from the rest of the chip. In case of contacted trenches, only the inner trench is contacted; the outer trench has floating poly. Figs 2(c) and 2(d) show a zoom-in of Figs 2(a) and 2(b) respectively, highlighting the corners of the structures. The double trench is clearly visible.

Reverse bias stress experiments are performed by biasing the drain and the trench gate to a given voltage, while the source and the p-substrate are put to ground. At given time intervals, some electrical trench characteristics are measured (V_{th} , transconductance g_m , leakage current I_{cak} , etc.). In addition, charge pumping experiments are performed by putting the source, drain and bulk at ground while pulsing the trench poly. The charge pumping current I_{cp} is measured at the back-side of the wafer. The pulse width is $50\text{ }\mu\text{s}$, the pulse rise and fall times are $10\text{ }\mu\text{s}$. The pulse height V_{pulse} is 16 V , unless otherwise specified. The base voltage V_{base} is swept from -7 to -3 V . The pulse generator used is an Agilent 81101A with a maximum voltage swing of 20 V . All measurements are performed at room temperature.

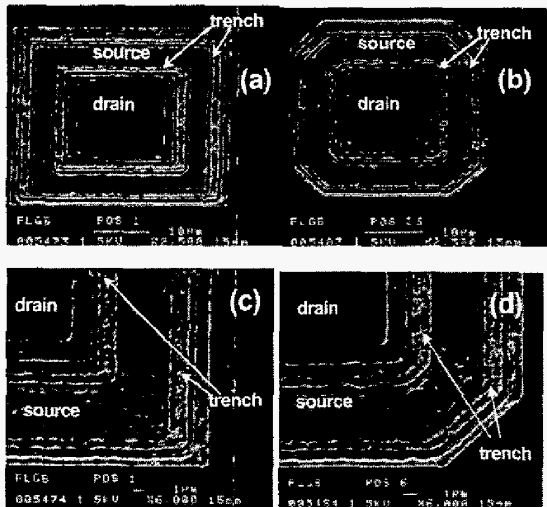


FIGURE 2. : SEM TOP-VIEW OF (A) : STRAIGHT CORNERS STRUCTURE ; (B) : 45° CUT CORNERS STRUCTURE. (C) AND (D) ARE A ZOOM-IN OF FIGURES 2(A) AND 2(B) RESPECTIVELY.

TRENCH OPERATION

Trench isolation structures are designed to withstand a given reverse blocking voltage. For general gate and drain biasing conditions, two different electrical effects can take place : (a) MOS turn-on when the trench gate voltage is larger than V_{th} ; (b) avalanche breakdown when V_{ds} is larger than a given voltage (dependent on V_{gs_trench}) [13]. Fig. 3 clearly shows the two different modes of operation of a trench : a constant current of 10 nA is forced at the drain (inside of the trench) while the trench gate

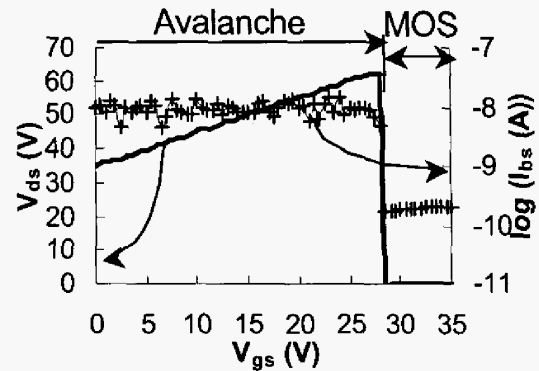


FIGURE 3. : ELECTRICAL BEHAVIOUR OF THE TRENCH WHEN FORCING A CONSTANT CURRENT OF 10 nA WHILE SWEEPING THE GATE. THE DRAIN VOLTAGE IS BEING MONITORED.

is being swept. The source contact is at ground. The drain voltage needed to supply the required 10 nA is monitored. For $V_{gs} < 27\text{ V}$, the structure is in avalanche ($I_{ds}=I_{bs}=10\text{ nA}$). The source current I_{ss} is negligible. For $V_{gs} > 27\text{ V}$, the parasitic MOS transistor turns on, and the I_{ds} is supplied by the source current (outside of the trench) instead of the bulk. As the drain current is no longer supported by the avalanche current I_{bs} , V_{ds} drops to a low voltage ($\sim 1\text{ V}$). The bulk current drops by two orders of magnitude.

CHARGE PUMPING ON TRENCH STRUCTURES

Fig. 4 (a) shows a typical charge pumping characteristic for different V_{pulse} conditions. The charge pumping signal increases with V_{pulse} , but the maximum is clearly not yet achieved. With the used pulse generator, it is not possible to pulse more than 20 V . As a result of this limitation, the total charge pumping signal can not be assessed and so no extraction of N_{it} can be performed. Fig. 4(b) shows the incremental charge pumping spectra, measured as a function of stress time for a trench structure stressed at $V_{gs}=0\text{ V}$ and $V_{ds}=30\text{ V}$ i.e. in

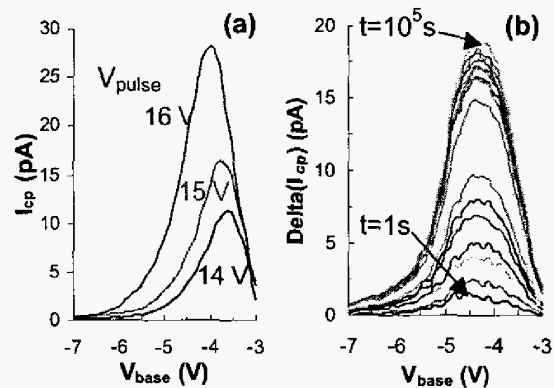


FIGURE 4. : (A) CP SPECTRA MEASURED ON A TRENCH STRUCTURE WITH STRAIGHT CORNERS. V_{PULSE} IS VARIED. $T_{PULSE}=50\text{ }\mu\text{s}$, $T_{FALL}=T_{RISE}=10\text{ }\mu\text{s}$. I_{CP} IS MEASURED AT THE BACKSIDE OF THE WAFER. (B) : INCREMENTAL CP SPECTRA MEASURED DURING STRESS AT $V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$. $V_{PULSE}=16\text{ V}$.

avalanche (see Fig. 3). The charge pumping signal increases monotonously with stress time, and a substantial increase in I_{cp} is observed. Moreover, the initial charge pumping spectrum correlates with the total trench perimeter length (L) and as such is believed to originate from the trench sidewall. This is shown in Fig. 5. It is verified that the observed charge pumping signal is not due to the so-called "geometrical" component which arises from recombination at bulk traps and is typically observed for long-channel devices [15]. The parasitic MOS of the trench structures has a channel length of approximately $10\ \mu\text{m}$. For this channel length, the critical fall time above which the geometrical component is expected to vanish is 100ns . The experimentally used t_{fall} of $10\ \mu\text{s}$ is hence large enough to make sure that the charge pumping signal is not contaminated by the geometrical component.

The fact that not the complete charge pumping signal is measured seriously hampers the extraction of the location of the N_{it} formation along the trench sidewall. However, the falling edge of the variable base charge pumping spectrum is independent of V_{pulse} and is fixed at around -3.5V (see Fig. 4(a)). The falling edge corresponds to $V_{g,h}$ defined as the gate voltage that is required to attract 10^{13} cm^{-3} majority carriers at the interface [14]. The magnitude of $V_{g,h}$ along the trench interface can be calculated from the doping profile (as from TCAD) and the oxide thickness (as from TEM measurements). This is shown in Fig. 6. A measured $V_{g,h}$ of -3.5V originates from

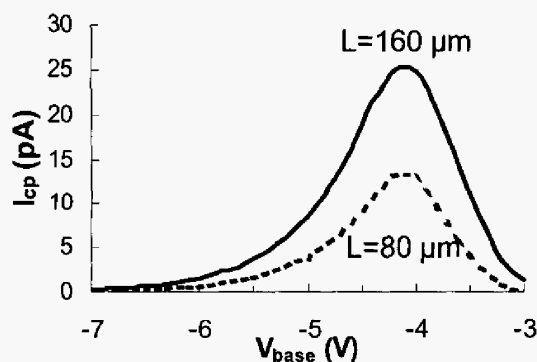


FIGURE 5. : INITIAL CHARGE PUMPING SPECTRA MEASURED ON A TRENCH STRUCTURE WITH STRAIGHT CORNERS WITH DIFFERENT TOTAL TRENCH PERIMETER LENGTH L . $V_{\text{PULSE}}=16\text{V}$.

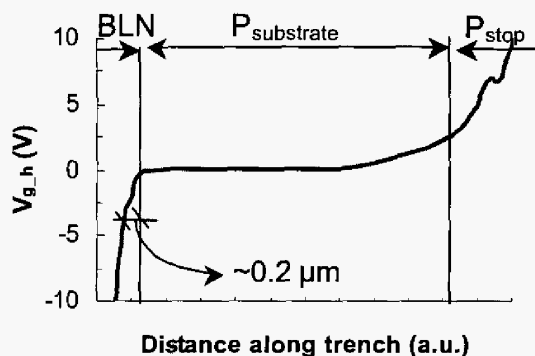


FIGURE 6. : GATE VOLTAGE FOR INDUCING $1e13\text{ cm}^{-3}$ MAJORITY ($V_{g,h}$) CARRIERS ALONG THE TRENCH INTERFACE.

N_{it} approximately $0.2\ \mu\text{m}$ above the BLN/p-substrate junction. N_{it} along the sidewall of the trench in the p-substrate would yield a CP signal with $V_{g,h}\sim 0\text{V}$, N_{it} formation at the bottom of the trench would result in a $V_{g,h}$ in excess of 5V . TCAD simulations indicate that the spot of maximum impact ionization is just above the BLN/p-substrate junction [13], in good agreement with the experimental charge pumping information. Hence it is believed that the charge pumping experiments give valuable information on the amount of N_{it} formation. An important conclusion is that the N_{it} formation occurs in the BLN region, and not in the p-substrate/p-stop region i.e. not in the channel of the parasitic MOS transistor.

RESULTS AND DISCUSSION

Fig. 7 shows the shift in I_{cp} , I_{leak} (measured at $V_{ds}=30\text{V}$, $V_{gs}=0\text{V}$) and V_{th} ($V_{ds}=1\text{V}$, gate is being swept up to 50V) as a function of stress time, for a reverse bias stress at $V_{ds}=30\text{V}$, $V_{gs}=0\text{V}$. I_{cp} and I_{leak} have the same time dependency. The absolute value of I_{leak} decreases as a function of stress time whereas I_{cp} increases upon reverse bias stress (see also Fig. 4(b)). All the parameters of the parasitic MOS transistor (V_{th} , g_m , R_{on}) do not shift upon reverse bias stress, as can be noticed from Fig. 7 for V_{th} . When stressing structures with

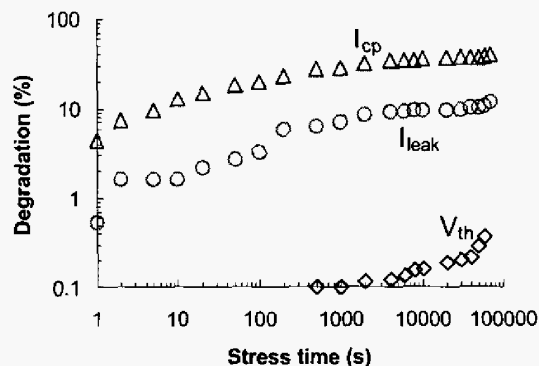


FIGURE 7. : SHIFT IN I_{cp} , I_{leak} (MEASURED AT $V_{gs}=0\text{V}$, $V_{ds}=30\text{V}$) AND V_{th} (MEASURED AT $V_{gs}=50\text{V}$, $V_{ds}=1\text{V}$) AS A FUNCTION OF STRESS TIME. STRESS CONDITIONS : $V_{ds}=30\text{V}$, $V_{gs}=0\text{V}$.

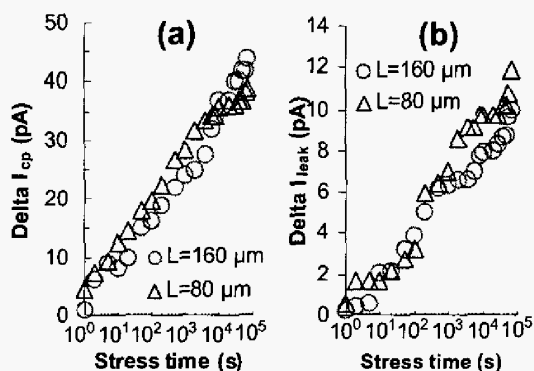


FIGURE 8. : (A) SHIFT IN I_{cp} UPON STRESS TIME ; (B) : SHIFT IN I_{leak} (MEASURED AT $V_{gs}=0\text{V}$, $V_{ds}=30\text{V}$) UPON STRESS TIME. STRESS CONDITIONS : $V_{ds}=30\text{V}$, $V_{gs}=0\text{V}$. THE RESULTS FOR DEVICES WITH DIFFERENT TOTAL TRENCH PERIMETER LENGTH (L) ARE SHOWN. MEASUREMENTS DONE ON STRUCTURES WITH STRAIGHT CORNERS.

different total trench perimeter length L , it is found that the increments in I_{cp} and I_{leak} upon reverse bias stress do not scale with L , although the initial measurements of I_{cp} and I_{leak} do scale with L (see Fig. 5 for scaling of initial I_{cp} with L). The results are shown in Fig. 8. This implies that the degradation originates from the device corners, and not from the trench sidewall. The decrease in leakage current is explained by the N_{it} formation and carrier trapping at the BLN/p-substrate junction upon reverse bias stress. This causes the electric field lines to relax and hence the breakdown of the trench to increase [13]. Avalanche occurs primarily in the trench corners. When the trench structure is measured as a MOS transistor, the complete trench is active and not only the corners. Hence no degradation of the MOS parameters is to be expected, as is indeed confirmed experimentally.

Additional evidence for trench corner degradation comes from reverse bias stress experiments on structures with cut corners (Figs. 1(c) and 2(b), 2(d)). From Fig. 9 it can be observed that both the initial values as well as the increment in I_{cp} are substantially lower compared to structures with straight corners. A similar behavior is observed for I_{leak} . The increase in N_{it} formation upon reverse bias

stress is substantially lower for the cut corner structures compared to the structures with straight corners. This is because the electric field at the corners is relaxed when using cut corners.

Other experimental evidence supporting the hypothesis of trench corner degradation is shown in Fig. 10 in which the source (outside trench) and drain (inside trench) are exchanged. Hence the trench structure is now stressed from the outside instead of the inside (see Fig. 2). Stressing at the inside of the trench results in much higher degradation of both I_{cp} and I_{leak} compared to stressing the outside of the trench. The electric field is believed to be maximal at the inner side of the trench, mainly due to the dopant pile-up of the Nsinker. Thus a larger degradation is expected for stressing the inside of the trench, in agreement with experimental findings. It seems however that by stressing the outside of the trench, the degradation rate accelerates for longer stress times. This was not observed for stressing the inside of the trench. No explanation for this effect is yet given. More experiments are in progress.

DRAIN AND GATE STRESS VOLTAGE DEPENDENCY

Stressing the trench isolation structures at different V_{ds} voltages for a $V_{gs}=0V$ i.e. in avalanche, results in shifts of I_{leak} as the most degrading electrical parameter. The parameters of the parasitic MOS transistor do not shift upon stress. The leakage current decreases as the impact ionization of the trench structure decreases upon N_{it} formation during reverse bias stress. Hence, in terms of reverse blocking voltage, the trench isolation structure become better during stress. Fig. 11 shows the lifetime extracted for 10% shift (decrease !) in I_{leak} , as a function of V_{ds} . Under avalanche condition, the usual $1/V_{ds}$ relation is observed [16].

Stressing the isolation structures under MOS turn-on conditions i.e. for high gate voltages shows a different picture. If the MOS transistor is on, the most degrading electrical parameters are g_m and R_{on} . G_m decreases upon stress, whereas R_{on} increases. Also the V_{th} decreases slightly (150 mV after 10^4 s of stress). The higher V_{gs} , the more important the degradation in g_m , as is shown in Fig. 12. For the isolation structure, it is especially the lowering of the V_{th} which is important as the other parameters are not degrading the reverse blocking capability of the structure. If the V_{th} would drop seriously upon stress, the risk of MOS turn-on during normal operating of the trench could occur. From the measurements however, the drop in V_{th} is negligible, and so no danger for MOS turn-on is present.

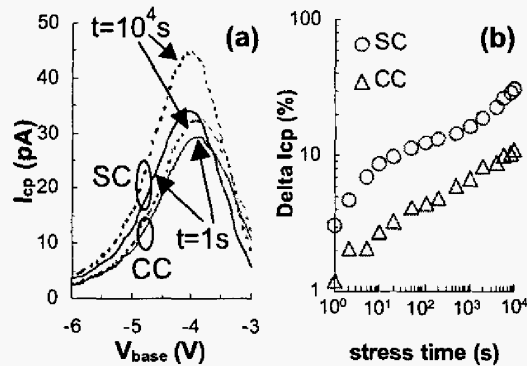


FIGURE 9 : (A) EFFECT OF TRENCH CORNERS ON THE CHARGE PUMPING SIGNAL (SC=STRAIGHT CORNERS, SEE FIG. 1 (b), CC=CUT CORNERS, SEE FIG 1 (c)). (B) : INCREASE IN I_{cp} AS A FUNCTION OF STRESS TIME (STRESSED AT $V_{ds}=30V$, $V_{gs}=0V$).

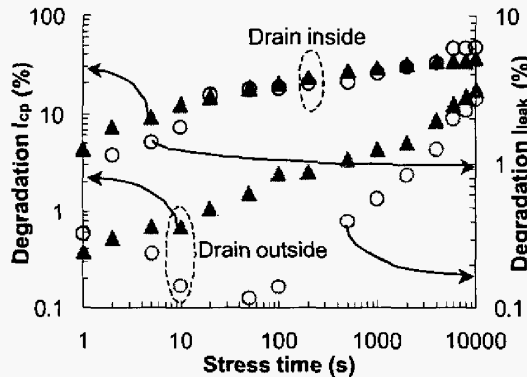


FIGURE 10 : EFFECT OF EXCHANGING SOURCE AND DRAIN (I.E. STRESSING THE INSIDE OR THE OUTSIDE OF THE TRENCH) ON THE DEGRADATION. STRESS CONDITIONS : $V_{ds}=30V$, $V_{gs}=0V$. MEASUREMENTS DONE ON STRUCTURES WITH STRAIGHT CORNERS.

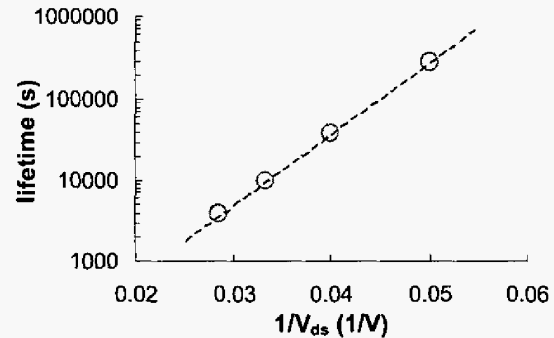


FIGURE 11 : LIFETIME EXTRACTED AT DIFFERENT V_{ds} STRESS CONDITIONS. CRITERION IS 10% IN I_{leak} . $V_{gs}=0V$. MEASURED ON STRAIGHT CORNER STRUCTURES.

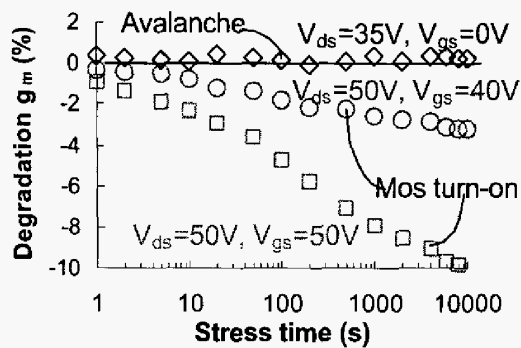


FIGURE 12. : DEGRADATION OF G_m UNDER AVALANCHE CONDITIONS ($V_{ds}=35V$; $V_{gs}=0V$), AND UNDER MOS TURN-ON CONDITIONS ($V_{ds}=50V$; $V_{gs}=40V$ AND $V_{ds}=50V$; $V_{gs}=50V$). MEASURED ON STRAIGHT CORNERS.

CONCLUSIONS

It is demonstrated that the degradation of trench isolation structures upon reverse bias stress with contacted gate is primarily due to N_H formation at the inner trench corners. The leakage current of the trench structure decreases upon reverse bias stress. Using cut corners drastically improves the reliability of the isolation structures. The V_{th} of the parasitic MOS transistor is not shifting during stress. This is because the parasitic MOS is mainly determined by the total trench perimeter and not only by the corners, and the N_H formation is in the BLN region being outside the channel area of the MOS. When stressing under MOS turn-on conditions, g_m becomes the most degrading electrical parameter. The drop in V_{th} is small. Thus there is no risk for MOS turn-on during normal operation of the trench structure.

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