

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case IPR2024-01403
U.S. Patent No. 7,772,673

**DECLARATION OF DR. SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 7,772,673**

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I, Dr. Scott E. Thompson, Ph.D., declare that:

I. INTRODUCTION

1. I, Scott E. Thompson, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”) in connection with an *inter partes* review (IPR) of U.S. Patent No. 7,772,673 (“the ’673 Patent”) (Ex. 1001). I have prepared this declaration in connection with Samsung’s Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1-17 of the ’673 Patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’673 Patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-17 of the ’673 Patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of March 16, 2007), it is my opinion that claims 1-17 of the ’673 patent would have been anticipated and/or obvious based on the grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '673 patent and the related prior art.

8. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of semiconductor devices.

9. I received a Ph.D. degree in Electrical Engineering from the University of Florida in 1992. Before that, I received a Master of Science degree in 1988 and a Bachelor of Electrical Engineering with Highest Honors in 1987, both from the University of Florida.

10. I was employed at Intel Corporation ("Intel") from 1992 to 2004. During that time, I worked on evaluating, implementing, and ramping into high-volume production new materials, process architectures, and transistor structures. I

was the yield manager and overall program manager for Intel's 90 nanometer (nm) process. In my role as program manager, I managed both deep and shallow trench isolation, junction capacitance and partially and fully depleted SOI transistor evaluations. For trench isolation, I managed trench etch, trench fill and minimum allowed isolation space between devices.

11. I played a key role at Intel in the development of a form of strained silicon using silicon germanium ("SiGe") implemented in the source and drain regions of p-type field effect transistors ("pFETs"). SiGe/Strained Silicon is now a nearly universal technology that speeds up transistors and hence all types of integrated circuits.

12. Working at Intel, I announced this integrated circuit technology to the industry in 2002. I managed a team of about 100 engineers that developed and implemented this technology in transistors that went into high-volume manufacturing in 2003 as part of Intel's 90 nm process. My team was responsible for fabricating, ramping into production, and transferring this transistor technology to Intel's design and fabrication sites worldwide. This transistor technology has been used by Intel for its entire microprocessor product line since the 90 nm process, including its 7th generation of SiGe/Strained Silicon. Within a few years after 2002, every advanced computer chip manufacturer was using SiGe/Strained Silicon technology.

13. My work on transistors helped me earn an Institute of Electrical and Electronics Engineers (IEEE) Fellow rank (awarded in 2006), along with numerous industry awards for our Intel development team. In 2008, I and key members of the Intel SiGe/Strained Silicon development team were awarded the SEMI AWARD NORTH AMERICA for “Process Integration of Strain-enhanced Mobility Techniques for CMOS Transistors.” This award is the highest honor achievable through SEMI, a 2,000-member trade organization.

14. In 2007, my Intel colleague Mark Bohr described my role and how Intel came to invent new technologies for transistors, including isolated transistors. At Intel, I worked on several generations of Intel’s planar transistors, each of which implemented SiGe/Strained Silicon technology after 2002.

15. I have given talks and organized and taught international courses on transistor technology, including electrically isolated transistors. For example, I was asked to give a lecture on strained silicon at the 2006 International Electron Devices Meeting.

16. I have also developed and taught graduate level courses on SiGe/Strained Silicon technology at the University of Florida, including a course entitled “EEE500: Future of Nano/Micro Electronics.”

17. As a professor at the University of Florida, I have been awarded over \$4 million in research funding largely directed towards understanding the

scalability of transistors. I have received research funding from the National Science Foundation, Semiconductor Research Corporation, and other agencies. I currently have a research contract to investigate strain in bipolar transistors (a type of transistor based on a different principle of operation than planar FETs or FinFETs).

18. As a result of my industry work, I am familiar with various areas of advanced computer chip technology. I have worked extensively on the use of shallow trench isolation (“STI”) in manufacturing processors, novel low resistance source and drain regions, silicides (titanium, cobalt, and nickel silicide), and low resistance tungsten plugs. Throughout 1991-2004, I was part of the Intel development team that introduced titanium, cobalt and nickel silicide into the production of high-performance microprocessors. My work experience has also extended to layout design rules, oxide and nitride spacer formation, gate and fin patterning, gate oxides, gate electrodes, contacts, silicide, copper interconnects, process integration (lithography, etch, diffusion, thin film deposition, and chemical mechanical polishing), and yield and reliability.

19. I also co-founded a low power transistor technology company called SuVolta in 2009 that developed transistors that could operate at ultra-low power for internet-of-things applications. SuVolta’s intellectual property was sold to Fujitsu and included patents on both planar transistors and transistors that could

operate at ultra-low power.

20. As the co-founder and Chief Technology Officer of SuVolta, and as an inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

21. I am a named inventor on over 100 granted United States patents and have authored over 60 peer-reviewed academic journal publications. I have co-authored a book on semiconductor devices titled *Strain Effects in Semiconductors: Theory and Device Applications* (2009). I have patents and publications on semiconductor technology, trench isolation, and transistors, all of which are relevant technologies in this case. A few examples relevant to this case are:

- My work on silicon semiconductor technology is described in the frequently cited IEEE peer-reviewed paper S. Thompson, et al., *A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell*, Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002).

- My work on trench isolation is described in a 1998 paper published in the Intel Technology Journal: A. Brand et al., *Intel's 0.25 Micron, 2.0 Volts Logic Process Technology*, *Intel Technology Journal*, Q3 (1998).

- My work on transistors is described in, for example, the paper S. Suthram et al., *Understanding Strain Effects on Double-Gate FinFET Drive-Current Enhancement, Hot-Carrier Reliability and*

Ring-Oscillator Delay Performance via Uniaxial Wafer Bending Experiments, 2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 163- 164 (2008).

22. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is, as noted above, attached to this report as Appendix A.

IV. MATERIALS CONSIDERED

23. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,772,673 to Yin et al. (“’673 Patent”)
Ex. 1002	Prosecution History of the ’673 Patent (downloaded from the USPTO’s Patent Center Website) (“’673 Patent File Wrapper”)
Ex. 1004	U.S. Patent No. 6,995,449 to Yin et al. (“ <i>Yin</i> ”)
Ex. 1005	U.S. Patent Publication No. 2005/0181569 to Koshimizu et al. (“ <i>Koshimizu</i> ”)
Ex. 1006	U.S. Patent No. 6,121,102 to Norström et al. (“ <i>Norström</i> ”).
Ex. 1007	Stanley Wolf, PH.D., SILICON PROCESSING FOR THE VLSI ERA, VOLUME 2: PROCESS INTEGRATION (1990) (“WOLF”)
Ex. 1008	U.S. Patent No. 6,362,040 to Tews et al. (“ <i>Tews</i> ”)

Exhibit	Description
Ex. 1009	P. Moens et al, <i>Reliability Assessment of Deep Trench Isolation Structures</i> , IEEE 43 rd Annual Int. Rel. Phys. Symp., (2005) (“ <i>Moens</i> ”)
Ex. 1010	Stiffler et al., <i>The Effect of Trench Corner Shapes on Local Stress Fields</i> , 40 IEEE TRANSACTIONS ON ELECTRONIC DEVICES 3, (1993) (“ <i>Stiffler</i> ”)
Ex. 1011	U.S. Patent No. 5,104,816 to Verret et al. (“ <i>Verret</i> ”)
Ex. 1012	Peter Shepherd, INTEGRATED CIRCUIT DESIGN, FABRICATION AND TEST (1996) (“ <i>SHEPHERD</i> ”)
Ex. 1013	James M. Murduck, Fabrication of Superconducting Devices and Circuits, FRONTIERS OF THIN FILM TECHNOLOGY, Vol. 28 (2001) (“ <i>MURDUCK</i> ”)
Ex. 1014	J.P. Patent No. 3,141,621 to Matsuzaki et al. (“ <i>Matsuzaki (JP)</i> ”)
Ex. 1015	Certified English Translation of J.P. Patent No. 3,141,621 to Matsuzaki et al. (“ <i>Matsuzaki</i> ”)

V. LEGAL STANDARDS

24. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

25. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a

claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

26. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

27. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-17 of the '673 Patent from the perspective of a person of ordinary skill in the art at the '673 Patent's earliest claimed priority date of March 16, 2007, as described in more detail below.

28. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

29. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

30. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the

art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

31. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

32. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

33. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing

date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

34. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

35. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject

matter in the '673 patent.

36. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is March 16, 2007. My opinions would not change if I assumed a later date of invention.

37. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

38. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds

cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

39. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

40. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

41. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every

claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

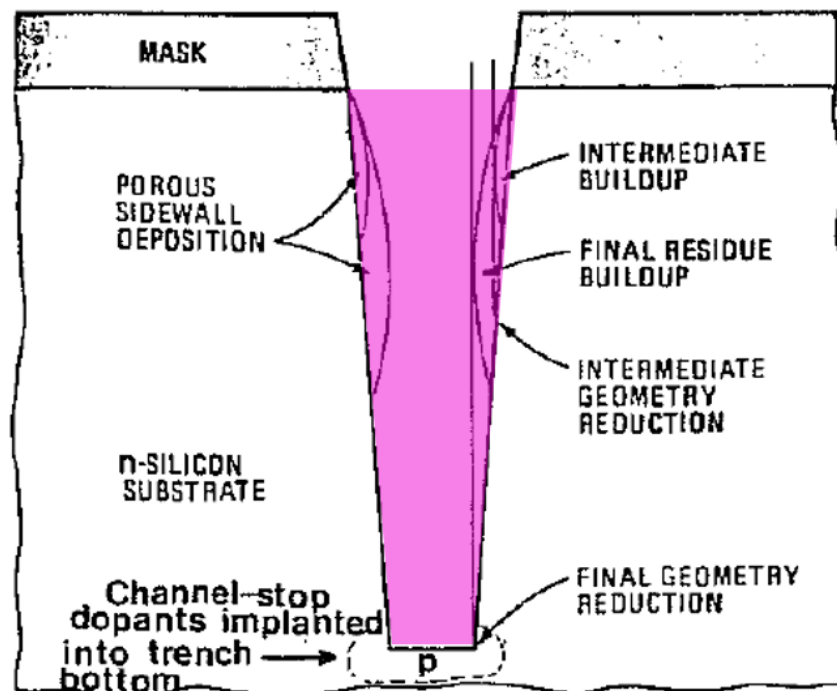
42. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

43. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND

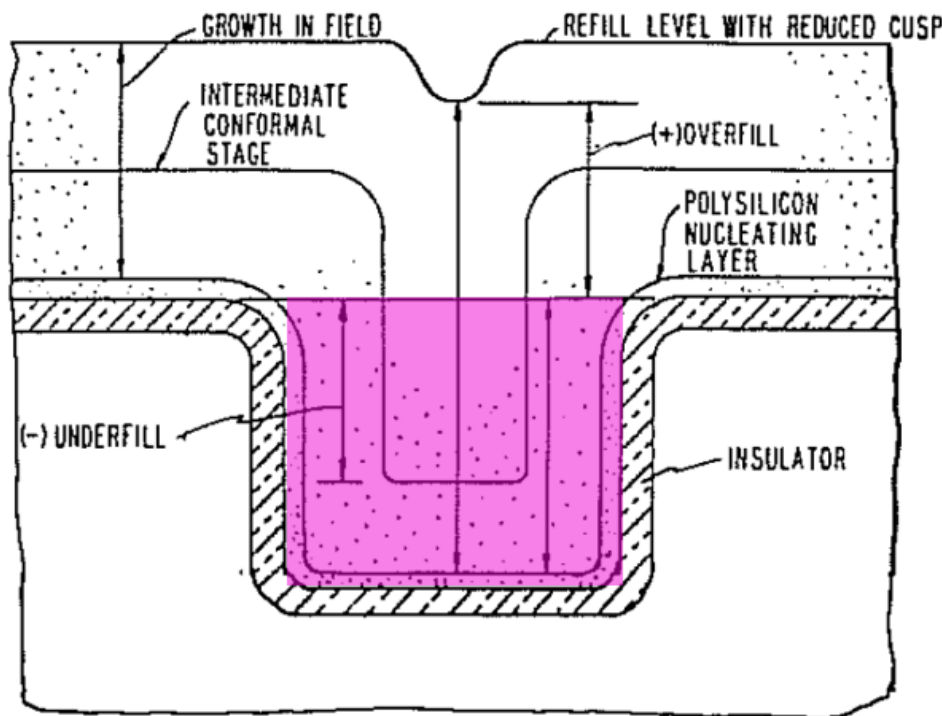
A. Deep Isolation Trenches

44. Deep trenches filled with polysilicon or other isolating materials have been used to electrically isolate semiconductor devices such as bipolar transistors for years. *See WOLF (Ex. 1007), 51-58.* The semiconductor devices upon which these trenches are dug are typically very small—being measured in micrometers well before the priority date of the '673 Patent. *See WOLF, 55.* As such, the trenches are etched *chemically* rather than physically into the substrate of the semiconductor die using a “mask” that outlines where the trench will go—and this mask prevents the corrosive chemicals from digging into the rest of the semiconductor die. *See WOLF, 51-58.*



WOLF, Fig. 2-37 (annotation added).

45. After being etched, these trenches are then refilled with electrically isolating material to protect the semiconductor device inside from electrical interference by neighboring semiconductors. *See* WOLF, § 2.6.3.2. Many materials can be used, and as early as 1990, in “trench-isolation structures, atmospheric-CVD polysilicon, LPCVD polysilicon, CVD SiO₂, and selective, epitaxially-grown (SEG) silicon [had] reportedly been used.” WOLF, 56. This refill process “proceeds by means of a conformal covering of the trench surfaces and the original substrate surface,” whereby the isolating material is gradually deposited along the sides and bottom of the trench until it is refilled:



WOLF at 55-57, Fig. 2-40(a) (annotation added). The thickness of polysilicon

required to fill a trench will scale with the width of a trench, and it was well known more than a decade before the '673 Patent that “[f] trenches of widely varying widths are filled, the narrow ones must be well overfilled in order for the wider ones to be filled completely.” WOLF, 56.

B. Semiconductor Devices

46. The '673 Patent also uses phrases like “semiconductor die” and “semiconductor package” *See, e.g.*, '673 Patent, Abstract, 9:10-18. The '673 Patent states that a POSITA at the time of the patent would have been familiar with both semiconductor dies and packages:

“It is understood to those of ordinary skill in the art that although the invention has been described in reference to a “wafer,” such wafer can be diced and singulated into individual dies and thereafter packaged using various semiconductor packaging techniques and processes. As such, the invention is manifestly applicable to fabricating wafers and/or dies, which may or may not be later packaged, in accordance with the teachings of the invention as described above.”

'673 Patent, 9:10-18. This is consistent with my own opinion and experience, which is that the use of semiconductor devices in dies, wafers, and packages was extremely common before the '673 Patent (*i.e.*, before March 16, 2007).

47. As Shepherd explains in his 1996 textbook, before “individual circuits on the wafer (die) are packaged, the circuit must be tested by probing the pads, in

order to identify any circuits that are faulty owing to random fabrication defects.

These are identified by placing an ink blob on them. The wafer is then diced up, and each individual die is mounted, bonded and packaged.” SHEPHERD (Ex. 1012),

5. In other words, a “semiconductor die” is simply a wafer of semiconductor material such as silicon, and a “semiconductor package” is the physical package in which an integrated circuit is stored. A semiconductor die houses the transistors, such as bipolar junction transistors, that make up the computer logic of the integrated circuit. SHEPHERD, 1.

48. Integrated circuits, also known as “computer chips” or “chips” had their beginnings “in the early 1960s and, over the intervening years, ha[ve] seen a massive increase in the complexity of circuit, the number of chips produced, the speed of the circuits and the different applications to which they are put.”

SHEPHERD, x. From the 1960s to before the ’673 Patent, computer chips and the semiconductor wafers, dies, and packages that they are built out from became increasingly common, used in everything from personal computers to personal phones. *See, e.g.*, SHEPHERD, 12. Thus, in my opinion, it is indeed correct that a POSITA at the time of the ’673 Patent would have been very familiar with integrated circuits as well as semiconductor wafers, dies, and packages.

VII. THE '673 PATENT

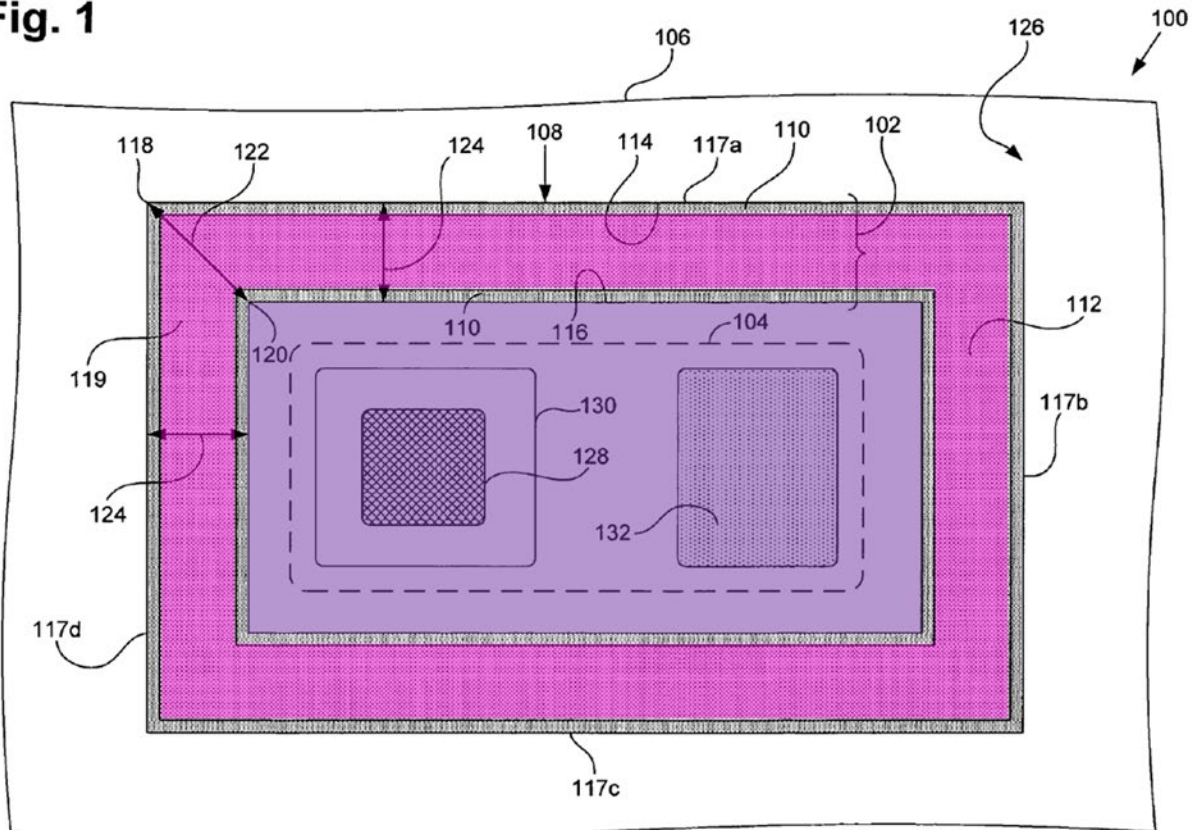
A. Priority Date

49. I note that the '673 Patent was filed on March 16, 2007 without any claim to an earlier priority date. I am not aware at this time of any basis for an assertion of a priority date that would be earlier than March 16, 2007. I understand that the references on which I base my opinions were all prior art as of March 16, 2007.

B. Specification

50. The '673 Patent is directed to “a semiconductor die including at least one deep trench isolation region for isolating an electronic device (for example, a bipolar device)[.]” ('673 Patent, Abstract). Figure 1 of the '673 Patent depicts a “top view” of what the inventors refer to as a “conventional” semiconductor die with **deep trench isolation region 102** isolating an electronic device such as a **bipolar transistor 104**:

Fig. 1

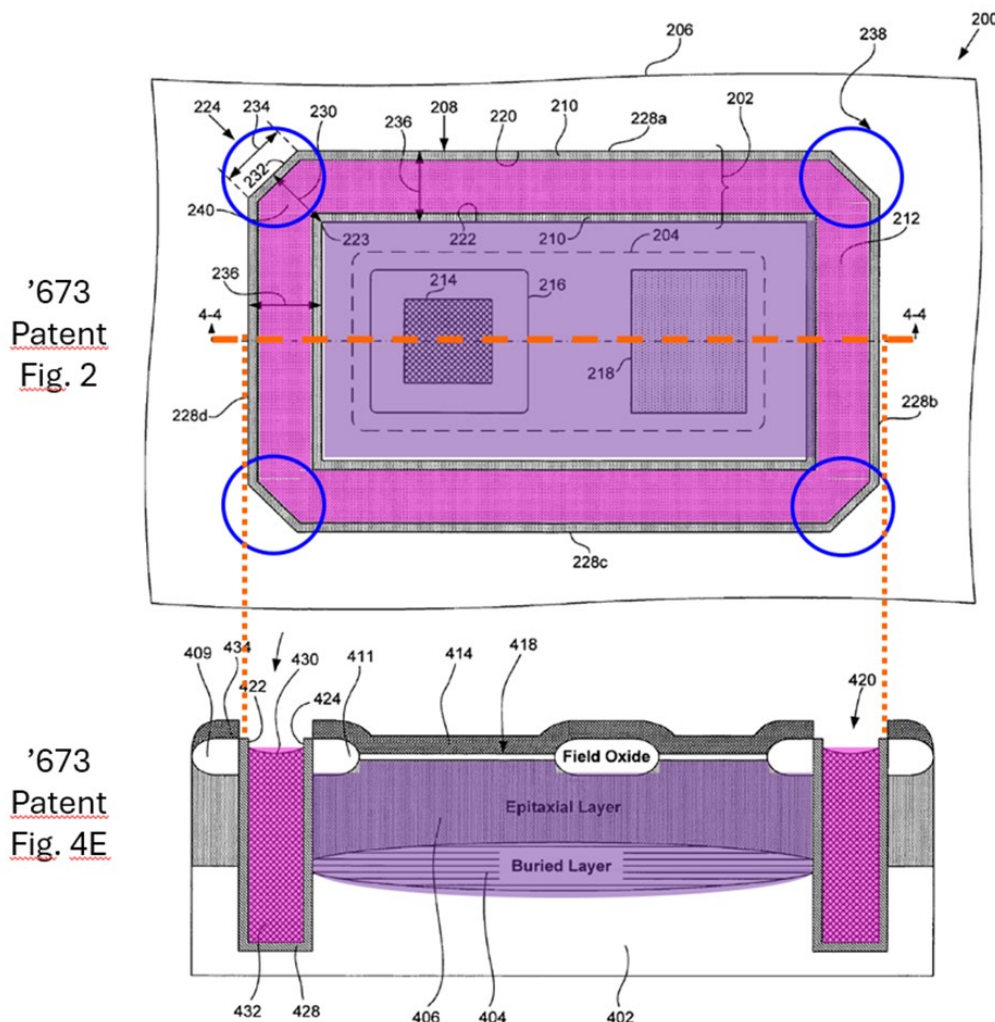


'673 Patent, Fig. 1 (annotation added); 2:35-3:50. The '673 Patent states that the conventional “[t]rench **108** has trench corner width **122**, which represents the perpendicular distance, i.e., the minimum distance, [sic] between corners **118** of outside wall **114** and corners **120** of inside wall **116**[.]” ’673 Patent, 3:12-15. As shown in this figure, the '673 Patent’s “conventional” semiconductor die has a **deep trench isolation region** with corners that form right angles (i.e., 90° angles) between connecting sides. ’673 Patent,

Fig. 1.

51. Figure 2 of the '673 Patent then depicts a birds-eye view of its claimed semiconductor die containing a **bipolar transistor** surrounded by a **deep**

isolation trench with chamfered outer corners. See '673 Patent, Fig. 2. The cut-away marker 4-4 in Figure 2 links to the side-cut view shown in Figure 4:



See '673 Patent, Figs. 2 (top), 4E (bottom) (both annotations added). The '673 Patent states that “a **bipolar device (i.e. a bipolar transistor)** is utilized as an example of an electronic device” to be isolated by the **deep trench isolation region**, and that “[b]ipolar device 204 is isolated by [the] **deep trench isolation region 202** from surrounding bipolar devices situated on substrate 206.” '673 Patent, 3:51-54; 4:17-19.

52. Regarding the **chamfered corners**, the '673 Patent explains that there are benefits to **chamfering the outside corners** of the **deep isolation trench**.

Specifically, it states that:

[B]y forming **trench chamfered corners 240** to reduce the trench corner width to approximately 0.9 microns compared to a trench corner width of approximately 1.4 microns for conventional **trench 108**, an embodiment of the present invention advantageously reduces the deposited polysilicon layer thickness from approximately 1.5 microns to approximately 0.7 microns.

'673 Patent, 5:15-21. Thus, by reducing the width of the trench at its otherwise-widest spots—i.e., its corners—by using a **chamfer**, the '673 Patent seeks to improve the polysilicon refilling process and reduce the overall amount of polysilicon needed to fill the entire **trench**. The '673 Patent claims that “[s]ince deposited polysilicon layer thickness is reduced by approximately one half, the present embodiment can increase polysilicon fill process throughput for **trench 208** by approximately 100 percent compared to the polysilicon fill process throughput for conventional **trench 108** in FIG 1.” '673 Patent, 5:21-26.

53. As I will explain in more detail below, chamfers on deep isolation trenches were not new at the time of the '673 Patent. In my opinion, the challenged claims of the '673 Patent would have been obvious to a POSITA in view of prior art.

C. Prosecution History

54. I understand that during prosecution of the '673 Patent, the Examiner rejected all claims, finding that the prior art either anticipated or rendered obvious all claims over the application's admitted prior art as well as a reference to *Kitaguro*. '673 Patent File Wrapper (Ex. 1002), 42-53.

55. I understand that for anticipation, the Examiner found original claims 1-3, 7-8, 21-23, and 26-27 anticipated by U.S. Patent No. 6,107,161 to *Kitaguro et al.* '673 Patent File Wrapper, 45-47.

56. I understand that for obviousness, the Examiner found original claims 6, 9, and 28 obvious over *Kitaguro* in view of the level of skill in the art (i.e., single-reference obviousness). '673 Patent File Wrapper, 48-49. The Examiner also found claims 1-9 and 21-28 obvious over the Applicant's admitted prior art (i.e., Figure 1 and accompanying disclosures) in view of U.S. Patent No. 5,933,749 to *Lee et al.*

57. I understand that, in response, the Applicant argued that nothing in the prior art discloses a trench chamfered corner that causes a reduction in thickness of a layer of polysilicon within the trench. '673 Patent File Wrapper, 29-38. The Applicant specifically argued that *Kitaguro* did not employ "chamfered" corners, but a "circular arc shape." '673 Patent File Wrapper, 31. The Applicant also argued that *Lee*'s chamfer was not along the corner of the trench, but along its vertical

inner walls—and that this kind of chamfering “cannot reduce the thickness of a material that may be situated within [it].” ’673 Patent File Wrapper, 31-34.

58. I understand that the Examiner was not aware of *Yin*, *Koshimizu*, or *Norström*, the prior art I address below, when the claims were allowed. In my opinion, *Koshimizu* and *Norström* disclose the chamfered outer corner the Applicant argued was not in the prior art.

D. Claim Construction

59. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent. I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent’s written description, the patent’s prosecution history, or both.

60. I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have

been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a POSITA in the relevant time period.

61. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '673 Patent.

62. I understand that no claim term's construction is in dispute at this time. Based on my review of these materials and my personal knowledge and experience, I have considered each term of the '673 Patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of March 16, 2007.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

63. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a person of ordinary skill in the art ("POSITA") at the time of the alleged invention, which I understand to be no earlier than Mar. 16, 2007. *See* '673 Patent, 1 (filing date). I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the

sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

64. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '673 Patent (Mar. 16, 2007) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and vice versa.

65. I had at least this level of skill in the art on or before Mar. 16, 2007.

IX. SUMMARY OF THE PRIOR ART

66. General descriptions provided for the following references and combinations thereof are incorporated into each subsection and my mapping of the claims that includes citations to these references.

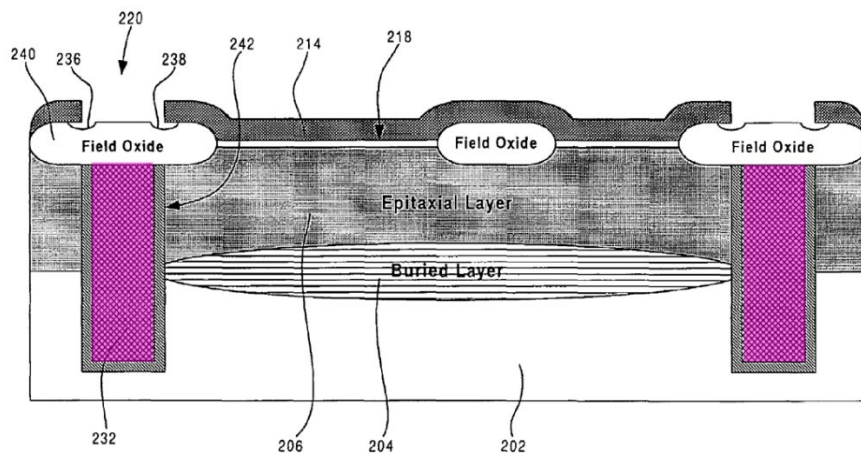
A. *Yin* (Ex. 1004)

67. I understand *Yin* (Ex. 1004) issued and published as U.S. Patent No. 6,995,449 on February 7, 2006. It discloses a semiconductor die with a **deep isolation trench** having the same features as the '673 Patent—except for a

chamfered outer trench corner. *Compare Yin*, Abstract with '673 Patent, Abstract.

Both *Yin* and the '673 Patent share much of their disclosure and figures because *Yin*'s two co-inventors—Kevin Yin and Amol Kalburge—are also named inventors of the '673 Patent. Yet *Yin* was not disclosed to the patent office during the prosecution of the '673 Patent.

68. Like the '673 Patent, Yin discloses a semiconductor die having an electronic device isolated by a **deep isolation trench** surrounding it:



Yin, Fig. 2G (annotation added). In Figure 2G, **220** represents the **trench** that comprises *Yin*'s “**deep trench isolation region** [which] may electrically isolate, for example, a **bipolar transistor**, . . . from an adjacent CMOS transistor, such as a PFET, fabricated on the same semiconductor substrate.” *Yin*, 1:19-24 (annotation added); *see also* '673 Patent, 1:17-20 (“A **deep trench isolation region** may also electrically isolate a **bipolar transistor** (i.e. a **bipolar device**) from adjacent bipolar transistors fabricated on the same semiconductor substrate.”).

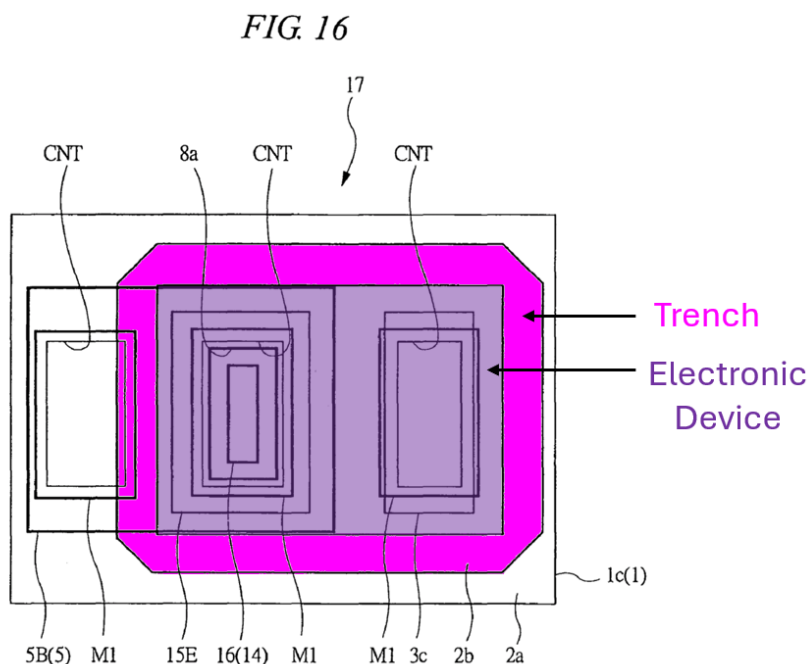
69. Like the '673 Patent, *Yin* further discloses that its deep trench isolation region is refilled with polysilicon. *See Yin*, 1:47-59; 6:29-53 (“[A] layer of polysilicon is conformally deposited over substrate 202 and etched in an etch back process . . . as a result of the conformal polysilicon deposition process, deposited polysilicon fills **trench 220**.”); *see also* '673 Patent, 8:11-14 (“[A] layer of polysilicon is conformally deposited over substrate **402** to fill **trench 420** and etched in an etch back process.”).

70. In my opinion, *Yin* is analogous art to the '673 Patent because *Yin*, like the '673 Patent, is directed to a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor. *Compare Yin*, Field of Invention (“The present invention relates to the field of fabrication of semiconductor devices. More specifically, the invention relates to forming isolation regions in semiconductor substrates.”); *with* '673 Patent, Field of Invention (“The present invention is generally in the field of semiconductor fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor substrates.”).

B. *Koshimizu* (Ex. 1005)

71. I understand *Koshimizu* (Ex. 1005) published as U.S. Patent Application Publication No. 2005/0181569 on August 18, 2005. It also discloses a semiconductor die with a **deep trench isolation region**. In particular, *Koshimizu*

discloses a “hetero-junction **bipolar transistor**” with a “manufacturing method for the semiconductor device.” *Koshimizu*, [0001]-[0006]. *Koshimizu*’s **bipolar transistor** is based in doped silicon and surrounded with a **deep isolation trench** as in *Yin* and the ’673 Patent. See *Koshimizu* at [0051]-[0061]; Figs. 15-16. Figure 16, which I have annotated below, shows a birds-eye view of *Koshimizu*’s semiconductor device:

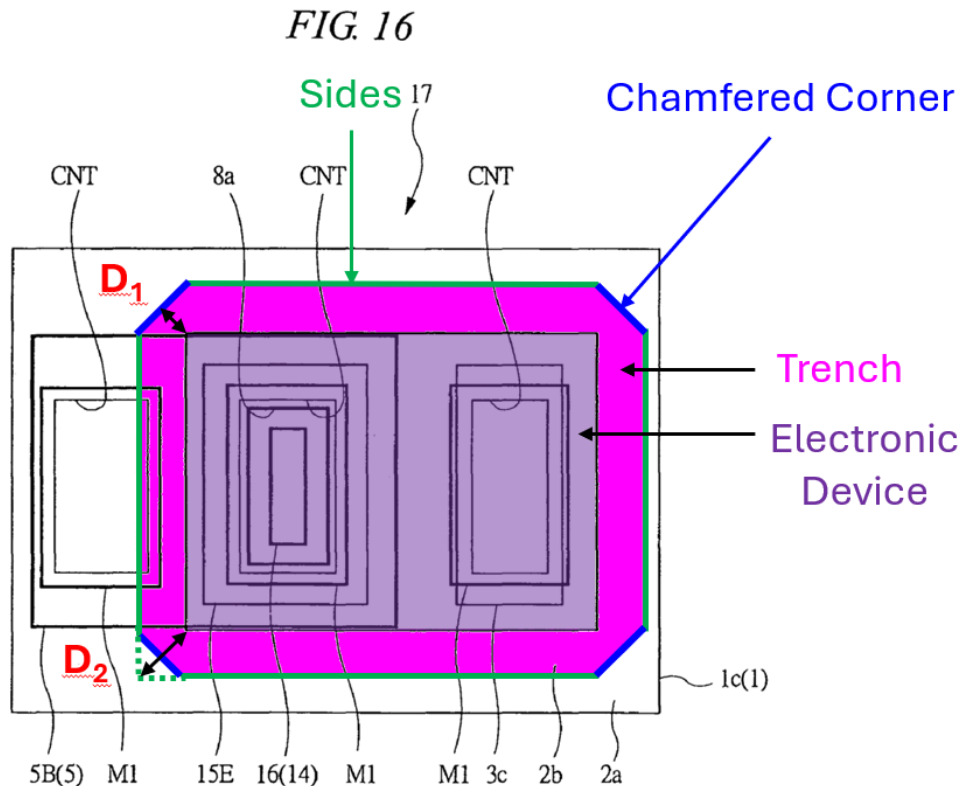


Koshimizu, Fig. 16 (annotation added).

72. In Figure 16, **2b** is a **deep isolation trench** electrically isolating *Koshimizu*’s **bipolar junction transistor**. *Koshimizu*, Fig. 16; [0052] (“By this **deep trench isolation 2b**, each **device region** in the semiconductor layer **1c** is

completely separated electrically.”) (annotation added). *Koshimizu* fills its deep trench isolation region with a “silicon oxide film.” *Koshimizu*, [0052]-[0053].

73. Below is Figure 16 of *Koshimizu* once again, this time with the **four sides** of the **trench** and its **chamfered outer corners** annotated as well:



Koshimizu, Fig. 16 (annotation added). As shown, the chamfered outer corners result in a narrower or thinner trench at the corners *without* a chamfer – or, in other words, **D₁** is narrower than **D₂**. See *Koshimizu*, Fig. 16 (annotation added).

74. In my opinion, *Koshimizu* is analogous art to the '673 Patent because, like the '673 Patent, it is directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from

neighboring transistors. *See, e.g., Koshimizu*, [0052]-[0053]; '673 Patent, Field of Invention.

C. *Norström* (Ex. 1006)

75. I understand *Norström* (Ex. 1006) issued and published as U.S. Patent No. 6,121,102 on September 19, 2000. It is directed to “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.” *Norström*, 1:7-10 (annotation added). Figure 13c shows a birds eye view of one of *Norström*'s disclosed semiconductor devices:

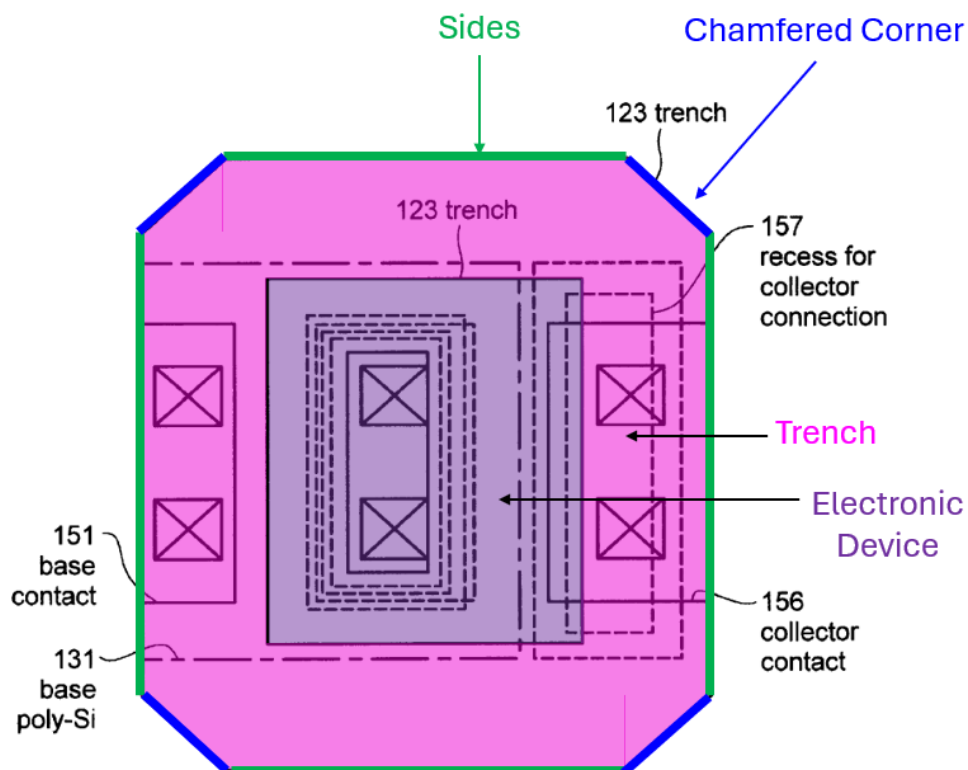


FIG. 13c

Norström, Fig. 13c (annotation added). As shown above, Norström's **trench 123** electrically isolates its **bipolar transistor** contained inside. Norström, Figs. 13a, c. The **four sides** of Norström's **trench** also give way to **chamfered outside corners**. Norström, Fig. 13c.

76. Figure 13a shows a cutaway view of this same **bipolar transistor** surrounded by an **isolating trench**:

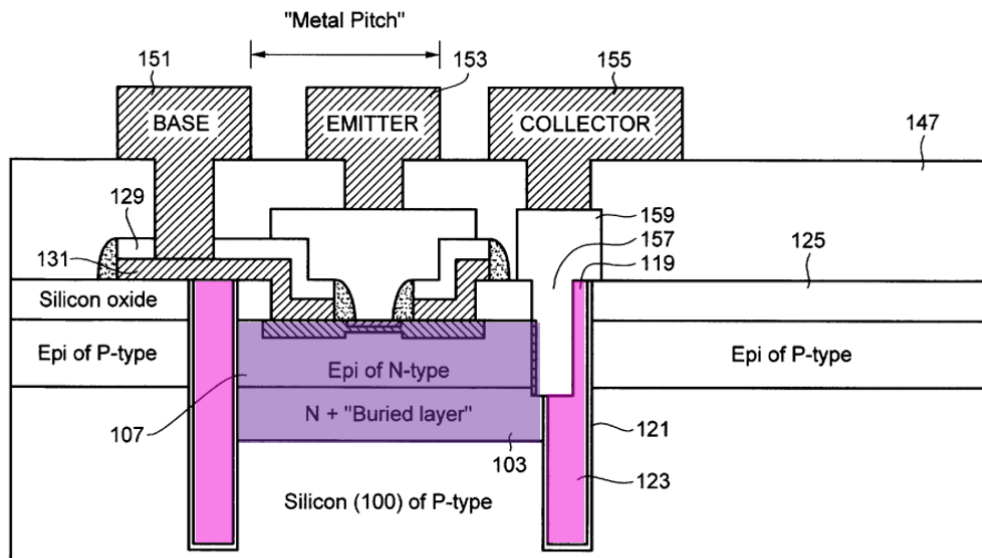


FIG. 13a

Norström, Fig. 13a (annotation added). Norström explains that the **bipolar transistor** depicted in Figure 13 is an “NPN-transistor,” with **deep isolation trenches** extending along the sides of the **transistor**. Norström, 6:23-34, 8:50-11:40 (describing the manufacturing process for the same). These **trenches** are refilled with filling **123**, which Norström discloses may be polycrystalline silicon. Norström, 7:47-50 (“the trenches are filled with an isolating or semi-isolating

material **123**, for example, silicon oxide or polycrystalline silicon[.]”).

77. In my opinion, *Norström* is analogous art to the '673 Patent because, like the '673 Patent, it is directed to the manufacture of “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.” *Norström*, 1:7-10; '673 Patent, Field of Invention.

X. GROUNDS OF UNPATENTABILITY

78. In my opinion, the challenged claims are unpatentable based on the following grounds:

Ground	Challenged Claims	Basis	Prior Art
1	1-17	Obviousness	<i>Yin</i> in view of <i>Koshimizu</i>
2	1, 3, 5, 7-8, 10, 12, 14-16	Anticipation	<i>Norström</i>
3	7, 15	Obviousness	<i>Norström</i>

79. I understand that the '673 Patent has two independent claims and 15 dependent claims. Both independent claims (1, 10) are directed to a semiconductor die; the primary difference between the two independent claims is that independent claim 10 requires that the “at least one trench hav[e] **four sides** surrounding [the] electronic device,” whereas independent claim 1 requires only a **plurality** of number of sides. Below, I have included a table illustrating the independent claims.

Claim 1	Claim 10
1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising: a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides; wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.	10. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising: at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides; each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.

See '673 Patent, Claims 1, 10 (annotation added). Given these similarities, my shared analysis for claims 1, 10 and their matching dependents will be provided together in the Sections below. To the extent that a reference requires separate analysis for one claim over the other (such as additional analysis to show four sides for claim 10), I will provide that analysis separately.

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

A. Ground 1: All Challenged Claims Would Have Been Obvious Over Yin in view of Koshimizu

80. In my opinion, a POSITA would have been motivated to add

Koshimizu's chamfered trench corners to *Yin's* deep isolation trench.

The combination of *Yin* and *Koshimizu* amounts to combining prior art elements according to known methods to yield predictable results.

81. *Yin* teaches a semiconductor die with a deep trench isolation region that surrounds and electrically isolates an electronic device such as a bipolar transistor. *See, e.g., Yin*, Abstract; 1:15-27. *Koshimizu* likewise teaches a semiconductor die with a bipolar transistor surrounded by a deep isolating trench. *See, e.g., Koshimizu*, [0051]-[0053].

82. *Yin* does not disclose the geometry of the corners of its deep trench isolation region. Thus, a skilled artisan looking to use *Yin*'s semiconductor die would have looked to other disclosures for a suitable corner geometry. *Koshimizu* provides that geometry, specifically teaching trenches with an unchamfered inner corner and a chamfered outer corner. *See Koshimizu*, Fig. 16, [0028]; *see also id.*, [0051]-[0061] (fully disclosing the manufacturing method and features of the same). *Koshimizu* is just one of many examples of a deep isolation trench with chamfered corners; these were a common feature of deep isolation trenches before the '673 Patent. *See Moens* (Ex. 1009), 573-74; *Tews* (Ex. 1008), Figs. 1, 4; *Norström*, Figs. 13, 25.

83. There are several reasons for this. First, chamfered corners were beneficial because they improved structural stability. *Stiffler* (Ex. 1010), 559-62.

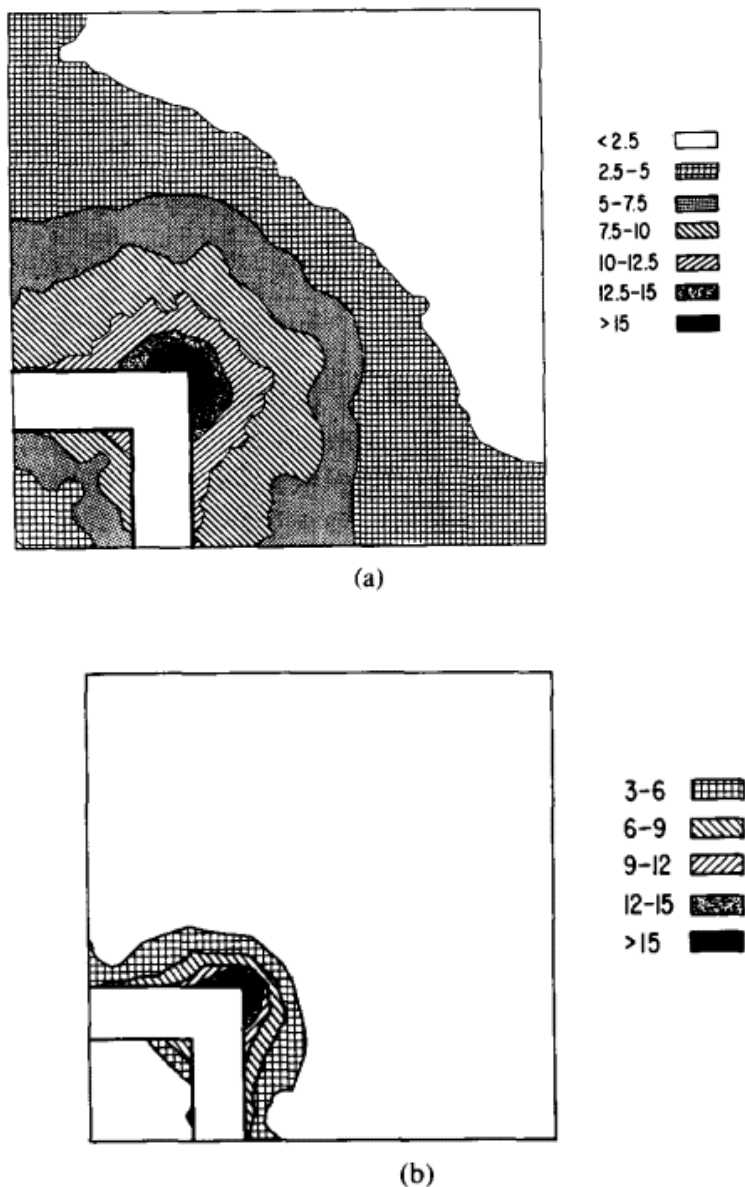
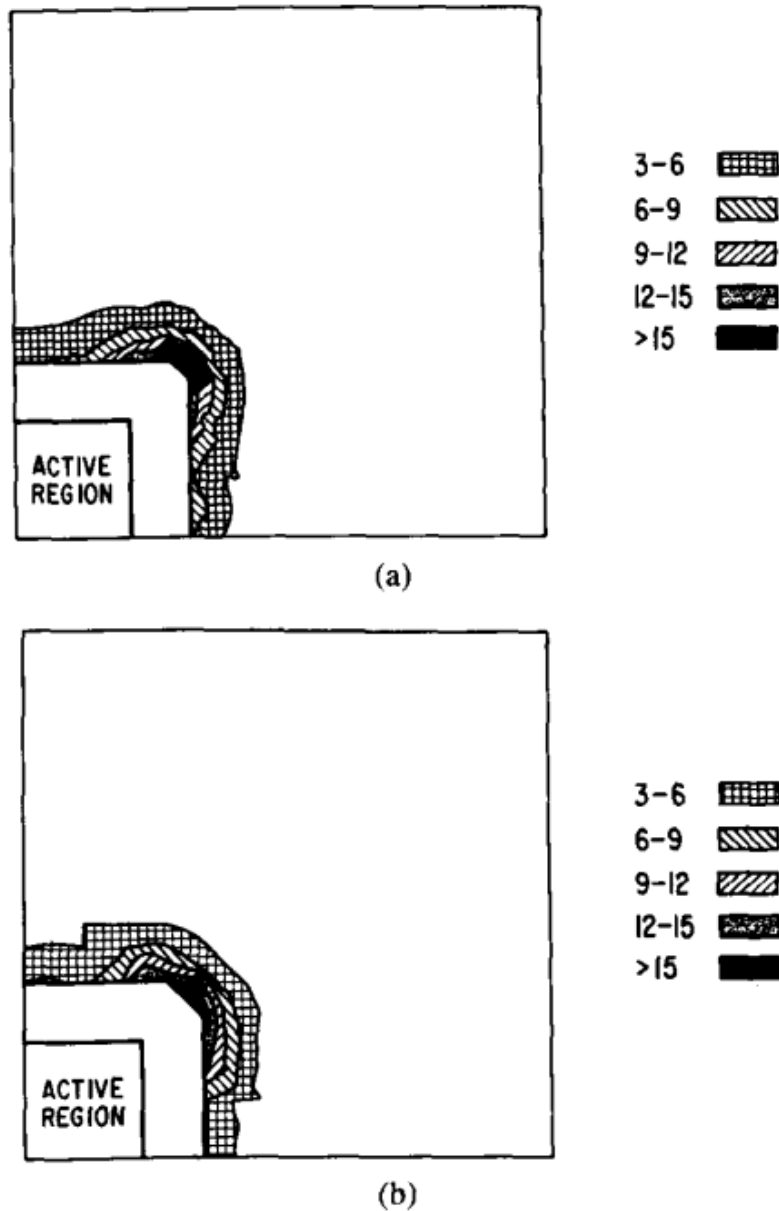


Fig. 4. (a) The Von Mises stress and (b) the elastic energy density on the substrate surface resulting from the temperature excursion discussed in the text. The trench-fill material has been removed for clarity. Contour values are given in units of 10^8 dynes/cm² for the Von Mises stress and in units of 10^5 dynes/cm² for the elastic energy density.

Stiffler, Figs. 4(a), (b). For example, as *Stiffler* explains, in the “base case” of a 90° corner, the Von Mises stress (i.e., the stress that will determine if a given material will yield or fracture) as well as the elastic energy is particularly great around the

sharp corner at the outside of a trench. By comparison, the chamfering of the outer corner can distribute that stress more evenly and disperse it along a larger surface.



See Stiffler, Figs. 6(a), (b).

84. Chamfered corners were also known to reduce the need for overfilling. For example, it was known before the '673 Patent that a deep isolation trench needs to be filled with isolating material such as polysilicon or silicon oxide such that all portions of the trench, including the *widest* portions of the trench, are completely filled. Because the portions of the trench are filled at the same time, this can cause overfill over the narrowest portions of the trench. WOLF, 55-57. It was textbook knowledge before the '673 Patent that “[i]f trenches of widely varying widths are filled, the narrow ones *must be well overfilled* in order for the wider ones to be filled completely.” WOLF, 56 (emphasis added). And chamfered corners normalize the width of the trench’s corners with the width of the trench’s sides, thus minimizing the variance between their widths and the widths of the sides of the trench and reducing the need to overfill the sides of the trench. *See, e.g.; Koshimizu*, Fig. 16.

85. Putting all of this together, it is my opinion that a POSITA would have been motivated to avoid the overfilling of trench sides in *Yin*’s deep isolation trench that would result from unchamfered corners by instead using chamfered corners. And this would also have the added benefit of improved structural stability. *See Stiffler*, 559-62. In my opinion, adding *Koshimizu*’s chamfered corners to *Yin* is therefore nothing more than using a known method (chamfering a

deep isolation trench) that yields a known result (e.g., a reduction in the necessary isolating material in said trench).

The combination of *Yin* and *Koshimizu* involves the use of a known technique to improve similar devices or methods in the same way

86. *Koshimizu*'s device is similar to *Yin*'s. *Yin* is directed to the use of a deep isolation trench filled with polysilicon to electrically isolate an electronic device such as a bipolar transistor. *Yin*, 1:10-27. *Koshimizu* is directed to a semiconductor die using a deep isolation trench filled with silicon dioxide to electrically isolate a bipolar transistor. *Koshimizu*, [0001]-[0006]; [0051]-[0053].

87. While *Koshimizu* uses silicon oxide, (*Koshimizu*, [0051]-[0053]), and *Yin* uses polysilicon, (*Yin*, 6:29-53), to refill their respective isolation trenches, the use of a chamfer on the trench's corners improves *Koshimizu* in the same way it would improve *Yin*. Polysilicon and silicon oxide were textbook alternatives for refilling isolating trenches for more than a decade before the date of the '673 Patent. WOLF, 56 ("In trench-isolation structures, atmospheric-CVD polysilicon, polysilicon, CVD SiO₂, and selective, epitaxially-grown (SEG) silicon have reportedly been used' as early as 1990.").

88. Both polysilicon and silicon dioxide are filled into trenches using the same process of conformal deposition, and both can result in overfilling if one portion of the trench is considerably wider—as unchamfered corners may be—

compared to the rest of the trench. *See* WOLF, 56-57. A POSITA would thus have expected the same benefits that *Koshimizu*'s chamfered corners grant to *Koshimizu*'s trench (e.g., reduced overfilling) would apply to *Yin*'s similar trench in the same way.

A POSITA would have had a reasonable expectation of success in combining *Yin* with *Koshimizu*

89. *Koshimizu*'s chamfered corners could have been easily implemented by a POSITA on *Yin*'s deep isolation trench with a reasonable expectation of success. Chamfering the outer corners of *Yin*'s trench would have required nothing more than an adjustment to the mask pattern that defines the outline of the trench to have chamfered corners instead of square corners. WOLF, 54. It was also known in the art that 135° angle corners (i.e., chamfered), rather than 90° angle corners (i.e., unchamfered) were one solution to improve problems associated with trench refill. *See Norström*, 16:27-36.

Design incentives and other market forces would have motivated the combination.

90. Finally, a POSITA would have been motivated to combine *Yin* with *Koshimizu*'s chamfered trench to reduce the waste associated with overfilling a deep isolation trench. It was desirable before the '673 Patent to improve the refilling process and reduce the overfilling of deep isolation trenches with isolating

materials. *Norström*, 16:27-36; *WOLF*, 55-57. By using *Koshimizu*'s chamfered corners on *Yin*'s deep isolation trench, a POSITA would have advantageously reduced the manufacturing costs associated with making semiconductor devices.

Claim 1[preamble]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”

91. In my opinion, and to the extent the preamble is limiting, *Yin* discloses a **semiconductor die** including at least one **deep trench isolation region** for isolating an **electronic device**. Annotated Fig. 2G from *Yin* is shown below:

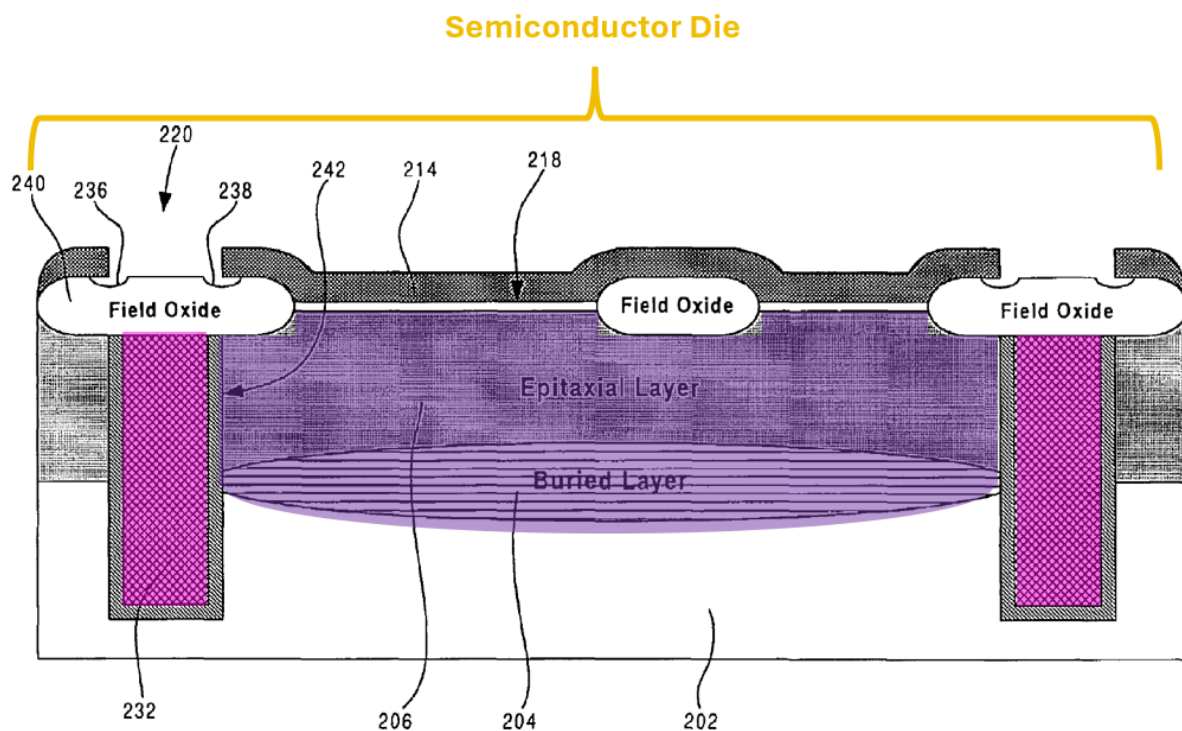


Fig. 2G, (annotation added). In Figure 2G, trench **220** represents a **deep isolation trench** filled with polysilicon **232**. See *Yin*, 6:29-53 (“As a result of the conformal polysilicon deposition process, deposited polysilicon fills **trench 220**.”)

(annotation added). *Yin* further discloses that Figure 2G depicts the cross-section of a wafer, which the '673 Patent refers to as a semiconductor die. *See Yin*, 3:13-16 (“FIG. 2G illustrates cross-sectional views, which include portions of a **wafer**. . .”) (emphasis added); '673 Patent, 5:52-57 (“The **wafer** may be referred to as a **semiconductor die**. . .”) (annotation added).

92. *Yin* also explains that this “**deep trench isolation region** may electrically isolate, for example, a **bipolar transistor**[.]”¹ *Yin*, 1:19-24. In the embodiment shown in Figure 2G, the **bipolar transistor** is shown to be surrounded by the **deep isolation trench**. *Yin*, 1:16-27. The overall structure shown in Figure 2G is located on the **semiconductor die** housing the **bipolar transistor** and **deep trench isolation region**. Compare *Yin*, Fig. 2G with '673 Patent, Fig. 4E (*Yin*'s Figure 2G providing a near-identical cut-away to the portion of the **semiconductor die** shown in '673 Patent Figure 4E).

Claim 1[a]: “a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;”

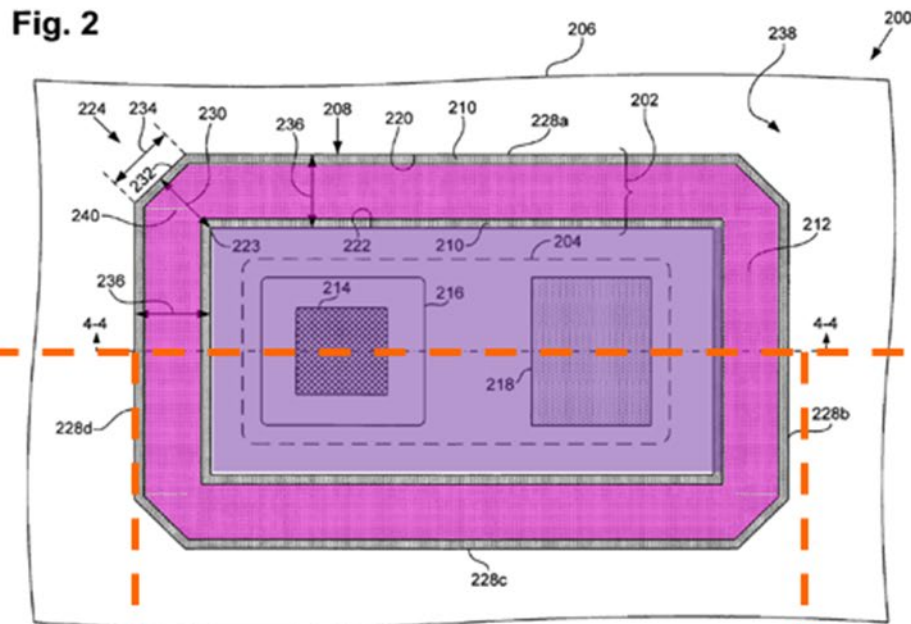
93. In my opinion, the combination of *Yin* and *Koshimizu* discloses a **four-sided trench** situated in a **substrate** of said **semiconductor die**, said **trench**

¹ I note that the '673 Patent specifically names a bipolar transistor as an example of an “electronic device.” *See* '673 Patent, 2:35-38, 3:51-54.

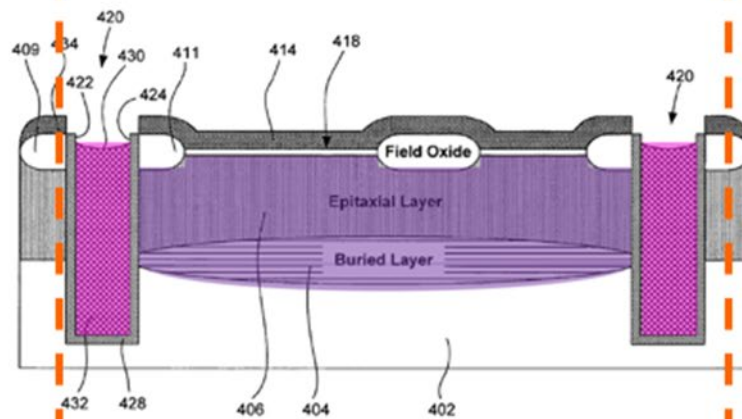
surrounding an **electronic device** and having **trench chamfered corners** (i.e., at least one) connecting said **four sides**.

94. First, *Yin* discloses the enclosure of an **electronic device** (e.g., a **bipolar transistor**) between the **sides** of a **deep isolation trench** situated in a **substrate**. As shown in Figure 2G below, **trench 220** surrounds a **bipolar transistor**. *See Yin* 1:19-27 (“a **deep trench isolation region** may electrically isolate, for example, a **bipolar transistor**[.]”) (annotation added). *Yin* Fig. 2G represents a **bipolar transistor** isolated by a **deep isolation trench** consistent with the manner in which the '673 Patent represents the same:

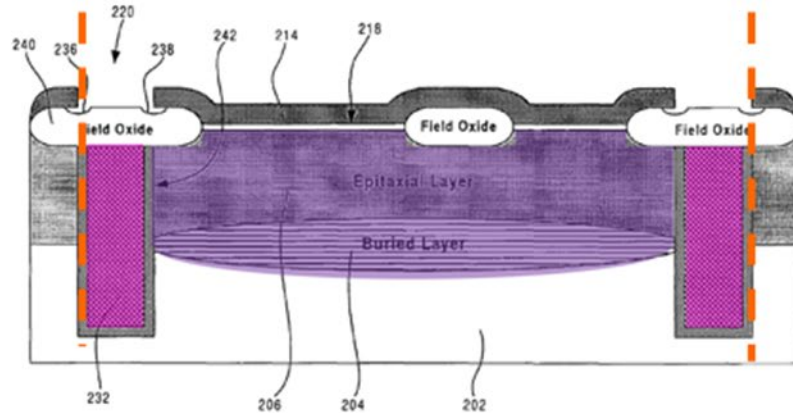
'673
Patent
Fig. 2



'673
Patent
Fig. 4E

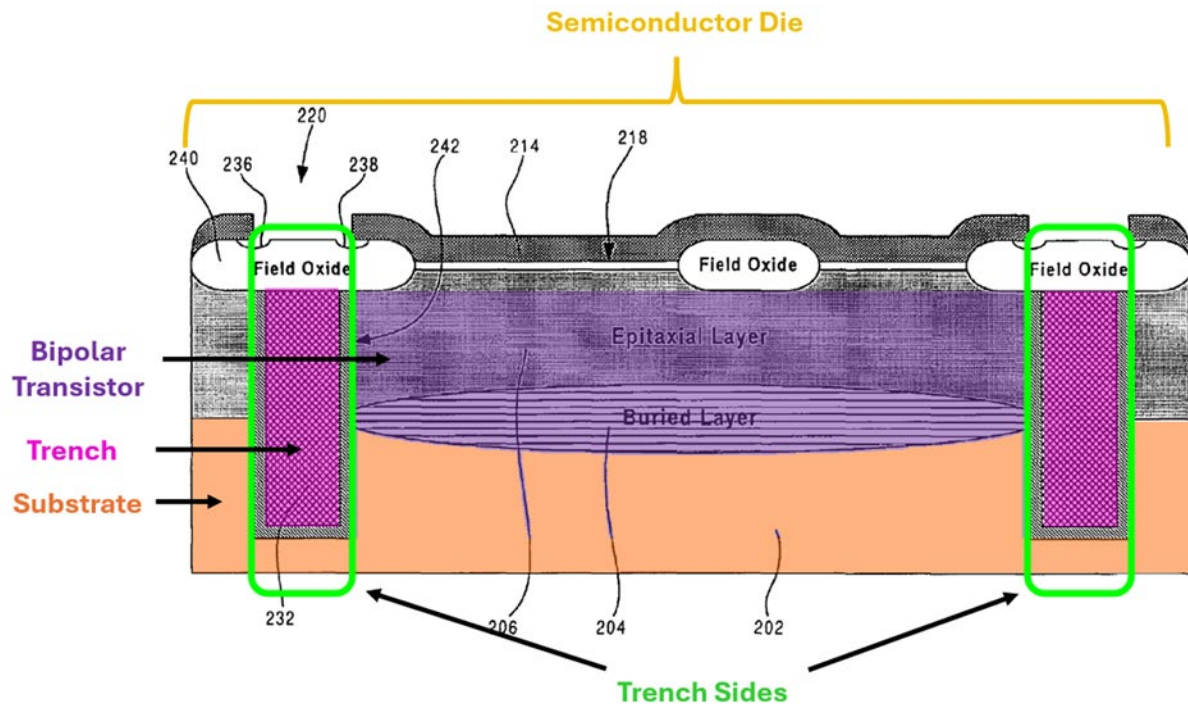


Yin
Fig. 2G



'673 Patent, Figs. 2, 4E, 4:4-23 ("For example, **bipolar device 204** can be a

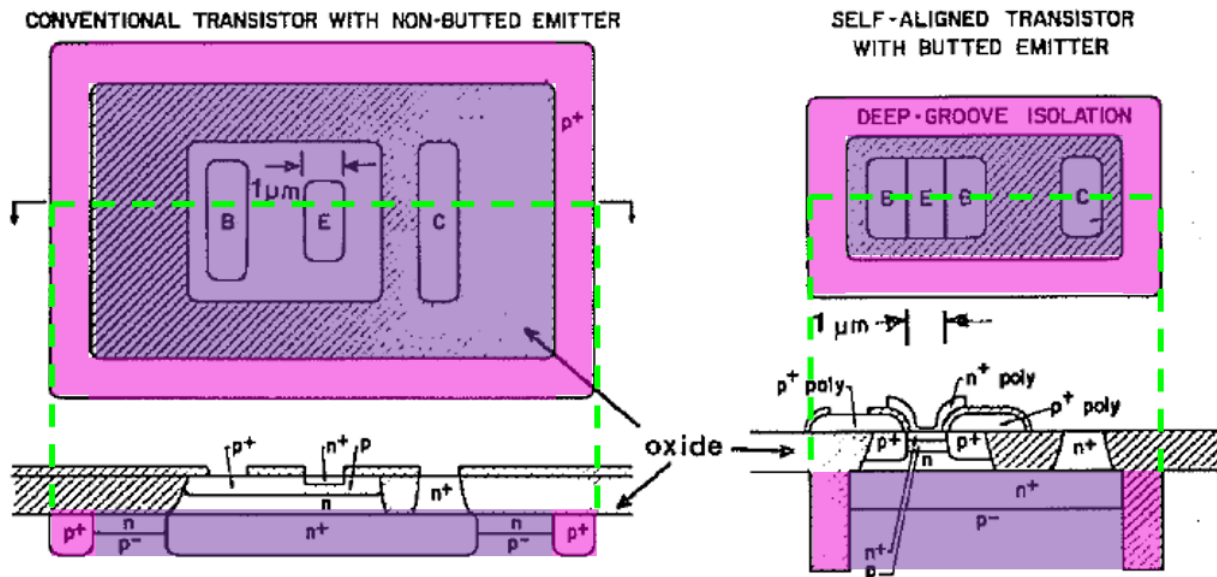
vertical **bipolar transistor**, such as a vertical NPN or PNP transistor.”) (annotation added); *Yin*, Fig. 2G (annotation added). The **trench 220** surrounds the **bipolar transistor** and is situated in **substrate 202**:



Yin, Fig. 2G (annotation added); 1:19-27).

95. Even though *Yin* itself does not provide a top-down view of its **bipolar transistor**, it would have been readily understood by a POSITA to be surrounded by a **four-sided trench**. The manner in which *Yin*'s cut-away is drawn

was standard for **four-sided** semiconductor devices before the '673 Patent.² As an example, this style was used for four-sided devices in textbooks directed to semiconductor devices:



See WOLF, 476 (annotation added)); see also Koshimizu, Figs. 15-16, Figs. 13a-c (showing the same relationship).

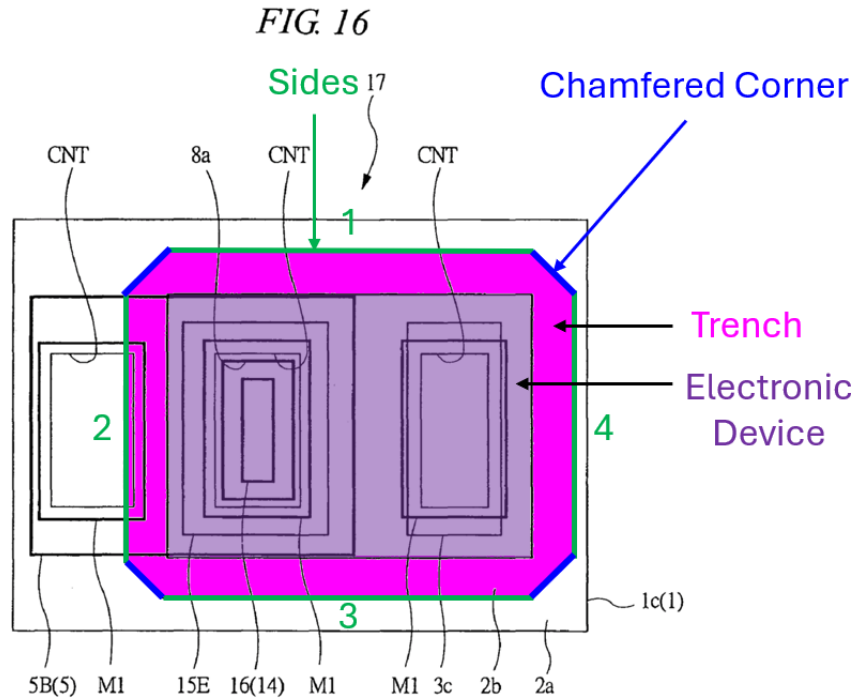
96. In the cut-away view, the two portrayed trenches correspond to two opposite sides of the rectangular die's **four sides**. See WOLF, 476. **Four-sided** semiconductor devices were also the most common type before the '673 Patent and, in the absence of any indication otherwise, a POSITA would have concluded

² It is worth noting once again that the cut-away figures of the '673 Patent (Figs. 4A-F) are nearly identical to those of Yin (Figs. 2A-G), and each of the former reflects a semiconductor die with four sides. See '673 Patent, Figs. 1-4.

Yin disclosed the most common variant. *Yin*, Figs. 2A-G; '673 Patent, Figs. 4A-F; *Verret* (Ex. 1011), Figs. 32-33; *Koshimizu*, Figs. 15-16; *Norström*, Figs. 13a-c; WOLF, 476.

97. Even if *Yin* did not disclose a four-sided trench, in my opinion it would have been obvious to implement *Yin* using a four-sided trench in view of *Koshimizu*'s own four-sided trench and the rest of the prior art. As noted above, four-sided trenches were extremely common, and *Koshimizu* discloses the use of one with its chamfered corners. *Yin*, Figs. 2A-G; '673 Patent, Figs. 4A-F; *Verret*, Figs. 32-33; *Koshimizu*, Figs. 15-16; *Norström*, Figs. 13a-c; WOLF, 476. A POSITA would thus not have needed to modify the overall shape of the trench when using this common configuration to integrate *Koshimizu*'s chamfered corner.

98. For the reasons I previously explained above, it is my opinion that a POSITA would have been motivated to add *Koshimizu*'s **chamfered trench corners** to the **semiconductor die** disclosed by *Yin*. These **chamfered corners** are depicted in Figure 16 of *Koshimizu*:



99. *Koshimizu*, Fig. 16 (annotation added). These **chamfered corners** connect the **four sides** of the **deep trench 2b** in *Koshimizu*. When integrated into *Yin*'s **semiconductor die**, these **chamfered corners** would have likewise connected the **four sides** of *Yin*'s **deep trench isolation region** in the same manner.

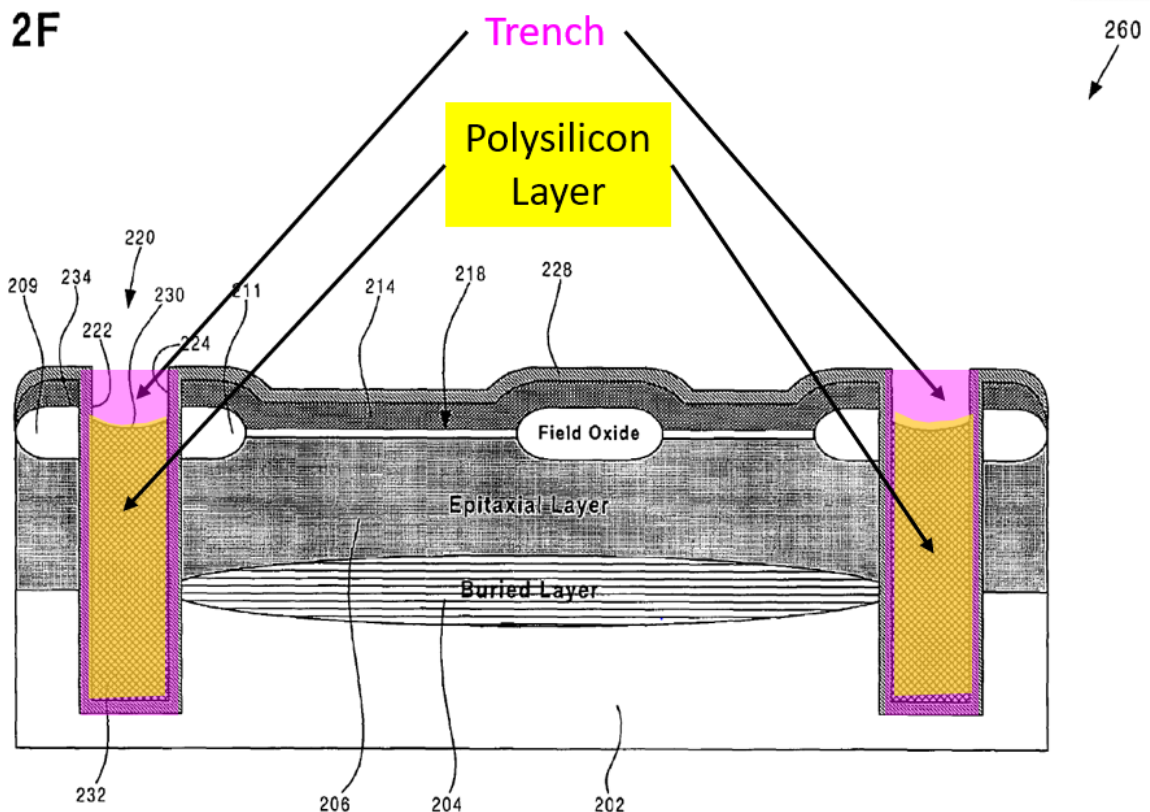
100. *Yin* in view of *Koshimizu* thus teaches a trench situated in a substrate of the semiconductor die, said trench having a plurality (*e.g., four*) of sides surrounding said electronic device, and at least one (*e.g., four*) trench chamfered corner formed between and connecting said plurality (*e.g., four*) of sides.

Claim 1[b]: “wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.”

101. In my opinion, *Yin* in view of *Koshimizu* teaches **trench chamfered corners** that cause a reduction in a thickness of a polysilicon layer within the **trench**, such as within the corners themselves.

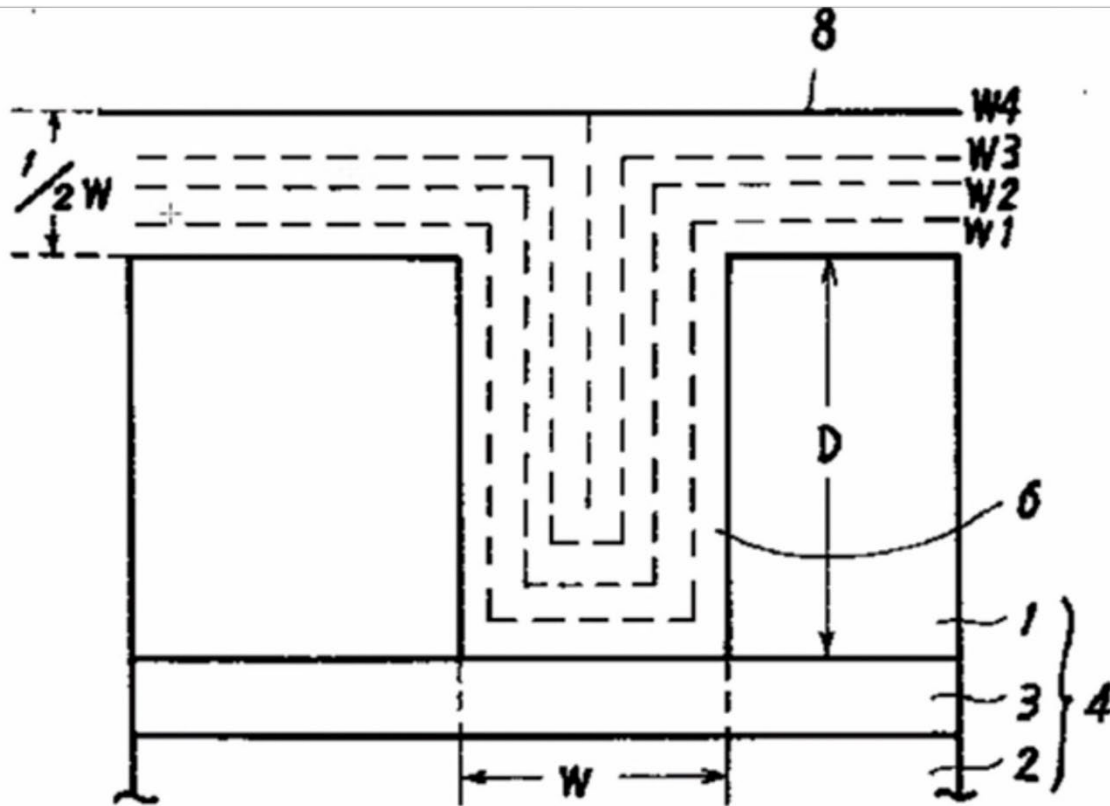
102. First, *Yin* teaches that its **deep isolation trenches** are filled with **polysilicon**. See *Yin*, 6:29-32 (“[I]n Fig. 2F, at step **160** of flowchart **100**, a **layer of polysilicon** is conformally deposited over substrate **202**[.]”); 6:43-44 (“[T]he **layer of polysilicon** is etched back to depth **230** inside **trench 220** to form **polysilicon portion 232**.”). This is shown, for example, in *Yin* Fig 2F:

Fig. 2F



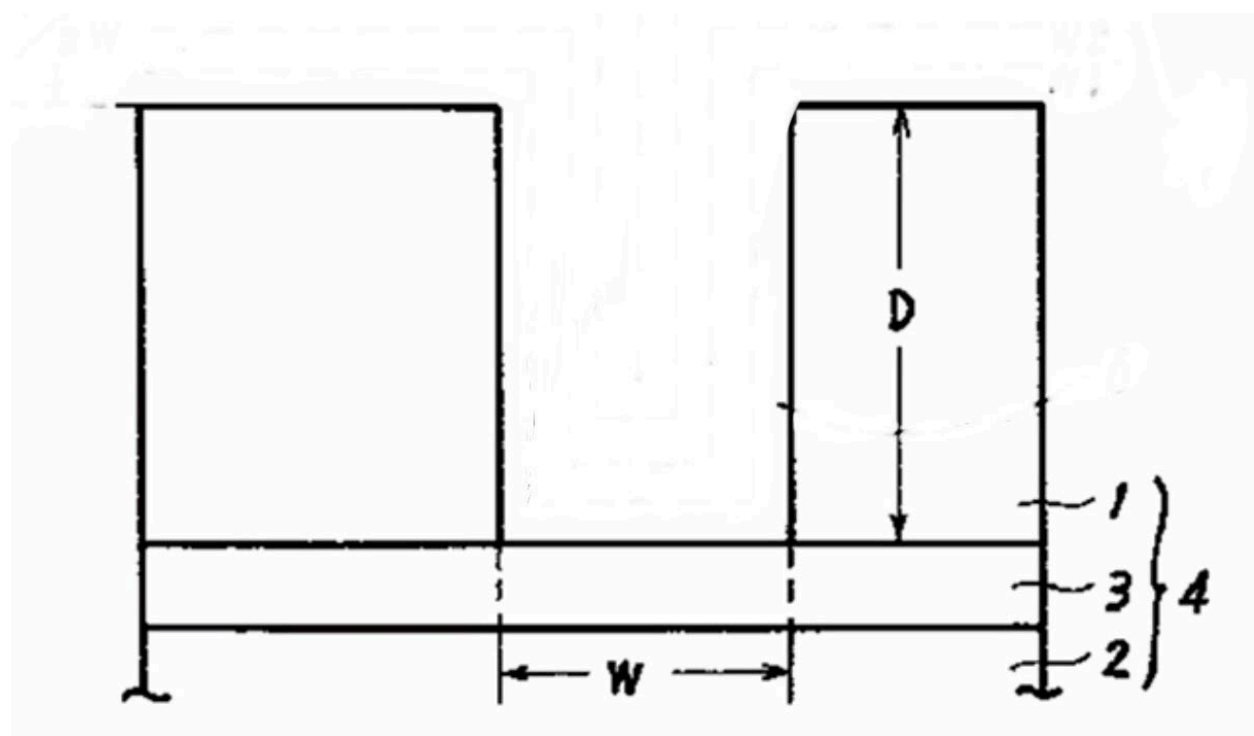
See Yin, Fig. 2F (annotation added). Furthermore, *Koshimizu*'s **chamfered corners** considerably reduce the width of the **trench** at the corners where they would otherwise be the widest if left unchamfered. *See* '673 Patent, Fig. 1 (showing wider corners in a "conventional," prior art unchamfered **trench**).

103. In my opinion, a POSITA would have understood that the thickness of a layer of **polysilicon** within a **trench** at a given location will be reduced if the width of the trench at that location is likewise reduced. As explained by both *Matsuzaki* and WOLF, conformal deposition is the process by which a **deep isolation trench** is refilled with isolating material such as *Yin*'s polysilicon. *See Matsuzaki* (Ex. 1015) 1-4, Fig 4; *see also Matsuzaki* (JP) (Ex. 1014); WOLF, 56, 62. This process is shown, for example, in *Matsuzaki* Fig. 4:

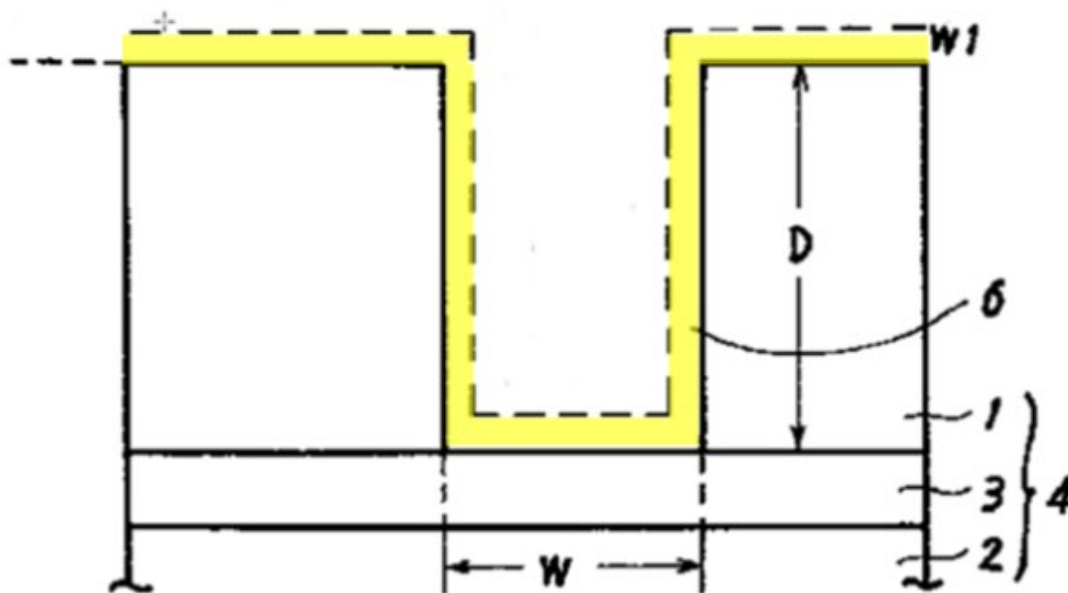


Matsuzaki, Fig. 4.

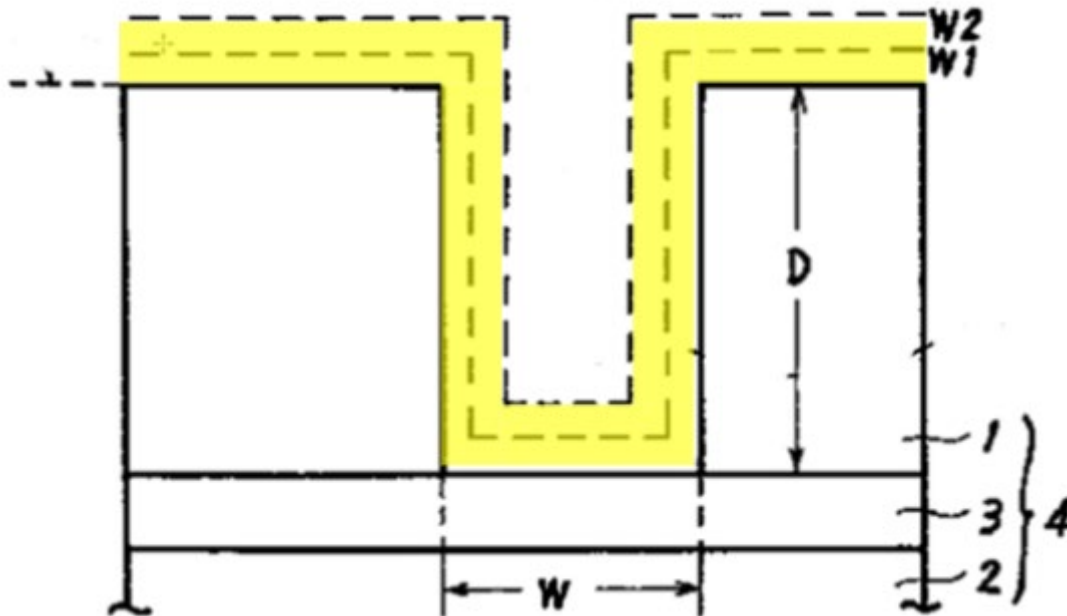
104. During this process, polysilicon is deposited along the surfaces of the trench (both the sides and bottom) as shown in the sequence below using, as an example, Fig. 4 of *Matsuzaki*, broken into pieces for each filling stage “W1,” “W2,” “W3,” and “W4.” The deposited layer of polysilicon grows in thickness until it reaches $W/2$ – or half the width of the trench.



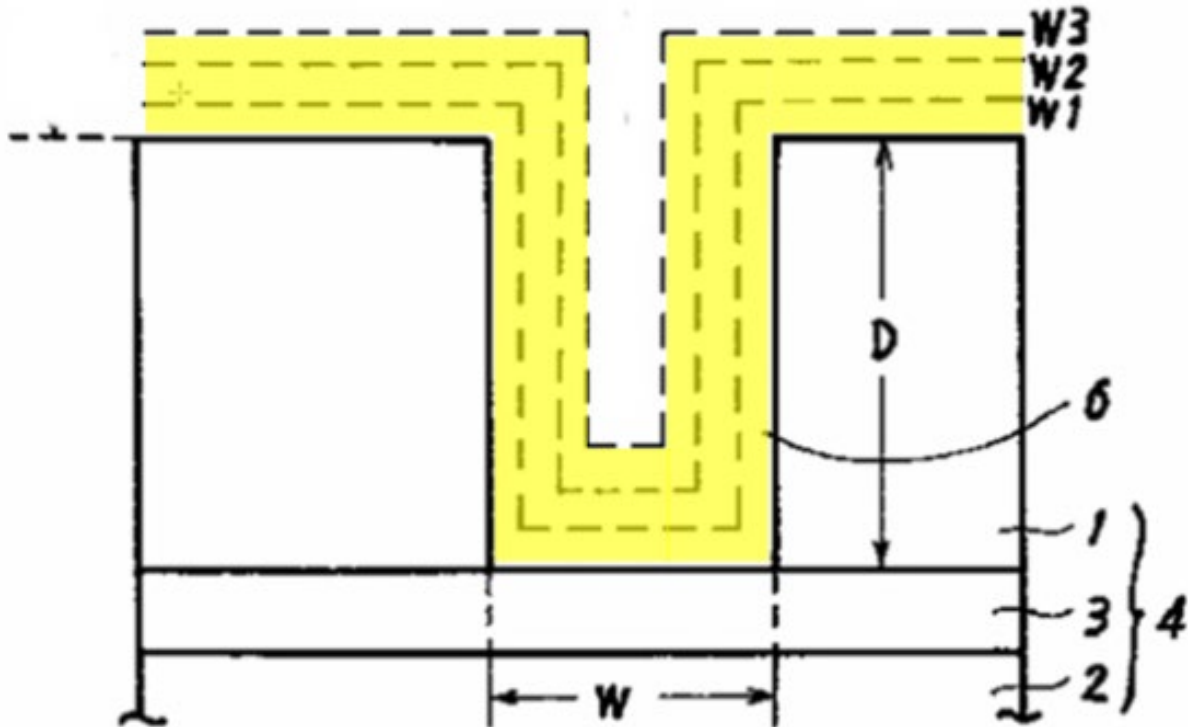
Matsuzaki, Fig. 4 (cropped) (unfilled). In this version of Fig. 4, the trench is dug to a width of " W " and a depth of " D " but no silicon has yet been deposited in it to refill it.



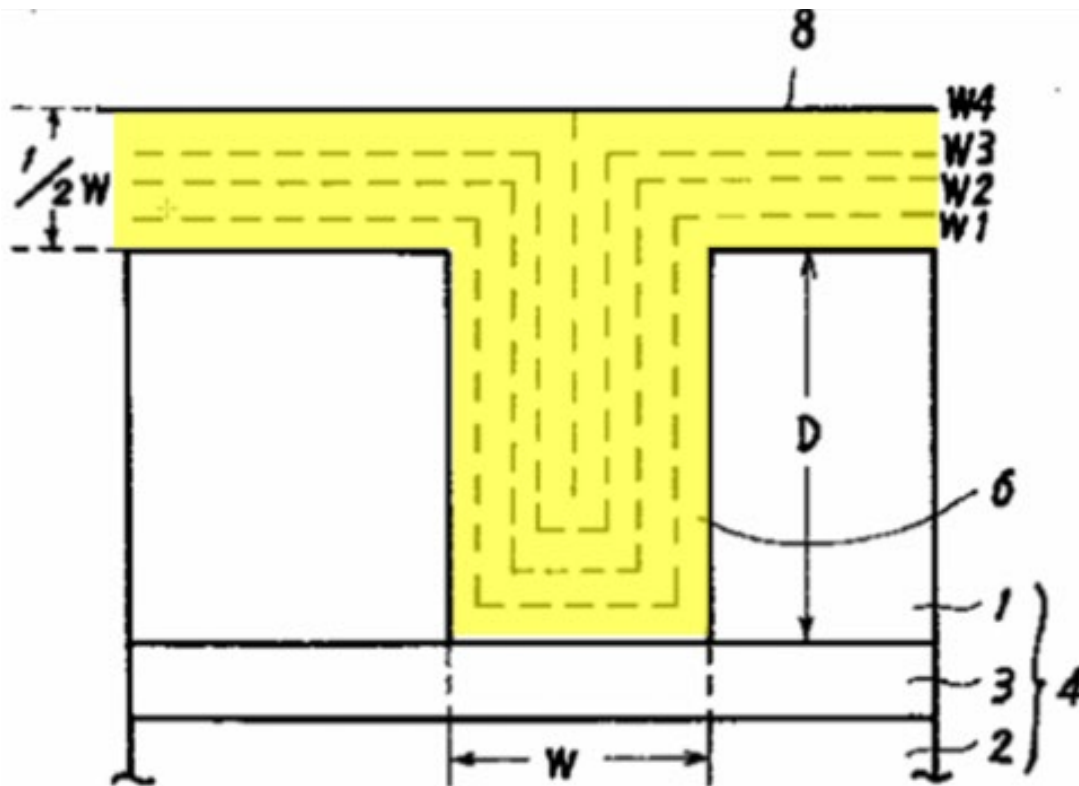
Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to W1)). In this version of Fig. 4, the polysilicon layer has been deposited along the sides and bottom of the trench to thickness “W1” or $W/8$.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to W2)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “W2” or $W/4$.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to $W3$)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “ $W3$ ” or $3W/8$.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to W4)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “W4” or $W/2$ (shown in the full, uncropped version of Fig. 4).

105. As shown in these examples, a POSITA would have understood before the '673 Patent that by reducing the width of a trench at a given location, the thickness of the layer of polysilicon within the trench would likewise be

reduced.³ *See Matsuzaki*, Fig. 4; *see also* WOLF, 56, 62. Thus, *Koshimizu*'s **chamfered corners** reduce the width of the widest portion of the **trench** and cause a reduction in thickness of the **polysilicon filling** them in at least the corner portions.

106. Thus, in my opinion, *Yin* in view of *Koshimizu* teaches a trench chamfered corner that causes a reduction in the thickness of a polysilicon layer within a trench.

Claim 2: "The semiconductor die of claim 1, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides."

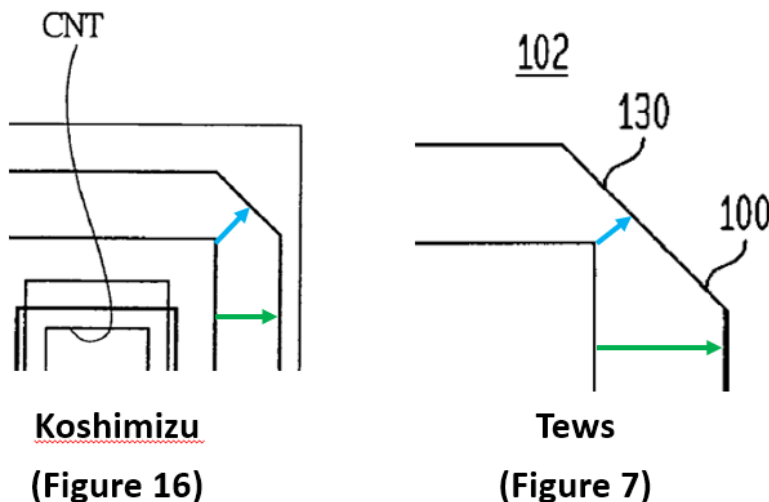
107. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitation of claim 2.

108. The '673 Patent states that "**trench corner width** . . . represents the perpendicular distance, i.e., the minimum distance between corners **118** of outside wall **114** and corners **120** of inside wall **116**, and **trench side width** **124**, which represents the perpendicular distance between outside wall **114** and inside wall **116** along each of sides **117a** through **117d**." '673 Patent, 3:12-18. In other words, the

³ While a POSITA would not have needed the '673 Patent to understand that narrower trenches yield thinner layers of polysilicon within them, the '673 Patent nevertheless confirms this phenomenon. *See, e.g.*, '673 Patent, 5:15-30.

“**trench corner width**” and “**trench side width**” refer to the minimum perpendicular distances across the trench’s corners and sides, respectively.

109. *Koshimizu*’s chamfered corners have, as depicted, less width than the trench side widths to which they connect. See *Koshimizu*, Fig. 16. A trench with a lower **trench corner width** than **trench side width** was not uncommon before the ’673 Patent, appearing in other references such as U.S. Patent No. U.S. 6,362,040 to *Tews* as well:



Koshimizu, Fig. 16 (cropped; annotations added); *Tews*, Fig. 7 (cropped, annotations added). A POSITA would thus have understood *Koshimizu*’s disclosed chamfered corner to be sufficiently chamfered to have a **trench corner width** that is less than a **trench side width**.

110. A POSITA would have also known before the ’673 Patent that trenches made via the etching process will vary in width during manufacturing due

to their very small scale. *See* MURDUCK (Ex. 1013), 288 (“Due to variation in the photolithography process the critical dimension may vary. This could be due to exposure and development of the photoresist or etching of the structure in question and much effort goes into precisely controlling this aspect of the process.”); *Koshimizu* [0048]-[0050]. This means that, as a matter of fact, a trench corner width that is intended to have approximately the same width as trench side widths will occasionally have either more **or less** width due to manufacturing tolerances.

111. If a POSITA were at all uncertain about whether *Koshimizu*’s chamfered trench corners would be thinner than their surrounding sidewalls (despite them being illustrated that way), the mere selection of parameters—in this case, relative width—is firmly within the realm of obviousness experimentation for a POSITA. In my opinion, it would have been a matter of obvious experimentation to adjust the trench chamfer width to be slightly narrower—or wider, for that matter—than the trench side walls to optimize for stability and fill speed. *See, e.g., Stiffler*, 559-62.

112. If a POSITA were at all uncertain about whether *Koshimizu*’s chamfered trench corners were thinner than their surrounding sidewalls (despite them being illustrated that way), I believe that it would have been a matter of obvious experimentation to adjust the trench chamfer width at least slightly around the width of the trench sides.

113. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 2's additional limitation.

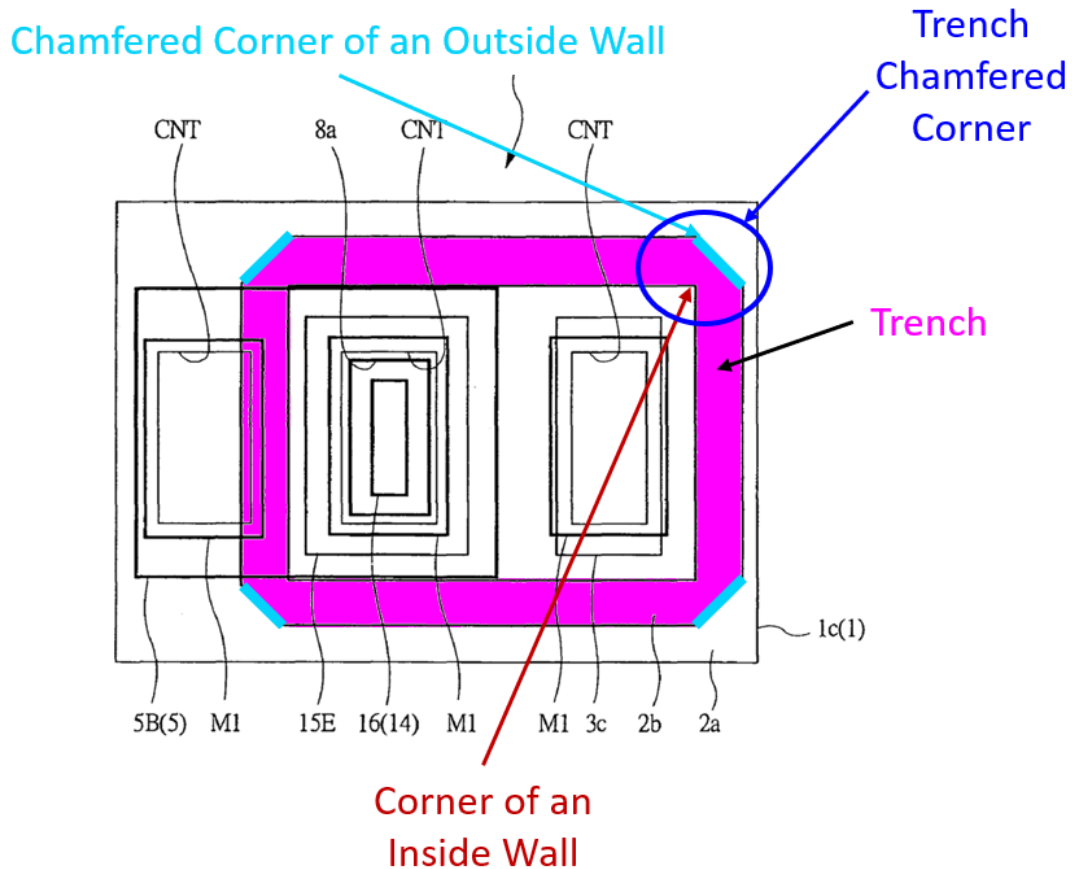
Claim 3: "The semiconductor die of claim 1, wherein said at least one trench chamfered corner comprises a portion of said trench situated between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench."

114. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitation of claim 3.

115. *Koshimizu*'s Figure 16 teaches the **chamfering** of a **corner of an outside wall** of a **trench**. The "**trench chamfered corner**" thus chamfer comprises a portion of the **trench** and is situated between the **chamfered corner of an outside wall** of the **trench** and a **corner of an inside wall of the trench**. See *Koshimizu*, Fig. 16, [0051]-[0061].

116. *Koshimizu* notes that "since FIG. 16 shows a design drawing, each planar shape of the emitter opening portion **14**, the first opening portion **8a**, and the contact holes CNT, etc. is shown in a rectangular shape. **However, such shapes actually become ones without corners.**" *Koshimizu*, [0060] (emphasis added). The bolded portion refers to "each planar shape of the emitter opening portion **14**, the first opening portion **8a**, and the contact holes CNT, etc." and does not refer to the inner corners of the trench **2b**. See below *Koshimizu*, Fig. 16 (annotation added).:

FIG. 16

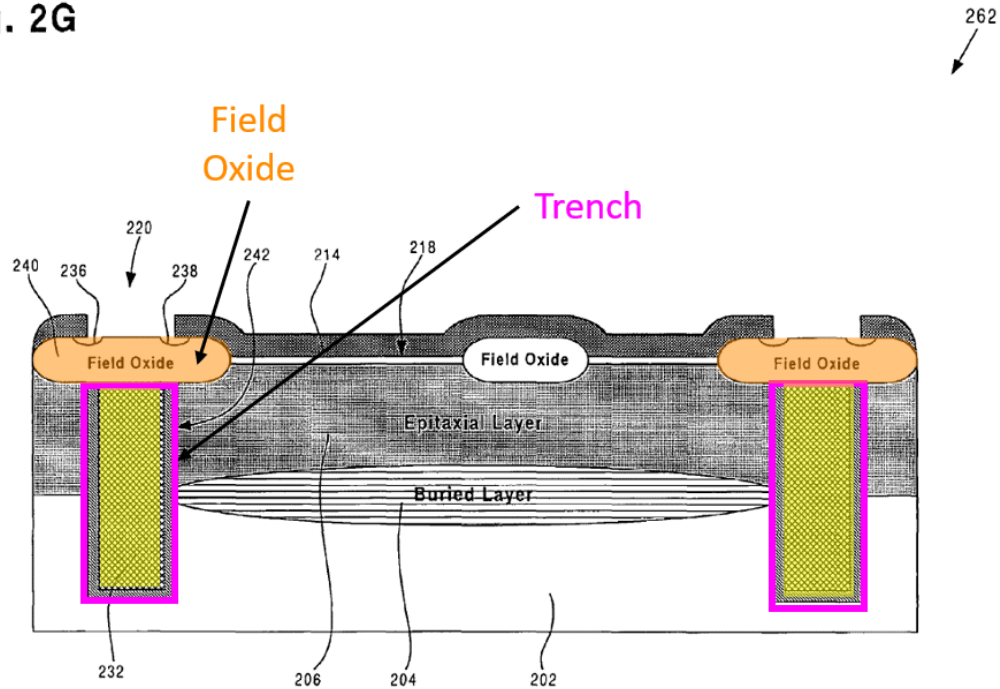


117. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 3's additional limitation.

Claim 4: “The semiconductor die of claim 1, wherein a field oxide region overlies said trench.”

118. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitations of claim 4. As shown in Figure 2G of *Yin*, a **field oxide region** overlies its **deep isolation trench**:

Fig. 2G



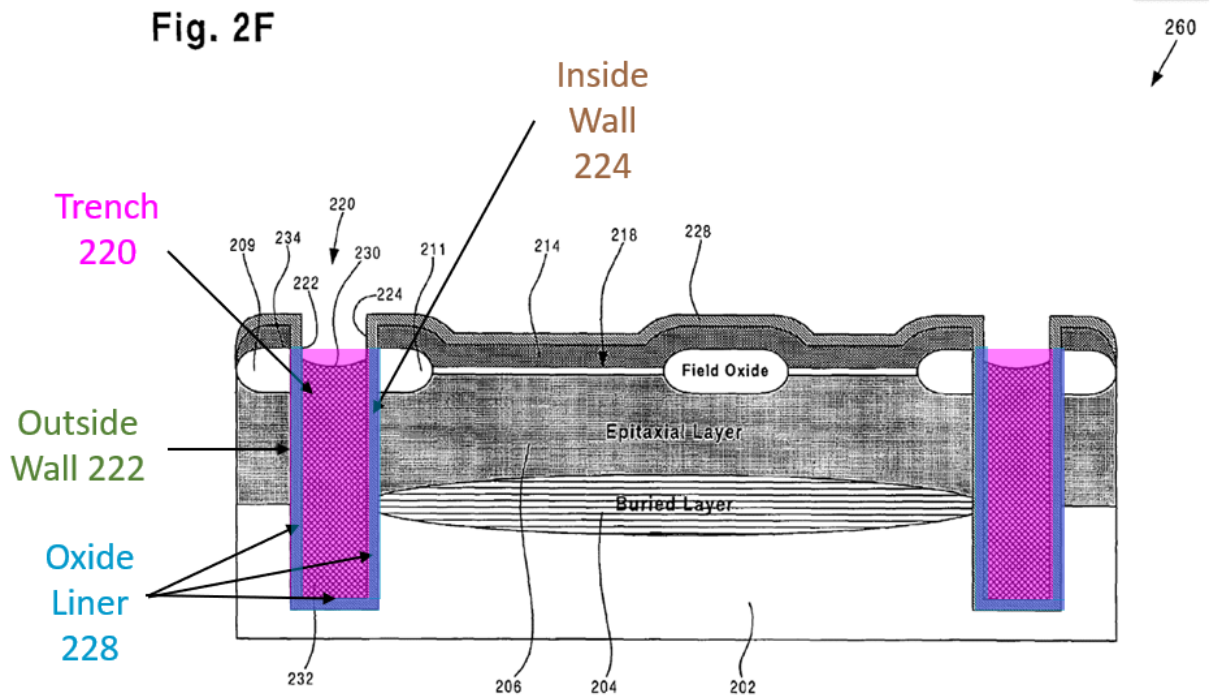
See Yin, Fig. 2G (annotation added), 6:54-65.

119. Therefore, Yin in view of Koshimizu renders obvious claim 4's additional limitation.

Claim 5: "The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on an inside wall and an outside wall of said trench."

120. Yin in view of Koshimizu teaches the additional limitation of claim 5.

121. As shown in Yin Figure 2F, an **oxide liner** is situated on the **inner** and **outer** walls of **trench 220**:



Yin, Fig. 2F; *see also Yin*, 6:13-16 (“Next, **oxide liner 228**, also referred to as a ‘CVD oxide liner’ in the present application, is formed by depositing a layer of TEOS oxide on sidewalls **222** and **224** and bottom surface **226** of **trench 220**”).

122. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 5’s additional limitation.

Claim 6: “The semiconductor die of claim 2, wherein said trench side width along said plurality of sides is approximately 1.0 micron.”

123. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitation of claim 6.

124. *Yin* discloses that the side width of its trench sidewalls is approximately 1.0 micron. *See Yin*, 4:64-67 (“The width of trench 220 . . . can be, for example, approximately 1.0 micron.”).

125. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 6's additional limitation.

Claim 7: "The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package."

126. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitation of claim 7.

127. *Yin* also discloses that its semiconductor die is designed for a "Bipolar Complementary-Metal-Oxide-Semiconductor ('BiCMOS') process" in which "deep trench isolation regions are typically formed to provide isolation between adjacent active regions of a semiconductor substrate." *Yin*, 1:15-19. *Yin* further discloses that its "deep trench isolation region may electrically isolate, for example, a bipolar transistor . . . from an adjacent CMOS transistor, such as a PFET, fabricated on the same semiconductor substrate." *Yin*, 1:19-24. "BiCMOS" technology with multiple bipolar transistor devices in one semiconductor package or chip was standard use for bipolar transistor devices before the '673 Patent. *See* SHEPHERD, 1-7. A POSITA would thus have understood that *Yin*'s disclosed semiconductor die was or would be enclosed in a semiconductor package with neighboring semiconductor devices from which electrical isolation was necessary and/or desirable.

128. Semiconductor devices such as *Yin*'s isolated bipolar transistor are customarily used in semiconductor wafers (referred to by the '673 patent as

semiconductor dies, *see* '673 Patent, 5:55-57) which are in turn customarily integrated into packages for use in computing applications—and they had been for decades before the '673 Patent. *See* WOLF, 1-5.

129. As I explained in the Technology Background Section, *supra*, integrated circuit technology with multiple semiconductor devices in one semiconductor package or chip was standard use for bipolar transistor devices at the time of the '673 Patent. *See* SHEPHERD, 1-7. This includes “BiCMOS” technology with multiple bipolar transistor devices in one semiconductor package or chip was standard use for bipolar transistor devices at the time of the '673 patent. *See id.*, 5-6. A POSITA would thus have understood that both *Yin*'s disclosed semiconductor die was or would be enclosed in a semiconductor package with neighboring semiconductor devices from which electrical isolation was necessary and/or desirable.

130. To the extent *Yin* is at all unclear, I believe it would have been obvious to enclose *Yin*'s semiconductor die in a semiconductor package in view of the level of ordinary skill in the art. The primary purpose of a deep isolation trench is to isolate a device—in this case, a bipolar transistor—from neighboring devices on the same semiconductor package. *Yin*, 1:19-24. As one example, computer chips such as high-density complementary MOS (“CMOS”) chips employ semiconductor packages enclosing multiple bipolar transistors. *See* SHEPHERD, 1-7.

A POSITA would thus have found it obvious to use *Yin*'s semiconductor die in an application enclosing it in a semiconductor package with multiple similar or identical semiconductor devices.

131. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 7's additional limitation.

Claim 8: "The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor."

132. In my opinion, *Yin* in view of *Koshimizu* teaches the additional limitation of claim 8.

133. *Yin* discloses that its "deep trench isolation region may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium heterojunction bipolar transistor[.]" *Yin*, 1:19-22.

134. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 8's additional limitation.

Claim 9: "The semiconductor die of claim 1, wherein said electronic device is a silicon-germanium bipolar transistor."

135. *Yin* in view of *Koshimizu* teaches the additional limitation of claim 9.

136. *Yin* discloses that its "deep trench isolation region may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium heterojunction bipolar transistor[.]" *Yin*, 1:19-22.

137. Therefore, in my opinion, *Yin* in view of *Koshimizu* renders obvious claim 9's additional limitation.

Claim 10[pre]: "A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:"

138. In my opinion, to the extent the preamble is limiting, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 1[pre]. See claim 1[pre], *supra*.

Claim 10[a]: "at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;"

139. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 1[a]. See claim 1[a], *supra*.

Claim 10[b]: "each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench."

140. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 1[b]. See claim 1[b], *supra*.

Claim 11: "The semiconductor die of claim 10, wherein a trench corner width at each of said four trench chamfered corners is less than a trench side width along each of said four sides of said at least one trench."

141. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 2. See claim 2, *supra*.

Claim 12: “The semiconductor die of claim 10, wherein said each of said four trench chamfered corners comprises a portion of said at least one trench situated between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.”

142. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 3. See claim 3, *supra*.

Claim 13: “The semiconductor die of claim 10, wherein a field oxide region overlies said at least one trench.”

143. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 4. See claim 4, *supra*.

Claim 14: “The semiconductor die of claim 10, wherein said at least one trench further comprises an oxide liner situated on an inside wall and an outside wall of said at least one trench.”

144. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 5. See claim 5, *supra*.

Claim 15: “The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package.”

145. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 7. See claim 7, *supra*.

Claim 16: “The semiconductor die of claim 10, wherein said electronic device is a bipolar transistor.”

146. In my opinion, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 8. See claim 8, *supra*.

Claim 17: “The semiconductor die of claim 10, wherein said electronic device is a silicon-germanium bipolar transistor.”

147. *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated for claim 9. See claim 9, *supra*.

B. Ground 2: Claims 1, 3, 5, 7-8, 10, 12, and 14-16 Are Anticipated By *Norström*

Claim 1[preamble]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”

148. To the extent the preamble is limiting, it is my opinion that *Norström* discloses a semiconductor die including at least one deep trench isolation region for isolating an electronic device, e.g., a bipolar transistor.

149. *Norström* discloses that its “present invention relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” *Norström*, 1:7-10. One example of this is shown in Fig. 13a, where a semiconductor die has a bipolar transistor electrically isolated by a deep trench isolation region:

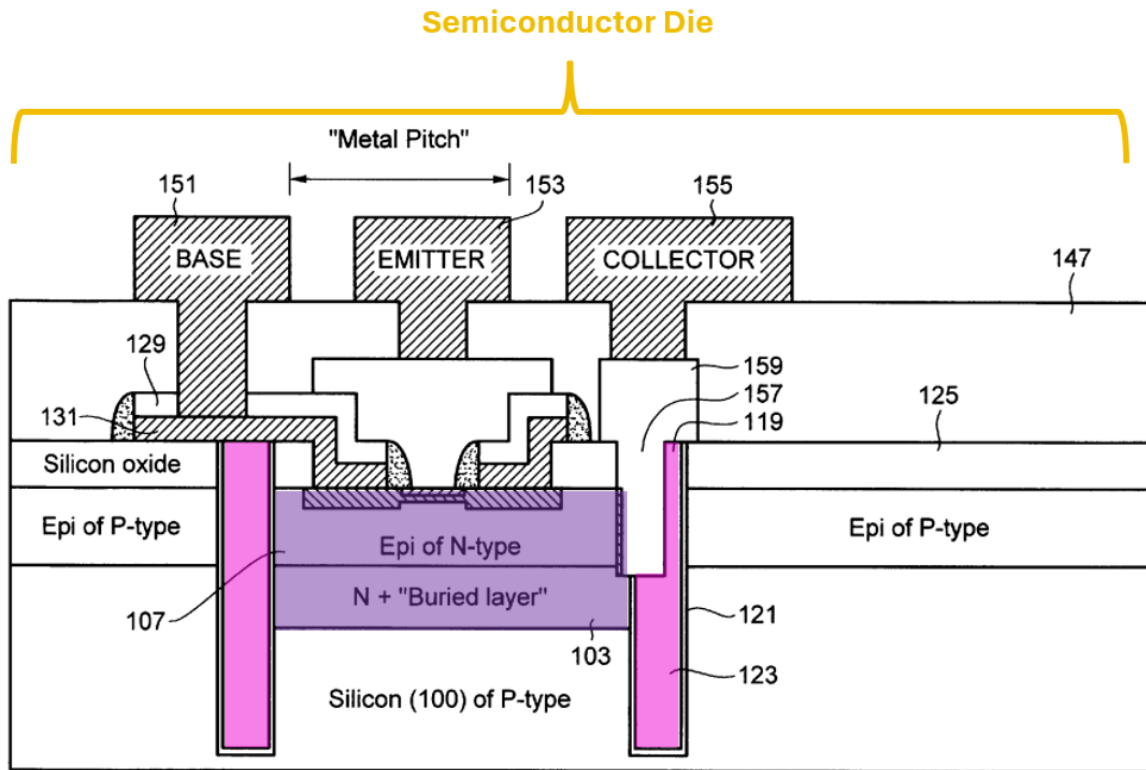


FIG. 13a

Norström, Fig. 13a (annotation added), Figs. 8-13 (showing manufacturing process); 6:24-27 (“Fig. 13a is a schematic cross sectional view . . . of the finished NPN transistor[.]”).

150. In my opinion, *Norström* thus discloses a **semiconductor die** including at least one **deep trench isolation region** for isolating an **electronic device**, *e.g.*, a **bipolar transistor**.

Claim 1[a]: “a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner between and connecting said plurality of sides;”

151. In my opinion, *Norström* discloses a **four-sided trench** situated in a **substrate** of said **semiconductor die**, said **trench** surrounding an **electronic device** and having four **trench chamfered corners** (i.e., at least one) connecting said **four sides**.

152. Figure 13c of *Norström* depicts the top view of the **semiconductor die** from Figure 13a:

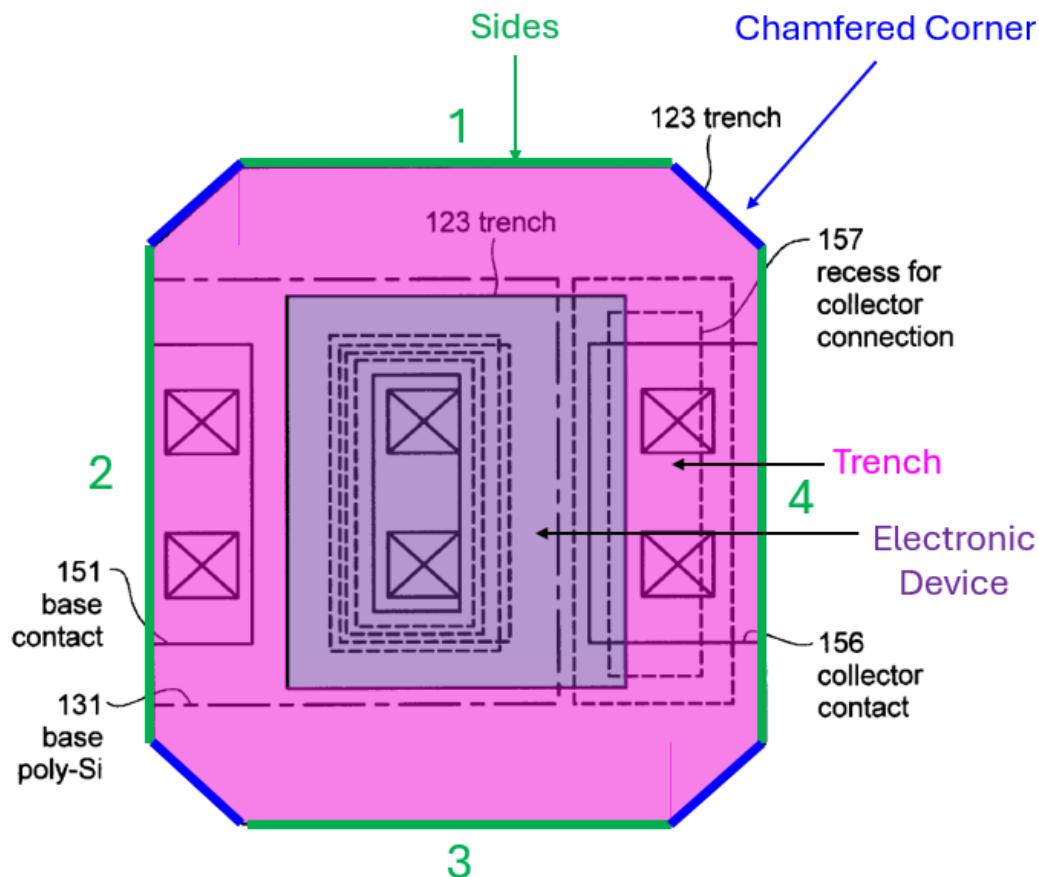


FIG. 13c

Norström, Fig. 13c (annotation added); 6:32-34; 11:6-7 (“The result appears from Fig. 13a, see also the plan view of Fig. 13c.”). As shown in Figure 13c, *Norström*’s **trench 123** surrounds the **bipolar NPN transistor** within, which is an **electronic device**. *Norström*, Figs. 13a & c. *Norström*’s **trench 123** also has **four sides**.

Norström, Fig. 13c. Figure 13c also depicts the four **trench chamfered corners** at the outer edge of **trench 123** connecting the **four sides** of the **trench**. *Norström*, Fig. 13c.

153. *Norström* provides specific angles for its **trench chamfered corners**, noting that “the outer sidewalls of the **trench 123** shown in Fig 13c have no right angles, but the flat sidewall segments form an angle of 135° to each other.” *Norström*, 16:39-42.

154. Returning to Figure 13a shows that both the **trench** and the **electronic device** (the **NPN bipolar transistor**) are situated in a **substrate** of silicon within the semiconductor die:

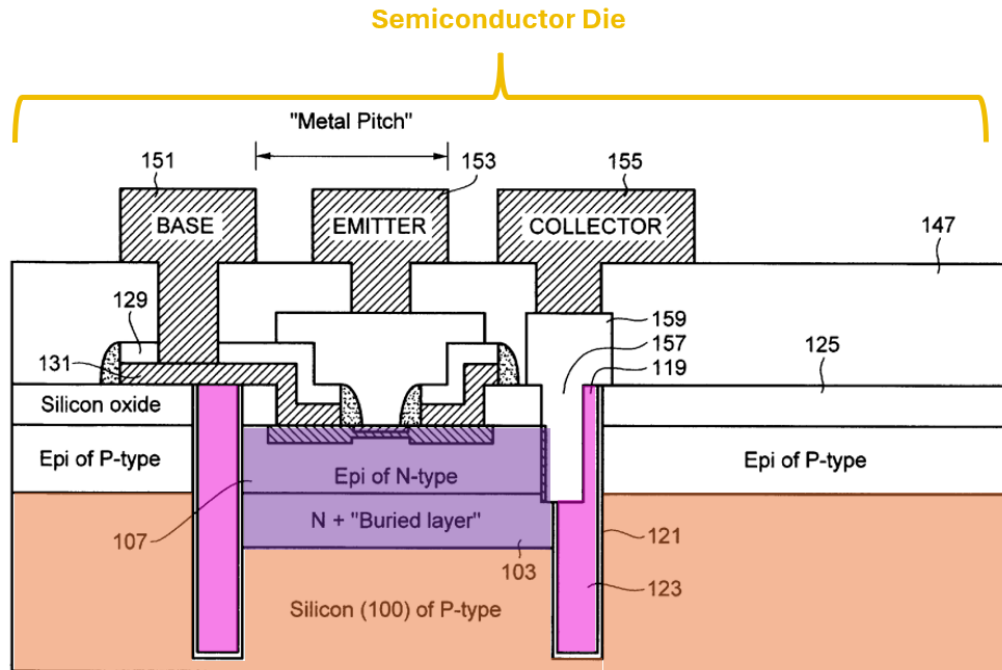


FIG. 13a

Norström, Fig. 13a, 9:31-55 (describing the features of Figures 8-13 being situated into a “P-type” **substrate**).

155. Therefore, in my opinion, *Norström* discloses a trench situated in a substrate of the semiconductor die, said trench having a plurality (*e.g., four*) of sides surrounding said electronic device, and at least one (*e.g., four*) trench chamfered corner formed between and connecting said plurality (*e.g., four*) of sides.

Claim 1[b]: “wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.”

156. *Norström* discloses **trench chamfered corners that** cause a reduction in a thickness of a **polysilicon layer** within the **trench**, such as within the corners themselves.

157. First, *Norström* discloses that its **isolation trenches** may be filled with **polysilicon**. *Norström*, 7:47-50 (“[T]he trenches are filled with an isolating or semi-isolating material **123**, for example, silicon oxide or polycrystalline silicon[.]”).

158. For the reasons explained for Ground 1, a POSITA would have understood that by chamfering the outer corners of a deep isolation trench, the thickness of the polysilicon layer within the trench would be reduced at the narrowed chamfer. In addition to these reasons, *Norström* specifically discloses that chamfered outer trench corners improve the refill process over non-chamfered corners. As *Norström* explains:

It should be observed that the exterior corners of the isolating trench 257, which surrounds the PNP-transistor as a frame, has [sic] been made oblique by an angle of about 45° ***in order to improve the refilling of the trench***. It appears advantageous to always form a deep groove, which is to be filled with some material, such as isolating or conducting material, to have walls, which do not form comers [sic] having angles about 90°, but these angles should instead be as large as possible, for

example 135°.

Norström, 16:28-36 (emphasis added). In other words, *Norström* discloses the same chamfer and reasoning for using that chamfer the '673 Patent itself disclosed – *i.e.*, that these chamfered corners improve the trench refill process and reduce polysilicon waste. See '673 Patent, 9:6-10 (“As a result, the invention’s deep trench isolation region significantly increases polysilicon fill process throughput and the average time between polysilicon deposition furnace cleaning, thereby advantageously reducing manufacturing cost.”).

159. Thus, in my opinion, *Norström* discloses a trench chamfered corner that causes a reduction in the thickness of a polysilicon layer within a trench.

Claim 3: “The semiconductor die of claim 1, wherein said at least one trench chamfered corner comprises a portion of said trench situated between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.”

160. In my opinion, *Norström* discloses the additional limitation of claim 3.

161. As I explained for Claim 1[a], *Norström*’s Figure 13c discloses the **chamfering** of a **corner of an outside wall** of a **trench**. The “**trench chamfered corner**” thus chamfer comprises a portion of the **trench** and is situated between the **chamfered corner of an outside wall** of the **trench** and a **corner of an inside wall of the trench**.

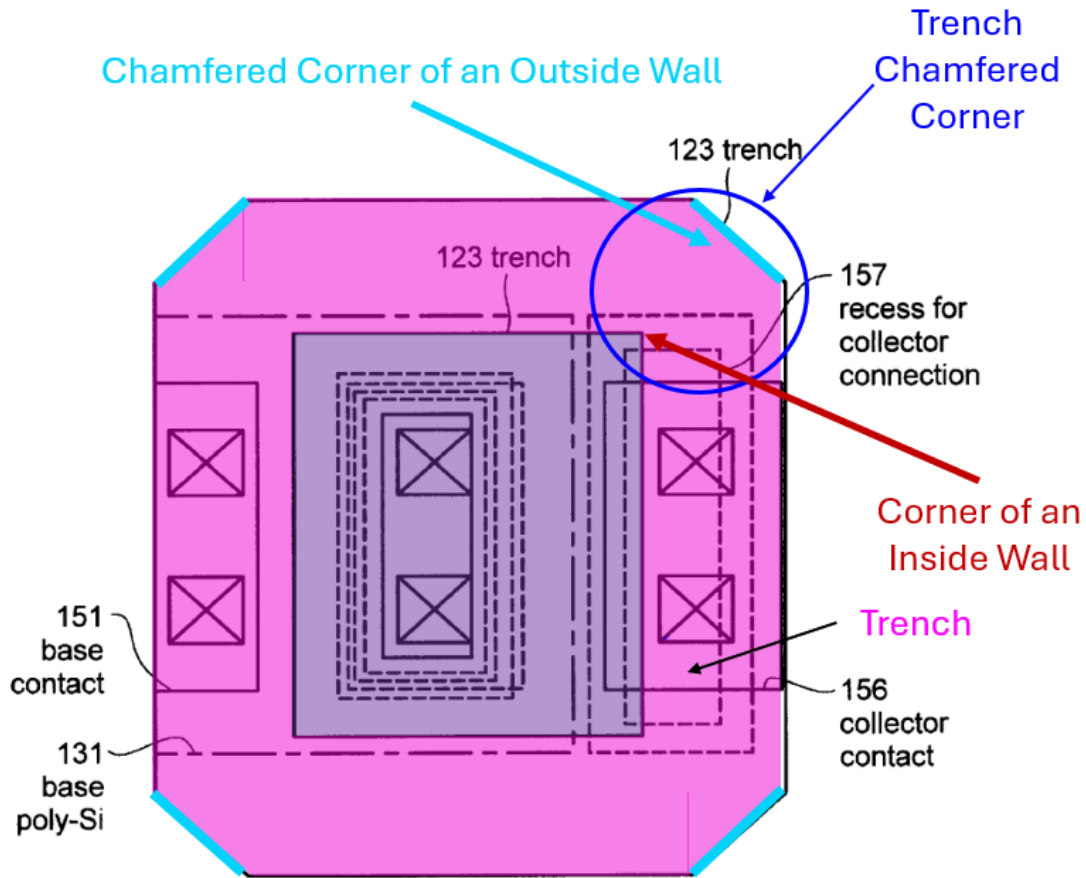


FIG. 13c

See Norström, Fig. 13c (annotation added); 16:28-36.

162. Therefore, in my opinion, *Norström* discloses claim 3's additional limitation.

Claim 5: "The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on an inside wall and an outside wall of said trench."

163. In my opinion, *Norström* discloses the additional limitation of claim 5.

164. *Norström* discloses that the semiconductor die depicted in Figures 13a and 13c contains a **thin surface layer of silicon oxide** on their **sidewalls**. See

Norström, 9:42-44 (“The **trenches 119** are then thermally oxidized so that their **sidewalls** and bottom surfaces obtain a **thin surface layer 121 of silicon oxide**[.]”) (annotation added); A POSITA would have understood this “**thin surface layer . . . of silicon oxide**” to be an **oxide liner**. See ’673 Patent, 3:29-50 (describing a thin layer of “silicon oxide” as an “oxide liner”). This is depicted in *Norström* Fig 13a:

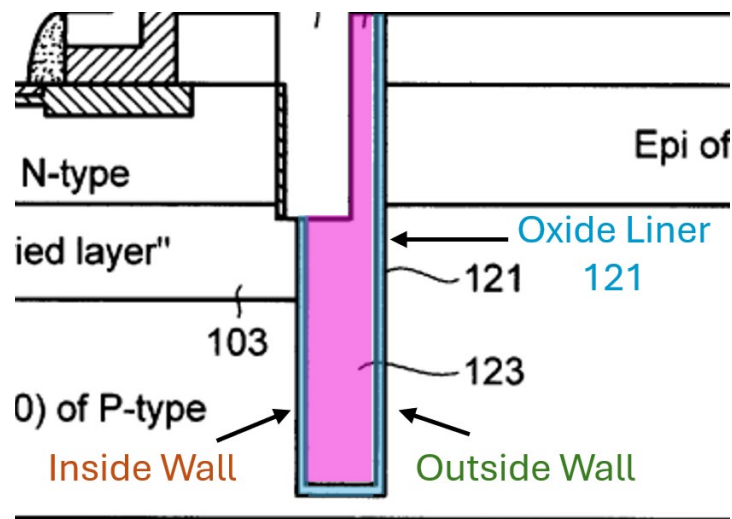


FIG. 13a

Norström, Fig. 13a (cropped, annotation added).

165. Therefore, in my opinion, *Norström* discloses claim 5’s additional limitation.

Claim 7: “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”

166. In my opinion, *Norström* discloses the additional limitation of claim 7.

167. *Norström* discloses that its subject matter is directed towards bipolar transistors manufactured on “the same silicon plate” that can be “isolated from each other by areas comprising deep P-diffusions, which extend through the epitaxial layer down to the inner or interior material of the silicon plate, i.e., the substrate, which in these cases is silicon of P-type.” *Norström*, 1:29-34. A POSITA would have understood the silicon plate to be a semiconductor package on which multiple isolated bipolar transistors—as well as the semiconductor die they are printed on—are housed next to each other. *See* SHEPHERD, 1-7.

168. Therefore, in my opinion, *Norström* discloses claim 7’s additional limitation.

Claim 8: “The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.”

169. In my opinion, *Norström* discloses the additional limitation of claim 8.

170. *Norström* explains that Figure 13 depicts an **NPN-type bipolar transistor** with **deep isolation trenches** electrically isolating the **transistor**. *Norström*, 6:23-34; *see also id.*, 8:50-11:40 (describing the manufacturing process for the same); 1:7-10 (noting disclosure is directed to “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.”).

171. Therefore, in my opinion, *Norström* discloses claim 8’s additional limitation.

Claim 10[pre]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”

172. In my opinion, to the extent the preamble is limiting, *Norström* discloses this limitation for the same reasons as stated for claim 1[pre]. See claim 1[pre], *supra*.

Claim 10[a]: “at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;”

173. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 1[a]. See claim 1[a], *supra*.

Claim 10[b]: “each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.”

174. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 1[b]. See claim 1[b], *supra*.

Claim 12: “The semiconductor die of claim 10, wherein said each of said four trench chamfered corners comprises a portion of said at least one trench situated between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.”

175. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 3. See claim 3, *supra*.

Claim 14: “The semiconductor die of claim 10, wherein said at least one trench further comprises an oxide liner situated on an inside wall and an outside wall of said at least one trench.”

176. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 5. *See* claim 5, *supra*.

Claim 15: “The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package.”

177. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 7. *See* claim 7, *supra*.

Claim 16: “The semiconductor die of claim 10, wherein said electronic device is a bipolar transistor.”

178. In my opinion, *Norström* discloses this limitation for the same reasons as stated for claim 8. *See* claim 8, *supra*.

C. Ground 3: Claims 7 and 15 Would Have Been Obvious Over *Norström*

Claim 7: “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”

179. To the extent *Norström* does not disclose the additional limitation of claim 7, in my opinion, a POSITA would have found it obvious over *Norström*.

180. *Norström* discloses each of the limitations of independent claim 1 for the same reasons stated in Ground 2. It would have then been obvious to enclose *Norström*'s semiconductor die in a semiconductor package in view of the level of ordinary skill in the art.

181. As I explained in the Technology Background Section, *supra*, bipolar transistors such as the one disclosed by *Norström* were commonly used to make up the computer logic of the semiconductor dies that make up integrated circuits or computer chips. And the primary purpose of a deep isolation trench is to isolate a device—in this case, a bipolar transistor—from neighboring devices on the same semiconductor package. *See Norström*, 1:29-34. As one example, computer chips such as high-density complementary MOS (“CMOS”) chips employ semiconductor packages enclosing multiple bipolar transistors. *SHEPHERD*, 1-7. Semiconductor devices such as *Norström*’s isolated bipolar transistor are also customarily used in semiconductor wafers (referred to by the ’673 patent as semiconductor dies, *see* ’673 Patent, 5:55-57) which are in turn customarily integrated into packages for use in computing applications—and they had been for decades before the ’673 Patent. *See WOLF*, 1-5.

182. A POSITA would have had a reasonable expectation of success in using *Norström*’s semiconductor die in a semiconductor package, since packaging a die was a common practice and only required simple steps such as placing the semiconductor die in a package made out of plastic or other commonly available materials. *See, e.g., id.* A POSITA would thus have found it obvious to use *Norström*’s semiconductor die in an application enclosing it in a semiconductor package with multiple similar or identical semiconductor devices.

183. Therefore, in my opinion, *Norström* renders obvious claim 7's additional limitation.

Claim 15: "The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package."

184. *Norström* discloses each of the limitations of claim 10 for the same reasons stated in Ground 2. *Norström* renders obvious the additional limitation of claim 15 for the same reasons as stated in claim 7. *See* claim 7, *supra*.

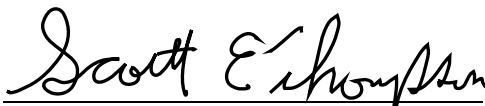
XII. CONCLUSION

185. For the reasons set forth in Section XI, it is my opinion that one skilled in the art would have found claims 1-17 of the '673 Patent anticipated by or obvious over the prior art.

186. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

187. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 20, 2024

By: 
Dr. Scott E. Thompson, Ph.D.

APPENDIX A

SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

- 1992 Ph.D. (Electrical Engineering), University of Florida
- 1988 Master of Science in Electrical Engineering, University of Florida
- 1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- ❑ Tenured Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- ❑ Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
 - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- ❑ Researcher on advanced chip technology at University of Florida totaling \$4M worth of research contracts.
 - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- ❑ Consultant (non litigation) last 5 years: Xperi Corporation
- ❑ **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- ❑ Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- ❑ Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- ❑ Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- ❑ National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

C. Legal cases

- ❑ Bold is the client
 - Godo Kaisha IP Bridge v/ **Xilinx/TSMC**
 - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017

- **KAIST IP v. Apple**
 - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
 - Case in Korea : Intellectual Property Trial and Appeal Board (“IPTAB”) regarding Korean Patent No. 10-0458288 (hereinafter, “KR ‘288 patent”).
- **Godo Kaisha IP Bridge, Inc. v. NVIDIA**
 - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1
- **Chinese Academy of Sciences v. Intel**
 - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
 - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
 - Beijing Court Testimony IME vs Lenovo 11/21/2021
 - Beijing court Testimony IME vs Intel China 1/12/2022
- **IFT v. TSMC (ITC case)**
 - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
 - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- **NXP v. Impinj**
 - 9,495,631, IPR2020-00543 - filed 2/10/2020
 - 9,633,302, IPR2020-00516 - filed 2/5/2020
 - 6,680,523, IPR2020-01630 - filed 9/17/2020
 - 7,538,444, IPR2021-00003 - filed 10/5/2020
 - Oakland District Court Case No. 4:19-cv-03161-YGR
- **Katana Silicon Technology LLC v. GlobalFoundries 2022**
 - IPR2022-01083
- **Ericsson v. Apple** Brazil Patent BRPI 9811639-8 filed 2022
- **Greenthread v. Intel** Case 6:22-cv-105-ADA filed 12/2022
- **ITC Daedalus v. TSMC** Case 337-TA-1336 filed 10/2022
- **Oasis Tooling, Inc v. GlobalFoundries** C.A. No. 22-312-CJB 3/2023
- **BiTMICRO LLC v. Intel** IPR2023-00781 filed 3/31/2023
- **Longitude Licensing LTD, v Western Digital Technologies, Inc.** IPR2023-01286 filed 8/08/2023

D. Honors and Awards

- ❑ 100 granted US patents, 60 publications and 1 book on semiconductors
- ❑ Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- ❑ Elected to Intel Fellow in 2003
- ❑ Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- ❑ 2008 SEMI award North American Recipient
- ❑ 2014 TiE 50: Top Startup (SuVolta)

- ❑ 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- ❑ 2011 EuroAsia IC Industry Award for start-up
- ❑ 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

E. Publications/Patents

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