

THIN FILMS

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Edited by
Maurice H. Francombe

Volume 1



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Thin Films

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Volume 28

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VOLUME 28



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Preface

Volume 28 of the book series *Thin Films*, titled *Frontiers of Thin Film Technology*, focusses primarily on recent developments in those technologies that are critical to the successful growth, fabrication, and characterization of newly emerging solid-state thin film device architectures. The device structures considered include not only the dominant and rapidly evolving semiconductor integrated circuit components, but also structures that depend for their function upon novel photonic properties, as well as superconducting, magnetic, and ferroelectric behavior.

The nine review articles included in this volume have been selected from a new five-volume work, *Handbook of Thin Film Devices*, now being prepared for publication by Academic Press. This handbook, from which the chapters are drawn, provides a comprehensive, multi-topical scientific and engineering source embracing key aspects of a field that is basic to all commercial, defense, and space high-technology systems. *Thin Films Volume 28, Frontiers of Thin Film Technology*, is a condensed sampler, authored and edited by well-known experts, and offered in a convenient format for use by professional scientists, engineers, and students involved with the materials, design, fabrication, diagnostics, and measurements aspects of these important new devices.

In Chapter 1, Ian T. Ferguson, Alan G. Thompson, Scott A. Barnett, Fred H. Long, and Zhe Chuan Feng address the strengths and weaknesses of the modern non-equilibrium epitaxial methods of MBE and MOCVD for semiconductor compound growth and techniques for characterization of quality and parameter control and feedback. The more advanced devices now emerging can use the different properties caused by varying the composition or elastic strain of the epitaxial layer to effect changes in bandgap, refractive index, or carrier concentration. In addition, growth of very thin layers and quantum confinement have facilitated precise modification of electronic properties of compound semiconductor structures. This chapter provides a broad overview of the growth and characterization approaches needed for epitaxial III-V structures used in fabrication of superior high electron mobility transistors (HEMTs), Hetero-bipolar transistors (HBTs), and optical devices.

Prashant Chavarkar and Umesh Mishra illuminate the important technologies and performance possibilities of FETs and HEMTs in Chapter 2. HEMTs, which use the two-dimensional electron gas (2DEG) as the current conducting channel, have proved to be excellent candidates for microwave and millimeter wave analog

applications and high-speed digital applications. The authors stress that to optimize performance it is crucial to understand the principles of device operation, to consider the effect of scaling in designing a microwave or millimeter wave HEMT device, and to appreciate the advantages and limitations of the materials system involved.

Chapter 3, by C.E.A. Grigorescu and R.A. Stradling, reviews the status of antimony-based infrared materials and devices previously confined mainly to defense (imaging and tracking) scenarios in the mid-wavelength MWIR (3–5 micron) spectral range. Thin film research studies, for example, of strained superlattices and of metastable alloy compositions, have led to Sb-based detector structures demonstrating IR sensitivity extending into the long wavelength LWIR (8–12 micron) range. Both detectors and emitters are discussed, covering the basic device physics and mechanisms limiting the performance as well as materials properties.

HgCdTe (mainly as a photoconductor) has long been the incumbent detector technology for military and space applications, ranging in wavelength from 2 to beyond 16 microns. Chapter 4, by Arvind D'Souza, Priyalal Wijewarnasuriya and John Poksheva, gives a summary review of this technology, covering the aspects of material preparation, junction-device characteristics, photovoltaic architectures, and recent developments in focal plane arrays (FPA). Over the last decade, with significant developments in Europe and the US in low-temperature molecular beam epitaxy (MBE), HgCdTe has advanced substantially as a large area FPA technology, with device producibility and uniformity ensuring its dominant presence in the high-end IR market.

The growth and characterization of the thin films and multilayers needed for low- and high- T_c superconducting devices is described by Chang-Beom Eom and Jim Murduck in Chapter 5. Since this area serves as the foundation of the device process, the authors give a careful overview of the growth techniques, discussing strengths and weaknesses as well as the standard characterization tools needed to validate the film's properties before continuing to a device fabrication phase.

In Chapter 6, Jim Murduck presents the guidelines for device fabrication for the standard materials used in industry: niobium, niobium nitride, and $YBa_2Cu_3O_7$. The layout of the standard processing and analysis steps to insure high quality devices are laid out, as well as discussing the difference in the state of the art for the low and high T_c production lines.

Ferrite devices play a key role in most microwave and millimeter wave systems where they provide duplexing, isolation, switching, phase shifting and power limiting functions. While much effort has been directed towards the size reduction and integration of active semiconductor devices, relatively little work has been directed towards achieving comparable size and cost reductions for ferrite devices. Douglas Chrisey, Paul Dorsey, and J. Douglas Adam provide an overview of recent developments in microwave magnetic film devices in

Chapter 7. Approaches used to deposit ferrite films are reviewed and compared, and the state of the art in the formation of garnet, spinel, and hexaferrite films is described. This chapter concludes with a detailed description of exploratory work on the integration of ferrite film devices with semiconductors. Although several problems remain to be solved, thin film ferrite devices appear attractive for millimeter wave applications in communications and radar systems.

In Chapter 8, S.B. Krupanidhi provides a comprehensive review of preparation and characterization techniques used in developing ferroelectric thin films for device applications. Deposition methods, uniquely suited to the controlled fabrication of such films, employ either physical growth with low energy bombardment (e.g. magnetron sputtering from a single or multiple target source, multi-ion beam reactive sputtering, and pulsed laser ablation) or chemical routes that involve no such bombardment (e.g. sol-gel, chemical vapor deposition, and metal organic chemical vapor deposition). The structure processing relationship of some ferroelectric oxide films that are being developed for high-performance memories and microelectromechanical systems (MEMS) are described. Finally, the reader is provided with a useful summary of the key techniques employed in electrical characterization of ferroelectric films for device applications.

Practical realization of stable, high-performance ferroelectric random access memories (FeRAMs) also depends critically on successful control of integration and processing parameters. Chapter 9, by Deborah Taylor, addresses the important issues related to the design and fabrication of the memory cells that are implemented in high-density FeRAMs and ultra-dense DRAMs. Among the items discussed are approaches for forming and patterning the capacitor stack, the damaging effects that hydrogen-containing ambients have on ferroelectric capacitors, the impact of ferroelectric processing on the silicon devices, and equipment issues for the commercial manufacturing of ferroelectric film memories. Finally, the author presents a summary and an outlook on the future of these ferroelectric film memories, which have the potential to capture a larger share of the total memory market, estimated for 1999 to be worth over \$60 billion.

Maurice H. Francombe

Thin Films

Frontiers of Thin Film Technology

Volume 28

Fabrication of Superconducting Devices and Circuits

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The insertion of superconducting circuits as a technology has been only as successful as the capabilities developed to fabricate these circuits. Clearly, the greatest strides in circuit demonstration have been taken using niobium-based integrated circuit (IC) fabrication where IC technology has matured to support large-scale integration levels ($\sim 10^6$ gates/cm²). To successfully fabricate large-area and dense IC, stable and reproducible processes are needed. Moreover, IC fabrication involves a number of subprocess steps. Each step has its own inherent variability, the combination of which contributes to the overall degree of circuit functionality, or yield. Fabrication groups face challenges in reducing variability or spreads in critical device parameters such as junction critical currents, values of inductance, and layer-to-layer alignment. In addition, there are design-driven needs to reduce device dimensions and parasitic inductances that put further constraints on practical circuit fabrication.

These challenges are multiplied in IC fabrication using ceramic high-temperature superconductors (HTS). Also there are inherent material issues in this family of superconductors such as maintaining film epitaxy and environmental sensitivity. As a result, the aforementioned fabrication issues are even more daunting. Current HTS circuit fabrication requires an increased understanding of the relative importance of topology and film morphology in vital circuit elements. This is the case in multilayer process elements such as interconnect crossovers,

layer-to-layer vias and Josephson junctions, where trade-offs often exist between ease of fabrication and requirements for applications. Despite the increased challenge, if these material and processing issues can be successfully implemented, it would allow more compact, lower-power systems, making them increasingly attractive for applications.

In this chapter, the emphasis will be on the practical aspects of active-device superconductor fabrication, especially with respect to their relationship to system application. Present limitations will be noted along with the future direction of the field necessary to allow insertion of superconducting IC technology into commercial systems.

6.1 Introduction

6.1.1 A BRIEF HISTORY

The history of Josephson junction fabrication began in 1963 with the experimental confirmation of the Josephson effect by Anderson and Rowell [1, 2] at Bell Laboratories, one year after Josephson's theoretical predictions [3]. These rudimentary thin-film devices were the precursors of today's superconducting integrated circuit processing. The fabrication of these first junctions was accomplished by producing a thin strip of tin on a glass slide through a metal mask, heating the tin in an oxygen atmosphere to create an oxide barrier and then overlaying with a thin strip of deposited lead. A useful barrier thickness in these devices is on the order of 1 to 2 nm and must completely cover the area between the electrodes, which can range from a few to dozens of square microns. This coverage is proportionally equivalent to an area the size of a football field being perfectly covered with less than 1 cm of snowfall. With these extreme dimensional requirements it is apparent that the underlying base electrode must be smooth and the barrier growth nearly perfect to enable this device fabrication.

Early efforts to fabricate these thin-film junctions were so time-consuming and plagued with yield issues that alternate methods of creating Josephson junctions were quickly developed. One such method, point-contact, was introduced and consisted of a niobium screw contacting a superconducting plate also made of niobium [4] that could be mechanically adjusted to the desired junction parameters. These mechanical devices found their way into some of the earliest commercial products utilizing superconductivity and were integral to device fabrication understanding throughout the 1970s. Clearly, however, fabrication of larger circuits must be done in a monolithic fashion. Considerable advancement was made in thin-film fabrication of Josephson junctions in the 1970s due primarily to IBM's 100-million dollar, 14-year effort to create a computer based

on Josephson effects. The junction materials of choice at the start of that project were lead and lead alloys. Researchers at IBM found that with the addition of indium and gold to the lead, smoother base electrodes could be deposited allowing more complete oxide barrier coverage. With barriers on the order of 10 atoms thick, coverage of the base electrode will be a theme repeated in whatever material system is used for fabrication. These lead alloy junctions allowed for a remarkable degree of control over junction parameters and were integrated with resistors and superconducting interconnects in monolithic integrated circuits. However, lead films stretch inelastically when cooled to liquid helium temperature and upon warming to room temperature create mounds that rupture the native oxide tunneling barrier [5]. Even with these limitations, Jaycox and Ketchen [6] successfully fabricated a monolithic dc SQUID by integrating lead alloy junctions with other IC elements such as resistors and an input coil that requires multilayer elements such as crossovers and vias.

Ultimately, the materials limitations of lead alloy junctions helped define and spur research for more robust materials. With a T_c of 9.2 K, niobium was considered an attractive candidate material. However, there were a number of difficulties that had to be resolved before it could be used as a junction electrode. As a refractory metal, niobium has a melting point above 2400 °C making it impractical to be deposited by thermal evaporation as lead alloys had been. In addition, niobium readily oxidizes and for every 1% oxygen concentration in a Nb film, the T_c is reduced by 1 K. Typical vacuum systems at the time had insufficient base pressures to prevent degradation of the critical temperature of the deposited niobium films. The resolution to both these issues is found in what is today's standard deposition equipment. Niobium is sputter-deposited, usually with a dc magnetron source, in vacuum systems capable of ultrahigh vacuum. Prior to the termination of the IBM Josephson computer program, niobium was introduced as a base electrode.

With niobium, researchers had a material that was mechanically hard, could be thermally cycled, and had T_c significantly above liquid helium. However, barrier deposition on niobium base electrodes was still problematic. Although niobium readily oxidizes, it can form various oxides and in practice was difficult to control. It was left to Gurvitch *et al.* [7] at Bell Laboratories to put the final piece in the puzzle. Rather than rely on niobium's native oxide, a thin layer of aluminum was deposited on the niobium and then oxidized. The aluminum is deposited thin enough (~5 to 10 nm) to be superconducting through the proximity effect. Aluminum has the attractive properties of both wetting (completely covering) niobium well and having a self-limiting oxide making controllable barrier fabrication possible; Nb/Al/AIO_x/Nb junctions continue to be the *de facto* standard for Nb IC processing.

In circuit fabrication in general there is often a competition between the ease of fabrication and capability of circuit operation, and superconducting circuit

fabrication is no exception. One distinctive burden to insertion of superconducting electronics is the required cryogenic cooling. After the establishment of the Gurvitch process in Nb, the superconductor electronics community continued to search for materials that could be used for large-scale integration (LSI) superconducting circuits that operate at higher operating temperatures. As will be seen, materials have been developed that can reduce this burden of cooling but at the cost of significant complexity in manufacturability.

6.1.2 Nb, NbN AND YBCO MATERIAL COMPARISON

Specifically, we will examine three processes: niobium as the most mature process; NbN with its nearly $2\times$ improvement in T_c ; and YBCO with its $10\times$ improvement in T_c . As these are the three material systems that are primarily being pursued for integrated-circuit fabrication, we will focus our consideration on these technologies and their issues. The goal is to examine these processes in terms of what they can currently achieve and to consider the materials-specific issues that are limiting them.

These three-materials systems provide an interesting progression of properties which in turn impacts circuit fabrication. From niobium to niobium nitride to YBCO is a progression from a metal to a semi-metal, to a ceramic. The transition temperatures also vary dramatically from 9.2 K for niobium, to 16 K for niobium nitride, and to 90 K for typical YBCO.

The coherence length, a characteristic length scale associated with the superconductor, varies in these materials from 30 nm in Nb to 5 nm in NbN. In YBCO, which is anisotropic, the coherence length is 2 nm in the a - b plane and 0.2 nm along the c -axis. Since junction characteristics are greatly influenced by the properties of the superconductor within a coherence length of the barrier, for junction fabrication it is critical that the film properties within a coherence length of the barrier be as optimal as possible.

Ideally, one would want a perfectly ordered superconductor within the base electrode up to the very surface of the barrier and perfectly recommencing at the opposite surface of the barrier. In reality, when films are grown, there is disorder at the interface due to imperfect lattice matching or reactive chemistry. As the film is grown there is a characteristic thickness where the bulk properties of the crystal are re-established. Materials with longer coherence lengths allow for a wider disordered region next to the barrier without degrading the junction characteristics. Considering the coherence lengths of our three superconductors and the distances from the barrier necessary for reasonably good superconducting properties to be regained in a given superconductor [8], one can gain some insight into the relative difficulty of making controllable Josephson junctions in these three material systems (Fig. 6.1). Note that for the case of niobium, greater than

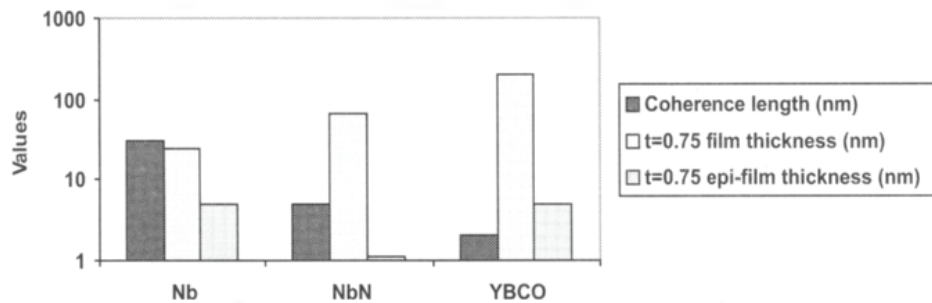


FIG. 6.1. Comparison of parameters of the three material systems used for superconducting circuit processes. $t=0.75$ film thickness is the minimum thickness at which the film T_c reaches 75% of its bulk value.

75% of the film critical temperature has been regained in a distance less than the coherence length in that material (Fig. 6.1). This distance is reduced by epitaxial deposition of niobium. For NbN, the film thickness necessary to regain 75% of the bulk T_c is dramatically affected by film epitaxy as is the case for YBCO. For epitaxial film growth the distance necessary to regain the maximum critical temperature in niobium is 5 nm and for niobium nitride it is less than 1 nm; for YBCO it is 5 nm. By comparing the distance necessary to regain good superconducting properties to the distance that the junction parameters are affected by disorder, one can see the necessary strategy for fabrication. For niobium junctions, nonepitaxial niobium deposition on the aluminum oxide barrier has been as successful as one would expect from a comparison of the relatively large coherence length with respect to the thickness necessary to regain reasonable T_c (Fig. 6.1).

However, for NbN fabricating oxidized aluminum barriers produces junctions with degraded junction parameters such as reduced gap voltage. Replacing this barrier with the refractory insulator MgO dramatically improves the quality of the NbN junction due to superior lattice matching. MgO, which also has a B1 structure, has a lattice mismatch of only 4% with NbN. Talvacchio *et al.* [9] have observed using reflection high-energy electron diffraction (RHEED) that rf-sputtered MgO barriers grow initially epitaxially on NbN, although diffuse diffraction spots in low-energy electron diffraction (LEED) analysis suggested that these films were rough. This is consistent with LeDuc *et al.* [10] who proposed that the initial layer of MgO film grows in a planar epitaxial fashion. Subsequent MgO film growth proceeds by nucleation resulting in islands that account for the film roughness. This Stanski-Krastanov [11] epitaxial growth mode occurs when the initial monolayer of deposited film has a lower surface energy than the material upon which it is being deposited. This lowering of

surface energy can dominate strain energy resulting from lattice mismatch. Subsequent deposition of a monolayer does not reduce the surface energy further and island growth proceeds because it minimizes strain energy. In contrast to these results, Shoji *et al.* [12] reported that MgO was observed to form amorphously on NbN. However, the difference in these results may be due to a lower substrate temperature during deposition. Transmission electron microscopy (TEM) analyses [13, 14] of another well-matched barrier material (AlN) also suggests that epitaxial growth can be continued through the dielectric barrier.

Finally, it is apparent from Fig. 6.1 that even with strict epitaxy of the YBCO junction electrodes through the barrier, junction parameters may still be degraded. This is due to the film thickness necessary to regain near-bulk values of T_c being significantly larger than the coherence length in this material system.

6.1.3 Nb, NbN AND YBCO FABRICATION PROCESSES

The choice of material for superconducting IC fabrication is driven primarily by the temperature requirements of a given application. In general, superconducting circuits benefit from as low a temperature of operation as possible. Thermal noise is reduced, penetration depths decrease, and a parameter such as junction critical current becomes less sensitive to thermal variation. This must be balanced by the difficulty and inefficiency of fighting this entropy-reducing battle.

Due to the success and universal acceptance of the Gurvitch-style Nb junction, what distinguishes the various foundry and foundry-like efforts in niobium processing is typically other aspects of the circuit process. Although NbN circuit fabrication is not as common worldwide, there are ongoing efforts directed at developing aspects of NbN junction fabrication. The YBCO circuit processing represents the other extreme, where the junction process is very much in flux and there are nearly as many junction processes as there are groups researching their fabrication (Table 6.1).

6.2 Nb Circuit Process

6.2.1 INTRODUCTION

Much of the success of superconducting circuitry in recent years has occurred using niobium circuitry [41, 42] resulting in a number of material-specific advantages. Niobium has the desirable properties of a relatively long coherence length and relatively short penetration depth compared to most other type-II superconductors. This permits a control of Josephson junction properties impor-

TABLE 6.1
VARIOUS SUPERCONDUCTING CIRCUIT PROCESSES UTILIZING Nb, NbN AND YBCO

Circuit process	Institution	Ref.	Dielectric	Resistor	Ground-plane	Comments
Niobium process	ETL	[15, 16]	Nb ₂ O ₅ , SiO ₂ , MgO	Pd	bottom	
	Hitachi	[17]	SiO	MoNx	bottom	
	Hypres	[18, 19]		Mo	bottom	
	NEC	[20, 21]		Mo	bottom	4.74 μ m Nb jj ($1 - \sigma = 0.54\%$) 0.74 μ m Nb jj ($1 - \sigma = 4.8\%$)
	NIST	[22, 23]		Pd-Au	bottom	Developing Pd-Au barrier SNS junctions
	Northrop-Grumman	[24]	Sputtered SiO ₂	Mo/Ti	top	
	PTB	[25, 26]		Pd	bottom	
	TRW	[27]	Bias-sputtered SiO ₂	Mo, NbNx	bottom	
	UC Berkeley	[28]	ECR PECVD SiO ₂	Mo	top	$1 - \sigma < 0.2\%$ Nb jj I_c for chip $1 - \sigma < 0.7\%$ Nb jj I_c for 4" wafer
	Univ. Karlsruhe	[29]		Pd/Al	bottom	
Advanced niobium process	MIT Lincoln Labs	[30]	PECVD SiO ₂	Ti/Pt		DPARTS, <i>i</i> -line photolithography, 150-mm wafers
	SUNY, Stony Brook	[31]	SiO	Au, Pd-Au		PARTS, electron beam lithography
	NEC	[32]	Bias-sputtered SiO ₂	Mo		ECR-etching, <i>i</i> -line photolithography
Niobium nitride process	CEA-Bremable	[33]	SiO ₂ , Si ₃ N ₄			MgO buffer
	Hypres	[18]				NbN/Mg/NbN (SNS)
	Kansai	[34]		Au		NbN/AlN/NbN
	TRW	[35]		Mo, NbNx	bottom	NbN/MgO/NbN
YBCO process	Conductus	[36]	SAN		bottom	IEJ, Co-YBCO edge, bi-crystal
	DERA	[37]	PBCO			CAM jj
	MagnaSensors	[38]	SrTiO ₃		bottom	Metallic SNS jj
	Northrop-Grumman	[39]	SrTiO ₃ , SAT		top or bottom	Co-YBCO edge jj
	TRW	[40]	SrTiO ₃ , SrTiO ₃ /SAT/SrTiO ₃	Mo/Ag	bottom	Co-YBCO, Ga-PBCO edge jj

tant to circuit design such as critical current I_c , and junction quality V_m . Even with the more forgiving properties of niobium, the critical current is still highly dependent on the insulating barrier material and the process used to fabricate it. In addition, as a refractory material Nb is quite hard and generally adheres well as

a film. Moreover, Nb is typically grown as a polycrystalline film and is not particularly dependent on the crystallinity of the substrate.

In many respects, niobium-based circuit processing stands on the shoulders of previous work done in the semiconducting industry. Techniques such as reactive ion etching and photolithographic processes that had been developed for silicon-based processing have direct application in superconducting circuit processing. Even the wafers that are used for niobium technology are the same as those found in semiconductor foundries, the high quality of which is due to the tremendous demand in the semiconductor industry.

6.2.2 PROCESS FLOWS

Fabrication process flows are typically a meld between application requirements and the practical reality of being able to deposit and define metals and dielectrics to realize those requirements. Fortunately, a given process flow that may have a groundplane, a junction layer, a resistor layer, and a couple layers of superconducting interconnects, is flexible enough to fulfill many of the requirements imposed by various superconductor applications. The particulars of how a process flow is accomplished has been the center of quite a bit of inventiveness by researchers throughout the world. However, there is an advantage for those designing superconducting circuitry in standardizing the fabrication process.

Sharing design modules has emerged as one of the strategies for sharing a process flow and process parameters in a given technology. This has begun for fabricating single-flux quantum (SFQ) circuits [43] but is quite process-flow specific (Fig. 6.2). However, the advantages to the designer may be so significant that careful consideration should be given to developing advanced process flows with this in mind.

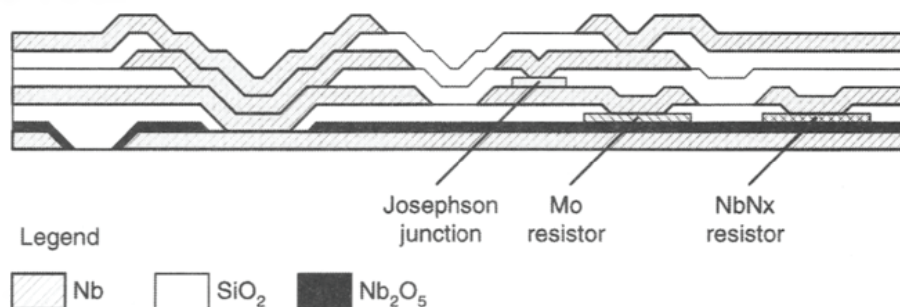


FIG. 6.2. Cross section of niobium process flow from TRW standard Nb-based junction process from Reference [44].

One process flow, SNAP (selective niobium anodization process), is an example of how a given process flow can be realized with a minimum of processing complexities while allowing as much robustness in the process as possible. The SNAP takes advantage of niobium's capability of forming an anodic oxide by simply exposing a photolithographically defined sample to an electrolytic solution of ammonia pentaborate, ethylene glycol, and de-ionized water (31:224:152) with a dc voltage applied to the niobium layer. This approach works well to form a dielectric with high dielectric integrity. However, it is difficult to extend this process to smaller junction sizes due to the isotropic nature of the wet processing along with the stress induced by the formation of the anodic oxide.

A myriad of processing techniques have been invented that address aspects of circuit processing such as ease of fabrication, planarization, reducing junction size and relieving film stress as indicated in Table 6.2. These techniques vary also in their degree of planarization. For example, chemical or mechanical polishing achieves a high degree of planarization resulting in a nearly planar surface for subsequent depositions.

The capabilities of a superconductor IC fabrication process go well beyond the performance of junctions or any other single circuit element. A given process can be subdivided into numerous processing elements such as junctions, resistors, interconnects, vias, and the necessary dielectric to isolate these structures. Each one of these elements may consist of dozens of submodule steps, all of which must be performed adequately in order to ensure successful circuit fabrication. Process details concerning dielectric integrity, contact resistance, critical current of interconnects, bridging between layers, opening of lines, insufficient clearing of dielectric, overetching of critical layers, resistor targeting, proper sizing of photoresist structures and the subsequent etching or lift-off, sufficiency of layer-to-layer registration can and does occupy much of the efforts of those maintaining a superconductor IC foundry. As any of these issues can negate the considerable time, effort, and expense that goes into a circuit fabrication, much attention is paid to increasing the yield of each step in the circuit-fabrication process.

In order to track the numerous subprocesses involved in a single wafer fabrication, techniques such as statistical process control (SPC) are utilized. A given process element can be evaluated over time to determine if a process is varying due to random variation or whether a systematic problem has arisen. A series of statistically derived rules (Western Electric rules) readily formalized this procedure. In practice, tracking metrics that are readily measurable and pertain to critical aspects of the process are most desirable. Film thicknesses and film resistivities, parameters critical to successful circuit operation, can be tracked in-process.

Film inductance is an example of a parameter vital to successful circuit operation which is difficult to measure until after a wafer has completed

TABLE 6.2
PROCESS TECHNIQUES APPLIED TO NIOBIUM-BASED CIRCUIT FABRICATION

Reference	Processing technique	Degree of planarization	Description
[45]	CLIP (Cross-Line Patterning)	Low	Provides good scaling to small junction dimensions. Cumbersome geometry for design.
[32]	MPP (mechanical-polishing planarization)	High	Neutral slurry to reduce SiO_2 etch rate for controllability. $0.24\text{ }\mu\text{m} \times 0.24\text{ }\mu\text{m}$ junctions demonstrated.
[31, 46]	PARTS (planarized all-refractory technology)	High	Uses chemical-mechanical polishing. $0.08\text{ }\mu\text{m} \times 0.08\text{ }\mu\text{m}$ junctions demonstrated.
[47]	RHEA (Resist-Hardened Etch and Anodization)	Medium	A modified SNAP that allows a greater degree of planarization.
[48]	SAWW (Self-Aligning Whole Wafer)	Low	Addresses stress-induced degradation of small junctions.
[49]	SCAN (Self-aligned Contact with Anodized Niobium)	Medium	Uses anodization to define junction and allow outside contacts in addition to dielectric other than Nb_2O_5 .
[50]	SNAP (Selective Niobium Anodization Process)	Medium	Uses anodization to define junction and allow outside contacts. Considerable anodization makes small-area junction definition problematic.
[51]	SNEP (Selective Niobium Etch Process)	Low	Further developed by Yuda <i>et al.</i> [52] to include lift-off as a stress-relief mechanism.
[53]	SNIP (Self-aligned Niobium Isolation Process)	Medium	Deposits SiO as the self-aligned dielectric after the counterelectrode etch.

fabrication. As such, correlating inductance measurements with film thicknesses and resistivities allows one to respond more quickly to process drift that could result in ill-targeted inductance values.

The insensitivity of process characteristics to inevitable variations that occur in wafer fabrication often determines the success of circuit fabrication. An increasing number of groups [54, 55, 56] are employing statistical techniques of process development that have been more commonly applied in the semiconducting industry in order to develop increased robustness to variation.

6.2.3 PROCESS ELEMENTS

Critical to fabrication of a niobium circuit is the quality of the film deposition. Details of superconducting film deposition have been reviewed in Chapter 1. In this section, other elements necessary to put the superconducting films into useful circuitry will be discussed.

6.2.3.1 Junctions

As discussed earlier, the Gurvitch-style Nb junction has been key to enabling medium-scale integration (MSI) and then LSI-scale superconductor IC fabrication. These Nb junction techniques are still being developed. Vital to circuit operation are high-quality junctions with low leakage current and small junction-to-junction critical current variability. In addition, reduction of junction size and capacitance while maintaining parameter reproducibility and uniformity across ever larger wafer areas is an ongoing need in order to meet the next generation of IC applications.

As is often the case in fabrication, a deposition system-specific characterization must be made to assess the system geometry effect on the particulars of the film process. With that proviso, it is still illustrative to consider the practical aspects associated with a given Nb junction fabrication and understand how a basic process is developed.

- 1) A High-quality Nb film deposition process must first be developed (as outlined in Chapter 1); depositing nearly stress-free films is vital to high-quality device fabrication. This is especially true for fabrication of small-area junctions ($<2.5\ \mu\text{m}^2$) as reported by Nakagawa *et al.* [57]. Once patterned, stress relaxation can result in damage to the junction edges and in increased junction leakage current. The effect of this stress can be reduced, but not eliminated, by choice of a junction-patterning technique (Table 6.2).
- 2) During junction base-electrode deposition, wafers should be kept sufficiently cool during deposition so as to control grain growth and to keep the film surface reasonably smooth. Due to the excellent wetting and oxidation of the overlying aluminum layer this roughness is not as critical as it is in the case of NbN or YBCO processing. The resulting aluminum oxide barrier is typically smoother than the Nb base-electrode surface.
- 3) Al is deposited after the base-electrode deposition. Other materials have been explored for this purpose such as Yb [58] and Ta [59], however, Al remains the most common material of choice.
- 4) Al thicknesses greater than 4 to 8 nm can reduce gap voltage, but thicknesses much less than 4 to 8 nm can result in catastrophic loss of

- yield. Increasing the deposition rate of the Al is one method to improve the crystallinity of the Al film and reduce junction leakage.
- 5) In post-Al deposition, the sample is oxidized preferably in a separate chamber that is kept under vacuum in order to avoid a partial pressure of water that can cause wafer-to-wafer reproducibility issues. For targeting purposes, it is critical that the pressure, time of oxidation, and substrate temperature be well controlled. A strength of this junction process is that by simply controlling these parameters, junction critical current densities from less than 1000 A/cm^2 to greater than $400,000 \text{ A/cm}^2$ can be targeted.
 - 6) These barrier fabrication steps can be repeated *in situ* to obtain ultralow critical-current densities ($J_c = 5$ to 200 A/cm^2) [60].
 - 7) The niobium counterelectrode is then deposited making sure that the oxygen from the thermal oxidation chamber is sufficiently evacuated. The counterelectrode thickness should be enough to allow some measure of overetch of the via through the dielectric and into the counterelectrode without endangering the few tens of nanometers near the barrier.

High-critical current densities are desirable for many applications. This is due to the characteristic frequency that can limit device operation following the relation:

$$w_j = \{(4\pi e/h)\beta_c J_c (A/C)\}^{1/2} \quad (6.1)$$

where β_c is the McCumber parameter; A is the junction area; and C is the junction capacitance. This limiting frequency can be extended by increasing the junction critical-current density. In order to obtain device-operating frequencies in the hundreds of gigahertz to THz, critical-current densities in the hundreds of kiloamps/centimeters square are needed. For the Nb/Al/AlO_x/Nb system, barrier thicknesses on the order of 1 nm are needed. This equates to ~ 3 monolayers of the AlO_x barrier, thus making it susceptible to film roughness and microshorts. These microshorts can consist of unit-cell-sized metallic defects in the oxide structure. A single monolayer reduction equates to greater than one hundred times the conductance and is thought to dominate the conductance of high- J_c junctions [61]. In practice, junction critical-current densities of greater than 400 kA/cm^2 have been demonstrated by simply limiting the oxygen exposure of the aluminum barrier without severe degradation of the junction I-V characteristics.

An alternate barrier material, aluminum nitride, has been explored as a candidate barrier for controllable high- J_c junctions [62]. Unlike oxidation, the nitridation of aluminum proceeds much more slowly and can be accomplished by exposure to a nitrogen plasma. Junctions fabricated in this fashion have reduced subgap leakage and hold the promise of greater control of junction critical-current density targeting.

6.2.3.2 Dielectric Depositions

Dielectric films are needed in superconducting circuitry for a number of purposes and these films impact to varying degrees capacitance, inductance, isolation, and device-to-device crosstalk. On a microscopic scale, most dielectric films used in IC processes are amorphous and are generally insensitive to considerable variation in stoichiometry. Polycrystalline films are usually avoided as they tend to be leak more [63].

Early superconducting circuitry used thermally evaporated SiO dielectric layers. De-adhesion and pinhole shorts made this dielectric problematic. Although Nb junctions are limited to processing temperatures less than 200 °C due to concerns of altering junction parameters, there have been numerous dielectrics developed by the semiconducting industry that are applicable to Nb circuit processing. A measure of how well a dielectric film serves as an insulator is the calculated dielectric defect density D as defined by the Poisson distribution:

$$Y = \exp(-DA) \quad (6.2)$$

This can be determined by measuring the fractional yield Y of nondefective planar capacitors of area A . Low-temperature (<150 °C) PECVD Si₃N₄, Nb₂O₅, ECR PECVD SiO₂ [64] and bias-sputtered SiO₂ (Fig. 6.3a) are all methods that can provide dielectric integrity of less than 1 defect/cm² and a degree of planarization to improve subsequent coverage of superconducting interconnects.

Single crystalline films often require too high a temperature to be readily fabricated and are critically dependent on stoichiometry, and consequently, they are not common. The exception to this is in high-temperature superconductors due to the requirement of continued epitaxial film growth through the dielectric layer in a multilayer process.

For Nb and NbN IC processing the following list of specifications should be considered in choosing a useful dielectric material:

- 1) complete wetting of the dielectric on the material that is to be insulated. (Note that unlike semiconductor circuitry a single “pinhole” can represent a zero-resistance superconducting short between layers.);
- 2) good adhesion to the adjacent films above and below;
- 3) low film-stress (which can affect adhesion, loss tangent);
- 4) stable chemistry. If an oxide, it should not have a greater affinity towards oxygen than niobium oxide or long-term diffusion will be an issue;
- 5) it should be insensitive to moisture in order to allow standard aqueous processing techniques;
- 6) amorphous; and
- 7) leaves a consistent and smooth surface as a template for subsequent depositions.

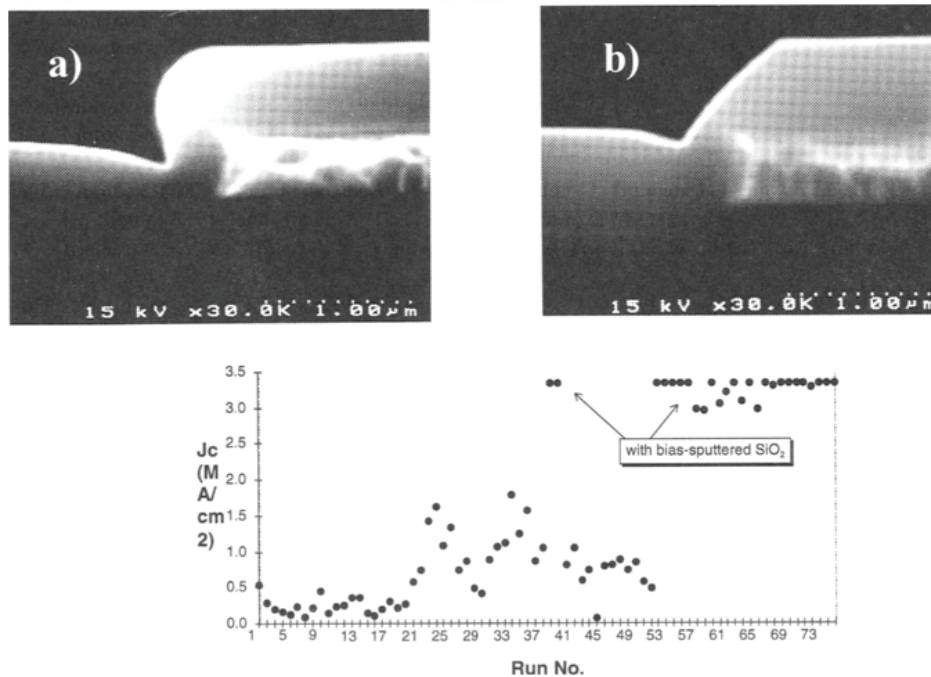


FIG. 6.3. Bias-sputtered SiO_2 demonstrating partial planarization (a) along with a trend chart indicating the increase in critical current of the interconnect crossovers (b) from Reference [35].

This last point is especially significant in maintaining consistent properties of layers that are deposited on the dielectric. For example, thin-film resistors can vary in resistivity as a function of the roughness of the underlying film, thus it is critical in developing a process to have a consistent surface from wafer to wafer.

6.2.3.3 Resistors

Thin-film resistors predate thin-film junction technology by over 40 years [65]. The maturity and relative simplicity of resistor fabrication belies its critical role in superconducting circuit fabrication. It is often the case in digital circuit fabrication that targeting and variability in resistor values is of equal significance to junction critical-current targeting and variability. Resistor materials currently in use with superconducting circuit processes include Mo, nitrogen-deficient NbN, MoN_x , Mo/Ti, Pd, Pd-Au, Pd/Al, Ti/Pt, Au, and Pd-Au.

Resistors can occupy over half the “real estate” in many SFQ circuits, and as such, directly impact circuit density and performance. This circuit element has its own parasitic inductance and capacitance associated with its geometry that must be considered. In addition, simply by the area it occupies, it lengthens the

interconnects necessary to connect one gate to another, thus increasing circuit latency. Directly reducing the resistor dimensions becomes impractical at some point as vias of finite size are needed to connect it. In addition, as the resistor size decreases, the variability of the resistor values increases due to fluctuations of the critical dimension. In other words, a 0.1- μm variation in linewidth means little in a 10- μm -wide resistor (1%) whereas this variability in a 1- μm width creates an intolerable 10% resistance variation.

Resistors are generally used for two purposes in digital circuitry: as shunting resistors in parallel with junctions, and as bias resistors for the larger circuit. Shunt resistors are needed in Nb and NbN circuitry to sufficiently damp the otherwise hysteretic behavior of the junction I-V characteristics. Generally, the shunt-resistor value is on the order of the resistance of the junction in the voltage state. The dimension of the resistor should be such that its value will be well-targeted in ~ 2 squares of resistor. For smaller dimensions, spreading resistance at the contacts becomes troublesome; for larger dimensions, the resistor incurs excessive inductance and capacitance and occupies too great a circuit area. The other dimension, that is, the thickness of the resistor film, should be sufficiently thick as to be reasonably insensitive to small variations in surface roughness, but not so thick as to add topological concerns of step-coverage in order to contact to it. Typical resistor thicknesses range from 50 to 300 nm for these reasons.

It may not be desirable for the aforementioned reasons to form all resistors out of the same material. Often, digital circuits require resistances on the order of a couple of ohms to shunt junctions and bias resistors on the order of tens of ohms. The same resistor to satisfy both these disparate requirements would be awkward from a design perspective.

Alternate approaches currently are being explored [66] to entirely integrate the resistor with the Josephson junction. One such approach is the development of superconductor/normal-metal/superconductor, or SNS junctions, and alternately superconductor/insulator/normal-metal/insulator/superconductor, or SINIS junctions [67]. These overdamped junctions could be directly insertable into an SFQ circuit process, and would eliminate the need for a separate resistor to shunt the otherwise hysteretic junctions. This approach is attractive in that it would simplify the overall number of process layers, reduce the circuit dimensions and reduce the inductance associated with the shunt resistor. However, in order to be useful as an RSFQ logic element, normal state resistances of greater than $1\ \Omega$ are desired in order to drive microstrip-line interconnects. In addition, the product of the critical current and the junction resistance, $I_c R_m$, must be sufficiently high to overcome thermally induced errors. Development of these devices is focused on increasing both the junction critical-current density and junction normal-state resistances to levels necessary for future applications. Theoretical treatments suggest that considerable progress can be made in increasing both these parameters from their current values [68].

The prospect of incorporating a separate process element (resistor) into the active device (Josephson junction) is a challenging one. This involves a fundamental change to a device whose properties (I_c uniformity, $I_c R_n$, V_g , V_m) are critical to circuit margin. It should be noted that in combining these two process elements, the designer loses the flexibility of independent targeting of the values of these process elements. For these reasons, it is worth considering whether the same objectives could be accomplished without modifying the active device or losing the option of individually targeting the different process elements. Further miniaturization of the resistor element would support this. However, further miniaturization of the resistor in its planar geometry is limited by the area required to form contact vias. A long-standing approach [69] to this issue that has yet to be fully explored is the use of vertical resistors. This, similar to the SNS-junction approach, would greatly reduce the inductance of the shunt resistor. Depending on the aggressive-ness of its implementation, it could conceivably reduce the circuit dimensions nearly as much as the SNS junction approach. For example, a vertical resistor consisting of a concentric ring connecting the counterelectrode of a circular junction directly to the base electrode is one approach that would be nearly indistinguishable from an SNS junction in circuit area, while maintaining the capability of independent targeting of the separate process elements.

As junction sizes decrease and critical-current densities increase, neither of these process modifications may be needed [70]. At very high critical-current densities, standard SIS junctions become overdamped exhibiting nonhysteretic I-V characteristics and require no further shunting by external or internal resistance. These devices are quantified as having a McCumber [71]-Stewart [72] damping parameter β_c less than one, where

$$\beta_c = \frac{2\pi I_c R_d^2 C}{\Phi_o^2} \quad (6.3)$$

Here, I_c is the junction critical current, R_d is the shunt damping resistance, C is the total shunt capacitance and Φ_o is the flux quantum. For SFQ applications, there is a need for overdamped, nonhysteretic junctions. For a given critical current, as junction size decreases, capacitance will decrease proportionally. In addition, subgap transport mechanisms occur that decrease the shunt resistance to the point that β_c reduces to less than one and no further resistive shunting is needed. The reason that this is not immediately and universally implemented is that this occurs at junction areas of 0.1 to 0.2 μm^2 , which in turn require critical-current densities on the order of 100 kA/cm², both of which stringently challenge current processing capabilities. Attaining these deep submicron dimensions and critical-current densities are just beginning to be demonstrated using planarization techniques [70].

6.2.3.4 Photolithography

Photolithography is a technique common in integrated circuit fabrication that allows precise patterning of thin films into devices. It is based on the application of light-sensitive polymer film (photoresist) that is spun onto a wafer as a thick film, typically 1 to 3 μm thick. Selective areas are then exposed to light through a glass plate with patterned chrome. The exposed photoresist is then developed out similarly to common photographic processes. The remaining polymer is hardened and protects the underlying film during the subsequent etch process. Once the etch is completed the photoresist is removed by dissolution in an acetone bath or commercially available photoresist stripper. Fortunately for superconducting circuit fabrication, the basic photolithography process has been greatly developed by the semiconductor industry and many of the same techniques can be directly applied.

Aspects of this process significant to circuit fabrication are: 1) the minimum feature size resolvable (resolution); 2) the fidelity of the etched feature with respect to the initial design (called the critical dimension, or CD); and 3) the CD variation across the area of the circuit of interest.

These aspects stress circuit yield in varying ways. Minimum feature resolution helps define the minimum size of the active device. In niobium circuitry, the junction size can limit the ultimate speed of operation of a given circuit. The larger the junction, the greater the capacitance and the longer the associated RC charging time constant. Junction size is considerably larger than the minimum feature resolution in processes that do not use self-alignment or planarization. In order to contact the top electrode of the junction, a via must be made through the dielectric overlaying the junction. If any portion of the via overlaps the edge of the junction top electrode, the subsequent interconnect layer will short the top electrode to the bottom electrode. It is vital that the via be correctly aligned to the top of the electrode. Thus the minimum junction size is a sum of the minimum feature resolution of the via and the allowed layer-to-layer registration error.

The layer-to-layer alignment is a critical aspect of circuit fabrication; as seen from the foregoing, it can limit minimum junction size. It can also increase unwanted parasitic inductances and parasitic capacitances in order to ensure interconnects being connected to various process elements. Fortunately, great strides have been taken in this aspect of processing by the introduction of automated alignment equipment. These systems optically recognize designed structures, or optical alignment targets (OAT), and mechanically adjust the mask positioning until alignment is achieved. With the use of this technology, layer-to-layer registration error can be readily reduced to a 3-sigma of less than 0.4 μm . Next-generation photolithography equipment using smaller-wavelength x-rays is purported to allow less than 0.1 μm resolution and a 3-sigma of 0.0054 μm in layer-to-layer alignment [73]. These remarkable advances in photolithographic

technique will only be useful if the capability exists to controllably etch and reproduce those features into the film, as will be discussed in the next section.

Due to variation in the photolithography process the critical dimension may vary. This could be due to exposure and development of the photoresist or etching of the structure in question and much effort goes into precisely controlling this aspect of the process. It is not obligatory that the critical dimension is precisely the same dimension as the device size on the mask, but that it is simply consistent from process run to process run. It is quite common that an offset, or sizing, is added to the original design in order to account for the shrinking or growth of the structure size during the processing. Clearly, this offset can limit the ultimate dimension for extremely small structures. The control of the critical dimension impacts circuit yield in a fashion similar to parameter value targeting.

In practice, the variability of the critical dimension from wafer-to-wafer and within wafer is tantamount to a direct variation in parameter values. It becomes more severe for small-dimension structures. The impacts of CD variation, especially with respect to junction critical current and resistor values, can significantly reduce the margin of circuit operation or entirely prevent operation altogether.

6.2.3.5 Etching

The most common approach to defining the structures in a given layer of niobium-based superconductor IC processes is by reactive ion etching (RIE). Reactive ion etchers accelerate reactive ions formed in a plasma in a parallel plate configuration. The reactive ions have relatively long mean free paths due to reduced operating pressures and are directionalized due to high voltages created by RF biasing of the substrate electrode. This allows RIE to provide anisotropic etching needed for small-feature definition. Thus, CF_4 , or $\text{CF}_4 + \text{O}_2$, will etch anisotropically only for relatively low pressures and high RF power; SF_6 and Cl-based compounds are other reactive gases that are employed especially for fine-line resolution. The plasma created in the RIE dissociates the gas into ions and F radicals which primarily chemically, but also physically, attack the Nb. Ideally, an etch process should selectively etch only the intended film without etching any of the underlying film. Through a combination of chemistry, partial pressures of the gases, and input power used to create the etching plasma, a wide variety of relative etch rates, or selectivity, between various materials can be achieved. Due to across-wafer variation in both the film-deposition technique and the etch-rate profile, regions of the underlying layer will be etched to a greater degree than others. The higher the selectivity between the two materials, the smaller the magnitude of the undesired overetch. An alternate approach to ensure high selectivity is to intentionally insert layers that act as etch stops which are then entirely removed at a later step.

Because perfect selectivity is not attainable and limiting the overetch into the underlying film is desirable, methods of determining when a film is completely etched are employed. Numerous techniques are used that are compatible with reactive ion etching. One is a method is to monitor the spectrum of the light emitted in the plasma by the etched species. As each material emits light in the plasma of characteristic wavelengths, the completion of the etch can be determined by both the reduction of the amplitude of the signal from the film being etched and from the onset of a signal from the underlying film. This schema is successful provided there is enough area on the wafer that is being etched. This is not always the case, especially for dielectric vias. It is not uncommon to purposefully include large fields of film to be etched for no other reason than to increase the endpoint signal amplitude.

The edge profile can be controlled by the addition of oxygen to the RIE plasma. The oxygen serves to recede the photoresist pattern during the etch process, creating a progressively larger etched area and resulting in a sloped edge. This edge is desirable in allowing ordered growth of subsequent layers crossing these edges. Without planarization, the standard approach towards fabricating robust interconnect crossovers and vias is by "sculpting" the underlying layers through lithographic and etch techniques combined with conformal dielectric deposition. This approach is increasingly critical for NbN, a semimetal, compared to metallic Nb presumably due to the ductility on the microscopic level of these films. As will be discussed later, it becomes vital in ceramic YBCO, which has the added complexity of requiring film epitaxy.

In competition with this is the need to create sharp edges that allow minimum-feature resolution. Superconducting circuit processes balance these needs on a layer-to-layer basis. For example, in order to attain minimum-feature resolution, only enough oxygen to prevent polymerization of the photoresist during etch should be used. In contrast, groundplane etches that do not require small pitch will be intentionally sloped in order to facilitate subsequent crossovers of that edge.

Another aspect of etching to be considered relates to the energy of the etchant and its effect on the resulting film edge. In the RIE mode, anisotropic etching is improved by decreasing gas pressure. The ion energy of the etchant increases with decreasing gas pressure and increasing mean free path. This causes the photoresist mask to rapidly deteriorate and the elevated ion energies can have adverse effects on the film morphology of the etched edge.

One general difficulty with RIE methods is that greater anisotropy is accomplished with higher voltages, which means greater potential for both film damage and radiation damage to the photoresist. This hardened photoresist can be difficult to remove even with commercial photoresist strippers and can leave detrimental residue on the wafer surface. An alternate method of ion generation using electron cyclotron resonance (ECR) has been used to reactively etch Nb and

NbN circuitry [74]. The ECR plasma etching is performed at lower gas pressures than RIE. Since the ion energy is controlled by an external bias voltage and pressure, anisotropic etching is achieved with low ion-energy etchants. In this way film damage, especially on critical edges, can be minimized.

An alternate approach to etching is lift-off. This is accomplished by first applying photoresist and patterning it preferably with an inverted profile. Metal is then deposited through the mask in the desired locations; the metal deposition on the resist will be lifted off during the acetone dissolution of the photoresist. This approach is useful as it has the advantage of not imposing any overetch but is limited to lower temperature depositions, thinner films, and reduced resolution.

6.2.3.6 Planarization

Although not a required process element for most current applications, planarization in some form is critical to advanced processing. The motivation to planarize becomes increasingly evident from a processing perspective as aspect ratios (the height of superconducting devices divided by their planar dimension) approach one [75]. In order to obtain both minimum-feature resolution and sufficient planarity to allow interconnects to cross over the edges, advanced processes utilize planarization techniques for at least a subset of their process flow (Table 6.2). Because such planarization techniques are generally labor-intensive, other more facile methods that allow various degrees of planarization are employed for specific process steps. One such method, commonplace in semiconducting processing, is RF-bias sputtering of dielectrics. This has been extended to the use of a low-frequency (40 kHz) substrate bias eliminating the need for the conventional RF generator and substrate tuning network [76]. Under proper conditions bias-sputtered SiO₂ can cover and provide a smoother surface than underlying NbN films. This can enable the fabrication of tunnel junctions on dielectrics over a groundplane, critical to reducing circuit inductance. In addition, the use of this technique facilitates higher yield of interconnect crossovers with respect to both dielectric integrity and crossover critical currents (Fig. 6.3).

6.2.4 APPLICATION EXAMPLE: DIGITAL PROCESSING

It is didactic to consider where the future lies for fabrication. One application that superconducting electronics can uniquely fulfill is being proposed in the Hybrid Technology Multi-Threaded (HTMT) petaflop scale computer [77]. This concept as envisioned would ultimately require junctions with critical current density of 20 kA/cm² and submicron junctions, but not necessarily deep submicron (0.8 μ m feature size). A total junction count of 100 billion is projected, distributed over 40,000 chips interconnected among 512 MCM that would function with 100-GHz on-chip clock speed to achieve the desired computational density.

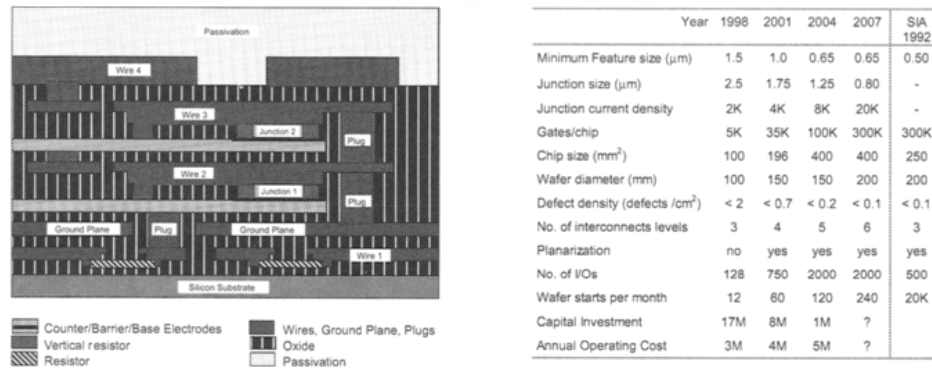


FIG. 6.4. Ultimate process flow for HTMT along with road map from Reference [78].

The fabrication aspects of these junction sizes and current densities are well within the realm of achievability in the near term (Fig. 6.4). A further issue of latency, the time required for a signal to traverse by interconnects between operations, is critical at the proposed speeds of operation. Despite signal propagation equal to one-third the speed of light, the finite time required for the signal to propagate between a given pair of gates can dominate gate delay and be more critical at these extreme frequencies of operation. This latency can be addressed by increasing circuit density. This can be done directly by reducing the lateral design rules for linewidths, line spacing, and layer-to-layer alignment. Decreasing pitch (linewidth plus line spacing), can be advanced by creating features with sharper edges. This can be done with improved resolution photolithographic techniques coupled with anisotropic etch techniques. This strategy for increasing feature density creates difficulties of its own for either dielectric films to completely cover these sharp edges, or for superconducting interconnects to traverse these edges without significant reduction of transport properties due to disordered film growth. This further emphasizes the need for high degree-of-planarization processing techniques. In addition, superconducting circuits that are inherently low-power (I^2R heating of zero-resistance superconducting interconnects is also zero) can enable true 3D integration. A fully planarized process with vertical integration can further increase circuit densities by orders of magnitude.

6.3 NbN Circuit Process

6.3.1 INTRODUCTION

6.3.1.1 History

In 1941, Aschermann, Friederich, Justi, and Kramer reported superconductivity in the compound NbN with a superconducting transition temperature of about

16 K [79]. This work was advanced by Gavalier *et al.* [80] by reactively sputtering high-quality NbN films; NbN/native oxide/NbN tunnel junctions were inserted into a circuit process flow, but the first high-quality, high-gap NbN Josephson junctions were fabricated by Shoji, *et al.* [12]. These junctions and their subsequent refinements are quite competitive with Nb junctions in terms of parameter spreads; MgO barriers continue to be the standard for NbN junctions, although some high-quality, very high- J_c (127 kA/cm^2) junctions have been fabricated using AlN as a barrier material [34].

6.3.1.2 Why NbN?

Liquid helium has been a “friendly” cryogen in the sense that it provides stable cooling with little cavitation or boiling that can affect circuit operation. In application, cryogen must be periodically replenished although that period in the case of the best cryostats can be measured in months to years. Still, such extreme care must be taken to preserve and replenish cryogen that one must also consider, based on the application, the use of circuitry at temperatures greater than 4.2 K.

The combination of cryocoolers with NbN circuits will allow construction of systems that do not require periodic replenishment of a cryogen, enabling use in a wide variety of ground- and space-based applications. In order to illustrate this, let us consider a single LSI chip of 10,000 gates, a gate typically consisting of a dozen junctions and resistors. The nominal thermal dissipation of this circuit during performance of its electrical operation has been estimated at $10 \mu\text{W}$. If one includes inevitable parasitic heat loads from the input/output leads along with radiation effects, the total heat load has still been estimated to be less than 100 mW [81].

More electrical input power is required by a cryocooler for a given cooling capacity in order to obtain lower operating temperatures. This involves both the ideal Carnot efficiency and the further reduced efficiency of real cryogenic refrigerators. For an operating temperature of 4.2 K used in Nb circuitry, the necessary electrical input power is estimated at 352 W for 100 mW of cooling capacity. For NbN circuits operational at 10 K, the electrical input power to the cryocooler to achieve 100 mW is reduced to 145 W. More significantly, it can be reached by a two-stage cooler. This departure from liquid cryogen cooling is a significant advancement towards developing applications that will be accepted by the user community.

One can equally consider a Nb-based circuit operating in a cryocooler. An increase in operating temperature from 4.2 to 6 K would represent a savings of 33% in cooling power simply based on a Carnot limit. Practical cryocoolers never obtain that limit and are often only a few percent of the cooling based on Carnot. In addition, further inefficiency is incurred by going from one-stage to two- or

three-stage cryocoolers. Although a variety of cryocoolers can certainly obtain 4-K operation, one approach that holds particular promise for superconducting circuitry is the pulse-tube cooler due to its reduced mechanical vibrations ($<10^{-3}$ g) compared to systems with moving displacers. This aspect impacts systems that operate without shielding in the earth's magnetic field, where even miniscule displacement can equate to significant signal noise due to the extreme sensitivity of superconducting devices to magnetic field variation [82]. Commercial systems, although large compared to 10-K cryocoolers, are currently available that provide 4-K operation using only two stages [83].

Another separate motivation for use of NbN junctions is found in the fabrication of SIS mixers. Due to their higher T_c electrodes and gap voltages (5 mV compared to 2.8 mV), the corresponding gap frequency extends to 1.5 THz. These junctions must also operate with very high current densities for optimum operation. Some remarkable progress has been made by Wang *et al.* by deposition NbN/AlN/NbN tunnel junctions with J_c as high as 100 kA/cm² while maintaining high-quality junction parameters [34].

6.3.2 PROCESS FLOWS

The differences between Nb and NbN process flows are few but significant. Due to the considerably greater ($>3\times$) penetration depth of NbN, the groundplane needs to be made considerably thicker to be able to reproduce and target inductance values on chip. This increased thickness of the first deposited layer creates an edge, once etched, that in turn requires thicker dielectric layers and thicker interconnect layers to fully cover this edge. Beveling of edges is more significant for NbN than for the more metallic Nb processing, both because the edge height is more severe and that NbN as a semimetal does not conform to contours as readily as Nb.

6.3.4 PROCESS ELEMENTS

6.3.4.1 NbN Junction Fabrication

The NbN circuit fabrication shares the same process elements with Nb-based processing, including dielectrics, resistors, photolithography and similar dry etch recipes. A primary departure is in the area of junction fabrications as elaborated in what follows.

Similar to niobium, high-quality NbN junctions are obtainable using a number of different deposited barriers; it is just typically harder to accomplish. As one

would anticipate, NbN with its relatively short coherence lengths makes nearly all aspects of NbN junction fabrication a more demanding task.

The NbN film morphology is typically textured polycrystalline in slightly tilted, columnar grains. The grains generally coalesce into larger grains with increasing film thickness. Due to the slightly tilted columnar grains, surface roughness increases with grain size and thus also with film thickness. When the base electrode film roughness is on the order of the barrier thickness, junction quality degrades. Empirically, this can occur at an RMS roughness on the order of one to two nanometers. Thus, care must be taken to grow smooth base electrodes and this is often done by keeping base-electrode thicknesses less than 200 nm. The disadvantage to this approach in practice is that using base-electrode thicknesses less than the penetration depth will result in large values of inductance of interconnections using this layer. Currently, designers can limit but not eliminate this concern through prudent circuit architecture.

In order to demonstrate the considerations that go into a NbN junction-fabrication process, the following is one example of developing a NbN junction-fabrication process:

- 1) NbN films are deposited as discussed in detail in Chapter 1: Fabrication Methods, Processing and Measurement for Superconducting Film Structures. The same considerations discussed in that section of optimization of film-transport properties along with film stress apply to junction deposition. A practical NbN film process includes film $T_c > 15$ K for 500-nm NbN films, resistivity < 180 micro-ohm-cm, and low stress.
- 2) Other attributes that are junction-specific must also be considered. Film qualification must include not only film T_c but also base-electrode roughness, which should be kept to less than or on the order of the barrier thickness.
- 3) A reasonable starting point for junction fabrication once a NbN film process is established is depositing a series of films at various thicknesses ranging from 50 to 500 nm. By measuring the T_c of these films one should observe an increase in film T_c as a function of thickness, which is characteristic of NbN growth.
- 4) It is useful to measure the film roughness of the very same films. This can be readily done with any number of commercially available atomic force microscopy systems. In addition, services are available that will provide quick-turnaround analysis [84] for this purpose. Generally, film roughness increases monotonically with NbN film thickness.
- 5) Film roughness obtained with this film-deposition process should be less than or equal to 2-nm RMS to be useful as a base electrode.

The increasing roughness of the base electrode must be balanced with the necessary thickness in order to obtain near-bulk values of the film

parameters. One can obtain near-bulk values with thinner films by heating the substrate temperature above ambient during deposition. This can be done by both external heating or depositing at higher power. The resulting film is also rougher due to the increased substrate temperature so that this approach is not a panacea.

- 6) A relatively simple barrier material to begin fabricating NbN junctions is MgO, which can be deposited by RF-sputtering.
- 7) Even dense MgO targets formed by a hot, isostatic press are hygroscopic, which can drastically effect their use as a barrier material.
- 8) A pre-sputtering of the MgO target for 6 to 8 h will serve to reduce the water content in the target material and in practice, is done after every exposure of the target to the atmosphere. For this reason, load-locked systems that minimize atmospheric exposure is recommended.
- 9) Deposition temperatures from 100 to 300 °C help facilitate both NbN and barrier growth. Deposition temperatures much above these values degrade the junction formation as evidenced by leakiness and shorting in the resulting junction I-V characterization.

6.3.4.2 NbN Operating Temperature

Currently, much of NbN circuit fabrication is focused at 10-K operation. Indeed, there is nothing absolutely preventing 20% higher temperature of operation, further reducing the cryocooling burden by another 7%. Thermal noise will further reduce circuit margin and inductances will increase due to an increase of the penetration depth (<6%). Folded into the question of temperature of operation is the variation in parameter spreads. However, even within present NbN processing technology there is room for improving T_c . Addition of carbon by reactively sputtering in a partial pressure of methane [85] can increase T_c by one to two degrees Kelvin. Successfully developing an NbCN process operational at 14 K reduces the cooling burden input power by some 71% over that of 4.2-K operation. When one considers that 77-K operation reduces this input power by only another 25%, one needs to seriously weigh that advantage over the considerable and daunting challenges of YBCO circuit manufacturing that is outlined in the next section.

6.4 HTS Circuit Process

6.4.1 INTRODUCTION

With the advent of the discovery of high-temperature superconductors, the prospect of reducing the burden of cooling superconducting circuitry for useful

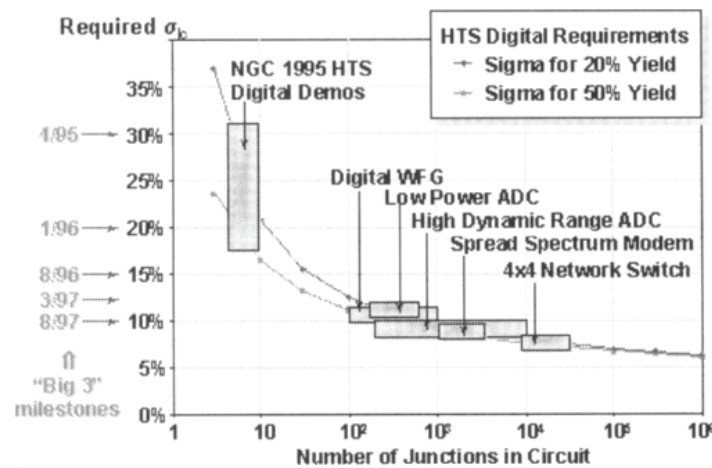


FIG. 6.5. Margin analysis of junction parameters spread and predicted circuit demonstration yield from Reference [39].

operation seemed near. Of course “high-temperature” superconductors is still an oxymoron for those accustomed to room-temperature electronics, as “high temperature” superconductor circuits typically need cooling by hundreds of degrees Celsius for 77-K operation. However, relative to Nb or NbN operation at 4 or 10 K, the cooling required for 77 K is dramatically reduced. Unlike Nb and NbN process flows, which can be likened to minor variations of a theme, HTS circuit fabrication varies dramatically from lab to lab in efforts to develop a useful circuit process. In terms of parameter spreads, it is evident that without a proven junction process with parameter spreads less than 10%, LSI or even MSI is not realizable (Fig. 6.5). It also poignantly points out where success has occurred in YBCO processing, with one- or two-junction SQUID.

As a circuit process, HTS is still in its infancy and has yet to settle on a process flow that can meet anything but the simplest of circuit requirements. A result of this is that there are disparate approaches that are being pursued in research labs throughout the world. This competition is still at a very dynamic stage and has not at all been resolved. It is generally conceded that although there are junction processes that perform better than others for given applications, the junction process that will be in use a decade from now has likely yet to be developed [86].

6.4.2 PROCESS FLOWS

The relative immaturity of HTS processing is such that present process flows are typically far simpler than corresponding LTS process flows. This is due in large

part to the epitaxial requirements of the HTS films in order to avoid greatly degraded superconducting transport properties. Unlike Nb or NbN processing discussed earlier, the addition of even a groundplane beneath the junction layer has major ramifications on the HTS junction process and must be carefully developed and controlled. As an HTS film is grown, any defect that is produced is propagated into the epitaxial layers grown above that defect. The effect of these defects remains deleterious even after the typical ion beam etch removal of the area of the defect. Because the point defect often produces a larger defect structure, such as an a -axis grain or void, the topology of the defect replicates into the layer beneath after ion milling. The result is that film quality is increasingly difficult to maintain as the number of processing layers increases as is needed for complex circuit fabrication.

Another aspect of HTS process flows that significantly differentiates them from their LTS counterpart is in the junction structure. Although much effort has gone into producing a trilayer junction process, there have been few circuits demonstrated with this technology. Due to the anisotropic nature of HTS materials including $\text{YBa}_2\text{Cu}_3\text{O}_7$ (YBCO), the coherence length in the a - b plane is significantly greater than along the c -axis. As discussed previously, the longer coherence length eases the fabrication of junctions. For this reason, and because film growth with the c -axis normal to the substrate plane (denoted hereafter as “ c -axis films”) is more readily obtainable, most HTS junction processes consist of junctions with current flowing parallel to the substrate. This topology readily produces subsquare micron area junctions. One side of the junction is defined by the film thickness, which is typically 0.2 to 0.3 μ , but could be varied to less than 0.1 μ in many junction technologies. Using standard photolithography 2- μ junction widths are readily obtainable with junction areas then as low as 0.5 μ^2 . This is equivalent to an LTS planar junction process with 0.8- μ diameter circular junctions.

The geometries of these HTS junctions naturally produce junctions low in capacitance and high in inductance relative to planar junctions. For practical digital circuits this puts an emphasis on lowering inductance through circuit design. The management of this parasitic inductance has strong ramifications for HTS digital-circuit fabrication.

6.4.3 PROCESS ELEMENTS

6.4.3.1 Films

High-quality, smooth film growth is critical in many aspects of circuit fabrication using YBCO. As elaborated in Chapter 1, numerous innovative deposition techniques have been developed, but no standard method has yet been established

so that the development of deposition techniques remains a very active area of investigation. The properties of junctions and other process elements such as interconnect crossovers and superconducting vias have been observed to be particularly sensitive to fundamental film properties. Not unlike the early days of Nb junction development that was limited by the ability to make quality Nb films, junctions may be limited considerably by issues inherent to the reproducible deposition of HTS films.

Yet another factor that makes fabrication of HTS Josephson junctions difficult is the number of constituents that comprise the material. Niobium has but a single element, niobium nitride has two elements, and depending on its stoichiometry, it can range from a superconductor to a resistor to an insulator; YBCO, with its four different elements, has possibilities of all sorts of stoichiometries different from that of the ideal. As the number of elements increases with doping of the HTS materials, this issue of stoichiometry becomes increasingly severe. In particular, the oxygen within HTS materials is relatively mobile and its concentration can vastly change the superconducting properties of the material. One of the challenges in fabrication has been to determine ways to maintain or replenish the oxygen within these materials to obtain optimum superconducting parameters. Considering the myriad of difficulties surrounding the fabrication of HTS and Josephson junctions, there has been remarkable success in creating many different types of Josephson junctions.

6.4.3.2 Junctions

In order to form a junction, barrier thicknesses must be controlled within a fraction of a coherence length across junction areas of the order of square microns. With YBCO unit cell dimensions (1.17 nm) on the order of the coherence length, little margin of error is available. Near-atomic level smoothness must be realized on the surface of the base electrode. Perfect crystallinity is required both within the deposited film and at interfaces. Any variation from the ideal epitaxy can suppress the superconducting order parameter, thus reducing the $I_c R_n$ product and causing considerable variation of critical junction parameters. Even without epitaxial flaws, stressed YBCO thin-film structures at interfaces can lead to localized and nonuniform oxygen loss, further degrading the superconducting transport properties [36].

It is safe to say that there is no single junction process that has been developed that satisfies all of the various requirements of superconducting applications for the HTS junctions. Rather than attempt to comprehensively categorize all of the various junction types that have been fabricated using HTS, we will examine a number of approaches that have been common to circuit fabrication. These are: bi-crystal grain boundary junctions, step-edge grain boundary junctions, SNS edge junctions, and finally, ion-beam damaged junctions (Fig. 6.6). A comment

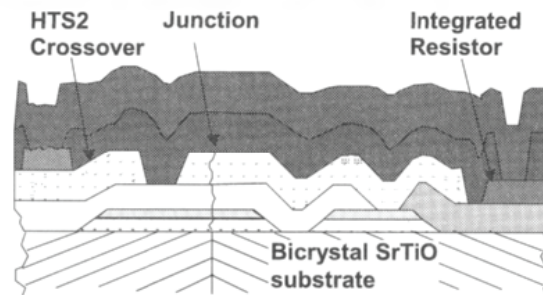


FIG. 6.6. Cross section of bi-crystal junction in multilayer process flow.

on planar junctions will be included, although in practical terms, the yield and reproducibility of this process is considerably less than these other junction processes.

The maturity of most HTS processes is such that incorporation of a junction process with other multilayer elements has only recently been developed. The fundamental building blocks of a multilayer film process for active circuit applications include: high-quality films for all superconducting and interconnect layers, high- I_c superconducting crossovers, good dielectric integrity, a stable, high-yield junction process, and an integrated resistor.

Although magnetometry is a clear example of a useful application that has met many requirements with single-layer YBCO junction processing, even this circuit could be enhanced with the availability of reliable, low-flux noise multilayer circuit processing. Low-inductance junctions are needed for the fabrication of digital circuitry. In order to reduce parasitic inductance, one is driven to tighter layer-to-layer alignments and the fabrication of junctions either above or below a superconducting groundplane. Design tolerances require controlled penetration depths and geometries and put further constraints on a junction process usable for digital circuitry. It is difficult to foresee an integrated circuit process that does not have at least the forementioned elements. To this end, present junction processes extendable to multilayer geometries will be examined in what follows in terms of their reproducibility and parameter spreads.

Bi-crystal junction. Likely the most straightforward and reliable approach to junction fabrication has been by deposition of YBCO on bi-crystal substrates. The substrate is formed by dicing a single crystal substrate into two and fusing the parts back together with an intentional misorientation of the crystal lattice. This approach was one of the first methods for fabricating HTS junctions [87] and remains one of the most reliable in terms of reproducibility of useful junction parameters. This approach to junction fabrication also is one of the simplest and requires little more than being able to fabricate a high-quality c -axis YBCO film

on a commercially available bi-crystal substrate, along with subsequent definition and metallization steps. The most commonly used substrate material for this purpose is SrTiO_3 ; however, due to the high permittivity of SrTiO_3 ($\epsilon_r = 1930$ at 77K) in applications where parasitic capacitance is detrimental, LaSrAlTaO (LSAT), with $\epsilon_r \sim 25$ has been used.

Although this is the most common approach for single SQUID applications such as magnetometry, difficulties with extending this fabrication technique to complex circuits are manifold. Regardless of whether the groundplane is positioned above or below the junction it will have an ill-placed weak link directly beneath the junction that can considerably alter device inductance. Also, interconnects crossing the bi-crystal boundary (as typically needed for a multi-layer coil) will include an undesirable I_c -reducing junction. Most significantly, for larger circuits, design will be greatly limited by the constrained positioning of junctions along the single bi-crystal boundary. This geometric limitation will incur greater than allowable parasitic inductance, which must be dealt with for complex digital circuitry.

Step-edge junctions. An alternate approach for inducing a grain-boundary junction in a YBCO film is by purposefully creating an edge that the YBCO film must traverse. This is the so-called step-edge junction proposed by Simon *et al.* [88] and investigated by many other groups [89]. As a c -axis YBCO film grows on a sloped edge of SrTiO_3 or LaAlO_3 (the most common materials for this junction type), it is energetically favorable for a -axis film growth as the slope approaches 45° . This "flipping" from c -axis to a -axis and back to c -axis creates grain boundary junctions in series [90], of which, the lower I_c junction is used in circuitry. Care must be taken in this technique to properly form the step-edge in these materials. For this reason, multilayer masking using Nb and diamond films has been utilized to ensure sharp, reproducible edge formation.

Other material systems have also been investigated that have a much different dependence on edge topology and the resulting YBCO film morphology. For steps created in MgO [91], a much shallower edge (19°) will form a grain boundary. In addition, by sculpting the bottom of the step-edge, the second inductance-increasing grain boundary can be eliminated [92].

This technique, similar to bi-crystal junctions, requires only a single deposition of YBCO to form the junction. It is well suited to magnetometry and has resulted in some of the lowest-noise SQUID fabricated in HTS [93]. In contrast to bi-crystal junctions, these junctions can be formed in any position and orientation. They can also be formed above a groundplane in a step formed in a deposited dielectric without creating grain boundaries in the underlying groundplane (Fig 6.7). The critical-current densities of these junctions are typically higher than bi-crystal junctions but have been demonstrated to decrease linearly with the deposited junction layer thickness. This method of reducing I_c , however,

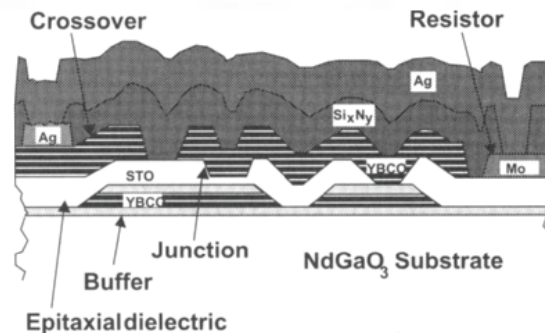


FIG. 6.7. Cross section of step-edge junction in multilayer process flow.

has the disadvantage of increasing the characteristic film inductance for circuit components. For film thicknesses necessary to target $I_c = 200 \mu\text{A}$ for a $4\text{-}\mu\text{m}$ -wide junction, film thicknesses are on the order of one-third of the penetration depth, and as such are in a regime where characteristic film inductance increases sharply. Because this LI_c product can be the limiting consideration for digital circuitry, this becomes problematic for physically realizable inductance structures. In addition, margin must be allowed on both sides of the grain boundary junction, so that lead length for step-edge junctions is a function of twice the alignment capability dictated by the photolithographic equipment. This lead length, especially in the thin YBCO layer whose thickness is tailored to correctly target I_c , greatly increases the junction parasitic inductance. An alternate method to reduce the I_c without increasing inductance is to purposefully deoxygenate the exposed grain boundary. This can be done by annealing in an argon atmosphere at 200 to 300°C , which will reduce junction critical current. This will also increase junction R_n , but not in proportion with the reduction I_c , thereby resulting in a smaller junction $I_c R_n$ product.

An alternate geometry involves using steps in a substrate with a subsequent epitaxial dielectric and HTS deposition as an overlaying groundplane. However, this groundplane is no longer planar and could form weak links directly above the junctions due to the underlying topology. The possibly diverted current flow in this groundplane due to the weak links not only increases inductance but does so in a fashion that is difficult to predict.

Ramp-edge SNS. Edge junctions have been previously made using Pb and Nb and is an effective approach for making small-area junctions (Fig. 6.8). Difficulties arise in these material systems due to the necessary *ex situ* processing, that is, the base electrode edge is formed and exposed to the atmosphere and process chemicals prior to barrier and counterelectrode deposition. This same issue arises again in doing *ex situ* processing on exposed YBCO base-electrode edges with

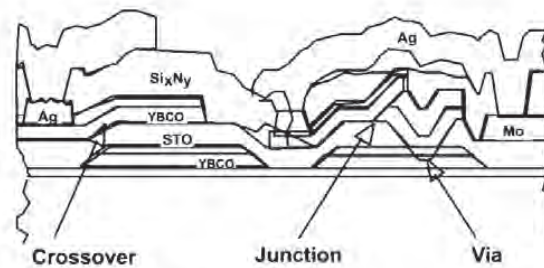


FIG. 6.8. Cross section of SNS edge junction in multilayer process flow.

the reactivity of YBCO. These edges must be carefully cleaned prior to barrier deposition to ensure good electrical contact. Early barriers consisted of noble metals such as Ag and Au that “bridged” between adjacent YBCO sections, and these type junctions still find a use in magnetometry applications [38]. At present, however, most SNS work utilizes epitaxial barriers followed by epitaxial YBCO counterelectrode deposition.

Among HTS junctions, epitaxial ramp-edge junctions have the greatest design flexibility. This junction is formed by first etching a YBCO film with dielectric overlayer to form a shallow edge ($15\text{--}35^\circ$). This “ramp edge” structure is then deposited upon with a normal barrier material followed by a YBCO counterelectrode. The smoothness of the base-electrode edge [40] is critical to the fabrication of this junction. This in turn requires a smooth base-electrode film, made even more difficult to achieve when formed over a YBCO groundplane and dielectric, which can translate roughness into the base electrode film. Despite such processing challenges, some of the best I_c spread results have been achieved using this junction type.

There are several major advantages offered by this junction design. First, I_c can be controlled by varying the thickness of the barrier layer, and second, its parasitic inductance is only half as sensitive to the junction lead length compared to the previous approaches. This benefit can lead to greater circuit operating margin. Third, these junctions can be formed either above or below a superconducting groundplane without damaging the groundplane.

Interface-engineered junctions (IEJ) are a variation of this junction design. In this case the process flow creates a barrier by exposing the base-electrode edge to a sequence of plasma, chemical, and annealing treatments [94]. This approach is currently the object of intense research efforts.

Ion-beam damaged junction process. Numerous attempts at using electron and ion beams to fabricate junctions have met with varying degrees of success [95]. These junctions have been successful in demonstrating the operation of simple digital circuits. This fabrication process has the flexibility of targeting I_c

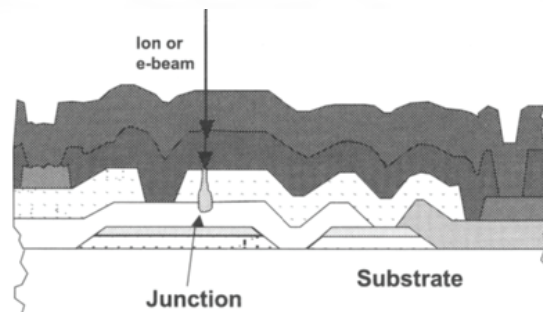


FIG. 6.9. Cross section of e -beam damaged junction in multilayer process flow.

by repeatedly applying the ion or e -beam to reduce I_c or annealing out damage to increase it (Fig. 6.9). Doubts concerning long-term stability have recently been credibly resolved. For wafer-level fabrication this technique would be beam-intensive and difficult to extend to the LSI level.

Planar junctions. All the junction types previously described (ramp-edge, bi-crystal, step-edge and ion implantation) rely on using film cross-section to achieve small junction area and coupling along the a - b axes (where the coherence lengths are greatest). The “price” that is paid for that geometry in terms of circuit parameters is generally higher parasitic inductance. For this reason, a fabrication process that produces junctions with a low-inductance trilayer geometry would be attractive to circuit designers. However, this is difficult to realize in practice. Topologically, this process flow is similar to the Nb-based process cross section (Fig. 6.2).

There are two primary approaches using this geometry. The first utilizes the intrinsic junctions that are formed by weak coupling between adjacent a - b planes. The second approach involves forming the junction electrodes from film grown with the a -axis normal to the substrate plane (so-called “ a -axis films”). Both these approaches are attractive because of their low-inductance geometry but require deep-submicron lithography to reduce the junction critical current to desired levels. Furthermore, the resulting $I_c R_n$ product is relatively small.

The first type, CAM (c -Axis Mesa) [96] junctions, are Likharev-type microbridges [97]. They require a very small, photolithographically defined junction area ($\sim 0.5 \mu\text{m} \times 0.5 \mu\text{m}$). This has been achieved by a combination of e -beam lithography and etch-back planarization. Even with minute cross-sectional area, the resulting inductance of this geometry is much reduced relative to the previous junction types. The capacitance incurred in this junction structure is greater; however, even this has been recently reduced through further innovation [37].

The second approach uses *a*-axis films and their longer coherence length (1.5 nm). This has been explored, especially by the Japanese research community, but as yet has met with limited success. Once again, the obtaining of a sufficiently smooth base electrode is a major obstacle limiting progress. Difficulties arise in being able to consistently grow *a*-axis films (base-electrode, barrier, and counter-electrode) that are homogeneous within the junction area. The fact that *a*-axis film growth proceeds more rapidly than *c*-axis growth, any *c*-axis inclusions create large topological variations that compromise junction performance. In addition, as *a,b*-axis coupling results in relatively high critical current densities, the cross-sectional area must be kept very small to achieve the required critical current. Otherwise, to avoid lithographically defining submicron junction dimensions, methods of reducing the critical current density must be employed. Despite the limited success in fabricating circuits with this junction process, ultimately this may be the junction geometry necessary to extend HTS technology to the MSI or LSI level.

6.4.3.3 YBCO-compatible Dielectric Films

As discussed previously, amorphous dielectric films are commonly used in IC processing. This, however, is not an option in YBCO-based multilayer processing. Dielectric materials must be lattice matched with YBCO, have electrical properties appropriate for the given application, and must allow oxygen diffusion to underlying YBCO films. This last criterion is unique to high-temperature superconductors and is due to the high oxygen mobility within YBCO. Care must be taken in the entire process flow to reduce oxygen loss and employ methods that re-oxygenate the films. These methods include 400 to 500 °C thermal annealing in an oxygen atmosphere, plasma treatments, and exposure to ozone. The latter two methods expose the YBCO film to increased concentrations of the more reactive monoatomic oxygen. With the multiple criteria that these layers must meet, obtaining defect densities less than 100 defects/cm² is challenging. Dielectric integrity may improve as YBCO film quality continues to improve as evidence suggests that defects arise from outgrowths and voids generated in the YBCO underlayers [39]. Material systems that have been successfully used as insulators in multilayer structures include SrTiO₃, SrAlNbO (SAN) [98], SrAl-TaO (ST) [39], PrBaCuO (PBCO), CeO₂ [99], and a trilayer of SrTiO₃/SAT/SrTiO₃ [100].

6.4.3.4 Vias and Interconnect Crossovers

Control of film epitaxy and stoichiometry are key to growing smooth, defect-free, superconducting YBCO films. The lattice match of the substrate to the film, deposition temperature, and deposition gas composition and pressure must be

controlled and optimized. Other issues such as target composition variation from deposition-to-deposition can degrade film morphology. This would then result in costly re-optimization of the film-deposition process. In the fabrication of vias and interconnect crossovers these requirements for defect-free film growth remain the same, but accomplishing them becomes considerably more difficult. Circuit fabrication requires patterning of the initial layers for all but the most basic of applications. Epitaxial film growth must then occur over various topologies rather than on the near-perfect template of a single crystal substrate. This has numerous yield-limiting failure mechanisms. Defects occurring in the epitaxy of initial layers can propagate into the overlying structures. Crystalline damage occurring on film edges during the etching process can inhibit later epitaxial growth. Once the film is patterned, chemical reactions induced by solvents and airborne contaminants can also occur on the exposed film edges [101].

From a film-growth perspective vias and crossovers represent two distinctly different process scenarios. For vias, the YBCO film is required to grow over an etched dielectric edge. In the case of crossovers, epitaxial dielectric and subsequent YBCO is required to grow over an etched YBCO edge. Due to the greater sensitivity of YBCO to the processing environment compared to the epitaxial dielectric, successful film growth is often more difficult to achieve in the crossover-forming process. In either scenario, grain boundary formation will occur, as with step-edge junctions [90], when the slope of the underlying film edge approaches 45° (Fig. 6.10a). In practice, edge angles need to be considerably less than 45° in order to avoid grain boundary formation at points where local variations cause steeper slopes. Incorporation of processing techniques can increase the critical current density that crossovers can sustain, often by several orders of magnitude, and correspondingly improve epitaxy of the film deposited along the edge as evidenced by TEM cross section (Fig. 6.10b, c).

The following guidelines should be considered in fabrication of crossovers and vias in YBCO:

- 1) Defects caused during epitaxial growth of the initial layers will limit critical current regardless of how careful subsequent processing is performed. Generation of outgrowths, voids, and other common defects in YBCO films (as elaborated in Chapter 1) can be more damaging in the strained growth over edges than is apparent from measurements of planar-film transport properties.
- 2) The most common approach for accomplishing YBCO film growth over nonplanar topologies is to simply make the structures as planar as possible. To this end, film edges are sloped to as low as 5° (with respect to the substrate plane) to allow unperturbed growth on the edge. However, this gentle sloping results in longer lead lengths required to traverse those edges. The increased lead lengths can generate increased parasitic induc-

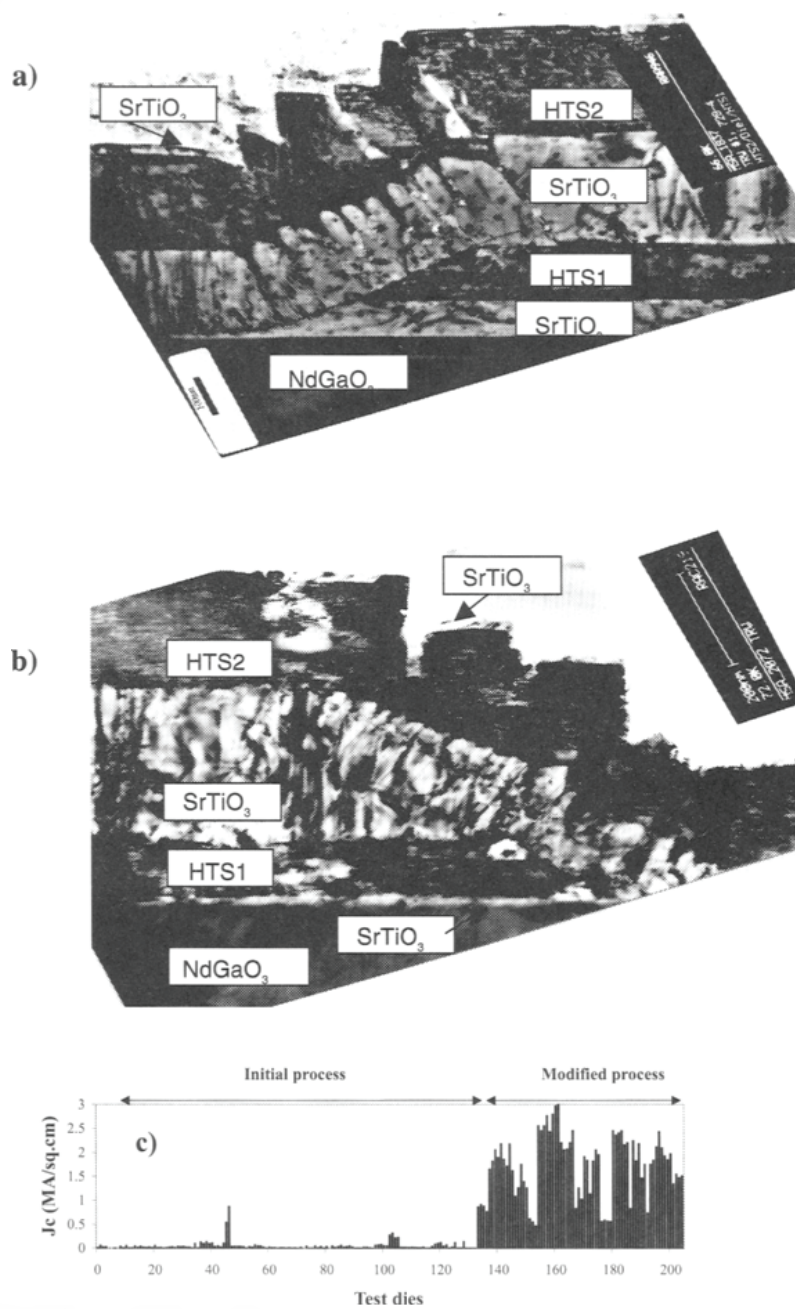


FIG. 6.10. TEM cross section of YBCO growth along SrTiO_3 -covered edge both before and after critical process insertions from Reference [103].

- tances, which can reduce circuit operating margins. Thus, edge lengths, especially for digital circuit considerations, should be as short as possible. These conflicting requirements are in practice met with edge angles of 20 to 30°. This allows reasonably short lead lengths along with edge angles that are reasonably robust against grain boundary formation.
- 3) Edge damage during the etching process should be minimized. This occurs during IBE due to ion bombardment. Operating the ion source at a reduced voltage lowers ion kinetic energy, thereby reducing edge surface damage. Most ion mills using Kaufman sources cannot operate at voltages much below 500 V; RF sources are less common and more expensive, but can generate ions at considerably lower voltages. Electron cyclotron resonance (ECR) ion sources offer an even more effective method for generating a high-flux density of low-energy ions. In these systems ion formation is independent of the acceleration voltage and reasonable etch rates at low voltages can be obtained simply due to the vast number of ions generated.
 - 4) The temperature of the wafer should be kept low during the etching process. Local heating due to the ion beam can be considerable and along with being in vacuum can de-oxygenate the YBCO film. This heat should be quickly removed from the wafer; consequently a water-cooled platen within the IBE system is common. A layer of vacuum grease or indium foil between the wafer and the platen significantly improves this heat transfer. Further improvements especially with respect to small-feature definition have been noted with substrate holders cooled to liquid nitrogen temperature during the etch process.
 - 5) Once the sample is etched, the photoresist must be removed and the bare edges are then exposed to the chemistry involved in that process. Commercial photoresist strippers are generally not an option for this process. Acetone followed by an isopropyl alcohol rinse is most common, although using oxygen plasma strip is also possible.
 - 6) The damage that occurs on the edges during the etching and photoresist removal should be removed prior to further deposition. This is ideally done *in situ* prior to the subsequent deposition but can be done *ex situ* if the wafer is transferred to the deposition chamber in a timely fashion. An alternate approach that does not expose the YBCO film edge to either the atmosphere or photoresist removal chemistry is using a multilayer masking and *in situ* etching prior to deposition [102]. This involves etching partially through the dielectric overlayer, stripping the photoresist and then *in situ* etching through the remaining dielectric and YBCO film immediately prior to deposition.
 - 7) Specific to via fabrication, etches are often continued through the dielectric and well into if not through the underlying YBCO film. This is done in order to maximize the area of contact with the higher critical current density *a-b* planes in typical *c*-axis YBCO growth.

6.4.3.5 Photolithography and Etching

The requirements of structure definition of even simple YBCO circuits can be quite diverse. As discussed previously, the fabrication of gently sloped edges facilitates epitaxial film growth on those edges. The preferred profile of other edges that do not require subsequent epitaxial depositions is typically as sharp as possible. For magnetometry applications, this reduces sources of flux noise in the thinned and possibly damaged edge region. For digital applications, sharp-profiled edges decreases the interconnect pitch (linewidth plus necessary line-to-line spacing necessary for clearance). For the forementioned reasons controlling the YBCO edge profile from 15 to 90° is desirable and can typically be accomplished through photolithographic and etching techniques.

Photolithographic processes that are well suited for Nb circuit processing may not be necessarily optimal for YBCO. Due to the reactivity of YBCO with the trace chemicals dissolved in water, contact of the YBCO film with water is typically avoided or minimized. Passivating YBCO with SrTiO₃ is one method of limiting exposure of YBCO surfaces to potentially degrading chemical reactions. Unfortunately, edges that are exposed in the etching process are more difficult to passivate. These edges are then typically exposed to various chemicals involved in photolithographic processing and great care must be taken to remove this contamination before subsequent epitaxial deposition. In practice this is commonly done by ion-beam etching or wet etching in a very weak acid such as EDTA. An innovative approach towards avoiding such contamination is through multilayer masking techniques. This can be accomplished by depositing a mask material such as TiN by conventional techniques. The edge is then etched by ion-beam etching until the mask material is entirely depleted. The thickness of this mask layer is determined by the etch rate of both the TiN and the YBCO and the thickness of the YBCO that is intended to be etched [102].

Film etching is also another technique that departs from typical Nb or NbN processing. Wet etching of YBCO is readily accomplished, so much so that diligent care must be taken to avoid exposure to even slightly acidic water during processing. This technique is routinely accomplished for large-feature definition. Although nearly all acids etch YBCO quite aggressively, it is interesting to note that hydrofluoric does not. The HF quickly passivates the YBCO surface effectively preventing further etching. The etch selectivity of HF to STO and YBCO has been successfully used to etch SrTiO₃ out from beneath a planar film of YBCO for bolometric applications. However, due to its wicking or undercutting of the photoresist, this technique is undesirable for accurate and reproducible patterning as device sizes shrink.

Rather than standard dry etching techniques, such as RIE, which have not been effective for YBCO, argon ion-beam etching (IBE) has been the predominant method. Film selectivity by IBE is much less dramatic than is typical of RIE

processing owing to the ballistic rather than chemical nature of IBE. This puts further onus on endpointing capabilities to avoid excessive overetching. Etch completion is often determined by assessing the etch rate from previous test pieces, which as a process is both time-consuming and costly. In addition, the time selected for a given etch is often overestimated to take into account wafer-to-wafer variation in the etch rate, which can lead to considerable overetching. For simple circuits, there is little penalty incurred by this. However, for multilayer processing, any overetching adds difficulty to achieving high-quality step coverage by subsequent epitaxial layers. It is important, therefore, to be able to stop etching at, or near, the desired interface. One flexible approach for endpoint detection is to employ a differentially pumped residual gas analyzer directed toward the wafer in order to sample the different species as they are etched away. This approach is essentially large-area secondary ion mass spectrometry (SIMS) so that endpoint detection of nearly any material of known composition can be effectively accomplished. Currently, commercially available units [104] are sensitive enough to endpoint film areas less than 1 cm^2 .

The use of automated lithographic alignment between circuit layers can significantly broaden the range of circuit designs that can be fabricated. This is common in both semiconducting and Nb process foundries and routinely allows alignment with a precision of $3\sigma < 0.4\text{ }\mu\text{m}$. The significance of this capability is especially important in layer-to-layer registration of digital circuitry where the lack of precise alignment forces circuit elements to have longer line lengths to accommodate larger misalignment. These longer line lengths increase circuit parasitic inductances that in turn reduces circuit margins and places tighter constraints on junction parameters such as I_c uniformity. These photolithographic tools, typically require full-size (2 in or greater diameters) wafers. In addition, these wafers must not distort during process temperature cycling and they must be flat to within $5\text{ }\mu\text{m}$ across the wafer. For these reasons and for film-growth considerations, NdGaO₃ and LSAT substrates reasonably satisfy these requirements.

6.4.3.6 Planarization

While YBCO film growth becomes more difficult on nonplanar surfaces, its growth on smooth and flat surfaces does not ensure defect-free growth. This is clearly evidenced by optically smooth bi-crystal substrates whose purpose is to generate grain boundaries. At the other extreme, YBCO films purposefully grown over steep step-edges can conduct supercurrent albeit with lower critical-current densities. Furthermore, film thicknesses on the order of the step-height can begin to overcome the current-limiting aspects of the grain boundaries along the step-edge. For planarization to be useful in a circuit, films must not only achieve

planarity but must also retain near-perfect epitaxy in order to transport high current densities with minimal flux noise.

Another motivation for the development of HTS planarization is the reduction of pitch in the groundplane definition. As discussed in the previous sections, the present approach for fabricating interconnect crossovers requires beveling of YBCO edges in order to allow high-quality dielectric and YBCO film growth over the edges. The beveled edges have angles from 5 to 30° with respect to the substrate plane. In order to make the characteristic inductance of YBCO/insulator/YBCO structures insensitive to run-to-run thickness variations, the YBCO thicknesses should be at least equal to the penetration depth. Note that Nb and NbN film thicknesses are typically 1.5× to 3× the penetration depth. For YBCO films, penetration depths are on the order of 200 to 350 nm depending on the precise film morphology. Thus, in the worst case, for a film thickness of 350 nm and groundplane edge angle of 5°, the edge length will be 4 μm. Although this long edge length can be accommodated by today's simple HTS digital circuitry, it would be deleterious to larger-scale integration.

Planar trilayer and CAM junctions particularly need a planarization technique to incorporate them into integrated circuits. In order to reduce their critical current to useful levels for most SQUID and circuit applications (~100–200 μA), junction diameters of 2 μm or less are needed. Clearly, beveled edge lengths of 4 μm would be unacceptable for this purpose. As in the push towards smaller-dimension junctions, sharp edges are useful in controlling the junction area and thus the junction critical current and its variation. These disparate needs are met through a dielectric etchback planarization technique used by the Cambridge group [96]. This technique involves applying a planarizing material such as a spin-on photoresist or bias-sputtered dielectric. This dielectric is then etched back to the YBCO surface. A useful degree of planarization can be achieved assuming reasonably similar IBE etch rates for the dielectrics used for planarization and circuit structures. This procedure can be repeated to further improve the planarization at the cost of much processing time and labor.

6.4.3.7 Resistors and Metallic Contacts to YBCO

The HTS junctions naturally exhibit nonhysteretic I-V characteristics and as such do not need the shunting resistor that standard Nb and NbN junctions require. However, there are circuit architectures, such as resistor-coupled SFQ circuitry, which require low-inductance resistors and, hence, resistors over groundplane. The effect of the across-circuit variation of these resistors for these circuits, can add in quadrature with junction I_c variation. Although not inherently difficult to fabricate, any resistor value variation results in more stringent demands on already challenging junction requirements. Common thin-film resistor materials, such as molybdenum, can be utilized after the high-temperature depositions have

been completed. This resistor can then be connected to the HTS circuits through normal metal wiring straps and annealed noble metal/HTS contacts. Care must be taken to reduce the noble metal/HTS contact resistance to values less than $10\ \Omega\text{-}\mu\text{m}^2$ in order not to be a major cause of variation in resistor values. Contacts made with *in situ* deposition of Au or Ag after the final YBCO deposition can readily attain these values. However, the removal of the contact Au or Ag from areas outside the contacts requires ion milling that will remove some of the top layer YBCO, thereby resulting in an undesirable thinning of that film. Alternatively, *ex situ* processing of the contacts with lift-off patterning can avoid a lossy normal metal on top of the YBCO film or having to etch off the metal and etch into the YBCO surface. This can be done by sputtering or evaporating Au or Ag after doing a brief *in situ* cleaning of the YBCO surface and annealing the sample in an oxygen furnace at temperatures near 550°C [105]. This anneal can also serve to provide re-oxygenation of the lower HTS layers that may have been depleted during processing.

6.4.4 APPLICATION EXAMPLES

6.4.4.1 Digital Considerations

In fabrication of digital circuitry, low-inductance junctions are needed. In order to reduce the inductance, and especially the parasitic inductance, one is driven to tighter layer-to-layer alignments and the fabrication of junctions either above or below a superconducting groundplane. Design tolerances require controlled penetration depths and geometries and put further constraints on a usable junction process for digital circuitry.

The primary unity in the majority of logic schemes for superconductors involves a loop of inductance L and its interaction with either an applied or an induced flux. A common condition arising in SFQ and other logic families is that the inductance-critical current product should be on the order of one flux quantum or less. In order to satisfy $L_p I_c < \Phi_0$, both junction critical current and total inductance need to be relatively small; reasonable values that satisfy this relation are $200\ \mu\text{A}$ and $10\ \text{pH}$, respectively. This pair of numbers arises because of the conditions on physically producing the inductive loop and in potential mutual coupling concerns. The parasitic inductance is taken as the inductance generated primarily by the junction leads that is not useful for signal processing. At $I_c = 200\ \mu\text{A}$, the allowable parasitic L_p must then be less than $1.2\ \text{pH}$. This parasitic inductance is a consequence of the penetration depth, finite junction lead length, junction critical-current density, layer-to-layer alignment, and the film thicknesses of groundplane, junction layer and interceding dielectric. In HTS processing, even monitoring thickness of these film layers during deposition

provides difficulty due to their epitaxial growth and elevated processing temperatures. One factor, the penetration depth, is an inherent function of film morphology and is not readily targetable. However, in order to optimally design digital circuits, the value and variation of the penetration depth needs to be accurately and empirically determined for a given process flow (see Chapter 3: Superconductor Electronics For Digital Devices, Circuits & Systems).

Digital circuitry in YBCO has enjoyed limited success with current levels of I_c variation for junction processes with useful geometries, consistent with Fig. 6.5. This application continues to be the most daunting of challenges for this material system.

6.4.4.2 Magnetometry

In contrast, the development of HTS films and junctions operational at the boiling point of liquid nitrogen had immediate and practical ramifications to this field of magnetometry. For example, SQUID magnetometry has been applied to such diverse applications as aircraft-based geophysical exploration, characterization and exploration of brain activity, failure analysis of critical aircraft parts and failure analysis of integrated microcircuits. Niobium-based SQUID have been well established in meeting many of the requirements that could operationally use liquid He temperatures. The motivation for HTS device insertion is due to cost of operation and convenience, and for numerous applications were quickly realized due to the higher temperature of operation. In addition, reduced thermal insulation would be required, which brings the SQUID sensor closer to the room-temperature object being measured, resulting in the potential for greater sensitivity. Relative to digital circuit fabrication, the fabrication requirements are less severe and present a credible opportunity for insertion of the less-mature HTS processing.

SQUID measurements in the ideal case approach the quantum limit in their sensitivity. However, real-world processing issues can prevent that measure of sensitivity from being obtained. Fortunately, there is correlation between film quality and reducing $1/f$ noise in magnetometers. The ideal that is sought for in film deposition is a purely c -axis oriented film of high critical-current density. Even small inclusions of a -axis grains can significantly increase $1/f$ flux noise. Large a -axis inclusions can be readily observed by SEM and methods of eliminating these are dealt with in Chapter 1. A more sensitive technique of identifying a -axis inclusions that are not necessarily evident by SEM is by performing a ϕ -scan in an x -ray diffraction unit.

Once the film morphology is under control in the deposition process, a common follow-up is to optimize films with respect to critical-current density. The motivation behind striving towards high critical-current density in these films is not due to a need for large supercurrents in these devices. The actual

supercurrent used in the operation of these devices is several orders of magnitudes less than the films can typically sustain. A mechanism that accounts for higher critical current densities is “pinning” of flux vortices, making it energetically unfavorable for them to move. This same pinning allows “magnetically quiet” devices to be fabricated as it is the movement of these flux vortices during device operation that is a source of $1/f$ noise.

Once it is understood that $1/f$ noise arises from movement of flux vortices, there are further implications to device processing, especially with respect to edge formation. As the strength of the pinning of the flux vortices decreases with decreasing film thickness, gently tapered edges should be avoided. Entry of flux vortices in the thinned edge area is a noise source; this area can be minimized on a given device by fabricating edges as sharply as possible. These near-vertical edges provide large edge-pinning forces. Recent magnetometer designs that include a grid-work of narrow lines put further emphasis on the importance of making high-quality edges.

In order to create vertical device edges, anisotropic etching by argon ion-beam etching is the most common method. Factors such as angle of ion-beam etching and argon pressure during ion-beam etching do affect the resulting edge angle after ion-beam etch; however, steepness of the photolithographic mask has the most direct bearing on the resulting edge topology. High-contrast photoresist with minimal or no post-baking provides a sharp-walled photolithographic mask with angles greater than 88° with respect to the film surface. In contrast, wet etching in slightly acidic solutions is an isotropic etch process and typically undercuts the photolithographic mask creating a shallow and undesirable edge for this purpose.

Finally, another fabrication-related aspect of YBCO-based magnetometry is choice of junction. The single most significant parameter for this choice is $I_c R_n$ at the temperature of operation. Due to the low-level integration the choice of junction is not constrained by requirements of junction uniformity, nor ultralow inductance as is the case in digital fabrication. Grain boundary junctions, especially bi-crystal junctions, perform admirably for this application due to both their simplicity of fabrication and their resulting electrical characteristics (see Chapter 6: SQUID Magnetometers).

6.5 Summary

Superconducting circuit fabrication has benefited from the rapid development of techniques for the semiconducting IC industry. It has been material issues that have often paced the progress of superconducting circuit fabrication. One theme that has repeated itself through the short history of Josephson junction fabrication is the need for junction electrode material, especially base-electrode films, that are

both sufficiently smooth to allow complete barrier coverage and robust to the operational environment. This issue has been successfully addressed in the Nb/Al/AlO_x/Nb system, reasonably met in the NbN/MgO/NbN system, and found wanting in YBCO. That YBCO circuits have yet to reach a high level of maturity should not be a surprising realization considering the challenges inherent to the material and the limited amount of time since its discovery. Historically, it has been a materials development that has improved junction processes to the point of greater utility. This was accomplished in lead by alloying, in niobium by overlaying with Al, and in niobium nitride by finding a compatible barrier material in MgO. It will likely again be needed before a circuit process useable for large-scale integration will be developed in YBCO.

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