

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS
AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

Case IPR2024-01403
Patent No. 7,772,673

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

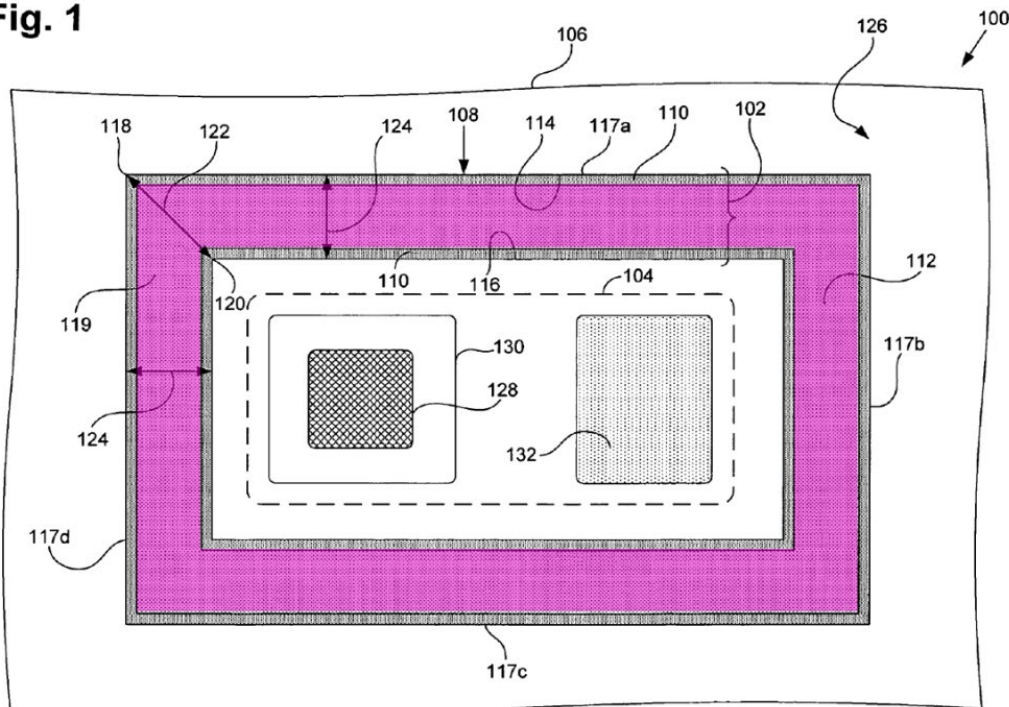
Exhibit	Description
Ex. 1001	U.S. Patent No. 7,772,673 to Yin et al. (“’673 Patent”)
Ex. 1002	Prosecution History of the ’673 Patent (downloaded from the USPTO’s Patent Center Website) (“’673 Patent File Wrapper”)
Ex. 1003	Declaration and Curriculum Vitae of Scott Thompson, Ph.D. (“Thompson Dec.”)
Ex. 1004	U.S. Patent No. 6,995,449 to Yin et al. (“ <i>Yin</i> ”)
Ex. 1005	U.S. Patent Publication No. 2005/0181569 to Koshimizu et al. (“ <i>Koshimizu</i> ”)
Ex. 1006	U.S. Patent No. 6,121,102 to Norström et al. (“ <i>Norström</i> ”).
Ex. 1007	Stanley Wolf, PH.D., SILICON PROCESSING FOR THE VLSI ERA, VOLUME 2: PROCESS INTEGRATION (1990) (“WOLF”)
Ex. 1008	U.S. Patent No. 6,362,040 to Tews et al. (“ <i>Tews</i> ”)
Ex. 1009	P. Moens et al, <i>Reliability Assessment of Deep Trench Isolation Structures</i> , IEEE 43 rd Annual Int. Rel. Phys. Symp., (2005) (“ <i>Moens</i> ”)
Ex. 1010	Stiffler et al., <i>The Effect of Trench Corner Shapes on Local Stress Fields</i> , 40 IEEE TRANSACTIONS ON ELECTRONIC DEVICES 3, (1993) (“ <i>Stiffler</i> ”)
Ex. 1011	U.S. Patent No. 5,104,816 to Verret et al. (“ <i>Verret</i> ”)
Ex. 1012	Peter Shepherd, INTEGRATED CIRCUIT DESIGN, FABRICATION AND TEST (1996) (“SHEPHERD”)
Ex. 1013	James M. Murduck, Fabrication of Superconducting Devices and Circuits, FRONTIERS OF THIN FILM TECHNOLOGY, Vol. 28 (2001) (“MURDUCK”)
Ex. 1014	J.P. Patent No. 3,141,621 to Matsuzaki et al. (“ <i>Matsuzaki</i> (JP)”)
Ex. 1015	Certified English Translation of J.P. Patent No. 3,141,621 to Matsuzaki et al. (“ <i>Matsuzaki</i> ”)
Ex. 1016	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2-24-cv-00140, Plaintiff’s Infringement Contentions Cover Pleading (July 18, 2024)
Ex. 1017	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2-24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)

I. PRELIMINARY STATEMENT

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.
(collectively “Samsung” or “Petitioner”) request *inter partes* review of U.S. Patent No. 7,772,673 (Ex. 1001), assigned to Patent Owner Harbor Island Dynamic, LLC (“HID”), and cancellation of claims 1-17.

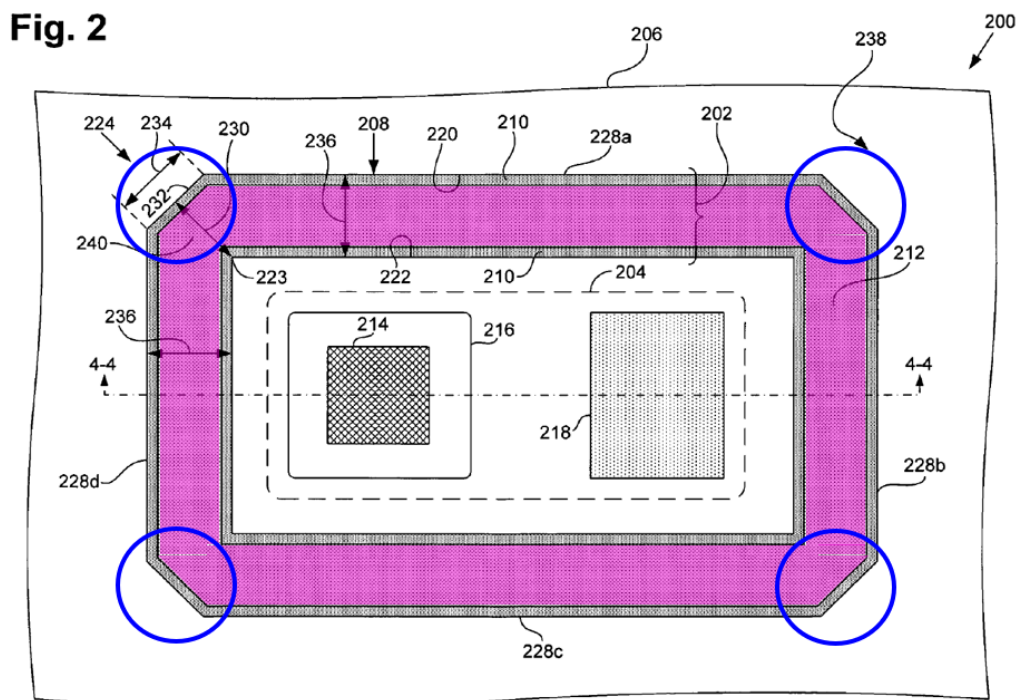
The challenged claims are directed to a semiconductor die with a **deep trench isolation region** having **at least one chamfered corner**. Annotated Figure 1 below depicts the admitted prior art of the '673 Patent—i.e., what the '673 Patent terms a “conventional” semiconductor die. *See* '673 Patent, 1:52-54. It shows a “top view of an exemplary conventional **deep trench isolation region** in a semiconductor die.” *Id.* (color added).

Fig. 1



Id., Fig. 1 (annotation added). As shown in this figure, the '673 Patent's "conventional" semiconductor die has a **deep trench isolation region** with corners that form right angles (i.e., 90° angles) between connecting sides. Thompson Dec. (Ex. 1003), ¶ 50 (citing '673 Patent, Fig. 1).

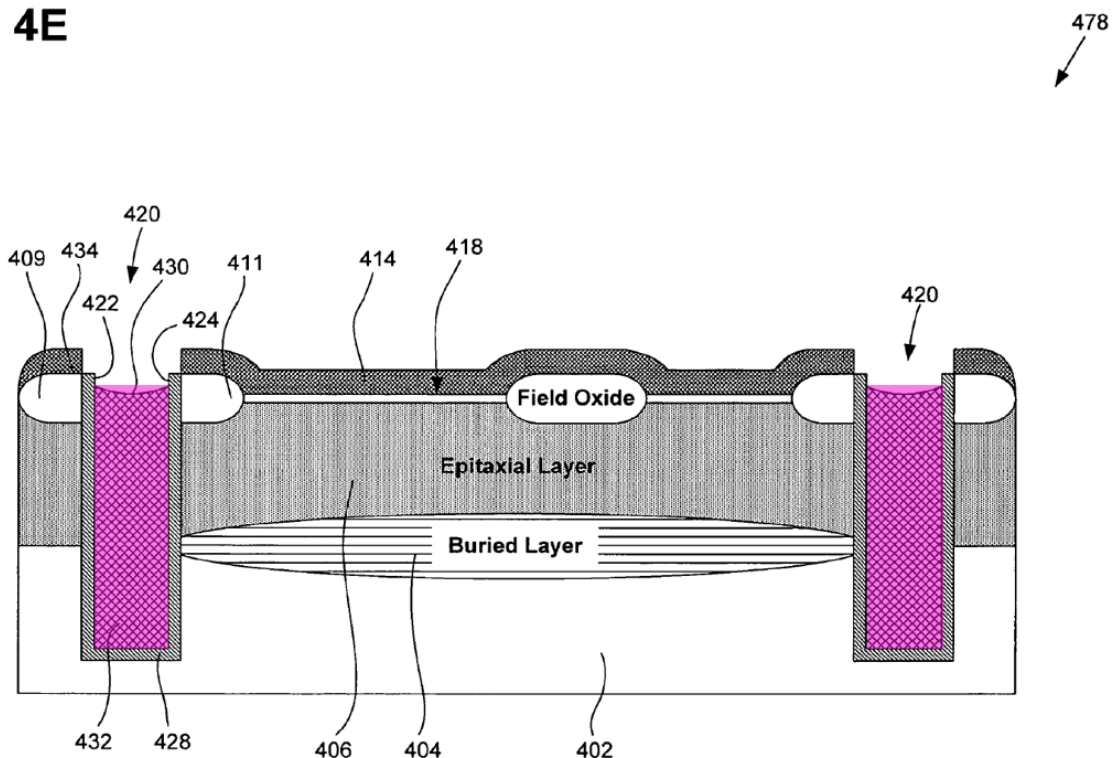
Annotated Figure 2 of the '673 Patent depicts "a top view of an exemplary **deep trench isolation region** in a semiconductor die in accordance with one embodiment of the present invention." *Id.*, 1:55-57 (color added).



Id., Fig. 2 (annotation added). Unlike the "conventional" semiconductor die depicted in Figure 1, the embodiment in Figure 2 includes **chamfered corners** at each of the four corners of the **deep isolation trench**.

According to the '673 Patent, these **chamfered corners** allow for a reduction in the amount of polysilicon needed to fill the **deep isolation trench**, depicted in annotated Figure 4E, thus allowing for reduced “polysilicon flaking” and “significantly increasing the average time between consecutive polysilicon deposition furnace cleanings.” *Id.*, 5:26-30.

Fig. 4E



Id., Fig. 4E (annotation added).

A chamfer is not invention. But all the alleged invention has added over the inventors' prior work was a chamfered corner at the outer corners of a semiconductor die. Chamfered trench corners were well-known and routine features of semiconductor devices, and it was already known that their use

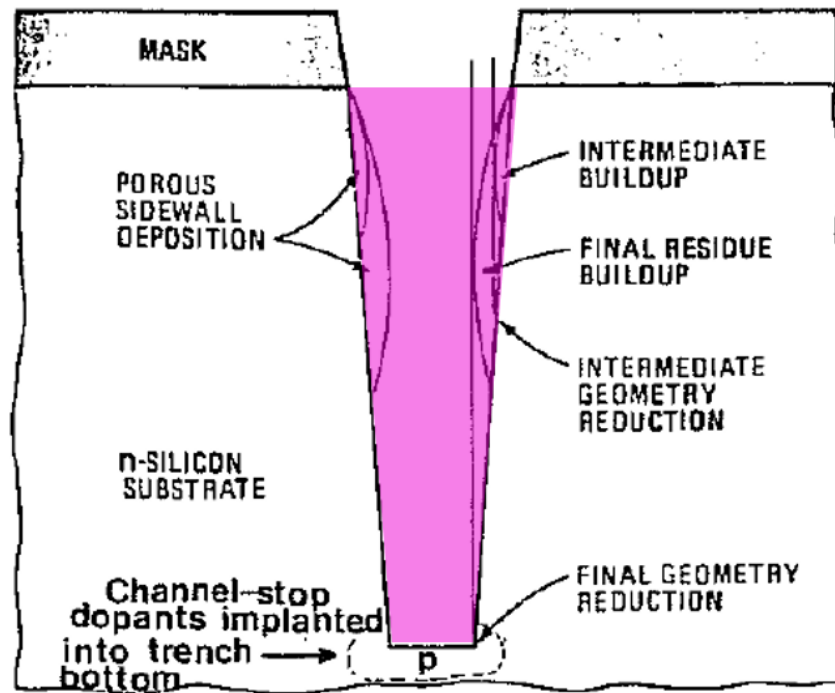
improves the refill process for a deep isolation trench. *See, e.g., Norström* (Ex. 1006), 16:27-36. A skilled artisan would have found these chamfers both obvious to add to a prior art semiconductor die from the same named inventors of the '673 Patent as well as outright disclosed by prior art by other inventors.

The Board should institute review and cancel all claims.

II. PRIOR ART BACKGROUND

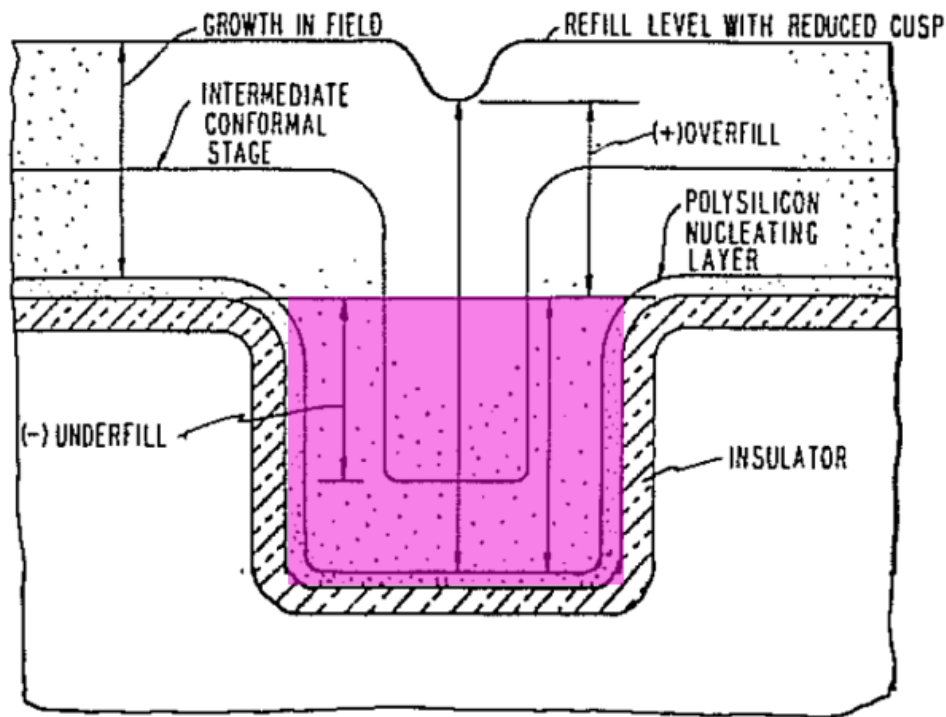
A. Overview of Deep Isolation Trenches in Semiconductor Devices

Deep trenches filled with polysilicon or other isolating materials have been used to electrically isolate semiconductor devices such as bipolar transistors for years. Thompson Dec., ¶ 44 (citing WOLF (Ex. 1007), 51-58). The semiconductor devices upon which these trenches are dug are typically very small—being measured in micrometers well before the priority date of the '673 Patent. *See* Thompson Dec., ¶ 44 (citing WOLF, 55). As such, the trenches are etched *chemically* rather than physically into the substrate of the semiconductor die using a “mask” that outlines where the trench will go—this mask prevents corrosive chemicals from digging into the rest of the semiconductor die. Thompson Dec., ¶ 44 (citing WOLF, 51-58).



Thompson Dec., ¶ 44 (citing WOLF, Fig. 2-37 (annotation added)).

After being etched, these trenches are then refilled with electrically isolating material to protect the semiconductor device inside from electrical interference by neighboring semiconductors. *See* Thompson Dec., ¶ 45 (citing WOLF, § 2.6.3.2). Many materials can be used, and as early as 1990, in “trench-isolation structures, atmospheric-CVD polysilicon, LPCVD polysilicon, CVD SiO₂, and selective, epitaxially-grown (SEG) silicon [had] reportedly been used.” WOLF, 56. This refill process “proceeds by means of a conformal covering of the trench surfaces and the original substrate surface,” whereby the isolating material is gradually deposited along the sides and bottom of the trench until it is refilled:



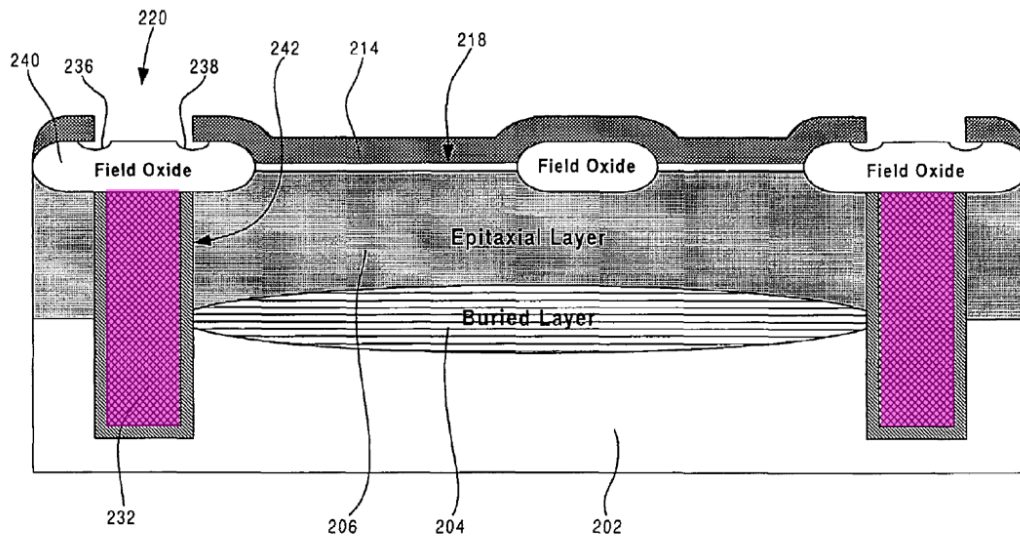
Thompson Dec., ¶ 45 (citing WOLF at 55-57, Fig. 2-40(a) (annotation added)).

The thickness of polysilicon required to fill a trench will scale with the width of a trench, and it was known more than a decade before the '673 Patent that “[i]f trenches of widely varying widths are filled, the narrow ones must be well overfilled in order for the wider ones to be filled completely.” Thompson Dec., ¶ 45 (quoting WOLF, 56). It was thus known that a trench with widely varying widths would require overfilling of narrower portions of the trench in order to ensure the wider portions are fully refilled.

B. Yin

Yin (Ex. 1004) issued as U.S. Patent No. 6,995,449 on February 7, 2006, and discloses a semiconductor die with a **deep isolation trench** having the same features as the '673 Patent—except for a chamfered outer trench corner. *Compare Yin*, Abstract with '673 Patent, Abstract; *see* Thompson Dec., ¶ 67. Both *Yin* and the '673 Patent share much of their disclosure and figures because *Yin*'s two co-inventors—Kevin Yin and Amol Kalburge—are also named inventors of the '673 Patent. Yet *Yin* was not disclosed to the patent office during the prosecution of the '673 Patent.

Like the '673 Patent, *Yin* discloses a semiconductor die having an electronic device isolated by a **deep isolation trench** surrounding it:



Yin, Fig. 2G (annotation added).

In Figure 2G, trench 220 represents the **trench** that comprises *Yin*'s “**deep trench isolation region** [which] may electrically isolate, for example, a **bipolar**

transistor, . . . from an adjacent CMOS transistor, such as a PFET, fabricated on the same semiconductor substrate.” *Yin*, 1:19-24 (annotation added); *see also* ’673 Patent, 1:17-20 (“A **deep trench isolation region** may also electrically isolate a **bipolar transistor** (i.e. a **bipolar device**) from adjacent bipolar transistors fabricated on the same semiconductor substrate.”); Thompson Dec., ¶ 68.

Like the ’673 Patent, *Yin* further discloses that its deep trench isolation region is refilled with polysilicon. *See Yin*, 1:47-59; 6:29-53 (“[A] layer of polysilicon is conformally deposited over substrate 202 and etched in an etch back process . . . as a result of the conformal polysilicon deposition process, deposited polysilicon fills **trench 220**.”); *see also* ’673 Patent, 8:11-14 (“[A] layer of polysilicon is conformally deposited over substrate **402** to fill **trench 420** and etched in an etch back process.”); *see* Thompson Dec., ¶ 69.

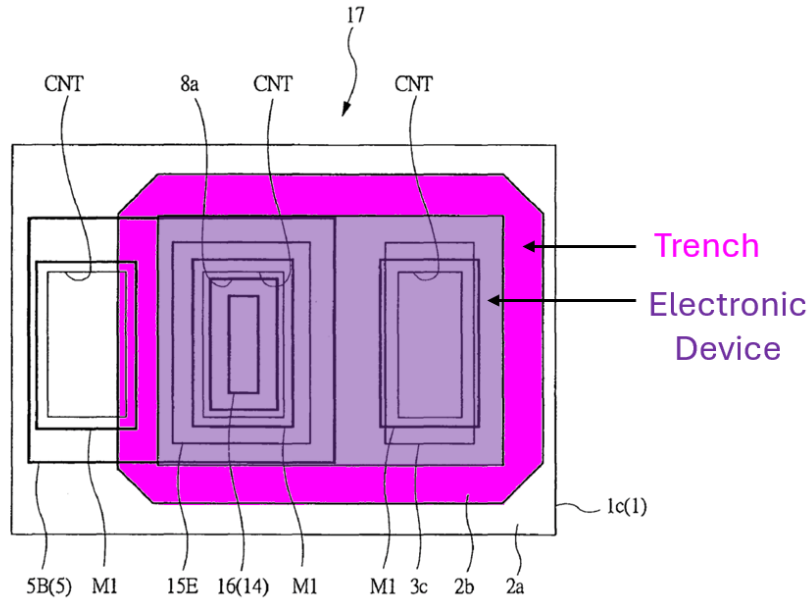
Yin is analogous art to the ’673 Patent because *Yin*, like the ’673 Patent, is directed to a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor. *See* Thompson Dec., ¶ 70; *compare Yin*, Field of Invention (“The present invention relates to the field of fabrication of semiconductor devices. More specifically, the invention relates to forming isolation regions in semiconductor substrates.”); *with* ’673 Patent, Field of Invention (“The present invention is generally in the field of semiconductor

fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor substrates.”).

C. Koshimizu

Koshimizu (Ex. 1005) published as U.S. Patent Application Publication No. 2005/0181569 on August 18, 2005, and also discloses a semiconductor die with a **deep trench isolation region**. See Thompson Dec., ¶ 71. In particular, *Koshimizu* discloses a “hetero-junction **bipolar transistor**” with a “manufacturing method for the semiconductor device.” *Koshimizu*, [0001]-[0006]. *Koshimizu*’s **bipolar transistor** is based in doped silicon and surrounded with a **deep isolation trench** as in *Yin* and the ’673 Patent. See Thompson Dec., ¶ 71 (citing *Koshimizu* at [0051]-[0061]; Figs. 15-16). Figure 16, annotated below, shows a birds-eye view of *Koshimizu*’s semiconductor device:

FIG. 16

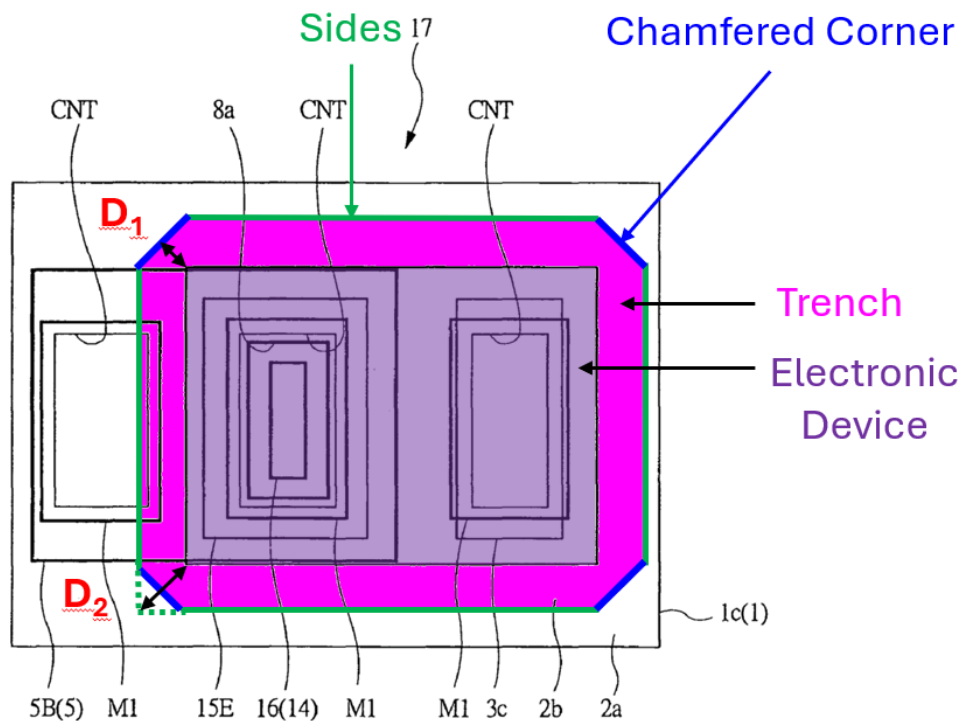


Koshimizu, Fig. 16 (annotation added); Thompson Dec., ¶ 71.

In Figure 16, **2b** is a **deep isolation trench** electrically isolating *Koshimizu*'s **bipolar junction transistor**. *Koshimizu*, Fig. 16; [0052] ("By this **deep trench isolation 2b**, each **device region** in the semiconductor layer **1c** is completely separated electrically.") (annotation added); See Thompson Dec., ¶ 72. *Koshimizu* fills its deep trench isolation region with a "silicon oxide film." *Koshimizu*, [0052]-[0053].

Below is Figure 16 of *Koshimizu* once again, this time with the **four sides** of the **trench** and its **chamfered outer corners** annotated as well:

FIG. 16



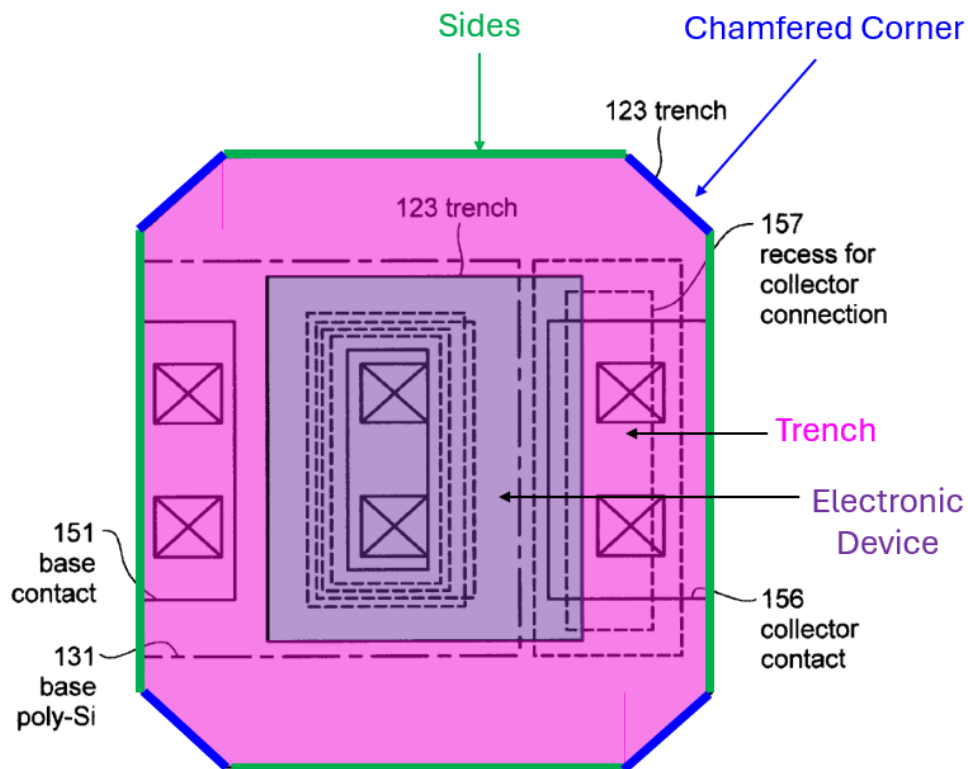
Koshimizu, Fig. 16 (annotation added). As shown, the chamfered outer corners result in a narrower or thinner trench at the corners *without* a chamfer – or, in other words, **D₁** is narrower than **D₂**. See Thompson Dec., ¶ 73 (citing *Koshimizu*, Fig. 16 (annotation added)).

Koshimizu is analogous art to the '673 Patent because, like the '673 Patent, it is directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors. See Thompson Dec., ¶ 74 (citing *Koshimizu*, [0052]-[0053]; '673 Patent, Field of Invention).

D. Norström

Norström issued as U.S. Patent No. 6,121,102 on September 19, 2000, and is directed to “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.”

Norström, 1:7-10 (annotation added). Figure 13c shows a birds-eye view of one of *Norström*’s disclosed semiconductor devices:



Thompson Dec., ¶ 75 (citing *Norström*, Fig. 13c (annotation added)). As shown above, *Norström*’s **trench 123** electrically isolates its **bipolar transistor** contained inside. Thompson Dec., ¶ 75 (citing *Norström*, Figs. 13a, c). The **four sides** of

Norström's **trench** also give way to **chamfered outside corners**. Thompson Dec., ¶ 75 (citing *Norström*, Fig. 13c).

Figure 13a shows a cutaway view of this same **bipolar transistor** surrounded by an **isolating trench**:

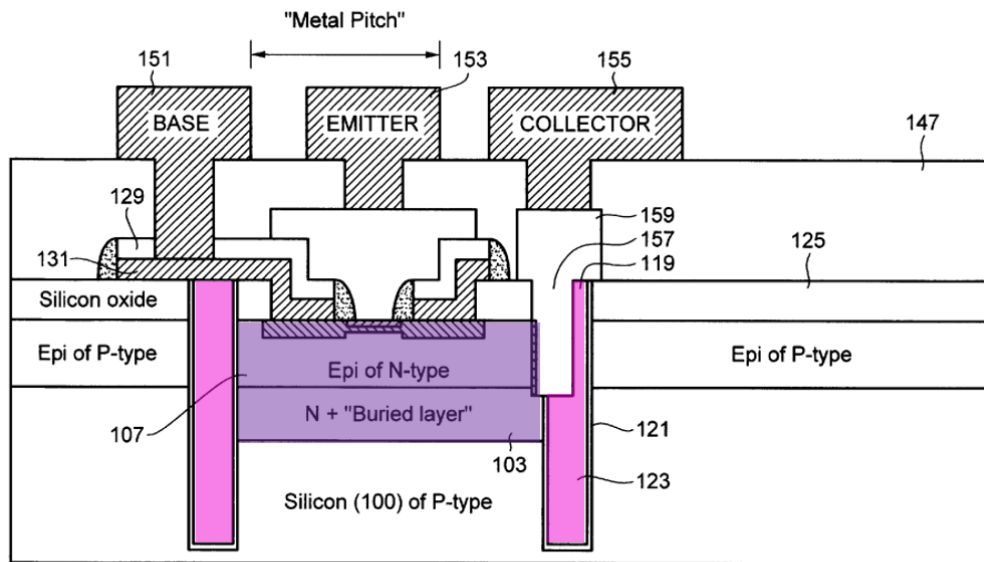


FIG. 13a

Thompson Dec., ¶ 76 (citing *Norström*, Fig. 13a (annotation added)). *Norström* explains that the **bipolar transistor** depicted in Figure 13 is an “NPN-transistor,” with **deep isolation trenches** extending along the sides of the **transistor**.

Thompson Dec., ¶ 76; *Norström*, 6:23-34, 8:50-11:40 (describing the manufacturing process for the same). These **trenches** are refilled with filling **123**, which *Norström* discloses may be polycrystalline silicon. *Norström*, 7:47-50 (“the

trenches are filled with an isolating or semi-isolating material **123**, for example, silicon oxide or polycrystalline silicon[.]”).

Norström is analogous art to the ’673 Patent because, like the ’673 Patent, it is directed to the manufacture of “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.” Thompson Dec., ¶ 77 (quoting *Norström*, 1:7-10; ’673 Patent, Field of Invention).

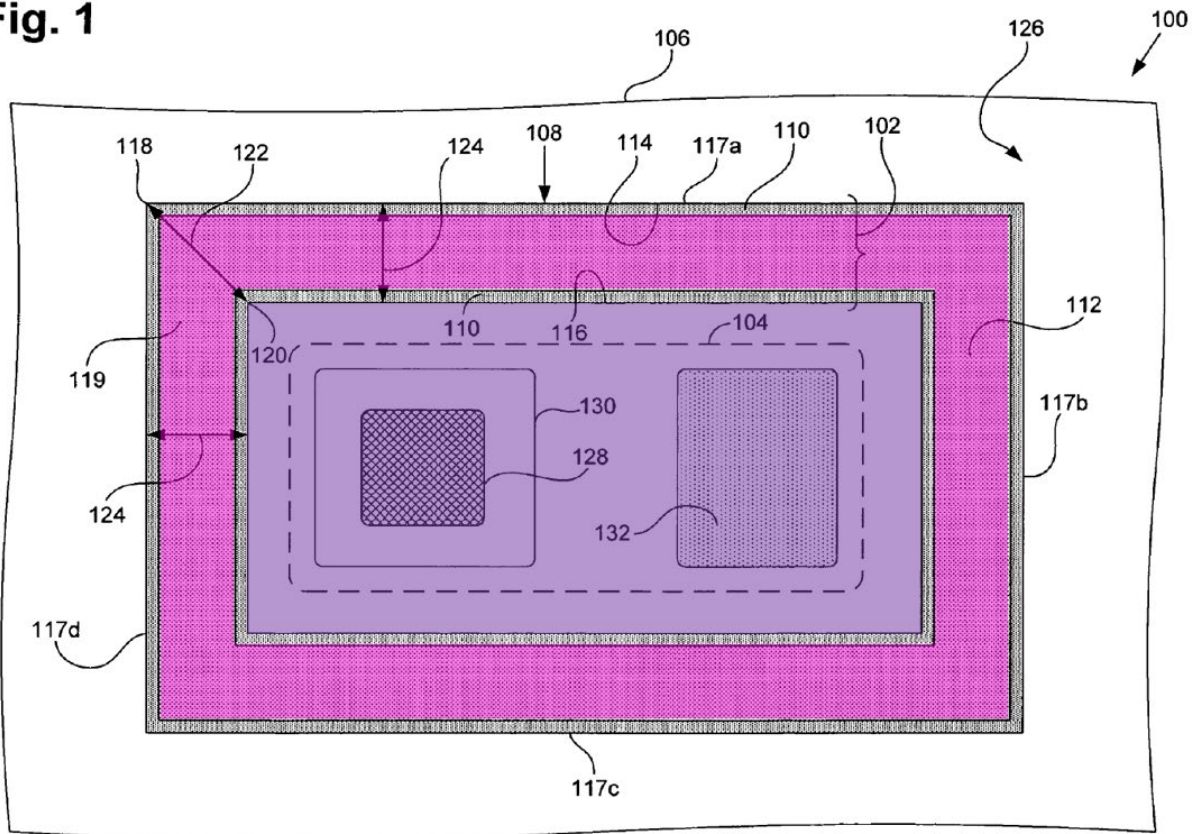
III. THE ’673 PATENT

The ’673 Patent simply takes the semiconductor die the inventors previously described in *Yin* and adds a chamfer—like in *Koshimizu* or *Norström*—to the outer corners of its trench. Viewed against this backdrop, the ’673 Patent is not directed to new or non-obvious subject matter.

A. Alleged Invention of the ’673 Patent in View of Prior Art

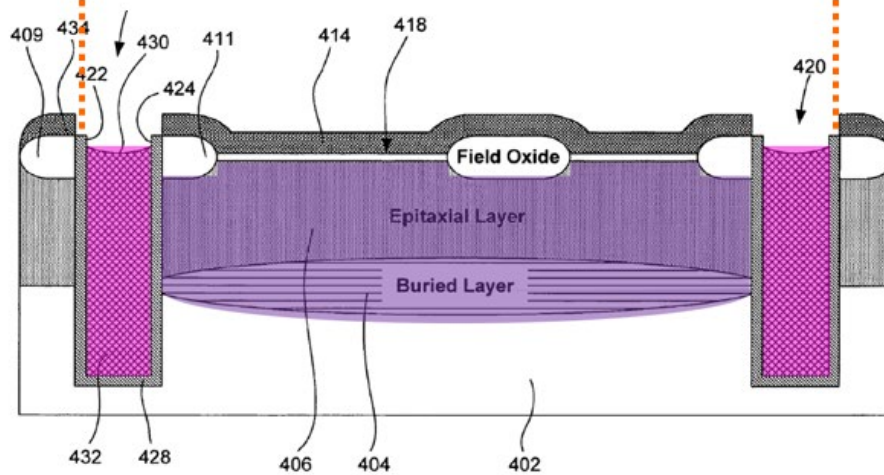
The ’673 Patent is directed to “a semiconductor die including at least one deep trench isolation region for isolating an electronic device (for example, a bipolar device)[.]” (’673 Patent, Abstract). Figure 1 of the ’673 Patent depicts the “top view” of what the inventors refer to as a “conventional” semiconductor die with **deep trench isolation region 102** isolating an electronic device such as a **bipolar transistor 104**:

Fig. 1



'673 Patent, Fig. 1 (annotation added); 2:35-3:50; Thompson Dec., ¶ 50. The '673 Patent states that the conventional "[t]rench **108** has trench corner width **122**, which represents...the minimum distance, [sic] between corners **118** of outside wall **114** and corners **120** of inside wall **116**["]' '673 Patent, 3:12-15.

Figure 2 of the '673 Patent then depicts a birds-eye view of its claimed semiconductor die containing a **bipolar transistor** surrounded by a **deep isolation trench** with **chamfered outer corners**. See '673 Patent, Fig. 2; Thompson Dec., ¶ 51. The **cut-away marker 4-4** in Figure 2 links to the side-cut view shown in Figure 4:



See Thompson Dec., ¶ 51 (citing '673 Patent, Figs. 2 (top), 4E (bottom) (both annotation added)). The '673 Patent states that “a **bipolar device (i.e. a bipolar transistor)** is utilized as an example of an electronic device” to be isolated by the **deep trench isolation region**, and that “[b]**ipolar device 204** is isolated by [the]

deep trench isolation region 202 from surrounding bipolar devices situated on substrate 206.” ’673 Patent, 3:51-54; 4:17-19.

Regarding the **chamfered corners**, the ’673 Patent explains that there are benefits to **chamfering the outside corners** of the **deep isolation trench**.

Specifically, it states that:

[B]y forming **trench chamfered corners 240** to reduce the trench corner width to approximately 0.9 microns compared to a trench corner width of approximately 1.4 microns for conventional **trench 108**, an embodiment of the present invention advantageously reduces the deposited polysilicon layer thickness from approximately 1.5 microns to approximately 0.7 microns.

’673 Patent, 5:15-21. Thus, by reducing the width of the trench at its otherwise-widest spots—i.e., its corners—by using a **chamfer**, the ’673 Patent seeks to improve the polysilicon refilling process and reduce the overall amount of polysilicon needed to fill the entire **trench**. Thompson Dec., ¶ 52. The ’673 Patent claims that “[s]ince deposited polysilicon layer thickness is reduced by approximately one half, the present embodiment can increase polysilicon fill process throughput for **trench 208** by approximately 100 percent compared to the polysilicon fill process throughput for conventional **trench 108** in FIG 1.” ’673 Patent, 5:21-26.

As explained in more detail below, chamfers on deep isolation trenches were not new before the '673 Patent. Nothing about the '673 Patent's chamfer rises to the level of patentability over the prior art.

B. Prosecution History

During prosecution of the '673 Patent, the Examiner rejected all claims as anticipated or obvious. '673 Patent File Wrapper (Ex. 1002), 42-53.

For anticipation, the Examiner found original claims 1-3, 7-8, 21-23, and 26-27 anticipated by U.S. Patent No. 6,107,161 to *Kitaguro*. '673 Patent File Wrapper, 45-47. For obviousness, the Examiner found original claims 6, 9, and 28 obvious over *Kitaguro* in view of the level of skill in the art (i.e., single-reference obviousness). '673 Patent File Wrapper, 48-49. The Examiner also found claims 1-9 and 21-28 obvious over the Applicant's admitted prior art (i.e., Figure 1 and accompanying disclosures) in view of U.S. Patent No. 5,933,749 to *Lee et al.*

In response, the Applicant argued that nothing in the prior art discloses a trench chamfered corner that causes a reduction in thickness of a layer of polysilicon within the trench. '673 Patent File Wrapper, 29-38. The Applicant specifically argued that *Kitaguro* did not employ "chamfered" corners, but a "circular arc shape." '673 Patent File Wrapper, 31. The Applicant also argued that *Lee*'s chamfer was not along the corner of the trench, but along its vertical inner

walls—and that this kind of chamfering “cannot reduce the thickness of a material that may be situated within [it].” ’673 Patent File Wrapper, 31-34.

The Examiner then allowed the claims. ’673 Patent File Wrapper, 13-18. The Examiner, however, was not aware of *Yin*, *Koshimizu*, or *Norström*, the prior art applied in this Petition. *Yin* disclosed every element of the challenged claims *other* than the claimed chamfered corner. And *Koshimizu* and *Norström* disclosed the chamfered corner. The claims are not patentable over *Yin*, *Koshimizu*, and/or *Norström*.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.¹

¹ Petitioner reserves the right to argue in an appropriate forum that certain limitations in the challenged claims are indefinite.

IV. STATEMENT OF PRECISE RELIEF REQUESTED

A. Prior Art

The '673 Patent was filed on March 16, 2007, and did not claim priority to any earlier application. Its earliest claimed priority date is therefore March 16, 2007.

Yin was filed on May 10, 2004, and claims priority to Application No. 10/371,416, filed February 20, 2003. *Yin* issued as U.S. Patent No. 6,995,449 on February 7, 2006, and is prior art to the '673 Patent under pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Koshimizu was filed as PCT application No. PCT/JP02/03764 on April 16, 2002, designating the U.S., and published as US 2005/0181569 on August 18, 2005. *Koshimizu* is prior art to the '673 Patent under pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

Norström was filed on March 18, 1998 and issued as U.S. Patent No. 6,121,102 on September 19, 2000. *Norström* is prior art to the '673 Patent under pre-AIA 35 U.S.C. §§ 102(a), (b) and (e).

B. Challenge

Ground	Challenged Claims	Basis	Prior Art
1	1-17	§ 103	<i>Yin</i> in view of <i>Koshimizu</i>

2	1, 3, 5, 7-8, 10, 12, 14-16	§ 102	<i>Norström</i>
3	7, 15	§ 103	<i>Norström</i>

C. Independent Claims 1, 10

The '673 Patent has two independent claims and 15 dependent claims. Both independent claims (1, 10) are directed to a semiconductor die; the primary difference between the two independent claims is that independent claim 10 requires that the “at least one trench hav[e] **four sides** surrounding [the] electronic device,” whereas independent claim 1 requires only a **plurality** of sides:

Claim 1	Claim 10
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1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising: a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides; wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.	10. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising: at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides; each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.
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See '673 Patent, Claims 1, 10 (annotation added). Given these similarities, shared analysis for claims 1, 10 and their matching dependents will be provided together in Section VI. To the extent that a reference requires separate analysis for one claim over the other (such as additional analysis to show four sides for claim 10), that analysis will be provided separately.

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work

experience can compensate for less education, and *vice versa*. Thompson Dec., ¶ 63.

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

A. Ground 1: Claims 1-17 Would Have Been Obvious From *Yin* in View of *Koshimizu*

A POSITA would have been motivated to add *Koshimizu*'s chamfered trench corners to *Yin*'s deep isolation trench.

The combination of *Yin* and *Koshimizu* amounts to combining prior art elements according to known methods to yield predictable results.

Yin teaches a semiconductor die with a deep trench isolation region that surrounds and electrically isolates an electronic device such as a bipolar transistor. *See, e.g., Yin*, Abstract; 1:15-27; Thompson Dec., ¶ 81. *Koshimizu* likewise teaches a semiconductor die with a bipolar transistor surrounded by a deep isolating trench. *See, e.g., Koshimizu*, [0051]-[0053]; Thompson Dec., ¶ 81.

Yin does not disclose the geometry of the corners of its deep trench isolation region. *See* Thompson Dec., ¶ 82. Thus, a skilled artisan looking to use *Yin*'s semiconductor die would have looked to other disclosures for a suitable corner geometry. *Koshimizu* provides that geometry, specifically teaching trenches with an unchamfered inner corner and a chamfered outer corner. *See Koshimizu*, Fig. 16, [0028]; *see also id.*, [0051]-[0061] (fully disclosing the manufacturing method

and features of the same). *Koshimizu* is just one of many examples of a deep isolation trench with chamfered corners; these were a common feature of deep isolation trenches before the '673 Patent. *See* Thompson Dec., ¶ 82 (citing *Moens* (Ex. 1009), 573-74; *Tews* (Ex. 1008), Figs. 1, 4; *Norström*, Figs. 13, 25).

Chamfered corners were beneficial not only because they improved structural stability, Thompson Dec., ¶¶ 83-84 (citing *Stiffler* (Ex. 1010), 559-62), but also because they could reduce the need for overfilling. For example, it was known before the '673 Patent that a deep isolation trench needs to be filled with isolating material such as polysilicon or silicon oxide such that all portions of the trench, including the *widest* portions of the trench, are completely filled. Because the portions of the trench are filled at the same time, this can cause overflow over the narrowest portions of the trench. Thompson Dec., ¶ 84 (citing WOLF, 55-57). It was “textbook knowledge before the '673 Patent that ‘i[f] trenches of widely varying widths are filled, the narrow ones *must be well overfilled* in order for the wider ones to be filled completely.’” Thompson Dec., ¶ 84 (quoting WOLF, 56) (emphasis added). And chamfered corners normalize the width of the trench’s corners with the width of the trench’s sides, thus minimizing the variance between their widths and the widths of the sides of the trench and reducing the need to overflow the sides of the trench. *See* Thompson Dec., ¶ 84; *Koshimizu*, Fig. 16.

Putting all of this together, a POSITA would have been motivated to avoid the overfilling of trench sides in *Yin*'s deep isolation trench that would result from unchamfered corners by instead using chamfered corners. Thompson Dec., ¶ 85. And this would also have the added benefit of improved structural stability. Thompson Dec., ¶ 85. Adding *Koshimizu*'s chamfered corners to *Yin* is nothing more than using a known method (chamfering a deep isolation trench) that yields a known result (e.g., a reduction in the necessary isolating material in said trench). Thompson Dec., ¶ 85.

The combination of *Yin* and *Koshimizu* involves the use of a known technique to improve similar devices or methods in the same way.

Koshimizu's device is similar to *Yin*'s. *Yin* is directed to the use of a deep isolation trench filled with polysilicon to electrically isolate an electronic device such as a bipolar transistor. Thompson Dec., ¶ 86 (citing *Yin*, 1:10-27). *Koshimizu* is directed to a semiconductor die using a deep isolation trench filled with silicon dioxide to electrically isolate a bipolar transistor. Thompson Dec., ¶ 86 (citing *Koshimizu*, [0001]-[0006]; [0051]-[0053]).

While *Koshimizu* uses silicon oxide, (*Koshimizu*, [0051]-[0053]), and *Yin* uses polysilicon, (*Yin*, 6:29-53), to refill their respective isolation trenches, the use of a chamfer on the trench's corners improves *Koshimizu* in the same way it would improve *Yin*. Thompson Dec., ¶ 87. Polysilicon and silicon oxide were textbook

alternatives for refilling isolating trenches for more than a decade before the date of the '673 Patent. Thompson Dec., ¶ 87 (quoting WOLF, 56) (“In trench-isolation structures, atmospheric-CVD polysilicon, polysilicon, CVD SiO₂, and selective, epitaxially-grown (SEG) silicon have reportedly been used’ as early as 1990.”).

Both polysilicon and silicon dioxide are filled into trenches using the same process of conformal deposition, and both can result in overfilling if one portion of the trench is considerably wider—as unchamfered corners may be—compared to the rest of the trench. *See* Thompson Dec., ¶ 88 (citing WOLF, 56-57). A POSITA would thus have expected the same benefits *Koshimizu*’s chamfered corners grant to *Koshimizu*’s trench (e.g., reduced overfilling) to apply to *Yin*’s similar trench in the same way. Thompson Dec., ¶ 88.

A POSITA would have had a reasonable expectation of success in combining *Yin* with *Koshimizu*

Koshimizu’s chamfered corners could have been easily implemented by a POSITA on *Yin*’s deep isolation trench with a reasonable expectation of success. Chamfering the outer corners of *Yin*’s trench would have required nothing more than an adjustment to the mask pattern that defines the outline of the trench to have chamfered corners instead of square corners. Thompson Dec., ¶ 89 (citing WOLF, 54). It was also known in the art that 135° angle corners (i.e., chamfered), rather than 90° angle corners (i.e., unchamfered) were one solution to improve problems

associated with trench refill. *See* Thompson Dec., ¶ 89 (citing *Norström*, 16:27-36); *see also In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) (finding that when the prior art identifies a problem and provides “explicit guidance” on how to fix the problem, it is reasonable to conclude that the skilled artisan would have had a reasonable expectation of success in combining the prior art.).

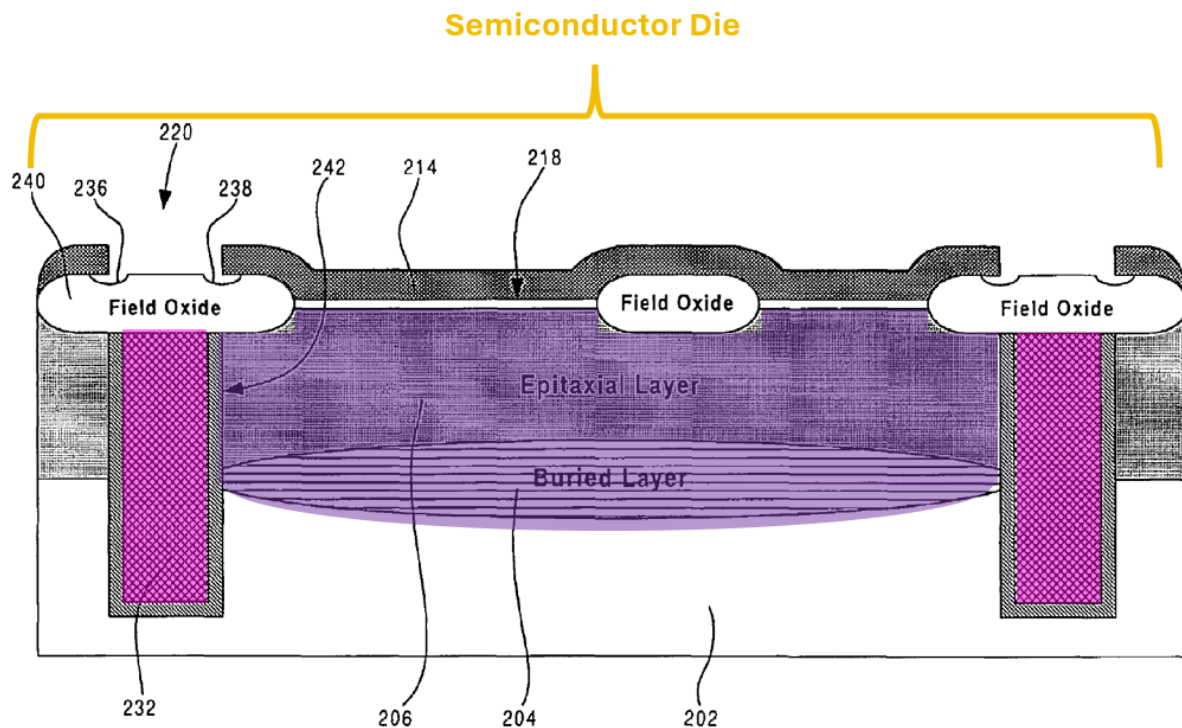
Design incentives and other market forces would have motivated the combination.

Finally, a POSITA would have been motivated to combine *Yin* with *Koshimizu*’s chamfered trench to reduce the waste associated with overfilling a deep isolation trench. It was desirable before the ’673 Patent to improve the refilling process and reduce the overfilling of deep isolation trenches with isolating materials. Thompson Dec., ¶ 90 (citing *Norström*, 16:27-36; *WOLF*, 55-57). By using *Koshimizu*’s chamfered corners on *Yin*’s deep isolation trench, a POSITA would have advantageously reduced the manufacturing costs associated with making semiconductor devices. Thompson Dec., ¶ 90.

1. Independent Claim 1

- a. 1[pre]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”

To the extent the preamble is limiting, *Yin* discloses a **semiconductor die** including at least one **deep trench isolation region** for isolating an **electronic device**. Thompson Dec., ¶ 91. Annotated Fig. 2G from *Yin* is shown below:



Thompson Dec., ¶ 91 (citing Fig. 2G, (annotation added)). In Figure 2G, trench 220 represents a **deep isolation trench** filled with polysilicon 232. *See Yin*, 6:29-53 (“As a result of the conformal polysilicon deposition process, deposited polysilicon fills **trench 220**.”) (annotation added). *Yin* further discloses that Figure

2G depicts the cross-section of a wafer, which the '673 Patent refers to as a semiconductor die. *See Yin*, 3:13-16 (“FIG. 2G illustrates cross-sectional views, which include portions of **a wafer**. . . .”) (emphasis added); '673 Patent, 5:52-57 (“The **wafer** may be referred to as a **semiconductor die**. . . .”) (annotation added); Thompson Dec., ¶ 91.

Yin also explains that this “**deep trench isolation region** may electrically isolate, for example, a **bipolar transistor**[.]”² *Yin*, 1:19-24. In the embodiment shown in Figure 2G, the **bipolar transistor** is shown to be surrounded by the **deep isolation trench**. Thompson Dec., ¶ 92 (citing *Yin*, 1:16-27). The overall structure shown in Figure 2G is located on the **semiconductor die** housing the **bipolar transistor** and **deep trench isolation region**. *Compare Yin*, Fig. 2G with '673 Patent, Fig. 4E (*Yin*'s Figure 2G providing a near-identical cut-away to the portion of the **semiconductor die** shown in '673 Patent Figure 4E); Thompson Dec., ¶ 92.

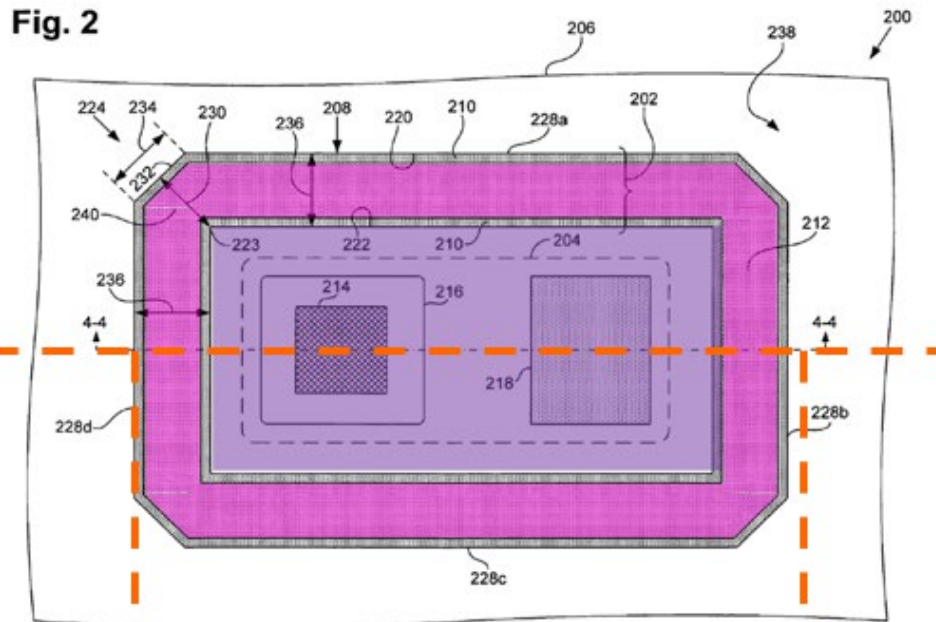
² The '673 Patent specifically names a bipolar transistor as an example of an “electronic device.” *See* '673 Patent, 2:35-38, 3:51-54.

- b. 1[a]: “a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;”

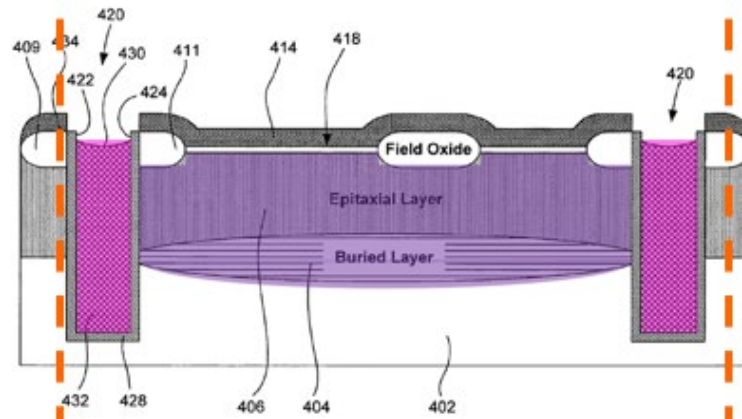
The combination of *Yin* and *Koshimizu* discloses a **four-sided trench** situated in a **substrate** of said **semiconductor die**, said **trench** surrounding an **electronic device** and having **trench chamfered corners** (i.e., at least one) connecting said **four sides**. Thompson Dec., ¶ 93.

First, *Yin* discloses the enclosure of an **electronic device** (e.g., a **bipolar transistor**) between the **sides** of a **deep isolation trench** situated in a **substrate**. As shown in Figure 2G below, **trench 220** surrounds a **bipolar transistor**. *See Yin* 1:19-27 (“a **deep trench isolation region** may electrically isolate, for example, a **bipolar transistor**[.]”) (annotation added); Thompson Dec., ¶ 94 (citing *Yin*, Fig. 2G; 1:19-27). *Yin* Fig. 2G represents a **bipolar transistor** isolated by a **deep isolation trench** consistent with the manner in which the ’673 Patent represents the same:

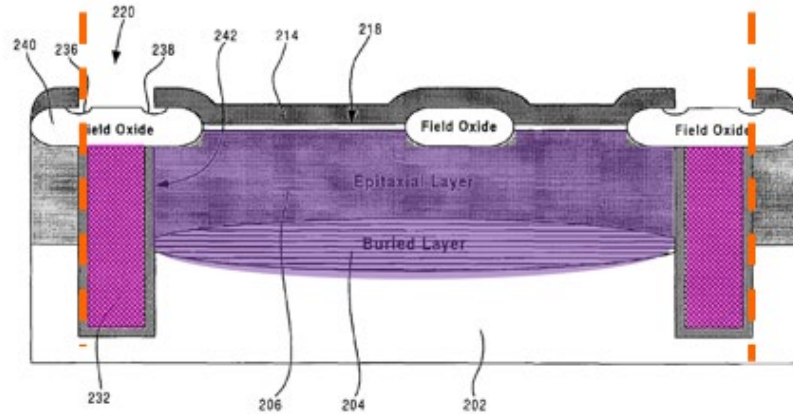
'673
Patent
Fig. 2



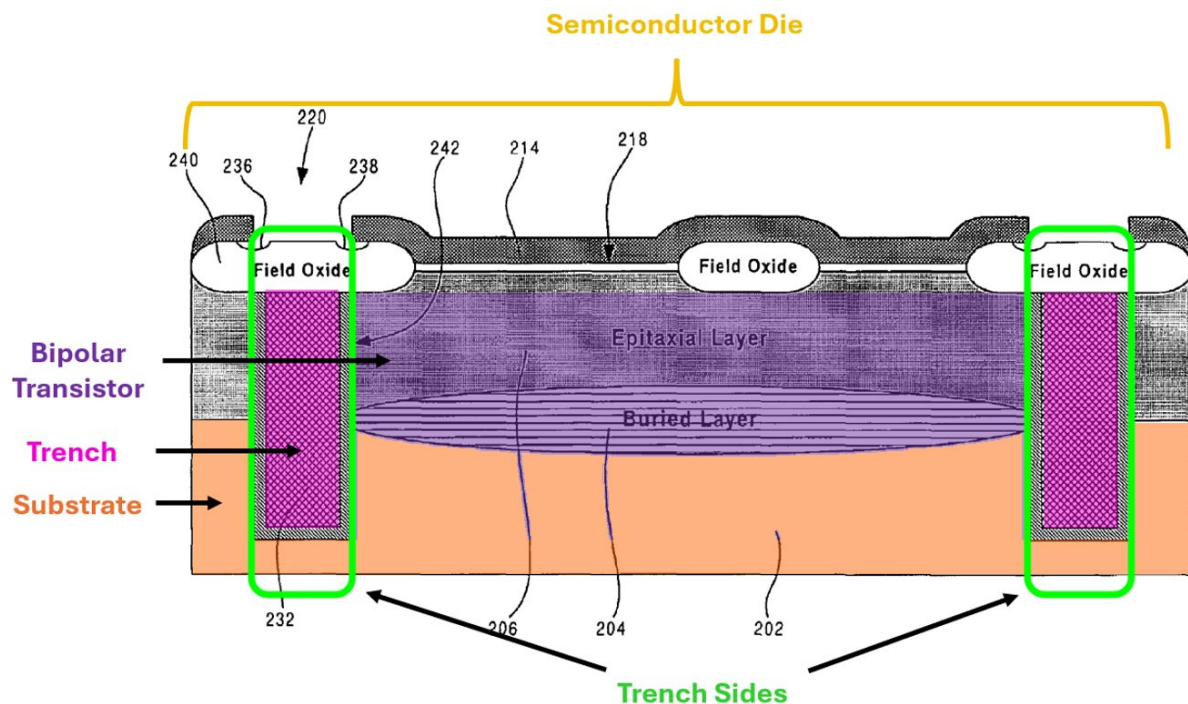
'673
Patent
Fig. 4E



Yin
Fig. 2G



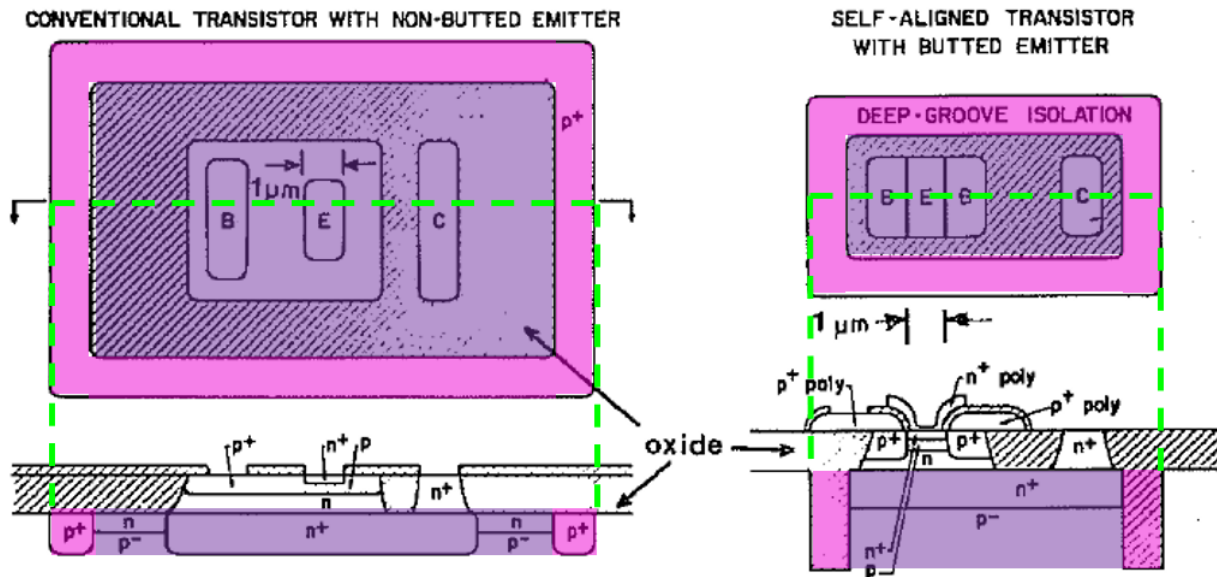
See Thompson Dec., ¶ 94 (citing '673 Patent, Figs. 2, 4E, 4:4-23 (“For example, **bipolar device 204** can be a vertical **bipolar transistor**, such as a vertical NPN or PNP transistor.”) (annotation added); *Yin*, Fig. 2G (annotation added)). The **trench 220** surrounds the **bipolar transistor** and is situated in **substrate 202**:



See Thompson Dec., ¶ 94 (citing *Yin*, Fig. 2G (annotation added); 1:19-27).

Even though *Yin* itself does not provide a top-down view of its **bipolar transistor**, it would have been readily understood by a POSITA to be surrounded by a **four-sided trench**. Thompson Dec., ¶ 95. The manner in which *Yin*'s cut-away is drawn was standard for **four-sided** semiconductor devices before the '673

Patent.³ As an example, this style was used for four-sided devices in textbooks directed to semiconductor devices:



See Thompson Dec., ¶ 95 (citing WOLF, 476 (annotation added)); see also Koshimizu, Figs. 15-16, Figs. 13a-c (showing the same relationship).

In the cut-away view, the two portrayed trenches correspond to two opposite sides of the rectangular die's **four sides**. See Thompson Dec., ¶ 96 (citing WOLF, 476). **Four-sided** semiconductor devices were also the most common type before

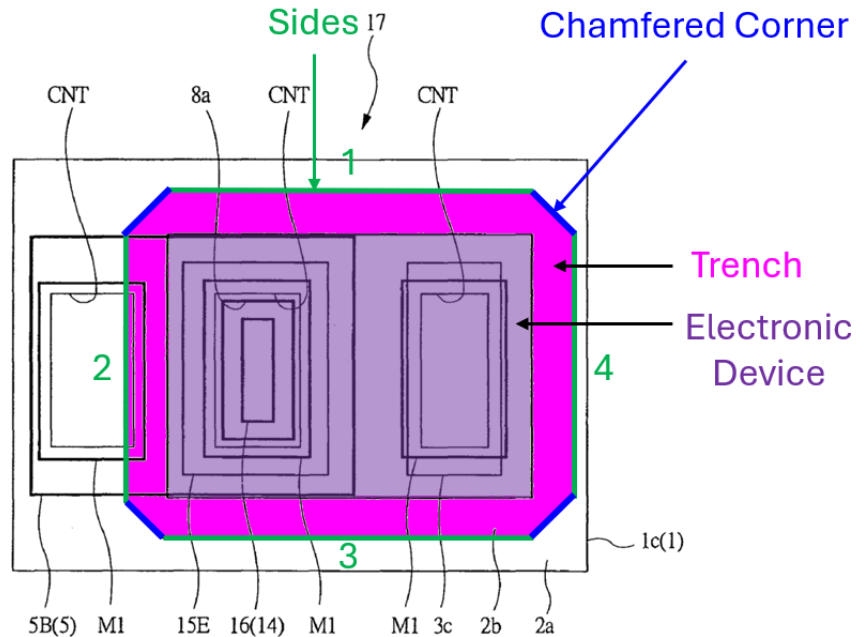
³ It is worth noting once again that the cut-away figures of the '673 Patent (Figs. 4A-F) are nearly identical to those of *Yin* (Figs. 2A-G), and each of the former reflects a semiconductor die with four sides. See Thompson Dec., ¶ 95 (n. 2); '673 Patent, Figs. 1-4.

the '673 Patent and, in the absence of any indication otherwise, a POSITA would have concluded *Yin* disclosed the most common variant. Thompson Dec., ¶ 96 (citing *Yin*, Figs. 2A-G; '673 Patent, Figs. 4A-F; *Verret* (Ex. 1011), Figs. 32-33; *Koshimizu*, Figs. 15-16; *Norström*, Figs. 13a-c; WOLF, 476).

To the extent HID disputes that *Yin* discloses a four-sided trench, it would have been obvious to implement *Yin* using a **four-sided trench** in view of *Koshimizu*'s own **four-sided trench** and the rest of the prior art. Thompson Dec., ¶ 97. As noted above, four-sided trenches were extremely common, and *Koshimizu* discloses the use of one with its chamfered corners. Thompson Dec., ¶ 97 (citing *Yin*, Figs. 2A-G; '673 Patent, Figs. 4A-F; *Verret*, Figs. 32-33; *Koshimizu*, Figs. 15-16; *Norström*, Figs. 13a-c; WOLF, 476). A POSITA would thus not have needed to modify the overall shape of the trench when using this common configuration to integrate *Koshimizu*'s chamfered corner. Thompson Dec., ¶ 97.

For the reasons explained in Section VI.A., a POSITA would have been motivated to add *Koshimizu*'s **chamfered trench corners** to the **semiconductor die** disclosed by *Yin*. These **chamfered corners** are depicted in Figure 16 of *Koshimizu*:

FIG. 16



Thompson Dec., ¶¶ 98-99 (citing *Koshimizu*, Fig. 16 (annotation added)). These **chamfered corners** connect the **four sides** of the **deep trench 2b** in *Koshimizu*.

When integrated into *Yin*'s **semiconductor die**, these **chamfered corners** would have likewise connected the **four sides** of *Yin*'s **deep trench isolation region** in the same manner. Thompson Dec., ¶ 99.

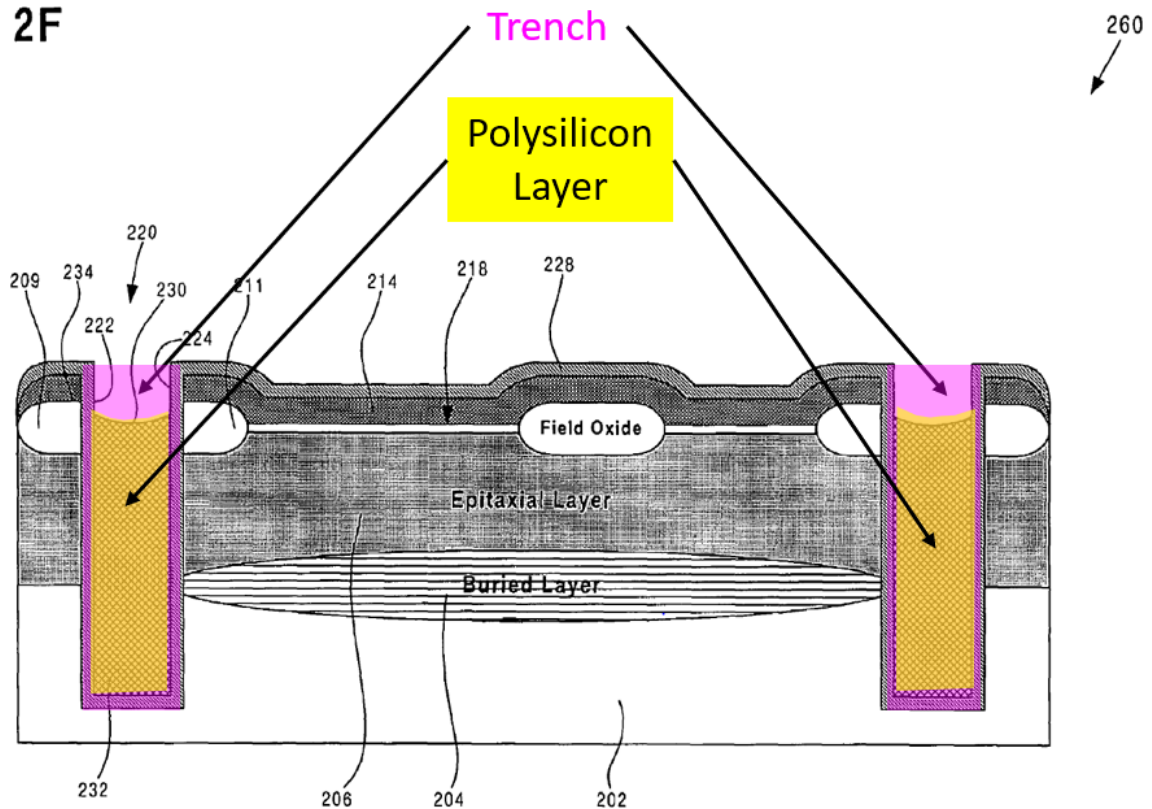
Yin in view of *Koshimizu* thus teaches a trench situated in a substrate of the semiconductor die, said trench having a plurality (*e.g.*, *four*) of sides surrounding said electronic device, and at least one (*e.g.*, *four*) trench chamfered corner formed between and connecting said plurality (*e.g.*, *four*) of sides. Thompson Dec., ¶ 100.

- c. **1[b]: “wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.”**

Yin in view of *Koshimizu* teaches **trench chamfered corners** that cause a reduction in a thickness of a **polysilicon layer** within the **trench**, such as within the corners themselves. Thompson Dec., ¶ 101.

First, *Yin* teaches that its **deep isolation trenches** are filled with **polysilicon**. See *Yin*, 6:29-32 (“[I]n Fig. 2F, at step **160** of flowchart **100**, a **layer of polysilicon** is conformally deposited over substrate **202**[.]”); 6:43-44 (“[T]he **layer of polysilicon** is etched back to depth **230** inside **trench 220** to form **polysilicon portion 232**.”). This is shown, for example, in *Yin* Fig. 2F:

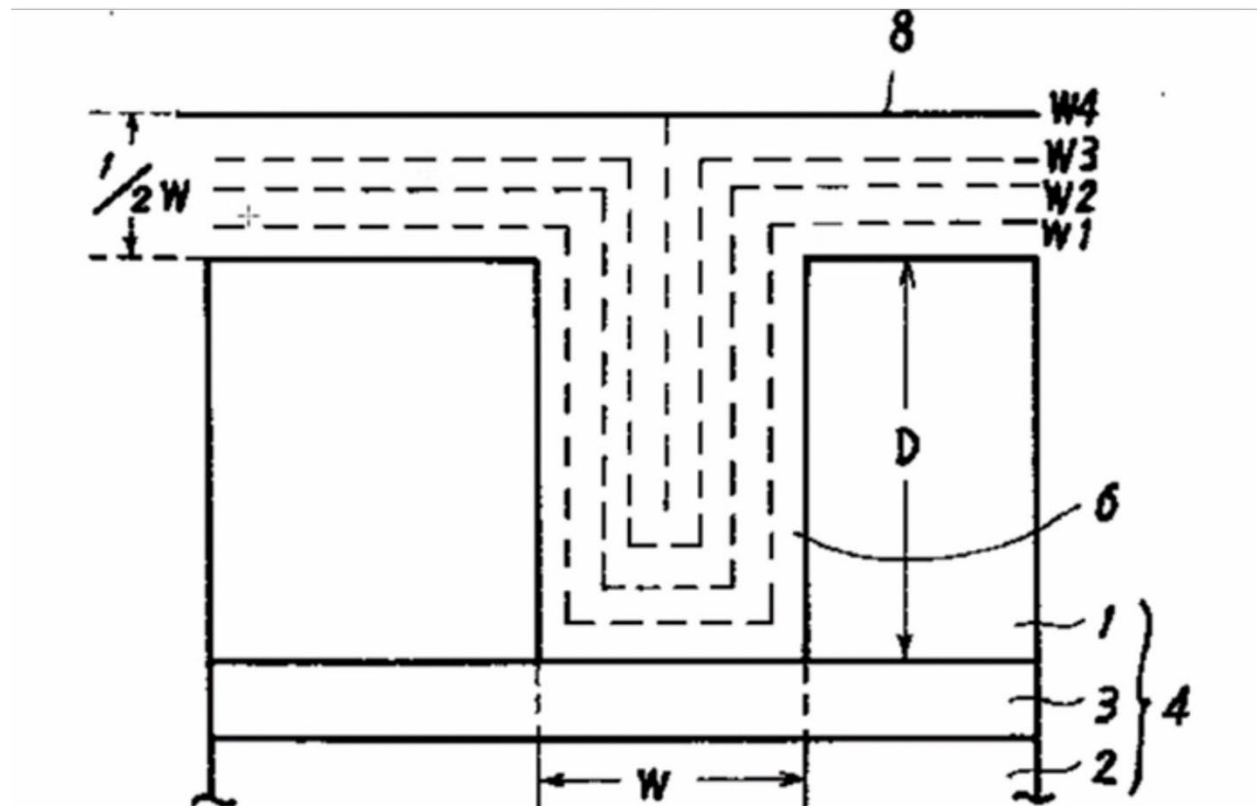
Fig. 2F



See Thompson Dec., ¶ 102 (citing *Yin*, Fig. 2F (annotation added)). Furthermore, *Koshimizu*’s **chamfered corners** considerably reduce the width of the **trench** at the corners where they would otherwise be the widest if left unchamfered. See *supra*, Section VI.A.1.b; Thompson Dec., ¶ 102 (citing *Koshimizu*, Fig. 16); see also ’673 Patent, Fig. 1 (showing wider corners in a “conventional,” prior art unchamfered **trench**).

A POSITA would have understood that the thickness of a layer of **polysilicon** within a **trench** at a given location will be reduced if the width of the trench at that location is likewise reduced. Thompson Dec., ¶ 103. As explained by

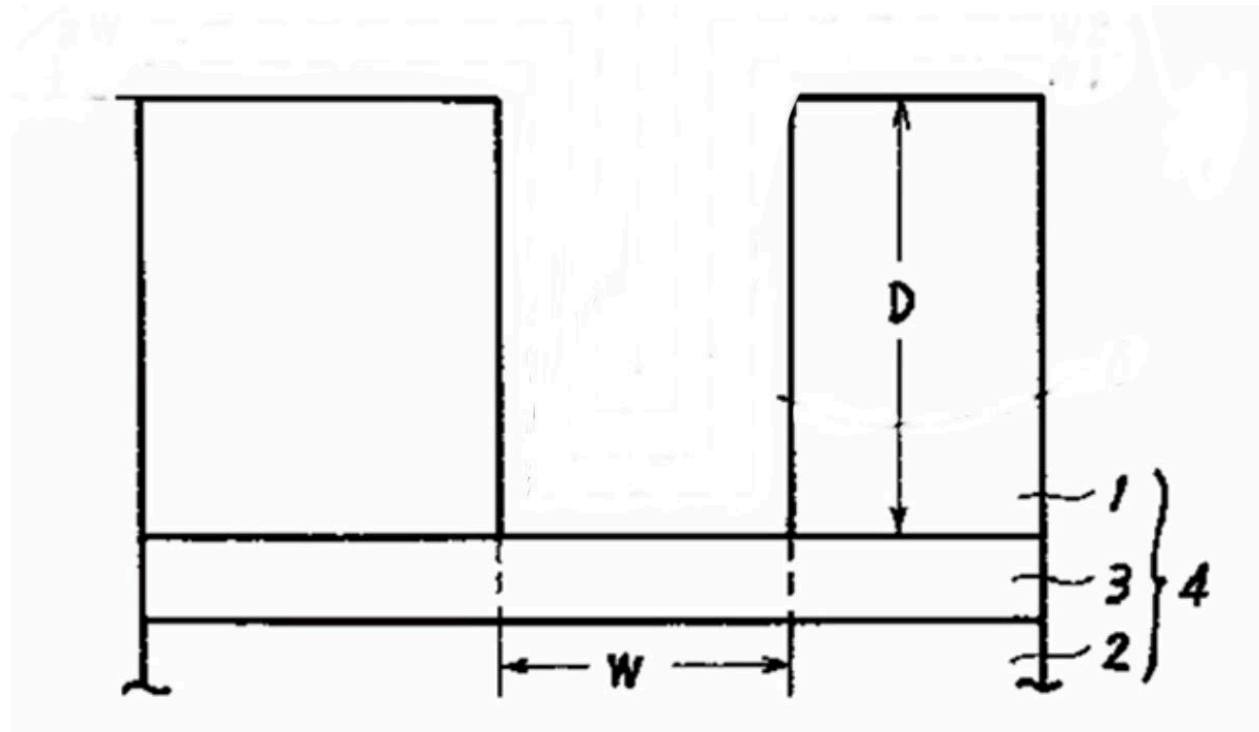
both *Matsuzaki* and WOLF, conformal deposition is the process by which a **deep isolation trench** is refilled with isolating material such as *Yin*'s polysilicon. See *Matsuzaki* (Ex. 1015) 1-4, Fig. 4; see also *Matsuzaki* (JP) (Ex. 1014); WOLF, 56, 62; Thompson Dec., ¶ 103. This process is shown, for example, in *Matsuzaki* Fig. 4:



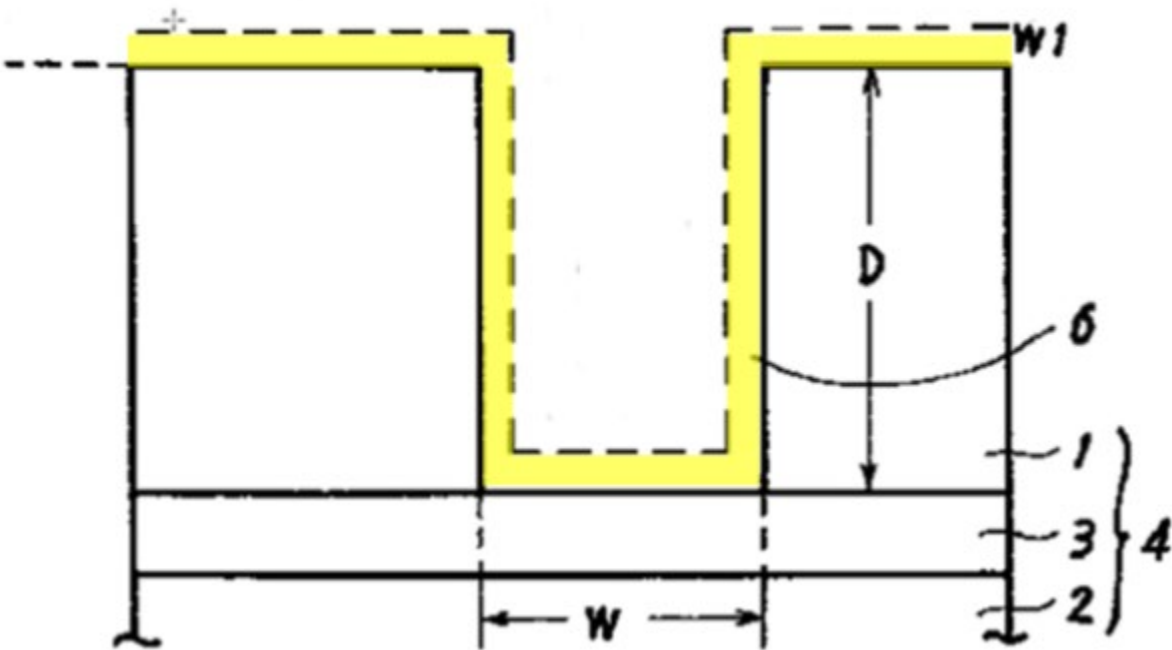
During this process, polysilicon is deposited along the surfaces of the trench (both the sides and bottom) as shown in the sequence below, illustrated by Dr.

Thompson using Fig. 4 of *Matsuzaki*, broken into pieces for each filling stage “W1,” “W2,” “W3,” and “W4.” Thompson Dec., ¶ 104. The deposited layer of

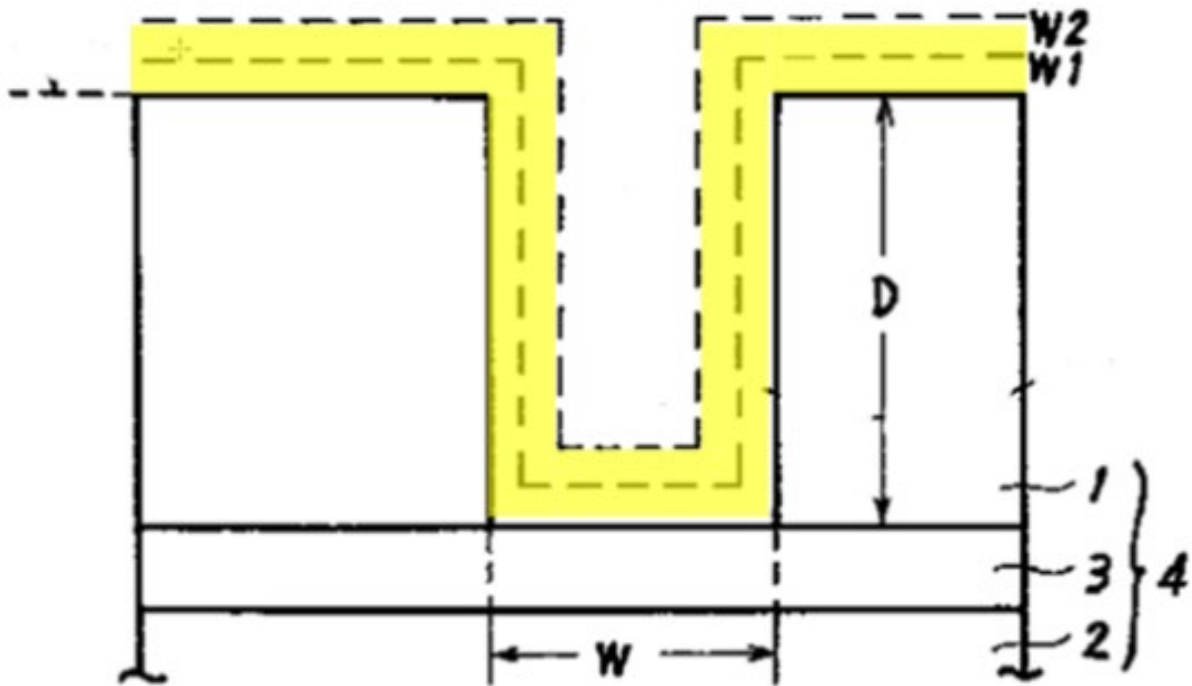
polysilicon grows in thickness until it reaches $W/2$ – or half the width of the trench.



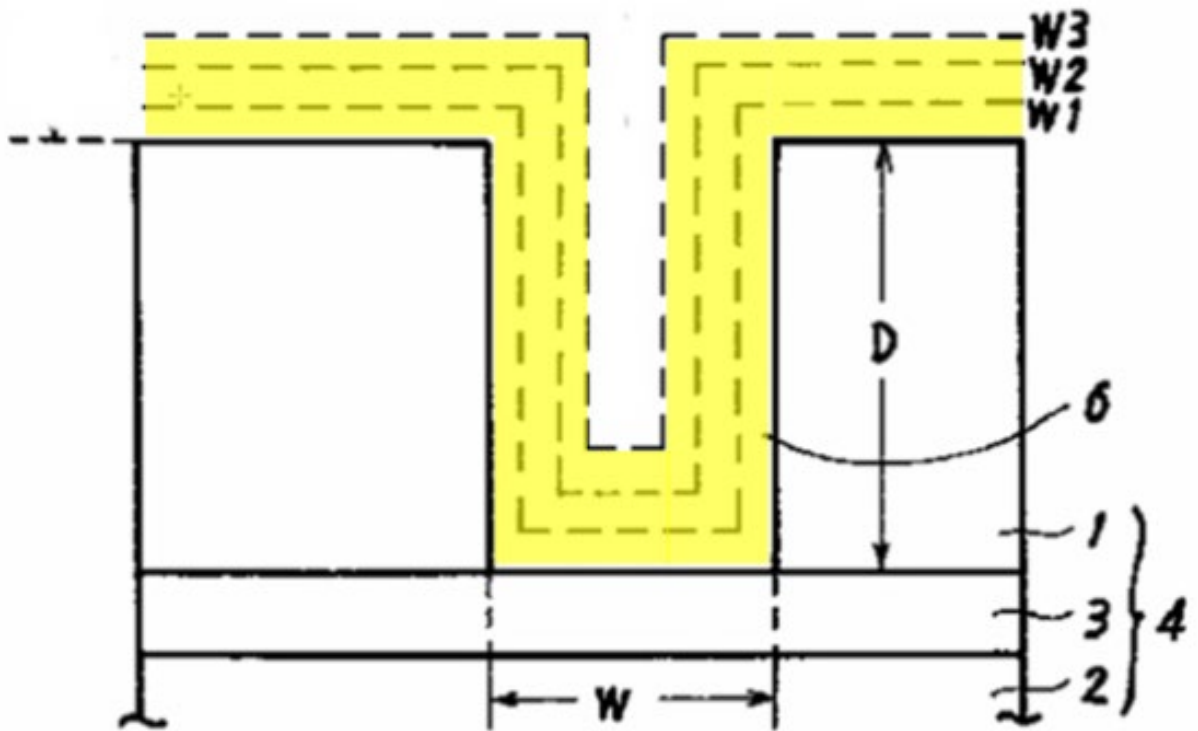
Matsuzaki, Fig. 4 (cropped) (unfilled). In this version of Fig. 4, the trench is dug to a width of “W” and a depth of “D” but no silicon has yet been deposited in it to refill it. Thompson Dec., ¶ 104.



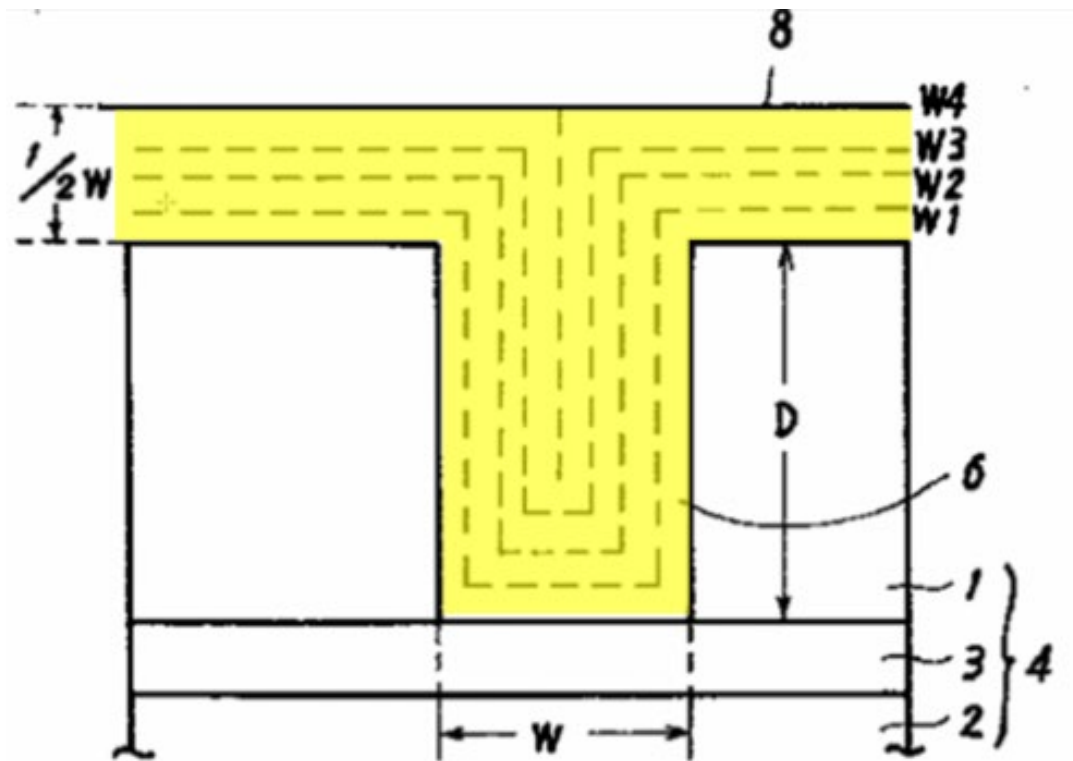
Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to $W1$)). In this version of Fig. 4, the polysilicon layer has been deposited along the sides and bottom of the trench to thickness “ $W1$ ” or $W/8$. Thompson Dec., ¶ 104.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to $W2$)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “ $W2$ ” or $W/4$. Thompson Dec., ¶ 104.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to W3)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “W3” or $3W/8$. Thompson Dec., ¶ 104.



Matsuzaki, Fig. 4 ((annotation added, cropped) (filled to W4)). In this version of Fig. 4, the polysilicon layer has continued to be deposited along the sides and bottom of the trench to thickness “W4” or $W/2$ (shown in the full, uncropped version of Fig. 4). Thompson Dec., ¶ 104.

As shown by Dr. Thompson in these examples, a POSITA would have understood before the '673 Patent that by reducing the width of a trench at a given location, the thickness of the layer of polysilicon within the trench would likewise

be reduced.⁴ *See* Thompson Dec., ¶ 105; *Matsuzaki*, Fig. 4; *see also* WOLF, 56, 62. *Koshimizu*'s **chamfered corners** reduce the width of the widest portion of the **trench** and cause a reduction in thickness of the **polysilicon filling** them in at least the corner portions. Thompson Dec., ¶ 105.

Thus, *Yin* in view of *Koshimizu* teaches a trench chamfered corner that causes a reduction in the thickness of a polysilicon layer within a trench. Thompson Dec., ¶ 106.

2. Claim 2

- a. **“The semiconductor die of claim 1, wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of sides.”**

Yin in view of *Koshimizu* teaches the additional limitation of claim 2. Thompson Dec., ¶ 107.

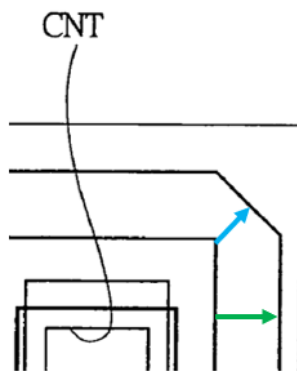
The '673 Patent states that “**trench corner width** . . . represents the perpendicular distance, i.e., the minimum distance, between corners **118** of outside wall **114** and corners **120** of inside wall **116**, and **trench side width** **124**, which

⁴ While a POSITA would not have needed the '673 Patent to understand that narrower trenches yield thinner layers of polysilicon within them, the '673 Patent nevertheless confirms this phenomenon. *See, e.g.*, '673 Patent, 5:15-30.

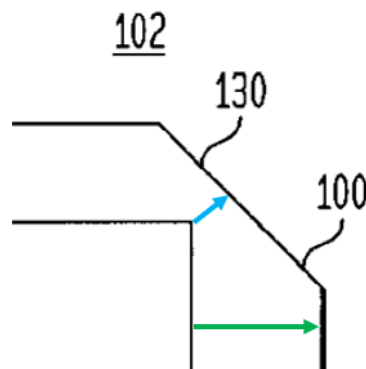
represents the perpendicular distance between outside wall **114** and inside wall **116** along each of sides **117a** through **117d**.” ’673 Patent, 3:12-18. In other words, the “**trench corner width**” and “**trench side width**” refer to the minimum perpendicular distances across the trench’s corners and sides, respectively.

Thompson Dec., ¶ 108.

Koshimizu’s chamfered corners have, as depicted, less width than the trench side widths to which they connect. *See Koshimizu*, Fig. 16; Thompson Dec., ¶ 109. A trench with a lower **trench corner width** than **trench side width** was not uncommon before the ’673 Patent, appearing in other references such as U.S. Patent No. U.S. 6,362,040 to *Tews* as well:



Koshimizu
(Figure 16)



Tews
(Figure 7)

See Thompson Dec., ¶ 109 (citing *Koshimizu*, Fig. 16 (cropped; annotations added); *Tews*, Fig. 7 (cropped, annotations added)). A POSITA would thus have understood *Koshimizu*’s disclosed chamfered corner to be sufficiently chamfered to

have a **trench corner width** that is less than a **trench side width**. Thompson Dec., ¶ 109. *See In re Aslanian*, 590 F.2d 911, 914 (C.C.P.A. 1979) (a drawing teaches all that it “reasonably disclose[s] and suggest[s]” to a POSITA); *see also In re Mraz*, 455 F.2d 1069, 1972 (C.C.P.A. 1972) (supporting the same even if a drawing is not to scale).

A POSITA would have also known before the ’673 Patent that trenches made via the etching process will vary in width during manufacturing due to their very small scale. *See MURDUCK* (Ex. 1013), 288 (“Due to variation in the photolithography process the critical dimension may vary. This could be due to exposure and development of the photoresist or etching of the structure in question and much effort goes into precisely controlling this aspect of the process.”); Thompson Dec., ¶ 110; *Koshimizu* [0048]-[0050]. This means that, as a matter of fact, a trench corner width that is intended to have approximately the same width as trench side widths will occasionally have either more **or less** width due to manufacturing tolerances. Thompson Dec., ¶ 110.

If a POSITA were at all uncertain about whether *Koshimizu*’s chamfered trench corners would be thinner than their surrounding sidewalls (despite them being illustrated that way), the mere selection of parameters—in this case, relative width—is firmly within the realm of obviousness experimentation for a POSITA. *See In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955) (“[W]here the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”); Thompson Dec., ¶ 111 (“ . . . it would have been a matter of obvious experimentation to adjust the trench chamfer width to be slightly narrower—or wider, for that matter—than the trench side walls to optimize for stability and fill speed.”).

A finding of obviousness is especially appropriate where the claimed invention does not provide evidence as to why the claimed range is critical or unexpected. *See In re Hoeschele*, 406 F.2d 1403 (C.C.P.A. 1969) (finding claimed elastomeric polyurethanes that fell within the broad scope of the references were held to be unpatentable thereover because, among other reasons, there was no evidence of the criticality of the claimed ranges of molecular weight or molar proportions). Here, the ’673 Patent states that a reduction in the width of the trench corners can improve the polysilicon refill process. *See* ’673 Patent, 5:15-30. But the ’673 Patent never establishes or provides any evidence as to why reducing the width of those corners to specifically be “less than a trench side width” is critical, provides unexpected results, or is significant in any way over simply reducing the trench corner width over an unchamfered corner *generally*. *See* ’673 Patent, 5:15-30.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 2’s additional limitation. Thompson Dec., ¶ 112.

3. Claim 3

- a. **“The semiconductor die of claim 1, wherein said at least one trench chamfered corner comprises a portion of said trench situated between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.”**

Yin in view of *Koshimizu* teaches the additional limitation of claim 3. *See* Thompson Dec., ¶ 114.

Koshimizu’s Figure 16 teaches the **chamfering** of a **corner of an outside wall** of a **trench**. The **“trench chamfered corner”** thus comprises a portion of the **trench** and is situated between the **chamfered corner of an outside wall** of the **trench** and a **corner of an inside wall of the trench**. *See* Thompson Dec., ¶¶ 115-116 (citing *Koshimizu*, Fig. 16; [0051]-[0061]).

FIG. 16



Trench
Chamfered
Corner

Trench

Corner of an Inside Wall

Koshimizu, Fig. 16 (annotation added).

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 3's additional limitation. Thompson Dec., ¶ 117.

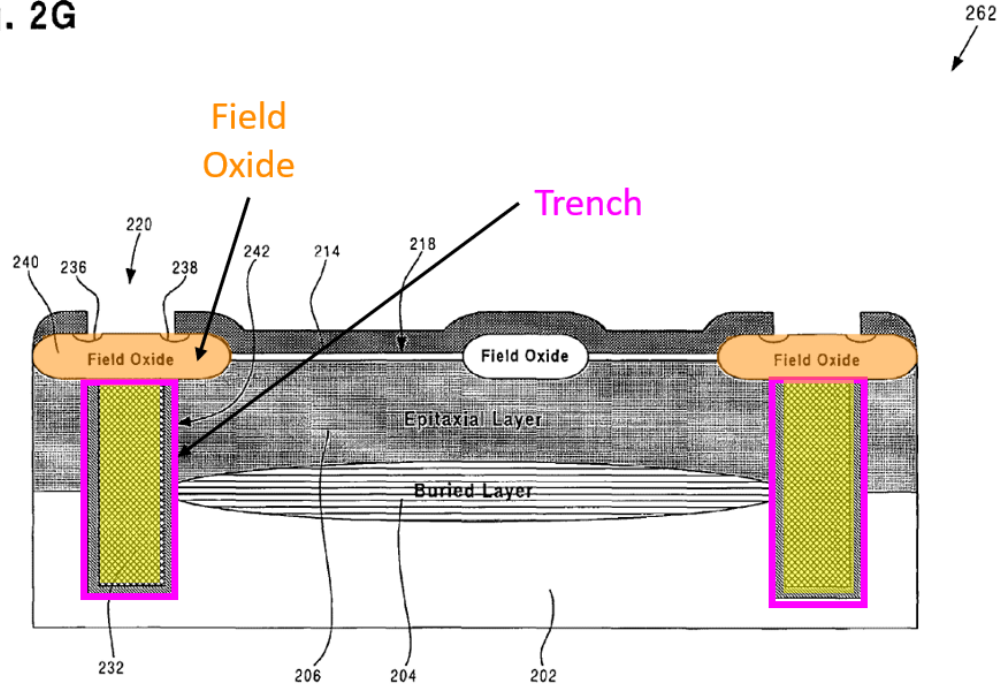
4. Claim 4

a. “The semiconductor die of claim 1, wherein a field oxide region overlies said trench.”

Yin in view of *Koshimizu* teaches the additional limitation of claim 4.

Thompson Dec., ¶ 118. As shown in Figure 2G of *Yin*, a **field oxide region** overlies its **deep isolation trench**:

Fig. 2G



See Thompson Dec., ¶ 118 (citing *Yin*, Fig. 2G (annotation added), 6:54-65).

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 4’s additional limitation. Thompson Dec., ¶ 119.

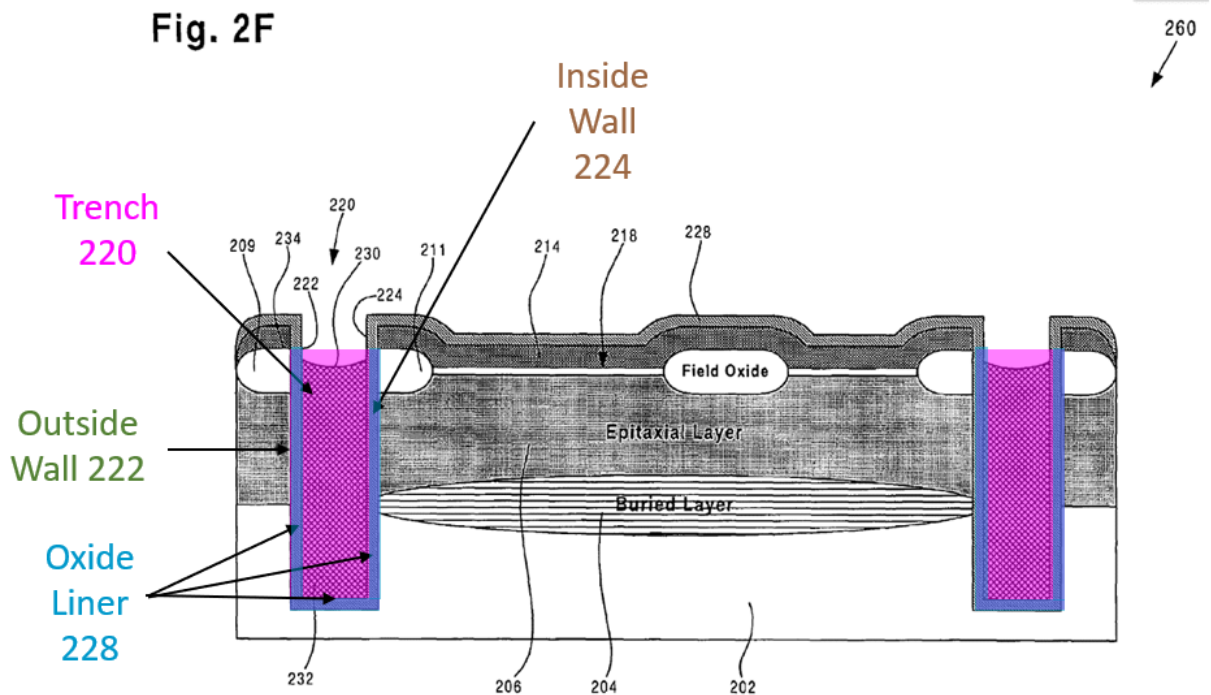
5. Claim 5

- a. “The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on an inside wall and an outside wall of said trench.”

Yin in view of *Koshimizu* teaches the additional limitation of claim 5.

Thompson Dec., ¶ 120.

As shown in *Yin* Figure 2F, an **oxide liner** is situated on the **inner** and **outer** walls of **trench 220**:



Yin, Fig. 2F; *see also Yin*, 6:13-16 (“Next, **oxide liner 228**, also referred to as a ‘CVD oxide liner’ in the present application, is formed by depositing a layer of TEOS oxide on sidewalls **222** and **224** and bottom surface **226** of **trench 220**”); Thompson Dec., ¶ 121.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 5’s additional limitation. Thompson Dec., ¶ 122.

6. Claim 6

- a. “The semiconductor die of claim 2, wherein said trench side width along said plurality of sides is approximately 1.0 micron.”

Yin in view of *Koshimizu* teaches the additional limitation of claim 6.

Thompson Dec., ¶ 124. *Yin* discloses that the side width of its trench sidewalls is

approximately 1.0 micron. *See Yin*, 4:64-67 (“The width of trench 220 . . . can be, for example, approximately 1.0 micron.”); Thompson Dec., ¶ 124.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 6’s additional limitation. Thompson Dec., ¶ 125.

7. Claim 7

- a. “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”**

Yin in view of *Koshimizu* teaches the additional limitation of claim 7. Thompson Dec., ¶ 126.

Yin discloses that its semiconductor die is designed for a “Bipolar Complementary-Metal-Oxide-Semiconductor (‘BiCMOS’) process” in which “deep trench isolation regions are typically formed to provide isolation between adjacent active regions of a semiconductor substrate.” *Yin*, 1:15-19. *Yin* further discloses that its “deep trench isolation region may electrically isolate, for example, a bipolar transistor . . . from an adjacent CMOS transistor, such as a PFET, fabricated on the same semiconductor substrate.” *Yin*, 1:19-24. “BiCMOS” technology with multiple bipolar transistor devices in one semiconductor package or chip was standard use for bipolar transistor devices before the ’673 Patent. Thompson Dec., ¶¶ 127-28; *see* SHEPHERD (Ex. 1012), 1-7. A POSITA would thus have understood that *Yin*’s disclosed semiconductor die was or would be enclosed

in a semiconductor package with neighboring semiconductor devices from which electrical isolation was necessary and/or desirable. Thompson Dec., ¶¶ 127-28.

To the extent HID contends otherwise, it would have been obvious to enclose *Yin*'s semiconductor die in a semiconductor package in view of the level of ordinary skill in the art. The primary purpose of a deep isolation trench is to isolate a device—in this case, a bipolar transistor—from neighboring devices on the same semiconductor package. Thompson Dec., ¶¶ 129-131 (citing *Yin*, 1:19-24). As one example, computer chips such as high-density complementary MOS (“CMOS”) chips employ semiconductor packages enclosing multiple bipolar transistors. Thompson Dec., ¶¶ 130-31 (citing SHEPHERD, 1-7). Semiconductor devices such as *Yin*'s isolated bipolar transistor are customarily used in semiconductor wafers (which the '673 patent refers to semiconductor dies, *see* '673 Patent, 5:55-57) which are in turn customarily integrated into packages for use in computing applications—and they had been for decades before the '673 Patent. *See* Thompson Dec., ¶ 128 (citing WOLF, 1-5).

A POSITA would have had a reasonable expectation of success in using *Yin*'s semiconductor die in a semiconductor package, since packaging a die was a common practice and required only simple steps such as placing the semiconductor die in a package made out of plastic or other commonly available materials. Thompson Dec., ¶¶ 129-130. A POSITA would thus have found it obvious to use

Yin's semiconductor die in an application enclosing it in a semiconductor package with multiple similar or identical semiconductor devices.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 7's additional limitation. Thompson Dec., ¶ 130.

8. Claim 8

- a. “The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.”**

Yin in view of *Koshimizu* teaches the additional limitation of claim 8. Thompson Dec., ¶ 132. *Yin* discloses that its “deep trench isolation region may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium heterojunction bipolar transistor[.]” *Yin*, 1:19-22; Thompson Dec., ¶ 133.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 8's additional limitation. Thompson Dec., ¶ 134.

9. Claim 9

- a. “The semiconductor die of claim 1, wherein said electronic device is a silicon-germanium bipolar transistor.”**

Yin in view of *Koshimizu* teaches the additional limitation of claim 9. Thompson Dec., ¶ 135. *Yin* discloses that its “deep trench isolation region may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium heterojunction bipolar transistor[.]” *Yin*, 1:19-22; Thompson Dec., ¶ 136.

Therefore, *Yin* in view of *Koshimizu* renders obvious claim 9's additional limitation. Thompson Dec., ¶ 137.

10. Independent Claim 10

- a. **10[pre]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”**

To the extent the preamble is limiting, *Yin* in view of *Koshimizu* renders this limitation obvious for the same reasons as stated in claim 1[pre]. *See* claim 1[pre], *supra*.

- b. **10[a]: “at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;”**

Yin in view of *Koshimizu* renders this limitation obvious for the same reasons as stated in claim 1[a]. *See* claim 1[a], *supra*.

- c. **10[b]: “each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.”**

Yin in view of *Koshimizu* renders this limitation obvious for the same reasons as stated in claim 1[b]. *See* claim 1[b], *supra*.

11. Claim 11

- a. “The semiconductor die of claim 10, wherein a trench corner width at each of said four trench chamfered corners is less than a trench side width along each of said four sides of said at least one trench.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 2. *See* claim 2, *supra*.

12. Claim 12

- a. “The semiconductor die of claim 10, wherein said each of said four trench chamfered corners comprises a portion of said at least one trench situated between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 3 *See* claim 3, *supra*.

13. Claim 13

- a. “The semiconductor die of claim 10, wherein a field oxide region overlies said at least one trench.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 4. *See* claim 4, *supra*.

14. Claim 14

- a. “The semiconductor die of claim 10, wherein said at least one trench further comprises an oxide liner situated on an inside wall and an outside wall of said at least one trench.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 5. *See* claim 5, *supra*.

15. Claim 15

- a. “The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 7. *See* claim 7, *supra*.

16. Claim 16

- a. “The semiconductor die of claim 10, wherein said electronic device is a bipolar transistor.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 8. *See* claim 8, *supra*.

17. Claim 17

- a. “The semiconductor die of claim 10, wherein said electronic device is a silicon-germanium bipolar transistor.”**

Yin in view of *Koshimizu* renders this additional limitation obvious for the same reasons as stated for claim 9. *See* claim 9, *supra*.

B. Ground 2: Claims 1, 3, 5, 7-8, 10, 12, and 14-16 Are Anticipated By *Norström*

1. Independent Claim 1

- a. 1[pre]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”

To the extent the preamble is limiting, *Norström* discloses a **semiconductor die** including at least one **deep trench isolation region** for isolating an **electronic device**, *e.g.*, a **bipolar transistor**. Thompson Dec., ¶ 148.

Norström discloses that its “present invention relates to bipolar semiconductor devices, in particular **bipolar transistors** and semiconductor diodes, which are electrically isolated or confined by **trenches**.” *Norström*, 1:7-10; Thompson Dec., ¶ 149. One example of this is shown in Fig. 13a, where a **semiconductor die** has a **bipolar transistor** electrically isolated by a **deep trench isolation region**:

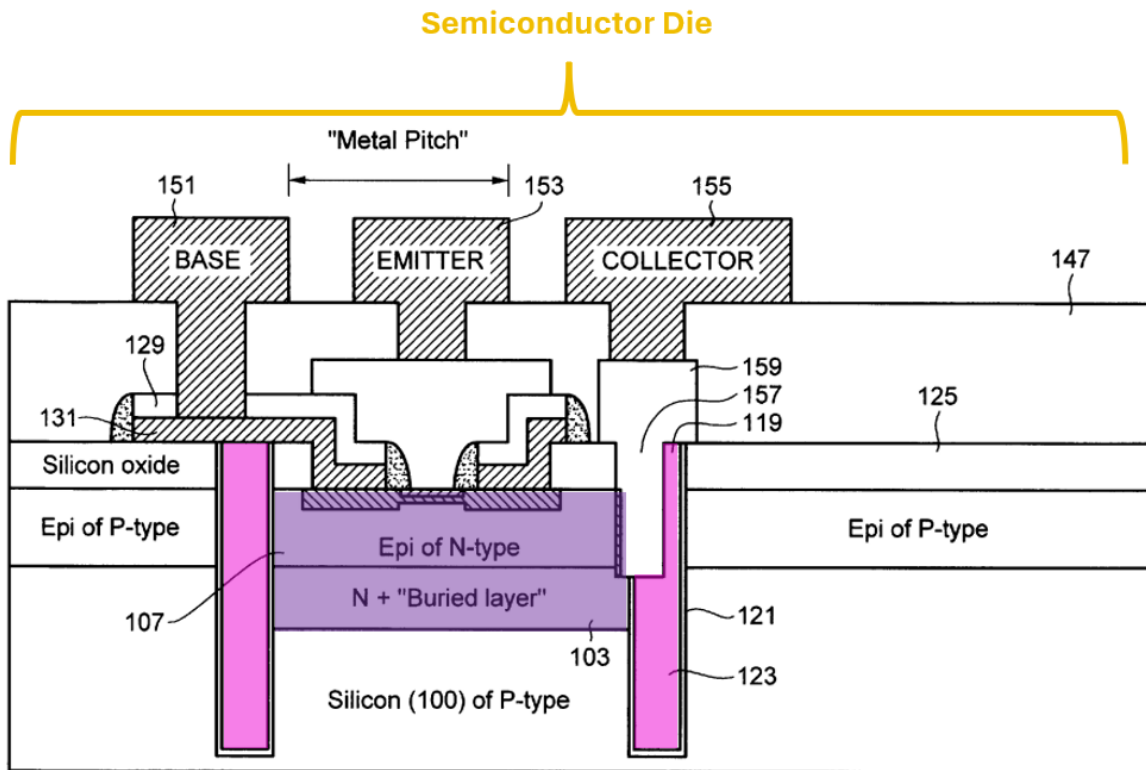


FIG. 13a

Norström, Fig. 13a (annotation added), Figs. 8-13 (showing manufacturing process); 6:24-27 (“Fig. 13a is a schematic cross sectional view . . . of the finished NPN transistor[.]”); Thompson Dec., ¶ 149.

Norström thus discloses a **semiconductor die** including at least one **deep trench isolation region** for isolating an **electronic device**, *e.g.*, a **bipolar transistor**. Thompson Dec., ¶ 150.

- b. 1[a]: “a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner between and connecting said plurality of sides;”

Norström discloses a **four-sided trench** situated in a **substrate** of said **semiconductor die**, said **trench** surrounding an **electronic device** and having four **trench chamfered corners** (i.e., at least one) connecting said **four sides**.

Thompson Dec., ¶ 151.

Figure 13c of *Norström* depicts the top view of the **semiconductor die** from Figure 13a:

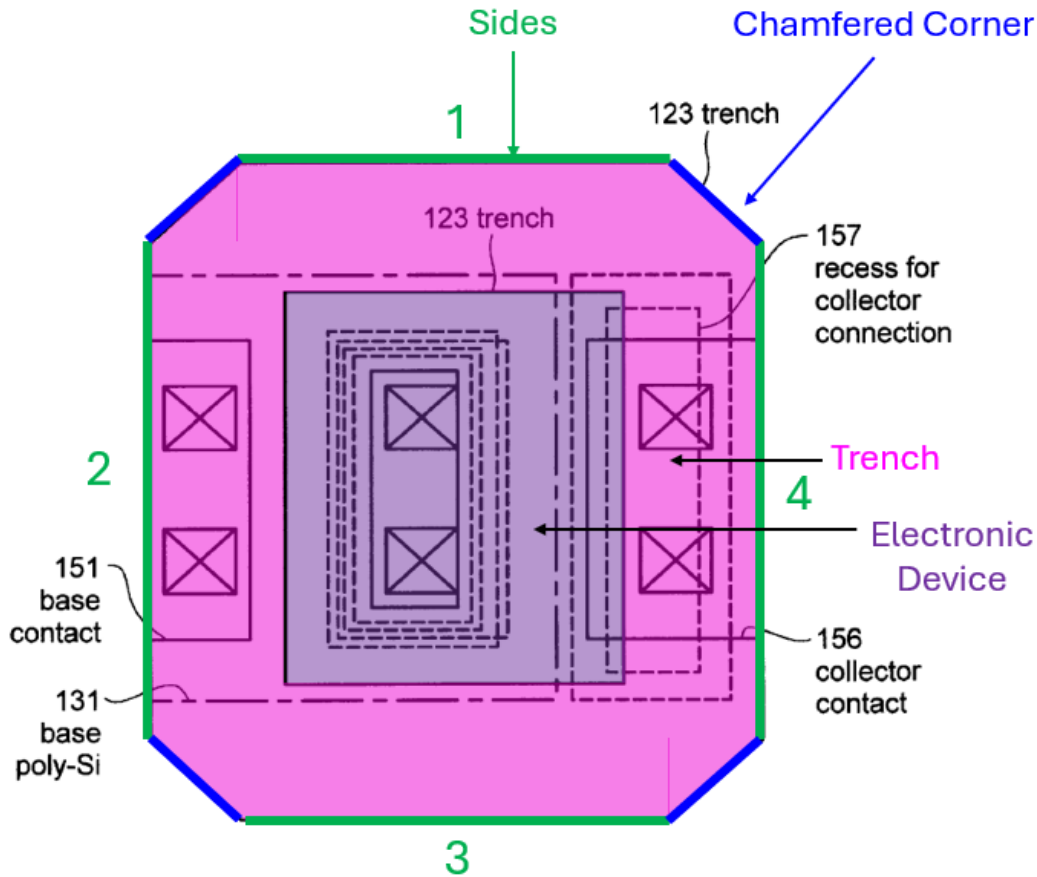


FIG. 13c

Thompson Dec., ¶ 152 (citing *Norström*, Fig. 13c (annotation added); 6:32-34; 11:6-7 (“The result appears from Fig. 13a, see also the plan view of Fig. 13c.”)). As shown in Figure 13c, *Norström*’s **trench 123** surrounds the **bipolar NPN transistor** within, which is an **electronic device**. Thompson Dec., ¶ 152 (citing *Norström*, Figs. 13a & c). *Norström*’s **trench 123** also has **four sides**. Thompson Dec., ¶ 152 (citing *Norström*, Fig. 13c). Figure 13c also depicts the four **trench chamfered corners** at the outer edge of **trench 123** connecting the **four sides** of the **trench**. Thompson Dec., ¶ 152 (citing *Norström*, Fig. 13c).

Norström provides specific angles for its **trench chamfered corners**, noting that “the outer sidewalls of the **trench 123** shown in Fig. 13c have no right angles, but the flat sidewall segments form an angle of 135° to each other.” *Norström*, 16:39-42. Thompson Dec., ¶ 153.

Figure 13a shows that both the **trench** and the **electronic device** (the **NPN bipolar transistor**) are situated in a **substrate** of silicon within the semiconductor die:

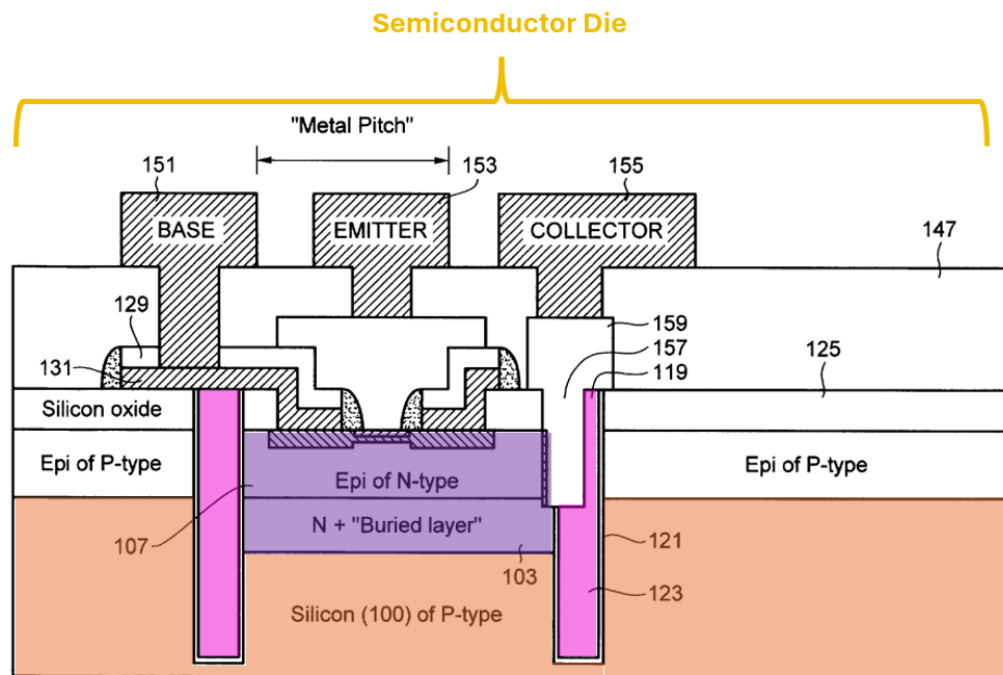


FIG. 13a

Thompson Dec., ¶ 154; Norström, Fig. 13a (annotation added), 9:31-55 (describing the features of Figures 8-13 being situated into a “P-type” **substrate**). Thompson Dec., ¶ 154.

Therefore, *Norström* discloses a trench situated in a substrate of the semiconductor die, said trench having a plurality (*e.g., four*) of sides surrounding said electronic device, and at least one (*e.g., four*) trench chamfered corner formed between and connecting said plurality (*e.g., four*) of sides. Thompson Dec., ¶ 155.

c. 1[b]: “wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.”

Norström discloses **trench chamfered corners that** cause a reduction in a thickness of a **polysilicon layer** within the **trench**, such as within the corners themselves. Thompson Dec., ¶ 156.

First, *Norström* discloses that its **isolation trenches** may be filled with **polysilicon**. *Norström*, 7:47-50 (“[T]he trenches are filled with an isolating or semi-isolating material **123**, for example, silicon oxide or polycrystalline silicon[.]”); Thompson Dec., ¶ 157.

For the reasons explained for Ground 1, a POSITA would have understood that by chamfering the outer corners of a deep isolation trench, the thickness of the polysilicon layer within the trench would be reduced at the narrower chamfered corner. *See* Section VI.A.1.c, *supra*; Thompson Dec., ¶ 158. In addition to these reasons, *Norström* specifically discloses that chamfered outer trench corners improve the refill process over non-chamfered corners. As *Norström* explains:

It should be observed that the exterior corners of the isolating trench 257, which surrounds the PNP-transistor as a frame, has [sic] been made oblique by an angle of about 45° ***in order to improve the refilling of the trench***. It appears advantageous to always form a deep groove, which is to be filled with some material, such as isolating or conducting material, to have walls, which do not form comers [sic] having angles about 90°, but these angles should instead be as large as possible, for example 135°.

Norström, 16:28-36 (emphasis added). In other words, *Norström* discloses the same chamfer and reasoning for using that chamfer the '673 Patent itself disclosed – i.e., that these chamfered corners improve the trench refill process and reduce polysilicon waste. *See* Thompson Dec., ¶ 158; '673 Patent, 9:6-10 (“As a result, the invention’s deep trench isolation region significantly increases polysilicon fill process throughput and the average time between polysilicon deposition furnace cleaning, thereby advantageously reducing manufacturing cost.”).

Thus, *Norström* discloses a trench chamfered corner that causes a reduction in the thickness of a polysilicon layer within a trench. Thompson Dec., ¶ 159.

2. Claim 3

- a. “The semiconductor die of claim 1, wherein said at least one trench chamfered corner comprises a portion of said trench situated between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.”

Norström discloses the additional limitation of claim 3. Thompson Dec., ¶ 160.

As explained for Claim 1[a], *Norström*’s Figure 13c discloses the **chamfering** of a **corner of an outside wall** of a **trench**. The “**trench chamfered corner**” thus comprises a portion of the **trench** and is situated between the **chamfered corner of an outside wall** of the **trench** and a **corner of an inside wall of the trench**:

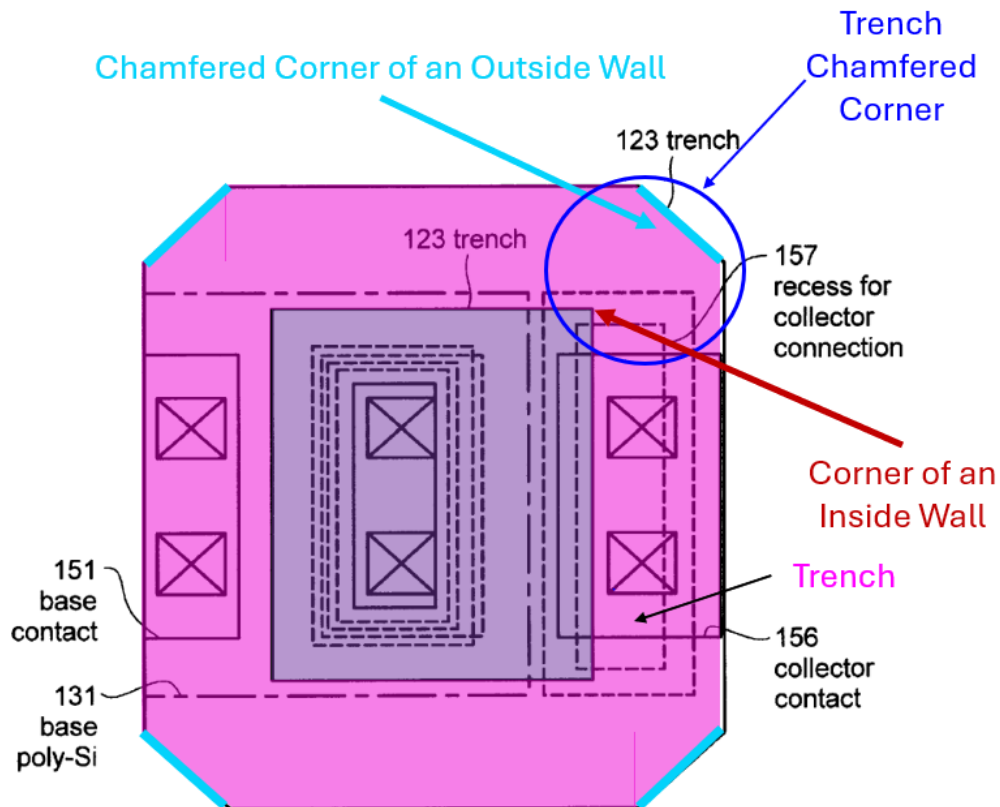


FIG. 13c

See Thompson Dec., ¶ 161 (citing *Norström*, Fig. 13c (annotation added); 16:28-36).

Therefore, *Norström* anticipates claim 3’s additional limitation. Thompson Dec., ¶ 162.

3. Claim 5

- a. **“The semiconductor die of claim 1, wherein said trench further comprises an oxide liner situated on an inside wall and an outside wall of said trench.”**

Norström discloses the additional limitation of claim 5. Thompson Dec.,

¶ 163.

Norström discloses that the semiconductor die depicted in Figures 13a and 13c contains a **thin surface layer of silicon oxide** on their **sidewalls**. See *Norström*, 9:42-44 (“The **trenches 119** are then thermally oxidized so that their **sidewalls** and bottom surfaces obtain a **thin surface layer 121 of silicon oxide**[.]”) (annotation added); A POSITA would have understood this “**thin surface layer . . . of silicon oxide**” to be an **oxide liner**. Thompson Dec., ¶ 164; see ’673 Patent, 3:29-50 (describing a thin layer of “silicon oxide” as an “oxide liner”). This is depicted in *Norström* Fig. 13a:

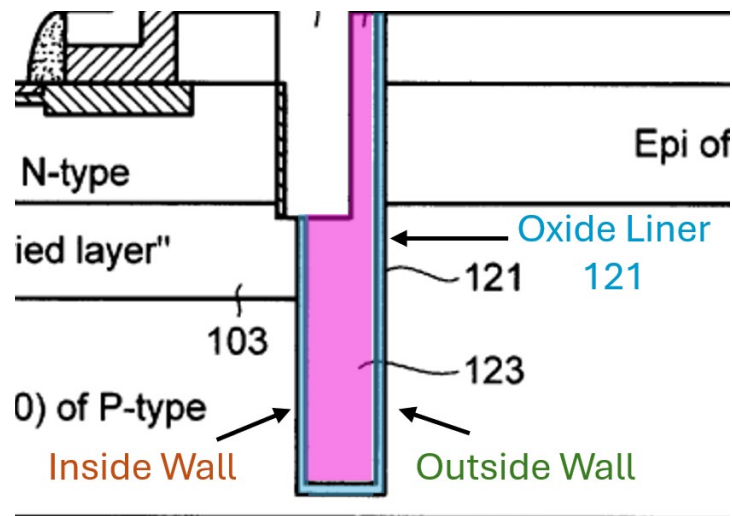


FIG. 13a

Thompson Dec., ¶ 164, *Norström*, Fig. 13a (cropped, annotation added).

Therefore, *Norström* anticipates claim 5’s additional limitation. Thompson

Dec., ¶ 165.

4. Claim 7

- a. “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”**

Norström discloses the additional limitation of claim 7. Thompson Dec., ¶ 166.

Norström discloses that its subject matter is directed towards bipolar transistors manufactured on “the same silicon plate” that can be “isolated from each other by areas comprising deep P-diffusions, which extend through the epitaxial layer down to the inner or interior material of the silicon plate, i.e., the substrate, which in these cases is silicon of P-type.” *Norström*, 1:29-34; Thompson Dec., ¶ 167. A POSITA would have understood the silicon plate to be the semiconductor package on which multiple isolated bipolar transistors—as well as the semiconductor die they are printed on—are housed next to each other. Thompson Dec., ¶ 167.

Therefore, *Norström* anticipates claim 7’s additional limitation. Thompson Dec., ¶ 168.

5. Claim 8

- a. “The semiconductor die of claim 1, wherein said electronic device is a bipolar transistor.”**

Norström discloses the additional limitation of claim 8. Thompson Dec., ¶ 169.

Norström explains that Figure 13 depicts an **NPN-type bipolar transistor** with **deep isolation trenches** electrically isolating the **transistor**. Thompson Dec., ¶ 170; *Norström*, 6:23-34; *see also id.*, 8:50-11:40 (describing the manufacturing process for the same); 1:7-10 (noting disclosure is directed to “bipolar semiconductor devices, in particular **bipolar transistors** and **semiconductor diodes**, which are electrically isolated or confined by **trenches**.”).

Therefore, *Norström* anticipates claim 8’s additional limitation. Thompson Dec., ¶ 171.

6. Independent Claim 10

- a. 10[pre]: “A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:”**

To the extent the preamble is limiting, *Norström* discloses it for the same reasons as stated in claim 1[pre]. *See* claim 1[pre], *supra*.

- b. 10[a]: “at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;”**

Norström discloses this limitation for the same reasons as stated in claim

1[a]. *See* claim 1[a], *supra*.

- c. 10[b]: “each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.”**

Norström discloses this limitation for the same reasons as stated in claim

1[b]. *See* claim 1[b], *supra*.

7. Claim 12

- a. “The semiconductor die of claim 10, wherein said each of said four trench chamfered corners comprises a portion of said at least one trench situated between a respective chamfered corner of an outside wall of said at least one trench and a corner of an inside wall of said at least one trench.”**

Norström anticipates this additional limitation for the same reasons as stated in claim 3. *See* claim 3, *supra*.

8. Claim 14

- a. “The semiconductor die of claim 10, wherein said at least one trench further comprises an oxide liner situated on an inside wall and an outside wall of said at least one trench.”**

Norström anticipates this additional limitation for the same reasons as stated in claim 5. *See* claim 5, *supra*.

9. Claim 15

- a. “The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package.”**

Norström anticipates this additional limitation for the same reasons as stated in claim 7. *See* claim 7, *supra*.

10. Claim 16

- a. “The semiconductor die of claim 10, wherein said electronic device is a bipolar transistor.”**

Norström anticipates this limitation for the same reasons as stated in claim 8. *See* claim 8, *supra*.

C. Ground 3: Claims 7 and 15 Would Have Been Obvious Over *Norström*

1. Claim 7

- a. “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”**

To the extent HID contends that *Norström* does not disclose the additional

limitation of claim 7, a POSITA would have found it obvious over *Norström*.

Thompson Dec., ¶ 180.

Norström discloses each of the limitations of independent claim 1 for the same reasons stated in Ground 2. It would have then been obvious to enclose *Norström*'s semiconductor die in a semiconductor package in view of the level of ordinary skill in the art. The primary purpose of a deep isolation trench is to isolate a device—in this case, a bipolar transistor—from neighboring devices on the same semiconductor package. Thompson Dec., ¶ 181 (citing *Norström*, 1:29-34). As one example, computer chips such as high-density complementary MOS (“CMOS”) chips employ semiconductor packages enclosing multiple bipolar transistors. Thompson Dec., ¶ 181 (citing SHEPHERD, 1-7). Semiconductor devices such as *Norström*'s isolated bipolar transistor are customarily used in semiconductor wafers (which the '673 Patent refers to as semiconductor dies, *see* '673 Patent, 5:55-57) which are in turn customarily integrated into packages for use in computing applications—and they had been for decades before the '673 Patent. *See* Thompson Dec., ¶ 181 (citing WOLF, 1-5).

A POSITA would have had a reasonable expectation of success in using *Norström*'s semiconductor die in a semiconductor package, since packaging a die was a common practice and only required simple steps such as placing the semiconductor die in a package made out of plastic or other commonly available

materials. Thompson Dec., ¶ 182. A POSITA would thus have found it obvious to use *Norström*'s semiconductor die in an application enclosing it in a semiconductor package with multiple similar or identical semiconductor devices.

Therefore, *Norström* renders obvious claim 7's additional limitation.

Thompson Dec., ¶ 183.

2. Claim 15

- a. “The semiconductor die of claim 10, wherein said semiconductor die is enclosed in a semiconductor package.”**

Norström discloses each of the limitations of claim 10 for the same reasons stated in Ground 2. *Norström* renders obvious the additional limitation of claim 15 for the same reasons as stated in claim 7. *See* claim 7, *supra*.

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office's interim guidelines dated June 21, 2022 (“Interim Procedures”) require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions only on July 18, 2024. *See* Ex. 1016. Fact discovery opened only last month, and

will not close until August 18, 2025, with expert discovery closing September 22, 2025. *See* Ex. 1017, 3. The parties will not begin claim construction until March 4, 2025, and the hearing will not take place until July 8, 2025. *Id.*, 3-4.

Factor 4 favors institution because this Petition additionally challenges claims 2, 4, 6, 8, 9, 11, 13, 16, 17, which are not involved in the litigation. Moreover, Petitioner has not served invalidity contentions, so no overlap currently exists. Petitioner reserves the right to submit a stipulation after serving invalidity contentions.

Regarding Factors 1, 2, and 5, no stay has been requested, and trial is currently scheduled for January 5, 2026, (*id.*, 1), two months before the anticipated FWD in March 2026. In these circumstances, Factors 1, 2, and 5 are at worst neutral. *Protect Animals with Satellites v. OnPoint Sys.*, IPR2021-01483, Paper 11 at 12-13, 17 (Mar. 4, 2022). Indeed, the Board has instituted with far more time between trial and FWD. *See NetNut v. Bright Data*, IPR2021-01492, Paper 12 at 9-16 (Mar. 21, 2022) (instituting IPR without stipulation and patent owner arguing trial date six months before FWD); *Protect Animals*, IPR2021-01483, Paper 11 at 18-19 (same with patent owner arguing trial date two months before FWD); Interim Procedures, 8.

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under 35 U.S.C. § 325(d)

No other proceedings involving the '673 Patent are currently pending or have been brought before the Patent Office. Additionally, the asserted prior art references (*Yin*, *Koshimizu*, and *Norström*) were not before the Examiner. Thus, the same or substantially the same prior art or arguments have not been previously presented to the Patent Office and denial of institution is not warranted under § 325(d).

VIII. MANDATORY NOTICES

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.

B. Related Matters

HID asserted the '673 Patent in *Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al.*, Case No. 2-24-cv-00140 (E.D. Tex).

The '673 Patent is not related to any known pending applications.

C. Lead and Backup Counsel, and Service Information

Lead Counsel	Backup Counsel
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Please address all correspondence to counsel at the addresses above.

Petitioner consents to electronic service by email at the above email addresses.

IX. GROUNDS FOR STANDING

Petitioner certifies that the '673 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

X. CONCLUSION

For the reasons set forth above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 20, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under § 42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 10,749.

Dated: September 20, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on September 20, 2024, a copy of the foregoing Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1017 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's Patent Center website for U.S. Patent No. 7,772,673:

Bever Hoffman & Harms, LLP
c/o Carrie Reddick, Office Manager
18486 Spring Valley Drive
Grass Valley, CA 95945

Date: September 20, 2024

By: /William Esper/
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Legal Assistant and PTAB Coordinator
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