

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG
ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01403
Patent 7,772,673 B2

Before WILLIAM V. SAINDON, GREGGI. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively “Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1–17 (“the challenged claims”) of U.S. Patent No. 7,772,673 B2 (“the ’673 patent,” Ex. 1001). Paper 1 (“Pet.”). Petitioner filed a Declaration of Dr. Scott E. Thompson, Ph.D., in support of the Petition. Ex. 1003. Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(a). *See* 37 C.F.R. § 42.4(a) (2023) (“The Board institutes the trial on behalf of the Director.”). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Considering the Petition, the Preliminary Response, and all supporting evidence, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in its challenge of at least one claim of the ’673 patent as unpatentable. Pursuant to 35 U.S.C. § 314, we hereby institute an *inter partes* review of all challenged claims of the ’673 patent on all grounds stated in the Petition.

Our factual findings, claim construction, if any, and legal conclusions at this stage of the proceeding are based on the evidentiary record developed thus far. This decision to institute trial is not a final decision as to the unpatentability of the claims for which *inter partes* review

is instituted. Our final decision will be based on the full record developed during trial.

A. Related Matters

The parties identify the following proceedings as related matters: *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) (“District Court Litigation”) and *Harbor Island Dynamic, LLC v. NXP Semiconductors N.V.*, No. 2:24-cv-00717-JRG-RSP (E.D. Tex.). Pet. 75; Paper 6 (Patent Owner’s Mandatory Notices), 2.

B. Real Parties in Interest

Petitioner identifies “Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.” as the real parties-in-interest. Pet. 75. Patent Owner identifies “Harbor Island Dynamic, LLC” as the real parties-in-interest. Paper 6, 2.

C. The ’673 patent (Ex. 100)

The ’673 patent is titled “Deep Trench Isolation and Method for Forming Same.” Ex. 1001, code (54). The ’673 patent relates “generally [to] the field of semiconductor fabrication,” and, “[m]ore particularly, . . . [to] the field of isolation region formation in semiconductor substrates.” *Id.* at 1:7–10. The invention’s background is described as “[d]eep trench isolation regions . . . formed to provide electrical isolation for electronic devices in a semiconductor die.”¹ *Id.* at 1:12–14. A described problem is

¹ Dr. Thompson explains that “a ‘semiconductor die’ is simply a wafer of semiconductor material such as silicon, and a ‘semiconductor package’ is the physical package in which an integrated circuit is stored,” and further, “[a] semiconductor die houses the transistors, such as bipolar junction transistor,

that, “for a rectangular-shaped trench, a thick layer of polysilicon can be required to adequately fill the trench with polysilicon” and “depositing a thick layer of polysilicon can significantly reduce polysilicon fill process throughput.” *Id.* at 1:32–36.

Figure 1 is reproduced below:

Fig. 1

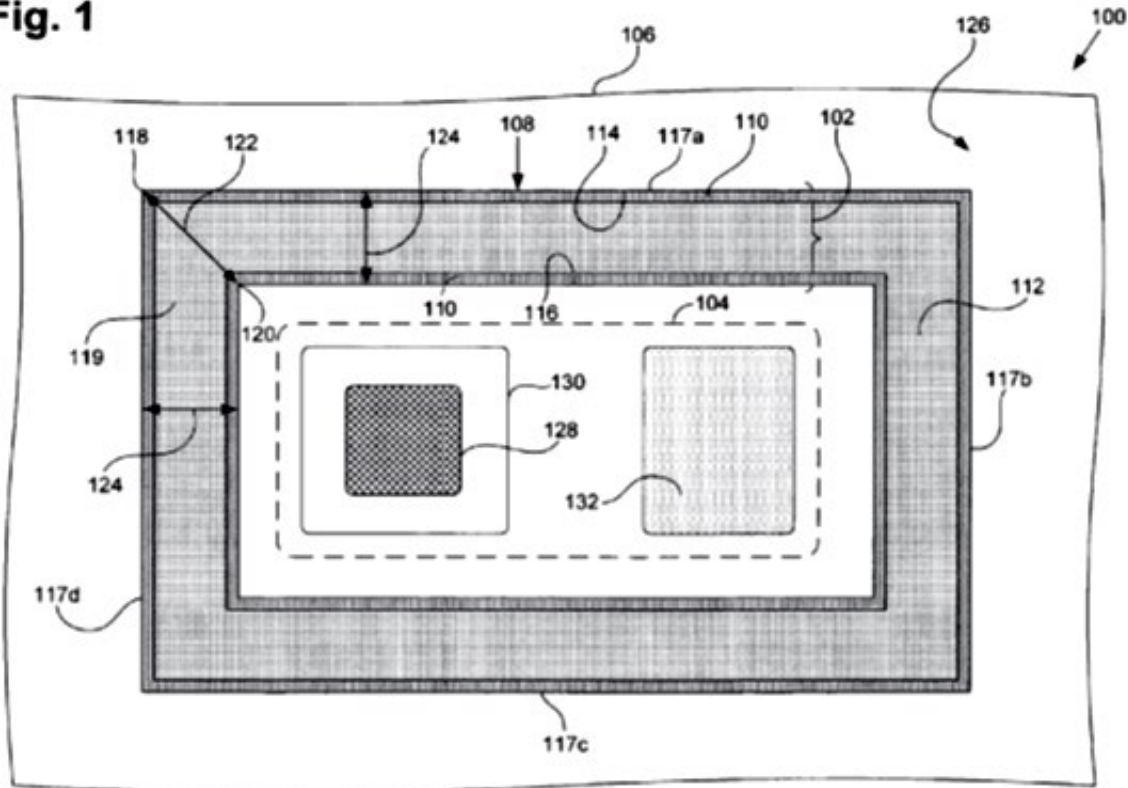


Figure 1 “shows a top view of an exemplary conventional deep trench isolation region in a semiconductor die.” Ex. 1001, 1:53–54. As shown, the semiconductor die 100 includes silicon substrate 106, bipolar device 104, and the conventional deep trench isolation region 102. Ex. 1001, 2:39–43. The deep trench isolation region 102 includes a rectangular trench 108, silicon oxide liner 110, and polysilicon filling 112. *Id.* at 2:43–45, 3:31. The

that make up the computer logic of the integrated circuit.” Ex. 1003 ¶ 47 (citing Ex. 1012, 1).

bipolar device 104 includes an active region 130, an emitter 128 situated over the active region 130, and a collector 132. *Id.* at 2:45–46. Field oxide regions overlay the deep trench isolation region 102 and separate the active region 130 from the collector 132. *Id.* at 2:47–49.

The rectangular trench 108 is situated in the substrate 106, has an outside wall 114 including corners 118, an inside wall 116 including corners 120, and sides 117a, 117b, 117c, and 117d. Ex. 1001, 3:6–12. A trench corner width 122 represents the perpendicular distance (i.e., the minimum distance) between the corners 118 of the outside wall 114 and corners 120 of the inside wall 116. *Id.* at 3:12–15. A trench side width 124 represents the perpendicular distance between the outside wall 114 and inside wall 116 along each of the sides 117. *Id.* at 3:15–18.

The silicon oxide liner 110 is situated on the outside walls 114, inside walls 116, and bottom surface (not shown) of the trench 108. Ex. 1001, 3:29–31. The polysilicon filling 112 is situated in trench 108 and formed by conformally depositing a layer of polysilicon (polycrystalline silicon) over top surface 126 of substrate 106. *Id.* at 3:34–37. By this configuration, the deep trench isolation region 102 encloses the bipolar device 104. *Id.* at 2:55–56. The enclosing isolates the bipolar device 104 from the substrate 106 and, in turn, from surrounding bipolar devices situated on the substrate 106. *Id.* at 2:66–3:2. The isolating of the collector 132 from the neighboring substrate also reduces collector-to-substrate capacitance. *Id.* at 3:2–5.

Figure 2 is reproduced below:

Fig. 2

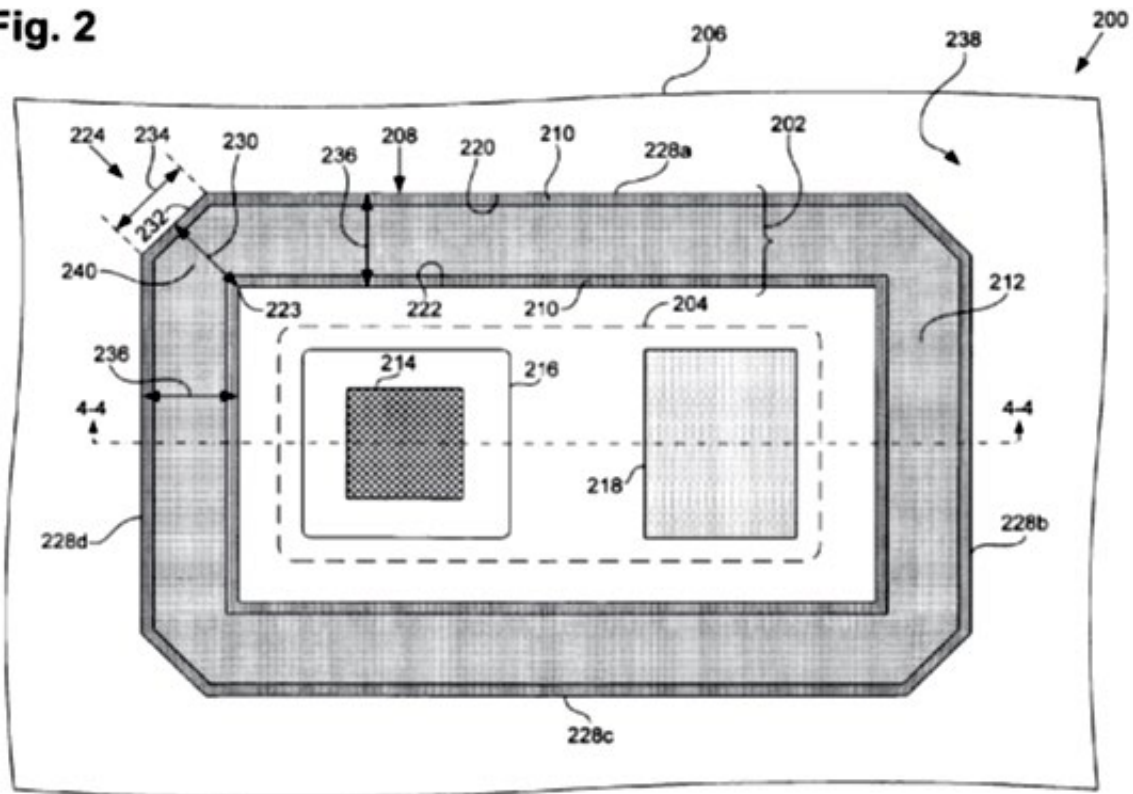


Figure 2 “shows a top view of an exemplary deep trench isolation region.” Ex. 1001, 1:55–56. Differing from the above-discussed rectangular trench 108, the embodiment’s trench 208 has an outside wall 220 including chamfered corners 224. *Id.* at 4:24–26. The length 234 of chamfered edge 232 is selected such that the trench corner width 230 is less than trench side width 236 (representing the perpendicular distance between the outside wall 220 and inside wall 222 along each of the sides 226 of the trench 208). *Id.* at 4:40–44. The chamfered edge 232 can have equal or unequal angles with the adjacent sides 228a, 228d of the trench 208. *Id.* at 4:48–52.

Relative to the rectangular trench 108 (Figure 1), the chamfered corners 240 of the embodiment's trench 208 (Figure 2) reduce the trench corner width 230 representing the perpendicular distance between the

chamfered edge 232 and each of the corners 223 of the inside wall 222 of the trench 208. Ex. 1001, 4:33–36. Though each of the trenches 108, 208 has a trench side width 124, 236 of 1.0 micron and a depth of 7.0 microns, the thicknesses of the deposited polysilicon layers for the rectangular trench 108 shown in Figure 1 and the Figure 2 embodiment's trench 208 are respectively 1.5 microns and 0.7 microns. *Id.* at 3:37–45; 5:4–26. Thus, relative to the embodiment's trench 208, manufacture of the rectangular trench 108 entails a greater polysilicon fill process throughput and accordingly increased cost. *Id.* at 3:41–50; 5:21–30.

Figure 4E of the '673 patent is reproduced below:

Fig. 4E

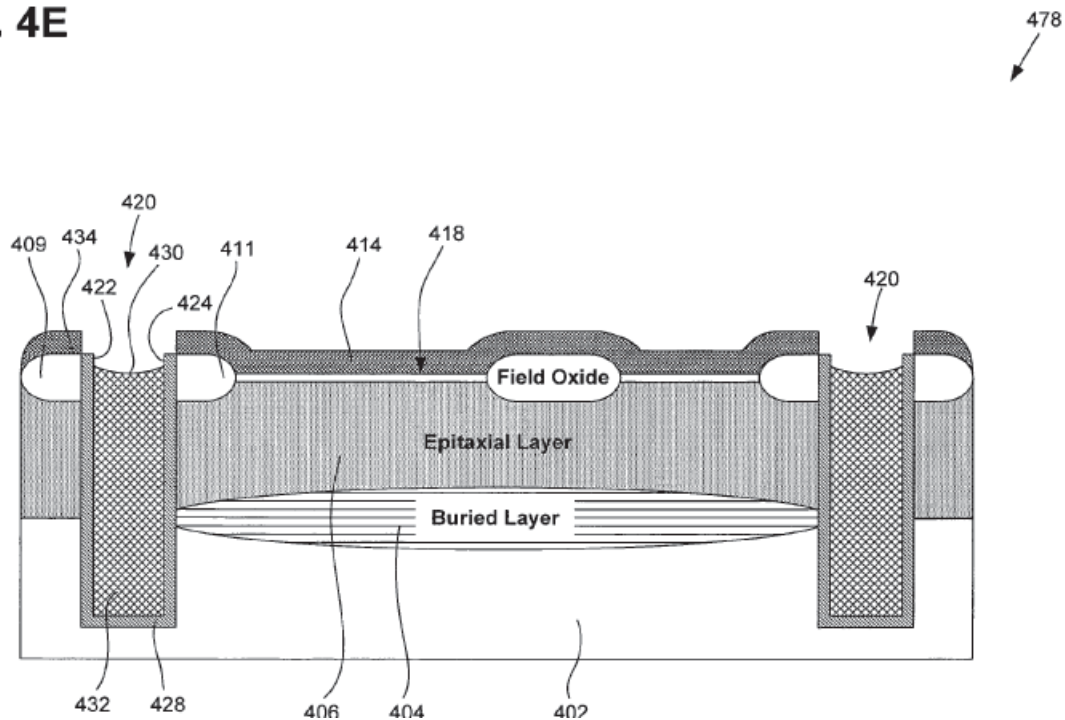


Figure 4E is “a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention.” Ex. 1001, 2:9–11. Figure 4E shows an oxide liner 428 formed on the “inside walls 422 and 424 and bottom surface 426 of trench 420. *Id.* at 7:59–61. Trench 420 is filled with polysilicon filling 432. *Id.* at 8:34–35.

D. Illustrative Claim

Claims 1 and 10 are independent claims. Claim 1 is reproduced, below, with Petitioner’s limitation identifiers in brackets (Pet. ii):

1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides; and

1[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Ex. 1001, 9:36–47.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–17 would have been unpatentable on the following grounds (Pet. 20–21):

Claim(s) Challenged	35 U.S.C. §²	References/Basis
1–17	103(a)	Yin, ³ Koshimizu ⁴
1, 3, 5, 7–8, 10, 12, 14–16	102	Norström ⁵

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103. Because the ’673 patent claims priority to an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of §§ 102, 103 applies.

³ U.S. Patent No. 6,995,449 to Yin et al. (Ex. 1004).

⁴ U.S. Patent Publication No. 2005/0181569 A1 to Koshimizu et al. (Ex. 1005).

⁵ U.S. Patent No. 6,121,102 to Norström et al. (Ex. 1006).

Claim(s) Challenged	35 U.S.C. § ²	References/Basis
7, 15	103(a)	Norström

II. ANALYSIS

A. Overview

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). At this stage of the proceeding, Petitioner bears the burden of demonstrating a reasonable likelihood that it would prevail with respect to at least one challenged claim for a petition to be granted. 35 U.S.C. § 314(a).

To establish anticipation under 35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting*

Tool Co., 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable as obvious “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).⁶ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained in *KSR International Co. v. Teleflex Inc.* that

Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning

⁶ No evidence of secondary considerations has been presented at this stage of the proceeding.

with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original)).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and *vice versa*.” Pet. 22–23 (citing Ex. 1003 ¶ 63). For purposes of the Preliminary Response, Patent Owner applies Petitioner’s level of ordinary skill in the art. Prelim. Resp. 7.

For the purposes of this Decision, we apply Petitioner’s proffered level of skill in the art because it appears consistent with the problems addressed in the ’673 patent and the prior art.

C. Claim Construction

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow

Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b) (2023). Accordingly, we construe each challenged claim of the '673 patent to generally be “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

If the specification “reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is “when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Uship Intellectual Props., LLC v. United States*, 714 F.3d 1311, 1313 (Fed. Cir. 2013) (quoting *Thorn v. Sony Comput. Ent. Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Neither Petitioner nor Patent Owner proposes any claim construction. Pet. 19; Prelim. Resp. 8. Based on our review of the record, we determine that no express construction of any claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

The parties are free to address the construction of any claim term in an authorize brief during trial. If either party chooses to do so, claim

construction arguments should be set forth in a separate delineated portion of the brief labelled accordingly.

*D. Ground 1: Alleged Obviousness of Claims 1–17
over Yin and Koshimizu*

Petitioner contends claims 1–17 would have been obvious over Yin in view of Koshimizu. Pet. 23–57. Petitioner supports its contentions with Dr. Thompson’s Declaration. Ex. 1003.

We begin with a brief summary of Yin and Koshimizu. We then address the parties’ contentions.

1. Yin (Ex. 1004)

Yin⁷ is titled “Deep Trench Isolation Region with Reduced-Size Cavities in Overlying Field Oxide.” Ex. 1004, code (54). Yin “relates to the field of fabrication of semiconductor devices” and, “[m]ore specifically, . . . to forming isolation regions in semiconductor substrates.” *Id.* at 1:11–14.

Yin describes a “typical conventional deep trench isolation process.” Ex. 1004, 1:28. Principally, a layer of silicon nitride is deposited on a silicon substrate. *Id.* at 1:29–30. A hard mask of dense oxide is then formed over the nitride layer. *Id.* at 1:31–34. A photoresist mask is patterned over the hard mask. *Id.* at 1:35–36. The trench is accordingly etched into the silicon substrate. *Id.* at 1:36–39. A dense oxide liner is formed on the sidewalls of the trench and on the surface of the silicon substrate. *Id.* at 1:43–45. A conformal layer of polysilicon is deposited over the silicon substrate and trench. *Id.* at 1:48–50. The hard mask is removed by a wet

⁷ The two named co-inventors on Yin are also two of the co-inventors named on the ’673 patent. Ex. 1001, code (75); Ex. 1004, code (75).

etch, which causes unwanted lateral etching of the dense oxide layer.

Id. at 1:53–59.

The invention provides “an effective method for removing a hard mask in a deep trench isolation process.” Ex. 1001, 2:18–20. The hard mask is removed by dry etching the hard mask. *Id.* at 2:35–37. An oxide liner is then deposited on the sidewalls of the trench and over the substrate. *Id.* at 2:39–41. The oxide liner is removed by a wet strip process. *Id.* at 2:42–43.

Figure 2G is reproduced below:

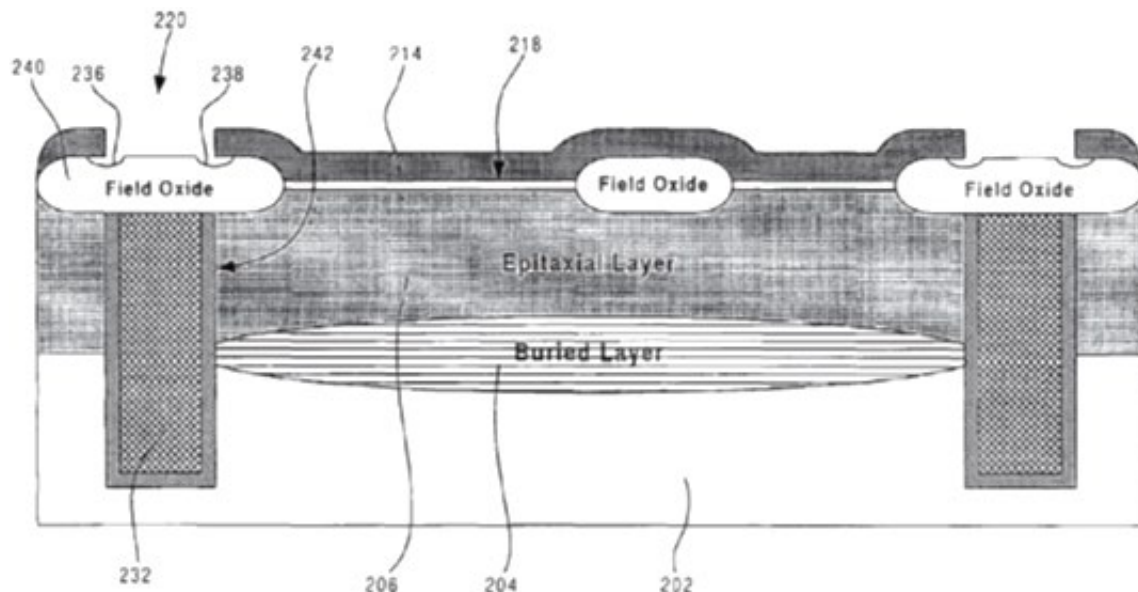


Figure 2G is cross-sectional view of a wafer processed according to an embodiment of the invention. Ex. 1001, 3:13–16. In Figure 2G, “the layer of polysilicon is etched back to depth 230 inside trench 220 to form polysilicon portion 232.” *Id.* at 6:43–44.

2. *Koshimizu (Ex. 1005)*

Koshimizu is titled “Semiconductor Device and Manufacturing Method Thereof.” Ex. 1005, code (54). Koshimizu “relates to a semiconductor device and a manufacturing technique therefor and

particularly to a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor . . . ‘HBT.’” *Id.* ¶ 1.

Koshimizu describes prior techniques for forming an HBT. Ex. 1005 ¶ 2. A described problem is that wet etching of an opening through a silicon oxide film stacked on silicon nitride film etches the silicon nitride faster than the silicon oxide and thereby causes a sidewall-protrusion of the silicon oxide into the opening. *Id.* ¶¶ 3–4. An unwanted consequence is that the protrusion interferes with subsequent epitaxial growth of insulator in the opening. *Id.* ¶ 4.

Figure 2 is reproduced below:

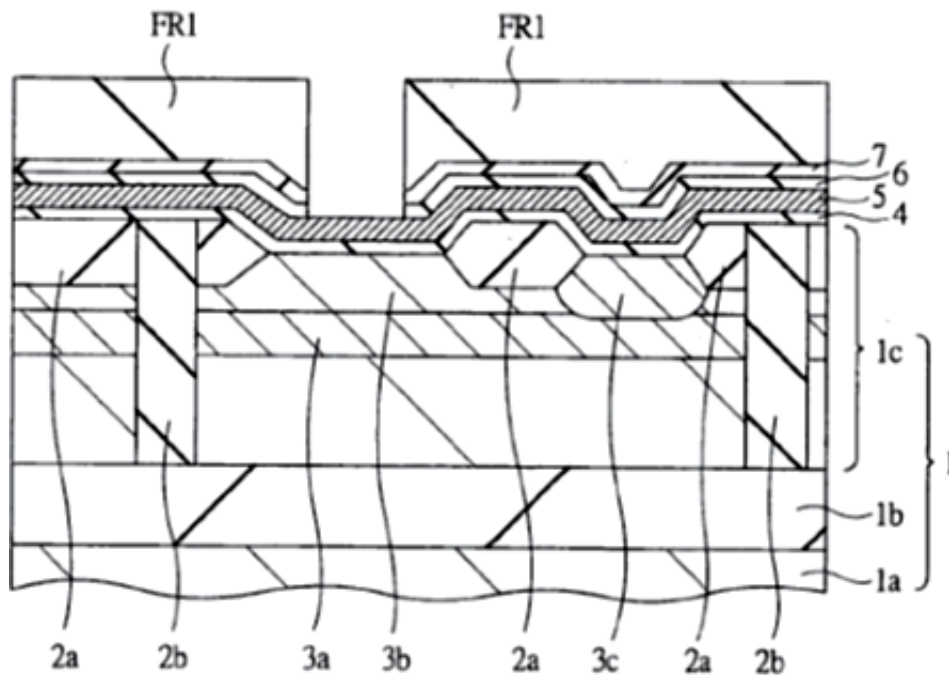


Figure 2 “is a sectional view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶ 14. To create the structure shown, a silicon oxide film 4, silicon film 5, a silicon nitride film 6, and a silicon oxide film 7 stacked onto (in this order) a substrate 1. *Id.* ¶ 53. Using photoresist FR1 patterned on the silicon oxide

film 7, an accordant opening is etched down to the upper surface of the silicon film 5. *Id.* The remaining illustrated structures 1–3 include a substrate region 1 having a silicon layer 1c, silicon oxide layer 1b, and semiconductor layer 1a; an isolation region 2 having a shallow isolation silicon oxide film 2a and deep trench isolation silicon oxide film 2b; and an HBT region 3 having an n⁺-type collector embedding region 3a, n⁺-type collector region 3b, and n⁺-type collector extraction region 3c. *Id.*

Figure 16 is reproduced below:

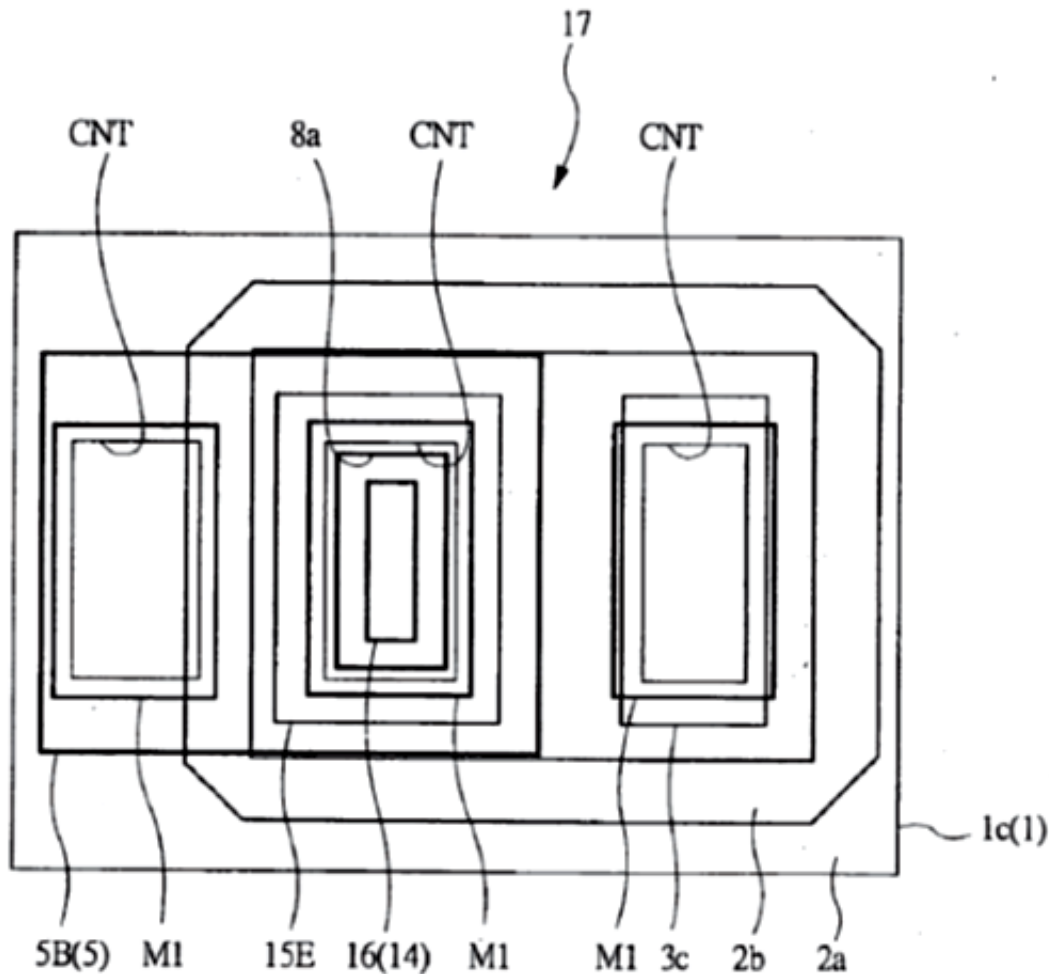


Figure 16 “is a plan view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶ 28. Contact holes (not labeled) expose a base extraction electrode 5B, emitter extraction electrode

15E, and the collector extraction region 3c of an and HBT 17. *Id.* ¶¶ 59, 61. The remaining illustrated structures include conductor polycrystalline silicon film 5 (*id.* ¶ 53), wirings M1 (*id.* ¶ 60), emitter region 16 (*id.* ¶ 59), and opening portion 8a (*id.* ¶ 54).

3. Claim 1

Petitioner provides a limitation-by-limitation analysis of claim 1, mapping each claim limitation to the combination of Yin and Koshimizu. Pet. 28–57. Petitioner also contends that a person of ordinary skill in the art would have been motivated to combine the references, with a reasonable expectation of success. *Id.* at 23–27. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003 ¶¶ 148–159.

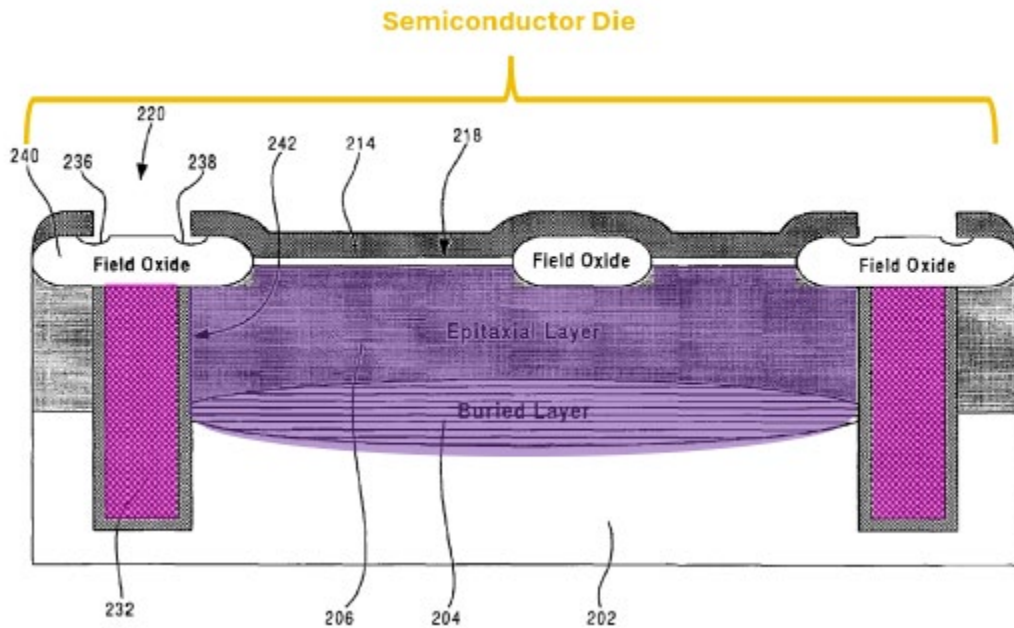
Patent Owner argues this challenge is deficient because Koshimizu is not analogous art to the '673 patent. Prelim. Resp. 11–15.

We start by analyzing Petitioner's contentions for the claim limitations.⁸ We then address Petitioner's motivation to combine, reasonable expectation of success and Patent Owner's argument that Koshimizu is not analogous art.

a) *1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:*

Petitioner contends that “[t]o the extent the preamble is limiting, *Yin* discloses a semiconductor die including at least one deep trench isolation region for isolating an electronic device.” Pet. 28 (citing Ex. 1003 ¶ 91). Petitioner provides the following annotated version of Yin's Figure 2G:

⁸ For ease of reference, we utilize Petitioner's limitation identifiers.



Pet. 28. Figure 2G is a cross-sectional view of “portions of a wafer processed according to an embodiment.” Ex. 1004 3:13–14. Petitioner annotates Figure 2G by highlighting trench 220 in magenta and adding an orange horizontal line on top of Figure 2G with orange text “Semiconductor Die.” Pet. 28.

Petitioner contends that “trench 220 represents a deep isolation trench filled with polysilicon 232.” Pet. 28 (citing Ex. 1004, 6:29–53). Petitioner further contends that Yin’s description of Figure 2G as “the cross-section of a wafer” corresponds to the ’673 patent’s “semiconductor die.” *Id.* at 28–29 (citing Ex. 1001, 5:52–57; Ex. 1003 ¶ 91; Ex. 1004, 3:13–16). Petitioner also contends that Yin’s trench 220 “may electrically isolate, for example, a bipolar transistor,” Figure 2G shows “the bipolar transistor . . . to be surrounded by the deep isolation trench,” and “the semiconductor die hous[es] the bipolar transistor and deep isolation trench region.” *Id.* at 29 (citing Ex. 1003 ¶ 92; Ex. 1004, 1:16–27, Fig. 2G).

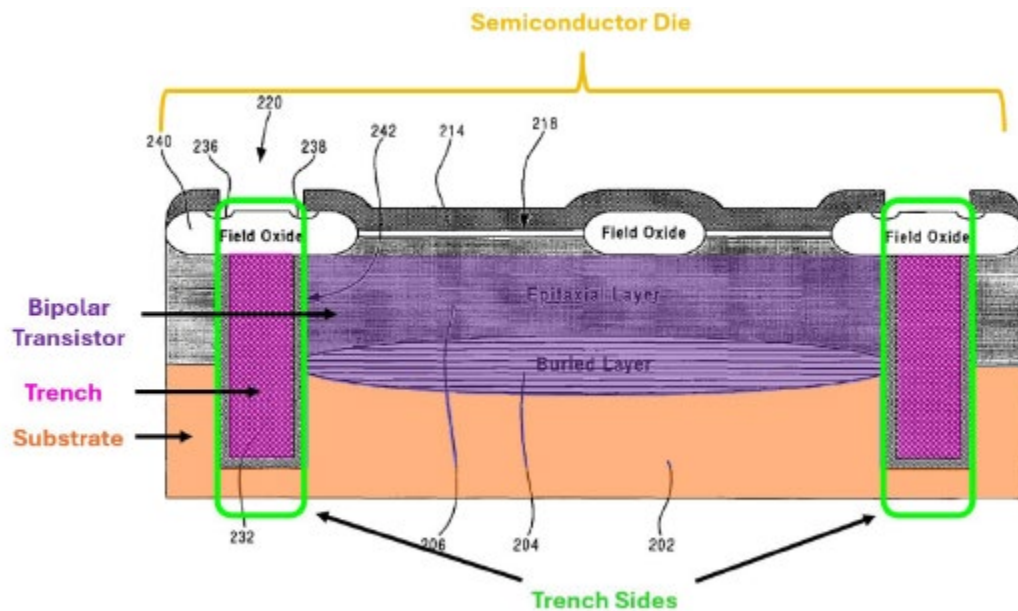
Patent Owner does not address the preamble of claim 1 in the Preliminary Response. *See* Prelim. Resp. 11–15.

We have reviewed Petitioner’s contentions and evidence and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Yin teaches the subject matter of the preamble. Consequently, we need not address whether the preamble of claim 1 is limiting.

- b) 1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;*

Petitioner contends that the combination of Yin and Koshimizu teaches limitation 1[a]. Pet. 30–35.

Petitioner first contends that Yin discloses an electronic device, i.e., a bipolar transistor surrounded by deep isolation trench 220 and situated in a substrate. Pet. 30 (citing Ex. 1003 ¶ 94; Ex. 1004 1:19–27, Fig. 2G). Petitioner argues that Yin’s Figure 2G “represents a bipolar transistor isolated by a deep isolation trench consistent with” Figures 2 and 4E of the ’673 patent. *Id.* at 30–31 (comparing Ex. 1001, Figs. 2, 4E and Ex. 1004 Fig. 2G). In support of this argument, Petitioner provides the following annotated version of Figure 2G of Yin:

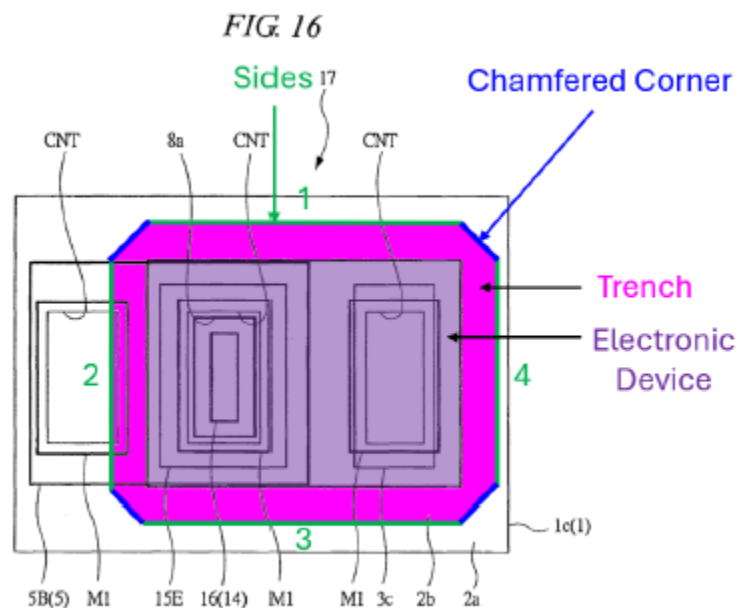


Pet. 32. Figure 2G is a cross-sectional view of “portions of a wafer processed according to an embodiment.” Ex. 1004 3:13–14. Petitioner annotates Figure 2G by highlighting trench 220 in magenta and adding magenta text, “Trench” with a black arrow pointing to the trench, highlighting elements 204 and 206 in purple and adding purple text, “Bipolar Transistor” with a black arrow pointing to elements 204 and 206, highlighting element 202 in orange and adding orange text, “Substrate” with a black arrow pointing to element 202, adding green rectangles around trench 220 and green text, “Trench Sides” with black arrows pointing to the trench, and adding an orange horizontal line on top of Figure 2G with orange text “Semiconductor Die.” Pet. 32.

Petitioner acknowledges that Yin does not provide a top-down view of its bipolar transistor but contends that “it would have been readily understood by a [person of ordinary skill in the art] to be surrounded by a four-sided trench.” Pet. 32 (citing Ex. 1003 ¶ 95); *see also id.* at 32–33 (arguing that the two portrayed trenches in Yin’s Figure 2G “correspond to

two opposite sides of the rectangular die's four sides.” (citing Ex. 1003 ¶96) (citing Ex. 1007, 476)).

Next, Petitioner reproduces an annotated version of Koshimizu's Figure 16:



Pet. 35. Figure 16 “is a plan view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶28.

Petitioner annotates Figure 16 by shading Koshimizu's trench magenta and adding magenta text, “Trench” with a black arrow, shading electronic device purple and adding purple text “Electronic device” with a black arrow, adding 4 green lines around the Electronic device and adding green text “Side” with green arrows, and adding blue lines to the corners with blue text “Chamfered Corner.” Pet. 35.

Petitioner contends that Koshimizu's “chamfered corners connect the four sides of the deep trench 2b in *Koshimizu*” and “[w]hen integrated into *Yin*'s semiconductor die, these chamfered corners would have likewise

connected the four sides of *Yin*'s deep trench isolation region in the same manner." Pet. 35 (citing Ex. 1003 ¶ 99).

Patent Owner does not address limitation [1a] in the Preliminary Response. *See* Prelim. Resp. 11–15.

We have reviewed Petitioner's contentions and evidence in light of Patent Owner's arguments and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that the combination of *Yin* and *Koshimizu* teaches this limitation.

- c) 1[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.*

Petitioner contends that the combination of *Yin* and *Koshimizu* teaches this limitation. Pet. 36–44.

Petitioner first contends that *Yin*'s "deep isolation trenches are filled with polysilicon." Pet. 36 (citing Ex. 1003 ¶ 102; Ex. 1004, 6:29–32, 6:43–44, Fig. 2F). Petitioner next contends that "*Koshimizu*'s chamfered corners considerably reduce the width of the trench at the corners where they would otherwise be the widest if left unchamfered." *Id.* at 37 (citing Ex. 1001, Fig. 1; Ex. 1003 ¶ 102; Ex. 1005, Fig. 16). According to Petitioner, an ordinarily skilled artisan "would have understood that the thickness of a layer of polysilicon within a trench at a given location will be reduced if the width of the trench at that location is likewise reduced." *Id.* (citing Ex. 1003 ¶ 103); *see also id.* at 43–44 ("*Koshimizu*'s chamfered corners reduce the width of the widest portion of the trench and cause a reduction in the thickness of the polysilicon filling them in at least the corner portions." (citing Ex. 1003 ¶ 105)).

Patent Owner does not address limitation [1b] in the Preliminary Response. *See* Prelim. Resp. 11–15.

We have reviewed Petitioner’s contentions and evidence in light of Patent Owner’s arguments and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes the combination of Yin and Koshimizu teaches this limitation.

d) Motivation to Combine and Reasonable Expectation of Success

Petitioner contends that both Yin and Koshimizu are analogous art to the ’673 patent. Pet. 8, 11. Petitioner supports this contention with the declaration testimony of Dr. Thompson. Ex. 1003 ¶¶ 70, 74.

Petitioner contends that Yin’s teachings would lead a POSITA to Koshimizu’s teachings because:

Yin does not disclose the geometry of the corners of its deep trench isolation region. *See* Thomson Dec. ¶ 82. Thus, a skilled artisan looking to use Yin’s semiconductor die would have looked to other disclosures for a suitable corner geometry. Koshimizu provides that geometry, specifically teaching trenches with an unchamfered inner corner and a chamfered outer corner. *See Koshimizu*, Fig. 16, [0028]; *see also id.*, [0051]–[0061] (fully disclosing the manufacturing method and features of the same).

Pet. 23–24. Petitioner further contends that “[c]hamfered corners were beneficial not only because they improved structural stability . . . but also because they could reduce the need for overfilling” and that “Koshimizu is just one of many examples of a deep isolation trench with chamfered corners; these were a common feature of deep isolation trenches before the ’673 Patent.” *Id.* at 24 (citing Ex. 1003, ¶ 82–84 (citing Ex. 1006, Figs. 13, 25; Ex. 1008, Figs. 1, 4; Ex. 1009, 573–74)).

Petitioner argues that an ordinarily skilled artisan “would have been motivated to avoid the overfilling of trench sides in *Yin*’s deep isolation trench that would result from using unchamfered corners by instead using chamfered corners.” Pet. 25 (citing Ex. 1003 ¶ 85). According to Petitioner combining Koshimizu and Yin “is nothing more than using a known method (chamfering a deep isolation trench) that yields a known result (e.g., a reduction in necessary isolating material in said trench).” *Id.* (citing Ex. 1003 ¶ 85).

Petitioner next contends that an ordinarily skilled artisan would have had a reasonable expectation of success because “[c]hamfering the outer corners of *Yin*’s trench would have required nothing more than an adjustment to the mask pattern that defines the outline of the trench to have chamfered corners instead of square corners.” Pet. 26 (citing Ex. 1003 ¶ 89). Petitioner further contends that “[i]t was also known in the art that 135° angle corners (i.e., chamfered), rather than 90° angle corners (i.e., unchamfered) were one solution to improve problems associated with trench refill.” *Id.* at 26–27 (citing Ex. 1003 ¶ 89).

Patent Owner does not directly address Petitioner’s motivation to combine and reasonable expectation of success arguments. Prelim. Resp. 11–15.

We have reviewed Petitioner’s contentions and evidence and find, based on the present record at this stage of the proceeding, that Petitioner sufficiently establishes that an ordinarily skilled artisan would have had a motivation to combine Yin and Koshimizu with a reasonable expectation of success.

Patent Owner’s only contention for this challenge is that Koshimizu is not analogous art to the ’673 patent. Prelim. Resp. 11. According to Patent Owner, “the ’673 Patent is directed to reducing the thickness of a polysilicon layer while Koshimizu is related to a method for manufacturing transistors.” *Id.*

Patent Owner contends that the ’673 patent and Koshimizu are not in the same field of endeavor and Koshimizu is not reasonably pertinent to the problem with which the inventor of the ’673 patent is involved. Prelim. Resp. 11, 15. In support, Patent Owner argues that “the ’673 Patent is ‘directed to deep trench isolation and method for forming same.’” *Id.* (citing Ex. 1001, 2:20–21). Patent Owner further argues that the ’673 patent “sought to solve problems that arise with the use of polysilicon. Specifically, filling prior art rectangular-shaped trenches required a thick layer of polysilicon to ensure the trench was adequately filled.” *Id.* at 12 (citing Ex. 1001, 1:32–34). Patent Owner argues for a narrow scope of the field of invention: “methods of filling deep isolation trenches with polysilicon.” *Id.*

Patent Owner next contends that “Petitioner’s description of the field of endeavor (‘manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors’) is far too broad.” Prelim. Resp. 13.

Patent Owner next contends that Koshimizu “is directed to a method of manufacturing hetero-junction bipolar transistor . . . devices that improve the reliability of such devices.” Prelim. Resp. 12 (citing Ex. 1005 ¶¶ 1, 5). Patent Owner concedes that “Koshimizu discusses the use of a deep isolation trench” and “shows chamfered corners of the . . . trench” but argues its

trench is filled with silicon oxide not polysilicon and “is silent on the purpose of [the chamfered corners], and whether they reduce the thickness of the fill material.” *Id.* at 12–13 (citing Ex. 1005 ¶ 52, Fig. 16). Patent Owner then argues that “Koshimizu’s field of endeavor is thus manufacturing transistors” and “[f]or similar reasons, Koshimizu is not ‘reasonably pertinent to the particular problem with which the inventor is involved.’” *Id.* at 13, 15.

For the following reasons, Patent Owner’s contention is unavailing based on the present record at this stage of the proceeding.

For a prior-art reference to qualify as analogous art, the reference must either be in the field of the applicant's endeavor or reasonably pertinent to the problem with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1447 (Fed. Cir. 1992). References are selected as being reasonably pertinent to the problem based on the judgment of a person having ordinary skill in the art. *Id.* (“[I]t is necessary to consider ‘the reality of the circumstances,’ — in other words, common sense—in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor.” (quoting *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979))). Further, in *Wyers v. Master Lock Co.*, 616 F.3d 1231 (Fed. Cir. 2010), the Federal Circuit directed that the scope of analogous art is to be construed broadly. *Id.* at 1238 (citing *KSR Intern’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 402 (2007)).

The ’673 patent describes “a semiconductor die including at least one deep trench isolation region for isolating an electronic device (for example, a bipolar device) includes a trench situated in a substrate of the semiconductor die.” Ex. 1001, code (57); *see also id.* at 1:7–8 (“The present invention is

generally in the field of semiconductor fabrication.”). Koshimizu discloses the “invention relates to a semiconductor device and a manufacturing technique therfor[e] and particularly to a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor . . . and to a manufacturing method for the semiconductor device.” Ex. 1005 ¶ 1.

Koshimizu’s device includes “deep trench isolation.” *Id.* ¶ 52. We preliminarily find that both the ’673 patent and Koshimizu relate to semiconductor devices (and methods of manufacturing semiconductor devices) with a deep trench for isolating a bipolar device. Consequently, we preliminarily find that the ’673 patent and Koshimizu are directed to the same field of endeavor.

Based on the present record at this stage of the proceeding, we preliminarily determine that Patent Owner’s attorney argument does not undercut Petitioner’s showing that “*Koshimizu* is analogous art to the ’673 Patent.” Pet. 11 (citing Ex. 1003 ¶ 74).

e) Summary of Claim 1

For the foregoing reasons, we determine that Petitioner establishes a reasonable likelihood of showing that claim 1 is obvious over the combination of Yin and Koshimizu.

4. Claims 2–17

Petitioner cites additional disclosures in Yin and Koshimizu corresponding to the additional limitations in these claims. Pet. 44–57. Patent Owner does not address these claims separately from the arguments raised regarding independent claim 1. *See* Prelim. Resp. We reviewed the evidence cited by Petitioner and find it sufficient for the reasons provided by Petitioner.

*E. Ground 2: Alleged Anticipation of
Claims 1, 3, 5, 7, 8, 10, 12, and 14–16 by Norström*

Petitioner contends that claims 1, 3, 5, 7, 8, 10, 12, and 14–16 are anticipated by Norström. Pet. 58–71. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003.

Patent Owner argues that this challenge fails because the Petition fails to identify structure in Norstrom corresponding to the “trench” as recited in limitations 1[a] and 1[b]. Prelim. Resp. 16–20.

We begin with a brief summary of Norström. We then address the parties’ contentions.

1. Norström (Ex. 1006)

Norström is titled “Method of Electrical Connection Through an Isolation Trench to Form Trench-Isolated Bipolar Devices.” Ex. 1006, code (54). Norström “relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” *Id.* at 1:7–10.

Figure 13a is reproduced below:

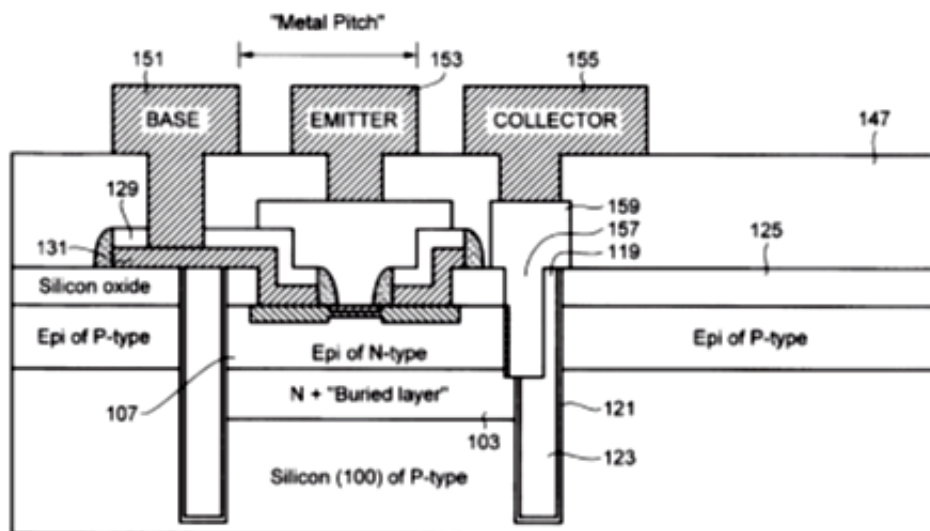


Figure 13a “is a schematic cross sectional view . . . of [a] finished NPN-transistor.” Ex. 1006, 6:24–26. Silicon oxide layer 147 is etched to form contact holes therethrough and then receive, therein, metal that forms a base plug 151, emitter plug 153, and collector plug 155. Ex. 1006, 10:66–11:6. The remaining illustrated structures include N- and P-regions 107, trenches filled 119 with isolating material 123 and having sidewalls overlaid with oxide layers 121, a buried N+ layer 103, and oxidation outer confining regions 125. *Id.* at 7:19–48.

FIG. 13c is reproduced below:

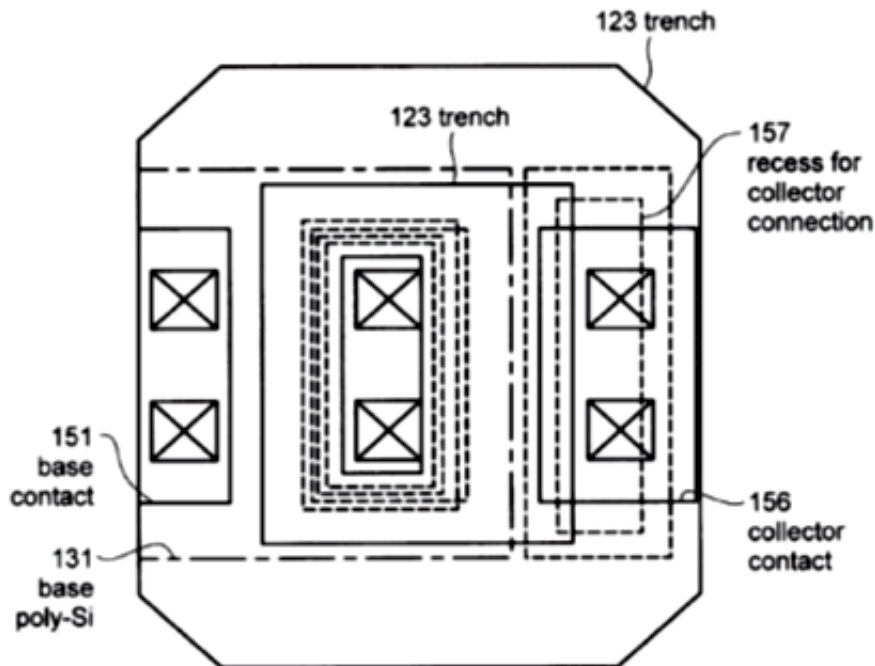
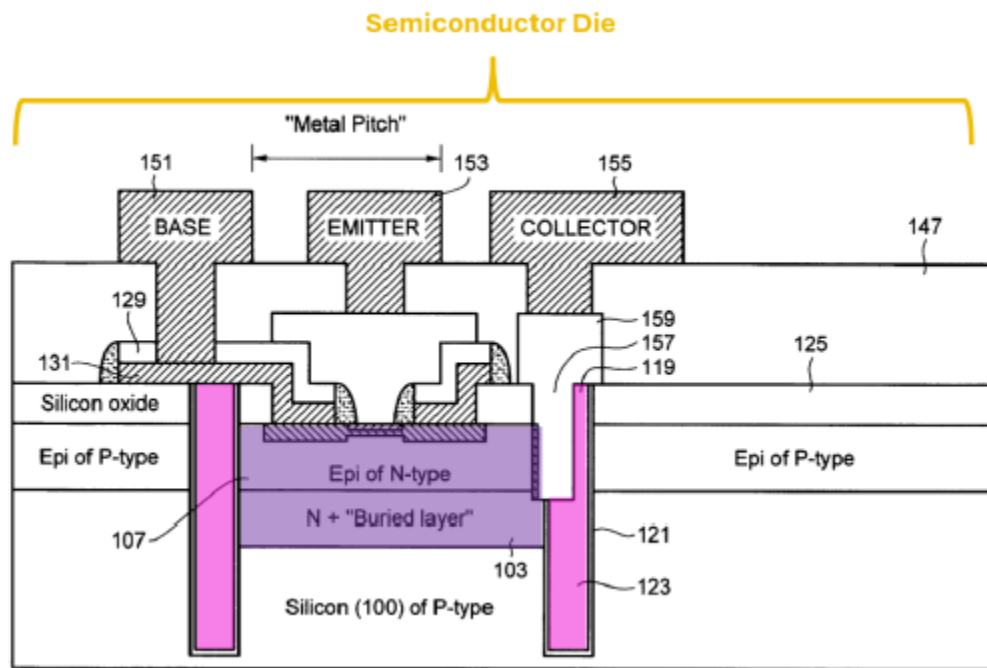


Figure 13c “is a view from above [that] schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.” Ex. 1006, 6:32–34.

2. Claim 1

- a) 1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising

Petitioner provides the following annotated version of Norström's Figure 13a:



Pet. 59. Figure 13a “is a schematic cross-sectional view . . . of the finished NPN-transistor.” Ex. 1006, 6:24–26. Petitioner annotates this figure by shading in purple the bipolar transistor, shading in magenta deep trench isolation region, and adding an orange horizontal line on top with text reading “Semiconductor Die.” Pet. 59.

Petitioner contends that “Norström discloses that its ‘present invention relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” Pet. 58 (citing Ex. 1003 ¶ 149; Ex. 1006, 1:7–10).

Patent Owner does not address the preamble of claim 1 in the Preliminary Response. *See* Prelim. Resp. 16–20.

We have reviewed Petitioner’s contentions and evidence and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Norström teaches the subject matter of the preamble. Consequently, we need not address whether the preamble of claim 1 is limiting.

- b) *1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;*

Petitioner provides the following annotated version of Norström’s Figure 13c:

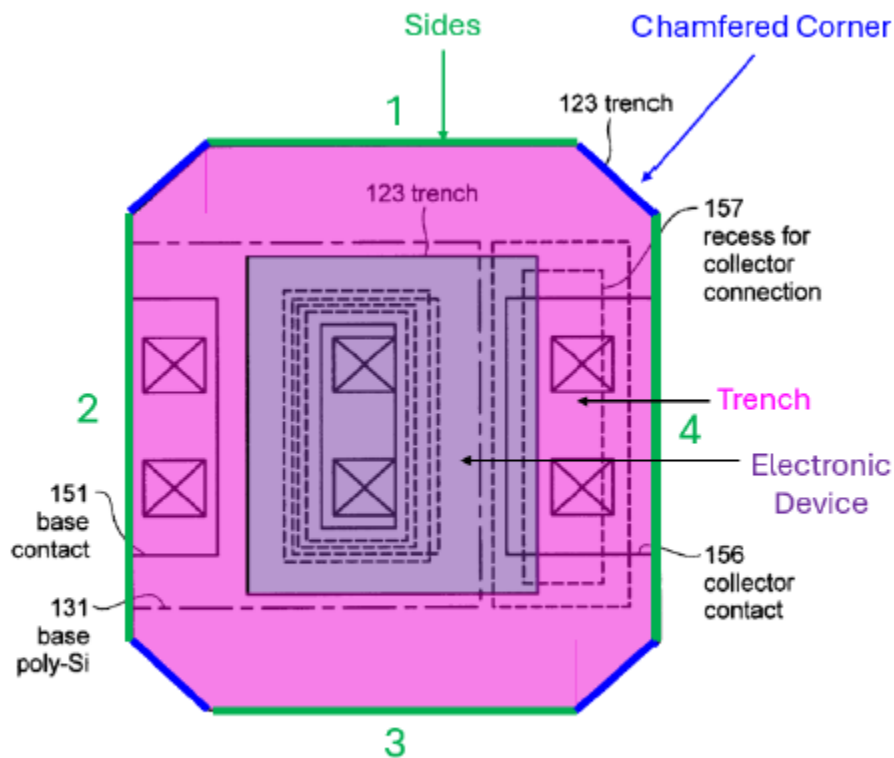


FIG. 13c

Pet. 61. Figure 13c “is a view from above, which schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.” Ex. 1006, 6:32-34. Petitioner annotates Figure 13c by shading Norström’s trench magenta and adding magenta text, “Trench” with a black arrow, shading electronic device purple and adding purple text “Electronic device with a black arrow, adding 4 green lines around the Electronic device and adding green text “Side” with green arrows, and adding blue lines to the corners with blue text “Chamfered Corner.” Pet. 61.

Petitioner contends that “Norström’s trench 123 surrounds the bipolar NPN transistor, within, which is an electronic device.” Pet. 61 (citing Ex. 1003 ¶ 152; Ex. 1006, Figs. 13a, 13c). Petitioner further contends that “Figure 13c also depicts the four trench chamfered corners at the outer edge of trench 123 connecting the four sides of the trench” and that Figure 13c shows that trench 123 “ha[s] no right angles but the flat sidewall segments form an angle of 135° to each other.” *Id.* at 61–62 (citing Ex. 1003 ¶¶ 152–153; Ex. 1006, 16:39–42, Fig. 13c). Petitioner also argues that Figure 13a shows that both the trench and NPS bipolar transistor “are situated in a substrate of silicon within the semiconductor die.” *Id.* at 62 (citing Ex. 1003 ¶ 154; Ex. 1006, 9:31–55, Fig. 13a).

Patent Owner does not address limitation 1[a] of claim 1 in the Preliminary Response. *See* Prelim. Resp. 16–20.

- c) *1[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.*

Petitioner contends that “Norström discloses that its isolation trenches may be filled with polysilicon.” Pet. 63 (citing Ex. 1003 ¶ 157; Ex. 1006, 7:47–50). Relying on its reasoning from Ground 1, Petitioner further

contends that an ordinarily skilled artisan “would have understood that by chamfering the outer corners of a deep isolation trench, the thickness of the polysilicon layer within the trench would be reduced at the narrower chamfered corner.” *Id.* (citing Ex. 1003 ¶ 158). Petitioner further contends that “Norström specifically discloses that chamfered outer trench corners improve the refill process over non-chamfered corners” similar to the ’673 patent. *Id.* at 63–64 (citing Ex. 1001, 9:6–10; Ex. 1003 ¶ 158; Ex. 1006, 16:28–36).

Patent Owner’s Trench Contentions

Patent Owner contends that “the Petition identifies two **different trenches**; one that it argues is in the substrate and one that it argues has the chamfered corner” but “does not show—indeed cannot show—that the trenches are the same.” Prelim. Resp. 16. According to Patent Owner, the Petition identifies two trenches in Figure 13a of Norström. *Id.* at 16–17 (reproducing showing Petitioner’s annotated version of Norström’s Figure 13a from page 62 of the Petition). Next, according to Patent Owner, the trench identified as numeral 123 in Figure 13c “**cannot be** the trenches 119 identified by Petitioner.” *Id.* at 19. We find this argument unavailing for the following reasons.

Norström’s Figures 13a and 13c are different views of the same embodiment. Ex. 1006, 6:24–27, 6:32–34. Petitioner’s contentions are supported by Dr. Thompson who explains that an ordinary skilled artisan would have readily understood that cut away views such as in Yin (and Norström’s Figure 13a) represent a bipolar transistor “surrounded by a four-sided trench.” Ex. 1003 ¶ 95; *see also id.* ¶ 152 (Dr. Thompson testifying that Norström discloses a four-sided trench with chamfered corners.). Patent

Owner’s contention, however, is attorney argument unsupported by testimony concerning how a person of ordinary skill in the art would understand Norström’s drawings. We note that Norström discloses that “isolating trenches 119 [shown in Figure 13a] . . . are filled with an isolating or semi-isolating material 123 [shown in both Figures 13a and 13c].” Based on this disclosure and our review of Figures 13a and 13c, it appears that Norström uses the numerals 119 and 123 interchangeably. For the foregoing reasons, based on the present record at this stage of the proceedings, Patent Owner’s argument does not undercut Petitioner’s trench contentions which are sufficiently supported by Dr. Thompson’s testimony and the disclosure of Norström.

We have reviewed Petitioner’s contentions and evidence and find that, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Norström discloses limitations 1[a] and 1[b].

Summary of Claim 1

For the foregoing reasons, we determine that Petitioner establishes a reasonable likelihood of showing that claim 1 is anticipated by Norström.

3. Claims 3, 5, 7, 8, 10, 12, and 14–16

Petitioner cites additional disclosures in Norström corresponding to the additional limitations in these claims. Pet. 65–71. Patent Owner does not address these claims separately from the arguments raised regarding independent claim 1. *See* Prelim. Resp. We reviewed the evidence cited by Petitioner and find it sufficient for the reasons provided by Petitioner.

*F. Ground 3: Alleged Obviousness of
Claims 7 and 15 by Norström*

Petitioner cites additional disclosures in Norström corresponding to the additional limitations in these claims. Pet. 71–73. Patent Owner does not address these claims separately from the arguments raised regarding Ground 1. *See* Prelim. Resp. 20–21. We reviewed the evidence cited by Petitioner and find it sufficient for the reasons provided by Petitioner.

III. DISCRETIONARY DENIAL

Patent Owner argues that, because of co-pending district court litigation between Patent Owner and Petitioner, we should exercise our discretion to deny institution under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). Pet. 21–27.

We consider the advanced state of a parallel district court action as a factor that may weigh in favor of denying a petition under § 314(a). *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential). The following factors inform our assessment of “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding”:

- 1) whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
- 2) proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
- 3) investment in the parallel proceeding by the court and the parties;
- 4) overlap of issues raised in the petition and in the parallel proceeding;

- 5) whether the petitioner and the defendant in the parallel proceeding are the same party; and
- 6) other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, IPR2020-00019, Paper 11 at 5–6.

1. Fintiv Factor 1

Patent Owner contends this factor supports exercising our discretion to deny institution because “[t]here is no stay of the parallel District Court Litigation and, in fact a motion for a stay by Petitioner has already been denied.” Prelim. Resp. 26 (citing Ex. 2002, 1). Petitioner argues that this factor is “at worst neutral.” Pet. 74.

Petitioner’s motion for a stay of the District Court Litigation was denied as premature because “the Patent Trial and Appeal Board has not yet acted on a petition for *inter partes* review.” Ex. 2002, 1.

Although no stay of the District Court Litigation has been issued, it appears that the district court would entertain a renewed request by Petitioner for a stay after this Decision on Institution is entered. Consequently, we find that this factor is neutral.

2. Fintiv Factor 2

Patent Owner contends that this factor “strongly weighs in favor of discretionary denial.” Prelim. Resp. 24. Patent Owner argues that trial in the District Court Litigation “is scheduled for January 5, 2026” which is three months before the projected statutory deadline for a Final Written Decision in this proceeding. *Id.* (citing Ex. 2001). Petitioner argues that this factor is “at worst neutral.” Pet. 74.

The District Court’s Docket Control Order, filed in the district court on August 5, 2024, sets January 5, 2026 as the date to commence Jury

Selection in the column labelled “Original Date.” Ex. 2001, 1. The column next to “Original Date” is labelled “Amended Date” and that column is blank. *Id.* The Docket Control Order is prefaced with the statement “it is hereby **Ordered** that the following schedule of deadlines is in effect until further order of this Court.” *Id.* The Docket Control Order also contemplates that the trial date may be continued under certain circumstances. *See id.* at 6 (“Motions for Continuance”). Based on this, it appears that January 5, 2026 date is not a firm date for starting jury selection in the District Court Litigation but contemplates the possibility of a continuance. Nonetheless, there remains the possibility that a trial could be concluded within approximately two to two and a half months after January 5, 2026 and prior to our statutory deadline in this case.

Fintiv instructs us that “the decision to institute will likely implicate other factors” when “the court’s trial date is at or around the same time as the projected statutory deadline.” *Fintiv*, IPR2020-00019, Paper 11 at 9. Given that the originally-scheduled trial date is far away and the final decision date in this case will be approximately three months after the originally scheduled trial date, we find that this factor weighs slightly in favor of exercising our discretion to deny institution.

3. *Fintiv* Factor 3

Patent Owner contends that this factor weighs heavily in favor of exercising our discretion because the district court has issued various orders, discovery is under way, and the parties exchanged infringement contentions and invalidity contentions. Prelim. Resp. 26.

Petitioner contends that this factor favors institution because it “acted diligently and almost no parallel investment has occurred.” Pet. 73.

According to Petitioner, Patent Owner served infringement contentions on July 18, 2024, fact discovery does not close until August 18, 2025, expert discovery closes on September 22, 2025, claim construction efforts by the parties begins on March 4, 2025, and the *Markman* hearing will not take place until July 8, 2025. *Id.* at 73–74 (citing Ex. 1016; Ex. 1017, 3–4).

Although the parties and district court have invested some minimal time in the District Court Litigation, substantial work remains to be done including the completion of fact and expert discovery, claim construction briefing, pretrial motions, and preparation of a joint pretrial order. *See* Ex. 2001, 1–5.

For these reasons, we find that this factor weighs in favor of not exercising our discretion to deny institution.

4. *Fintiv Factor 4*

After the Preliminary Response was filed, Petitioner submitted a stipulation stating that it will not pursue, in the District Court Litigation, any ground that was raised or could have reasonably been raised in this proceeding. Paper 8, 1. Petitioner’s stipulation, thus, aligns with the stipulation relied on by the Board in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12, 18–19 (PTAB Dec. 1, 2020) (precedential).

Patent Owner argues that we should reject any “late” *Sotera* stipulation. Prelim. Resp. 27. The only authority cited for this argument are Board decisions concerning stipulations filed *after* a Decision on Institution was entered. *Id.* at 28–29. Petitioner’s stipulation was filed prior to this Decision being entered, is not “late,” and, thus, we decline to reject Petitioner’s stipulation.

In *Sotera Wireless*, the Board found that a stipulation such as the one proffered here by Petitioner addressed “concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions” and “ensures that an *inter partes* review is a ‘true alternative’ to the district court proceeding.” *Sotera*, IPR2020-01019, Paper 12 at 19. For these reasons, we find that this factor weighs “strongly in favor of not exercising discretion to deny institution.” *Id.*

5. *Fintiv Factor 5*

Patent Owner contends this factor weighs in favor of exercising our discretion to deny institution because Petitioner and Patent Owner are parties in the District Court Litigation. Prelim. Resp. 23. Petitioner argues that this factor is “at worse neutral.” Pet. 73.

Because Petitioner is the defendant in the District Court Litigation, this factor weighs in favor of exercising our discretion to deny institution.

6. *Fintiv Factor 6*

Patent Owner contends that “Petitioner does not present a strong case on the merits, further supporting denial of institution.” Prelim. Resp. 27. Petitioner contends that the merits support institution. Pet. 73.

As discussed above, the Petition sets forth challenges that meet the reasonable likelihood standard for institution based on the present record. We find that this factor is neutral.

7. *Fintiv Conclusion*

When we evaluate the *Fintiv* factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. As discussed above, factor 4 weighs strongly in favor of not exercising our discretion to deny institution

and factor 3 also weighs in favor of not exercising our discretion to deny institution while factors 2 and 5 weigh in favor of exercising our discretion. After consideration of all factors, we determine that efficiency, fairness, and integrity of the system are best served by not exercising our discretion to deny institution.

IV. CONCLUSION

Based on the present record, we determine that Petitioner demonstrates a reasonable likelihood that it would prevail in establishing that at least one challenged claim of the '673 patent is unpatentable. We, thus, institute an *inter partes* review of all challenged claims of the '673 patent based on all grounds in the Petition. At this stage of the proceeding, we have not made a final determination under 35 U.S.C. § 318(a) with respect to the unpatentability of any challenged claim.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '673 patent is instituted with respect to all challenged claims and grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4(b), *inter partes* review of the '673 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2024-01403
Patent 7,772,673 B2

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