

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,772,673

Filing Date: March 16, 2007

Issue Date: August 10, 2010

Inventors: Kevin Q. Yin, Amol Kalburge, David J. Howard,
Arjun Kar-Roy, and Dieter Dornisch

Title: DEEP TRENCH ISOLATION AND METHOD OF FORMING SAME

DECLARATION OF JOHN BERG

Case No. IPR2024-01403

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I, John Berg, declare as follows:

I. INTRODUCTION

1. I am over eighteen years of age and I would be competent to testify as to the matters set forth herein if I am called upon to do so.

2. I have been retained by Fabricant LLP, counsel for the Patent Owner Harbor Island Dynamic LLC (hereinafter referred to as “HID” or “Patent Owner”), to review U.S. Patent No. 7,772,673 (the “’673 Patent”) entitled DEEP TRENCH ISOLATION AND METHOD OF FORMING SAME, and to provide my technical review, analysis, insights, and opinions regarding the ’673 Patent in view of the prior art cited by Petitioners Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung” or “Petitioner”). I submit this Declaration in support of Patent Owner’s Response in this IPR proceeding. I have personal knowledge of the matters stated herein and would be competent to testify to them if required.

II. BACKGROUND AND QUALIFICATIONS

3. This section summarizes my career history, education, publications, and other relevant qualifications. My full *curriculum vitae* (“CV”) is included as **Exhibit 2005**.

4. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980. My current work focuses on CMOS

circuit design, simulation, modeling, and processing.

5. I am currently an expert consultant in semiconductor design and manufacturing. Since 2010, I have performed this work as a Principal at Berg-Attenborough, Inc., a consulting firm that provides technical consulting and expert witness services to semiconductor companies and law firms. My work as an expert consultant has included developing advanced CMOS processes and multi-chip modules that incorporate logic circuits using SOI, memory devices such as dynamic random-access memory ("DRAM") and flash memory, as well as performing device analysis and testing using scanning electron microscope ("SEM") and transmission electron microscopy ("TEM") technology. In addition to my work as an expert consultant, I have over 35 years of experience as an executive and as an engineer in the semiconductor industry. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980, and now I am focusing on analog CMOS circuit design, simulation, modeling, and processing.

6. Prior to Transfer Devices, I was a Managing Director at Cypress Semiconductor, where I managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, I was Vice President of Technology Development at Zilog, where I managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and

embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier.

7. Because of my background, training, and experience, I am qualified as an expert to opine on the issues with which I have been tasked. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, Ex. 2005.

8. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

III. COMPENSATION

9. My compensation for time worked on this proceeding is not dependent on any issues related to the '673 Patent, the outcome of this proceeding, or the substance of my opinions. My compensation for time worked on this proceeding is at my customary rate of \$560 per hour. I have no financial interest in, or affiliation with, the Patent Owner or any of the real parties in interest.

IV. LEGAL PRINCIPLES

A. Claim Construction

10. I understand that claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, *i.e.*, the meaning that the term would have to a person of ordinary skill in the art

(“POSITA”) in question at the time of the invention in light of what the patent teaches, unless it appears that the inventors were using them to mean something else. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as his/her own lexicographer (*i.e.*, provided special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope).

11. I understand that a POSITA is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but also in the context of the entire patent, including the specification and the prosecution history. The prosecution file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower interpretation. For these reasons, the words of the claim must be interpreted in view of, and be consistent with, the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

12. I understand that, to determine how a POSITA would have understood a claim term, one should look to those sources available that show what a POSITA would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that one looks primarily to the intrinsic patent evidence, but extrinsic evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

13. Additionally, the context in which a term is used in the Asserted Claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and not asserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

14. I understand that, while intrinsic evidence is of primary importance, extrinsic evidence, *e.g.*, all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may help one better understand

the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, I understand that it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

B. Anticipation

15. I understand that to anticipate a claim, a prior art reference must disclose all elements of the claim within the four corners of the document, and it must disclose those elements arranged as in the claim. I understand that a reference may anticipate, even if it does not expressly disclose all the elements if a POSITA reading the reference would at once envisage the claimed arrangement or combination.

16. I understand that if a reference fails to disclose even one element, it does not anticipate that claim. I understand that references that must be modified to disclose a claim element do not anticipate that claim.

C. Obviousness

17. I understand that a patent claim is unpatentable as “obvious” if the

subject matter of the claim as a whole would have been obvious to a person of ordinary skill in the art (POSITA) as of the time of the invention at issue.

18. I understand that the question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence.

19. I further understand that the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

20. I further understand that, to qualify as prior art for an obviousness analysis, a reference must be analogous art to the claimed invention. Analogous art is either from the same field of endeavor or reasonably pertinent to the problem with which the inventor is involved.

V. MATERIALS CONSIDERED

21. In providing my technical review, analysis, insights, and opinions, I have considered the '673 Patent and its prosecution history.

22. I have also considered the Petition filed by the Petitioner in this proceeding and the relevant exhibits relied on by Petitioner, including the expert declaration submitted by Scott E. Thompson, Ph.D. I have also reviewed the transcript of the deposition of Dr. Thompson, dated June 9, 2025 ("Ex. 2010").

23. I have also considered my own experience and knowledge, as discussed above, and described more fully in my CV, in areas including semiconductor design, manufacturing, and other related technologies.

VI. LEVEL OF ORDINARY SKILL IN THE ART

24. It is my understanding that I must address the issues set forth in this Declaration, from the viewpoint of a POSITA at the time of the invention to which the Asserted Patent pertains.

25. I understand that this hypothetical POSITA is considered to have the normal skills of a person in a certain technical field. I understand that factors that may be considered in determining the level of ordinary skill in the art include: (1) the education level of the inventor; (2) the types of problems encountered in the art; (3) the prior art solutions to those problems; (4) rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the education level of active workers in the field.

26. Considering the above factors, in my opinion, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. I also agree that a person could also have qualified as a POSITA with some combination of (1) more formal education (such as Master of Science degrees) and less technical experience, or

(2) less formal education and more technical or professional experience in the fields listed above.

27. I understand that Dr. Thompson has opined that a POSITA would have at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Ex. 1003, ¶64. While our contentions are similar, I disagree that a master's degree represents the ordinary level of skill. The '673 Patent is directed to an audience of engineers working to implement manufacturing processes. In the industry, it is typical for such engineers to have a bachelor's degree. Indeed, I myself implemented such processes with a bachelor's degree.

28. I understand that the '673 Patent is entitled to a March 16, 2007, priority date, and that is the relevant time period from which a POSITA would evaluate its disclosure and any prior art.

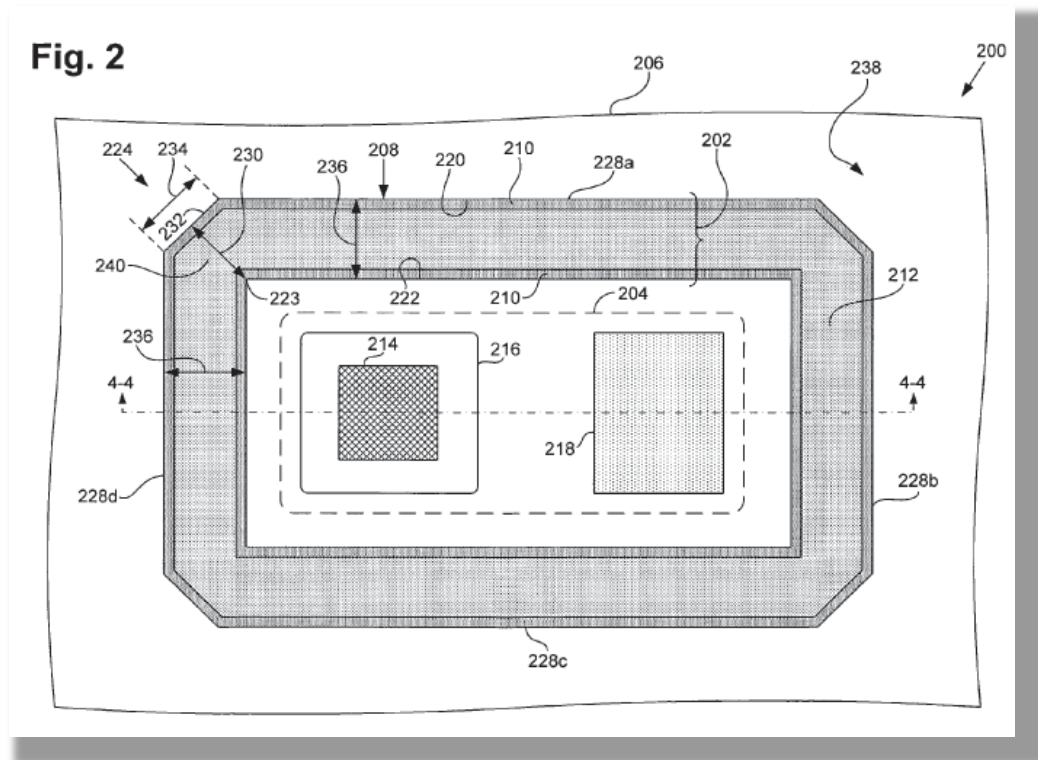
29. My qualifications and experience exceed those of a POSITA, under both my and Dr. Thompson's opinions. Nonetheless, my analysis and opinions herein regarding the Asserted Patent are given from the perspective of a POSITA.

VII. THE '673 PATENT'S CLAIMED INVENTION

30. The '673 Patent (Ex. 1001) is titled and directed to "Deep Trench Isolation and Method For Forming Same." It issued on August 10, 2010. The '673 Patent states that "the invention is in the field of isolation region formation in

semiconductor substrates.” ’673 Patent, 1:8-10. The ’673 Patent explains problems with existing deep trenches, namely that when using a “rectangular-shaped trench,” a “thick layer of polysilicon can be required to adequately fill the trench.” *Id.* 1:32-34. This reduces throughput. *Id.* at 1:35-38; 4:41-45. Moreover, the use of a thick polysilicon layer causes a significant amount of polysilicon flaking, requiring more frequent cleaning of the deposition furnaces and increasing manufacturing costs. *Id.* at 1:35-38; 4:45-50.

31. The ’673 Patent presents a novel solution, which is shown in Figure 2 of the ’673 Patent, below:



32. The corners of the deep trench 208, which includes outside wall 220 and inside wall 222, are “chamfered” to “significantly reduce trench corner width.” *Id.*, 4:24-36. Use of the claimed invention substantially reduces the thickness of the polysilicon layer, which “increases polysilicon fill process throughput and also significantly increases the average time between polysilicon deposition furnace cleaning.” *Id.* at 5:21-36.

VIII. CLAIM CONSTRUCTION

33. I understand that the parties agree that no claim construction is required to resolve this proceeding.

IX. THE RELEVANT PRIOR ART

A. Yin

34. I have reviewed U.S. Patent No. 6,995,449 to Yin et al. (Ex. 1004)¹ titled “Deep Trench Isolation Region With Reduced-Size Cavities in Overlying Field Oxide” and issued on Feb. 7, 2006. Yin is related to “forming isolation regions in semiconductor substrates.” Ex. 1004, 1:12-14.

35. Yin discloses problems with existing methods of forming deep trenches, noting that they cause “severe lateral etching of the field oxide region situated on the sidewalls of the trench.” *Id.* 1:57-59. Yin discloses and claims a

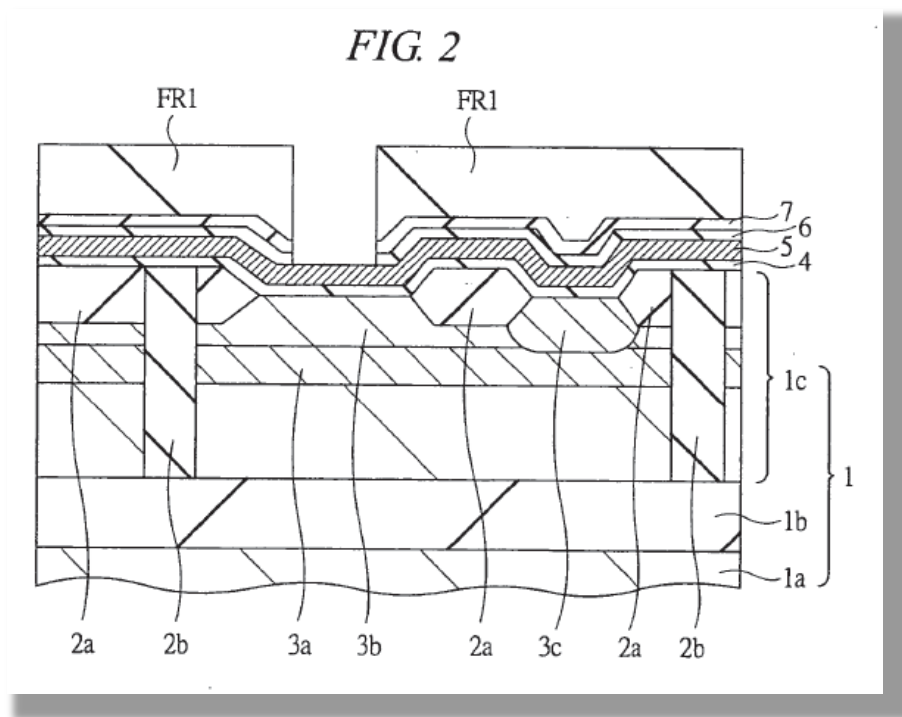
¹ Yin shares two inventors with the '673 Patent.

proposed solution, which is to create an “oxide liner” on the sidewalls of the trench by using Chemical Vapor Deposition, or CVD. *Id.* 2:38-41.

36. Yin does not disclose deep trenches used for isolation that are formed with chamfered corners.

B. Koshimizu

37. I have reviewed U.S. Patent Application Publication No. US 2005/0181569 to Koshimizu et al. (Ex. 1005) published on August 18, 2005. Koshimizu relates to “a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor.” Ex. 1005, ¶ [0001]. Koshimizu’s technique prevents “the sidewall-insulation film formed on the side surface” in a first opening portion from blocking the growth of a crystalline layer formed in a second opening portion. *Id.*, ¶¶ [0008]-[0012].



38. As shown above in Figure 2, Koshimizu discloses a deep isolation trench 2b, but does not disclose that this trench is filled with polysilicon. *Id.* ¶ [0052]. Koshimizu’s deep trench 2b “is formed by embedding, for example, a silicon oxide film in a deep trench dug so as to reach the insulation layer 1b through the isolation 2a and the semiconductor layer 1c from the upper surface of the isolation 2a. *Id.*

C. Norström

39. U.S. Patent No. 6,121,102 to Norström et al. (Ex. 1006) is titled “Method of Electrical Connection Through an Isolation Trench to Form Trench-Isolated Bipolar Devices” and issued on Sept. 19, 2000. Norström “relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes,

which are electrically isolated or confined by trenches.” Ex. 1006, 1:7-10. An object of the invention of Norström is to “provide a trench isolated transistor having good performance which takes a little area on a substrate.” *Id.* at 3:21-23. Norström discloses and claims the use of a “hole” in the trench under the active region of the bipolar device, which is filled with conducting material. *Id.* at 3:56-67.

40. The “hole” 157 in the trench 119 is disclosed below in Figure 13a:

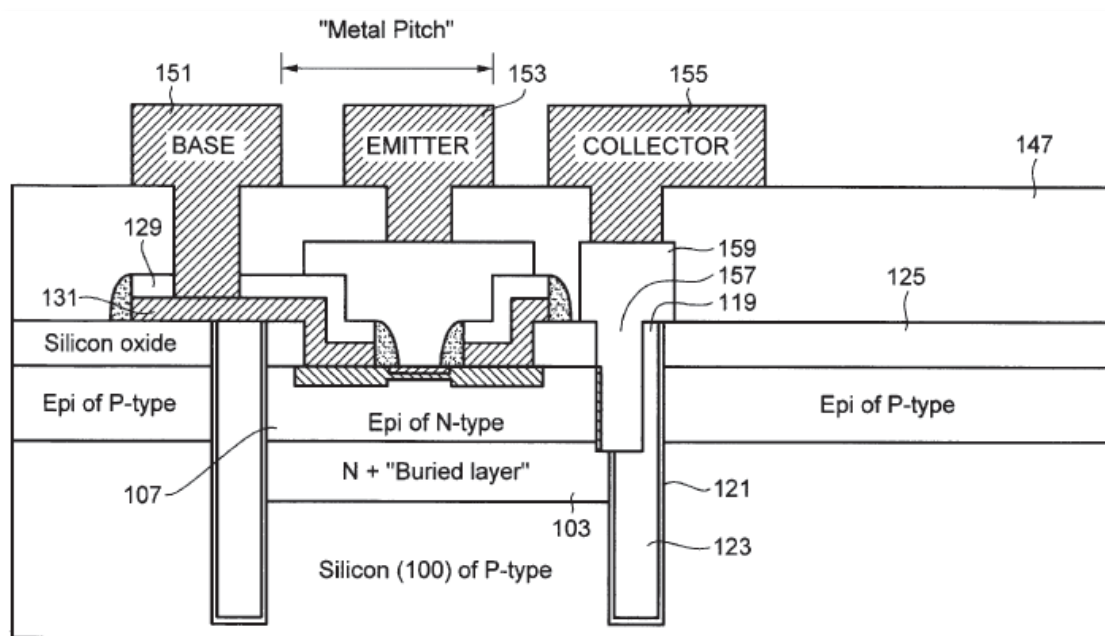


FIG. 13a

“The resulting hole 157 will then . . . have one of its sidewalls in direct contact with the N-doped epitaxial layer 107 and the bottom diffusion 103 and have its opposite sidewall located against the inner material in the trench.” *Id.* at 10:48-52.

X. GROUND 1: *Yin* and *Koshimizu* Do Not Render any Claims Obvious Because *Koshimizu* Is Not Analogous Art

41. As I explain above, the '673 Patent categorizes its field of the invention as “isolation region formation in semiconductor substrates.” '673 Patent, 1:7-10. More specifically, the '673 Patent is “directed to deep trench isolation and method for forming same.” *Id.*, 2:20-23. *See also id.*, Title. To that end, the specification provides detailed instructions on manufacturing such a trench and filling it. *Id.*, 5:42-9:3; Figs. 3, 4. A POSITA would recognize that the '673 Patent's field of endeavor is thus the formation of deep trench isolation regions.

42. Koshimizu's field of endeavor is the manufacture of semiconductor devices having a hetero-junction bipolar transistor. Ex. 1005, [0001].

43. These two fields of endeavor are not the same. The '673 Patent is not directed toward manufacturing a transistor; it focuses on filling a deep trench isolation region using a polysilicon filler. Indeed, the '673 Patent notes that a bipolar device is “utilized as an example of an electronic device to illustrate the present invention.” '673 Patent, 2:35-38. As the specification notes, the invention is agnostic to the type of device being isolated. *Id.* (“the invention's deep trench isolation region can be utilized to isolate[] electronic devices other than bipolar devices.”); *see also id.*, 3:51-55. A POSITA would recognize that the '673 Patent's deep trench isolation is not dependent on the type of device, such as a bipolar transistor.

44. In contrast to Koshimizu, the '673 Patent does not provide any instructions on manufacturing the components of a bipolar transistor. Instead, it provides detailed instructions on how to manufacture the deep trench and fill it with polysilicon. '673 Patent, 5:42-9:3; Figs. 3, 4.

45. Koshimizu, however, is focused on manufacturing a bipolar transistor. Koshimizu begins with a description of a prior art method of manufacturing such a transistor. Koshimizu, [0002]-[0003].

46. The Koshimizu inventors noted that:

[I]n the above method, an upper portion of the silicon nitride film on the bottom surface of the first opening portion is slightly etched when the first opening portion is formed. In particular, if the photoresist film is used as an etching mask at the time of forming the first opening portion, the silicon nitride film is easily etched because it is impossible to provide a sufficiently high selective ratio of the polycrystalline silicon film to the silicon nitride film. If the second opening portion is formed after forming the sidewall-insulation film on the side surface of the first opening portion under this condition as described above, a lower portion of the sidewall-insulation film becomes greatly protruded to a side of the second opening portion along a direction orthogonal to the main surface of the semiconductor substrate. If the above-mentioned dissimilar crystalline layer is made to grow under this condition, the growth of the dissimilar crystalline is blocked by the protrusion of the sidewall-insulation film. In particular, since the growth of the dissimilar crystalline is blocked at a portion of a bottom surface side of the polycrystalline silicon film for forming the base electrode, the dissimilar crystalline layer is unsuccessfully connected to the polycrystalline silicon film, whereby there is the problem that base resistance is greatly increased.

Koshimizu, [0004].

47. The problems described in Koshimizu have nothing to do with electrical isolation or forming of deep trench regions. They are, instead, related to issues in the prior art method of forming openings in film layers overlying the substrate, as needed for forming electrodes in the transistor. Koshimizu, [0003]-[0004]; *see also* Koshimizu, [0007]-[0012].

48. The remainder of Koshimizu is dedicated to its improved manufacturing process. Koshimizu, [0052]-[0064]. Koshimizu mentions deep trench isolation in a single paragraph and simply assumes that the reader can form such a region. Koshimizu, [0052]. Indeed, Koshimizu simply states “In an isolation region of the main surface (device forming surface) of the semiconductor layer 1e, a shallow isolation 2a and a deep trench isolation 2b are formed.” Koshimizu, [0052]. Koshimizu’s only discussion of forming the deep trench isolation is: “the deep trench isolation 2b is formed by embedding, for example, a silicon oxide film in a deep trench dug so as to reach the insulation layer 1b through the isolation 2a and the semiconductor layer 1e from the upper surface of the isolation 2a.” *Id.*

49. I understand that Petitioner argues first that the ’673 Patent is directed to “a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor.” Pet., 8. To the extent that Petitioner considers this the ’673 Patent’s field of endeavor, I disagree. The ’673 Patent’s field

of endeavor, as I explain above, is the formation of a deep trench isolation region, not merely the existence of one.

50. Petitioner next argues that the '673 Patent (and *Koshimizu*) is “directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors.” Pet., 11. To the extent that Petitioner considers this the '673 Patent’s field of endeavor, I disagree. The '673 Patent’s field of endeavor, as I explain above, is the formation of a deep trench isolation region, not manufacturing a transistor that happens to contain a deep trench. Petitioner’s proposal is too narrow because it does not include the focus of the '673 Patent (forming deep trench isolation). It is too broad because it characterizes the '673 Patent’s focus as manufacturing transistors—even though the '673 Patent is clear that transistors are merely an example.

51. Finally, Petitioner argues that the '673 Patent (and Norström) “is directed to the manufacture of ‘bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.’” Pet., 14. To the extent that Petitioner considers this the '673 Patent’s field of endeavor, I disagree. The '673 Patent’s field of endeavor, as I explain above, is the formation of a deep trench isolation region, not manufacturing a bipolar device or diode that happens to be isolated by a deep trench.

52. The '673 Patent and Koshimizu thus are in different fields of endeavor.

53. Petitioner does not argue that Koshimizu would be reasonably pertinent to the problem the '673 Patent inventors faced. In my opinion, it would not be reasonably pertinent.

54. As the '673 Patent explains, the problem faced by the inventors was that the prior art trenches required a thick layer of polysilicon to adequately fill them. '673 Patent, 1:30-34. Utilizing such a thick layer reduces the fill process throughput and requires more frequent deposition furnace cleaning, thus increasing costs. *Id.*, 1:34-38; 3:29-50. The inventors thus set out to design a process that formed a deep trench isolation region, filled by polysilicon, while at the same time reducing the amount of polysilicon required. *Id.*, 1:27-41, 3:29-50, 5:15-41.

55. A POSITA would not consider Koshimizu to be reasonably pertinent to this problem. Koshimizu does not mention polysilicon at all. Instead, Koshimizu's deep trench is filled with silicon oxide. Koshimizu, [0052]. Moreover, as I explain above, Koshimizu does not provide any details on manufacturing its trench or filling it.

56. Silicon oxide and polysilicon have vastly different stress characteristics, when used as deep trench fill material. Typically, the trench widths are on the order of tenths of microns to several microns, and the trench depths are on the order of ~1x to ~3x the width of the trench ('673 Patent, 4:55-5:14). It was

known to a POSITA at the time that having the trench fill material with a coefficient of thermal expansion (CTE) that was dissimilar to the CTE of the silicon substrate would cause potential defects in the silicon substates and thus, render the device useless. The CTE of silicon dioxide is known to be typically $\sim 0.24\text{E-}6/\text{deg K}^2$ and the CTE of silicon is known to be typically $\sim 2.6\text{E-}6/\text{deg. K}^3$ This order of magnitude difference in CTE was known to result in microdefects in the silicon substrate when wafers went through high temperature wafer processing. Such high temperature processing was used, post-deep trench fill, to activate dopants implanted after formation of the deep trench fill. Thus, today deep trench fill material is typically polysilicon, as polysilicon CTE of $2.9\text{E-}6/\text{degK}^4$, and the silicon substrate CTE are for all practical purposes nearly identical. Polysilicon deep trench fill eliminates the defects associated with using pure silicon dioxide films as deep trench material.⁵

57. Silicon oxide and polysilicon have vastly different electrical characteristics. These differences are important in the construction of the trench. Silicon dioxide is an electrically insulating layer. Polysilicon can be either an electrical semi-conductor, when it is not doped, or an electrical conductor, if it is

² Ex. 2006, C. Tsou, et.al., "Determination of Thermal Expansion Coefficient of Thermal Oxide," Sensors and Materials, Vol. 17, No. 8, 441-451 (2005).

³ Ex 2007, H Watanabe, et.al., "Linear Thermal Expansion Coefficient from 293 to 1000K," International Journal of Thermophysics, Vol. 25, No. 1, Jan. 2004, pp. 221-236.

⁴ Ex. 2008, J-H Chae, et. al., "Measurement of thermal expansion Coefficient of Poly-Si Using Microgauge Sensors," Sensors and Actuators, 75 (1999), pp. 222-229.

⁵ Ex. 2009, <https://anyisilicon.com/semipedia/deep-trench-isolation-dti/> : "By using materials like Polycrystalline silicon and high-reflectivity metal layers, these structures resist cracking."

heavily doped with arsenic, phosphorus, or boron.⁶ These differences require different process steps and different layout rules. Koshimizu teaches that the trench fill is a “silicon oxide film” 2b. Koshimizu, [0052]. In contrast, the ’673 Patent teaches an isolating “[silicon] oxide liner 428 (’673 Patent, 7:29) is grown along the walls and bottom surface of the deep trench prior to the deposition and formation of the “polysilicon filling 432” (*id.*, 8:36). The purpose of the ’673 liner is to electrically isolate the polysilicon trench fill material from the substrate: without such isolation to the substrate, the whole purpose of the deep trench isolation taught by the ’673 Patent is defeated. Koshimizu has no such liner, because Koshimizu’s deep trench fill is silicon oxide and silicon oxide by itself is electrically isolated, such that there is no electrical need for a liner material. Additionally, the thinness of the liner, when compared to the thickness of the polysilicon, is such that the CTE of the oxide liner does not increase the defects in the substrate.

58. For the stress and electrical reasons above, a POSITA would not have looked to prior art which used a silicon dioxide deep trench fill for inventing a polysilicon deep fill trench, as taught by the ’673 Patent.

59. Moreover, Koshimizu does not provide any detail on the formation of its trenches, the amount of material necessary to fill it, or any other detail that would

⁶ Ex. 2011, <https://www.universitywafer.com/silicon-resistivity.html> “For intrinsic (undoped) silicon, the resistivity is typically in the range of 1,000 to 10,000 ohm-cm. Doped silicon wafers can have resistivities as low as 0.001 ohm-cm for heavily doped n-type or p-type silicon, up to several thousand ohm-cm for lightly doped materials.”

be useful or relevant to a POSITA attempting to reduce the amount of polysilicon needed to fill its trenches.

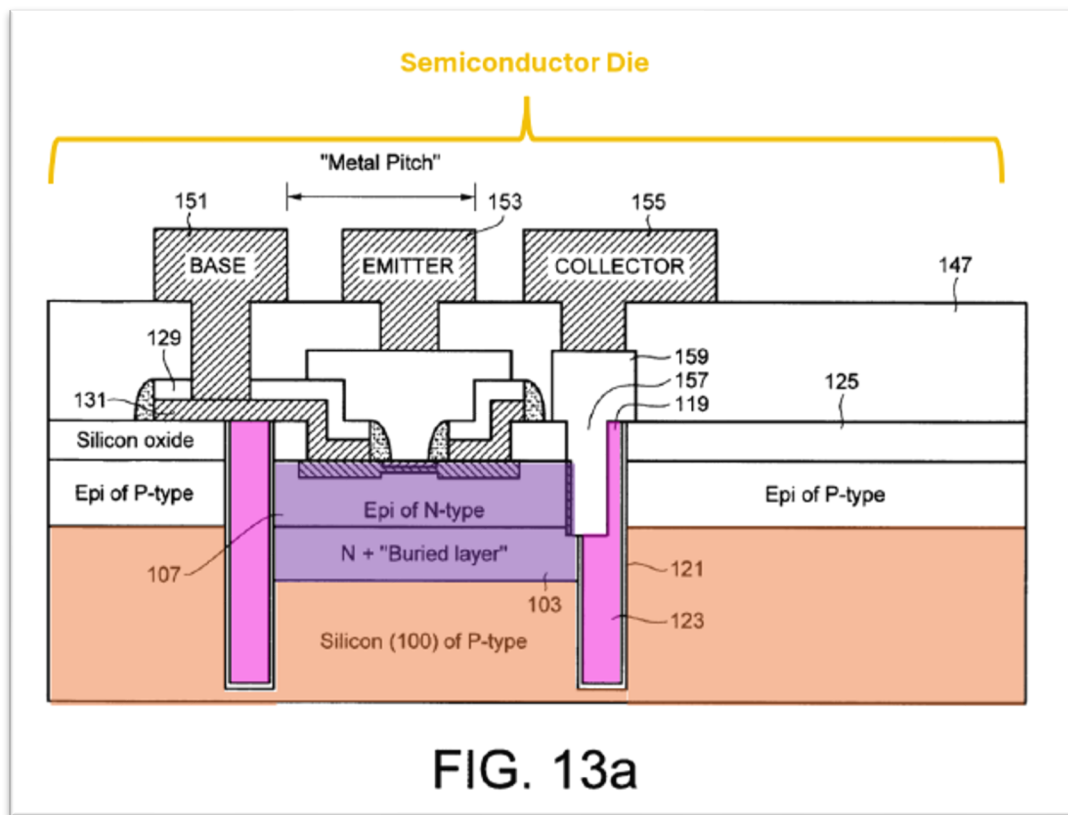
60. Accordingly, Koshimizu is not in the same field of endeavor as the '673 Patent, and a POSITA would not find it reasonably pertinent to the same problem.

61. Therefore, no claims are rendered obvious under Ground 1.

XI. Ground 2: *Norström* Does Not Anticipate any Claim

62. Norström does not anticipate any claim because it fails to disclose a “trench situated in a substrate of said semiconductor die” with at least one “trench chamfered corner” as required by all claims.

63. Petitioner relies on Figure 13a of Norström to show that its identified trench is in the substrate. Pet., 62.



Pet., 62.

64. Norström repeatedly explains that the structures in Fig. 13a, identified with 119, are “trenches.” Norström, Figs. 3, 8; 7:38-40 (“openings to isolating trenches 119 are lithographically defined...”); 7:50-54 (“the openings of the trenches 119”); 7:54-59 (“the openings of the trenches 119”), 7:60-64 (“After forming the trenches 119...”), 9:31-35 (“openings, in which isolating trenches 119 will be formed, are lithographically defined”), 9:36-47 (“multiple use of “the trenches 119”), 10:4-9 (“the trench 119 at this side”), 10:14-15 (“The opening of the trench 119 at this side...”), 10:34-38 (“the corresponding trench 119”), 10:44-46 (“inner

border line of the trenches”) 10:48-56 (“trench corresponding with hole 157”); 11:35-40 (“trench corresponding with contact hole for collector”); 11:37-40 (“the trenches 119 may then be filled with silicon dioxide”).

65. Indeed, Norström always discusses “trenches 119” as a set of multiple trenches. The few times when it uses trench 119 in the singular is when it is referring to a single trench on either: a) the side with the collector contact and corresponding hole 157 (10:48-56; 11:35-40) or b) the side with the emitter (10:14-15, 10:34-38).

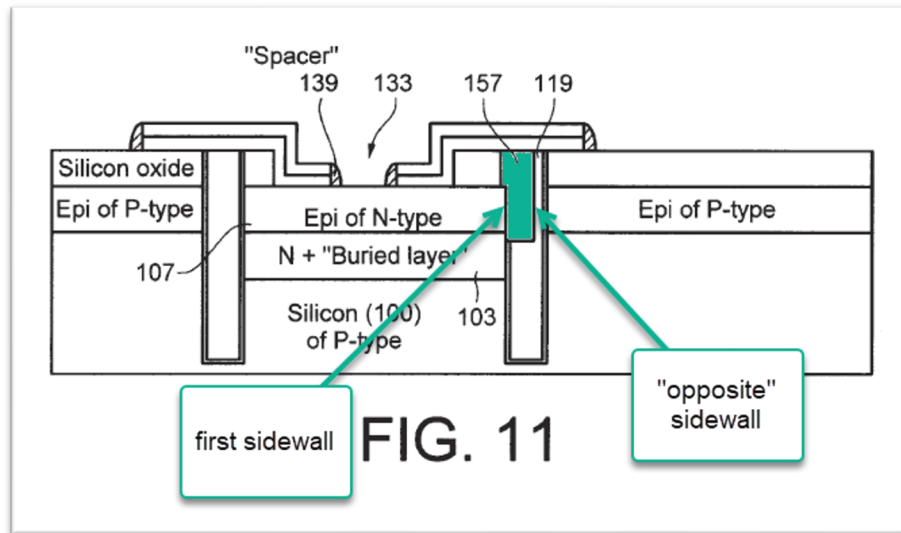
66. A POSITA would thus understand that the trenches 119 illustrated in Fig. 13a are a set of at least two trenches.

67. My opinion is further confirmed by Norström’s explanation that, on the left side,⁷ a region of layers 129 and 131 is left “so that they extend over the trench 119 at this side for forming a connecting region for the base.” Norström, 10:4-25. It goes on to state that the collector contact hole 157 is “self-aligned with the sidewall of the [right side] trench.” Norström, 10:32-56. Norström provides a detailed description of how it achieves this alignment. *Id.* The result is that “The resulting hole **157** will then, is apparent from FIG. **11**, have one of its sidewalls in direct contact with the N-doped epitaxial layer **107** and the bottom diffusion **103** and have

⁷ “At that side of the emitter opening **133**, which corresponds to the side of the base-emitter opening **115**,” *Id.*, 10:4-5.

its *opposite sidewall located against the inner material in the trench.*” *Id.*, 10:48-

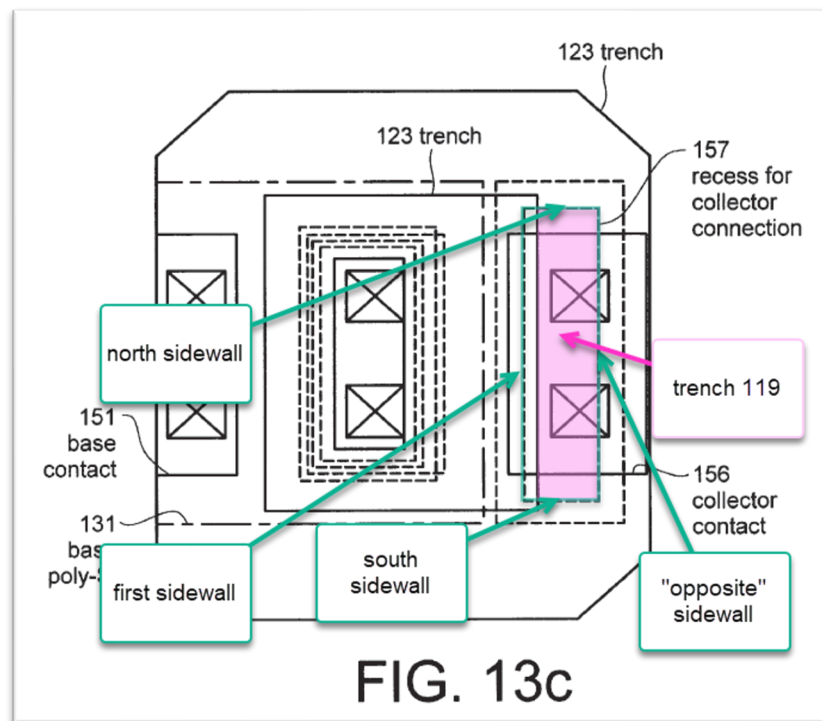
53. I have annotated Fig. 11 to show this arrangement:



Norström, Fig. 11 (annotations added).

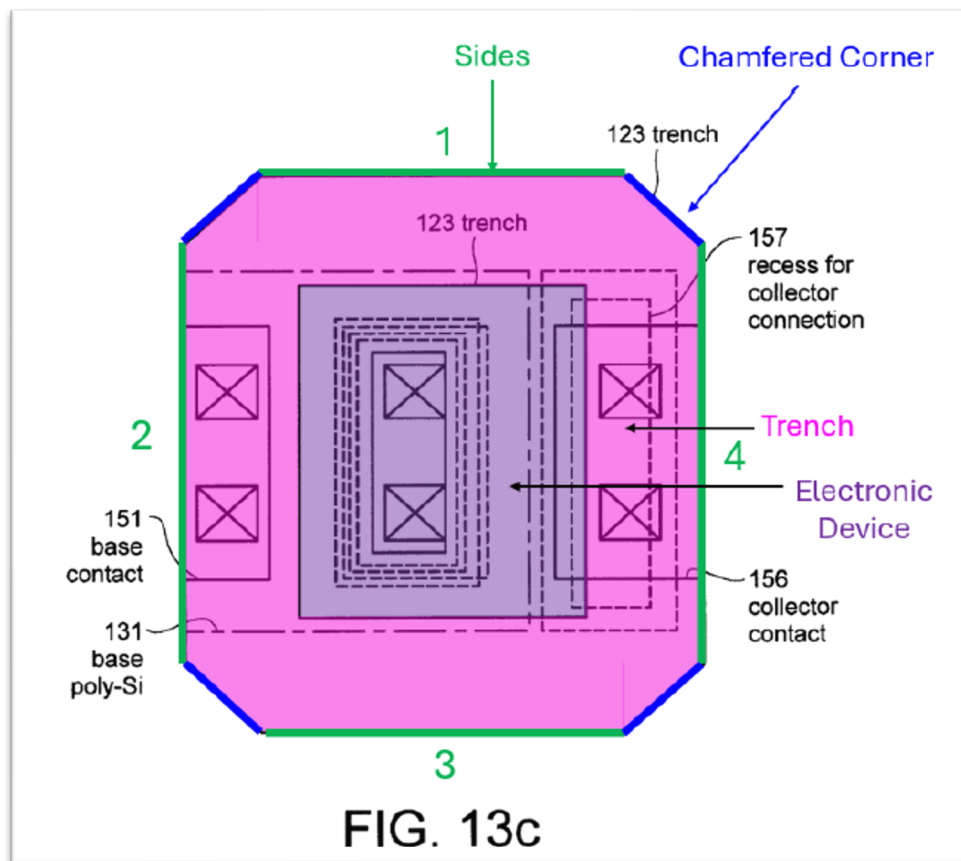
68. Fig. 13a shows the same arrangement, though later in the process. Norström, 10:57-11:2. The other two sidewalls of the collector hole 157, while not visible in Fig. 11 or 13a, “will in the normal case be located against the inner material of the trench 119.” *Id.*, 10:53-56. In other words, the north and south faces of the collector hole 157 will align with the north and south faces of the right-hand trench 119.

69. The plan view 13c shows the collector hole, but not the trench 119. Adding the right-hand trench 119 as described in Norström 10:32-56 results in:



70. The above Figure shows collector hole 157 (outlined in green), with its four sidewalls. The first (left) sidewall is aligned with the epitaxial layer 107. The opposite (right sidewall) is aligned with the right sidewall of the trench, and the north and south sidewalls are “located against the inner material of the trench 119.” Norström 10:32-56.

71. Unannotated Fig. 13c, in contrast, illustrates a different singular trench, labeled 123. Petitioner relies on this trench for the “trench chamfered corner” limitation. Pet., 60-63.



Pet., 61.

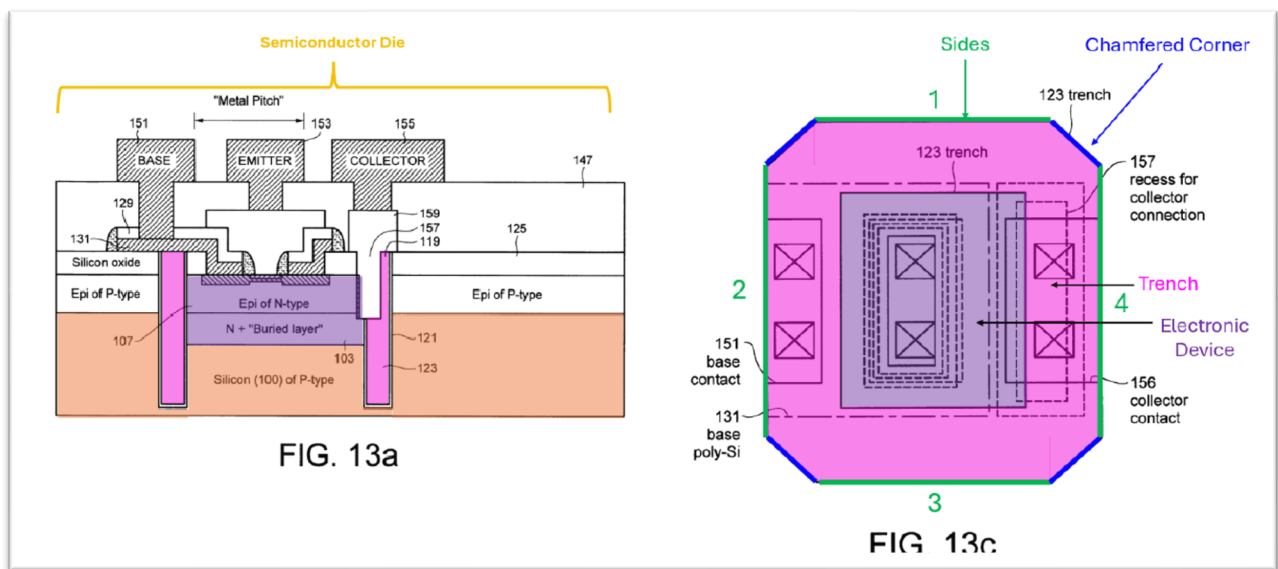
72. Petitioner treats the multiple “trenches 119” and singular “trench 123” as the same trench. Pet., 60-63.

73. In my opinion, a POSITA would not consider trenches 119 and trench 123 to be the same structure.

74. At the outset, 119 is always described as a set of multiple trenches, while 123 is a single trench. Norström only refers to 123 as “trench” once in the specification and only in the singular. Norström, 16:39-42 (“the outer sidewalls of the trench 123 shown in FIG. 13c have no right angles...”).

75. In all other portions of the specification, 123 is an “isolating material.”
Norström, 7:44-50, 9:42-48.

76. Besides the difference in identifying numbers, the geometry of trench 119 is radically different from that of trench 123. Below, I reproduce Petitioner’s annotated Figs. 13a and 13c side by side.



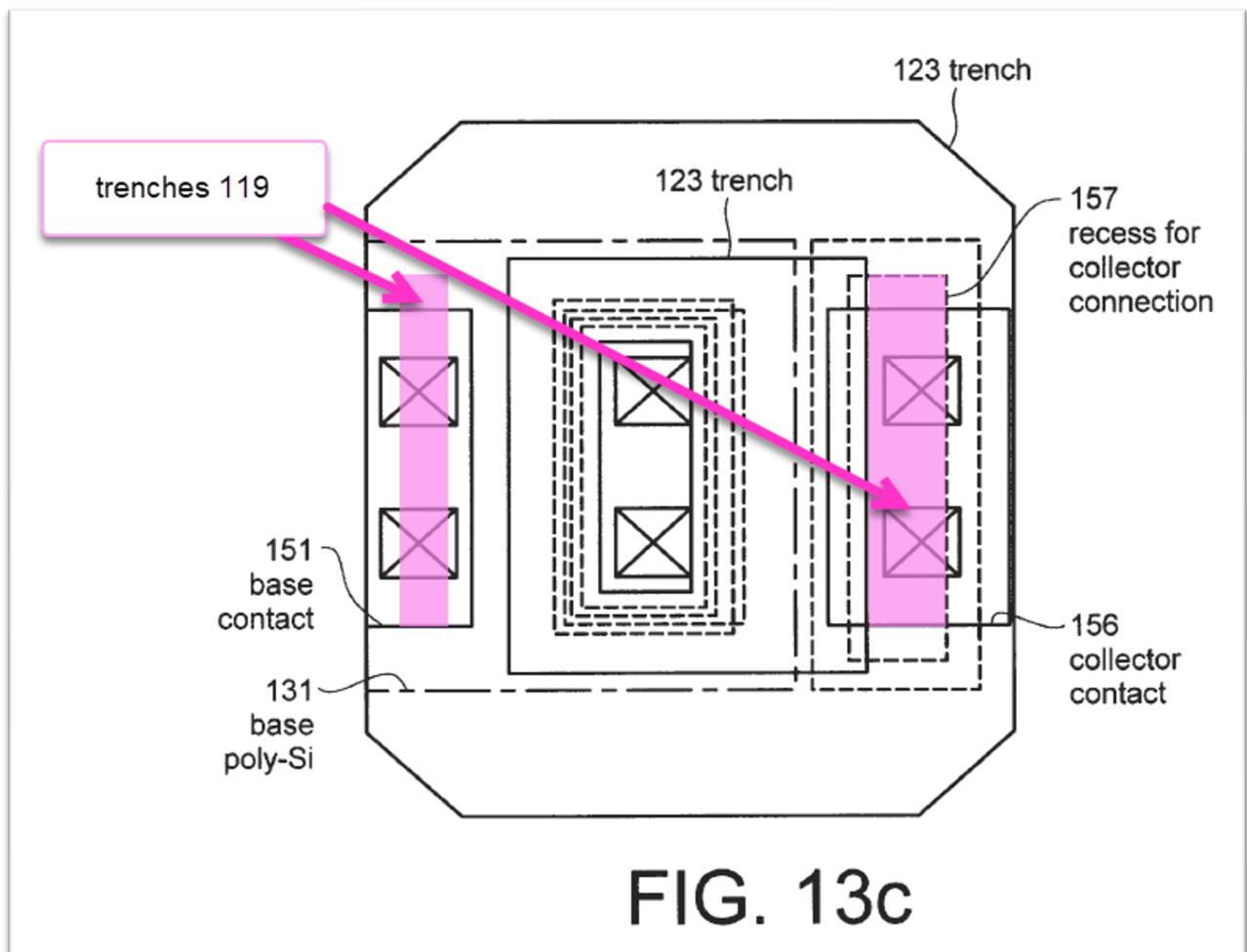
Pet., 61-62.

77. As shown above, Fig. 13a’s trenches 119 are narrow. The left most trench is entirely under the base contact 151. The right most trench is entirely under the collector contact and almost aligned with the right side of the collector contact hole 157.

78. In contrast, Fig. 13c shows a single large trench 123. Critically, trench 123 entirely envelops base contact 151. On the right-hand side, trench 123 extends

to the right beyond the collector contact hole 157. No part of trench 123 is shaped anything like trenches 119.

79. In the below Figure, I have drawn the approximate location of trenches 119 if they were visible in Fig. 13c, based on Fig. 13a's illustration and the description at 10:32-56:



80. As can be seen, trenches 119 are approximately centered under the collector contact, and offset towards the right of the base contact, as shown in Fig. 13a.

81. Even if the trenches 119 extended in a box around the emitter contact, they would not match the geometry of trench 123.

82. In sum, for trenches 119 to be the same structure as trench 123, one would have to ignore the difference in identifier markings (119 vs. 123); the difference in singular/plural; the explicit description of the location of the trenches shown in Fig. 13a and described in 10:32-56; and the explicit description that three of the collector hole 157's four sidewalls are in contact with the inner material of the trench 119. A POSITA would not ignore these issues, especially as the simpler explanation is that trench 119 and trench 123 are different structures.

83. Norström does not disclose trench 119 as having chamfered corners.

84. Norström does not disclose trench 123 as being in the substrate.

85. Norström thus does not disclose the trench claimed and required in all claims of the '673 Patent. Accordingly, Norström does not anticipate any claims.

XII. Ground 3: Norström Does Not Render Obvious Claims 7 and 15

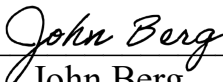
86. Ground 3 is directed solely to Claims 7 and 15, and does not remedy the deficiencies of *Norström* discussed above with respect to Ground 2.

87. Thus, Norström does not render obvious any claims under Ground 3.

XIII. CONCLUSION

88. I declare under penalty of perjury that the foregoing is true and correct.

Dated: June 16, 2025



John Berg