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IPR2024-01403: U.S. 7,772,673

US007772673B1

(10) **Patent No.:** US 7,772,673 B1
(45) **Date of Patent:** Aug. 10, 2010

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,933,749	A *	8/1999	Lee	438/435
6,107,161	A *	8/2000	Kitaguro et al.	438/463

* cited by examiner

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(74) Attorney, Agent, or Firm—Farjami & Farjami LLP

(57) ABSTRACT

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 469 days.

According to one exemplary embodiment, a semiconductor die including at least one deep trench isolation region for isolating an electronic device (for example, a bipolar device) includes a trench situated in a substrate of the semiconductor die, where the trench has sides surrounding the electronic device, and where the trench has at least one trench chamfered corner formed between and connecting the sides of the trench. The at least one trench chamfered corner is formed between a chamfered corner of an outside wall of said trench and a corner of an inside wall of the trench. A trench corner width at the at least one trench chamfered corner is less than a trench side width along the sides of the trench.

(21) Appl. No.: 11/724,916

(22) Filed: Mar. 16, 2007

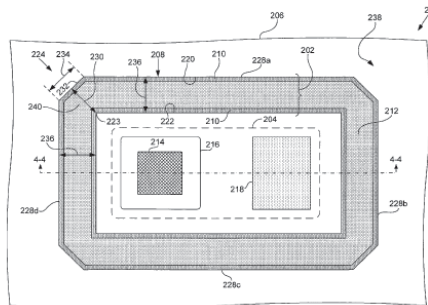
(51) Int. CL
H01L 21/04 (2006.01)

(52) U.S. CL 257/510; 257/520; 257/E:27.001
(58) Field of Classification Search 257/510

(58) **Field of Classification Search** 257/510,
257/520, E27.001
See application file for complete search history.

See application file for complete search history

17 Claims, 9 Drawing Sheets



Ground 1: *Koshimizu*

(12) **United States Patent** **Yin et al.**

(54) **DEEP TRENCH ISOLATION AND METHOD FOR FORMING SAME**

1. Field of the Invention

The present invention is generally in the field of semiconductor fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor substrates.

Deep trench isolation and method for forming same substantially as shown in and/or described in connection with at least one of the figures, as set forth more completely in the claims.

The present invention is directed to deep trench isolation and method for forming same. The following description contains specific information pertaining to the implementa-

Ex. 1001, Title, 1:5-10, 1:45-49, 2:20-23

Ground 1: *Koshimizu*

Yin is analogous art to the '673 Patent because *Yin*, like the '673 Patent, is directed to a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor. *See* Thompson Dec., ¶ 70;

Koshimizu is analogous art to the '673 Patent because, like the '673 Patent, it is directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors. *See*

Norström is analogous art to the '673 Patent because, like the '673 Patent, it is directed to the manufacture of “bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” Thompson Dec., ¶ 77 (quoting *Norström*, 1:7-10; '673

Pet., 8, 11, 14

Patent, Field of Invention).

POR, 13-15

Ground 1: Koshimizu

US 2005/0181569 A1

Aug. 18, 2005

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based gas can be explained by the magnitude of binding energy. When a photoresist film cures, Si—C binding energy (about 402 kJ/mol) is smaller than Si—O binding energy (465 kJ/mol). Consequently, an etching rate of SiO₂ by Cl is extremely slow. That is, the selective ratio is great. In contrast, when the photoresist film is used as an etching mask, carbon(C) exists in a reaction system. That is, since a surface of a photoresist pattern 59 is stuck in a dry-etching treatment, as shown in FIGS. 28 and 29, carbon is discharged from the photoresist pattern 59 into a chamber. Meanwhile, since the C—O binding energy (1077 kJ/mol) is stronger than the Si—C binding energy, a Si—O binding force weakens as shown in FIG. 20 if a bond of C—O is formed on the surface 72 of the silicon oxide film 70. If the Si—O binding force weakens, a bond of Si—Cl is formed and etching of the silicon oxide film 70 advances as shown in FIG. 31. That is, the etching selective ratio of the polycrystalline silicon film 56 to the silicon oxide film 70 lowers. This phenomenon becomes more prominent if the silicon nitride film is replaced with the silicon oxide film 70. Consequently, as shown in FIG. 23, when the silicon oxide film 58 and the lower polycrystalline silicon film 56 are etched by using the photoresist pattern 59 as an etching mask in forming the first opening portion 60, an upper portion of the underlying silicon nitride film 55 also is excessively etched, which results in occurrence of the above-mentioned problems.

[0050] Therefore, in the present embodiment, the sidewall insulation film formed on the side surface of the first opening portion is prevented from blocking the growth of the disordered crystalline layer formed in the second opening portion. As one example for this, the photoresist film is not used as an etching mask and the hard mask is used as an etching mask to form the first opening portion. In addition, the length of the portion of the sidewall-insulation film protruded to a side of the second opening portion is adjusted so that blocking of the growth of disordered crystalline layer is prevented. Hereinafter, one specific example of a manufacturing method for the semiconductor device according to the present embodiment will be described.

[0051] The semiconductor device of the present embodiment is one used for telecommunication equipment such as optical transmission systems (photoelectric transfer apparatus, etc.), cellular phones, high-frequency device products (VCO: voltage controlled oscillator or high-frequency amplifier circuits, etc.), radio (HF: radio frequency) telecommunication equipment (wireless LAN (local area network) or electronic equipment for Bluetooth, etc.).

[0052] In this case, a manufacturing method for a semiconductor device having an n-p-n-type HBT (hetero-junction bipolar transistor), which can achieve a high-speed operation, is illustrated. However, the present invention can be applied also to a manufacturing method for a semiconductor device having a p-n-p-type HBT. FIGS. 1 through 15 are schematic views showing a principal portion in the manufacturing process of a semiconductor device, and FIG. 16 is a plan view showing a principal portion of the semiconductor device of FIG. 15. As shown in FIG. 1, the semiconductor substrate (hereinafter abbreviated as "substrate") 1 is, for example, a nearly planar circular SOI (silicon on insulator) wafer. That is, the substrate 1 has a semiconductor layer 1c on a support substrate 1a via an insulation layer 1b. The support substrate 1a is made from, for example, single

crystalline silicon (Si) and has a function to secure mechanical strength of the substrate 1. The insulation layer 1b is made from, for example, a silicon oxide (SiO₂) film. The semiconductor layer 1c is made from, for example, a single crystalline silicon (Si) film.

On the main surface of the semiconductor layer 1c (that is, the main surface of the substrate 1), a device is formed. In an isolation region of the main surface (device forming surface) of the semiconductor layer 1c, a shallow isolation 2a and a deep trench isolation 2b are formed. The shallow isolation 2a is made from a silicon oxide film formed by, for example, a LOCOS (local oxidation of silicon) method. By this isolation 2a, a plane range of an active region is defined. In addition, the deep trench isolation 2b is formed by embedding, for example, a silicon oxide film in a deep trench dug so as to reach the insulation layer 1b through the isolation 2a, and the semiconductor layer 1c from the upper surface of the isolation 2a. By this deep trench isolation 2b, each device region in the semiconductor layer 1c is completely separated electrically. Note that the isolation 2a may be formed into a so-called shallow groove isolation (SGI) which is formed by

embedding, for example, a silicon oxide film inside a trench dug so as to reach the insulation layer 1b. In the semiconductor layer 1c of an HBT region, an n⁺-type collector embedding region 3a is formed. In this collector embedding region 3a, for example, antimony (Sb) is contained. On the other layer of the collector embedding region 3a, the n⁺-type collector region (first semiconductor region) 3b and the n⁺-type collector extraction region 3c are formed. In this collector region 3b, the collector extraction region 3c, for example, phosphorus (P) is contained. The collector region 3b and the collector extraction region 3c are separated by the isolation 2a provided therebetween and electrically connected through the collector embedding region 3a.

[0053] First, on the main surface of this kind of substrate 1 (SOI wafer), an about 95 nm thick insulation film (first insulation film) 4 made from, for example, a silicon oxide film etc., an about 200 nm thick conductor film (first semiconductor film, first polycrystalline silicon film) 5a, and an about 100 nm thick insulation film (second insulation film, hard insulation film) 6 made from a silicon nitride film etc., and an about 100 nm thick insulation film (third insulation film) 7 made from a silicon oxide film etc. are stacked up successively in this order from the bottom layer by a CVD (chemical vapor deposition) process etc. Subsequently, on the insulation film 7, a photoresist pattern (hereinafter abbreviated as "resist pattern") FR1, from which the first opening forming region is exposed out with which other region except it is covered, is formed by a photolithography technique (hereinafter abbreviated as "lithography technique"). Thereafter, as shown in FIG. 2, the resist pattern FR1 is used as an etching mask and the insulation films 7 and 6 exposed from it are etched successively by an anisotropic dry-etching treatment. Upon completion of the etching, the resist pattern FR1 is removed by etching etc., as shown in FIG. 3.

[0054] Next, the suppression insulation film 7 made from a silicon oxide film etc. is used as an etching mask (hard mask) and the conductor film 6 exposed therefrom is etched by an

on the main surface of the substrate 1, a device is formed. In an isolation region of the main surface (device forming surface) of the semiconductor layer 1c, a shallow isolation 2a and a deep trench isolation 2b are formed. The shallow isolation 2a is made from a silicon oxide film formed by, for example, a LOCOS (local oxidation of silicon) method. By this isolation 2a, a plane range of an active region is defined. In addition, the deep trench isolation 2b is formed by embedding, for example, a silicon oxide film in a deep trench dug so as to reach the insulation layer 1b through the isolation 2a, and the semiconductor layer 1c from the upper surface of the isolation 2a. By this deep trench isolation 2b, each device region in the semiconductor layer 1c is completely separated electrically. Note that the isolation 2a may be formed into a so-called shallow groove isolation (SGI) which is formed by embedding, for example, a silicon oxide film inside a

Ex. 1005, [0052]

Ground 1: *Koshimizu*

1. Field of the Invention

The present invention is generally in the field of semiconductor fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor substrates.

Ex. 1001, 1:5-10

TECHNICAL FILED OF THE INVENTION

[0001] The present invention relates to a semiconductor device and a manufacturing technique therefor and particularly to a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor (hereinafter abbreviated as "HBT") and to a manufacturing method for the semiconductor device.

Ex. 1005, [0001]

Ground 1: *Koshimizu*

1. Field of the Invention

The present invention is generally in the field of semiconductor fabrication. More particularly, the invention is in the field of isolation region formation in semiconductor substrates.

Ex. 1001, 1:5-10

35 It is noted that although a bipolar device is utilized as an example of an electronic device to illustrate the present invention, the invention's deep trench isolation region can be utilized to isolated electronic devices other than bipolar devices. FIG. 1 shows a top view of structure 100, which includes a conventional deep trench isolation region 102 and bipolar

Ex. 1001, 2:35-38

It is again noted that although a bipolar device (i.e. a bipolar transistor) is utilized as an example of an electronic device to illustrate the present invention, the invention's deep trench isolation region can be utilized to isolated electronic devices other than bipolar devices. FIG. 2 shows a top view of struc-

Ex. 1001, 3:51-55

Ground 2: *Norström*

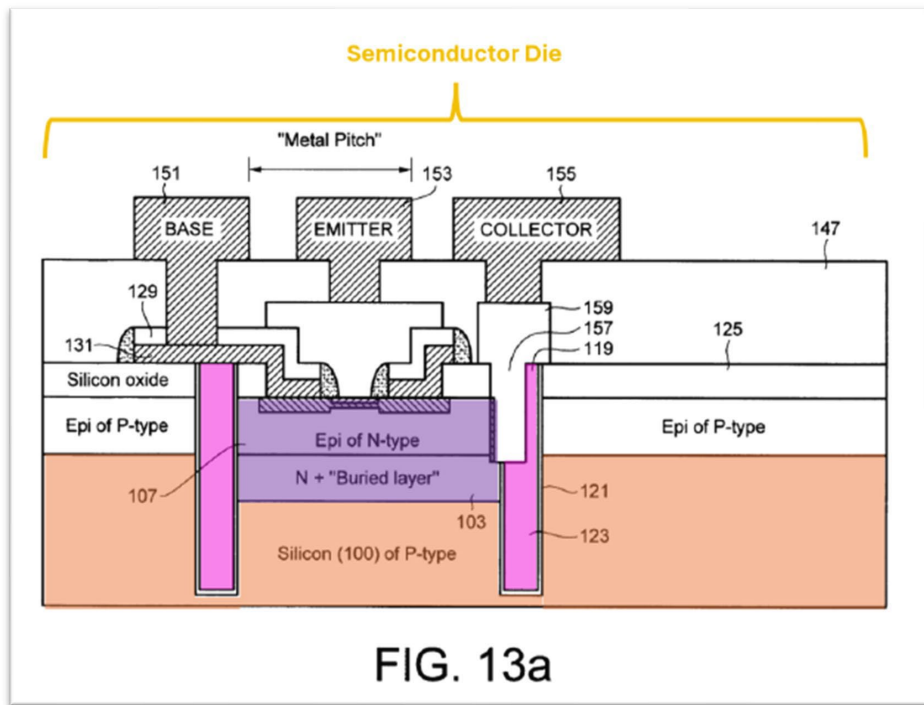
1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Ex. 1001, cl. 1

Ground 2: Norström



Pet., 62

N-type over the surrounding P-regions 109. Thereupon openings to isolating trenches 119 are lithographically defined to be made from the confining oxide regions 125, see FIG. 4. Then oxide material in the outer confining regions

Ex. 1006, 7:38-40

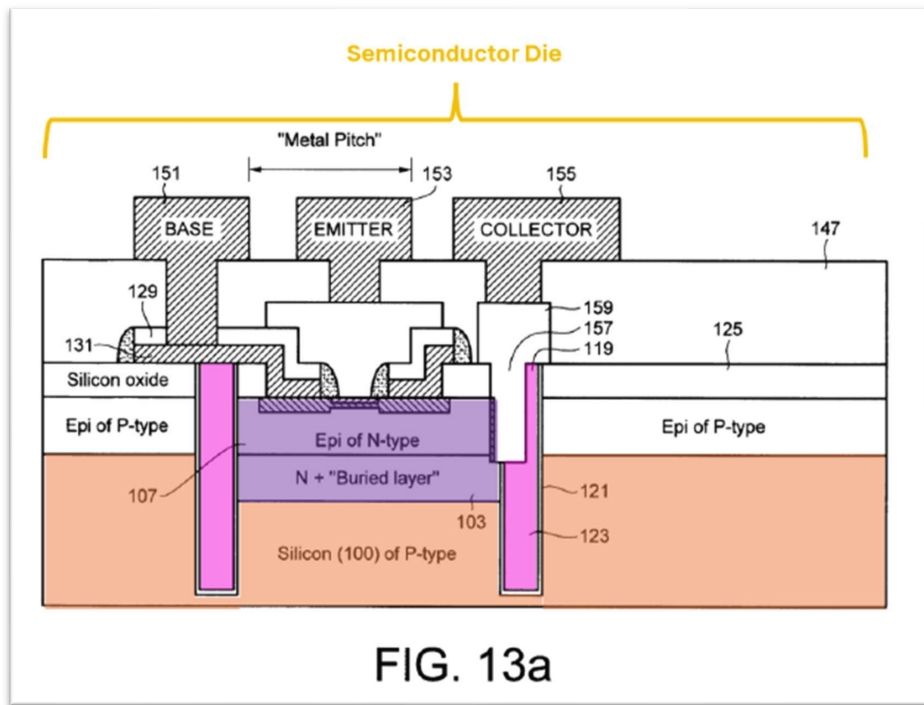
Then openings, in which isolating trenches 119 will be formed, are lithographically defined, see FIG. 9, these openings being arranged at the edges of the epitaxial layer

Ex. 1006, 9:31-35

oxide layer 125, which is placed over the epitaxial N-region 107. The opening of the trench 119 at this side is thus free from these layers 129, 131.

Ex. 1006, 10:14-15

Ground 2: Norström



Pet., 62

20 Q. Turning back to figure 13 (a),
21 what is element 157?

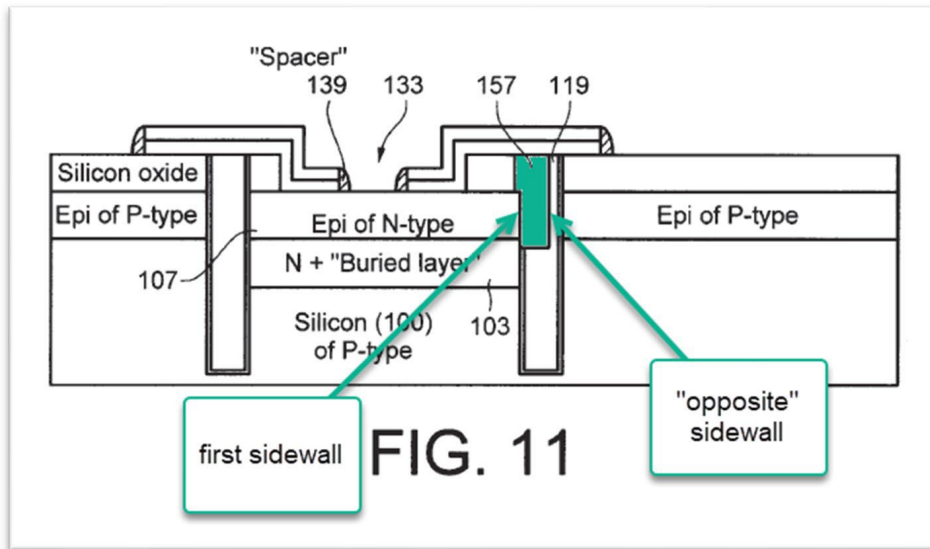
22 A. 157 is a collector contact
23 pole.

24 Q. And then what is 119?

25 A. 119 are isolating trenches.

Ex. 2010, Thompson Dep, 22:20-25

Ground 2: Norström



required. The resulting hole 157 will then, is apparent from FIG. 11, have one of its sidewalls in direct contact with the N-doped epitaxial layer 107 and the bottom diffusion 103 and have its opposite sidewall located against the inner material in the trench. The hole 157 will hereby be "self-aligned" with the sidewall of the trench. Also, the other two

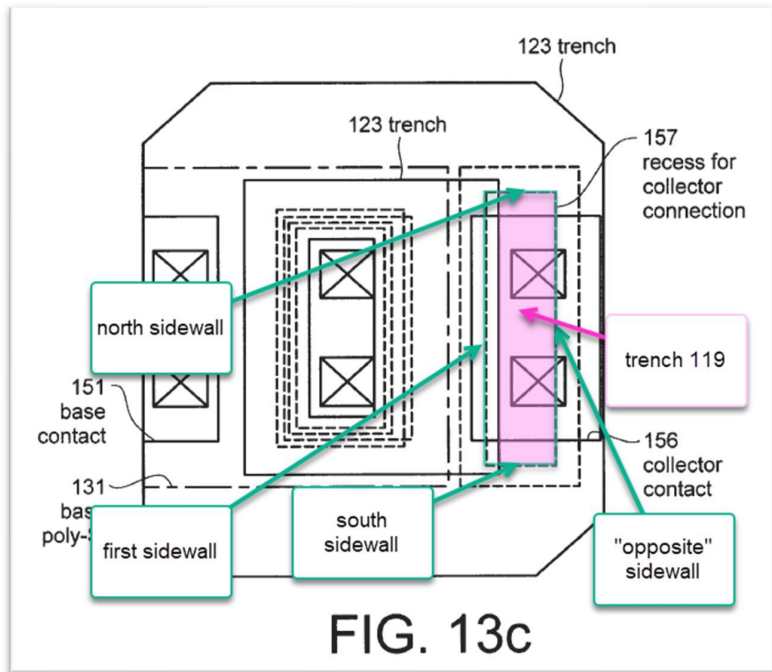
Ex. 1006, 10:48-53

aligned" with the sidewall of the trench. Also, the other two sidewalls will in the normal case be located against the inner material of the trench 119, see also the plan view of FIG. 13c.

Ex. 1006, 10:53-56

POR., 27

Ground 2: Norström

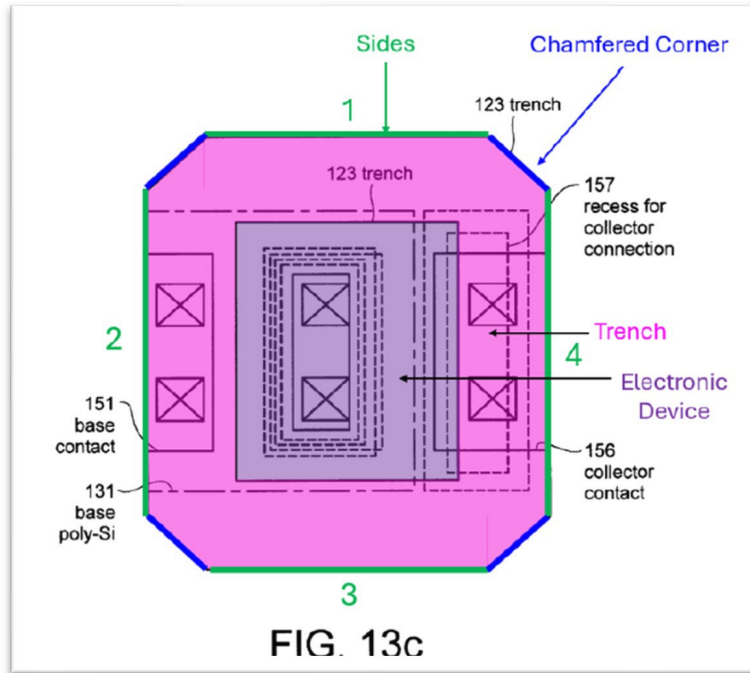


POR., 28

required. The resulting hole 157 will then, is apparent from FIG. 11, have one of its sidewalls in direct contact with the N-doped epitaxial layer 107 and the bottom diffusion 103 and have its opposite sidewall located against the inner material in the trench. The hole 157 will hereby be "self-aligned" with the sidewall of the trench. Also, the other two sidewalls will in the normal case be located against the inner material of the trench 119, see also the plan view of FIG. 13c.

Ex. 1006, 10:48-56

Ground 2: *Norström*

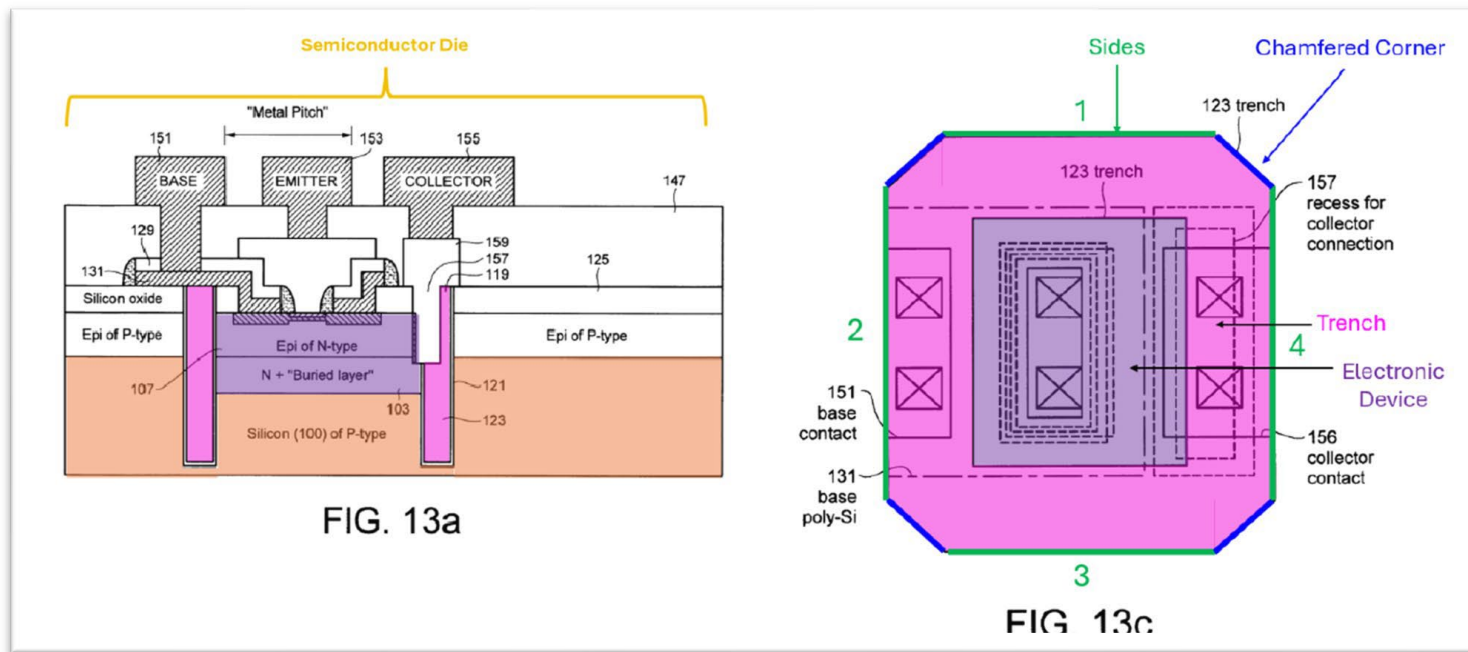


bevelled to an angle of about 45° . Also, the outer sidewalls of the trench 123 shown in FIG. 13c have no right angles, but the flat sidewall segments form an angle of 135° to each other.

Ex. 1006, 16:39-42

Pet., 61

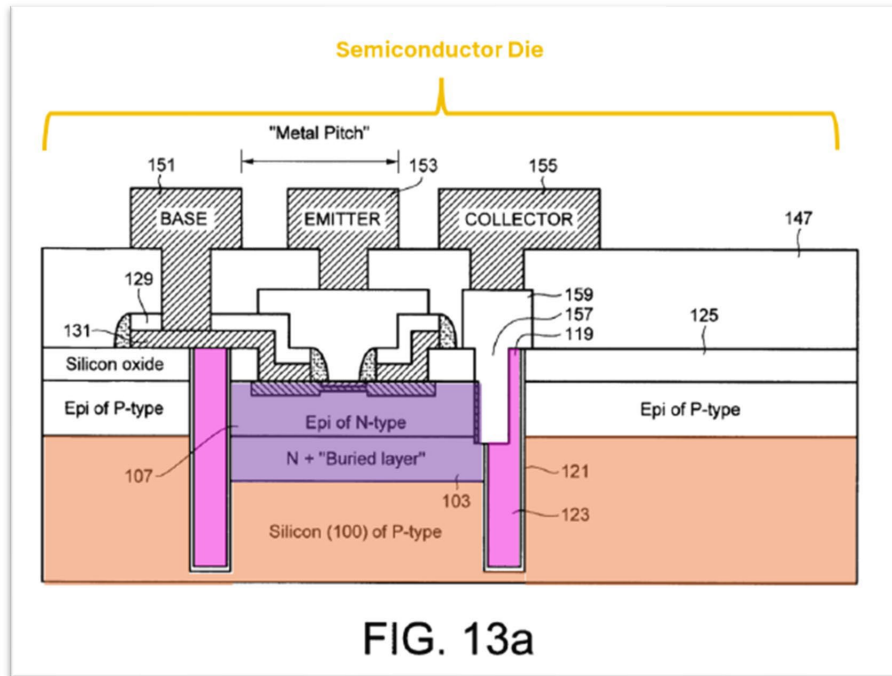
Ground 2: *Norström*



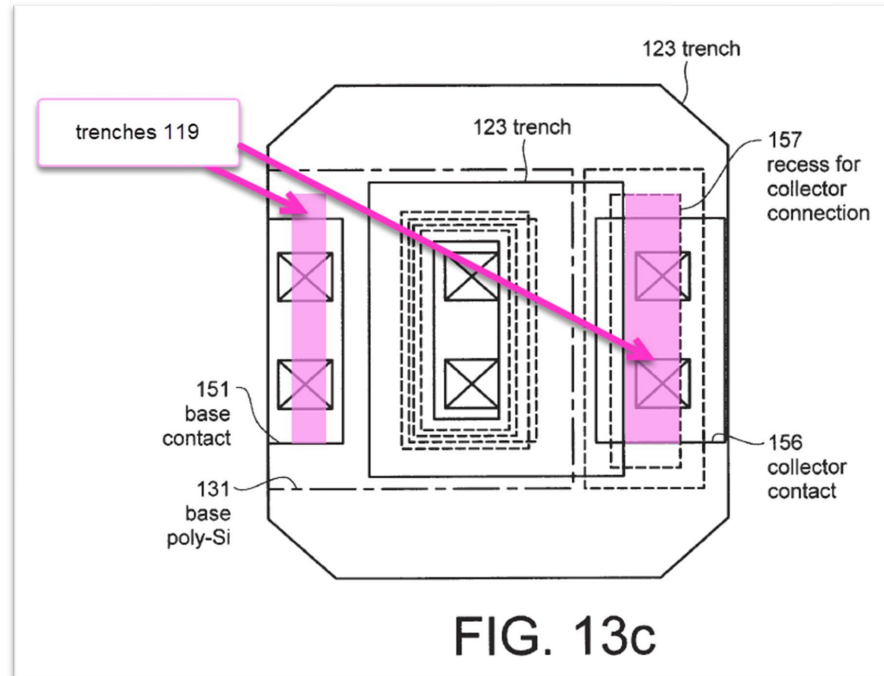
Pet., 61-62

POR, 28-33

Ground 2: *Norström*



Pet., 62



POR, 31

Ground 3: *Norström*

C. Ground 3: Claims 7 and 15 Would Have Been Obvious Over *Norström*

1. Claim 7

- a. “The semiconductor die of claim 1, wherein said semiconductor die is enclosed in a semiconductor package.”

To the extent HID contends that *Norström* does not disclose the additional

Pet., 71