

Petitioner's Demonstratives

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.,
Petitioner,

v.

Harbor Island Dynamic, LLC,
Patent Owner.

IPR2024-01403 – U.S. Patent No. 7,772,673

Grounds Presented

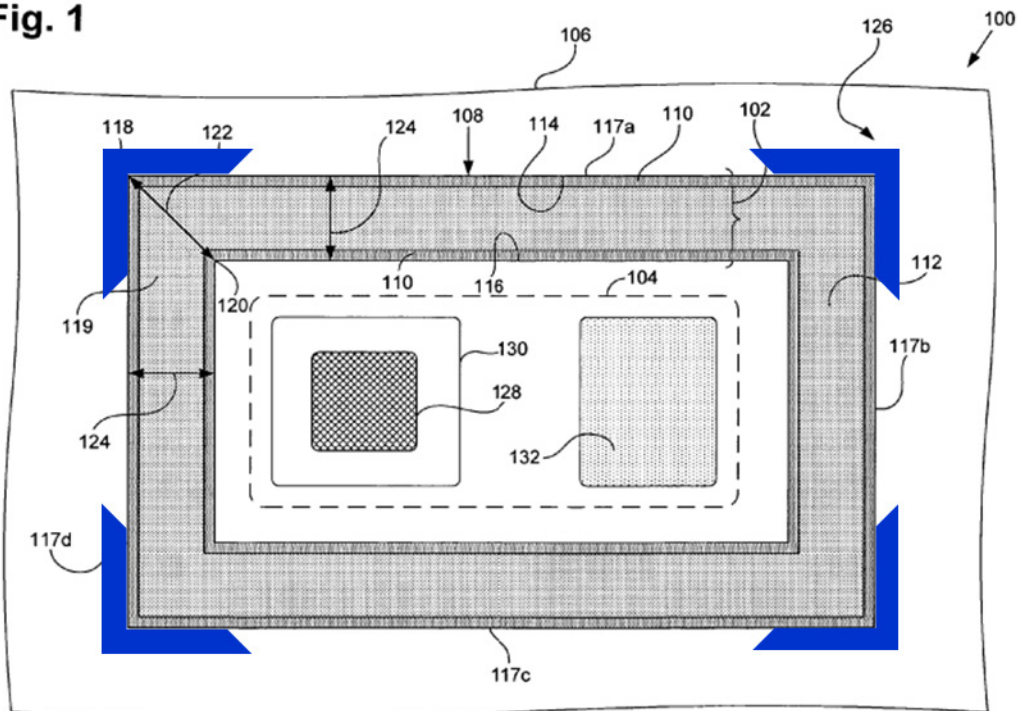
Claim(s) Challenged	35 U.S.C. § ²	References/Basis
1–17	103(a)	Yin, ³ Koshimizu ⁴
1, 3, 5, 7–8, 10, 12, 14–16	102	Norström ⁵
7, 15	103(a)	Norström

(Institution Decision at 8-9)

The '673 Patent's Alleged Invention: Chamfered Corners

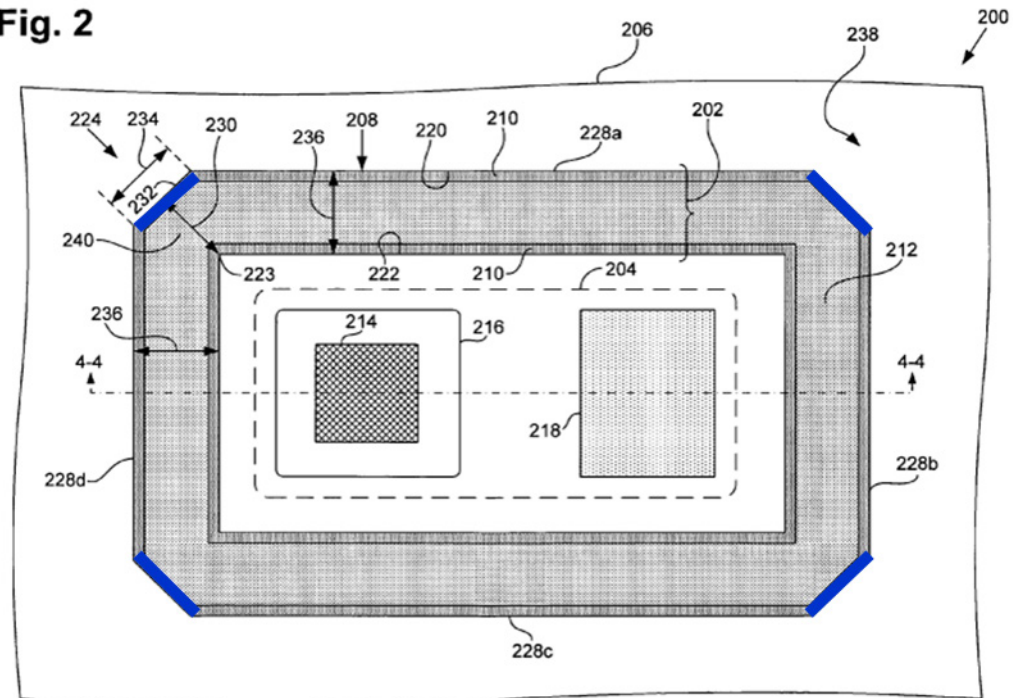
Admitted Prior Art – Semiconductor Devices with Deep Isolation Trenches

Fig. 1

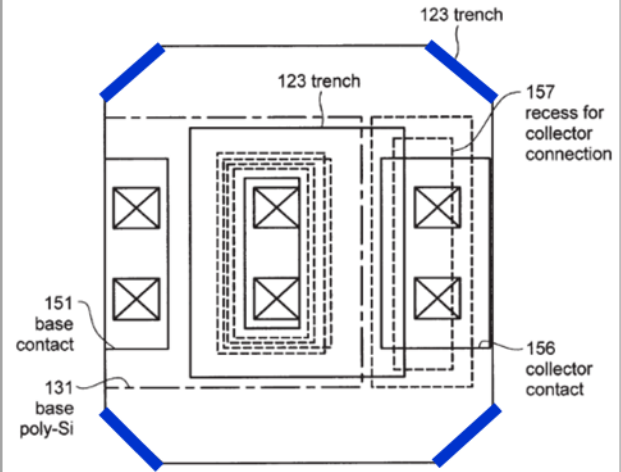
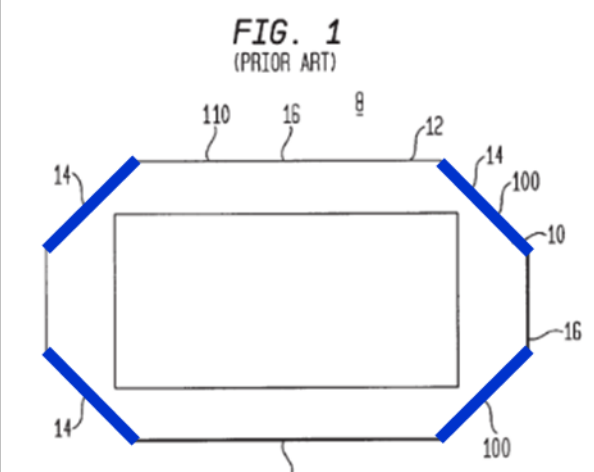
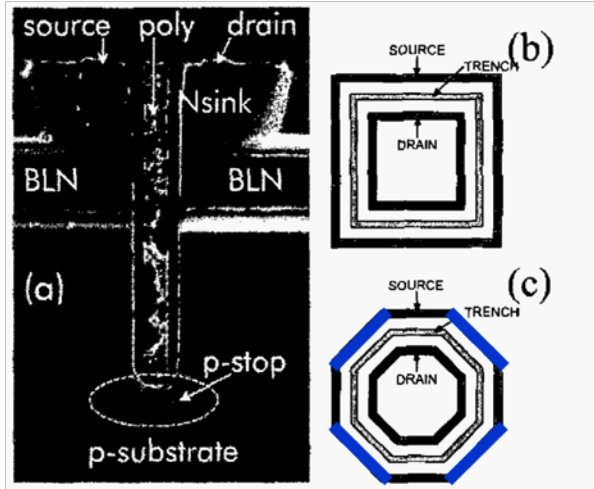
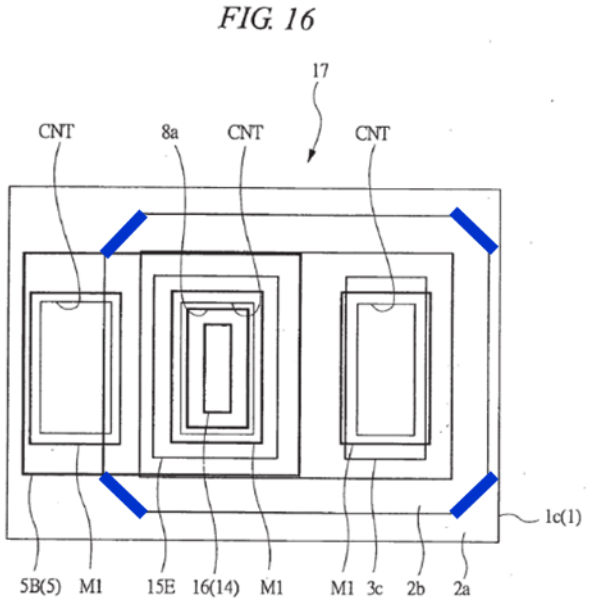


Alleged Invention – Chamfered Corners

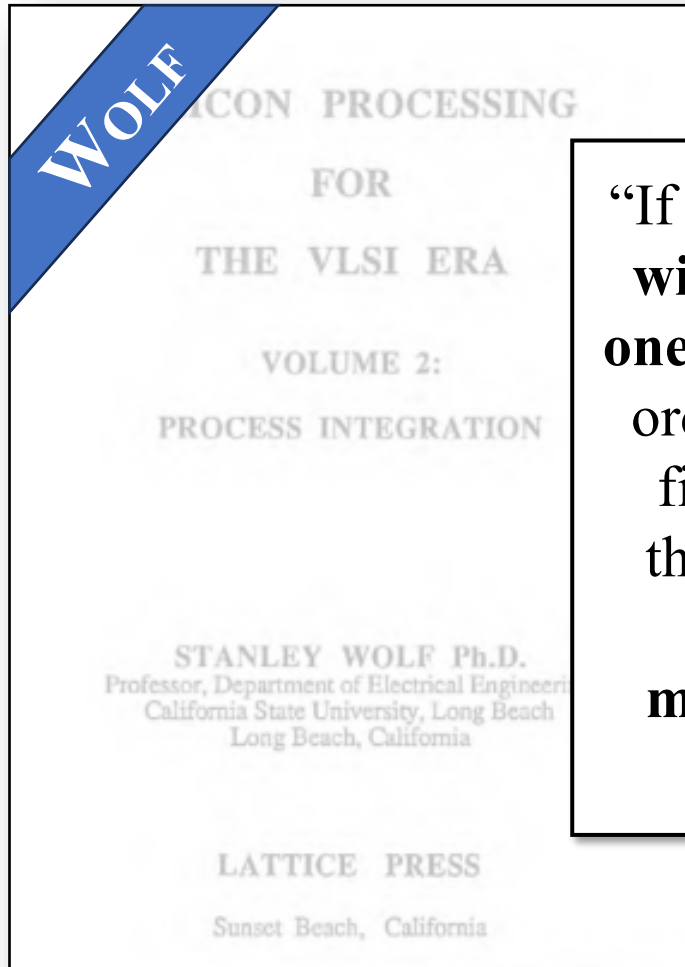
Fig. 2



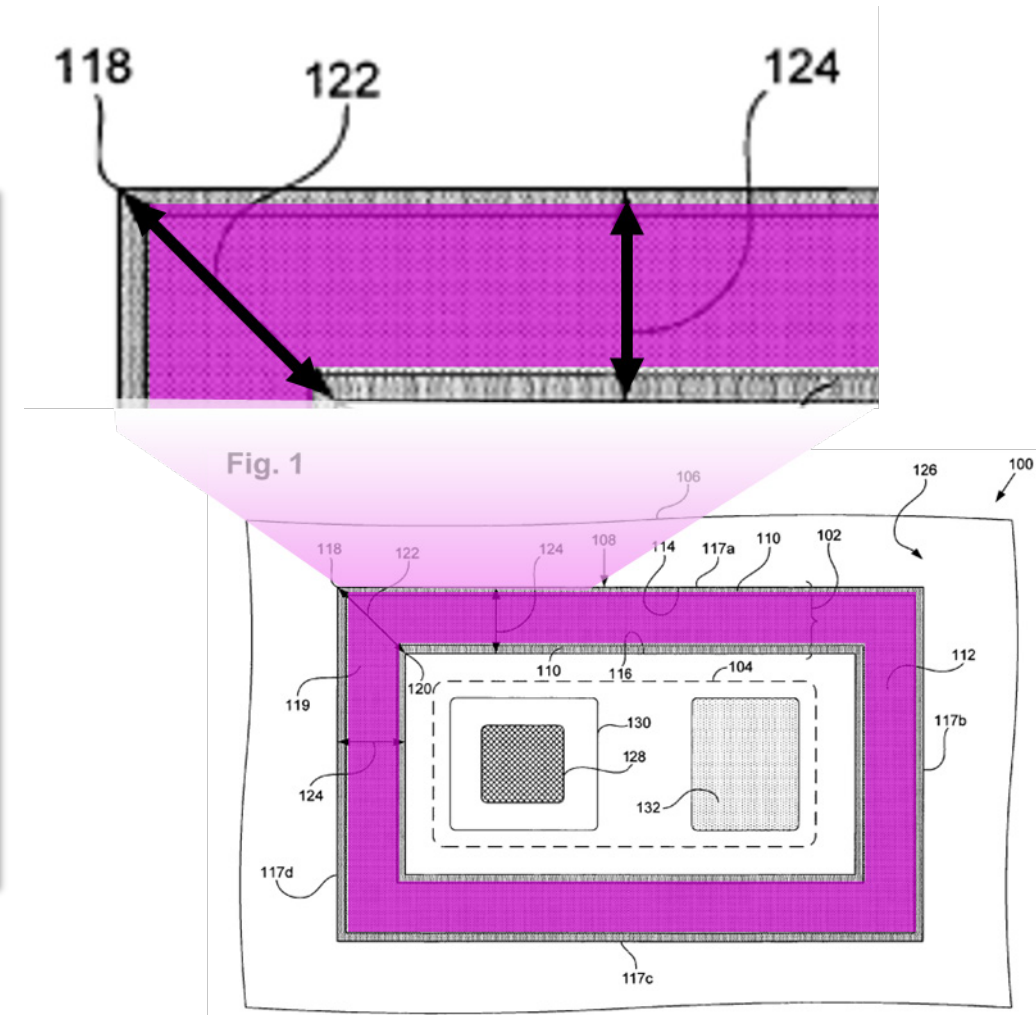
Chamfered Corners Were Well-Known In The Art

Norström (2000) (Grounds 2 and 3)	Tews (2002)	Moens (2005)	Koshimizu (2005) (Ground 1)
 FIG. 13c	 FIG. 1 (PRIOR ART)	 FIGURE 1. : (A) CROSS SECTION OF THE DEEP TRENCH ISOLATION STRUCTURE. (B) : TEST STRUCTURE WITH STRAIGHT CORNERS, (C) TEST STRUCTURE WITH 45° CUT CORNERS (NOT TO SCALE)	 FIG. 16

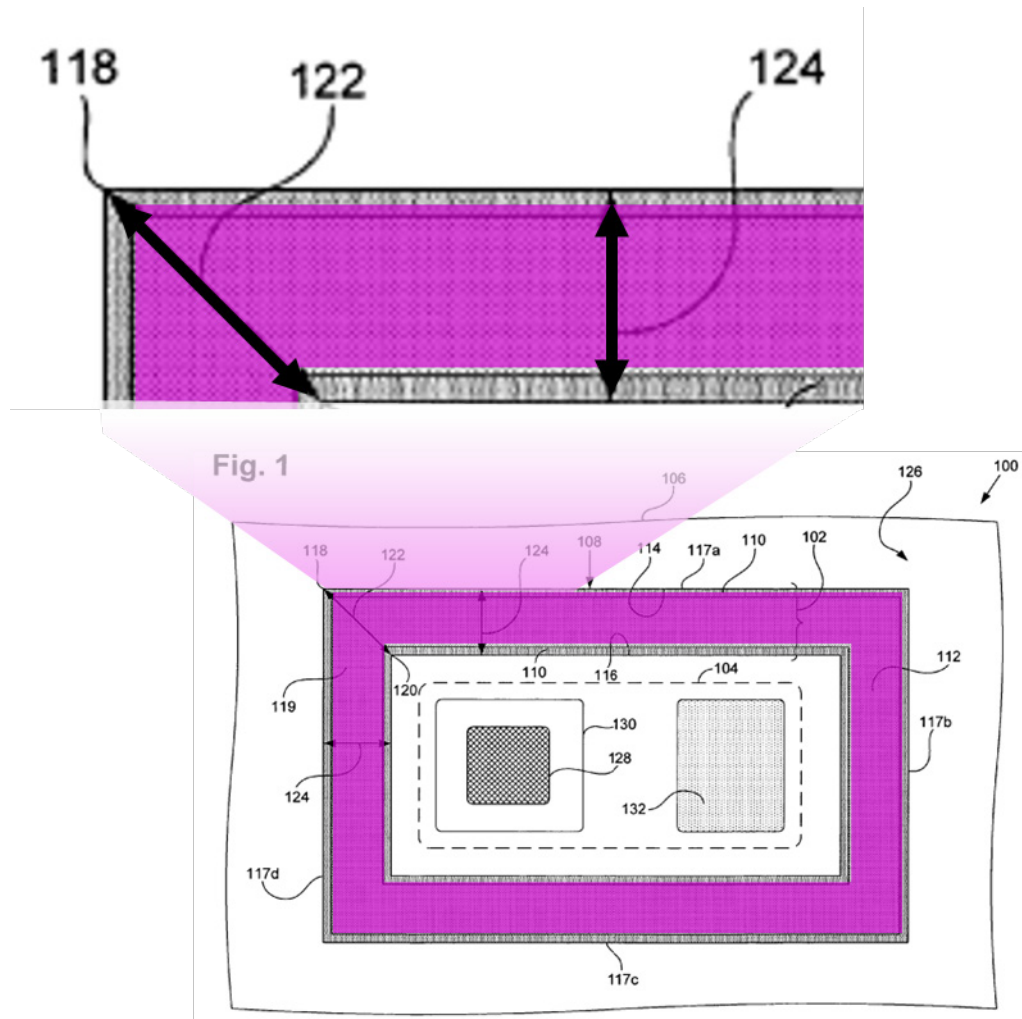
The Problem Faced By The '673 patent Was Well-Known In The Prior Art



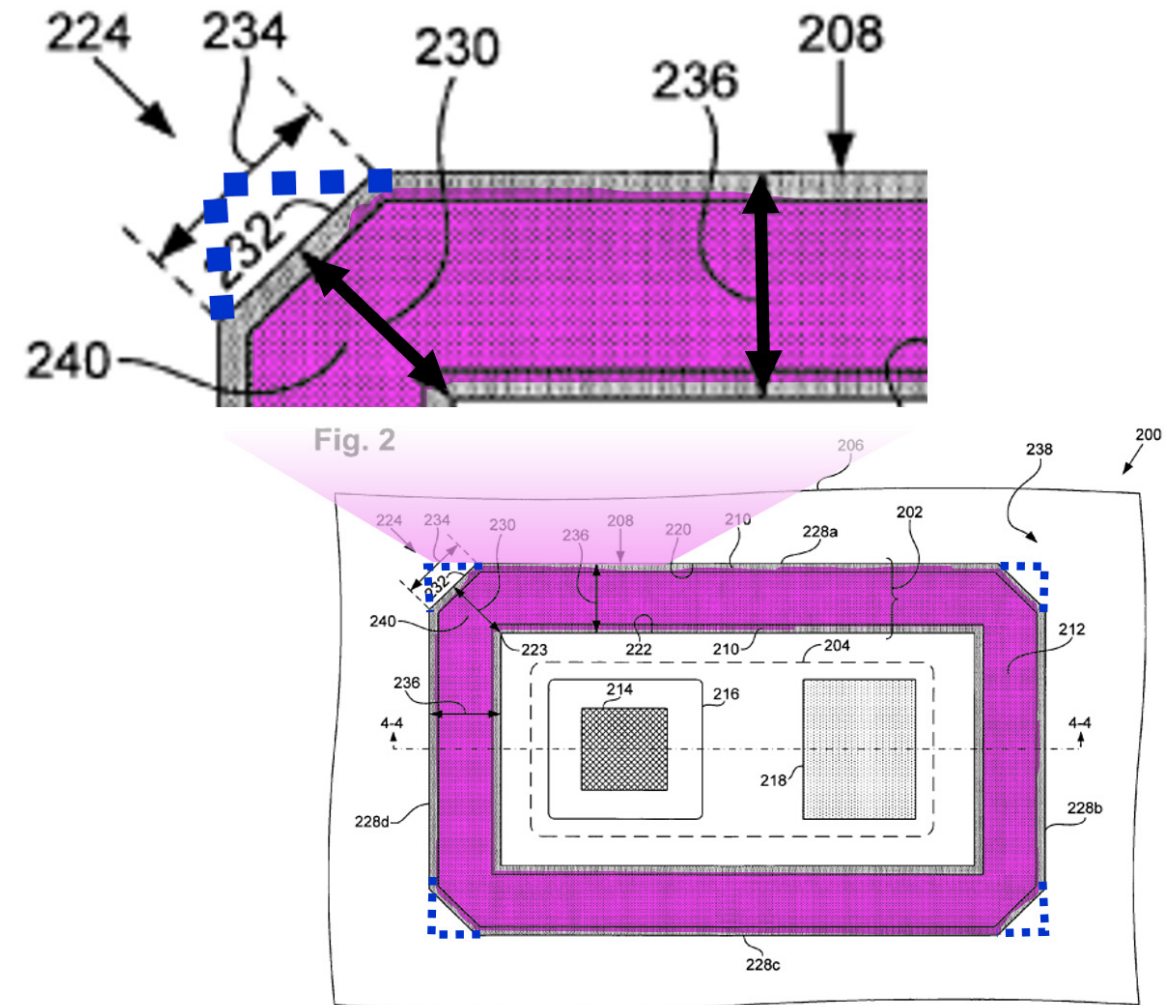
“If trenches of widely varying widths are filled, the narrow ones must be well overfilled in order for the wider ones to be filled completely. Thus, the thickness of the top-surface-deposited film will vary, making planarization very difficult.” WOLF, 56.



WOLF Encourages Chamfered Trenches – Trenches Without Varying Widths

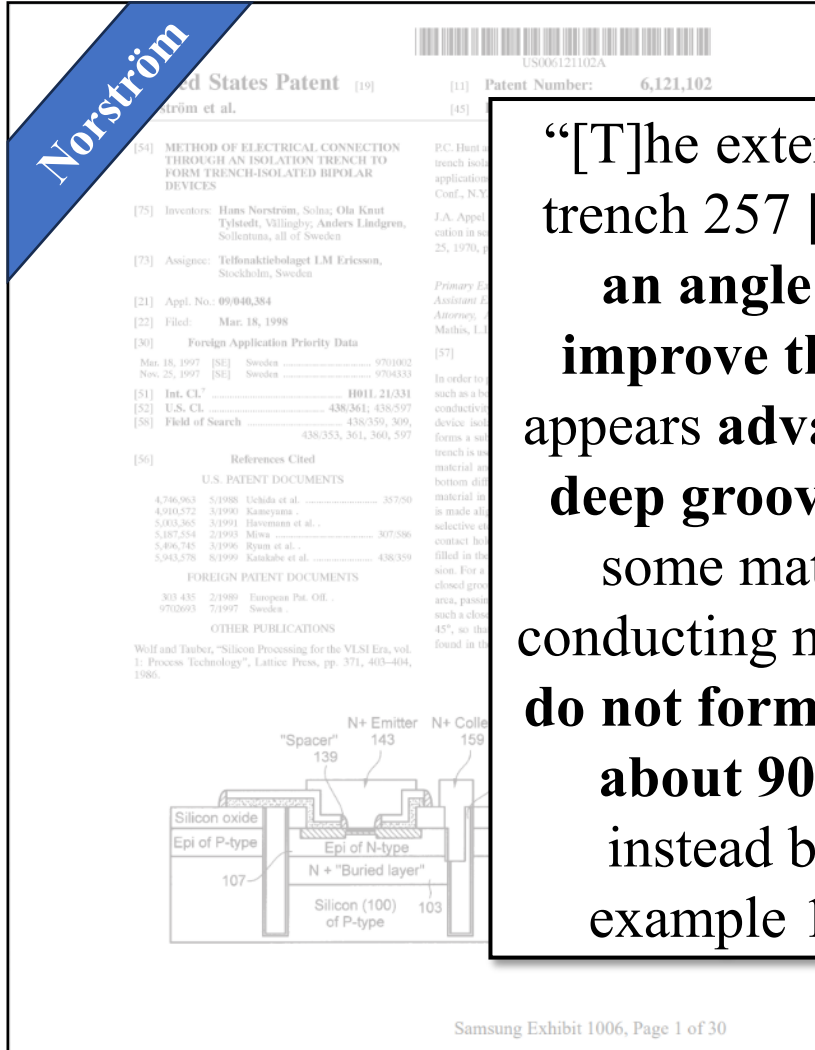


Prior Art



Alleged Invention

Norström Encourages Chamfered Corners To Improve Filling



“[T]he exterior **corners** of the isolating trench 257 [] has been made oblique by **an angle of about 45° in order to improve the refilling** of the trench. It appears **advantageous to always form a deep groove**, which is to be filled with some material, such as isolating or conducting material, to have walls, which **do not form comers [sic] having angles about 90°**, but these angles should instead be as large as possible, for example 135°. *Norström*, 16:28-36.

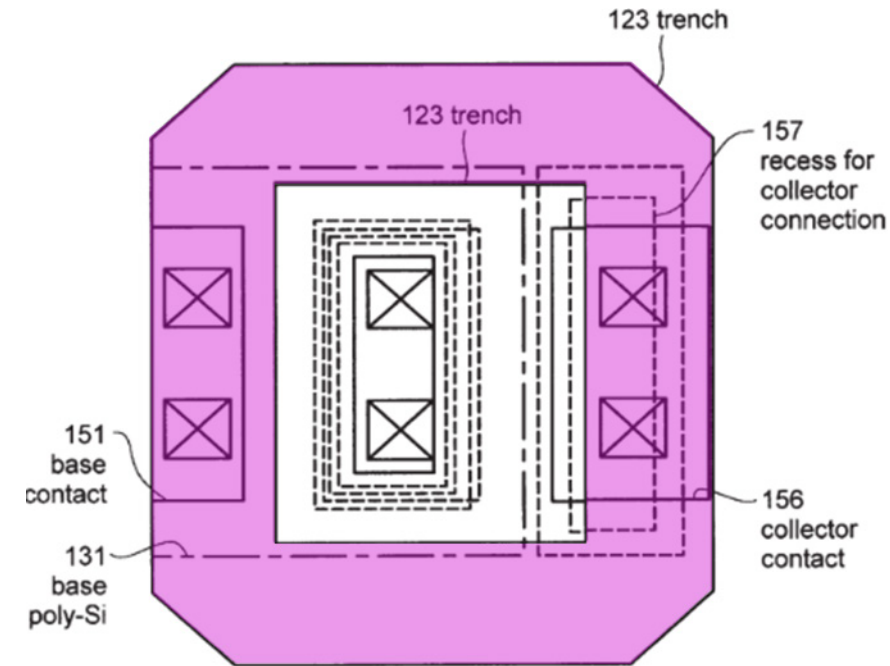


FIG. 13c

Claim 1 – Semiconductor Die

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

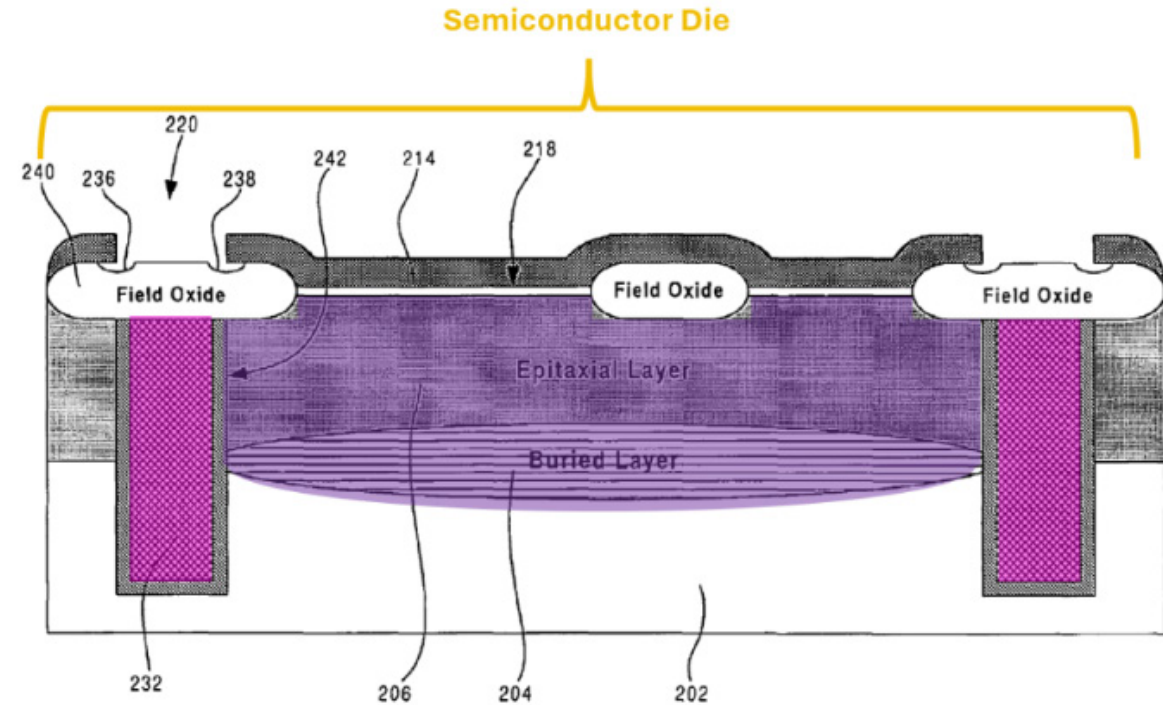


Fig. 4E

Claim 1 – Deep Isolation Trench

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

“[D]eep trench isolation region **442**, [] corresponds to deep trench isolation region **208** in FIG. 2” ’673 Patent, 8:60-62.

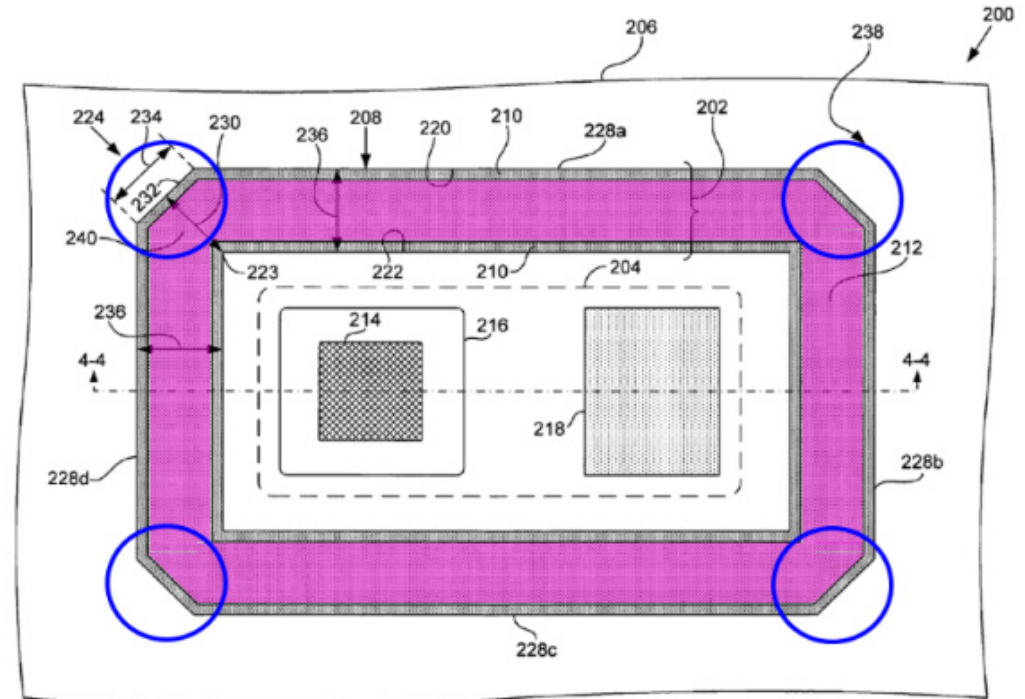


Fig. 2

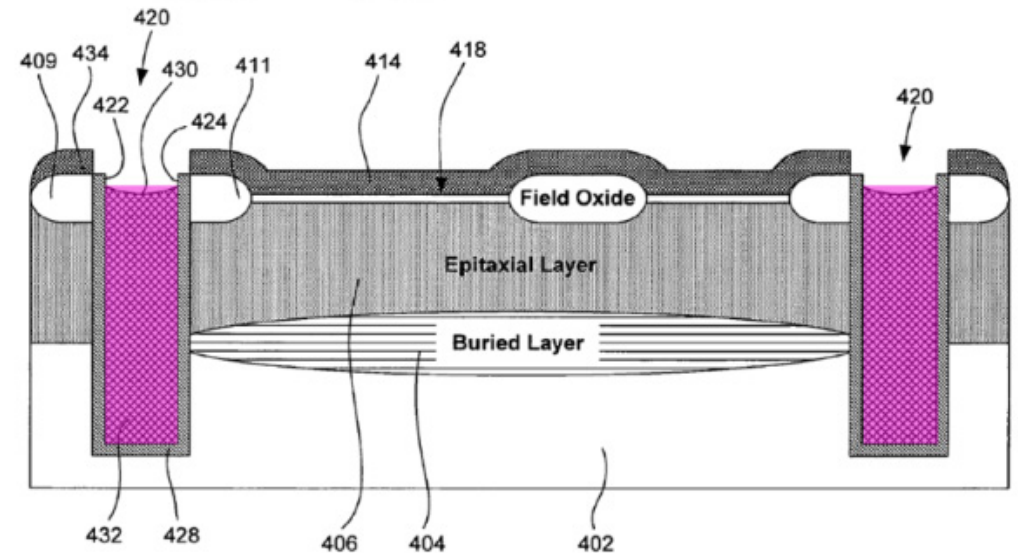


Fig. 4E

Claim 1 – Electronic Device

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

“[A] bipolar device is utilized as an example of an electronic device” ’673 Patent, 2:35-36.

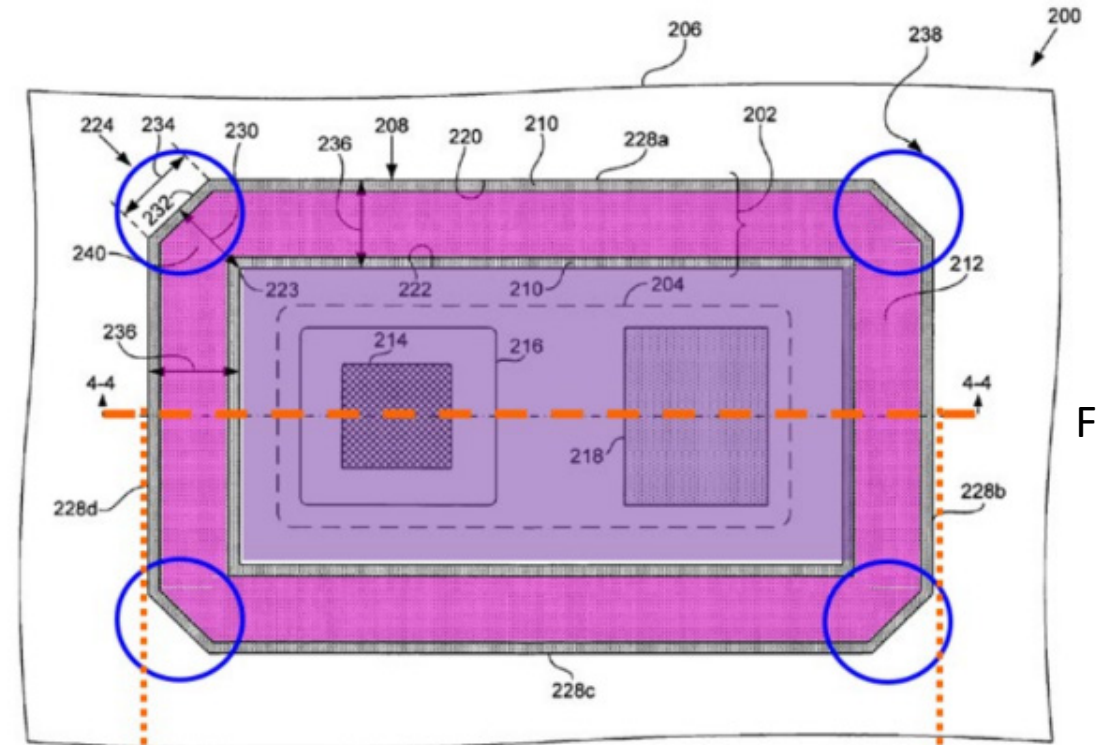


Fig. 2

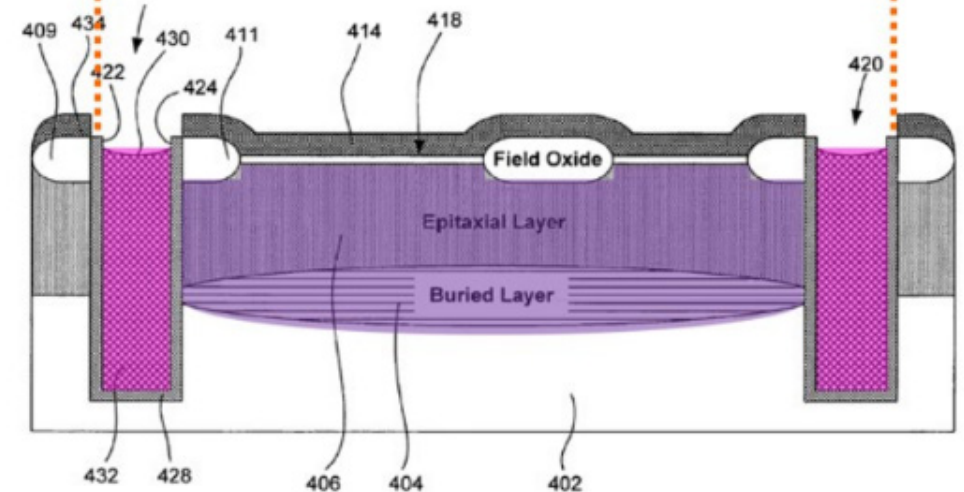


Fig. 4E

Claim 1 – Chamfered Corner(s)

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

“[T]rench chamfered corners [] reduce the trench corner width . . . [and] advantageously reduce[] the deposited polysilicon layer thickness” ’673 Patent, 5:15-20.

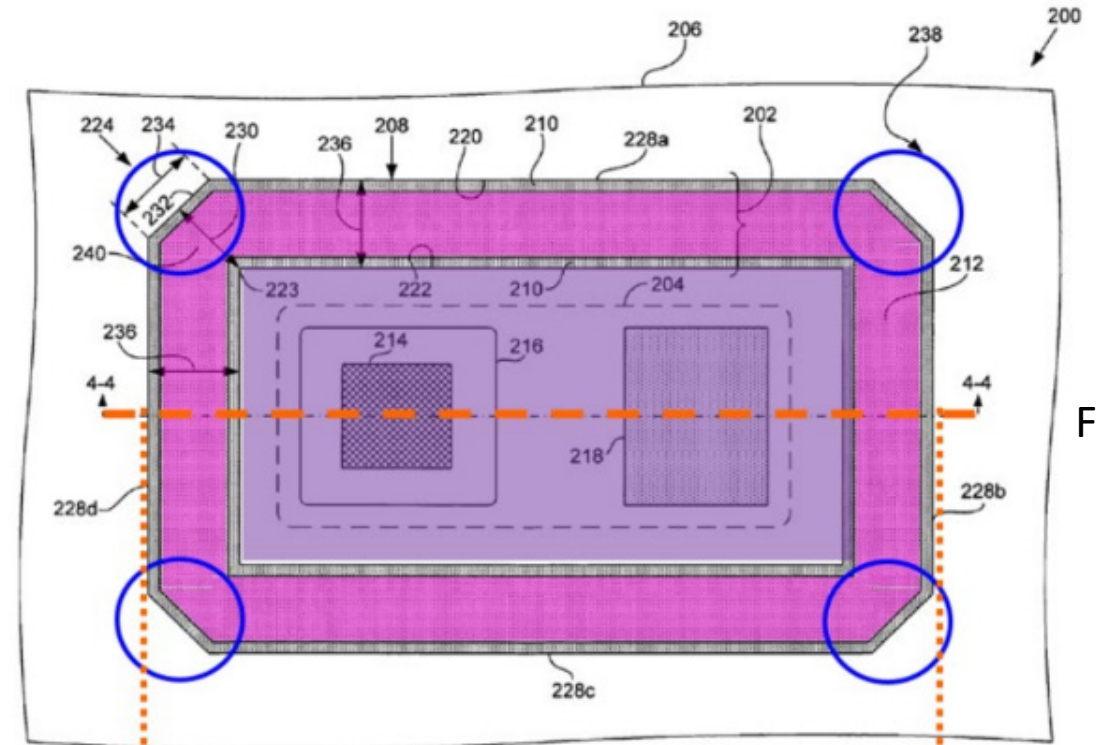


Fig. 2

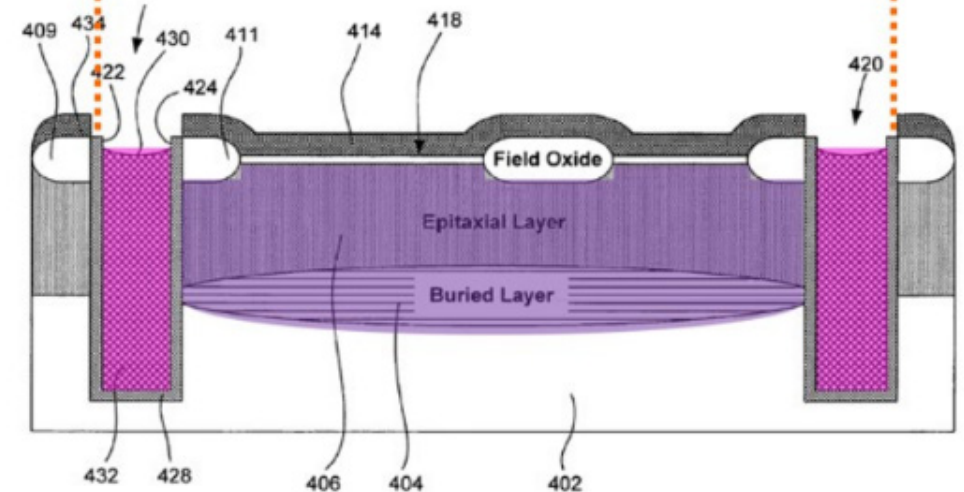


Fig. 4E

Overview of Claim 1

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

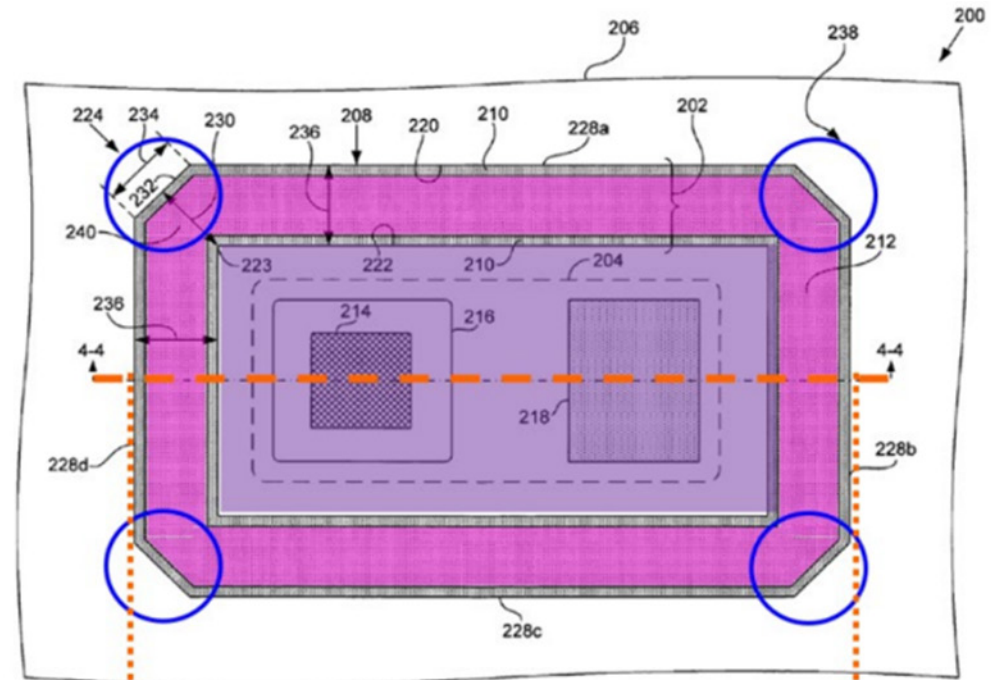


Fig. 2

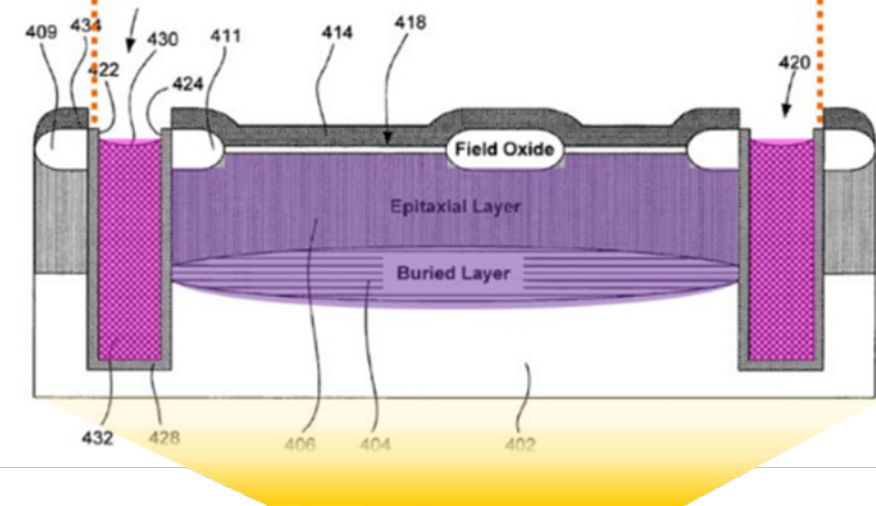


Fig. 4E

Semiconductor Die

Overview of The '673 Patent

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

- a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

10. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

- at least one trench situated in a substrate of said semiconductor die, said at least one trench having four sides surrounding said electronic device, wherein a respective one of four trench chamfered corners connects each pair of said four sides;

each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.

Overview of The '673 Patent

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

- a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

10. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

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each of said four trench chamfered corners causing a reduction in a thickness of a polysilicon layer within said at least one trench.

Limited Issues: What HID Does Not Dispute

✓ Chamfered isolation trenches for bipolar devices were known in the art.

✓ Ground 1:

- *Yin* and *Koshimizu* teach every element of every challenged claim.
- A POSITA would have been motivated to combine *Yin* and *Koshimizu* and would have had a reasonable chance of success in doing so.

✓ Grounds 2, 3:

- Other than claim 1's isolation trench, *Norström* teaches every element of every challenged claim.

Issues in Dispute

Ground 1

- ☐ Is *Koshimizu* analogous art?

Grounds 2, 3

- ☐ Does *Norström* disclose a trench that is both “situated in a substrate” and has “at least one trench chamfered corner”?

Ground 1: *Yin* in View of *Koshimizu*

HID Does Not Dispute *Yin* and *Koshimizu* teach every element of every challenged claim.



1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:



a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;



wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Koshimizu Is Analogous Art

Koshimizu Is Analogous Art

- Prior art is analogous if it is:
 - (1) from the same field of endeavor, or
 - (2) reasonably pertinent to the problem addressed by the patent.



In re Oetiker, 977 F.2d 1443, 1447 (Fed. Cir. 1992)

The Board Recognizes The Scope of Analogous Art Must Be Construed Broadly

Trials@uspto.gov
571-272-7822

Paper 9
Entered: March 24, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG
ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01403
Patent 7,772,673 B2

Before WILLIAM V. SAINDON, GREGGI. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

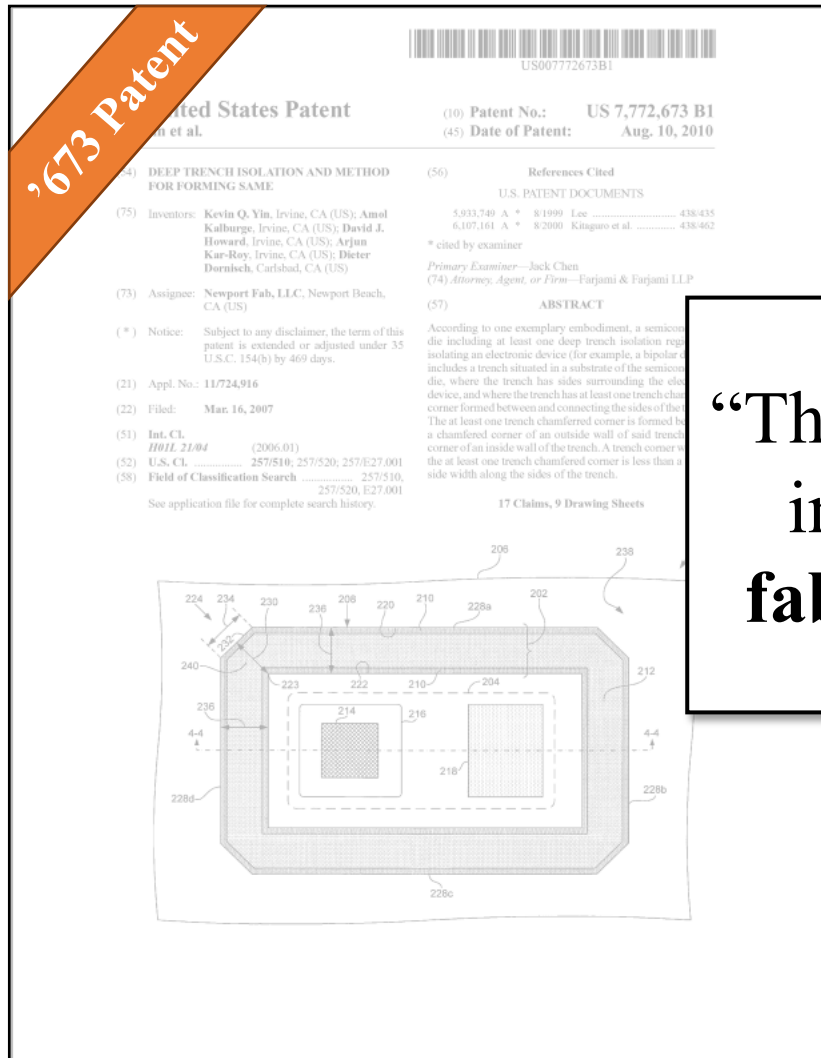
DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314



“[T]he Federal Circuit [has] directed that the scope of analogous art is to be construed broadly.” Inst. Dec., 26

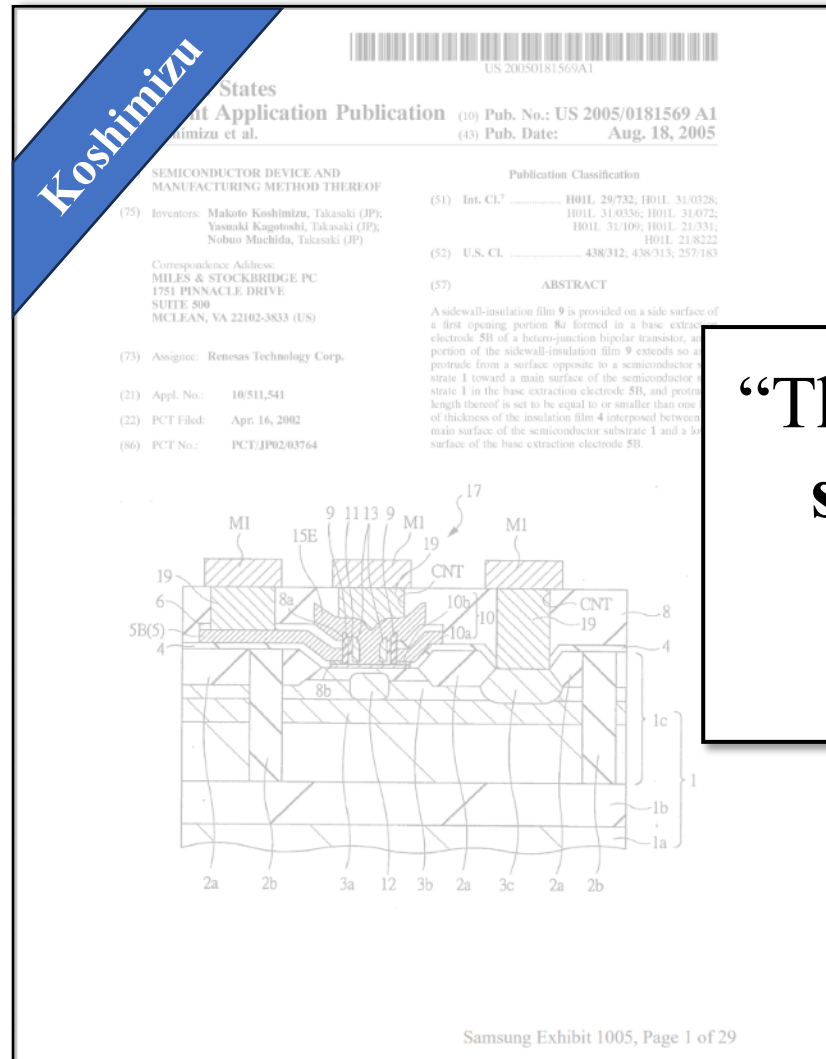
Koshimizu Is from the Same Field of Endeavor as the '673 Patent:
Semiconductor Devices with a Deep Trench for Isolating a Bipolar Device

The '673 Patent Describes Its Field Of Endeavor Broadly



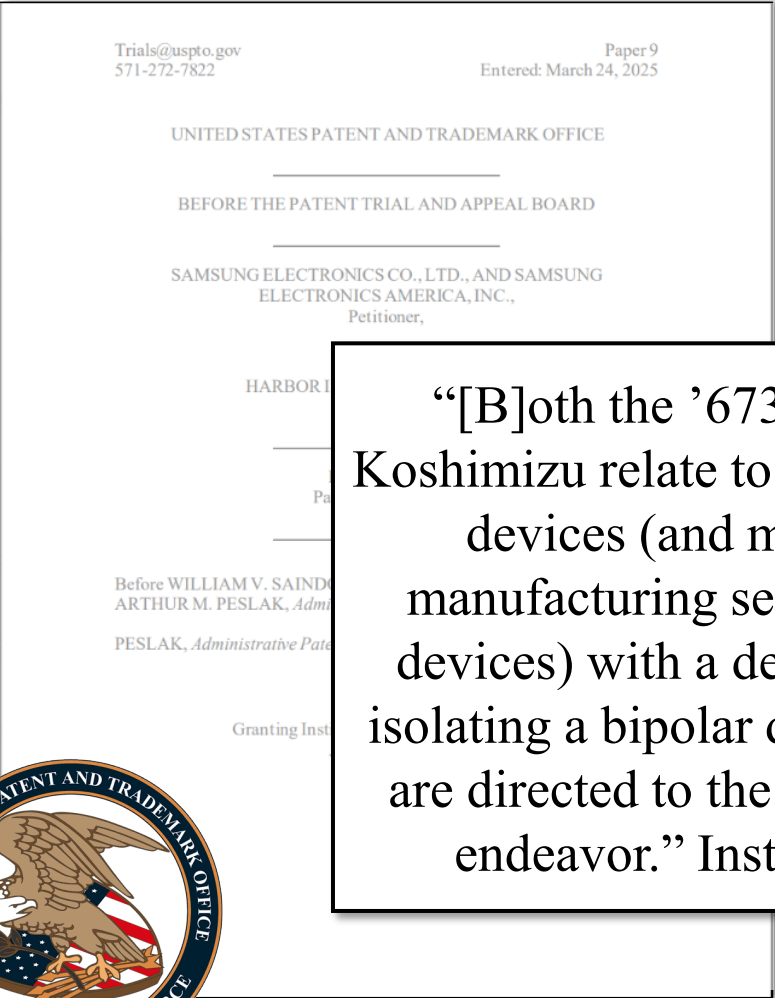
“The present invention is generally in the **field of semiconductor fabrication.**” '673 Patent, 1:7-8.

Koshimizu Describes The Same Field Of Endeavor As The '673 Patent

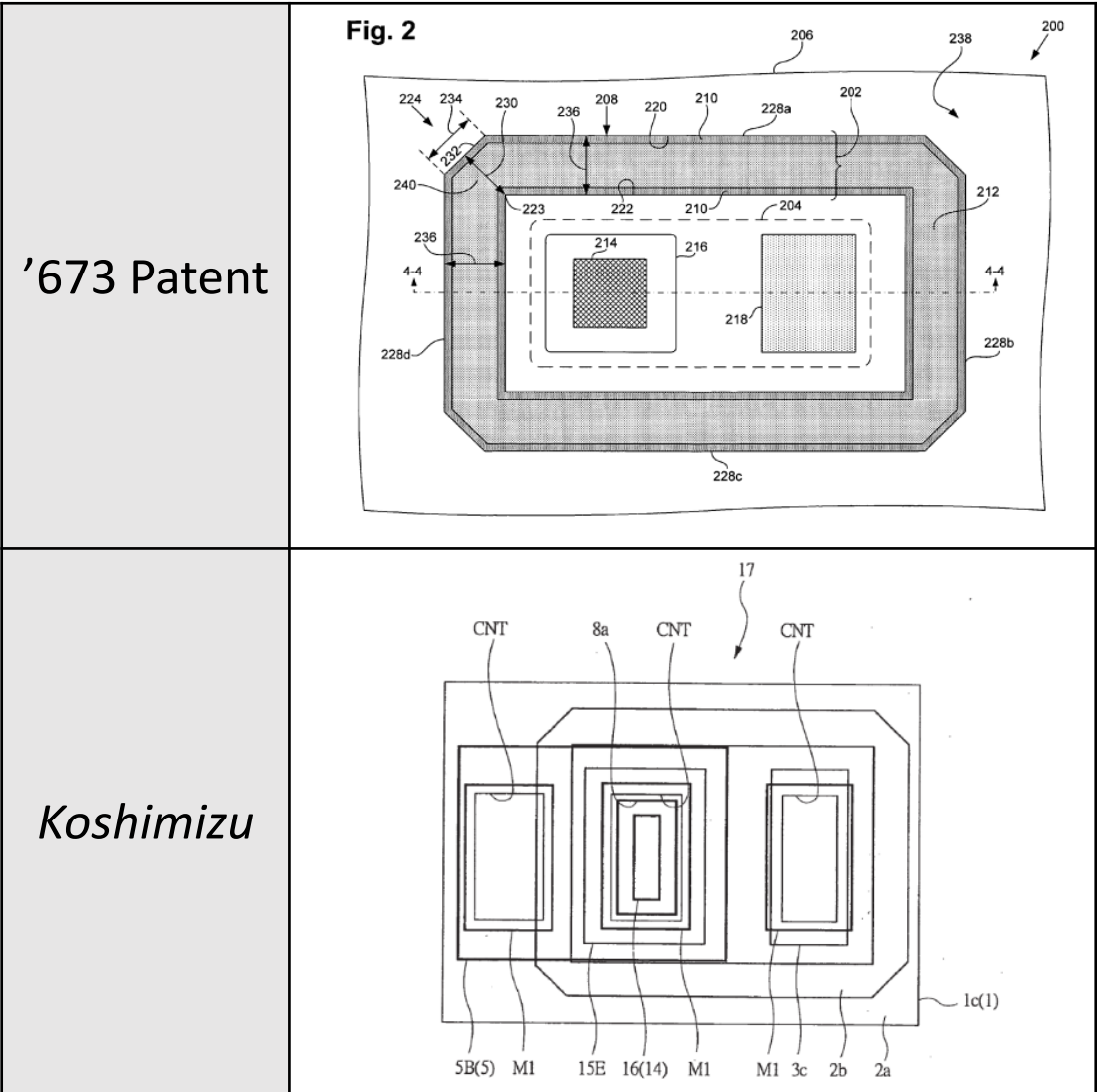


“The present invention relates to a semiconductor device and a manufacturing technique therefor” *Koshimizu*, [0001]

In Its Preliminary Findings, The Board Found that *Koshimizu* Qualifies as Analogous Art



“[B]oth the '673 patent and *Koshimizu* relate to semiconductor devices (and methods of manufacturing semiconductor devices) with a deep trench for isolating a bipolar device... [and] are directed to the same field of endeavor.” Inst. Dec., 27.



HID Does Not Rebut The Board's Findings

HID's Sur-Reply

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIEBUNAL

SAMSUNG ELECTRONICS CO., LTD.

SAMSUNG ELECTRONICS CO., LTD.

Patent No. 7,411,111

HARBOR ISLAND, VIRGINIA

Patent No. 7,411,111

Patent Filing Date: 08/01/2007

Issue Date: 07/10/2007

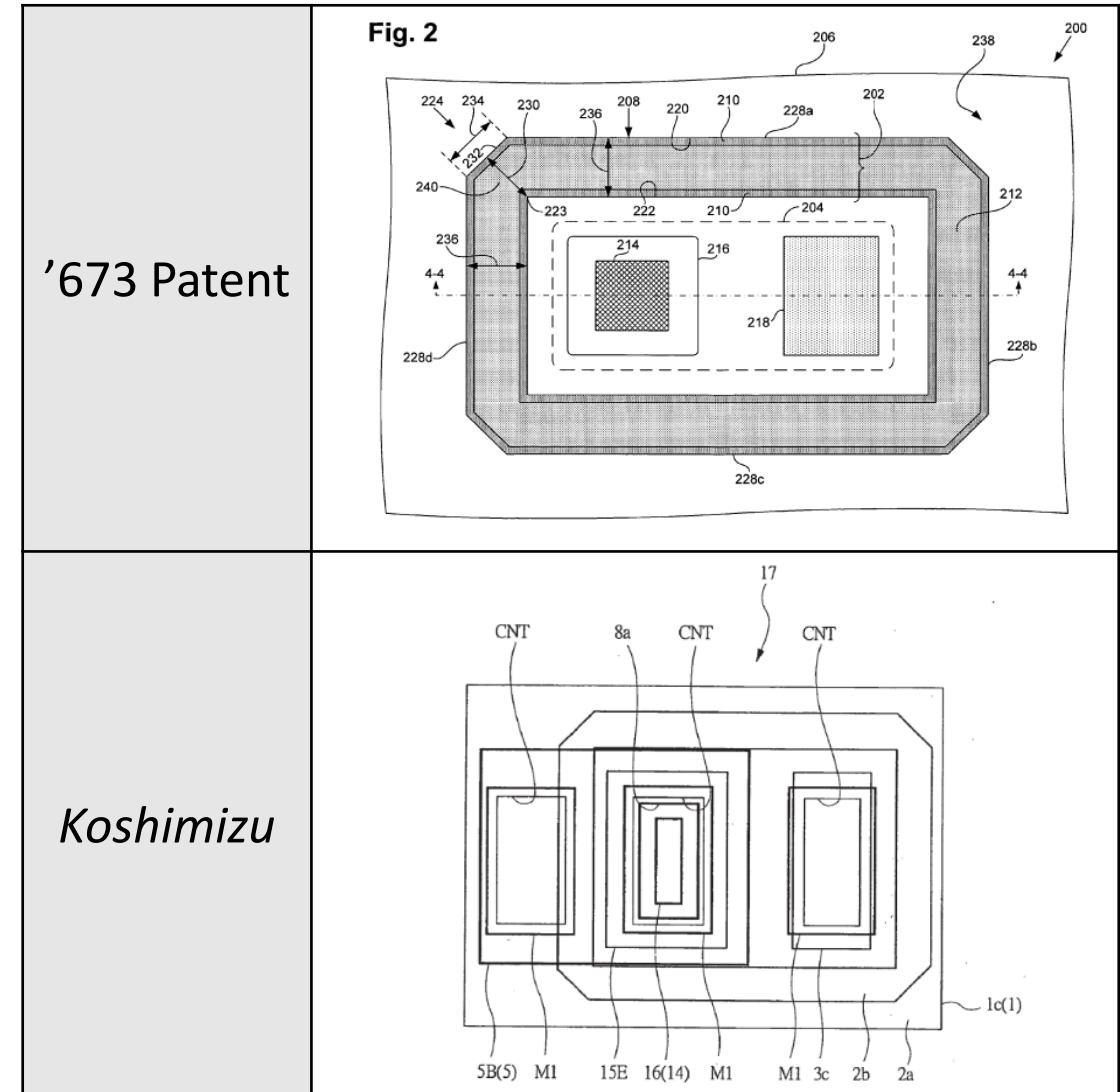
Inventors: Kevin Q. Yin, Arjun Kar-Roy

Title: DEEP TRENCH ISOLATION

PATENT OWNER: SAMSUNG ELECTRONICS CO., LTD.

Case No. 2007-00111

“The Board preliminarily found that ‘both the ’673 patent and Koshimuzu relate to semiconductor devices (and methods of manufacturing semiconductor devices) with a deep trench for isolating a bipolar device.’ The Board, however, did [sic] explicitly set out a field of endeavor.” Sur-Reply, 2.



HID Argues Semantics

- “[O]ur precedent does not require the use of magic words” with respect to the “field of endeavor” doctrine.



Netflix, Inc. v. DivX, LLC, 80 F.4th 1352, 1358-60 (Fed. Cir. 2023)

Gesture Does Not Help HID

- “[T]he Board’s adopted field of endeavor is consistent with one proposed by [petitioner] itself, albeit for a different prior art reference.”



Apple Inc. v. Gesture Tech. Partners, LLC, No. 2023-1494, 2025 WL 1584286, at *15 n.5 (Fed. Cir. June 5, 2025)

HID’s Position

“Petitioner cites the same portion of the ’673 Patent with respect to all three prior art references, but arrives at different fields each time without explanation. This inconsistency alone shows that Petitioner fails to carry its burden.” POR, 18-19 (citing *Gesture*).

Koshimizu Fits Into the Petition’s Fields Of Endeavor

Yin	Norström	Koshimizu
Both Yin and the '673 Patent are “directed to a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor.” Pet., 8	Both Norström and the '673 Patent are directed to the manufacture of “bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” Pet., 14	Koshimizu and the '673 Patent are “directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors.” Pet., 11.

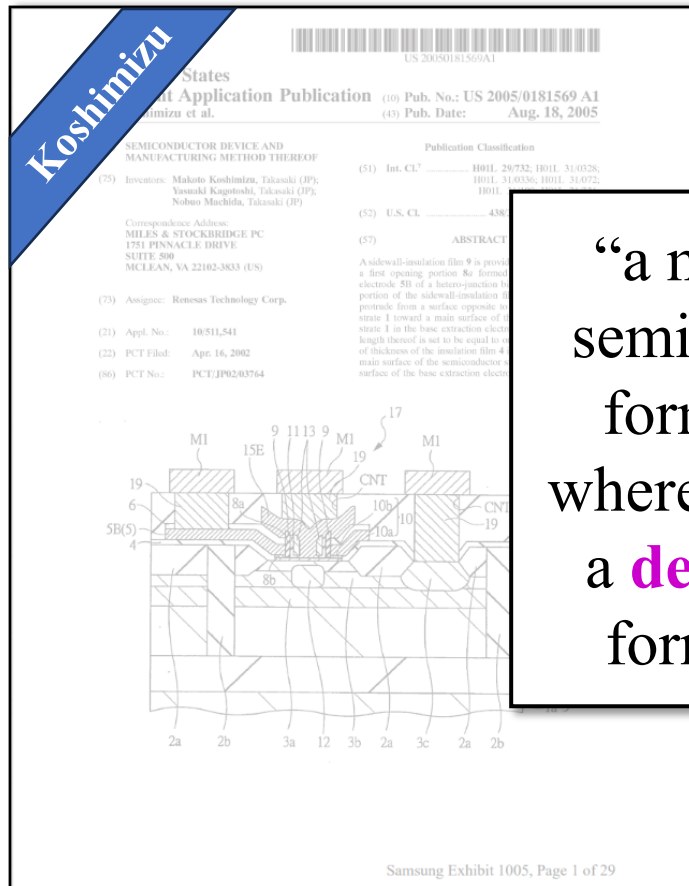
The ID’s preliminary field of endeavor is supported. Nevertheless, HID fails to explain why or how Koshimizu does not fit into any of the Petition’s fields of endeavor.

Pet., 8 (citing Thompson Dec., ¶ 69; Yin, Field of Invention; '673 Patent, Field of Invention); Pet., 14 (citing Thompson Dec., ¶ 77; Norström, 1:7-10; '673 Patent, Field of Invention)); Pet. 11 (citing Thompson Dec., ¶ 74 (citing Koshimizu, [0052]-[0053]; '673 Patent, Field of Invention); Sur-Reply, 7.

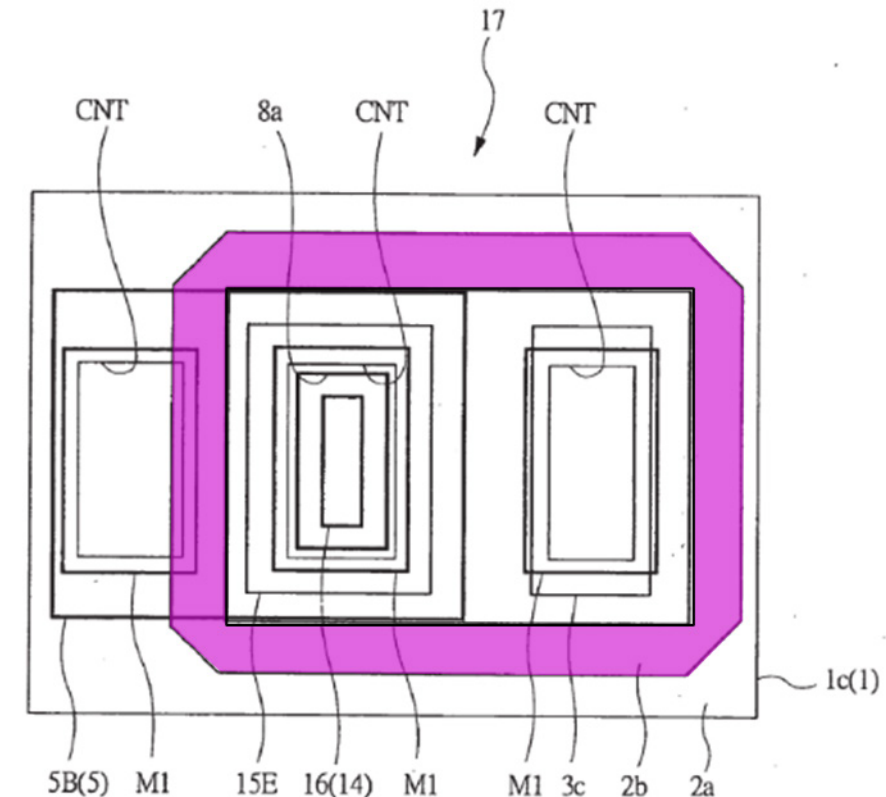
Koshimizu Is Analogous Art Even Under HID's Own Field Of Endeavor

HID's '673 Field of Endeavor

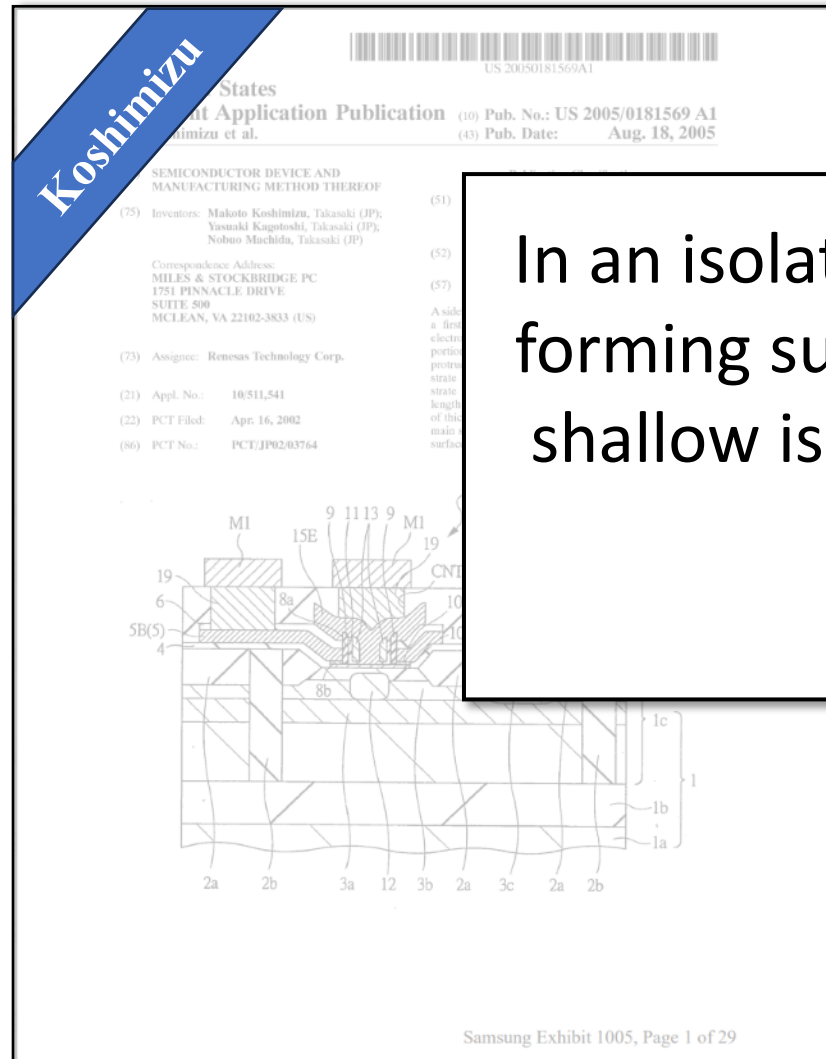
"[F]ormation of deep trench isolation regions." POR, 13.



"a manufacturing method for a semiconductor device" includes forming "an isolation region" where "a shallow isolation 2a and a **deep trench isolation 2b** are formed." *Koshimizu*, [0052].



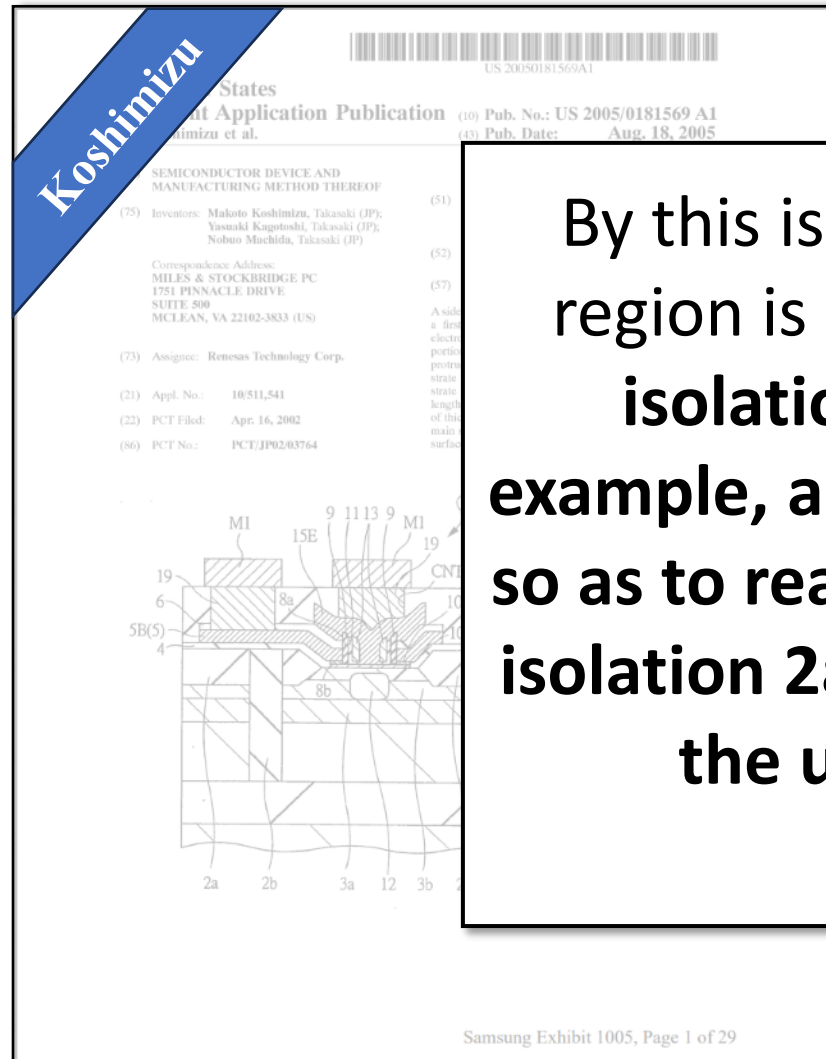
Koshimizu Is Analogous Art Even Under HID's Own Field Of Endeavor



In an isolation region of the main surface (device forming surface) of the semiconductor layer 1e, a shallow isolation 2a and a deep trench isolation 2b are formed.

Koshimizu, [0052].

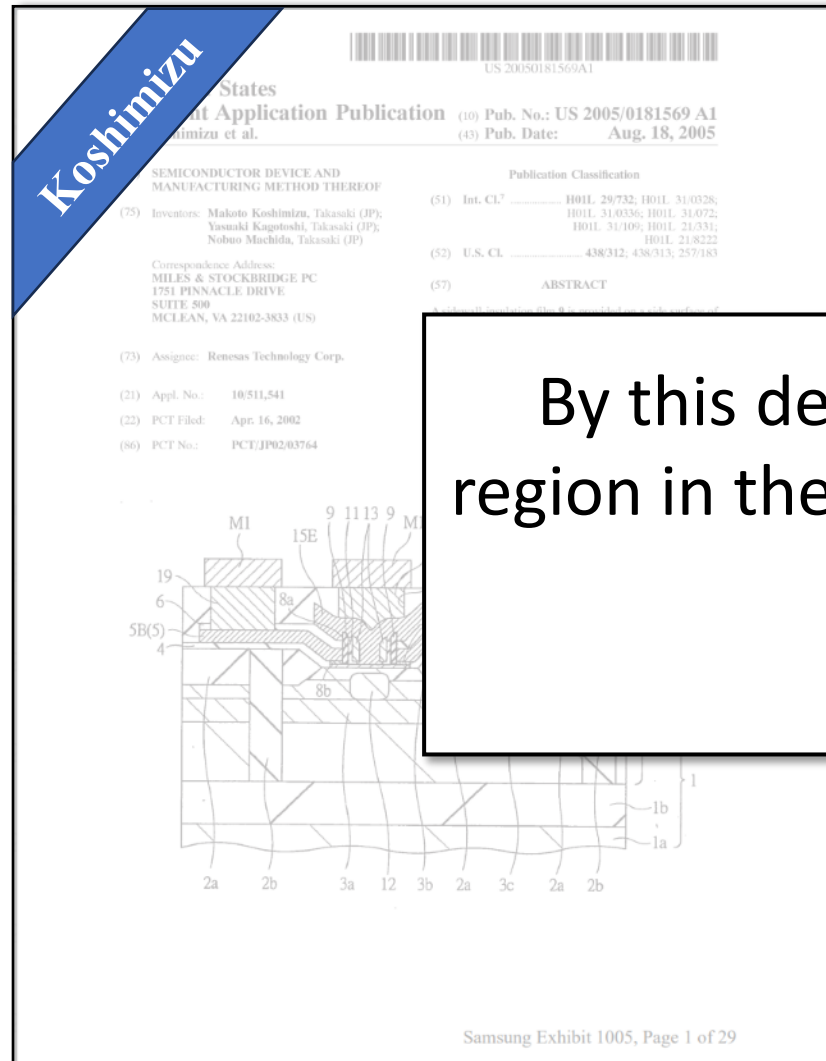
Koshimizu Is Analogous Art Even Under HID's Own Field Of Endeavor



By this isolation 2a, a plane range of an active region is defined. In addition, **the deep trench isolation 2b is formed by embedding, for example, a silicon oxide film in a deep trench dug so as to reach the insulation layer 1b through the isolation 2a and the semiconductor layer 1c from the upper surface of the isolation 2a.**

Koshimizu, [0052].

Koshimizu Is Analogous Art Even Under HID's Own Field Of Endeavor

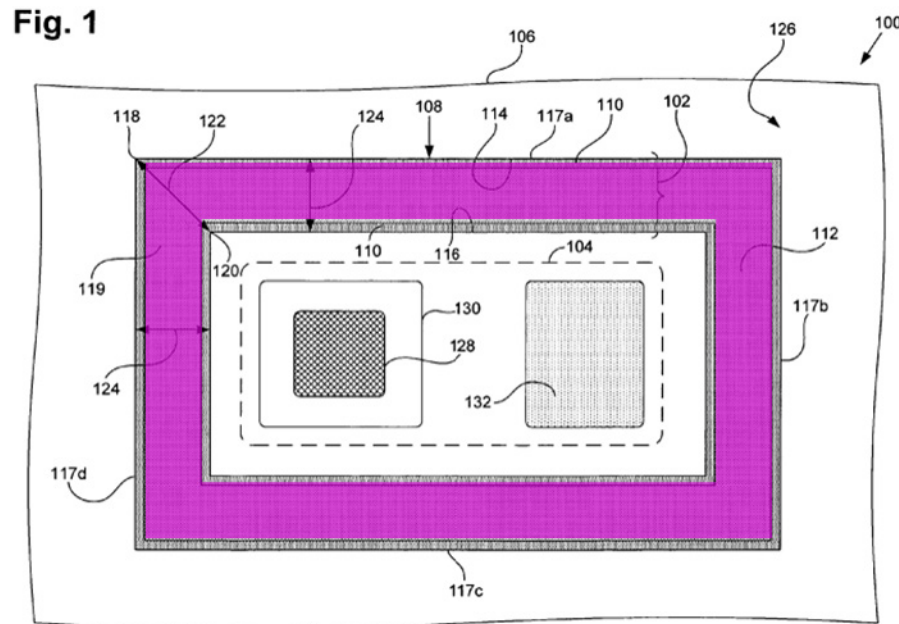


By this deep trench isolation 2b, each device region in the semiconductor layer 1c is completely separated electrically.
Koshimizu, [0052].

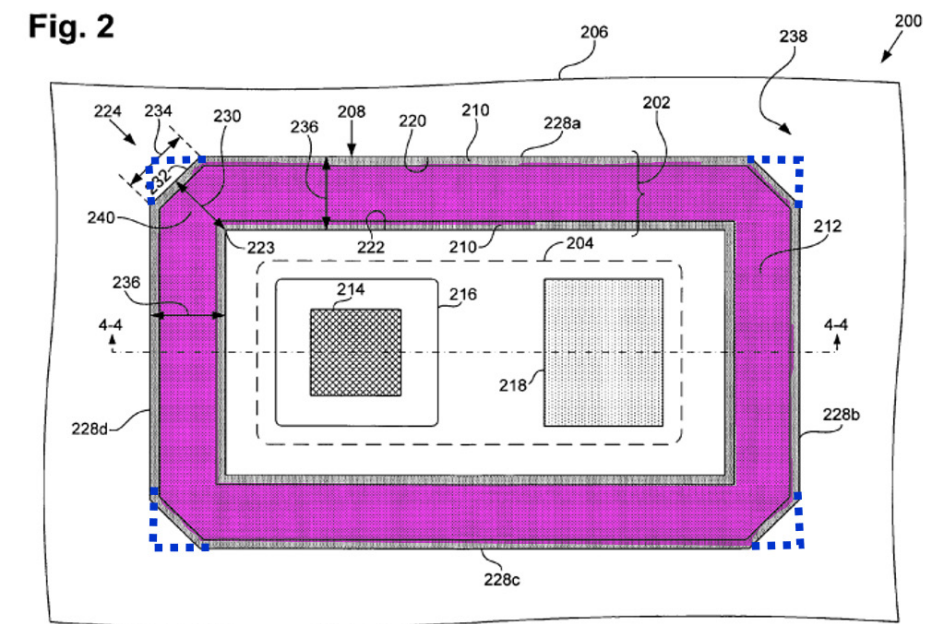
Koshimizu Is Reasonably Pertinent to the Problems Faced by the '673 Patent

Koshimizu Was Pertinent to The Problem Described In The Prior Art

- **Problem Faced by the '673 Patent:** “[P]rior art trenches required a thick layer of polysilicon to adequately fill them.” POR, 22.
- “[T]rench chamfered corners [] reduce the trench corner width . . . [and] advantageously reduce[] the deposited polysilicon layer thickness” ’673 Patent, 5:15-20.



Prior Art



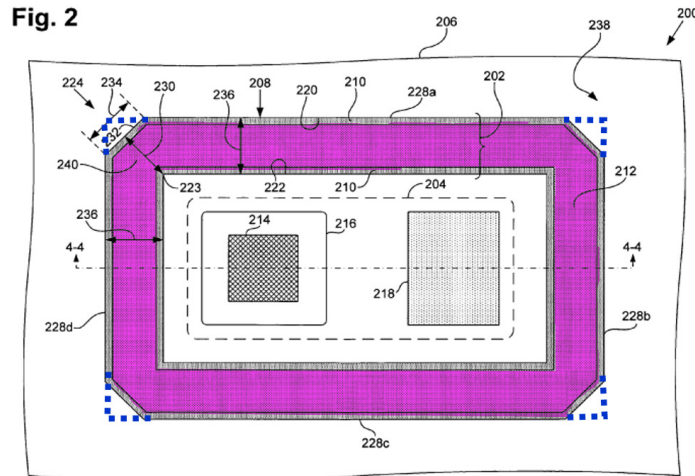
Alleged Invention

HID Does Not Rebut Petitioner's Expert Testimony

1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;

wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.



Expert, Dr. Scott Emmet Thompson

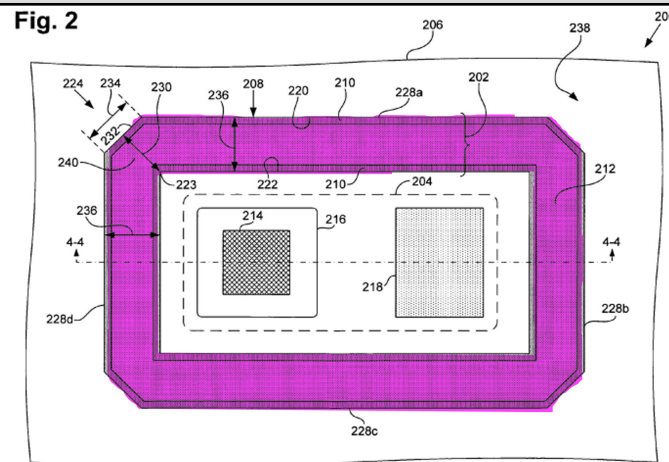
“Chamfered corners were also known to reduce the need for overfilling. For example, it was known before the '673 Patent that a deep isolation trench needs to be filled with isolating material such as polysilicon or silicon oxide such that all portions of the trench, including the widest portions of the trench, are completely filled. Because the portions of the trench are filled at the same time, this can cause overfill over the narrowest portions of the trench.” Thompson Dec., ¶184 (citing WOLF, 55-57) (emphasis added).

HID Finds Lack of Pertinence *Solely* Based on Fill Material

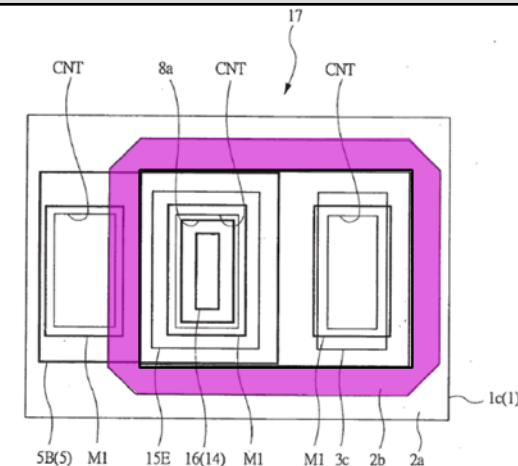
HID's Position

"A POSITA would not consider Koshimizu to be reasonably pertinent to this problem [because] Koshimizu does not mention polysilicon at all. Instead, **Koshimizu's deep trench is filled with silicon oxide . . . [which] has different stress . . . [and] electrical characteristics.**" POR, 23. "These differences, along with Koshimizu's complete lack of description as to how to manufacture a trench, would lead a POSITA to not look to Koshimizu." Sur-Reply, 5.

'673 Patent



Koshimizu



Koshimizu’s Isolating Material Does Not Change The Inquiry



Expert, Dr. Scott Emmet Thompson

“[I]t was known before the ’673 Patent that a deep isolation trench needs to be filled with *isolating material such as polysilicon or silicon oxide...*”
Thompson Dec., ¶84 (emphasis added).

Prior Art	Isolating Material Disclosure
WOLF (1990)	“If trenches of widely varying widths are filled, the narrow ones must be well overfilled in order for the wider ones to be filled completely. Thus, the thickness of the top-surface-deposited film will vary, making planarization very difficult. ”

Koshimizu’s Isolating Material Does Not Change The Inquiry



Expert, Dr. Scott Emmet Thompson

“[I]t was known before the ’673 Patent that a deep isolation trench needs to be filled with *isolating material such as polysilicon or silicon oxide...*”
Thompson Dec., ¶84 (emphasis added).

Prior Art	Isolating Material Disclosure
WOLF (1990)	“In trench-isolation structures, atmospheric-CVD polysilicon, LPCVD polysilicon, CVD SiO2 , and selective, epitaxially-grown (SEG) silicon have reportedly been used.”
Norström (2000)	“[T]he trenches are filled with an <i>isolating or semi-isolating material</i> 123, for example, <i>silicon oxide or polycrystalline silicon</i> [.]”.

Issues in Dispute

Ground 1

✓ *Koshimizu* is analogous art

Grounds 2, 3

☐ Does *Norström* disclose a trench that is both “situated in a substrate” and has “at least one trench chamfered corner”?

Norström Discloses a Trench that Is Both “Situated In A Substrate” and Has
“At Least One Trench Chamfered Corner”

Grounds 2 & 3: *Norström*

HID Does Not Dispute *Norström* teaches every element of every challenged claim except the trench limitation.



1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

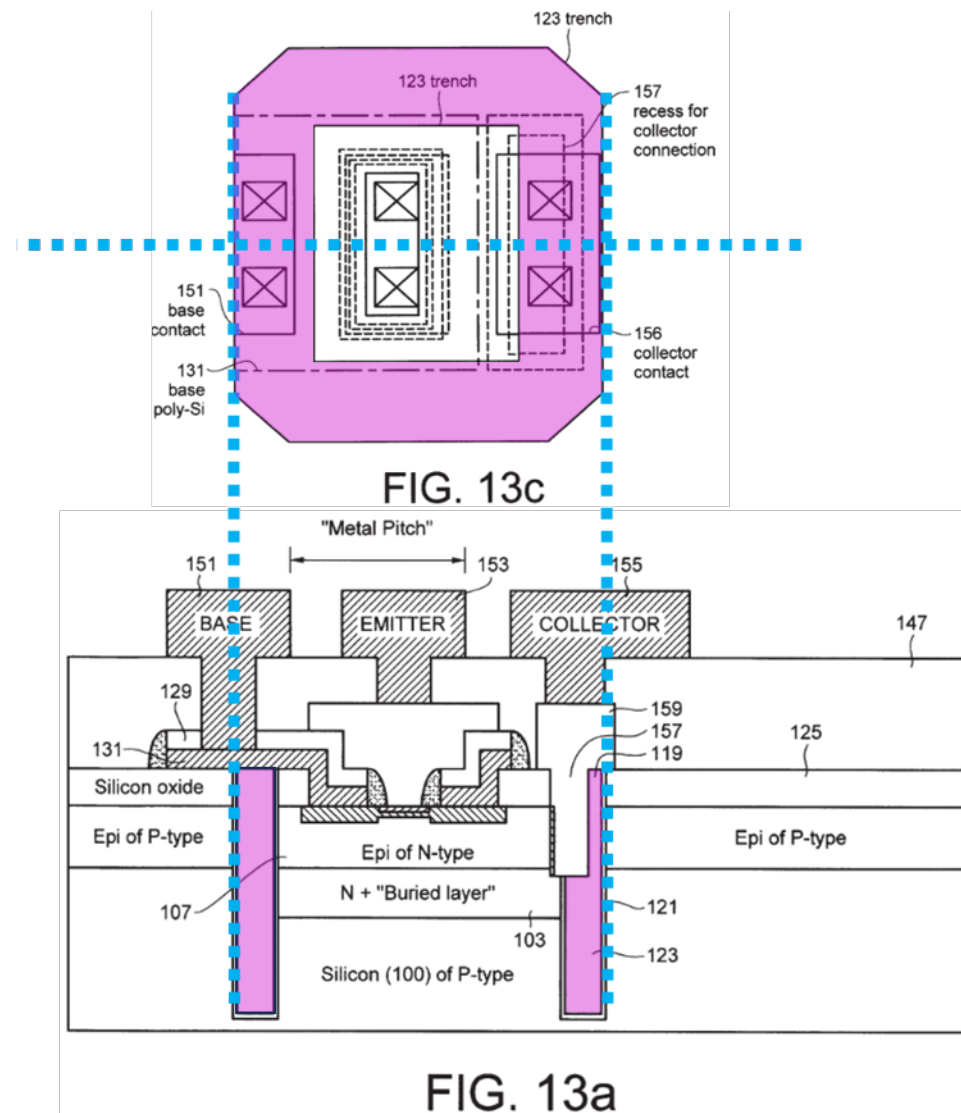
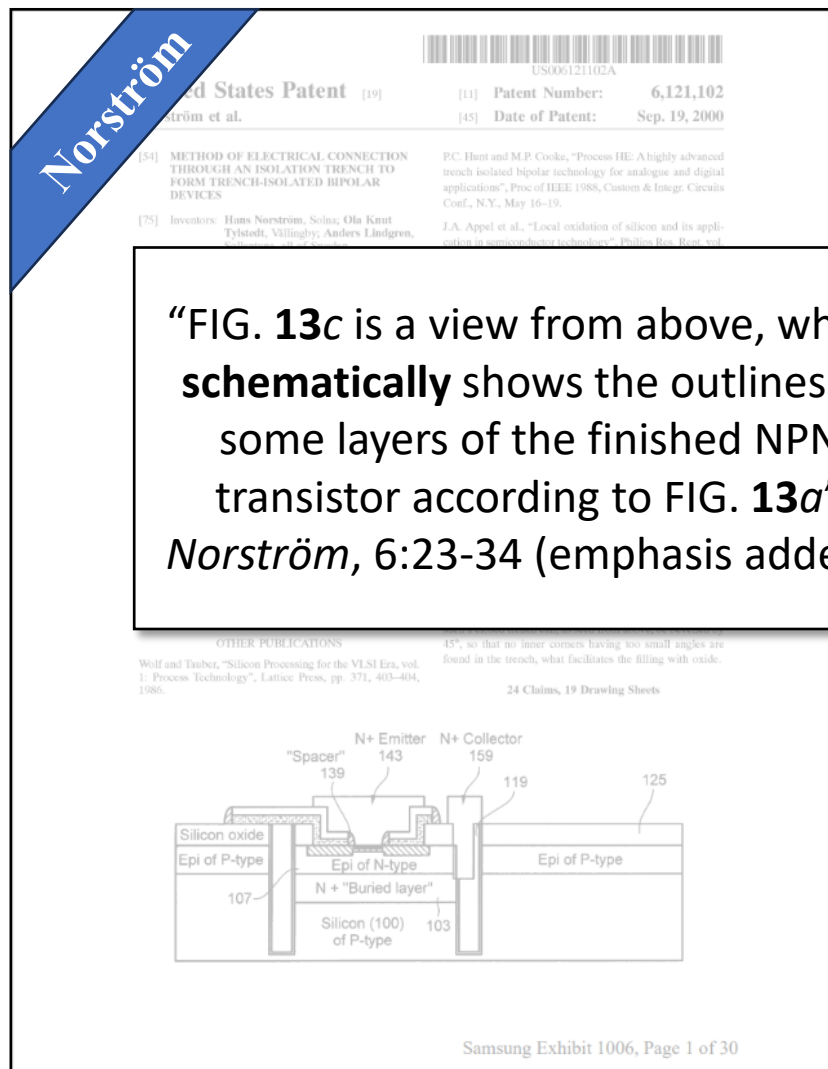


a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;



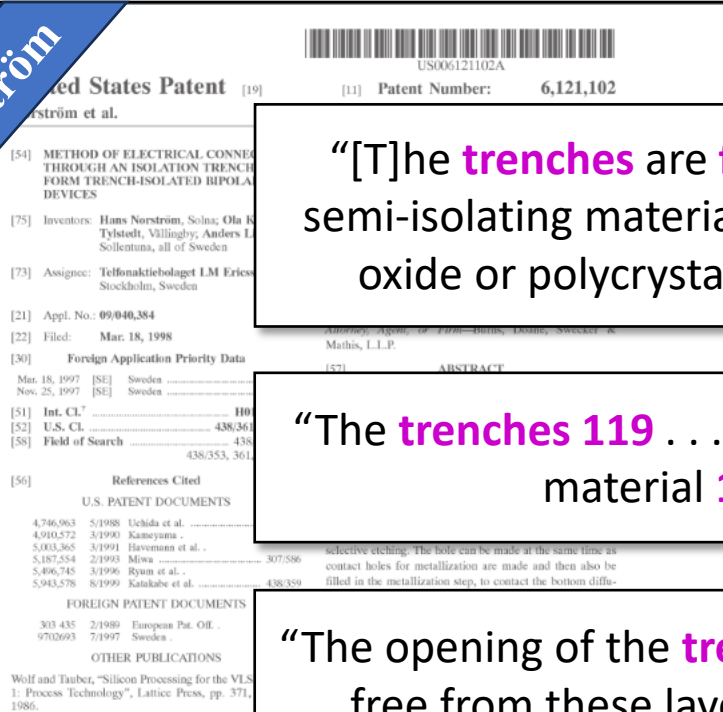
wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Norström Explains That Trench 123 is Both Chamfered and Situated in The Substrate



Norström Explains That Trench 123 is Both Chamfered and Situated in The Substrate

Norström



"[T]he **trenches** are **filled** with an isolating or semi-insulating material **123**, for example, silicon oxide or polycrystalline silicon[.]" 7:47-50.

"The **trenches 119** . . . are **filled** with an isolating material **123**." 9:42-48.

"The opening of the **trench 119** at this side is thus free from these layers 129, 131." 10:14-15.

"[T]he outer sidewalls of the **trench 123** shown in FIG. 13c **have no right angles**" and its corners can be beveled by 45° to become 135°. 16:28-42.

Samsung Exhibit 1006, Page 1 of 30

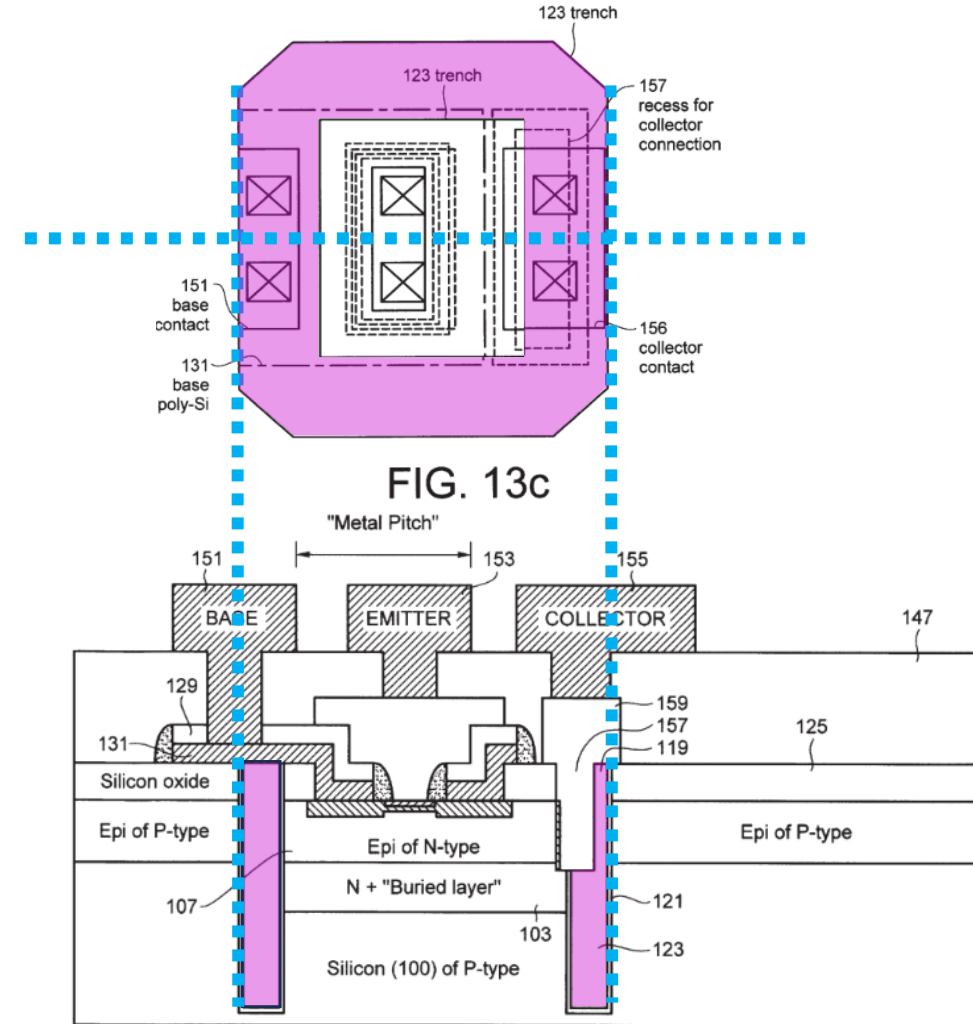


FIG. 13a

Norström Has One Four-Sided Trench



Expert, Dr. Scott Emmet Thompson

Q: “Okay, figure 13 (a) shows two isolating trenches?”

A: “Figure 13 (a) is a cross-sectional cut, so we’re seeing the regions where the cut interacted [sic] to a trench to the right and left of the bipolar device.”

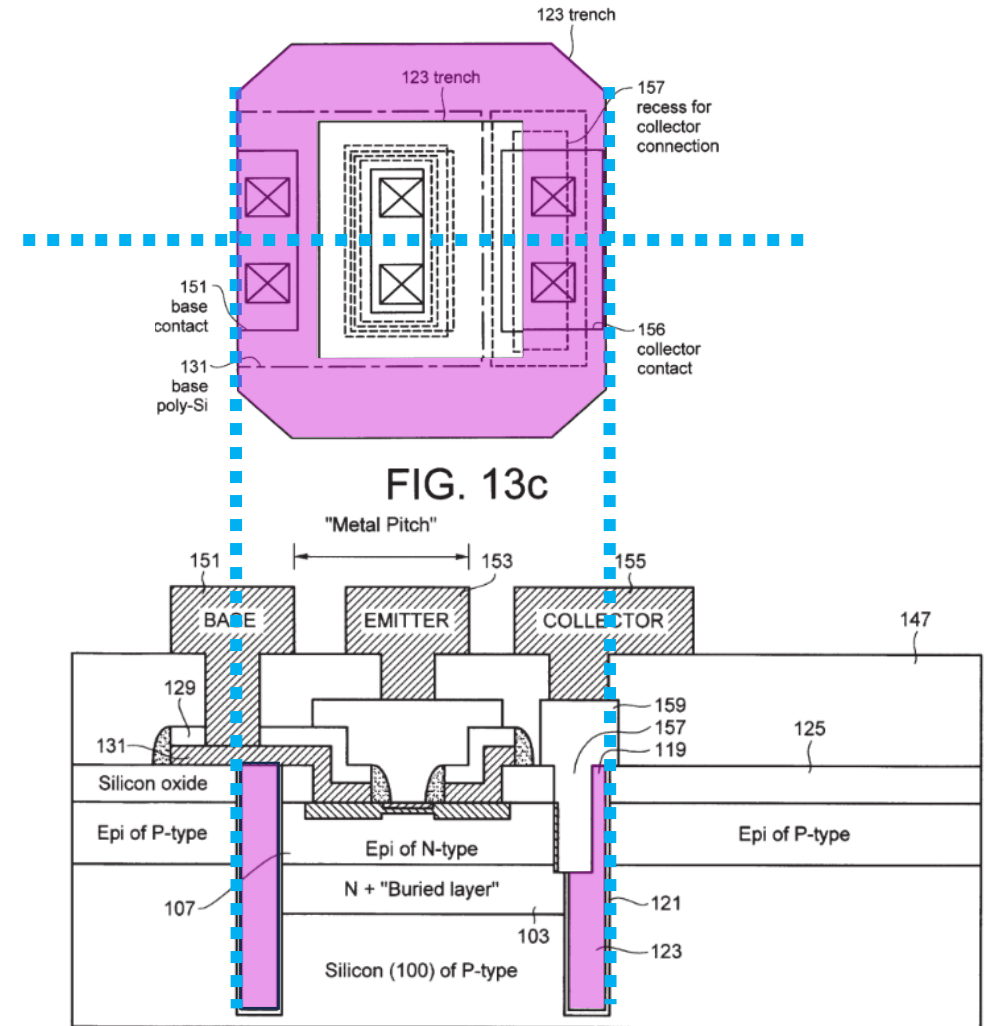
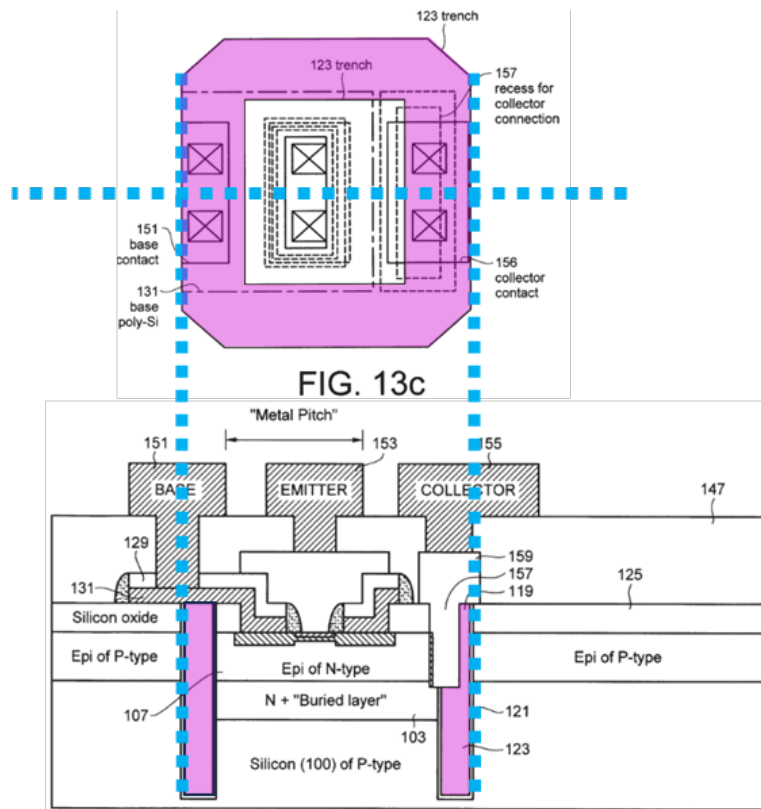


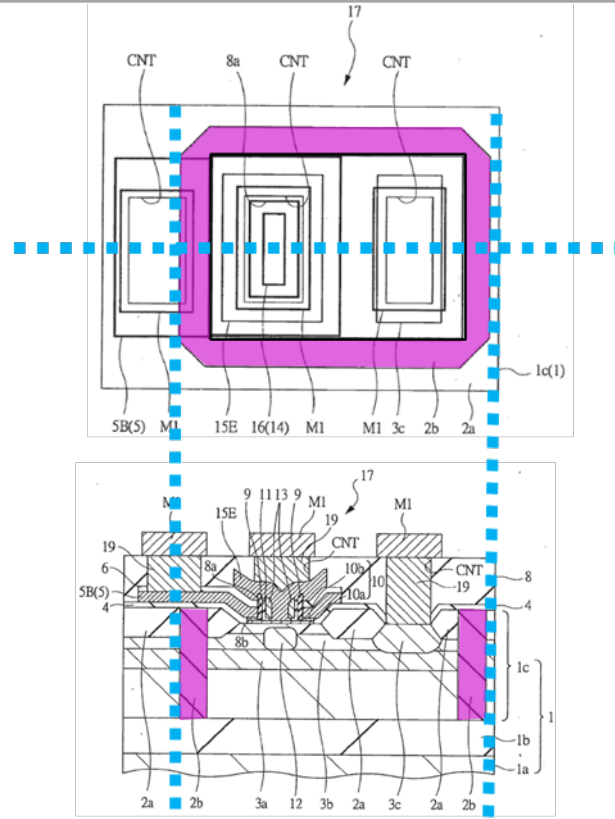
FIG. 13a

Cross-Sectional Views Showing Left And Right Sides Of Trenches Were Very Common In The Prior Art

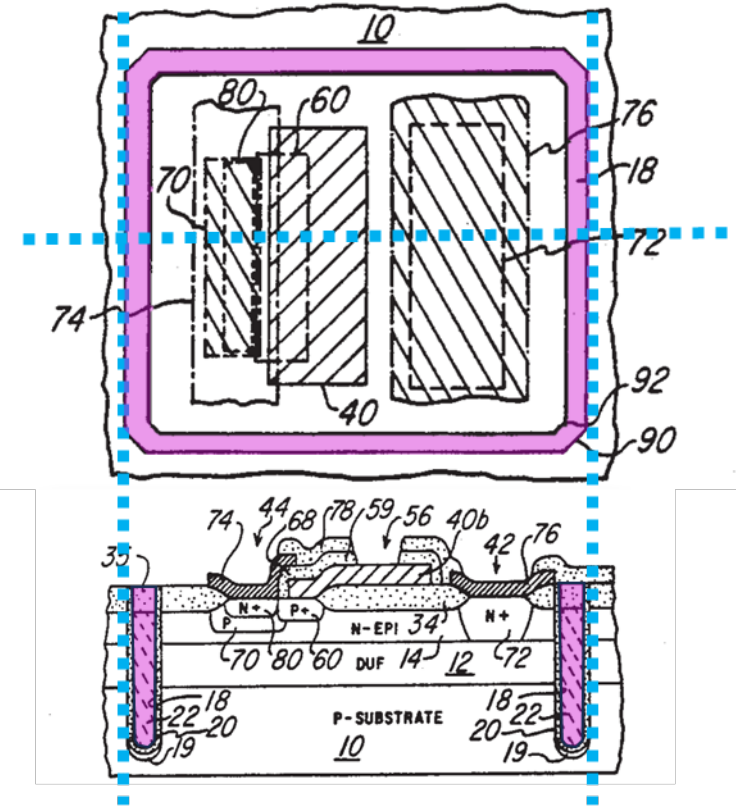
Norström (2000)



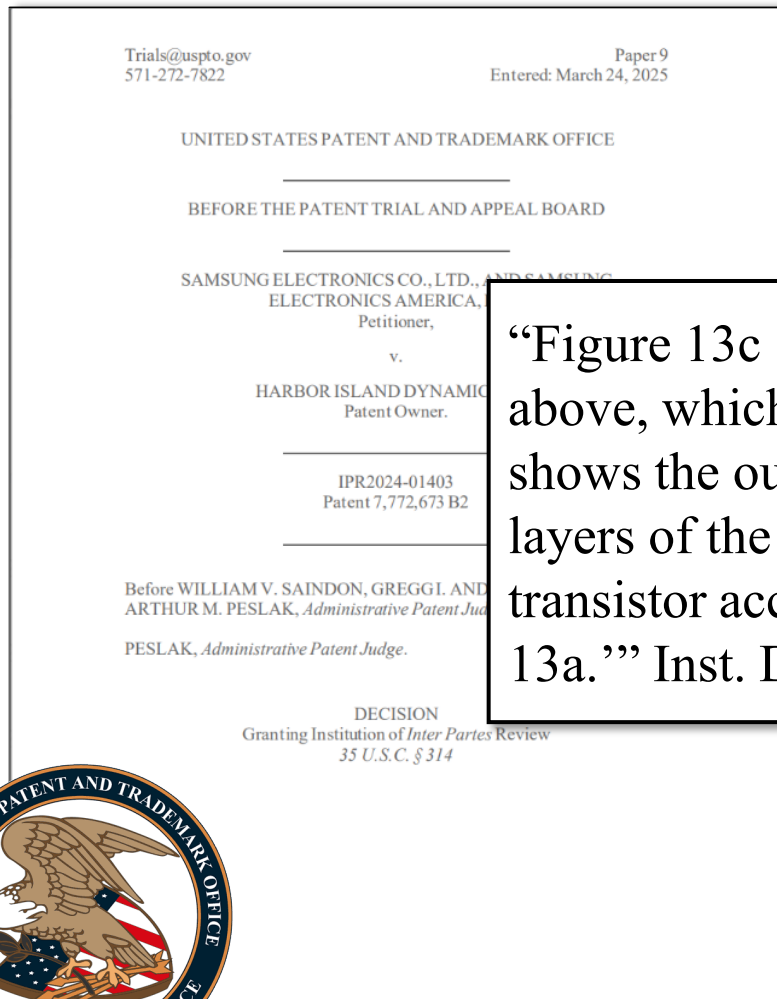
Koshimizu (2005)



'816 Patent (1992)



Norström Discloses the Accused Trench



“Figure 13c ‘is a view from above, which schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.’” Inst. Dec., 31.

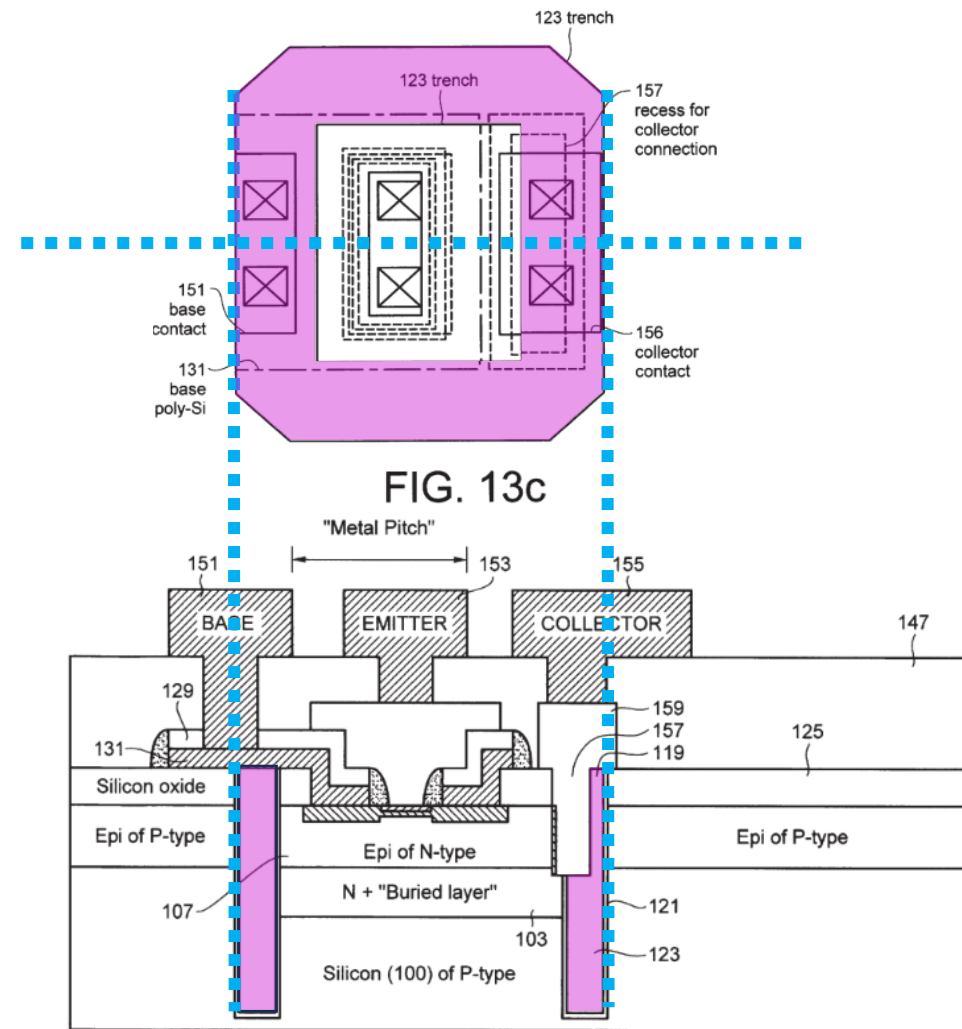


FIG. 13a

Grounds 2 & 3: *Norström*

Norström discloses a trench that is **both** “situated in a substrate” and has “at least one trench chamfered corner”



1. A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:



a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;



wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Issues in Dispute

Ground 1

✓ *Koshimizu* is analogous art

Grounds 2, 3

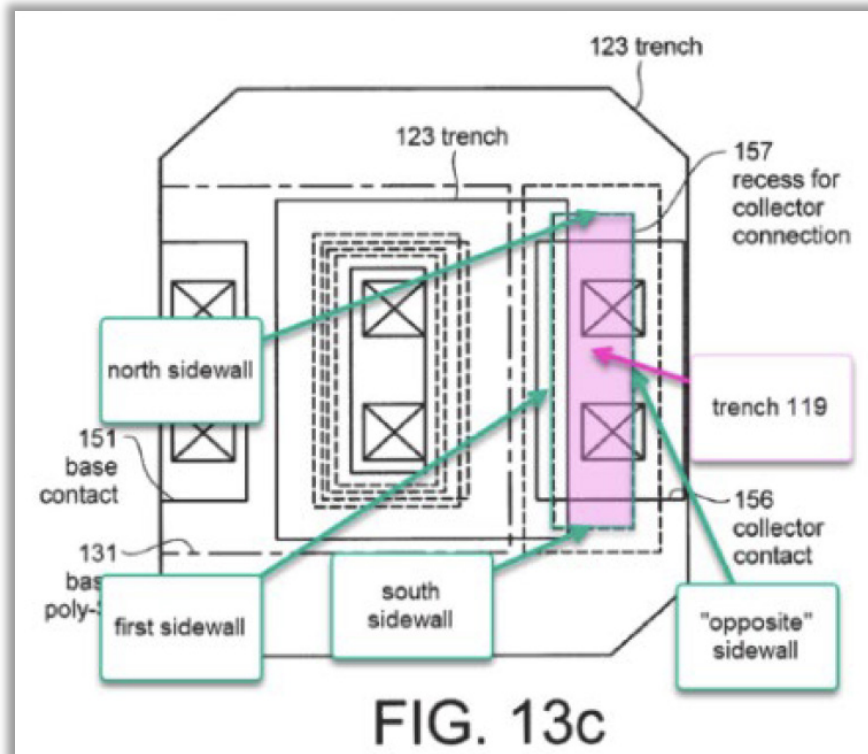
✓ *Norström* discloses a trench that is both “situated in a substrate” and has “at least one trench chamfered corner”

Additional Slides

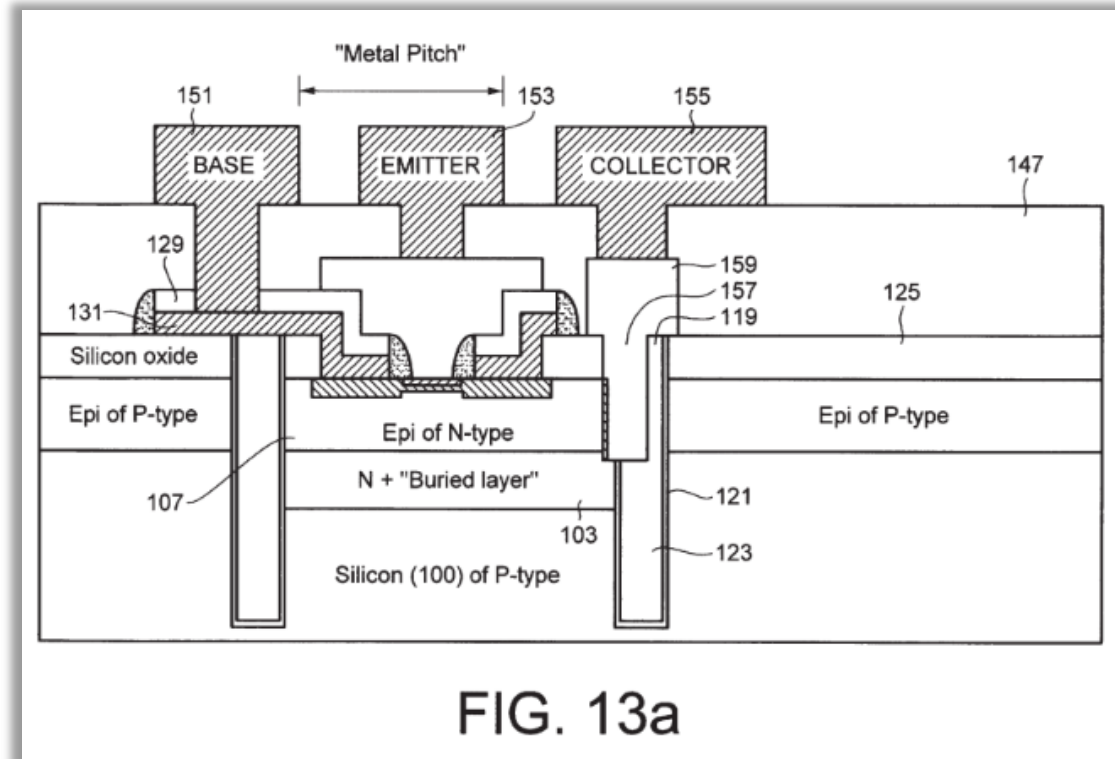
HID's Theory – 119 and 123 Are Structurally Separate Trenches

HID's "Interpretation" of *Norström*

Norström Elements 119 and 123 are two structurally separate trenches. POR, 25-33.



HID's Annotated FIG. 13c

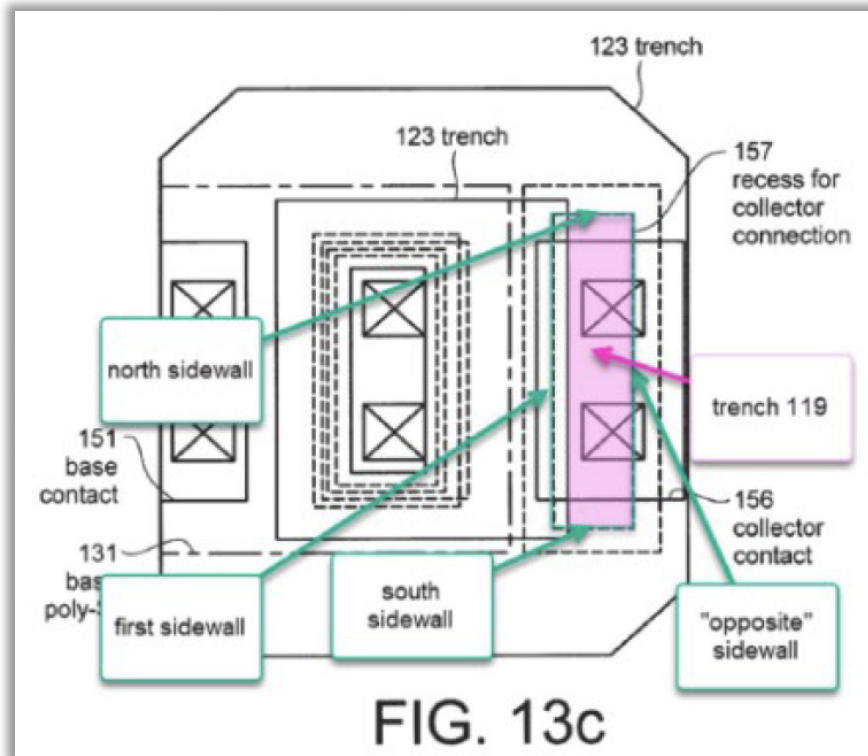


Original FIG. 13a

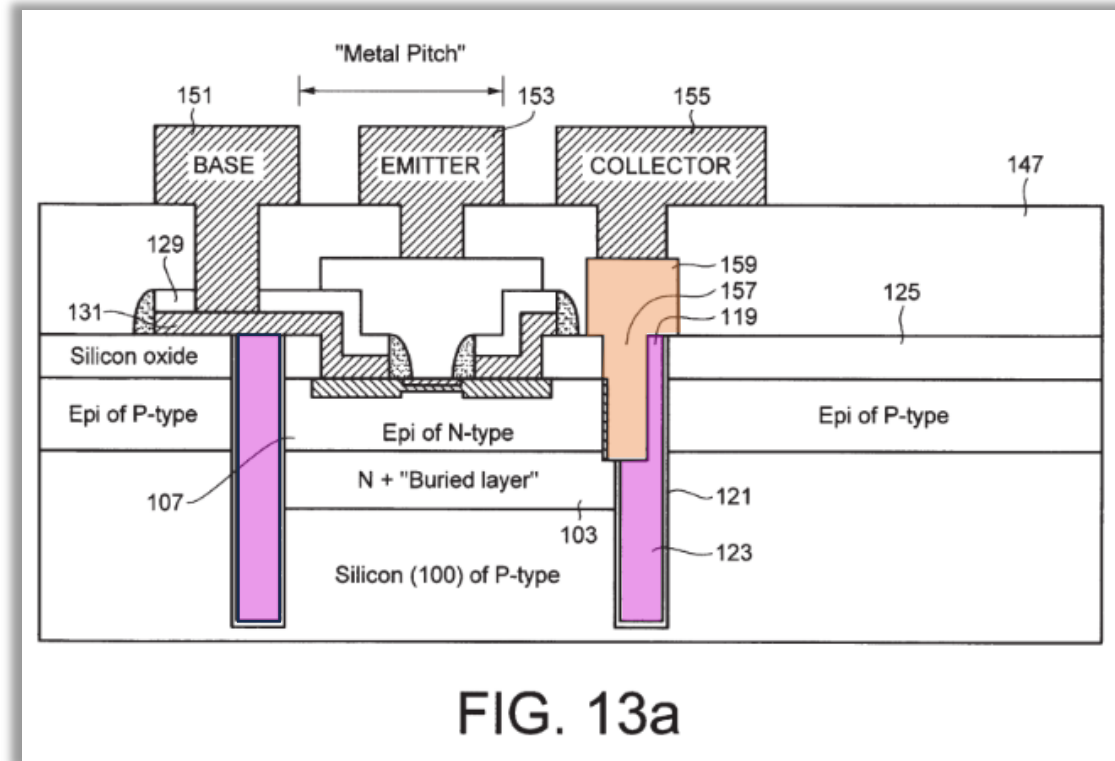
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HID's Annotated FIG. 13c



Petitioner's Annotated FIG. 13a

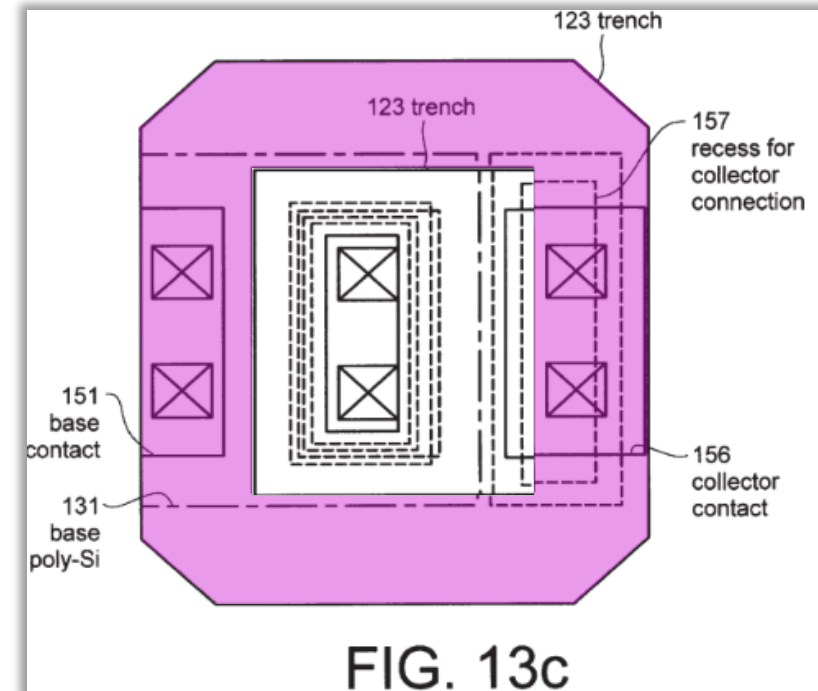
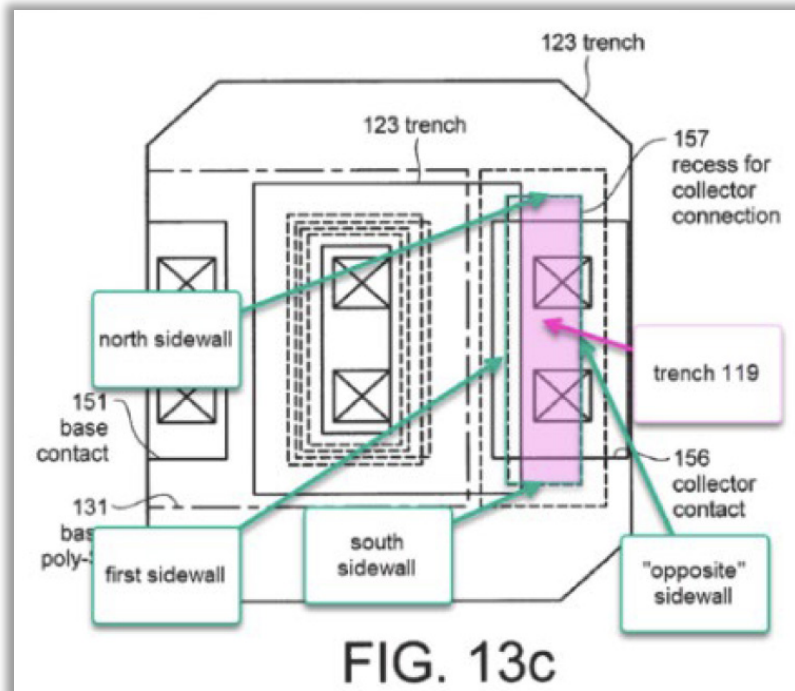
HID Seeks to Redraw *Norström's* Figures

HID's "Interpretation" of *Norström*

Reference numbers 119 and 123 are two separate trenches. "Trenches 119" do not have chamfered corners, and "trench 123" is not in the substrate of the semiconductor.

Norström

"The trenches 119 . . . are filled with an isolating material 123." *Norström*, 9:42-48. I.e., reference number 119 is the empty trench and 123 is the filled trench.

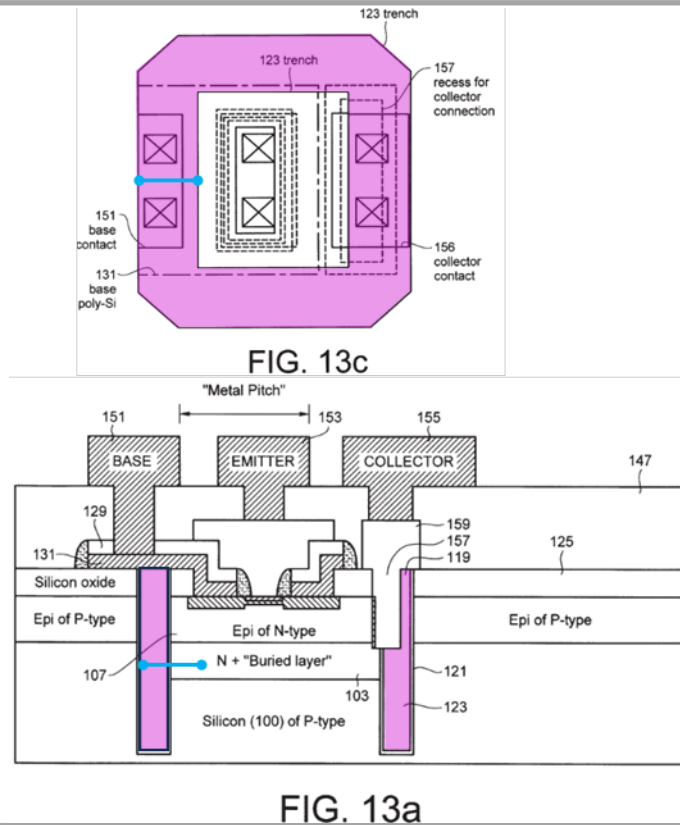


HID Wrongly Asserts *Norström's* Figures Must Be Drawn To Scale

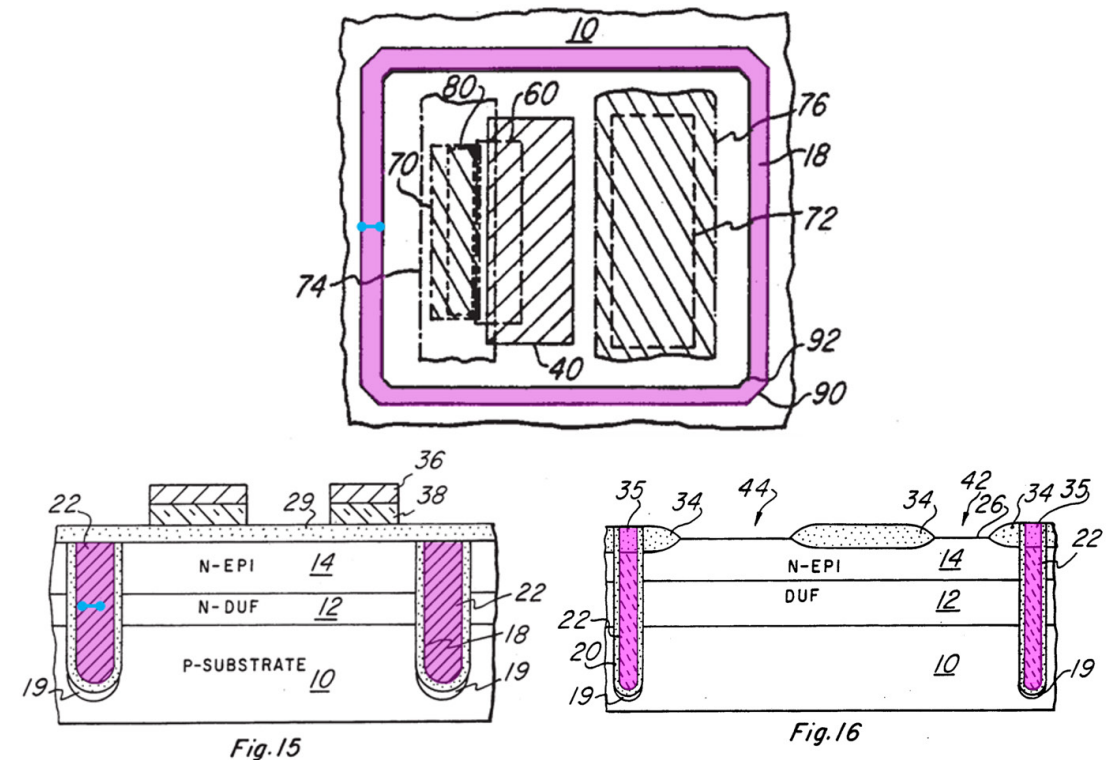
HID's "Interpretation" of *Norström*

Norström must have two structurally separate trenches because trenches 119 are "narrow." POR, 30-32.

Norström (2000)



'816 Patent (1992)

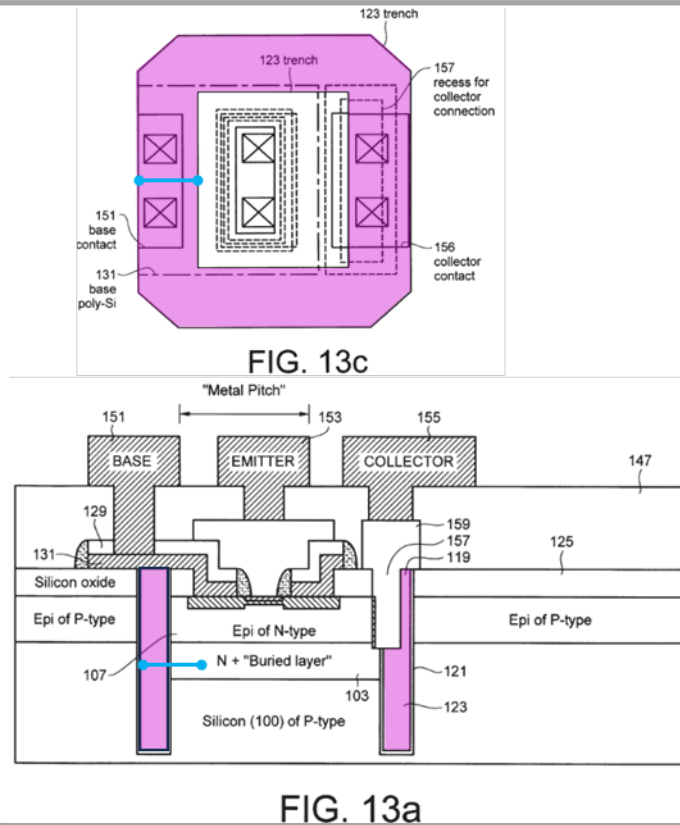


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Norström must have two structurally separate trenches because trenches 119 are "narrow." POR, 30-32.

Norström (2000)



'816 Patent (1992)

"FIGS. 1 to 27 are greatly enlarge [sic] sectional elevation views of one cell of a semiconductor chip made in accordance with a preferred embodiment of the invention and showing the device at successive stages of manufacture[.]"
'816 Patent, 2:50-54.

