

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD. AND  
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 7,772,673

Filing Date: March 16, 2007

Issue Date: August 10, 2010

Inventors: Kevin Q. Yin, Amol Kalburge, David J. Howard,  
Arjun Kar-Roy, and Dieter Dornisch

Title: DEEP TRENCH ISOLATION AND METHOD OF FORMING SAME

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**PATENT OWNER'S NOTICE OF APPEAL**

Case No. IPR2024-01403

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Pursuant to 35 U.S.C. §§ 141 and 142 and 37 C.F.R. §§ 90.2 and 90.3, Patent Owner Harbor Island Dynamic LLC (“HID” or “Patent Owner”) hereby provides notice that it appeals to the United States Court of Appeals for the Federal Circuit from the Final Written Decision entered February 9, 2026 (Paper 33, attached hereto as Exhibit A) and from all underlying orders, decisions, rulings, and opinions regarding U.S. Patent No. 7,772,673 (the “’673 patent”) in Case No. IPR2024-01403. This notice is timely under 37 C.F.R. § 90.3 having been filed within 63 days after the date of the Final Written Decision. For the limited purpose of providing the Director with the information requested in 37 C.F.R. § 90.2(a)(3)(ii), Patent Owner anticipates that the issues on appeal may include, but are not limited to: the Board’s claim constructions; its application of those constructions; any implied claim constructions; its obviousness determinations including that claims 1-17 of the ’673 patent are unpatentable under 35 U.S.C. § 103; any findings related to secondary considerations of non-obviousness; the findings, rulings and conclusions supporting or relating to those determinations; and any other issues decided adversely to Patent Owner in any orders, decisions, rulings, or opinions in IPR2024-01403.

Simultaneous with this submission, a copy of this Notice of Appeal is being filed with the Clerk of the United States Court of Appeals for the Federal Circuit

through the Court's CM/ECF system, together with the requisite fee in the amount of \$600.00. In addition, a copy of this Notice of Appeal is being filed with the Patent Trial and Appeal Board and served upon counsel of record for Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Respectfully submitted,

Dated: April 10, 2026

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# EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG  
ELECTRONICS AMERICA, INC.,  
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Patent Owner.

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IPR2024-01403  
Patent 7,772,673 B1

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Before HYUN J. JUNG, GREGG I. ANDERSON, and  
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining All Challenged Claims Unpatentable  
35 U.S.C. § 318(a)

## I. INTRODUCTION

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively “Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1–17 (“the Challenged Claims”) of U.S. Patent No. 7,772,673 B1 (“the ’673 patent,” Ex. 1001). Paper 1 (“Pet.”). Petitioner filed a Declaration of Dr. Scott E. Thompson, Ph.D., in support of the Petition. Ex. 1003. Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). On March 24, 2025, we instituted this *inter partes* review as to the Challenged Claims and all grounds presented in the Petition. Paper 9 (“Dec.”).

After institution, Patent Owner filed a Response to the Petition (“PO Resp.”). Paper 17. In support of the Patent Owner Response, Patent Owner filed a Declaration of John Berg. Ex. 2004. Petitioner filed a Reply (“Pet. Reply”). Paper 20. Patent Owner filed a Sur-reply (“Sur-reply”). Paper 22. An oral hearing was held on January 6, 2026, and the transcript is entered into the record. Paper 32.

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the Challenged Claims. For the reasons discussed below, we determine Petitioner establishes by a preponderance of the evidence that all Challenged Claims are unpatentable.

### A. *Related Matters*

The parties identify the following proceedings as related matters:  
*Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, No. 2:24-cv-00140-JRG-RSP

(E.D. Tex.) (“District Court Litigation”) and *Harbor Island Dynamic, LLC v. NXP Semiconductors N.V.*, No. 2:24-cv-00717-JRG-RSP (E.D. Tex.).  
Pet. 75; Paper 6 (Patent Owner’s Mandatory Notices), 2.

*B. Real Parties in Interest*

Petitioner identifies “Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.” as the real parties-in-interest. Pet. 75. Patent Owner identifies itself as the sole real party-in-interest. Paper 6, 2.

*C. The ’673 patent (Ex. 100)*

The ’673 patent is titled “Deep Trench Isolation and Method for Forming Same.” Ex. 1001, code (54). The ’673 patent relates “generally [to] the field of semiconductor fabrication,” and, “[m]ore particularly, . . . [to] the field of isolation region formation in semiconductor substrates.” *Id.* at 1:7–10. The invention’s background is described as “[d]eep trench isolation regions . . . formed to provide electrical isolation for electronic devices in a semiconductor die.”<sup>1</sup> *Id.* at 1:12–14. A described problem is that, “for a rectangular-shaped trench, a thick layer of polysilicon can be required to adequately fill the trench with polysilicon” and “depositing a thick layer of polysilicon can significantly reduce polysilicon fill process throughput.” *Id.* at 1:32–36.

Figure 1 is reproduced below:

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<sup>1</sup> Dr. Thompson explains that “a ‘semiconductor die’ is simply a wafer of semiconductor material such as silicon, and a ‘semiconductor package’ is the physical package in which an integrated circuit is stored,” and further, “[a] semiconductor die houses the transistors, such as bipolar junction transistors, that make up the computer logic of the integrated circuit.” Ex. 1003 ¶ 47 (citing Ex. 1012, 1).

**Fig. 1**

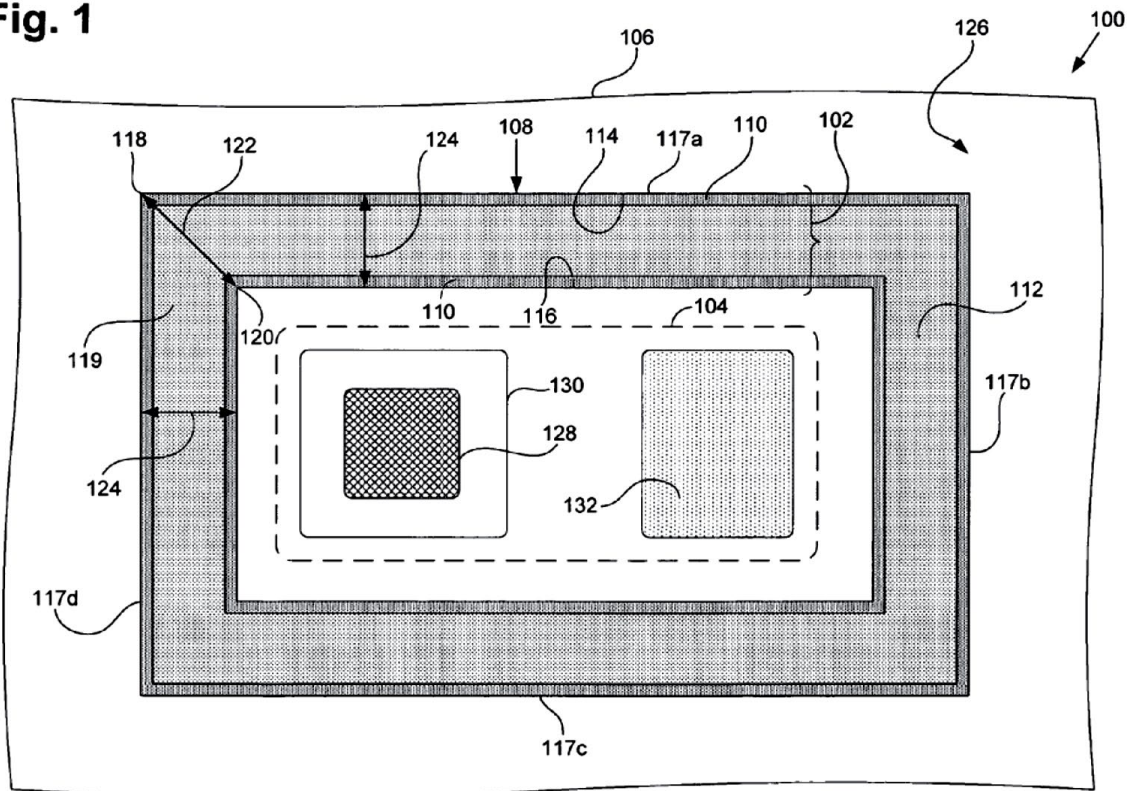


Figure 1 “shows a top view of an exemplary conventional deep trench isolation region in a semiconductor die.” Ex. 1001, 1:53–54. As shown, the semiconductor die 100 includes silicon substrate 106, bipolar device 104, and the conventional deep trench isolation region 102. *Id.* at 2:39–43. The deep trench isolation region 102 includes a rectangular trench 108, silicon oxide liner 110, and polysilicon filling 112. *Id.* at 2:43–45, 3:31. The bipolar device 104 includes an active region 130, an emitter 128 situated over the active region 130, and a collector 132. *Id.* at 2:45–46. Field oxide regions overlay the deep trench isolation region 102 and separate the active region 130 from the collector 132. *Id.* at 2:47–49.

The rectangular trench 108 is situated in the substrate 106, has an outside wall 114 including corners 118, an inside wall 116 including corners 120, and sides 117a, 117b, 117c, and 117d. Ex. 1001, 3:6–12. A trench

corner width 122 represents the perpendicular distance (i.e., the minimum distance) between the corners 118 of the outside wall 114 and corners 120 of the inside wall 116. *Id.* at 3:12–15. A trench side width 124 represents the perpendicular distance between the outside wall 114 and inside wall 116 along each of the sides 117. *Id.* at 3:15–18.

The silicon oxide liner 110 is situated on the outside walls 114, inside walls 116, and bottom surface (not shown) of the trench 108.

Ex. 1001, 3:29–31. The polysilicon filling 112 is situated in trench 108 and formed by conformally depositing a layer of polysilicon (polycrystalline silicon) over top surface 126 of substrate 106. *Id.* at 3:34–37. By this configuration, the deep trench isolation region 102 encloses the bipolar device 104. *Id.* at 2:55–56. The enclosing isolates the bipolar device 104 from the substrate 106 and, in turn, from surrounding bipolar devices situated on the substrate 106. *Id.* at 2:66–3:2. The isolating of the collector 132 from the neighboring substrate also reduces collector-to-substrate capacitance. *Id.* at 3:2–5.



chamfered edge 232 and each of the corners 223 of the inside wall 222 of the trench 208. Ex. 1001, 4:33–36. Though each of the trenches 108, 208 has a trench side width 124, 236 of 1.0 micron and a depth of 7.0 microns, the thicknesses of the deposited polysilicon layers for the rectangular trench 108 shown in Figure 1 and the Figure 2 embodiment's trench 208 are respectively 1.5 microns and 0.7 microns. *Id.* at 3:37–45; 5:4–26. Thus, relative to the Figure 2 embodiment's trench 208, manufacture of the rectangular trench 108 entails a greater polysilicon fill process throughput and accordingly increased cost. *Id.* at 3:41–50; 5:21–30.

Figure 4E of the '673 patent is reproduced below:

**Fig. 4E**

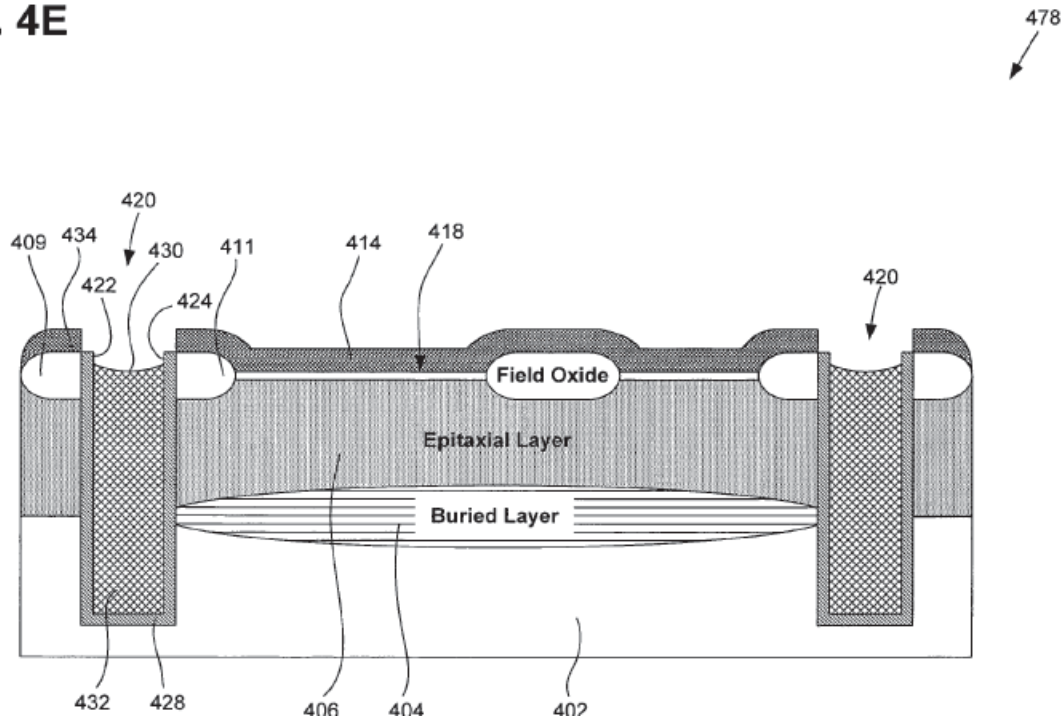


Figure 4E is “a cross-sectional view, which includes a portion of a wafer processed according to an embodiment of the invention.” Ex. 1001, 2:9–11. Figure 4E shows an oxide liner 428 formed on the “outside and inside walls 422 and 424 and bottom surface 426 of trench 420.” *Id.* at 7:59–61. Trench 420 is filled with polysilicon filling 432. *Id.* at 8:34–35.

*D. Illustrative Claim*

Claims 1 and 10 are independent claims. Claim 1 is reproduced, below, with Petitioner's limitation identifiers in brackets (Pet. ii):

1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:

1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides; and

1[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.

Ex. 1001, 9:36–47.

*E. Prior Art and Asserted Grounds*

Petitioner asserts that claims 1–17 would have been unpatentable on the following grounds (Pet. 20–21):

| <b>Claim(s) Challenged</b>   | <b>35 U.S.C. §<sup>2</sup></b> | <b>References/Basis</b>                  |
|------------------------------|--------------------------------|------------------------------------------|
| 1–17                         | 103(a)                         | Yin, <sup>3</sup> Koshimizu <sup>4</sup> |
| 1, 3, 5, 7, 8, 10, 12, 14–16 | 102                            | Norström <sup>5</sup>                    |
| 7, 15                        | 103(a)                         | Norström                                 |

II. ANALYSIS

*A. Overview*

“In an [inter partes review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in inter partes review).

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<sup>2</sup> The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103. Because the ’673 patent claims priority to an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of §§ 102, 103 applies.

<sup>3</sup> U.S. Patent No. 6,995,449 B1 issued Feb. 7, 2006 to Yin et al. (Ex. 1004).

<sup>4</sup> U.S. Patent Application Publication No. 2005/0181569 A1 published Aug. 18, 2005 to Koshimizu et al. (Ex. 1005).

<sup>5</sup> U.S. Patent No. 6,121,102 issued September 19, 2000 to Norström et al. (Ex. 1006).

To establish anticipation under 35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable as obvious “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and

(4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).<sup>6</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained in *KSR* that

Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original))).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

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<sup>6</sup> No evidence of secondary considerations has been entered into the record.

*B. Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and *vice versa*.” Pet. 22–23 (citing Ex. 1003 ¶ 63).

Patent Owner counters that a person of ordinary skill in the art would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. A person also would have qualified as a POSITA with some combination of (1) more formal education (such as Master of Science degrees) and less technical experience, or (2) less formal education and more technical or professional experience in the fields lists above.

PO Resp. 8–9 (citing Ex. 2004 ¶¶ 25–27). Patent Owner also criticizes Petitioner’s “requirement of a master’s degree[s]” because “engineers working in this field and implementing designs such as those described in the ’673 Patent, typically have bachelor’s degrees.” *Id.* (citing Ex. 2004 ¶ 27).

Petitioner in turn argues that Patent Owner’s proposed level of skill in the art is an “immaterial” variation of Petitioner’s proposal. Pet. Reply 1. Petitioner further argues that “[b]oth parties agree that a POSITA would have at least two years of experience in semiconductor design and fabrication, and nothing in the POR identifies any claim element or obviousness analysis that would turn on whether a POSITA held a bachelor’s or master’s degree.” *Id.* at 2.

We apply Petitioner’s proffered level of skill in the art because it appears consistent with the problems addressed in the ’673 patent and the prior art. However, our determinations herein would not change if we applied Patent Owner’s proffered level of skill in the art.

*C. Claim Construction*

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b) (2023). Accordingly, we construe each challenged claim of the ’673 patent to generally be “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

Neither Petitioner nor Patent Owner proposes any claim construction. Pet. 19; PO Resp. 9. Based on our review of the record, we determine that no express construction of any claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*D. Ground 1: Obviousness of Claims 1–17  
over Yin and Koshimizu*

Petitioner contends claims 1–17 would have been obvious over Yin in view of Koshimizu. Pet. 23–57. Petitioner supports its contentions with Dr. Thompson’s Declaration. Ex. 1003.

We begin with a brief summary of Yin and Koshimizu. We then address the parties' contentions.

*1. Yin (Ex. 1004)*

Yin<sup>7</sup> is titled “Deep Trench Isolation Region with Reduced-Size Cavities in Overlying Field Oxide.” Ex. 1004, code (54). Yin “relates to the field of fabrication of semiconductor devices” and, “[m]ore specifically, . . . to forming isolation regions in semiconductor substrates.” *Id.* at 1:11–14.

Yin describes a “typical conventional deep trench isolation process.” Ex. 1004, 1:28. Principally, a layer of silicon nitride is deposited on a silicon substrate. *Id.* at 1:29–30. A hard mask of dense oxide is then formed over the nitride layer. *Id.* at 1:31–34. A photoresist mask is patterned over the hard mask. *Id.* at 1:35–36. The trench is accordingly etched into the silicon substrate. *Id.* at 1:36–39. A dense oxide liner is formed on the sidewalls of the trench and on the surface of the silicon substrate. *Id.* at 1:43–45. A conformal layer of polysilicon is deposited over the silicon substrate and trench. *Id.* at 1:48–50. The hard mask is removed by a wet etch, which causes unwanted lateral etching of the dense oxide layer. *Id.* at 1:53–59.

The invention provides “an effective method for removing a hard mask in a deep trench isolation process.” Ex. 1004, 2:18–20. The hard mask is removed by dry etching the hard mask. *Id.* at 2:35–37. An oxide liner is then deposited on the sidewalls of the trench and over the substrate.

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<sup>7</sup> The two named co-inventors on Yin are also two of the co-inventors named on the '673 patent. Ex. 1001, code (75); Ex. 1004, code (75).

*Id.* at 2:39–41. The oxide liner is removed by a wet strip process.

*Id.* at 2:42–43.

Figure 2G is reproduced below:

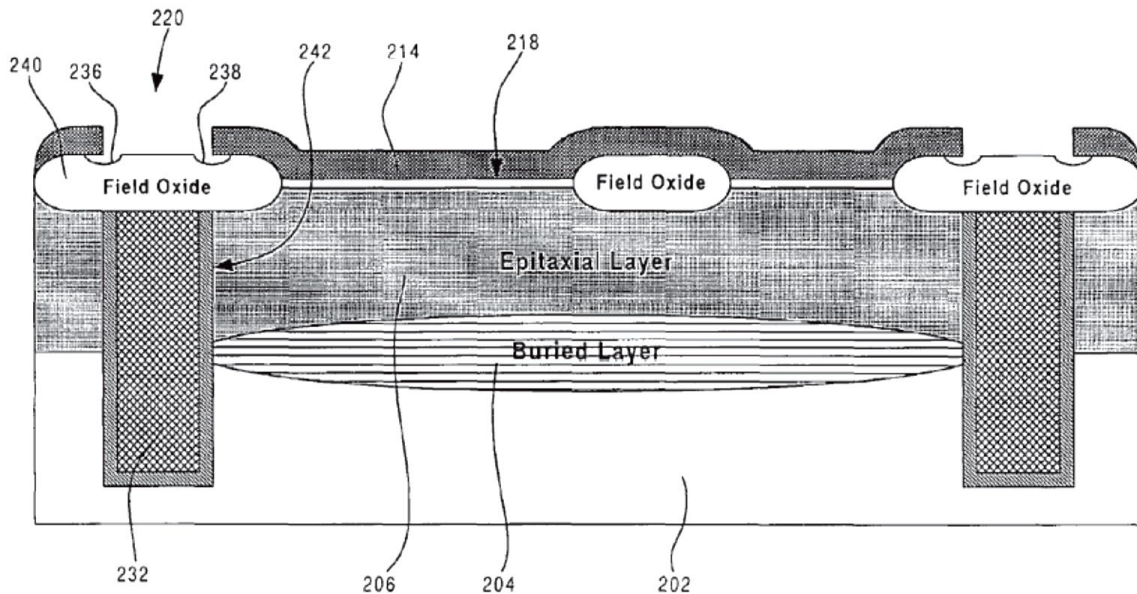


Figure 2G is cross-sectional view of a wafer processed according to an embodiment of the invention. Ex. 1004, 3:13–16. In Figure 2G, “the layer of polysilicon is etched back to depth 230 inside trench 220 to form polysilicon portion 232.” *Id.* at 6:43–44.

## 2. Koshimizu (Ex. 1005)

Koshimizu is titled “Semiconductor Device and Manufacturing Method Thereof.” Ex. 1005, code (54). Koshimizu “relates to a semiconductor device and a manufacturing technique therefor and particularly to a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor . . . ‘HBT.’” *Id.* ¶ 1.

Koshimizu describes prior techniques for forming an HBT. Ex. 1005 ¶ 2. A described problem is that wet etching of an opening through a silicon oxide film stacked on silicon nitride film etches the silicon nitride faster than the silicon oxide and thereby causes a sidewall-protrusion

of the silicon oxide into the opening. *Id.* ¶¶ 3–4. An unwanted consequence is that the protrusion interferes with subsequent epitaxial growth of insulator in the opening. *Id.* ¶ 4.

Figure 2 is reproduced below:

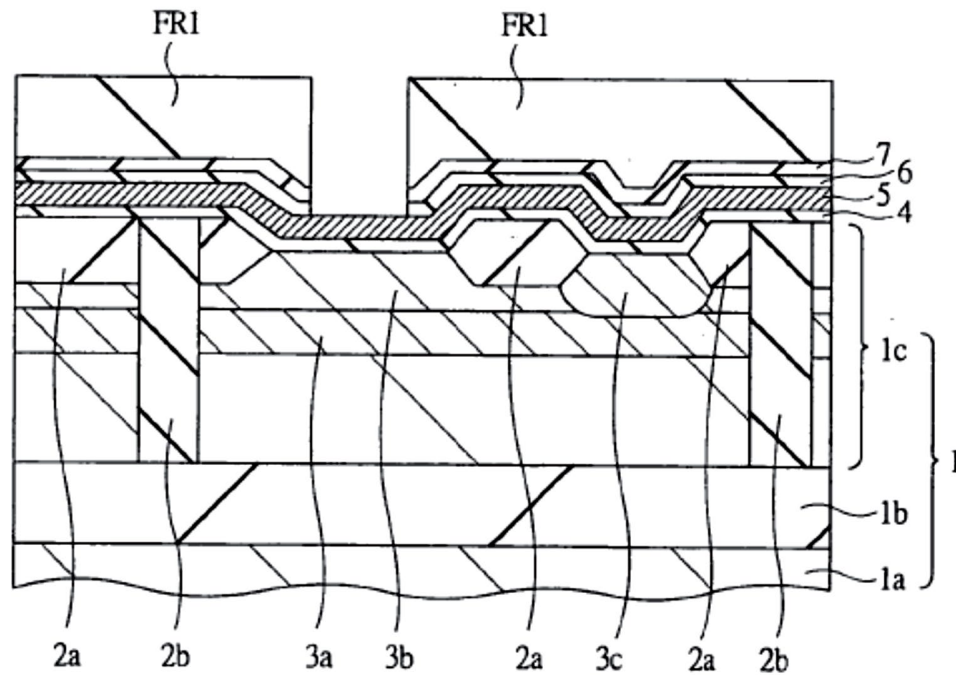


Figure 2 “is a sectional view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶ 14. To create the structure shown, a silicon oxide film 4, silicon film 5, a silicon nitride film 6, and a silicon oxide film 7 stacked onto (in this order) a substrate 1. *Id.* ¶ 53. Using photoresist FR1 patterned on the silicon oxide film 7, an accordant opening is etched down to the upper surface of the silicon film 5. *Id.* The remaining illustrated structures 1–3 include a substrate region 1 having a silicon layer 1c, silicon oxide layer 1b, and semiconductor layer 1c; an isolation region 2 having a shallow isolation silicon oxide film 2a and deep trench isolation silicon oxide film 2b; and an

HBT region 3 having an  $n^+$ -type collector embedding region 3a,  $n^-$ -type collector region 3b, and  $n^+$ -type collector extraction region 3c. *Id.*

Figure 16 is reproduced below:

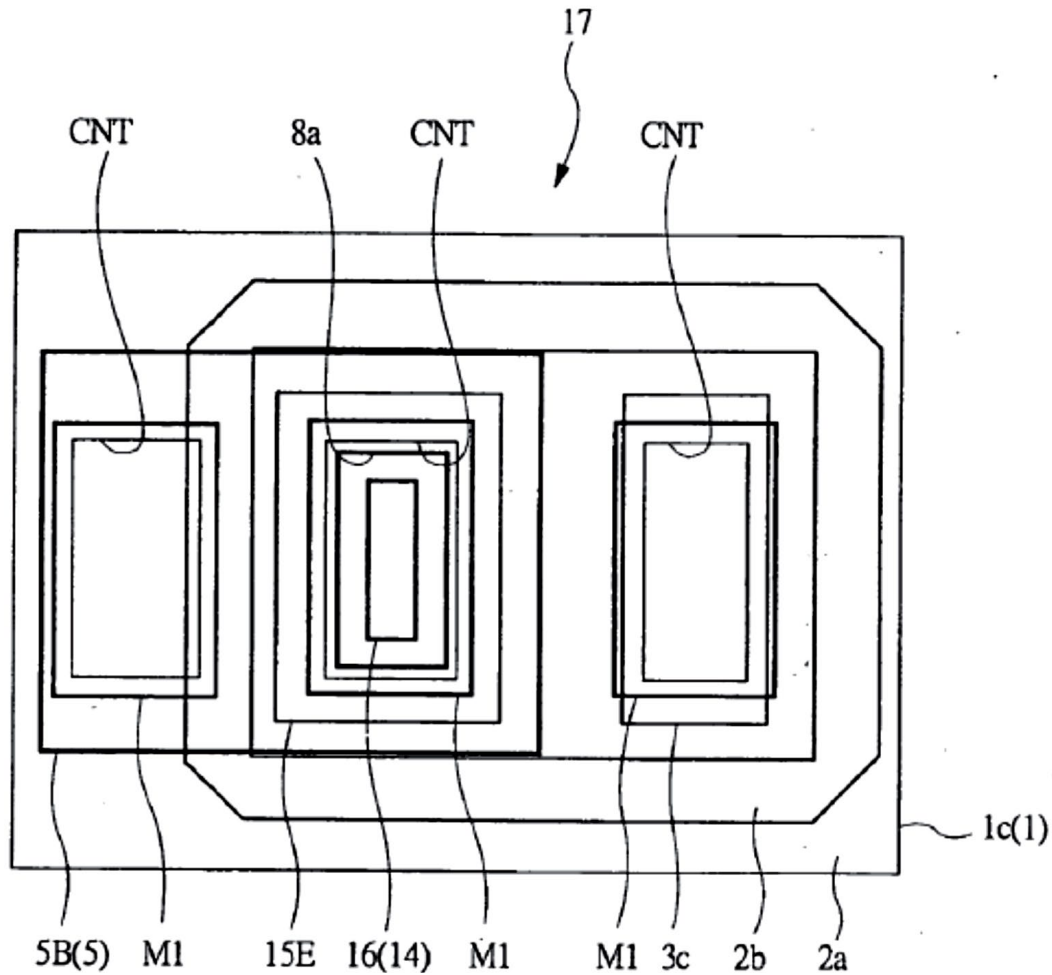


Figure 16 “is a plan view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶ 28. Contact holes (not labeled) expose a base extraction electrode 5B, emitter extraction electrode 15E, and the collector extraction region 3c of an HBT 17. *Id.* ¶¶ 59, 61. The remaining illustrated structures include conductor polycrystalline silicon film 5 (*id.* ¶ 53), wirings M1 (*id.* ¶ 60), emitter region 16 (*id.* ¶ 59), and opening portion 8a (*id.* ¶ 54).

### 3. Claim 1

Petitioner provides a limitation-by-limitation analysis of claim 1, mapping each claim limitation to the combination of Yin and Koshimizu. Pet. 28–57. Petitioner also contends that a person of ordinary skill in the art would have been motivated to combine the references, with a reasonable expectation of success. *Id.* at 23–27. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003 ¶¶ 148–159.

Patent Owner argues this challenge is deficient because Koshimizu is not analogous art to the '673 patent. PO Resp. 13–23.

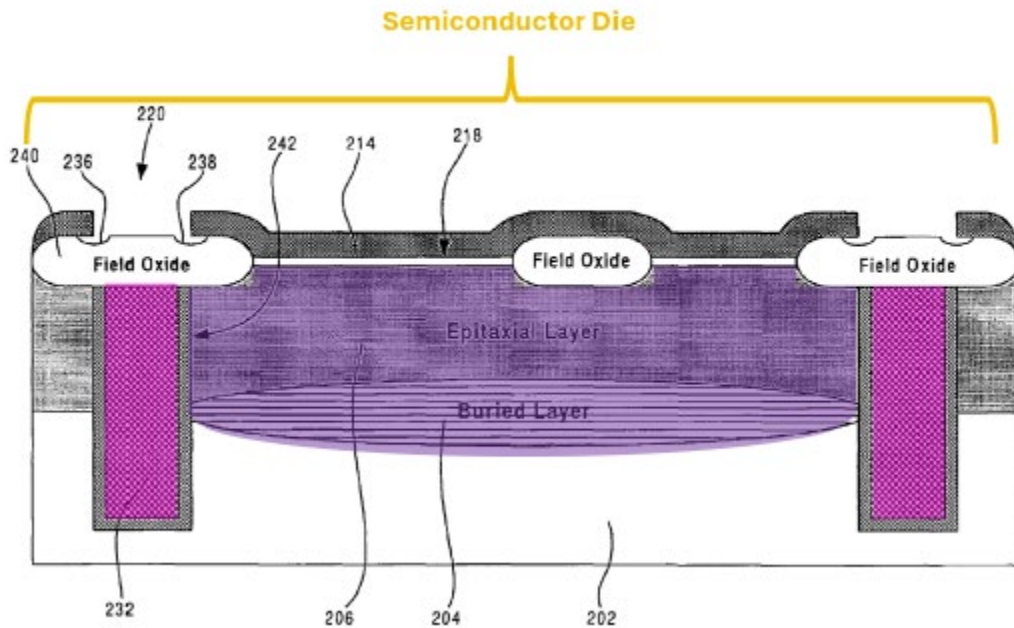
We start with Petitioner's mapping of the claim limitations<sup>8</sup> to the prior art and its motivation to combine and reasonable expectation of success arguments. We then address Patent Owner's argument that Koshimizu is not analogous art.

- a) *1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising:*

Petitioner contends that “[t]o the extent the preamble is limiting, *Yin* discloses a semiconductor die including at least one deep trench isolation region for isolating an electronic device.” Pet. 28 (citing Ex. 1003 ¶ 91). Petitioner provides the following annotated version of Yin's Figure 2G:

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<sup>8</sup> For ease of reference, we utilize Petitioner's limitation identifiers.



Pet. 28. Figure 2G is a cross-sectional view of “portions of a wafer processed according to an embodiment.” Ex. 1004, 3:13–14. Petitioner annotates Figure 2G by highlighting trench 220 in magenta and adding an orange horizontal line on top of Figure 2G with orange text “Semiconductor Die.” Pet. 28.

Petitioner contends that “trench 220 represents a deep isolation trench filled with polysilicon 232.” Pet. 28 (citing Ex. 1004, 6:29–53). Petitioner further contends that Yin’s description of Figure 2G as “the cross-section of a wafer” corresponds to the ’673 patent’s “semiconductor die.” *Id.* at 28–29 (citing Ex. 1001, 5:52–57; Ex. 1003 ¶ 91; Ex. 1004, 3:13–16). Petitioner also contends that Yin’s trench 220 “may electrically isolate, for example, a bipolar transistor,” Figure 2G shows “the bipolar transistor . . . to be surrounded by the deep isolation trench,” and “the semiconductor die hous[es] the bipolar transistor and deep isolation trench region.” *Id.* at 29 (citing Ex. 1003 ¶ 92; Ex. 1004, 1:16–27, Fig. 2G).

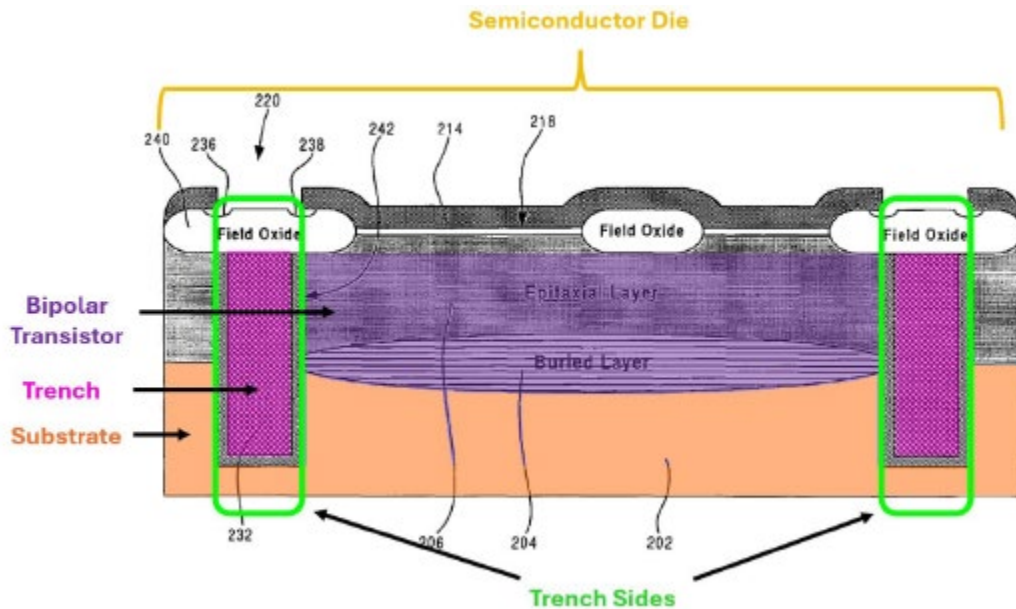
Patent Owner does not address the preamble of claim 1. *See* PO Resp. 13–23.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the subject matter of the preamble. Consequently, we need not address whether the preamble of claim 1 is limiting.

- b) 1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;*

Petitioner contends that the combination of Yin and Koshimizu teaches limitation 1[a]. Pet. 30–35.

Petitioner first contends that Yin discloses an electronic device, i.e., a bipolar transistor surrounded by deep isolation trench 220 and situated in a substrate. Pet. 30 (citing Ex. 1003 ¶ 94; Ex. 1004, 1:19–27, Fig. 2G). Petitioner argues that Yin’s Figure 2G “represents a bipolar transistor isolated by a deep isolation trench consistent with” Figures 2 and 4E of the ’673 patent. *Id.* at 30–31 (comparing Ex. 1001, Figs. 2, 4E and Ex. 1004, Fig. 2G). In support of this argument, Petitioner provides the following annotated version of Figure 2G of Yin:

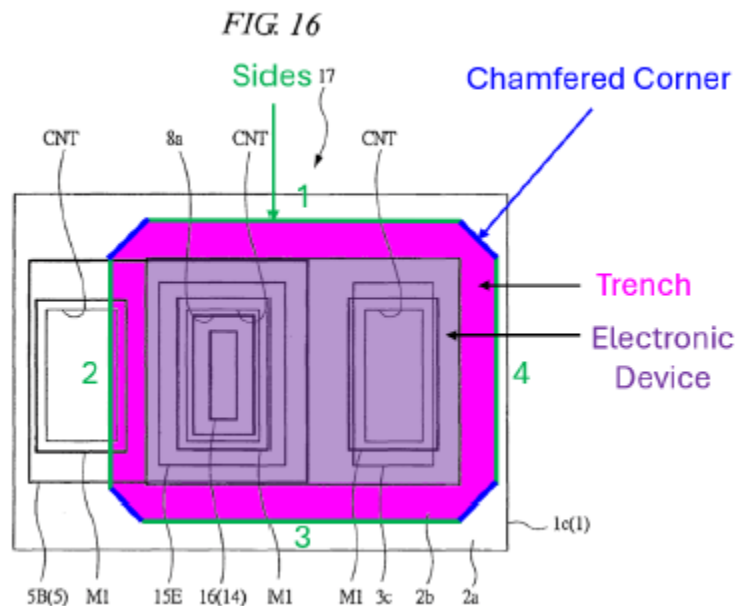


Pet. 32. Figure 2G is a cross-sectional view of “portions of a wafer processed according to an embodiment.” Ex. 1004, 3:13–14. Petitioner annotates Figure 2G by highlighting trench 220 in magenta and adding magenta text, “Trench” with a black arrow pointing to the trench, highlighting elements 204 and 206 in purple and adding purple text, “Bipolar Transistor” with a black arrow pointing to elements 204 and 206, highlighting element 202 in orange and adding orange text, “Substrate” with a black arrow pointing to element 202, adding green rectangles around trench 220 and green text, “Trench Sides” with black arrows pointing to the trench, and adding an orange horizontal line on top of Figure 2G with orange text “Semiconductor Die.” Pet. 32.

Petitioner acknowledges that Yin does not provide a top-down view of its bipolar transistor but contends that “it would have been readily understood by a [person of ordinary skill in the art] to be surrounded by a four-sided trench.” Pet. 32 (citing Ex. 1003 ¶ 95); *see also id.* at 32–33 (arguing that the two portrayed trenches in Yin’s Figure 2G “correspond to

two opposite sides of the rectangular die's four sides.” (citing Ex. 1003 ¶ 96) (citing Ex. 1007, 476)).

Next, Petitioner reproduces an annotated version of Koshimizu's Figure 16:



Pet. 35. Figure 16 “is a plan view showing a principal portion in the manufacturing process of the semiconductor device.” Ex. 1005 ¶ 28. Petitioner annotates Figure 16 by shading Koshimizu's trench magenta and adding magenta text, “Trench” with a black arrow, shading electronic device purple and adding purple text “Electronic Device” with a black arrow, adding 4 green lines around the Electronic Device and adding green text “Side” with green arrows, and adding blue lines to the corners with blue text “Chamfered Corner.” Pet. 35.

Petitioner contends that Koshimizu's “chamfered corners connect the four sides of the deep trench 2b in *Koshimizu*” and “[w]hen integrated into *Yin*'s semiconductor die, these chamfered corners would have likewise

connected the four sides of *Yin*'s deep trench isolation region in the same manner." Pet. 35 (citing Ex. 1003 ¶ 99).

Patent Owner does not address limitation [1a]. See PO Resp. 13–23.

We have reviewed Petitioner's contentions and evidence and find that the combination of *Yin* and *Koshimizu* teaches this limitation.

c) *1[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.*

Petitioner contends that the combination of *Yin* and *Koshimizu* teaches this limitation. Pet. 36–44.

Petitioner first contends that *Yin*'s "deep isolation trenches are filled with polysilicon." Pet. 36 (citing Ex. 1003 ¶ 102; Ex. 1004, 6:29–32, 6:43–44, Fig. 2F). Petitioner next contends that "*Koshimizu*'s chamfered corners considerably reduce the width of the trench at the corners where they would otherwise be the widest if left unchamfered." *Id.* at 37 (citing Ex. 1001, Fig. 1; Ex. 1003 ¶ 102; Ex. 1005, Fig. 16). According to Petitioner, an ordinarily skilled artisan "would have understood that the thickness of a layer of polysilicon within a trench at a given location will be reduced if the width of the trench at that location is likewise reduced." *Id.* (citing Ex. 1003 ¶ 103); see also *id.* at 43–44 ("*Koshimizu*'s chamfered corners reduce the width of the widest portion of the trench and cause a reduction in the thickness of the polysilicon filling them in at least the corner portions." (citing Ex. 1003 ¶ 105)).

Patent Owner does not address limitation [1b]. See PO Resp. 13–23.

We have reviewed Petitioner's contentions and evidence and find that the combination of *Yin* and *Koshimizu* teaches this limitation.

*d) Motivation to Combine and Reasonable Expectation of Success*

Petitioner contends that both Yin and Koshimizu are analogous art to the '673 patent. Pet. 8, 11. Petitioner supports this contention with the declaration testimony of Dr. Thompson. Ex. 1003 ¶¶ 70, 74.

Petitioner contends that Yin's teachings would lead a POSITA to Koshimizu's teachings because:

*Yin* does not disclose the geometry of the corners of its deep trench isolation region. See Thomson Dec. ¶ 82. Thus, a skilled artisan looking to use Yin's semiconductor die would have looked to other disclosures for a suitable corner geometry. *Koshimizu* provides that geometry, specifically teaching trenches with an unchamfered inner corner and a chamfered outer corner. See *Koshimizu*, Fig. 16, [0028]; see also *id.*, [0051]–[0061] (fully disclosing the manufacturing method and features of the same).

Pet. 23–24. Petitioner further contends that “[c]hamfered corners were beneficial not only because they improved structural stability . . . but also because they could reduce the need for overfilling” and that “*Koshimizu* is just one of many examples of a deep isolation trench with chamfered corners; these were a common feature of deep isolation trenches before the '673 Patent.” *Id.* at 24 (citing Ex. 1003, ¶ 82–84 (citing Ex. 1006, Figs. 13, 25; Ex. 1008, Figs. 1, 4; Ex. 1009, 573–574; Ex. 1010, 559–562)).

Petitioner next contends that

it was known before the '673 Patent that a deep isolation trench needs to be filled with isolating material such as polysilicon or silicon oxide such that all portions of the trench, including the *widest* portions of the trench, are completely filled. Because the portions of the trench are filled at the same time, this can cause overfill over the narrowest portions of the trench. . . . It was “textbook knowledge before the '673 Patent that ‘i[f] trenches of widely varying widths are filled, the narrow ones *must be well overfilled* in order for the wider ones to be filled completely.’” . . . And chamfered corners normalize the width of the

trench's corners with the width of the trench's sides, thus minimizing the variance between their widths and the widths of the sides of the trench and reducing the need to overfill the sides of the trench.

Pet. 24 (citing Ex. 1003 ¶ 84; Ex. 1005, Fig. 16).

Petitioner argues that an ordinarily skilled artisan “would have been motivated to avoid the overfilling of trench sides in *Yin*'s deep isolation trench that would result from unchamfered corners by instead using chamfered corners” resulting in an “added benefit of improved structural stability.” Pet. 25 (citing Ex. 1003 ¶ 85). According to Petitioner combining Koshimizu and Yin “is nothing more than using a known method (chamfering a deep isolation trench) that yields a known result (e.g., a reduction in the necessary isolating material in said trench).” *Id.* (citing Ex. 1003 ¶ 85); *see also id.* (“While *Koshimizu* used silicon oxide, . . . and *Yin* uses polysilicon, . . . , to refill their respective isolation trenches, the use of a chamfer on the trench's corners improves *Koshimizu* in the same way it would improve *Yin*.” (citing Ex. 1003 ¶ 87)).

Petitioner next contends that an ordinarily skilled artisan would have had a reasonable expectation of success because “[c]hamfering the outer corners of *Yin*'s trench would have required nothing more than an adjustment to the mask pattern that defines the outline of the trench to have chamfered corners instead of square corners.” Pet. 26 (citing Ex. 1003 ¶ 89). Petitioner further contends that “[i]t was also known in the art that 135° angle corners (i.e., chamfered), rather than 90° angle corners (i.e., unchamfered) were one solution to improve problems associated with trench refill.” *Id.* at 26–27 (citing Ex. 1003 ¶ 89).

Patent Owner does not address Petitioner’s motivation to combine and reasonable expectation of success arguments. PO Resp. 13–23; Pet. Reply 3 n.1.

We have reviewed Petitioner’s undisputed contentions and evidence and find that that an ordinarily skilled artisan would have been motivated to combine Yin and Koshimizu with a reasonable expectation of success because the combination uses a known method, chamfering the corners of a deep isolation trench with known results of not overfilling the sides of the trench and added structural stability. Ex. 1003 ¶¶ 81–89. Petitioner’s contentions are supported by the cited testimony of Dr. Thompson to which we accord substantial weight because it is supported by the disclosure of Yin, Koshimizu, Exhibit 1007 (“Wolf”), Exhibit 1008 (“Tews”), Exhibit 1009 (“Moens”), and Exhibit 1010 (“Stiffler”). *See id.*

Patent Owner’s only contention for this challenge is that Koshimizu is not analogous art to the ’673 patent. PO Resp. 13–23. Patent Owner contends that Koshimizu “is not in the same field of endeavor and . . . is not reasonably pertinent to the problem with which the ’673 Patent inventors were involved.” *Id.* at 13.

Patent Owner argues that “the ’673 Patent’s field of endeavor is “the formation of deep trench isolation regions.” PO Resp. 15 (citing Ex. 2004 ¶ 41). Patent Owner further argues that the ’673 patent states the field of invention is “isolation region formation in semiconductor substrates” and “deep trench isolation and method of forming same.” *Id.* at 13 (quoting Ex. 1001, 1:5–10, 1:45–49, 2:20–23). According to Patent Owner, the specification of the ’673 patent “provides detailed instructions on manufacturing a deep trench and filling it with polysilicon, and no

discussion of manufacturing a transistor or other device.” *Id.* at 14 (citing Ex. 1001, 5:42–9:3, Figs. 3, 4; Ex. 2004 ¶ 41).

Patent Owner next contends that an ordinarily skilled artisan “would recognize that Koshimizu’s field of endeavor is the manufacture of semiconductor devices having a hetero-junction bipolar transistor.” PO Resp. 17 (citing Ex. 2004 ¶¶ 42–48); *id.* at 16 (citing Ex. 1005 ¶ 1). Patent Owner argues that Koshimizu “describes an earlier method of manufacturing a bipolar transistor and notes several problems with the conventional technique.” *Id.* at 16 (citing Ex. 1005 ¶¶ 2–4, 45–47; Ex. 2004 ¶¶ 45–46. According to Patent Owner, the problems described in Koshimizu “are unrelated to electrical isolation or forming deep trench regions” but rather “are related to forming openings in the films lying atop the substrate as part of the process for manufacturing electrodes.” *Id.* (citing Ex. 1005 ¶¶ 3–4, 7–12, 47; Ex. 2004 ¶ 47).

Patent Owner next contends that Koshimizu “spends little space on its deep trench isolation” but “merely sets out that isolation exists, and focuses on the components of the transistor.” PO Resp. 18 (citing Ex. 1005 ¶ 52; Ex. 2004 ¶ 48). Patent Owner concedes that the ’673 patent “specifically, and repeatedly, states that it” discloses isolation trenches for “bipolar transistors”, but argues that the ’673 patent “is agnostic as to the type of device being isolated” because the repeated statements are merely “an illustrative example of the type of device that can be isolated under its invention.” *Id.* at 17–18 (citing Ex. 1001, 2:35–38, 3:51–55; Ex. 2004 ¶ 43).

Patent Owner also contends that “Petitioner’s characterization of the ’673 Patent varies based on which reference it is attempting to analogize.” PO Resp. 14; *see also id.* at 14–15 (arguing that Petitioner’s statements

concerning the field of the '673 patent are different when discussing each of Yin, Koshimizu, and Norström (citing Pet. 8, 11, 14)). Based on these purported inconsistencies,<sup>9</sup> Patent Owner contends that Petitioner fails to carry its burden to show that Koshimizu qualifies as analogous art to the '673 patent. *Id.* at 18; *see also* Sur-reply 2 (“On Reply, Petitioner still fails to define a field of endeavor for the '673 Patent, much less pick one of its three fields from the Petition.”).

Patent Owner also contends that Koshimizu is not reasonably pertinent<sup>10</sup> to the problem faced by the inventors of the '673 patent which, according to Patent Owner, “was that the prior art trenches required a thick layer of polysilicon to adequately fill them.” PO Resp. 22 (citing Ex. 1001, 1:30–34; Ex. 2004 ¶¶ 30, 53–59). Patent Owner contrasts this with Koshimizu that “does not mention polysilicon at all. Instead, Koshimizu’s deep trench is filled with silicon oxide.” *Id.* at 23 (citing Ex. 1005 ¶ 52, Ex. 2004 ¶ 55). Patent Owner argues that “silicon dioxide has different stress characteristics and different electrical characteristics.” *Id.* (citing Ex. 2004 ¶¶ 56–57). According to Patent Owner, Petitioner provides no evidence that an ordinarily skilled artisan “working to reduce polysilicon thickness would look to a reference describing silicon dioxide” and “[e]ven if a silicon dioxide reference were pertinent, Koshimizu, with its lack of description of the manufacture and fill of its trench, is not.” *Id.* (citing Ex. 2004 ¶¶ 55–57).

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<sup>9</sup> Patent Owner supports this argument with citation to *Apple, Inc. v. Gesture Tech Partners, LLC*, IPR2021-00923, Paper 27, 13–14 (PTAB Dec. 2, 2022), *affd*, 2025 WL 1584286 (Fed. Cir. June 5, 2025). PO Resp. 18–19, 20–22.

<sup>10</sup> Patent Owner argues that Petitioner “waived the use of the ‘reasonably pertinent’ test.” PO Resp. 22.

Petitioner, in turn, argues that Patent Owner ignores the broad description of the field of endeavor in both the '673 patent and *Koshimizu*. Pet. Reply 2 (citing Pet. 9–11, 14–18). Petitioner argues that Patent Owner downplays the statement in the '673 patent “that the ‘invention is generally in the field of semiconductor fabrication.” *Id.* at 2–3 (citing PO Resp. 13–15). Petitioner further argues that Patent Owner “removes a pertinent portion of *Koshimizu* by using a conveniently placed ellipsis” which “removes the words ‘to a semiconductor device and a manufacturing technique therefor’ from the quotation to *Koshimizu*’s technical field.” *Id.* at 3 (citing PO Resp. 16).

Petitioner contends that *Koshimizu* is in the same field of endeavor as the '673 patent, i.e., semiconductor devices with a deep isolation trench. Pet. Reply 4. In support of this contention, Petitioner argues that

Both the '673 Patent and *Koshimizu* describe (1) semiconductor devices (Ex. 1001 . . . , “Field of Invention”, Ex. 1005 . . . , “TECHNICAL FI[EL]D OF THE INVENTION”); (2) methods of fabricating those devices ('673 Patent, 5:42–8:45; *Koshimizu*, ¶¶ [0001]–[0003], [0044]–[0064]); and (3) the formation of deep isolation trenches to electrically isolate a bipolar device ('673 Patent, 4:4–5:41, Figs. 2, 3, 4B–4F; *Koshimizu*, Abstract, ¶ [0052], Figs. 3–16).

Pet. Reply 4.

Petitioner next contends that *Koshimizu*<sup>11</sup> is also reasonably pertinent to the problems faced by the inventors of the '673 patent. Pet. Reply 10–11. Petitioner argues that Patent Owner concedes that “one problem faced by the

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<sup>11</sup> In response to Patent Owner’s waiver argument, Petitioner argues that Patent Owner “identifies no controlling authority for its waiver theory” and argues that a petitioner “need not raise analogous art arguments in its petition *at all*.” Pet. Reply 9 (citing *Sanofi-Aventis Deutschland GmbH v. Mylan Pharms. Inc.*, 66 F.4th 1373, 1379 (Fed. Cir. 2023)).

inventors of the '673 Patent was that 'prior art trenches required a thick layer of polysilicon to adequately fill them.'" *Id.* at 10 (citing PO Resp. 22).

Petitioner next points to Dr. Thompson's testimony that "textbooks available to a [person of ordinary skill in the art] taught that the amount of polysilicon needed to fill a trench depended on the width of that trench at its widest point" and "trench geometry (including corner shape) was a known tool for improving deposition efficiency and defect avoidance in trench/sidewall structures by 2007." *Id.* (citing Ex. 1003 ¶¶ 44–45, 81–90).

For the following reasons, Patent Owner's contention that Koshimizu is not analogous art is unavailing.

For a prior art reference to qualify as analogous art, the reference must either be in the field of the applicant's endeavor or reasonably pertinent to the problem with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1447 (Fed. Cir. 1992); *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1237 (Fed. Cir. 2010) (explaining that the scope of the field of invention test is "whether the art is from the same field of endeavor, *regardless of the problem addressed.*" (emphasis added)). References are selected as being reasonably pertinent to the problem based on the judgment of a person having ordinary skill in the art. *Oetiker*, 977 F.2d at 1447 ("[I]t is necessary to consider 'the reality of the circumstances,' — in other words, common sense—in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor." (quoting *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979))). Further, in *Wyers*, the Federal Circuit directed that the scope of analogous art for the reasonably pertinent prong is to be construed broadly. *Id.* at 1238 (citing *KSR*, 550 U.S. at 402).

We find that the '673 patent broadly and explicitly states that the “Field of the Invention” is “generally in the field of semiconductor fabrication” and “[m]ore particularly, the invention is in the field of isolation region formation in semiconductor substrates.” Ex. 1001, 1:6–10.

We first turn to Patent Owner’s argument that Petitioner provides inconsistent descriptions of the field of endeavor of the '673 patent.

In connection with its summary of the '673 patent, the Petition states that the '673 patent “is directed to ‘a semiconductor die including at least one deep trench isolation region for isolating an electronic device.” Pet. 14 (citing Ex. 1001, code (57)). This description is consistent with the field of the invention explicitly set forth in the '673 patent. Further, it is consistent with Mr. Berg’s description of the field of the invention as “isolation region formation in semiconductor substrates,” “deep trench isolation and method of forming same,” and “manufacturing such a trench and filling it.” Ex. 2004 ¶ 41.

The alleged inconsistencies in the Petition argued by Patent Owner (PO Resp. 14–15) are:

- 1) The Petition argues that Yin is analogous art because “like the '673 Patent” it “is directed to a semiconductor die with a deep trench isolation region that electrically isolates an electronic device such as a bipolar transistor.” Pet. 8 (citing Ex. 1003 ¶ 70);
- 2) The Petition argues that Koshimizu is analogous art because “like the '673 Patent, it is directed to the manufacture of a silicon-based bipolar transistor employing a deep isolation region to isolate the transistor from neighboring transistors.” *Id.* at 11 (citing Ex. 1003 ¶ 74); and

- 3) The Petition argues that Norström is analogous art because “like the ’673 Patent, it is directed to the manufacture of ‘bipolar semiconductor devices, in particular bipolar transistor and semiconductor diodes, which are electrically isolated or confined by trenches.” *Id.* at 14 (citing Ex. 1003 ¶ 77).

Contrary to Patent Owner’s argument that Petitioner is providing differing statements of the field of endeavor of the ’673 patent, the cited statements show Petitioner is arguing the descriptions provided in Yin, Koshimizu, and Norström of their respective fields are all “like” the broad description of the field in the ’673 patent. Further, while there may be some semantic distinctions, all of these statements are consistent with the field of invention stated on page 14 of the Petition as well as the broad description of the field stated in the ’673 patent. Because we find that the Petition has in fact provided a description of the field of the ’673 patent and *has not* provided inconsistent descriptions thereof, we need not reach Patent Owner’s arguments based on the *Gesture* case.

Koshimizu discloses that its “invention relates to a semiconductor device and a manufacturing technique therefor[e] and particularly to a technique effectively applied to a semiconductor device having a hetero-junction bipolar transistor . . . and to a manufacturing method for the semiconductor device.” Ex. 1005 ¶ 1. Koshimizu’s device includes “deep trench isolation.” *Id.* ¶ 52. Further, it discloses a trench with chamfered corners. *Id.* at Fig. 16.

When evaluating whether the references are in the same field of endeavor, we look to “explanations of the subject matter in the patent application, including the embodiments, function, and structure of the

claimed invention.” *Netflix, Inc. v. DivX, LLC*, 80 F.4th 1352, 1359 (Fed. Cir. 2023) (citations omitted). Further “[t]he field of endeavor is ‘not limited to the specific point of novelty, the narrowest conception of the field, or the particular focus within a given field.’” *Id.*

In this case, Patent Owner and its declarant, Mr. Berg, admit that Koshimizu is directed to “manufacturing a bipolar transistor” and specifically teaches forming “a deep trench isolation 2b.” PO Resp. 16–17; Ex. 2004 ¶¶ 45, 48 (citing Ex. 1005 ¶¶ 2–3, 52). Based on the undisputed disclosure of Koshimizu, we find that Koshimizu is analogous art because it is in the same field of endeavor as the ’673 patent i.e., Koshimizu is “generally in the field of semiconductor fabrication” and “[m]ore particularly, the invention is in the field of isolation region formation in semiconductor substrates.” Ex. 1001, 1:6–10; Ex. 1003 ¶ 74.

Patent Owner’s argument (PO Resp. 17–18) that the ’673 patent and Koshimizu are directed to solving different problems is unavailing because “[u]nlike the reasonable-pertinence test, the field of endeavor test does not look to the problem that the patent purports to address . . . It is enough that the prior art reference falls within the relevant field of endeavor of the patent-in-suit.” *Netflix*, 80 F.4th at 1359 (citations omitted).

Because of the finding that Koshimizu is in the same field of endeavor as the ’673 patent, it is not necessary for us to reach the question of whether Koshimizu is a reasonably pertinent reference.

*e) Summary of Claim 1*

After consideration of Petitioner’s contentions and evidence in light of Patent Owner’s contentions, and for all the foregoing reasons, we determine

that Petitioner establishes by a preponderance of the evidence that claim 1 is obvious over the combination of Yin and Koshimizu.

4. *Claim 10*<sup>12</sup>

For independent claim 10, Petitioner relies on its contentions for claim 1 for substantially similar limitations in claim 10. Pet. 55. Patent Owner does not address claim 10 apart from its contentions for claim 1 discussed above. *See generally* PO Resp.

For the same reasons discussed above for claim 1, we determine that Petitioner establishes by a preponderance of the evidence that claim 10 is obvious over the combination of Yin and Koshimizu.

5. *Claims 2, 11*

Claim 2 depends from claim 1 and recites “wherein a trench corner width at said at least one trench chamfered corner is less than a trench side width along said plurality of side.” Ex. 1001, 9:48–50. Claim 11 depends from claim 10 and contains a substantially similar limitation. *Id.* at 10:30–33.

Petitioner relies on the same contentions for claims 2 and 11. Pet. 44–47, 56. Petitioner contends that Koshimizu discloses chamfered corners having “less width than the trench side width to which they connect.” Pet. 45 (citing Ex. 1005, Fig. 16; Ex. 1003 ¶ 109). Petitioner further contends that having “a lower trench corner width than trench side width was not uncommon before the ’673 Patent.” *Id.* (citing Ex. 1008, Fig. 7). According

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<sup>12</sup> Claim 10 differs from claim 1 in that it requires “four trench chamfered corners” as opposed to “at least one trench chamfered corner.” Ex. 1001, 9:45, 10:27. This difference is carried through to claims 11–17 that depend from claim 10. *Id.* at 10:30–49.

to Petitioner, an ordinarily skilled artisan would “have understood *Koshimizu*’s disclosed chamfered corner to be sufficiently chamfered to have a trench corner width that is less than a trench side width.” *Id.* at 45–46 (citing Ex. 1003 ¶ 109).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that *Koshimizu* teaches the limitations of claims 2 and 11.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 2 and 11 are obvious over the combination of Yin and *Koshimizu*.

#### 6. *Claims 3, 12*

Claim 3 depends from claim 1 and recites “wherein said at least one trench chamfered corner comprises a portion of said trench situated between a chamfered corner of an outside wall of said trench and a corner of an inside wall of said trench.” Ex. 1001, 10:1–4. Claim 12 which depends from claim 10 contains a substantially similar limitation. *Id.* at 10:34–38.

Petitioner relies on the same contentions for claims 3 and 12. Pet. 48–49, 70. Petitioner contends that Figure 16 of *Koshimizu* “teaches the chamfering of a corner of an outside wall of a trench” that “comprises a portion of the trench and is situated between the chamfered corner of an outside wall of the trench and a corner of an inside wall of the trench.” Pet. 48 (citing Ex. 1005 ¶¶ 51–61, Fig. 16; Ex. 1003 ¶¶ 115–116); *id.* at 49 (reproducing Figure 16 of *Koshimizu* with annotations illustrating Petitioner’s contentions).

Patent Owner does not address Petitioner's contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner's contentions and evidence and find that Koshimizu teaches the limitations of claims 3 and 12.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 3 and 12 are obvious over the combination of Yin and Koshimizu.

#### 7. Claims 4, 13

Claim 4 depends from claim 1 and recites "wherein a field oxide region overlies said trench." Ex. 1001, 10:5–6. Claim 13 depends from claim 10 and contains the same limitation. *Id.* at 10:39–40.

Petitioner relies on the same contentions for claims 4 and 13. Pet. 49–50, 56. Petitioner contends that Yin's Figure 2G, shows "a field oxide region overlies its deep isolation trench." Pet. 49; *id.* at 50 (reproducing Yin's Figure 2G with annotations illustrating Petitioner's contentions) (citing Ex. 1004, 6:54–65, Fig. 2G; Ex. 1003 ¶ 118).

Patent Owner does not address Petitioner's contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner's contentions and evidence and find that Yin teaches the limitations of claims 4 and 13.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 4 and 13 are obvious over the combination of Yin and Koshimizu.

#### 8. Claims 5, 14

Claim 5 depends from claim 1 and recites "wherein said trench further comprises an oxide liner situated on an inside wall and an outside wall of

said trench.” Ex. 1001, 10:7–9. Claim 14 depends from claim 10 and contains a substantially similar limitation. *Id.* at 10:41–43.

Petitioner relies on the same contentions for claims 5 and 14. Pet. 50–51, 57. Petitioner contends that Yin’s Figure 2F shows an oxide liner 228 “situated on the inner and outer walls of trench 220.” Pet. 50–51 (reproducing Yin’s Figure 2F with annotation illustrating Petitioner’s contentions) (citing Ex. 1004 6:13–16; Ex. 1003 ¶ 121).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the limitations of claims 5 and 14.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 5 and 14 are obvious over the combination of Yin and Koshimizu.

#### 9. Claim 6

Claim 6 depends from claim 2 and recites “wherein said trench side width along said plurality of sides is approximately 1.0 micron.” Ex. 1001, 10:10–12.

Petitioner contends that Yin discloses “the side width of its trench sidewalls is approximately 1.0 micron.” Pet. 51–52 (citing Ex. 1004, 4:64–67; Ex. 1003 ¶ 124).

Patent Owner does not address Petitioner’s contentions for this claim. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the limitations of claim 6.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claim 6 is obvious over the combination of Yin and Koshimizu.

*10. Claims 7, 15*

Claim 7 depends from claim 1 and recites “wherein said semiconductor die is enclosed on a semiconductor package.” Ex. 1001, 10:13–14. Claim 15 depends from claim 10 and contains the same limitations. *Id.* at 10:44–45.

Petitioner relies on the same contentions for claims 7 and 15. Pet. 52–54, 57. Petitioner contends that Yin’s “semiconductor die is designed for a ‘Bipolar Complementary-Metal-Oxide- Semiconductor (‘BiCMOS’) process’ in which ‘deep trench isolation regions are typically formed to provide isolation between adjacent active regions of a semiconductor substrate.’” Pet. 52 (citing Ex. 1004, 1:15–19). Petitioner further contends that Yin also discloses “its ‘deep isolation trench region may electrically isolate, for example, a bipolar transistor . . . from an adjacent CMOS transistor, such as a PFET, fabricated on the same semiconductor substrate.’” *Id.* (citing Ex. 1004, 1:19–24). Petitioner further contends that “‘BiCMOS’ technology with multiple bipolar transistor devices in one semiconductor package or chip was standard use for bipolar transistor devices before the ’673 Patent.” *Id.* (citing Ex. 1012, 1–7; Ex. 1003 ¶¶ 127–128). According to Petitioner, an ordinarily skilled artisan would “have understood that *Yin*’s disclosed semiconductor die was or would be enclosed in a semiconductor package with neighboring semiconductor devices from which electrical isolation was necessary and/or desirable.” *Id.* at 52–53 (citing Ex. 1003 ¶¶ 127–128).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the limitations of claims 7 and 15.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 7 and 15 are obvious over the combination of Yin and Koshimizu.

#### *11. Claims 8, 16*

Claim 8 depend from claim 1 and recites “wherein said electronic device is a bipolar transistor.” Ex. 1001, 10:15–16. Claim 16 depends from claim 10 and contains the same limitation. *Id.* at 10:46–47.

Petitioner relies on the same contentions for claims 8 and 16. Pet. 54, 57. Petitioner contends that Yin “discloses that its ‘deep trench isolation regions may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium hetrojunction bipolar transistor[.]” Pet. 54 (citing Ex. 1004, 1:19–22; Ex. 1003 ¶ 133).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the limitations of claims 8 and 16.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 8 and 16 are obvious over the combination of Yin and Koshimizu.

#### *12. Claims 9, 17*

Claim 9 depends from claim 1 and recites “wherein said electronic device is a silicon-germanium bipolar transistor.” Ex. 1001, 10:17–18.

Claim 17 depends from claim 10 and contains the same limitation. *Id.* at 10:48–49.

Petitioner relies on the same contentions for claims 9 and 17. Pet. 54–55, 57. Petitioner contends that Yin “discloses that its ‘deep trench isolation regions may electrically isolate, for example, a bipolar transistor, such as a silicon-germanium heterojunction bipolar transistor[.]’” Pet. 54 (citing Ex. 1004, 1:19–22; Ex. 1003 ¶ 136).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Yin teaches the limitations of claims 9 and 17.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 9 and 17 are obvious over the combination of Yin and Koshimizu.

*E. Ground 2: Anticipation of  
Claims 1, 3, 5, 7, 8, 10, 12, and 14–16 by Norström*

Petitioner contends that claims 1, 3, 5, 7, 8, 10, 12, and 14–16 are anticipated by Norström. Pet. 58–71. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003.

Patent Owner argues that an ordinarily skilled artisan “would not understand Norström to disclose the claimed trench that is both ‘situated in a substrate’ and has a ‘trench chamfered corner.’” PO Resp. 23.

We begin with a brief summary of Norström. We then address the parties’ contentions.

*1. Norström (Ex. 1006)*

Norström is titled “Method of Electrical Connection Through an Isolation Trench to Form Trench-Isolated Bipolar Devices.” Ex. 1006, code (54). Norström “relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.” *Id.* at 1:7–10.

Figure 13a is reproduced below:

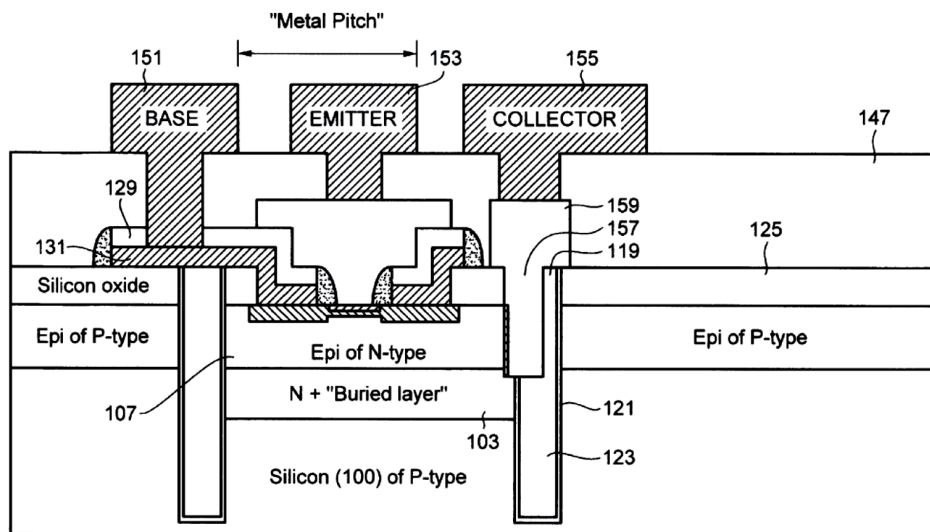


Figure 13a “is a schematic cross sectional view . . . of [a] finished NPN-transistor.” Ex. 1006, 6:24–26. Silicon oxide layer 147 is etched to form contact holes therethrough and then receive, therein, metal that forms a base plug 151, emitter plug 153, and collector plug 155. Ex. 1006, 10:66–11:6. The remaining illustrated structures include N- and P-regions 107, trenches filled 119 with isolating material 123 and having sidewalls overlaid with oxide layers 121, a buried N+ layer 103, and oxidation outer confining regions 125. *Id.* at 7:19–48.

Figure 13c is reproduced below:

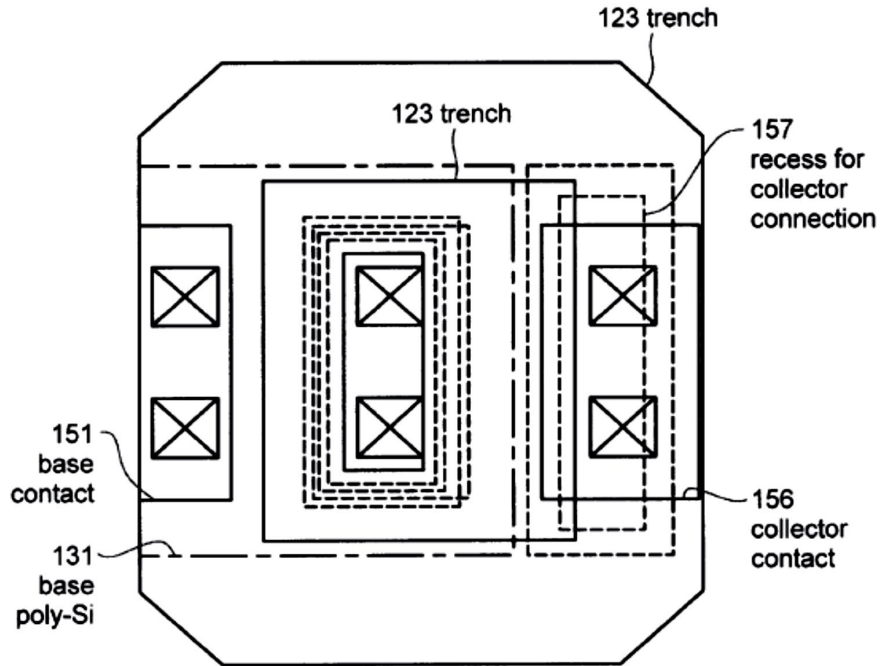


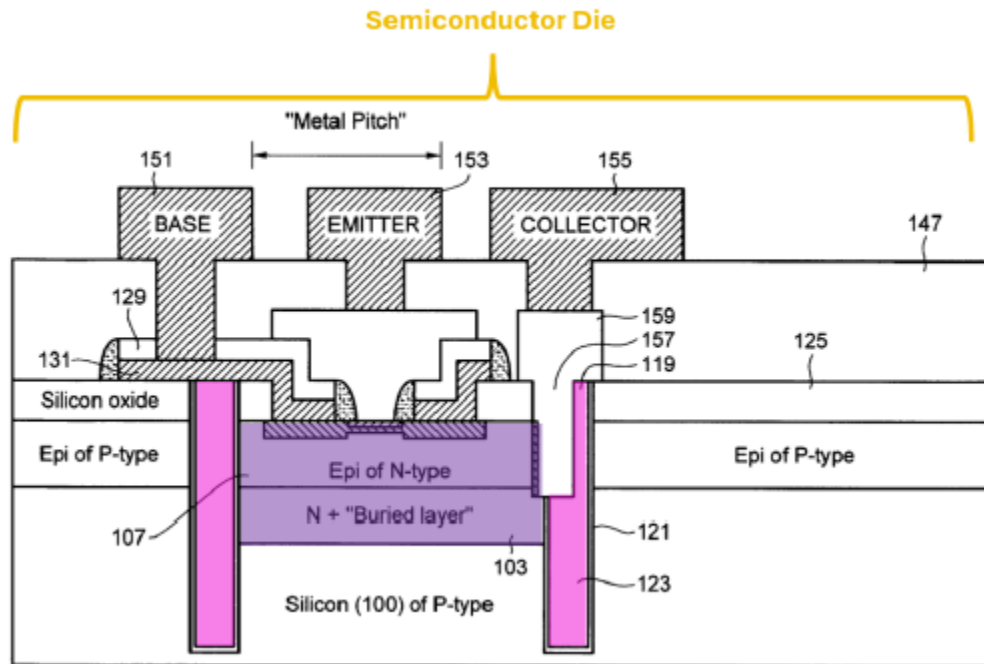
Figure 13c “is a view from above [that] schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.” Ex. 1006, 6:32–34.

## 2. Claim 1

We first summarize Petitioner’s contentions for claim 1 and then address Patent Owner’s contentions.

- a) *1[pre] A semiconductor die including at least one deep trench isolation region for isolating an electronic device, said at least one deep trench isolation region comprising*

Petitioner provides the following annotated version of Norström’s Figure 13a:



Pet. 59. Figure 13a “is a schematic cross-sectional view . . . of the finished NPN-transistor.” Ex. 1006, 6:24–26. Petitioner annotates this figure by shading in purple the bipolar transistor, shading in magenta deep trench isolation region, and adding an orange horizontal line on top with text reading “Semiconductor Die.” Pet. 59.

Petitioner contends that “*Norström* discloses that its ‘present invention relates to bipolar semiconductor devices, in particular bipolar transistors and semiconductor diodes, which are electrically isolated or confined by trenches.’” Pet. 58 (citing Ex. 1003 ¶ 149; Ex. 1006, 1:7–10).

b) *1[a] a trench situated in a substrate of said semiconductor die, said trench having a plurality of sides surrounding said electronic device, and at least one trench chamfered corner formed between and connecting said plurality of sides;*

Petitioner provides the following annotated version of Norström’s Figure 13c:

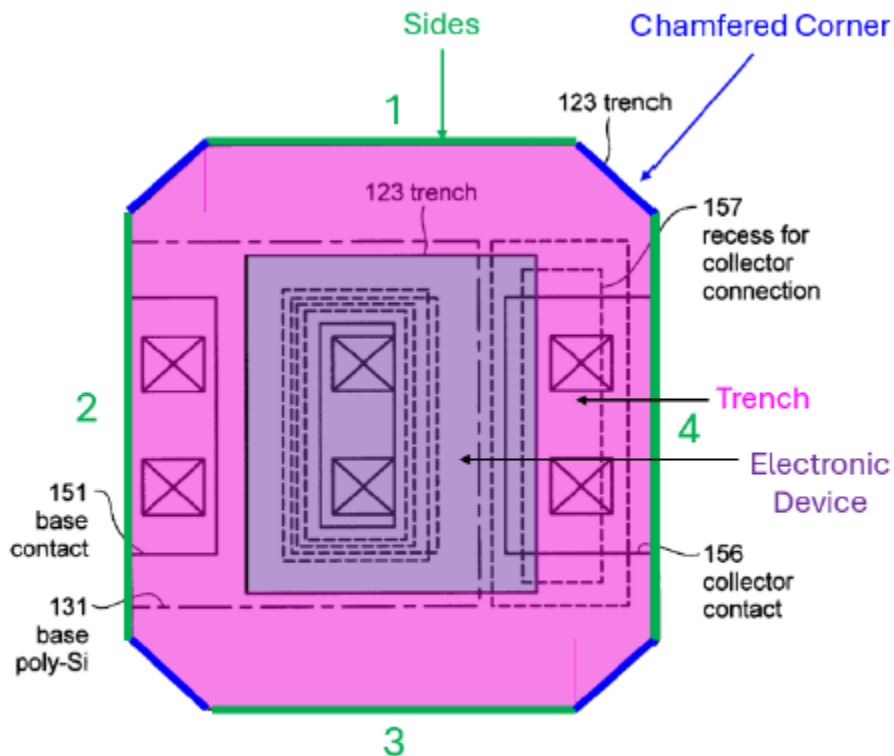


FIG. 13c

Pet. 61. Figure 13c “is a view from above, which schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.” Ex. 1006, 6:32–34. Petitioner annotates Figure 13c by shading Norström’s trench magenta and adding magenta text “Trench” with a black arrow, shading electronic device purple and adding purple text “Electronic Device” with a black arrow, adding 4 green lines around the Electronic Device and adding green text “Side” with green arrows, and adding blue lines to the corners with blue text “Chamfered Corner.” Pet. 61.

Petitioner contends that “*Norström*’s trench 123 surrounds the bipolar NPN transistor within, which is an electronic device.” Pet. 61 (citing Ex. 1003 ¶ 152; Ex. 1006, Figs. 13a, 13c). Petitioner further contends that “Figure 13c also depicts the four trench chamfered corners at the outer edge of trench 123 connecting the four sides of the trench” and that Figure 13c

shows that trench 123 “ha[s] no right angles but the flat sidewall segments form an angle of 135° to each other.” *Id.* at 61–62 (citing Ex. 1003 ¶¶ 152–153; Ex. 1006, 16:39–42, Fig. 13c). Petitioner also argues that Figure 13a shows that both the trench and NPS bipolar transistor “are situated in a substrate of silicon within the semiconductor die.” *Id.* at 62 (citing Ex. 1003 ¶ 154; Ex. 1006, 9:31–55, Fig. 13a).

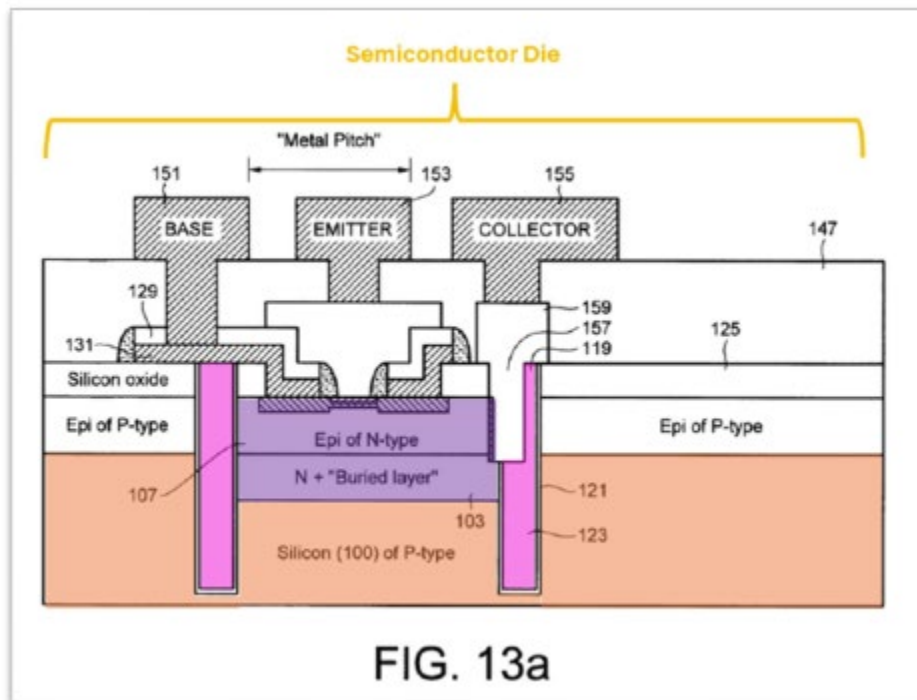
c) *I[b] wherein said at least one trench chamfered corner causes a reduction in a thickness of a polysilicon layer within said trench.*

Petitioner contends that “*Norström* discloses that its isolation trenches may be filled with polysilicon.” Pet. 63 (citing Ex. 1003 ¶ 157; Ex. 1006, 7:47–50). Relying on its reasoning from Ground 1, Petitioner further contends that an ordinarily skilled artisan “would have understood that by chamfering the outer corners of a deep isolation trench, the thickness of the polysilicon layer within the trench would be reduced at the narrower chamfered corner.” *Id.* (citing Ex. 1003 ¶ 158). Petitioner further contends that “*Norström* specifically discloses that chamfered outer trench corners improve the refill process over non-chamfered corners” similar to the ’673 patent. *Id.* at 63–64 (citing Ex. 1001, 9:6–10; Ex. 1003 ¶ 158; Ex. 1006, 16:28–36).

#### *Patent Owner’s Contentions*

Patent Owner contends that *Norström* “does not disclose the single trench claimed and required in all claims of the ’673 Patent.” PO Resp. 32.

Patent Owner reproduces Petitioner’s annotated version of Figure 13a shown on page 62 of the Petition:



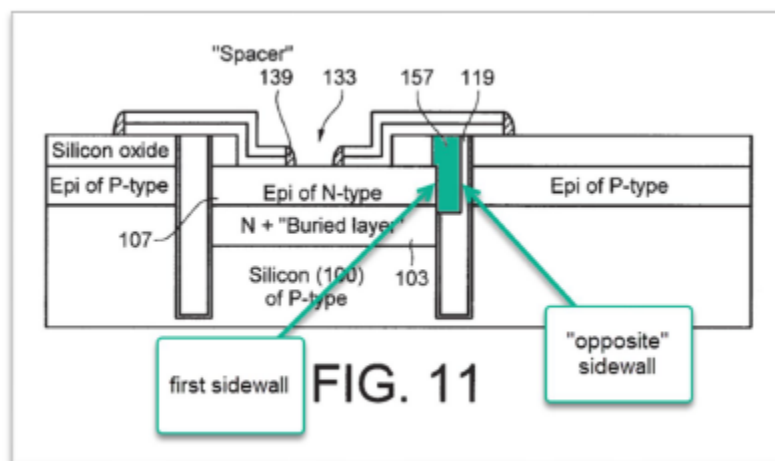
PO Resp. 24. Figure 13a “is a schematic cross-sectional view . . . of the finished NPN-transistor.” Ex. 1006, 6:24–26. Petitioner annotates this figure by shading in purple the bipolar transistor, shading in magenta deep trench isolation region, shading in orange silicon (100), and adding an orange horizontal line on top with text reading “Semiconductor Die.” Pet. 62.

Patent Owner contends that annotated Figure 13a “shows two trenches, [highlighted in magenta] one on either side of the center structure.” PO Resp. 24. Patent Owner further contends that “Norström explains repeatedly that the structures 119 in FIG. 13a are ‘trenches.’” *Id.* at 25 (citing Ex. 1006, 7:38–40, 7:60–64, 9:31–47, 10:14–15, 10:48–56, 11:35–40, Figs. 3, 8; Ex. 2004 ¶ 64). Patent Owner next contends that “[t]he few times when it uses trench 119 in the singular is when it is referring to a single trench on either: a) the side with the collector contact and

corresponding hole 157 . . . or b) the side with the emitter.” *Id.* (citing Ex. 1006, 10:14–15, 10:34–38, 10:48–56, 11:35–40; Ex. 2004 ¶ 65). According to Patent Owner, an ordinarily skilled artisan would “understand structure 119, as shown in Fig. 13a, to be a set of at least two trenches.” *Id.* at 26 (citing Ex. 2004 ¶ 66).

In connection with the reference to the label “123 trench” in Figure 13c, Patent Owner argues that Norström “discusses 123 in reference to any sort of trench only once, and in that case, it refers to trench 123 in the singular” but otherwise refers to 123 as “isolating material.” PO Resp. 29 (citing Ex. 1006, 7:44–50, 9:42–48, 16:39–42; Ex. 2004 ¶¶ 71–75).

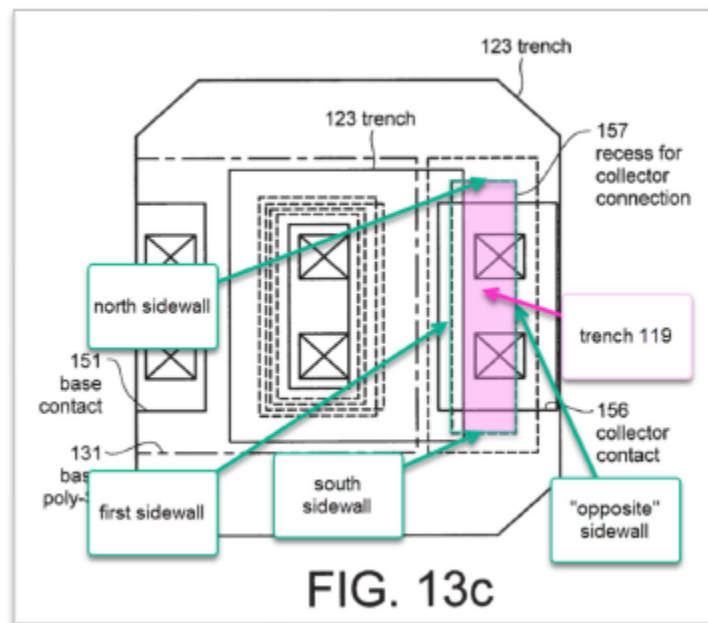
Patent Owner provides an annotated version of Norström’s Figure 11:



PO Resp. 27. Figure 11 is a schematic cross-sectional view of a device in Norström. Ex. 1006, 6:18–20. Patent Owner annotates Figure 11 by highlighting element 157 in green, adding a green box with text “first sidewall” with an arrow pointing to the lower left-side vertical edge of element 157, and a second green box with text “opposite sidewall” with an arrow pointing to the right-side vertical edge of element 157.

Patent Owner argues that Norström “explains that the collector contact hole 157 is ‘self-aligned with the sidewall of the [right side] trench.’” PO Resp. 26 (citing Ex. 1006, 10:32–56; Ex. 2004 ¶ 67). Patent Owner further argues that this alignment results in contact hole 157 “hav[ing] one of its sidewalls in direct contact with the N-doped epitaxial layer 107 and the bottom diffusion 103 and hav[ing] its *opposite sidewall located against the inner material in the trench.*” *Id.* (citing Ex. 1006, 10:48–53; Ex. 2004 ¶ 67) (emphasis added by Patent Owner).

Patent Owner next argues that Norström’s Figure 13c “shows the collector hole [157], but not the trench 119.” PO Resp. 27. Patent Owner then provides an annotated Figure 13c adding what Patent Owner argues is “the right hand trench 119 as described in Norström 10:32–56”:



PO Resp. 28 (citing Ex. 2004 ¶ 69). Figure 13c “is a view from above, which schematically shows the outlines of some layers of the finished NPN-transistor according to FIG. 13a.” Ex. 1006, 6:32-34. In this annotated version of Figure 13C, Patent Owner adds a magenta rectangle labelled

“trench 119” and labels the top edge of the rectangle as “north sidewall”, the bottom edge as “south sidewall”, the left edge as “first sidewall”, and the right edge as “opposite sidewall.” PO Resp. 28.

Patent Owner argues that what is labelled as the opposite sidewall “is aligned with the right sidewall of the trench, and the north and south sidewalls are ‘located against the inner material of the trench 119.’” PO Resp. 28 (citing Ex. 1006, 10:32–56; Ex. 2004 ¶ 70).

Patent Owner next delineates what it contends are numerous differences “between trenches 119 and trench 123” by comparing Petitioner’s annotated versions of Figures 13a and 13c. PO Resp. 29–31 (citing Ex. 1006, 10:32–56; Ex. 2004 ¶¶ 77–78; Ex. 2010, 24:17–26:19, 31:17–24).

Based on the foregoing, Patent Owner contends that “Norström does not disclose that trenches 119 have one or more trench chamfered corners.” PO Resp. 32 (citing Ex. 2004 ¶ 84). Patent Owner further contends that “Norström does not disclose that trench 123 is ‘in the substrate.’” *Id.*

Petitioner, in turn, argues that Patent Owner’s arguments are based on a false premise. Pet. Reply 12. According to Petitioner, it “does not need to tie trench 123 of Figure 13c to element 119 of Figure 13a” because Figure 13a shows trench 123 “being ‘situated in a substrate’ in the exact same manner as element 119 *because both occupy the same space in the substrate in the figure.*” *Id.* (reproducing annotated Figure 13a from Petition) (citing Pet. 62; Ex. 1003 ¶ 154). Petitioner further argues that “the Petition specifically laid out both the geometry of trench 123 and its location ‘situated in a substrate’ without *ever citing element 119.*” *Id.* at 13 (citing Pet. 60–63).

Petitioner next argues that the reason element 119 is not labelled in Figure 13c is that Norström “uses element 119 to refer to the *empty* structure of the isolating trench and element 123 to refer to the isolating filling *inside that same trench*” and “when the trench is filled . . . elements 119 and 123 occupy the same space.” Pet. Reply 14–15 (citing Ex. 1006, 9:42–48; Pet. 62 (citing Ex. 1006, 9:31–55)).

Petitioner next argues that Norström “interchangeably refers to element 119 in either the singular or plural form simply because—as Dr. Thompson explained—the cutaway view of Figure 13a shows two cut sides of the same single trench seen in Figure 13c.” Pet. Reply 16 (citing Ex. 1006, 10:14–15; Ex. 1003 ¶¶ 75–76).

#### *Analysis*

Petitioner relies on the element labelled as 123 in Norström’s Figure 13c as corresponding to the trench recited in claim 1. *See* Pet. 61 (referring to Norström’s trench 123 as shown in Figure 13c).

Norström teaches that Figures 8–13<sup>13</sup> illustrate a method of producing trench isolated bipolar components. Ex. 1006, 7:52–53. Element 119, shown in Figures 9–13a, are generally described as isolating trenches. *Id.* at 9:31–32. Norström discloses that “openings, in which isolating trenches 119 will be formed, are lithographically defined, see Fig. 9.” *Id.* at 9:31–32. In Figure 9, element 119 is labelled as “oxide isolated trench” with an arrow pointing to the rectangle on the right side only.<sup>14</sup> *Id.* at Fig. 9. Norström

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<sup>13</sup> Figures 8–13b are described as “schematic cross-sectional views.” Ex. 1006, 6:7–31.

<sup>14</sup> We find no support in Norstrom for Patent Owner’s assertion that this element represents “*right hand trench* 119 as described in Norstrom 10:32–56.” PO Resp. 27 (emphasis added).

further discloses that “trenches 119 are then thermally oxidized so that their sidewalls and bottom surfaces obtain a thin surface layer 121 of silicon oxide, *whereupon they are filled with an isolating material 123.*” *Id.* at 9:42–45 (emphasis added).

A collector contact hole 157 is formed as shown in Figure 11. Ex. 1006, 10:48–56. Collector contact hole 157 has “one of its sidewalls in direct contact with the N-doped epitaxial layer 107 . . . and its opposite sidewall located against the inner material in the trench.” *Id.* Collector contact hole 157 is subsequently filled with polysilicon creating collector contact 159. *Id.* at 10:57–63. This sequence of creating collector contact hole 157 and filling it with polysilicon is shown in Figure 11 where the unfilled collector contact hole 157 is shown and then in Figure 12 with collector contact 159 filling collector contact hole 157. *Id.* at Figs. 11, 12.

Figure 13a explicitly shows collector contact hole 157 filled with polysilicon (159) with its first sidewall in contact with epitaxial layer 107 and the opposite wall in contact with isolating material 123 in trench 119. Element 119 is shown in Figure 13a, similar to contact hole 157, filled with isolating material 123. *Id.* at 9:42–45. Figure 13a, consistent with the prior process steps, shows the result of creating openings, 157 and 119, that are later filled with material, 159 and 123. Based on this consistency, we find that Norström’s element numbers 119 and 123 represent the same structure in Figure 13a.

Figure 13c is “a view from above, which schematically shows the outlines of some layers of the finished NPN-transistor according to Figure 13a.” Ex. 1006, 6:32–34. Figure 13c, thus, represents a cross-sectional view taken from an undisclosed plane in Figure 13a and including only

“some layers of the . . . transistor . . . [shown in] Figure 13a.” Although there may be some inconsistencies between what is depicted in Figure 13a and Figure 13c from the perspective of a someone preparing manufacturing drawings, we are mindful that these are patent drawings and not detailed manufacturing drawings. Based on the process steps leading up to Figure 13a, we find that the element labelled “123 trench” in Figure 13c corresponds to the trench labelled 119 in Figures 9, 11, and 12, and labelled 119 and 123 in Figure 13a.

The crux of Patent Owner’s argument is that the cross-section view shown in Figure 13a can be interpreted as showing two isolation trenches 119, i.e., one represented by the rectangle on the right labelled with both 119 and 123 and the second represented by the rectangle on the left that is not designated with either element number 119 or 123.

We initially note that Petitioner’s position that Norström discloses one trench surrounding the electronic device is consistent with the portrayal of the drawings in the Specification of the ’673 patent. Figure 2 shows a top view of the device with one isolation trench surrounding the electronic device. Ex. 1001, Fig. 2. Figure 4E is a cross-section, similar to Norström’s Figure 13a, depicting the two-sides of the isolation trench. *Id.* at Fig. 4E.

Patent Owner’s description of Figure 11 is consistent with the disclosure of Norström that one sidewall of collector contact hole 157 contacts the N-doped epitaxial layer 107 and the opposite sidewall is located against the inner material of the trench. PO Resp. 26–27. As discussed above, the inner material of the trench is isolating material 123. Patent Owner’s description of Figure 11 is also consistent with Figure 13a which

shows that the opposite sidewall of collector contact hole 157 located against isolating material 123 inside of trench 119.

Patent Owner adds what it argues is “trench 119” to Figure 13c aligned with collector contact hole 157 and labels the four sidewalls of collector contact hole 157. PO Resp. 28. However, Patent Owner’s description of the interplay between the sidewalls of collector hole 157 and trench 119 is not consistent with its description of Figure 11 or with Figure 13a. Patent Owner argues that the “first (left) sidewall” of collector contact hole 157 “is aligned with the epitaxial layer 107” and the “opposite (right sidewall) is aligned with the right sidewall of the trench.” *Id.* Patent Owner argues that “the north and south sidewalls”<sup>15</sup> are “located against the inner material of the trench 119.” *Id.* As can be seen from Patent Owner’s annotated Figure 11 (PO Resp. 27), collector contact hole 157 *is not* aligned with the opposite sidewall of trench 119 and there is no disclosure in Norström of north and south sidewalls at all, let alone in contact with the inner material of trench 119. Consequently, Patent Owner’s argument that Norström discloses a second trench 119, as shown in its annotated Figure 13c, in addition to the filled trench identified with numeral 123 shown in original Figure 13c, is speculation unsupported by the disclosure of Norström and entitled to little, if any weight.

We find that Norström discloses that “the outer side-walls of the trench 123 shown in FIG 13c have no right angles but the flat sidewall segments form an angle of 135° to each other.” Ex. 1006, 16:39–42. Patent Owner does not dispute that trench 123 as shown in Figure 13c has

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<sup>15</sup> Our review of Norstrom reveals that the terms “north sidewall” or “south sidewall” of trench 119 do not appear in Norstrom.

chamfered corners. *See generally* PO Resp.; *see* Pet. Reply 4. We find that Norstom's Figure 13a discloses that trench 123 is situated in substrate "Silicon (100)." Patent Owner does not dispute that Figure 13a shows trench 123 situated in a substrate. *See generally* PO Resp.; *see* Pet. Reply.

#### *Summary of Claim 1*

We have reviewed Petitioner's evidence and contentions for claim 1 which we find to be persuasive. Because Patent Owner does not dispute that trench 123 has chamfered corners and is situated in a silicon substrate, we find that Norström discloses every limitation recited in claim 1.

For the foregoing reasons, after reviewing Petitioner's contentions and evidence in light of Patent Owner's contentions, we determine that Petitioner has shown by a preponderance of the evidence that claim 1 is anticipated by Norström.

#### *3. Claim 10*

For independent claim 10, Petitioner relies on its contentions for claim 1 for substantially similar limitations in claim 10. Pet. 69–70. Patent Owner does not address claim 10 apart from its contentions for claim 1 discussed above. *See generally* PO Resp.

For the same reasons discussed above for claim 1, we determine that Petitioner establishes by a preponderance of the evidence that claim 10 is anticipated by Norström.

#### *4. Claims 3 and 12*

For claims 3 and 12, Petitioner refers to its contentions for limitation 1[a]. Pet. 65–66, 70. In particular, Petitioner adds annotations to Figure 13c showing the alleged "corner of an inside wall" and "chamfered corner of an

outside wall.” *Id.* at 66 (citing Ex. 1003 ¶ 161; Ex. 1006, 16:28–36, Fig. 13c).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Norström discloses the limitations of claims 3 and 12.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 3 and 12 are anticipated by Norström.

#### 5. *Claims 5 and 14*

Petitioner relies on the same contentions for claims 5 and 14. Pet. 66–67, 71.

Petitioner contends that Norström’s “semiconductor die depicted in Figures 13a and 13c contains a thin surface layer of silicon oxide on their sidewalls.” Pet. 67 (citing Ex. 1006, 9:42–44). According to Petitioner, an ordinarily skilled artisan “would have understood this ‘thin surface layer . . . of silicon oxide’ to be an oxide liner.” *Id.* (citing Ex. 1001, 3:39–50; Ex. 1003 ¶ 164).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Norström discloses the limitations of claims 5 and 14.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 5 and 14 are anticipated by Norström.

6. *Claims 7 and 15*

Petitioner relies on the same contentions for claims 7 and 15. Pet. 68, 71.

Petitioner contends that the subject matter of Norström is “bipolar transistors manufactured on ‘the same silicon plate’ that can be ‘isolated from each other by areas comprising deep P-diffusions, which extend through the epitaxial layer down to the inner or interior material of the silicon plate, i.e., the substrate, which in these cases is silicon of P-type.” Pet. 68 (citing Ex. 1003 ¶ 167; Ex. 1006, 1:29–34). According to Petitioner, an ordinarily skilled artisan “would have understood the silicon plate to be the semiconductor package on which multiple bipolar transistor—as well as the semiconductor die they are printed on—are housed next to each other.” *Id.* (citing Ex. 1003 ¶ 67).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Norström discloses the limitations of claims 7 and 15.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 7 and 15 are anticipated by Norström.

7. *Claims 8 and 16*

Petitioner relies on the same contentions for claims 8 and 16. Pet. 69, 71.

Petitioner contends that Norström’s Figure 13 “depicts an NPN-type bipolar transistor with deep isolation trenches electrically isolating the

transistor.” Pet. 69 (citing Ex. 1003 ¶ 170; Ex. 1006, 1:7–10, 6:23–34, 8:50–11:40).

Patent Owner does not address Petitioner’s contentions for these claims. *See generally* PO Resp.

We have reviewed Petitioner’s contentions and evidence and find that Norström discloses the limitations of claims 8 and 16.

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 8 and 16 are anticipated by Norström.

*F. Ground 3: Obviousness of  
Claims 7 and 15 by Norström*

Petitioner alternately argues that claims 7 and 15 are obvious over Norström. Pet. 71–72 (citing Ex. 1003 ¶ 180).<sup>16</sup> Petitioner relies on the same contentions for both claims 7 and 15. *See id.* at 73.

Petitioner argues that “[t]he primary purpose of a deep isolation trench is to isolate a device—in this case, a bipolar transistor—from neighboring devices on the same semiconductor package.” Pet. 72 (citing Ex. 1003 ¶ 181). Petitioner contends that “[s]emiconductor devices such as *Norström*’s isolated bipolar transistor are customarily used in semiconductor wafers . . . which are in turn customarily integrated into packages for use in computing applications—and they had been for decades before the ’673 Patent.” *Id.* (citing Ex. 1003 ¶ 181 (citing Ex. 1007, 1–5)). According to Petitioner, an ordinarily skilled artisan would have had a reasonable expectation of success because “packaging a die was a common practice . . . in a package made out

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<sup>16</sup> As discussed above for Ground 2, we determine that Petitioner shows that claims 1 and 10 and are anticipated by Norstrom

of plastic or other commonly available materials” and would have “found it obvious to use *Norström*’s semiconductor die in an application enclosing it in a semiconductor package with multiple similar or identical semiconductor devices.” *Id.* at 72–73 (citing Ex. 1003 ¶ 182).

Patent Owner does not directly address Petitioner’s contentions for claims 7 and 15 in this challenge but argues that Ground 3 does not cure the deficiencies of Ground 1. PO Resp. 20–21.

We have reviewed Petitioner’s contentions and evidence and alternatively determine that Petitioner shows by a preponderance of the evidence that claims 7 and 15 would have been obvious over *Norström*.

### III. CONCLUSION<sup>17</sup>

Weighing the competing evidence and testimony, we determine that Petitioner establishes by a preponderance of the evidence that the Challenged Claims of the '673 patent are unpatentable.

In summary:

| <b>Claim(s)</b>                     | <b>35<br/>U.S.C.<br/>§</b> | <b>Reference(s)/<br/>Basis</b> | <b>Claim(s)<br/>Shown<br/>Unpatentable</b> | <b>Claim(s)<br/>Not Shown<br/>Unpatentable</b> |
|-------------------------------------|----------------------------|--------------------------------|--------------------------------------------|------------------------------------------------|
| 1–17                                | 103(a)                     | Yin, Koshimizu                 | 1–17                                       |                                                |
| 1, 3, 5, 7, 8,<br>10, 12, 14–<br>16 | 102                        | Norström                       | 1, 3, 5, 7, 8,<br>10, 12, 14–16            |                                                |
| 7, 15                               | 103(a)                     | Norström                       | 7, 15                                      |                                                |
| <b>Overall<br/>Outcome</b>          |                            |                                | 1–17                                       |                                                |

### IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–17 of the '673 patent have been shown by a preponderance of the evidence to be unpatentable; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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<sup>17</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

IPR2024-01403  
Patent 7,772,673 B1

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**CERTIFICATE OF SERVICE**

A copy of Patent Owner's Notice of Appeal is being served via email on Petitioner's attorneys of record on the 10th day of April, 2026, the same day as the filing of the above-identified document in the United States Patent and Trademark Office/Patent Trial and Appeal Board, by serving Petitioner's correspondence address of record with the USPTO as follows:

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