

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01404
U.S. Patent No. 9,147,609

**DECLARATION OF DR. SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 9,147,609**

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I. INTRODUCTION

1. I, Scott E. Thompson, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”) in connection with an *inter partes* review (IPR) of U.S. Patent No. 9,147,609 (“the ’609 patent”) (Ex. 1001). I have prepared this declaration in connection with Samsung’s Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1-18 of the ’609 patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’609 patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-18 of the ’609 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of October 7, 2011), it is my opinion that claims 1-18 of the ’609 patent would have been anticipated and/or obvious based on the grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '609 patent and the related prior art.

8. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of semiconductor devices.

9. I received my Bachelor of Electrical Engineering with Highest Honors from the University of Florida in 1987. I also received my Master of Science of Electrical Engineering in 1988 and my Ph.D. in Electrical Engineering in 1992, both from the University of Florida. My Ph.D. was funded by the Semiconductor Research Corporation. My Ph.D. dissertation studied CMOS integrated circuits, and I did extensive measurements and fabrication of CMOS test structures. My

Ph.D. dissertation earned a best paper award from the Semiconductor Research Corporation and a Best Ph.D. award from the University of Florida.

10. In 1992, after receiving my Ph.D., I joined Intel working on research and development of CMOS integrated circuits. From 1992 to 2004, I worked in Integrated Circuit development and semiconductor manufacturing. During this time, I managed the development of several integrated circuit manufacturing technologies for Intel including a 90 nanometer¹ and 130 nanometer² technologies.

11. These semiconductor manufacturing technologies used CMOS transistors, Copper interconnects and ball/pad connections. I won several Intel Achievement Awards for this work (Intel's highest award).

12. In 2000, I was promoted to Director of Semiconductor Technology Development in the Technology and Manufacturing Group at Intel. In that role, I was responsible for current and next-generation technology for integrated circuits.

¹ See S. Thompson et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 /spl mu/m/sup 2/ SRAM cell," Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 61-64, doi: 10.1109/IEDM.2002.1175779.

² See S. Thompson et al., "130nm Logic Technology Featuring 60nm Transistors, Low-K Dielectrics and Cu Interconnects" (<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=0691ee478ab78508ef236ccb63fc3a04660f2850>).

In that role I managed different areas including transistor technology, interconnects, integrated circuit package integration, integrated circuit yield, in-line defect metrology, and strategic long ranges plans for semiconductor technology. The Intel Technology and Manufacturing Group manufactured billions of dollars of CMOS integrated circuits each year. In 2002, I was appointed to the position of Intel Fellow, which is the highest technical position at Intel, and awarded for outstanding technical achievement both within Intel and industry. In that Intel role, I managed the development and manufacturing of the most advanced CMOS integrated circuits in the semiconductor industry—from 2000 to 2004, Intel surpassed IBM in integrated circuit development and became the industry leader. My team and I presented this work at many international conferences and invited talks and short courses.

13. Since 2004, I have been a professor of electrical and computer engineering at the University of Florida. I was granted tenure and promoted to full professor in 2006. During my teaching career, I developed graduate level courses on advanced semiconductor chip design, semiconductor manufacturing, and packaging technology (e.g., chip stacking). I also teach a graduate level course on the chip technology used for CPU, DRAM, GPU, image sensors, and 2D and 3D image sensor processing. My current research areas include modeling and reliability integrated circuits. I currently have a Research Contract with Texas

Instruments on how package balls and pads introduce mechanical stress and shift the electrical characteristics of integrated circuits. My research in advanced chip technology at the University of Florida has been funded by contracts worth \$4M. I have supervised approximately 20 Ph.D. candidates on topics related to CMOS integrated circuits and have won several University of Florida teaching awards.

14. In 2009, I founded SuVolta, a company that developed ultra-low power chip technology for image sensors, system-on-chip microchips, radio frequency integrated circuits, memory, CPUs, image sensors processors, and other chips. The technology developed by SuVolta was sold to Fujitsu in 2015 and was used in the commercial production of Milbeaut image sensor processors. The technology allowed Fujitsu to lower the power consumption of the image sensor processor by 50%. Working with Fujitsu, we also developed CMOS chips that operated at ultra-low power and operate at less than 0.5V power supply. SuVolta received several awards and honors: (1) 2011 EuroAsia IC Industry Award for start-ups; (2) 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology; and (3) 2014 TiE 50 Top Startup. SuVolta was granted about 80 patents directed to low power transistor structures and integrated circuits on which I am a named inventor.

15. In 2006, I was elected as an IEEE Fellow for Advancing Fabrication of nanoscale MOSFET. In 2008, I received the Semi Award North America for Development of Strained Silicon Transistors.

16. Since 2005, I have worked as a consultant for leading companies in the semiconductor and computer chip industry, including Applied Materials, Cypress Semiconductor, Qualcomm, SanDisk, and Taiwan Semiconductor. I am the author of over 60 papers and one book related to semiconductors and am a named inventor on over 100 granted patents directed to integrated circuits and transistor structures.

17. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

18. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,147,609 to Jebory et al. (“’609 patent”)
Ex. 1003	Prosecution History of the ’609 patent (downloaded from Public PAIR)
Ex. 1004	U.S. Patent Publication No. 2009/0278237 to Cooney, III et al., filed May 6, 2008, and published November 12, 2009 (“ <i>Cooney</i> ”)

Exhibit	Description
Ex. 1005	U.S. Patent Publication No. 2003/111733 to Pogge et al., filed December 19, 2001, and published June 19, 2003 (“ <i>Pogge</i> ”)
Ex. 1006	U.S. Patent Publication No. 2006/0027934 to Edelstein et al., filed October 3, 2005, and published February 9, 2006 (“ <i>Edelstein</i> ”)
Ex. 1007	U.S. Patent Publication No. 2011/0304026 to Tsui et al., filed June 14, 2010, and published December 15, 2011 (“ <i>Tsui</i> ”)
Ex. 1008	U.S. Patent Publication No. 2011/0159690 to Chandrashekar et al., filed January 28, 2011, and published June 30, 2011 (“ <i>Chandrashekar</i> ”)
Ex. 1009	U.S. Patent Publication No. 2011/0193241 to Yen et al., filed February 9, 2011, and published August 11, 2011 (“ <i>Yen</i> ”)
Ex. 1010	U.S. Patent Publication No. 2011/0057319 to Dean, Jr. et al., filed September 9, 2009, and published March 10, 2011 (“ <i>Dean</i> ”)
Ex. 1011	U.S. Patent Publication No. 2010/0032843 to Chen et al., filed August 5, 2008, and published February 11, 2010 (“ <i>Chen</i> ”)
Ex. 1012	KR 10-2010-0011480, filed on July 25, 2008, and published February 3, 2010
Ex. 1013	Certified English language translation of KR 10-2010-0011480, filed on July 25, 2008, and published February 3, 2010 (“ <i>Kim</i> ”)
Ex. 1014	Scott R. Stiffler et al., The Effect of Trench Corner Shapes on Local Stress Fields: A Three-Dimensional Finite Element Modeling Study, IEEE Transactions on Electron Devices, March 1993 (“ <i>Stiffler</i> ”)

Exhibit	Description
Ex. 1016	U.S. Patent No. 8,237,288 to Farooq et al. (" <i>Farooq</i> ")
Ex. 1017	U.S. Patent Publication No. 2012/0139127 to Beyne, filed December 2, 2011, and published June 7, 2012 (" <i>Beyne</i> ")
Ex. 1018	U.S. Patent Publication No. 2011/0237073 to Dao et al., filed March 26, 2010, and published September 29, 2011 (" <i>Dao</i> ")
Ex. 1021	U.S. Patent Publication No. 2009/0140395 to Davis et al., filed December 4, 2007, and published June 4, 2009 (" <i>Davis</i> ")
Ex. 1022	U.S. Patent Publication No. 2009/0302480 to Birner et al., filed June 6, 2008, and published December 10, 2009 (" <i>Birner</i> ")
Ex. 1023	U.S. Patent Publication No. 2008/0318361 to Han et al., filed July 13, 2007, and published December 25, 2008 (" <i>Han</i> ")
Ex. 1024	U.S. Patent Publication No. 2010/0171226 to West et al., filed December 29, 2009, and published July 8, 2010

V. LEGAL STANDARDS

19. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In

preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

20. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

21. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

22. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-18 of the '609 patent from the perspective of a person of ordinary skill in the art at the '609 patent's earliest claimed priority date in 2011, as described in more detail below.

23. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

24. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

25. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

26. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

27. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a

printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

28. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

29. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

30. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;

- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '609 patent.

31. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is October 7, 2011. My opinions would not change if I assumed a later date of invention.

32. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

33. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

34. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

35. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious

combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

36. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

37. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to

whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

38. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

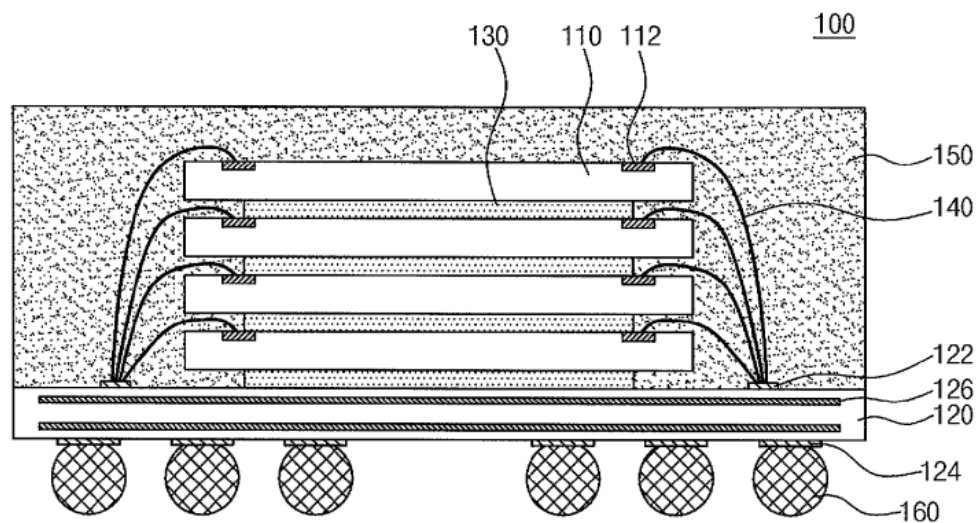
A. Through Silicon Vias (TSVs)

39. Traditionally, wire bonding is used to establish electrical interconnects between semiconductor chips. *Tsui* (Ex. 1007), ¶[0003]. However, wire bonding requires “greater in-plane size and out-of-plane size.” *Id.* To greatly reduce the 3D structure and to utilize a multilayer stacked structure, through-silicon via (TSV) technology is used instead “to provide the electrical interconnect and to provide mechanical support.” *Id.* Because the TSVs are fabricated directly in a silicon chip, the TSVs can “link bond pads on the top surface of the component with bond pads on the bottom surface of the component.” *Id.* This

forms “a conducting path along a vertical direction,” which allows multiple components to be “stacked and bonded together.” *See, e.g., Yen* (Ex. 1009), ¶[0005]; *Tsui*, ¶[0003].

40. For example, the following Figure 1 shows a traditional wire bonding package structure 100 “in which at least two semiconductor chips 110 are stacked on a substrate 120 by an adhesive 130 and the bonding pad 112 of each semiconductor chip 110 and the connection terminal 122 of the substrate 120 are electrically connected through a metal wire 140.” *Han* (Ex. 1023), ¶[0007].

FIG. 1



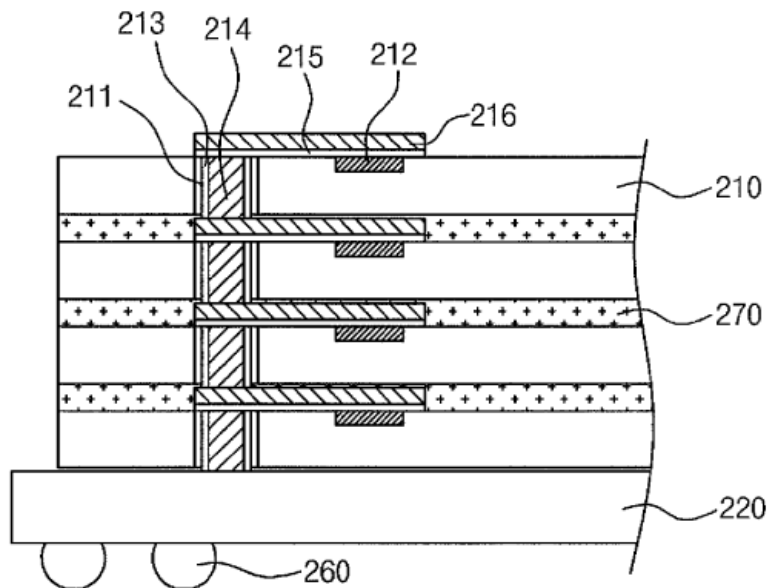
Han, Fig. 1.

41. But “since an electrical signal exchange is transmitted through the metal wire, the high number of wires used results in a low speed and a

deterioration in electrical properties.” *Han*, ¶[0009]. “Further, the formation of the metal wires necessitates an additional area on the substrate thereby increasing the size of the package and the space required between the semiconductor chips for bonding the metal wires increases the height of the package.” *Id.*

42. The above problems can be alleviated by “a conventional stack type semiconductor package using a through silicon via.” *Han*, ¶[0011]. As shown in the following Figure 2, “a stack type semiconductor package 200 using a through silicon via 214 has a structure in which the through silicon via 214, a semiconductor chip 210 formed with a redistribution layer 216 connecting the through silicon via 214 and a bonding pad 212 are stacked such that the through silicon vias 214 are aligned.” *Id.*, ¶[0012].

200

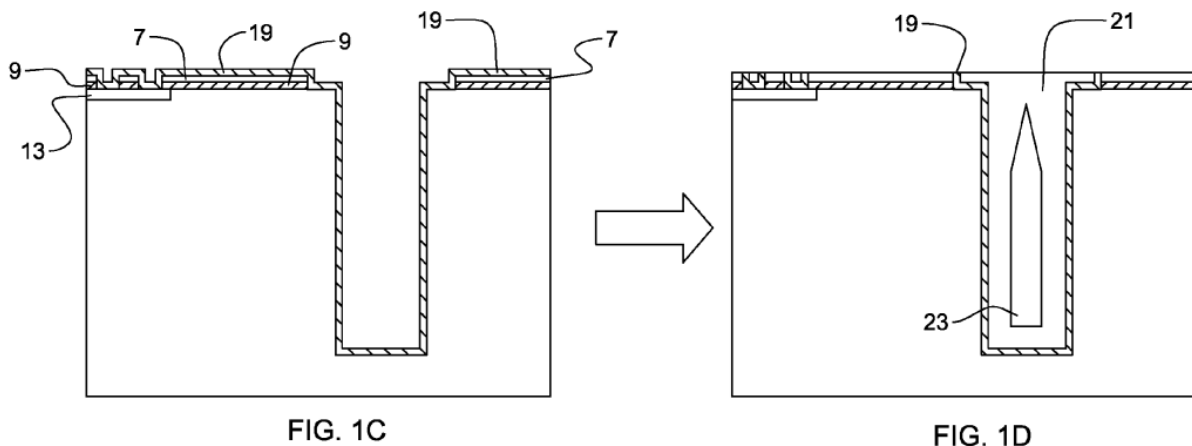


Han, Fig. 2.

43. “In the stack type semiconductor package 200 using a through silicon via, since an electrical connection is made through the through silicon via, a deterioration in electrical properties is prevented, thus increasing the operating speed of the semiconductor chip.” *Id.*, ¶[0014]. “Further, it is possible to miniaturize the stack type semiconductor package as an additional area on the substrate is removed and the distance between the stacked semiconductor chips is reduced.” *Id.*

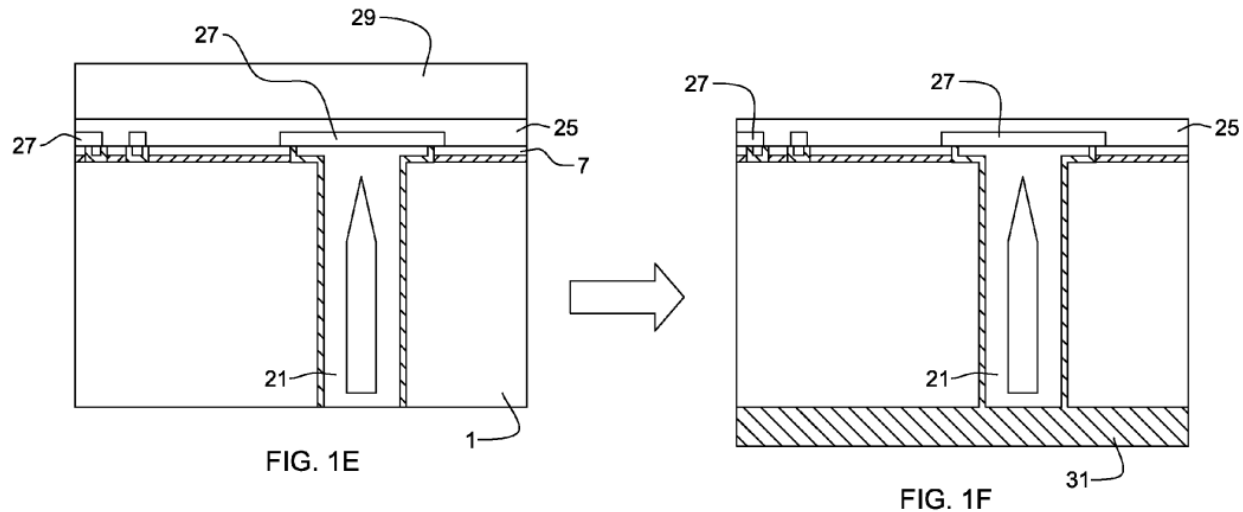
44. It is well known that during TSV fabrication, conformal deposition
s the deposited layers to follow the profile of any bottom layers. For example,

as shown in the following Figure 1C, to make an TSV in a semiconductor substrate, a via can be first etched in the substrate and a “liner 19 is conformally deposited in the via.” *Davis* (Ex. 1021), ¶[0045]. “The liner may, for example, be titanium, tantalum or tungsten, or compounds thereof, such as titanium nitride.” *Id.* Then, as shown in the following Figure 1D, the via “is filled with a conductive material, such as tungsten or copper, to form conductive via 21” *Id.* Often, “the conductive via material may not necessarily completely fill the via opening, as the central portion may have a void, as shown at 23.” *Id.*



Davis, Figs. 1C-1D.

45. After forming conductive via 21, “the back side of chip 1” is grinded “to remove silicon and expose conductive via connector 21, as shown in FIG. 1E.” *Id.*, ¶[0046]. Finally, as shown in the following Figure 1F, a “back side metal (BSM) 31” can be “formed on the back side of chip 1. *Id.*, ¶[0047].



Davis, Figs. 1E-1F.

46. It was well known in the art that conformal deposition processes like chemical vapor deposition (CVD) cause the deposited material to follow the shape of the underlying surface. *See id.*, [0048] (“[W]ell known processing, such as associated with chemical vapor deposition (CVD), is not described in detail . . .”). For example, *Chandrashekar* discloses that a “deposition process may result in a conformal layer of the materials [] built-up over the under-layer” and this “deposited layer follows the shape of the under-layer.” *Chandrashekar* (Ex. 1008), ¶[0031]. One example of such conformally-deposited layer is the liner 19 in *Davis*, above. Additionally, according to *Yen*, a profile of an underlying insulating layer may help the following formation of a conducting layer because the underlying insulating layer is conformally deposited to follow the profile the bottom layer. *Yen*, ¶[0063].

C. Thermally Induced Stress Due to TSVs

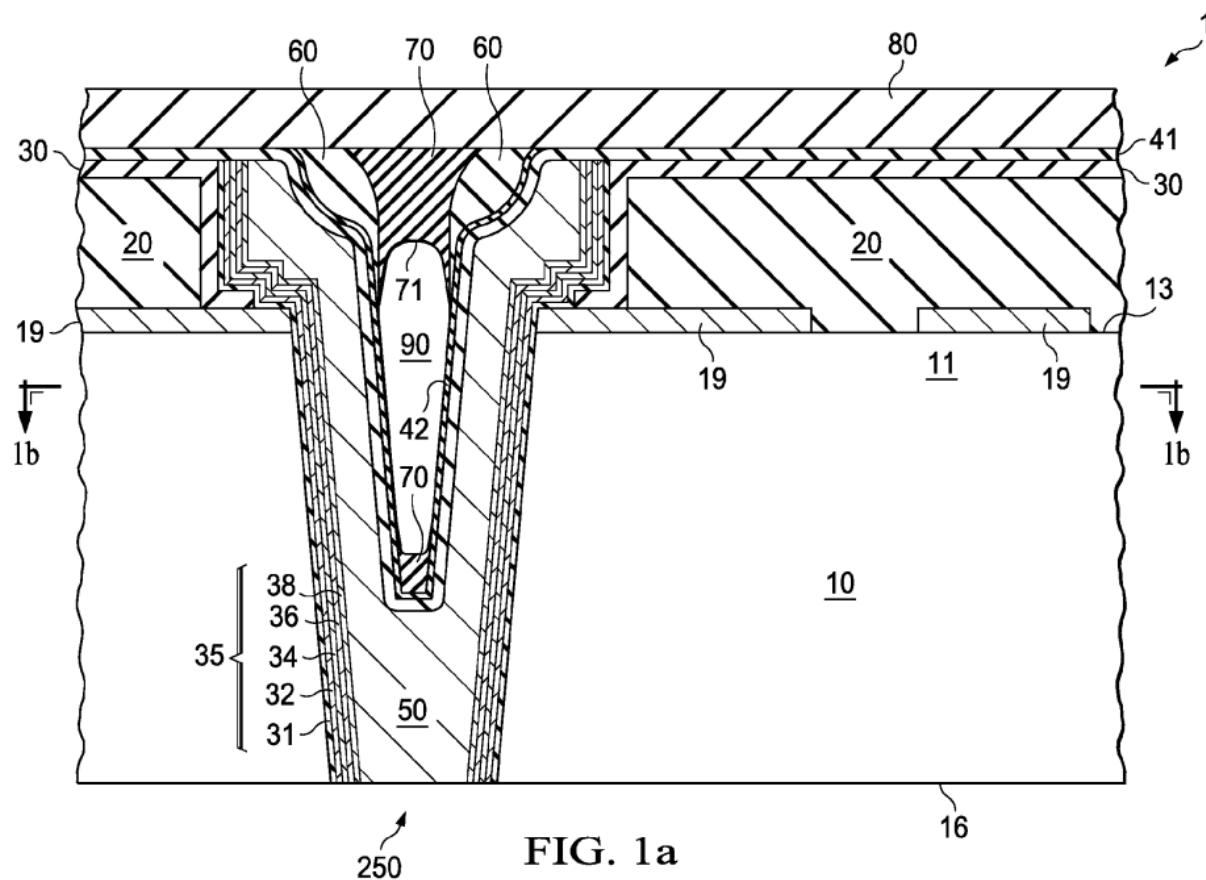
47. Using a large number of TSVs in the semiconductor substrate may cause thermally induced stress, making the substrate prone to cracking. This is because “[c]opper, as well as some other TSV filler materials, have a significantly higher coefficient of thermal expansion (CTE) as compared to conventional IC substrates, such as silicon.” *West*, [0005]. “For example, copper has a CTE of approximately 17 ppm/° C., whereas silicon has a CTE of approximately 2 to 3 ppm/° C.” *Id.* “This CTE mismatch (Δ CTE) can result in significant thermally induced stress in the silicon including the circuitry (e.g. MOS transistors) in the silicon surrounding the TSVs, particularly during certain fab processing subsequent to the fabrication of the TSV (e.g., 360 to 410° C. sinters), during assembly and test/operations as may occur during solder reflow (e.g., up to about 260° C.) or during thermo-compressive bonding (e.g., up to 400° C.), during certain temperature cycle reliability testing (e.g., -55° C. to 125° C.), or even during long-term field operation of the IC.” *Id.*

1. TSV Voids to Reduce Thermally Induced Stress

48. A number of solutions have been proposed to reduce problems caused by CTE mismatches for ICs having copper. As one example, *Pogge* (Ex. 1005) discloses that a void in a copper filled TSV “has an important function in relieving stress caused by differences in thermal coefficient of expansion (TCE) of the

various materials in and around the feature.” *Pogge*, ¶[0027]. Similarly, *Edelstein* (Ex. 1006) discloses that a “through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures.” *Edelstein*, ¶[0047]. Moreover, during prosecution of the ’609 patent, the Examiner cited *Edelstein* and *Beyne* for the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate, and Patent Owner acquiesced to the rejection and did not rebut the Examiner’s statement. Ex. 1003, at 88, 70-77, 67, 65.

49. The mechanism for the voids to reduce the stress was well known. This is because “metals typically expand faster than silicon, whereas voids, for example, filled with a gas having negligible expansion relative to the silicon substrate.” *Birner* (Ex. 1022), ¶[0024]. “Hence, a combination of metal with voids produces an effective material with a coefficient of expansion comparable to the substrate.” *Id.* For example, Figure 1a of *Birner*, below, shows that a TSV opening 250 includes a void 90 tailored to specific dimensions and shape. *Id.*, ¶¶[0024], [0032]. The void 90 forms an inner core region of the TSV, while a metal filler material 50 forms an outer layer of the TSV. *Id.* The void 90 provides room for the metal filler material 50 to expand and thus, on average, the void-metal combination has a thermal expansion profile similar to the silicon.



Id., Fig. 1a.

D. Backside Planarizing Process

50. As discussed in §VI.B, during TSV formation, the backside of the substrate may undergo a backside planarization process (i.e., backside grinding process) to expose the TSV’s conductive filler. *Davis*, ¶[0046]; *see also Birner*, ¶[0064]. Planarization is a flattening or smoothing out of the wafer surface topography. Chemical mechanical planarization (CMP) is one of the processes to achieve surface planarization. However, this process is inherently a “dirty” process that creates contamination. Thus, after “the CMP process is performed, it is

common to perform post-CMP cleaning to remove foreign matter such as CMP residue or particles.” *Kim* (Ex. 1013), ¶[0033]. Furthermore, it was well known to keep any voids sealed during the backside planarization process to avoid contamination. *Davis*, Fig. 1E; *see also Birner*, Fig. 1a.

VII. THE '609 PATENT

A. Alleged Invention of the '609 Patent

51. The '609 patent relates to “through silicon via structure, method of formation, and integration in semiconductor substrate.” Ex. 1001, 1:54-56.

52. For example, the '609 patent discloses “through silicon vias” (TSVs) in a substrate. Ex. 1001, 3:1-5. The '609 patent explains that the substrate “may also include various semiconductor devices” such as “various transistors, for example, NPN bipolar transistors, or any other device.” Ex. 1001, 3:5-10.

53. Various features of a TSV are disclosed in the '609 patent. In the following description of the '609 patent, I have used colored text to illustrate the various features with reference to annotated Figure 4 of the '609 patent.

54. For example, as illustrated in Figure 4, below, the '609 patent discloses “a through silicon via having a pinched off region such as, for example, TSV 402,” formed in substrate 412. Ex. 1001, 4:14-18.

Fig. 4

402

426

424

434

Pinched Off Region

428

412

Semiconductor Substrate

430

432

436

440

Hollow Center Portion

440

Through Silicon Via

450b

450a

438

Pinched Off Region

460

d_3

d_4

Conductive Filler

55. As further illustrated in Figure 4, above, the '609 patent discloses that “through silicon via 402 tapers from first depth d_3 to second depth d_4 .” Ex. 1001, 4:23-25. The '609 patent also discloses “depositing conductive filler 430 on sidewalls 440 of through silicon via 402 such that hollow center portion 432 and pinched off region 438 are formed in through silicon via 402.” Ex. 1001, 4:47-50. The '609 patent discloses that “[i]n addition to pinched off region 438 at a bottom portion of TSV 402, the present implementation may include forming pinched off region 434 at a top portion of TSV 402.” Ex. 1001, 5:3-5.

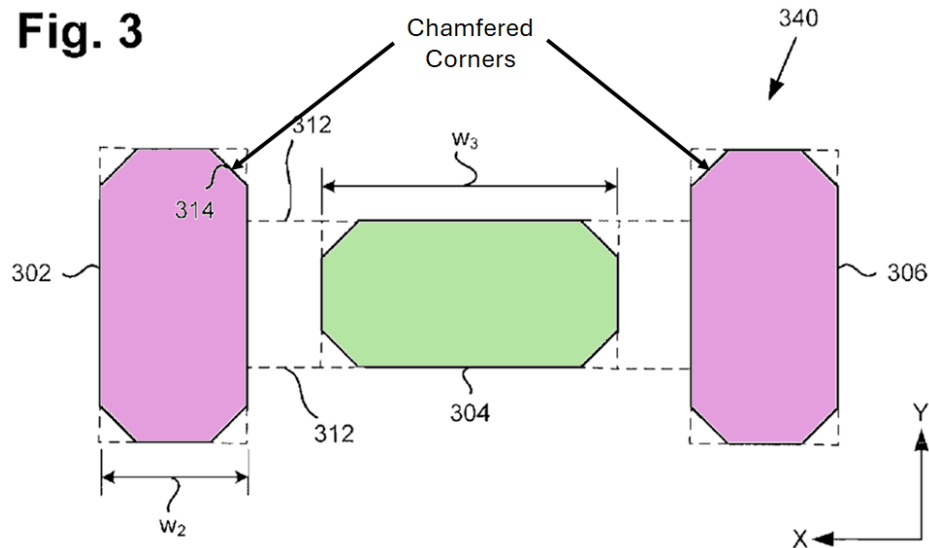
56. According to the '609 patent, the “[h]ollow center portion 432 provides many beneficial features.” Ex. 1001, 4:60-61. The '609 patent discloses that “hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402.” Ex. 1001, 4:61-62. Further, the '609 patent discloses that “[h]ollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions.” Ex. 1001, 4:62-66. The '609 patent explains that “[s]uch reduction in thermal and mechanical stress reduces cracking in substrate 412.” Ex. 1001, 4:66-67.

57. Referring back to Figure 4, the '609 patent discloses that “to ensure that hollow center portion 432 does not extend to the top of TSV 402, oxide layer 424 may be deposited over the top surface of substrate 412.” Ex. 1001, 5:7-10. Further, the '609 patent discloses that opening 428 may be formed in oxide layer 424, over TSV 402 such that the width of opening 428 is smaller than the width of TSV 402. Ex. 1001, 5:10-14. The '609 patent also discloses that “[d]epositing oxide layer 424 and forming opening 428 ensures **pinched off region 434** is formed in the top region of **TSV 402**, and that **hollow center portion 432** does not extend to the top of **TSV 402**.” Ex. 1001, 5:14-16.

58. In addition to these features of its TSV, the '609 patent discloses a particular arrangement of TSVs in the substrate. Specifically, the '609 patent

discloses that “each TSV in an array may be oriented at a 90° angle relative to an adjacent TSV.” Ex. 1001, 3:53-54. According to the ’609 patent, such an arrangement “may reduce cracking in the substrate by interrupting naturally forming cleavage planes 312 caused by thermal and mechanical stresses in the substrate.” Ex. 1001, 3:54-57. The ’609 patent also discloses that to “further reduce thermal and mechanical stress in the substrate, at least one corner of each of TSVs 302, 304 and 306 may be a chamfered corner” and that preferably “each corner of each TSV may be chamfered.” Ex. 1001, 3:58-61.

59. Annotated Figure 3 of the ’609 patent, below, illustrates the disclosed arrangement with TSVs 302 and 306 purportedly arranged in a “width direction” and TSV 304 disposed between TSVs 302 and 306 being oriented in a “length direction.” Ex. 1001, 3:46-52. As also seen in the figure below, the corners of TSVs 302, 304, and 306 are chamfered. Ex. 1001, 3:58-61.

Fig. 3

Ex. 1001, Fig. 3 (annotated)

60. As explained below, the prior art taught all of the above features disclosed by the '609 patent.

B. Challenged Claims

61. I understand that claims 1-18 of the '609 patent are being challenged in this proceeding.

62. In my opinion, claims 11, 13, 14, 15, 16, 18 are substantially similar to claims 1, 4, 5, 7, 8, 10 respectively. The following table demonstrates the similarity between claims 11, 13, 14, 15, 16, 18 and claims 1, 4, 5, 7, 8, 10 with substantially identical language italicized.

Claim 1	Claim 11
[1pre] <i>A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:</i>	[11pre] <i>A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:</i>

Claim 1	Claim 11
<i>[1a] a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;</i>	<i>[11a] a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;</i>
<i>[1b-1] a conductive filler disposed within each of said plurality of through silicon vias,</i> <i>[1b-2] each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,</i> <i>[1b-3] said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;</i>	<i>[11b] a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;</i>
<i>[1c-1] wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and</i> <i>[1c-2] wherein said hollow center is tapered in said pinched off region.</i>	<i>[11c] wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.</i>

Claim 4	Claim 13
4. <i>The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.</i>	13. <i>The semiconductor substrate of claim 11, wherein said conductive filler comprises a metallic filler.</i>

Claim 5	Claim 14
5. <i>The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.</i>	14. <i>The semiconductor substrate of claim 11, wherein said conductive filler comprises tungsten.</i>

Claim 7	Claim 15
<i>7. The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.</i>	<i>15. The semiconductor substrate of claim 11, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.</i>

Claim 8	Claim 16
<i>8. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.</i>	<i>16. The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias has at least one chamfered corner.</i>

Claim 10	Claim 18
<i>10. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills bottom portion, narrowing said hollow center.</i>	<i>18. The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.</i>

C. Prosecution History

63. The '609 patent was filed on March 8, 2012, as U.S. Patent Application No. 13/415,744, and claimed priority to U.S. Provisional Application No. 61/545,003, filed on October 7, 2011. Ex. 1003, at 286, 295. The '744 application included 20 application claims, including independent application claims 1, 11, and 13. Ex. 1003, at 307-311. During prosecution, the examiner

initially issued a restriction requirement, requiring Applicant to elect between an invention “drawn to a semiconductor device” and an invention “drawn to a method of forming a semiconductor device.” Ex. 1003, at 273-277. In response, Applicant cancelled two claims. Ex. 1003, at 260-264.

64. Subsequently, the Examiner rejected application claims 1-10 and 13-20 twice over Applicant’s Admitted Prior Art (“AAPA”) based on Figures 1A and 1B of the as-filed application in view U.S. Patent Publication No. 2012/0139127 (“*Beyne*”) (Ex. 1017) alone or in further view of U.S. Patent Publication No. 2011/0237073 (“*Dao*”) (Ex. 1018). Ex. 1003, at 193-206, 144-157. In the rejections, the Examiner asserted that “Beyne discloses (10B-H) each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate.” Ex. 1003, at 194, 144-145. I note that Applicant did not dispute the Examiner’s contention. Ex. 1003, at 176-183, 129-137, 111-119.

65. Instead, Applicant first amended independent application claims 1 and 13 to recite “said hollow center being surrounded by said conductive filler.” Ex. 1003, at 172, 174. Subsequently Applicant further amended independent application claims 1 and 13 to recite the hollow center being “entirely” surrounded by said conductive filler “to provide space for said conductive filler to expand inward.” Ex. 1003, at 107, 109.

66. The Examiner next rejected application claims 1-10 and 13-20 based on AAPA in view of *Beyne*, U.S. Patent Publication No. 2005/0121768 (“*Edelstein*”) or further in view of *Dao*. Ex. 1003, at 83-97. Again, Applicant did not dispute the Examiner’s contention that “*Edelstein* discloses Fig. 2b and 6d-f: Said hollow center (220) being entirely surrounded by said conductive filler (225) to provide space for said conductive filler to expand inward” or that “*Edelstein* discloses that providing the hollow portion 220 provides the benefit of reducing thermal stresses on the substrate.” Ex. 1003, at 88, 70-77. Instead, Applicant amended independent application claim 1 to additionally recite “said hollow center is tapered in said pinched off region” and independent application claim 13 to additionally recite that each of the plurality of through silicon vias has a pinched off region at a top portion “and another pinched off region at a bottom portion” and “said hollow center is tapered in said another pinched off region.” Ex. 1003, at 65, 67.

67. As a result, the Examiner allowed application claims 1-10 and 13-20. Ex. 1003, 21. In the reasons for allowance based on the prior art then known to the Examiner, the Examiner stated:

[T]he prior art fails to disclose and would not have rendered obvious:

each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination

during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region, as recited in claim 1;

and

each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region, as recited in claim 13.

Ex. 1003, at 21.

D. Claim Construction

68. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1003). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope

may be provided in the patent's written description, the patent's prosecution history, or both.

69. I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art in the relevant time period.

70. I was not asked to expressly construe any terms at this time but was asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '609 patent.

71. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '609 patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '609 patent (October 7, 2011).

VIII. LEVEL OF ORDINARY SKILL IN THE ART

72. In rendering the opinions set forth in this declaration, I have been asked to consider the '609 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSITA," or similar variation). I have considered factors

such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

73. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent the '609 patent (October 7, 2011) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and vice versa.

74. I was at least a person of ordinary skill in the art as of October 7, 2011.

IX. THE PRIOR ART

75. In forming my opinions, I found the following prior art relevant when considering whether the claims of the '609 patent are anticipated or would have been obvious.

Ex. 1004	U.S. Patent Publication No. 2009/0278237 to Cooney, III et al. ("Cooney")
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Ex. 1010	U.S. Patent Publication No. US 2011/0057319 to Dean, JR. et al. (“ <i>Dean</i> ”)
Ex. 1011	U.S. Patent Publication No. 2010/0032843 to Chen et al. (“ <i>Chen</i> ”)
Ex. 1016	U.S. Patent No. 8,237,288 to Farooq et al. (“ <i>Farooq</i> ”)

A. *Cooney* (US 2009/0278237)

76. *Cooney* published November 12, 2009, from U.S. Application No. 12/115,564, filed May 6, 2008. I understand and have been asked to assume that *Cooney* is prior art.

77. *Cooney* teaches a “microelectronic structure, such as a semiconductor structure, and a method for fabricating the microelectronic structure[.]” *Cooney*, Abstract. In particular, *Cooney* discloses a semiconductor substrate 10 that includes a contact region 12. *Cooney*, ¶[0026]; Fig. 1. *Cooney* explains that in addition to the contact region, “substrate 10 will also include located and formed therein semiconductor devices that are appropriate for a semiconductor circuit” and that such semiconductor devices may include, but are not necessarily limited to, resistors, transistors, diodes and capacitors. *Cooney*, ¶[0032].

78. *Cooney* also discloses a through substrate via (TSV). Throughout my discussion of *Cooney* below, I have used colored text to illustrate the various

features of *Cooney*'s TSV and substrate with reference to one or more annotated figures of *Cooney*. For example, as illustrated in annotated Figure 10, below, *Cooney* discloses a **through substrate via 24"** that penetrates from a **front side** (e.g., **top surface**) of a **semiconductor substrate 10"** to a **backside** (e.g., **bottom surface**) of the **semiconductor substrate 10**. *Cooney*, ¶[0065].

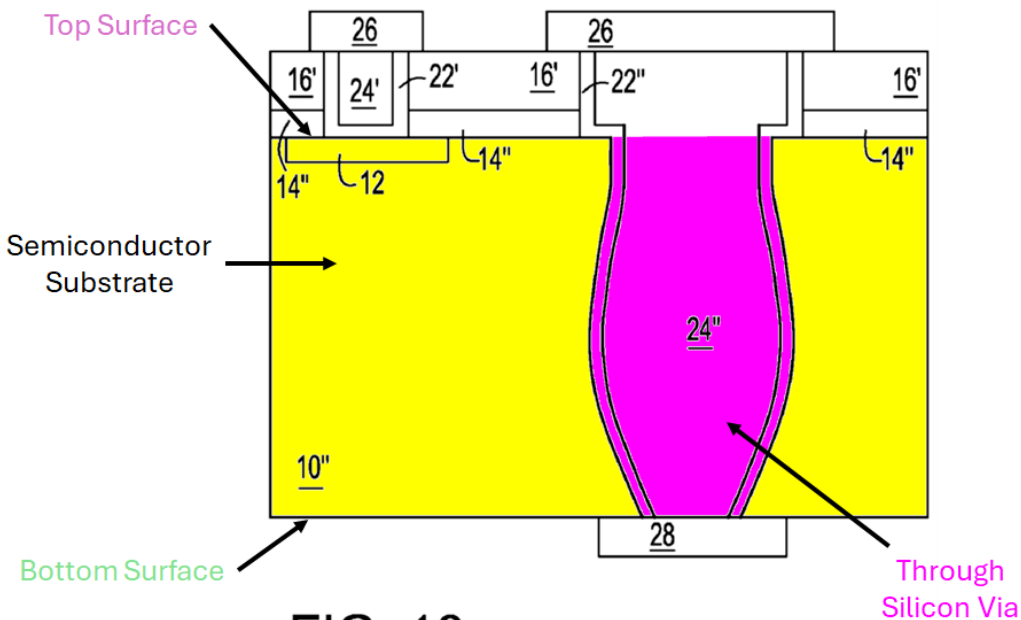


FIG. 10

Cooney, Fig. 10 (annotated).

79. *Cooney* explains that “a multiplicity of dimensionally similar or dimensionally identical apertures and corresponding vias may also be used within a single substrate.” *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. Thus, although each of Figures 1-10 of *Cooney* illustrates a single **TSV**, *Cooney*'s **substrate 10** includes a plurality of **TSVs**. Accordingly, in the following discussion,

the features disclosed in *Cooney* with reference to any of Figures 1-10 apply to each of the TSVs in *Cooney*.

80. *Cooney* discloses “a semiconductor substrate 10 that includes a contact region 12 located within the semiconductor substrate.” *Cooney*, ¶[0026]. *Cooney* explains that its disclosed embodiment is “not specifically limited to only a contact region within a semiconductor substrate” but rather it “contemplates that the semiconductor substrate 10 will also include located and formed therein semiconductor devices” such as but not necessarily limited to “resistors, transistors, diodes and capacitors.” *Cooney*, ¶[0032]. Further, *Cooney* discloses that an “etch stop layer 14 is located upon the semiconductor substrate 10 including the contact region 12.” *Cooney*, ¶[0026]. *Cooney* explains that “etch stop layer 14 will typically comprise a dielectric etch stop material.” *Cooney*, ¶[0034].

81. *Cooney* discloses etching the semiconductor substrate 10 in an etching step “to leave exposed a portion of the semiconductor substrate 10 within an aperture A2.” *Cooney*, ¶[0037]. *Cooney* discloses a subsequent process step in which “a second photoresist layer 20 located and formed upon the semiconductor structure” such that “second photoresist layer 20 forms an aperture A3 at the bottom of which is exposed a portion of the semiconductor substrate 10 that is fully exposed within the second aperture A2.” *Cooney*, ¶[0040]. In a subsequent step, “an aperture A4 that is etched into a semiconductor substrate 10’ derived from

the semiconductor substrate 10.” *Cooney*, ¶[0042]. *Cooney* discloses that its extended aperture has a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶[0042]. Annotated Figure 4 of *Cooney*, below, illustrates the extended aperture.

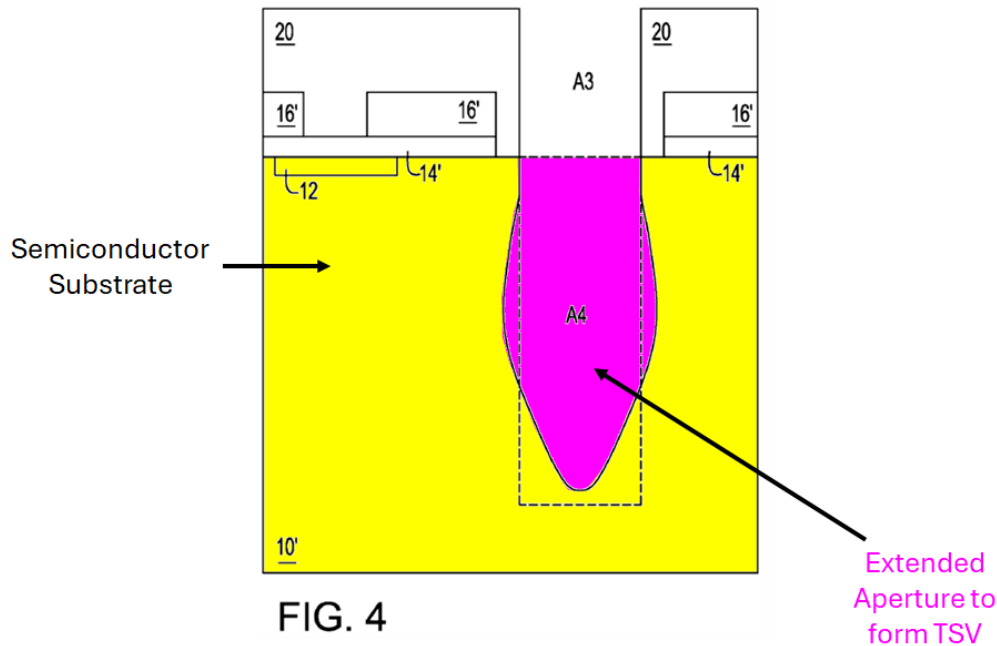


FIG. 4

Cooney, Fig. 4 (annotated).

82. *Cooney* discloses that the aperture formed in its semiconductor substrate for the formation of each TSV has varying widths and comprises four regions R1, R2, R3, and R4. *Cooney*, ¶¶[0049]-[0054]. Specifically, *Cooney* discloses the linewidth of the third region R3 is preferably greater than the linewidth of the first region R1 which in turn is preferably greater than the linewidth of the fourth region R4.” *Cooney*, ¶[0054]. *Cooney* also discloses that “the linewidth of the second region R2 is no greater than about 0.9 times (and

preferably from about 0.8 to about 0.95 times) the linewidth of the first region R1.”

Cooney, ¶[0054]. Annotated Figure 5 of *Cooney* illustrates regions R1, R2, R3, and R4 of the extended aperture etched in *Cooney*’s substrate to form a TSV.

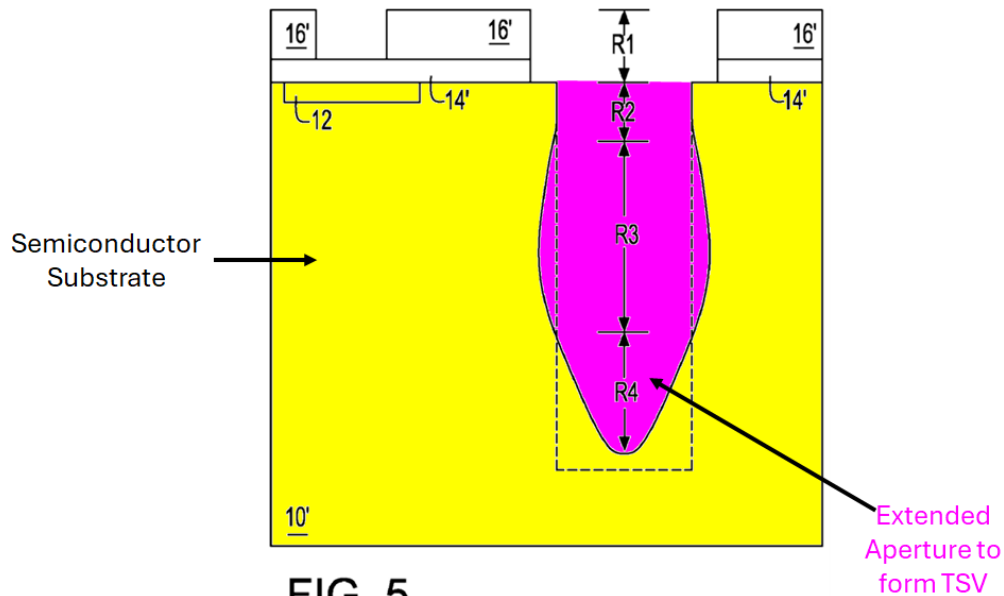


FIG. 5

Cooney, Fig. 5 (annotated).

83. *Cooney* discloses a liner layer 22 located and formed conformally and incompletely filling the extended aperture. *Cooney*, ¶[0055]. As illustrated in Figure 6, below, *Cooney* further discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* explains that “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3 and to localize that void to the third region R3.” *Cooney*, ¶[0051].

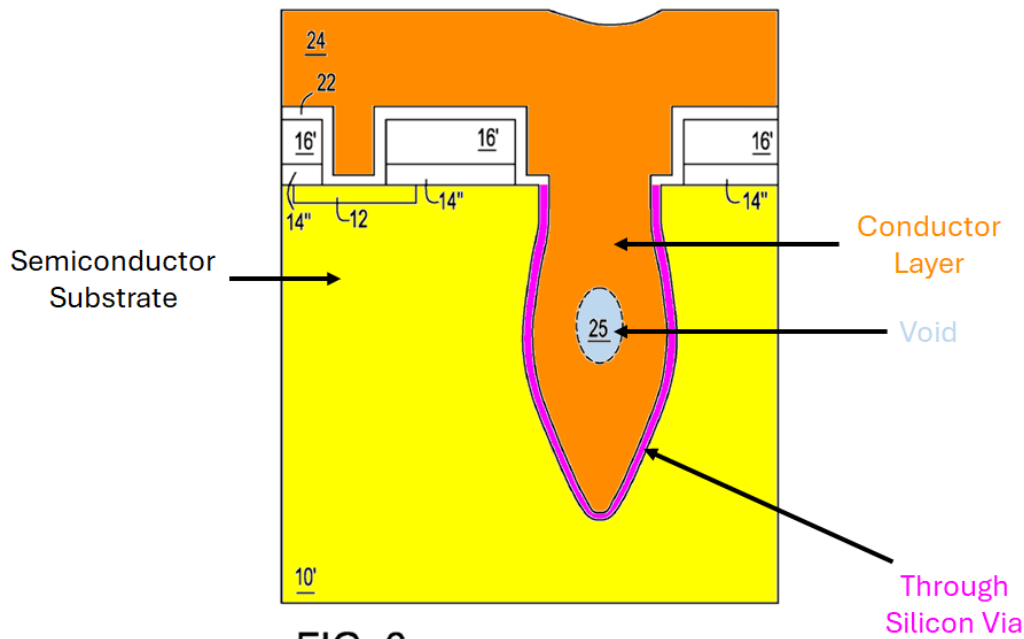


FIG. 6

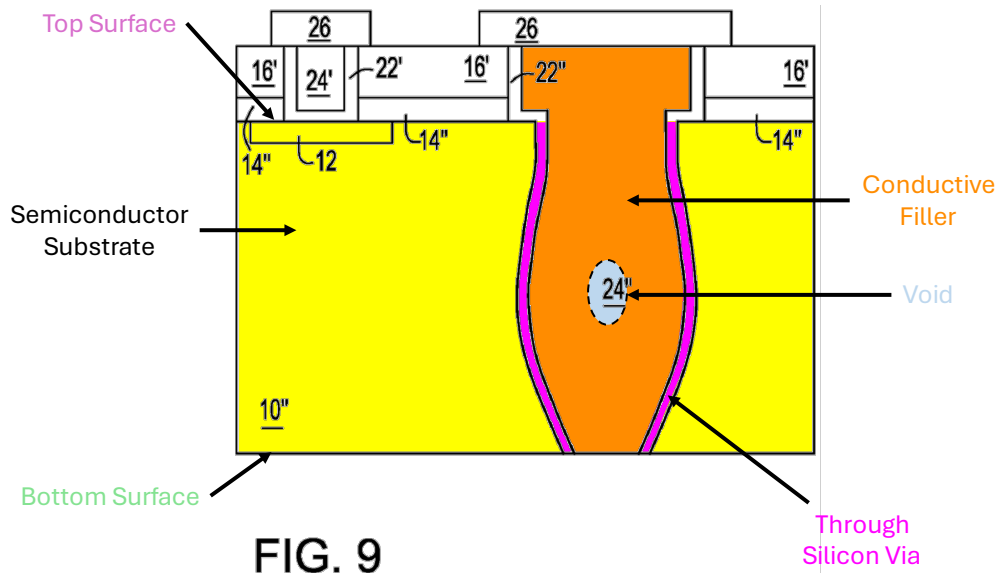
Cooney, Fig. 6 (annotated).

84. The “conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys,” and “typically comprises a tungsten material.” *Cooney*, ¶[0059].

85. *Cooney* discloses “backside planarizing of the semiconductor substrate 10', the liner layer 22' and the conductor layer 24'.” *Cooney*, ¶[0063]. *Cooney* explains that “[s]uch a backside planarizing is intended to remove a thickness from about 0.1 to about 10 microns from the semiconductor substrate 10' while leaving exposed portions of both the liner layer 22'' and the conductor layer 24'.” *Cooney*, ¶[0063]. *Cooney* also discloses that the backside planarizing may use methods such as “mechanical polish planarizing methods and chemical mechanical polish planarizing methods.” *Cooney*, ¶[0063]. Annotated Figure 9 of

Cooney, below, illustrates the semiconductor substrate 10", and TSV filled with conductor layer 24" and with a void that result from a backside planarizing.

Although Figure 9 of *Cooney* does not illustrate void 25, I have included void 25 in the annotated figure below to illustrate the final form of *Cooney*'s TSV.



Cooney, Fig. 9 (annotated and modified to include the void as shown in Fig. 6).

86. I note that according to *Cooney*, "FIG. 1 to FIG. 10 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic structure in accordance with a particular embodiment of the invention." *Cooney*, ¶[0025]. A skilled artisan would have understood from *Cooney* that features such as a substrate, TSV, conductor layer, void, shown in one figure of *Cooney* correspond to similar structures shown in other figures of *Cooney*. For example, the skilled artisan would have understood that elements

labeled 10, 10', 10" correspond to the same substrate, and similarly, elements labelled 24, 24', and 24" correspond to the same conductor layer.

87. Additionally, one skilled in the art would have understood that because Figures 4-8 of *Cooney* illustrate intermediate steps in fabricating *Cooney*'s TSV, the TSV shown in Figures 4-8 does not extend from the top surface to the bottom surface of the semiconductor substrate. In my opinion, this is similar to Figure 4 of the '609 patent, in which TSV 402 does not extend from the top surface of substrate 412 to a bottom surface of substrate 412. *Compare* Ex. 1001, Fig. 4 with *Cooney*, Fig. 6. Indeed, the '609 patent discloses "polishing bottom surface 460 of substrate 412 to expose conductive filler 430 from the bottom surface of the substrate" as the final step 540 in manufacturing substrate 412. *Id.*, 5:18-21, Fig. 5. Similarly, Figures 9 and 10 of *Cooney* illustrate *Cooney*'s TSV extending from the top surface to the bottom surface of substrate 10 after backside planarizing to expose the TSV. *Cooney*, ¶[0063].

88. *Cooney* is analogous art to the '609 patent because *Cooney*, like the '609 patent, "relates generally to through substrate vias within microelectronic substrate" and to "a method for fabricating the microelectronic structure, include an aperture within a substrate." *Cooney*, ¶[0002], Abstract; Ex. 1001, 1:54-56 ("The present application is directed to through silicon via structure, method of formation, and integration in semiconductor substrate."). *Compare* *Cooney*,

Abstract, ¶¶[0018]-[0020], [0023], [0026], [0042]-[0043], [0051]-[0055], [0058]-[0060], *with* Ex. 1001, Abstract, 1:54-56, 3:1-5, 4:9-5:24.

B. *Dean* (US 2011/0057319)

89. *Dean* published March 10, 2011, from U.S. Application No. 12/555,981, filed September 9, 2009. I understand and have been asked to assume that *Dean* is prior art.

90. Like *Cooney*, *Dean* relates to TSVs, and more particularly, to arranging TSVs in an integrated circuit (IC) layout to reduce or eliminate wafer breakage. *Dean*, ¶[0002]. *Dean* recognizes that “[t]hrough silicon vias (TSVs) are typically elongated vias,” and “when TSVs are aligned they act like perforations [in the wafer] making it easy to break a wafer into which they are formed.” *Dean*, ¶[0017] (“In particular, wafers having aligned, regularly repeating TSV arrays break at an approximately 66% rate[.]”). To alleviate this problem, *Dean* discloses a system for “identifying linearly aligned through silicon vias (TSVs) in a portion of an integrated circuit (IC) layout that includes a plurality of TSVs” and “modifying at least the portion of the IC layout to reduce a number of the linearly aligned TSVs.” *Dean*, ¶[0006], Abstract.

91. *Dean* discloses, for example, an “IC layout 90 including array 160 having nine TSV sets 162” in which “all of the TSVs . . . initially extend in a

single, given direction[.]” *Dean*, ¶[0031]. Figure 4 of *Dean* illustrates this example layout with TSV sets 162 aligned in the Y direction. *Id.*, Fig. 4.

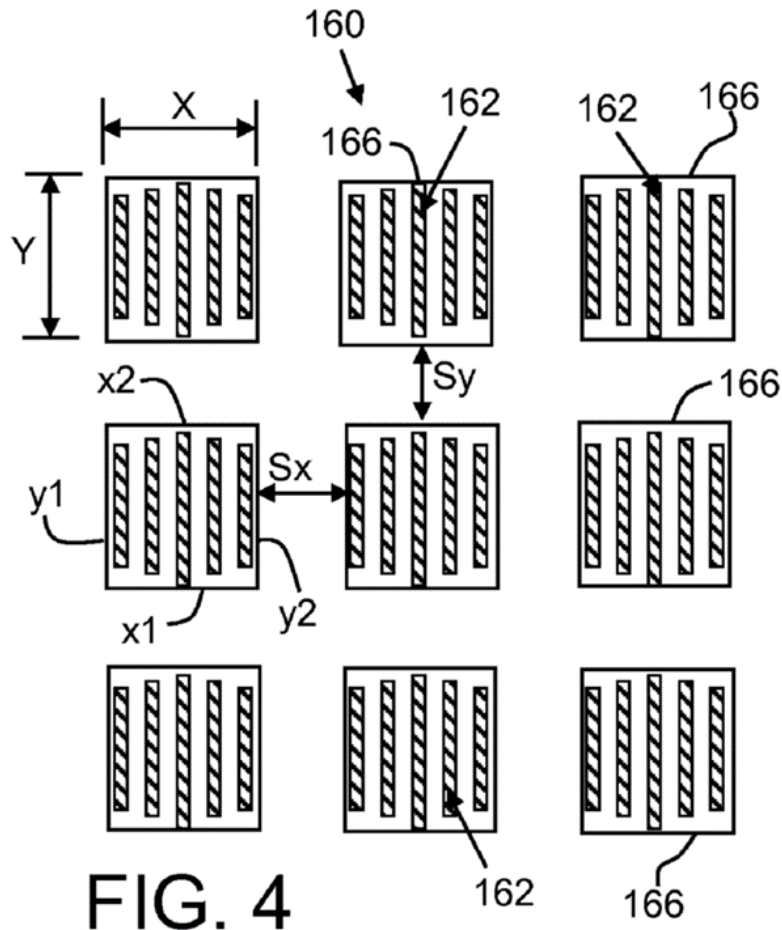


FIG. 4

Dean, Fig. 4.

92. *Dean* discloses rotating alternate TSV sets 162 to be non-aligned to the given direction (e.g., the Y direction). *Dean*, ¶[0033]. According to *Dean*, rotation of the TSV sets “reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing.” *Dean*, ¶[0039].

93. In my discussion of *Dean*, I use colored text to illustrate the various features of *Dean*'s TSV arrangement with reference to one or more annotated figures of *Dean*. For example, Figure 6 of *Dean*, below, illustrates the results of the rotation of some of the TSV sets 162 such that some TSV sets 162 are aligned with a vertical direction, whereas other rotated TSV sets 162 are aligned in a horizontal direction.

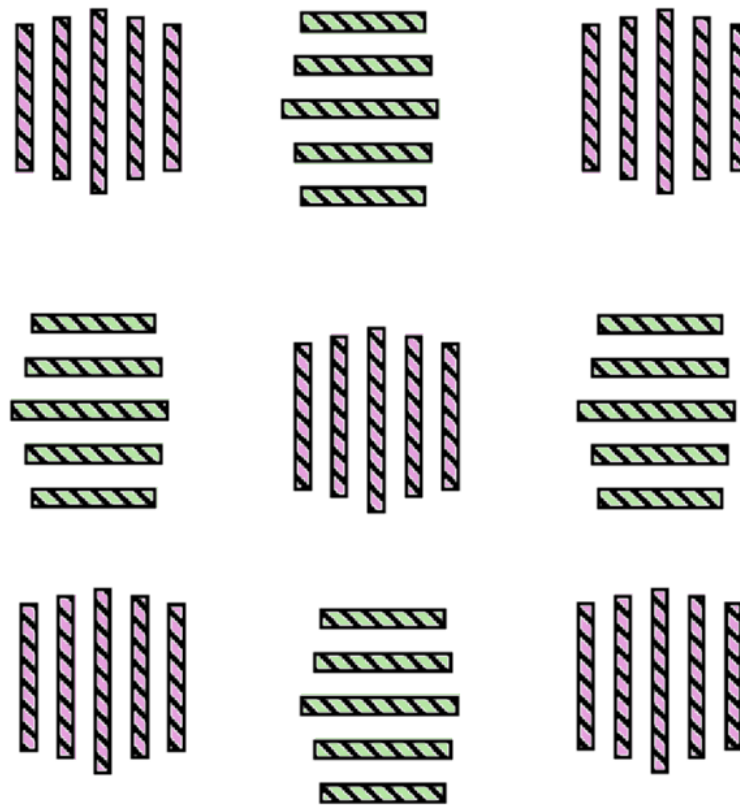


FIG. 6

Dean, Fig. 6 (annotated).

94. According to *Dean*, the rotation of the TSV sets “reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid

alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing.” *Dean*, ¶[0039].

95. *Dean* is analogous art to the ’609 patent because *Dean*, like the ’609 patent, “relates generally to through silicon vias, and more particularly, to arranging through silicon vias (TSVs) in an integrated circuit (IC) layout to reduce linearly aligned TSVs.” *Dean*, ¶[0002]; Ex. 1001, 1:54-56 (“The present application is directed to through silicon via structure, method of formation, and integration in semiconductor substrate.”); *Compare Dean*, Abstract, ¶¶[0002], [0005]-[0007], [0042], with Ex. 1001, Abstract, 1:54-56, 3:1-5, 4:9-5:24.

C. *Chen* (US 2010/0032843)

96. *Chen* published February 11, 2010, from U.S. Application No. 12/186,105, filed August 5, 2008. I understand and have been asked to assume that *Chen* is prior art.

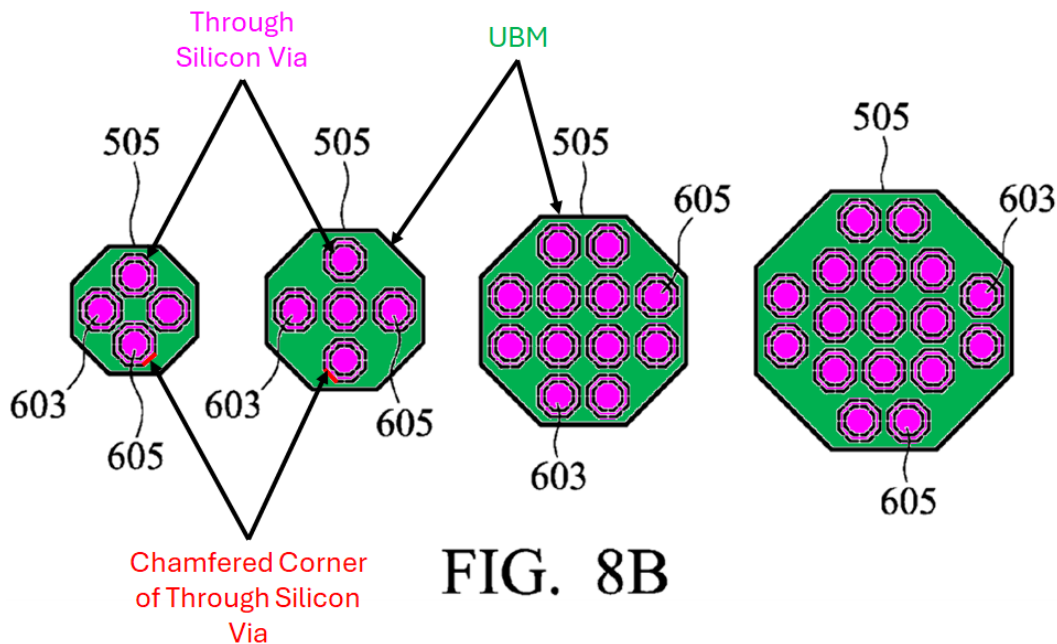
97. *Chen* relates to TSV layout to reduce the overall footprint and save space on a die’s surface. *Chen*, Abstract, ¶¶[0001], [0005]-[0008]. Specifically, *Chen* is directed to “a system and method for manufacturing through silicon vias.” *Chen*, ¶[0001]. *Chen* notes that a semiconductor die can be connected to other die or devices through bumps. *Chen*, ¶[0002]. *Chen* discloses that the bumps themselves are “normally connected to the semiconductor die . . . by layers of

conductive material collectively known as under bump metallization [UBM].”

Chen, ¶[0002].

98. *Chen* explains that by placing the TSVs under the UBM, “less space on the surface of the die needs to be taken up by trace lines,” so that the “die may be spaced closer together,” which helps to “reduce the size of circuit components in general, leading to smaller devices overall.” *Chen*, ¶[0044]. *Chen* further explains that different layouts of the TSVs are used depending on the UBM shape, as shown below. *Chen*, ¶[0042].

99. In my discussion of *Chen*, I use colored text to illustrate the various features of *Chen*’s TSV arrangement with reference to one or more annotated figures of *Chen*. For example, Figure 8 of *Chen* discloses an exemplary embodiment in which the UBM is formed in an octagonal shape and the TSVs under the UBM are formed with chamfered corners and arranged to fit them under the UBM. *Chen*, ¶[0042].



Chen, Fig. 8B (annotated).

100. *Chen* is analogous art to the '609 patent because *Chen*, like the '609 patent, “relates generally to a system and method of manufacturing semiconductor devices, and more particularly to a system and method for manufacturing through silicon vias. discloses methods of formation of TSVs in a semiconductor substrate.” *Chen*, ¶[0001]; Ex. 1001, 1:54-56 (“The present application is directed to through silicon via structure, method of formation, and integration in semiconductor substrate.”); *Compare Chen*, Abstract, ¶¶[0001], [0006]-[0008], [0024]-[0027], with Ex. 1001, Abstract, 1:54-56, 3:1-5, 4:9-5:24.

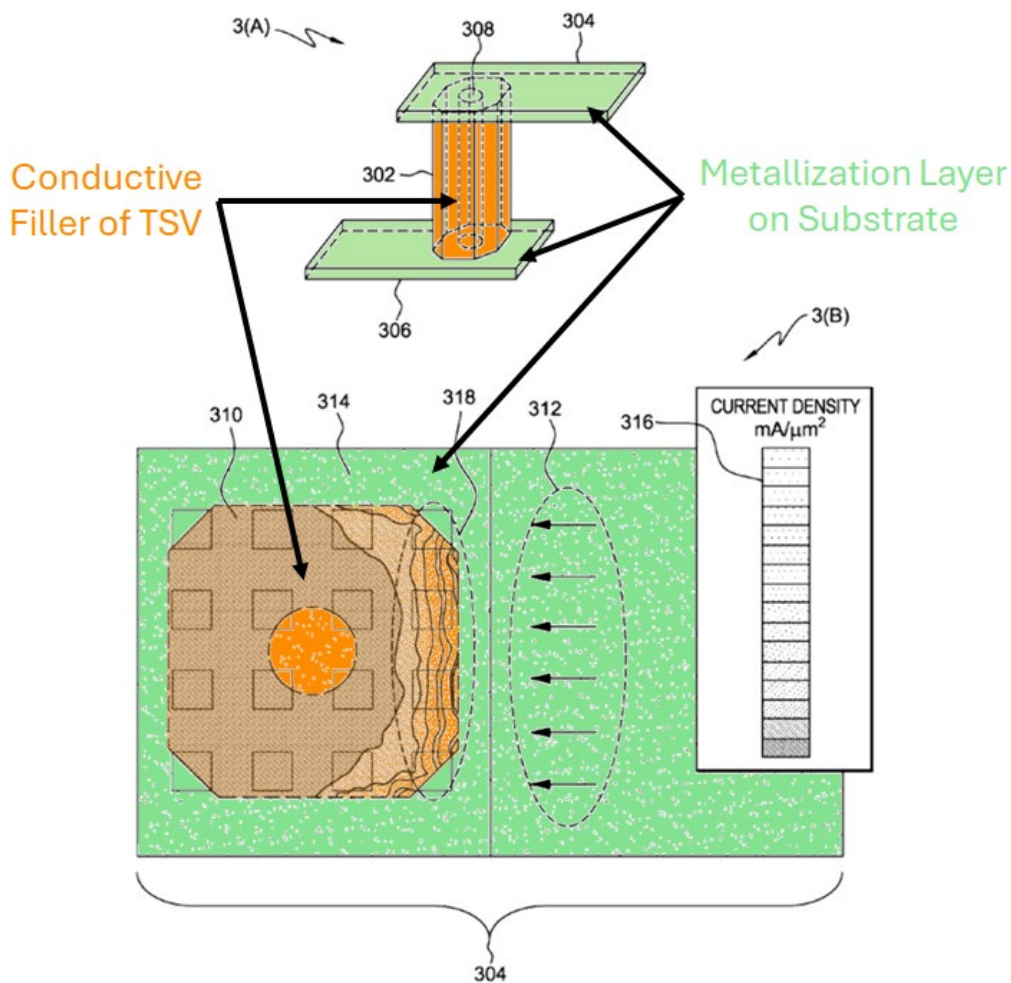
D. *Farooq* (US 8,237,288)

101. *Farooq* issued on August 7, 2012, from U.S. Application No. 13/023,743, filed on February 9, 2011. I understand and have been asked to assume that *Farooq* is prior art.

102. *Farooq* discloses “a method for reducing electromigration in a circuit containing a through-silicon via (TSV) and the resulting novel structure for the TSV.” *Farooq*, Abstract.

103. According to *Farooq*, electromigration through the TSV causes a gap to form in the material, leading to higher resistance or even circuit failure. *Id.*, 1:62-2:5, 4:10-26. This occurs when current crowding in a region causes the current density to exceed a certain value. *Farooq*, 3:65-4:5.

104. To reduce electromigration, *Farooq* discloses using a “truncated square” or “octagonal” shaped TSV structure, so “the current is evenly distributed over the length of the edge.” *Farooq*, 4:29-34. As current (312) enters the TSV, “relatively uniform current densities can be seen” along the flat edge of the truncated square, as shown below. *Farooq*, 5:15-17, 5:40-42.



Farooq, Fig. 3 (annotated).

105. *Farooq* is analogous art to the '609 patent because *Farooq*, like the '609 patent, discloses methods of formation of TSVs in a semiconductor substrate. Compare *Farooq*, 1:18-37, 5:6-12, 6:4-19, with '609 patent, Abstract, 1:54-56, 3:1-5, 4:9-5:24.

X. GROUNDS OF UNPATENTABILITY

106. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my

opinion that claims 1-18 of the '609 patent would have been anticipated and/or obvious to one of ordinary skill in the art.

107. In particular, it is my opinion that claims 1-18 of the '609 patent would have been anticipated and/or obvious to a person of ordinary skill in the art based on the prior art shown below:

Ground	Claims	Basis	Prior Art
1A	1-6, 9-14, 17, and 18	§ 102	<i>Cooney</i>
1B	1-6, 9-14, 17, and 18	§ 103	<i>Cooney</i>
2	7 and 15	§ 103	<i>Cooney</i> in combination with <i>Dean</i>
3	8 and 16	§ 103	<i>Cooney</i> in combination with <i>Farooq</i>
4	8 and 16	§ 103	<i>Chen</i> in combination with <i>Cooney</i>

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

108. In my opinion claims 1-18 would have been anticipated and/or obvious to one skilled in the art at the earliest priority date of the '609 patent.

A. Claims 1-6, 9-14, 17, and 18 Are Anticipated by *Cooney* (Ground 1A) or Alternatively Obvious over *Cooney* (Ground 1B)

1. Claim 1:

109. In my opinion, *Cooney* discloses (Ground 1A) or would have rendered obvious (Ground 1B) every element of independent claim 1.³

a. [1pre] “A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:”

110. To the extent the preamble is limiting, *Cooney* discloses a semiconductor substrate having a plurality of devices.

111. In particular *Cooney* discloses a semiconductor substrate 10 that includes a contact region 12. *Cooney*, ¶[0026]. *Cooney* explains that in addition to the contact region, “substrate 10 will also include located and formed therein semiconductor devices that are appropriate for a semiconductor circuit” and that such semiconductor devices may include, but are not necessarily limited to, “resistors, transistors, diodes and capacitors.” *Cooney*, ¶[0032]. Annotated Figure 1 of *Cooney*, below, illustrates *Cooney*’s semiconductor substrate 12 that may include a plurality of semiconductor devices.

³ I have noted specific discussions related to Ground 1B throughout my declaration wherever such distinction is needed, but my discussions Ground 1A would apply equally to each of the positions in Ground 1B.

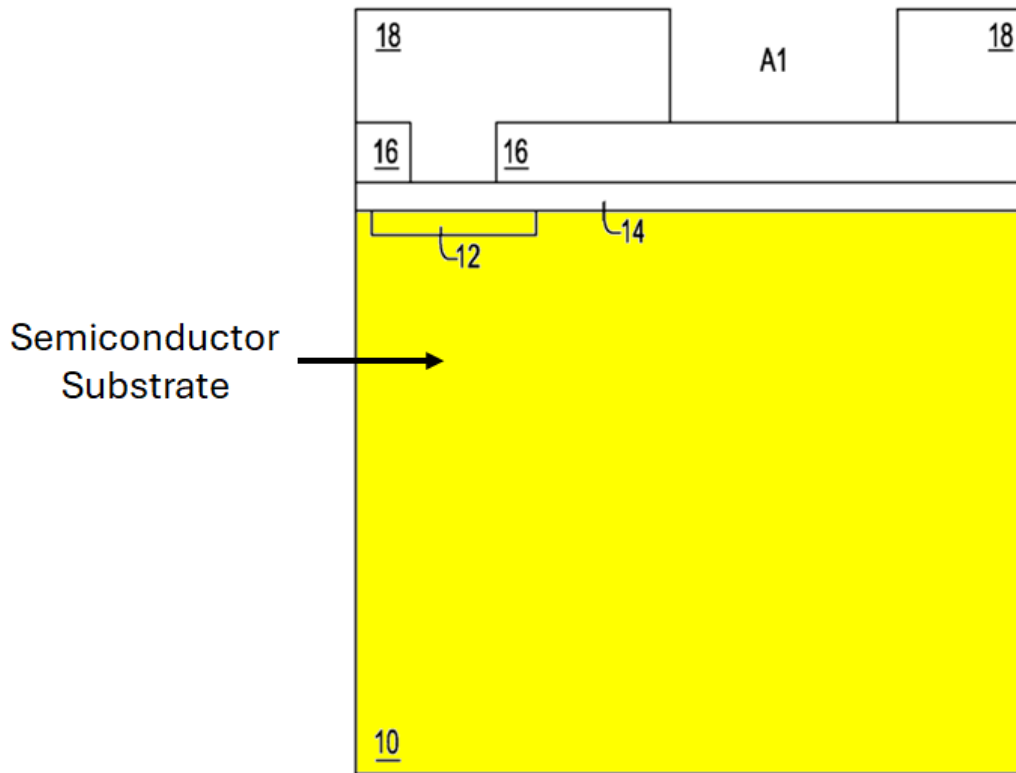


FIG. 1

Cooney, Fig. 1 (annotated).

- b. [1a]: “a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;”

112. In my opinion, *Cooney* discloses a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate.

113. For example, *Cooney* discloses a semiconductor structure that includes a through substrate via 24” that penetrates from a front side of a semiconductor substrate 10” to a backside of the semiconductor substrate 10.

Cooney, ¶[0065]. *Cooney* also discloses that an “etch stop layer 14 is located upon

the semiconductor substrate 10 including the contact region 12.” *Cooney*, ¶[0026].

Because the etch stop layer 14 is positioned on top of substrate 10, in my opinion, *Cooney*’s front side surface abutting on the etch stop layer 14 constitutes the claimed “top surface” and the backside of *Cooney*’s substrate 10 constitutes the claimed “bottom surface.”

114. Annotated Figure 10 of *Cooney*, below, illustrates *Cooney*’s TSV (e.g., through substrate via 24”) that penetrates from a top surface (e.g., front side) of a semiconductor substrate 10” to a bottom surface (e.g., “backside”) of the semiconductor substrate 10.

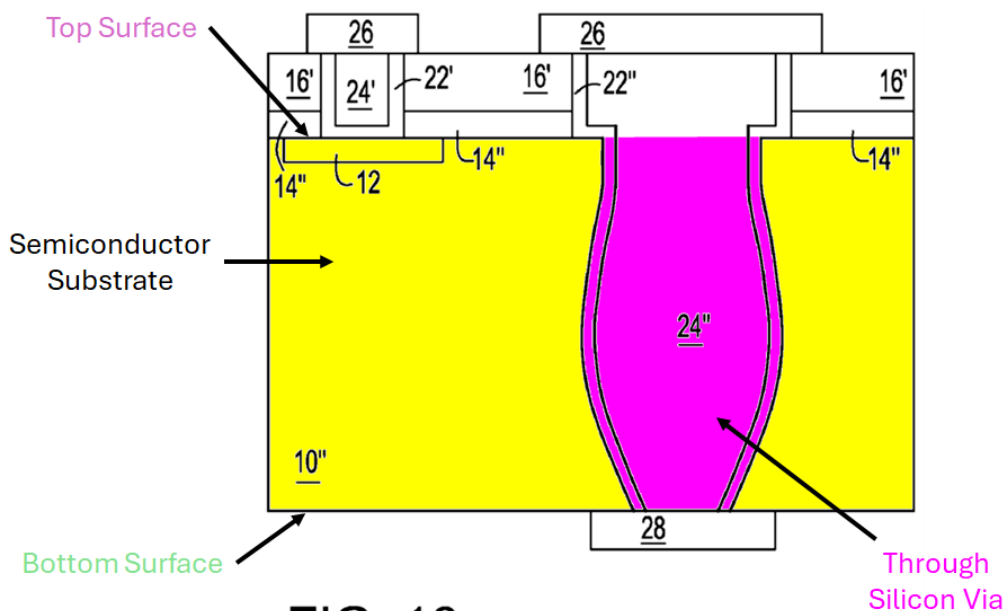


FIG. 10

Cooney, Fig. 10 (annotated).

115. Furthermore, as I discussed in Section IX.A, although Figure 10 of *Cooney* illustrates a single TSV, *Cooney*’s substrate 10 includes a plurality of

similar TSVs, each of which extends from a top surface of Cooney's substrate 10 to a bottom surface of Cooney's substrate 10. Cooney, ¶[0066]; see also Cooney, Abstract, ¶¶[0018], [0020].

c. [1b-1]: “a conductive filler disposed within each of said plurality of through silicon vias,”

116. In my opinion, Cooney discloses a conductor layer disposed within and filling the TSVs. For example, Cooney discloses a conductive filler disposed within each of said plurality of through silicon vias.

117. For example, as I discussed in Section IX.A, Cooney discloses etching an extended aperture in a semiconductor substrate 10 for forming one or more TSVs through the semiconductor substrate 10. Cooney, ¶[0042]. Further, Cooney discloses “a liner layer 22 located and formed conformally upon the semiconductor structure” and “incompletely filling the extended aperture.” Cooney, ¶[0055]. Cooney further discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” Cooney, ¶[0055]. In my opinion, the conductor layer 24 is located within Cooney's TSV because the conductor layer 24 completely fills the extended aperture that forms Cooney's TSV.

118. Cooney also discloses that “the conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys.” Cooney, ¶[0059]. In my opinion, the conductor layer 24 of

Cooney is conductive because *Cooney*'s conductor layer 24 is made of metals or metal alloys, which are electrically conductive. I also note that *Cooney* itself designates layer 24 as a "conductor." *Cooney*, ¶[0059]. Annotated Figure 6 of *Cooney* illustrates conductor layer 24 that constitutes the conductive filler within the TSV, along with the void 25..

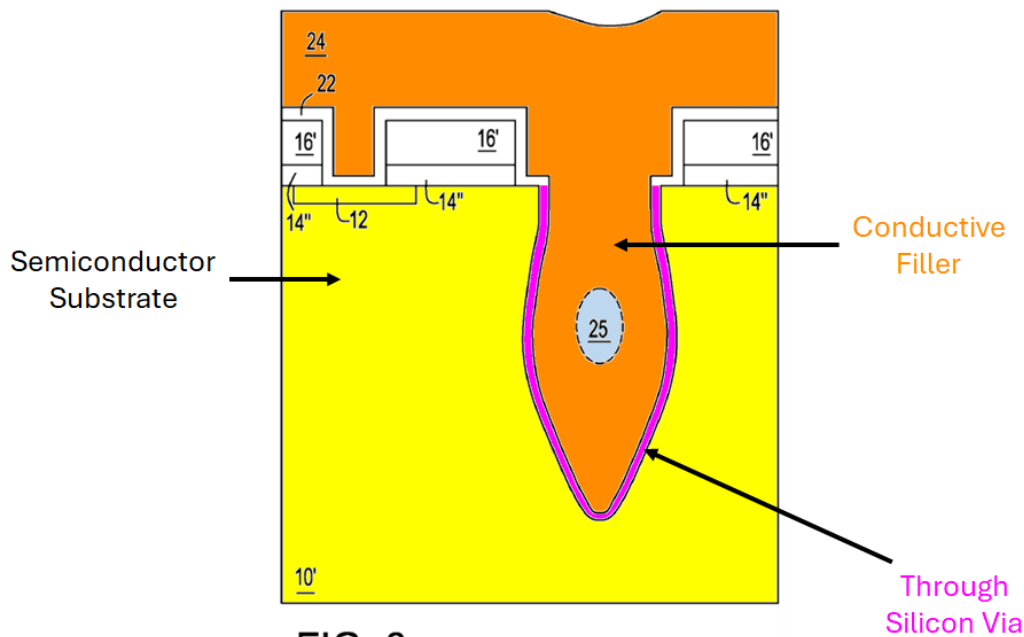


FIG. 6

Cooney, Fig. 6 (annotated).

119. Furthermore, as I discussed in Section IX.A, although Figure 10 of *Cooney* illustrates a single TSV, *Cooney*'s substrate 10 includes a plurality of similar TSVs. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. Each of *Cooney*'s TSVs includes a conductive filler (e.g., conductor layer 24) disposed within a respective TSV.

- d. [1b-2]: “each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”

120. In my opinion, *Cooney* discloses (**Ground 1A**) or would have rendered obvious (**Ground 1B**) that each of said plurality of through silicon vias has a hollow center to reduce thermal stress in said semiconductor substrate.

121. For example, as I discussed in Section XI.A.1.c, *Cooney* discloses “a liner layer 22 located and formed conformally upon the semiconductor structure” and “incompletely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* also discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]; *see also Cooney*, Abstract, ¶[0051]. *Cooney* explains: “As is illustrated by the phantom line enclosure within the schematic diagram of FIG. 6, the conductor layer 24 may be deposited or formed with a void 25.” *Cooney*, ¶[0060]. In my opinion, *Cooney*’s void 25 constitutes the claimed hollow center. Annotated Figure 6 of *Cooney*, below, illustrates the hollow center (e.g., void 25) within *Cooney*’s through silicon via in substrate 10.

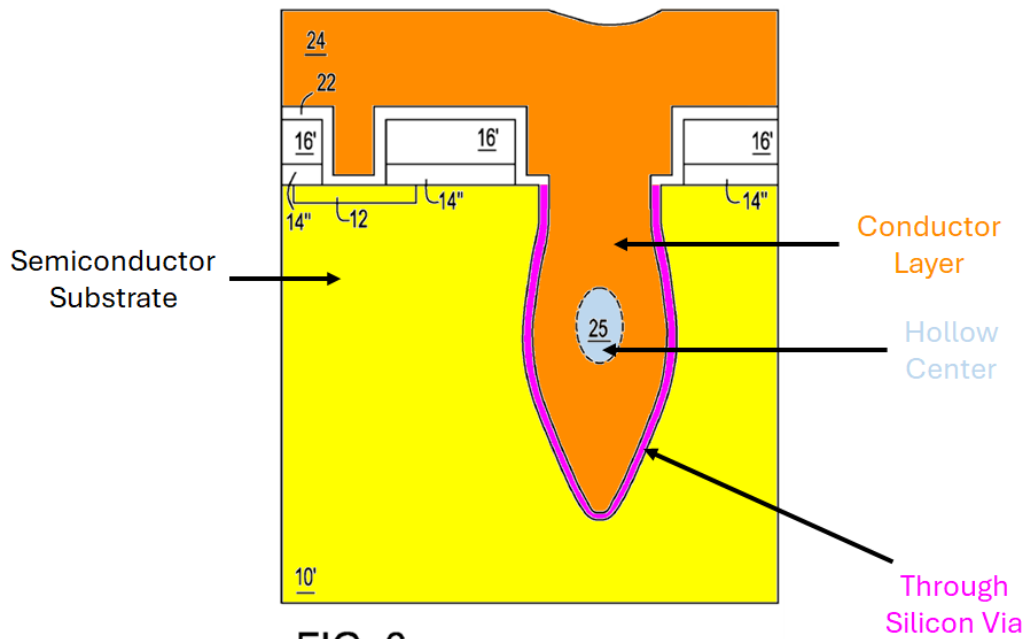


FIG. 6

Cooney, Fig. 6 (annotated).

122. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single TSV, *Cooney*'s substrate 10 includes a plurality of similar TSVs. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. In my opinion, therefore, each of the plurality of TSVs in *Cooney*'s substrate 10 has a hollow center.

123. **Ground 1A:** Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney*'s void 25 reduces thermal stress in *Cooney*'s substrate. The '609 patent does not identify any characteristics or properties of the hollow center that contribute to thermal stress reduction in the semiconductor substrate. Ex. 1001, 4:60-61; see generally Ex. 1001. In my opinion, a POSITA would have understood that void 25 in *Cooney*'s TSV would

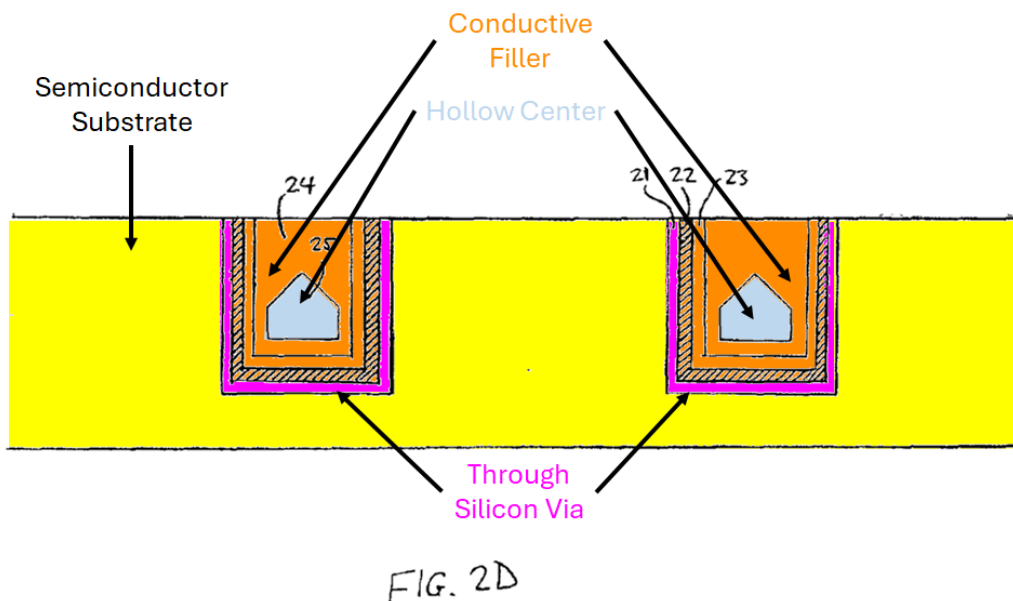
also reduce thermal stress in *Cooney*'s substrate, *see supra* VI.C.1, consistent with the hollow center of the '609 patent providing stress reduction in the substrate of the '609 patent.

124. **Ground 1B:** To the extent the Patent Owner argues otherwise, a POSITA would have found it obvious to include *Cooney*'s purposeful void 25 to "reduce thermal stress in said semiconductor substrate," in view of the POSITA's knowledge of the state of the art.

125. A POSITA would have recognized that it was well known in the art that the presence of a void in a TSV reduces thermal stress in the surrounding substrate. For example, I have provided at least two references that explains this feature: U.S. Patent Publication No. 2003/0111733 to Pogge et al. ("*Pogge*," Ex. 1005), published on June 19, 2003, and U.S. Patent Publication No. 2006/0027934 to Edelstein et al. ("*Edelstein*," Ex. 1006), published on February 9, 2006.

126. *Pogge* is directed to "a process for chip-level and wafer-level integration in which vertical interconnections are formed." *Pogge*, ¶[0001]. *Pogge* discloses that its vertical interconnections are through-vias in a chip or TSVs. *Pogge*, ¶[0009]. *Pogge* explains that a "metallized through-via in a semiconductor substrate, such as a silicon wafer, may be formed by depositing metal in a trench and thinning the wafer to open the bottom of the trench[.]" *Pogge*, ¶[0025]. *Pogge* also discloses etching trenches 2, and depositing copper and tungsten in the

trenches such that “a void 25 remains near the bottom of [each] trench.” *Pogge*, ¶¶[0026]-[0027]. Annotated Figure 2D of *Pogge* illustrates TSVs (e.g., trench structure 20) including an oxide layer 21, a conductive filler (e.g., layers 22-24) and a hollow center (e.g., void 25) formed in a semiconductor substrate. *Pogge*, ¶¶[0026]-[0028].

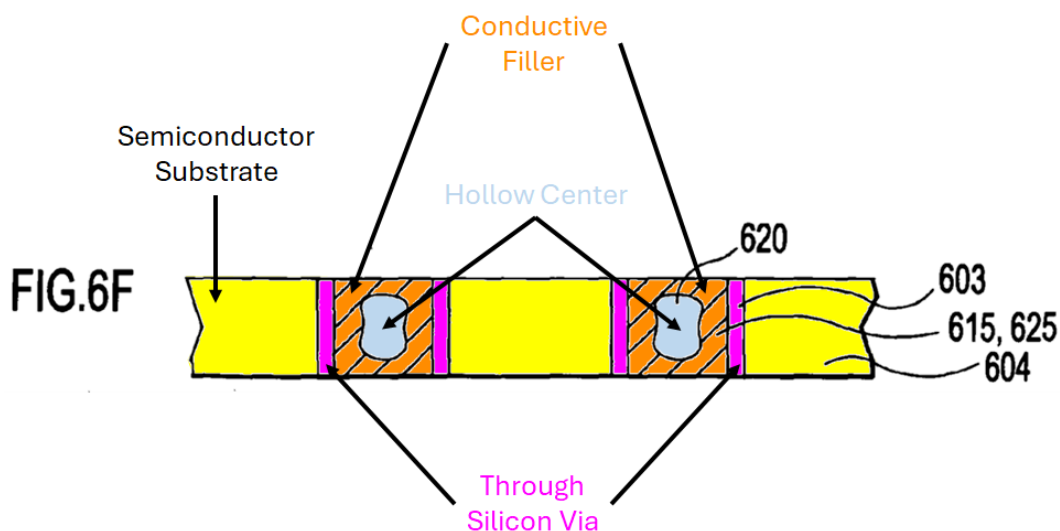


Pogge, Fig. 2D (annotated)

127. *Pogge* discloses that a void in a copper filled TSV “has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature.” *Pogge*, ¶[0027]. As seen in the figure above, the structure of the TSV in *Pogge* is very similar to that in *Cooney* and in the ’609 patent. Compare *Pogge*, Fig. 2D, with *Cooney*, Fig. 6 and Ex. 1001, Fig. 4. A skilled artisan would have understood that

because of the common structural features in *Pogge* and *Cooney*, the stress relieving characteristics of the void in *Pogge*'s TSV would also be manifested by the void in *Cooney*'s TSV. In my opinion, therefore, a POSITA would have understood that voids in TSVs like those of *Cooney* would reduce the amount of thermal stress in the substrate generated due to the differences in TCE of the various materials like the conductive filler and the substrate.

128. *Edelstein* is directed to “a self-supporting semiconductor or insulator carrier substrate with conductive through-vias.” *Edelstein*, ¶[0001]. *Edelstein* discloses etching blind vias in substrate 604, forming an insulating layer 603 in the blind vias, filling the vias with metal 615 and providing additional metal 625 to seal void 620 within the via. *Edelstein*, ¶[0049]. Annotated Figure 6F of *Edelstein* illustrates TSVs (e.g., **vias**) including a **conductive filler** (e.g., **metal 615 and 625**) and a **hollow center** (e.g., **void 620**) formed in a **substrate 604**.



Edelstein, Fig. 6F (annotated).

129. *Edelstein* discloses that a “through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures.” *Edelstein*, ¶[0047]. I note that during prosecution of the ’609 patent, the Examiner cited *Edelstein* and *Beyne* for the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate. Section VII.C. As I discussed there, the Applicant of the ’609 patent did not rebut the Examiner’s contention that the voids in the TSVs of both *Edelstein* and *Beyne* reduced the amount of thermal stress on the surrounding substrate.

130. As seen in the Fig. 6F of *Edelstein* above, the structure of the TSV in *Edelstein* is very similar to that in *Pogge*, *Cooney*, and in the ’609 patent. Compare *Edelstein*, Fig. 6F, with *Pogge*, Fig. 2F, *Cooney*, Fig. 6, and Ex. 1001, Fig. 4. A skilled artisan would have understood that because of the common structural features in *Edelstein* and *Cooney*, the stress relieving characteristics of the void in *Edelstein*’s TSV would also be manifested by the void in *Cooney*’s TSV. In my opinion, therefore, a POSITA would have understood that voids in TSVs like those of *Edelstein* or *Cooney* would reduce the amount of thermal stress in the substrate generated due to the differences in coefficient of thermal expansion of materials like the conductive filler and the substrate.

131. A POSITA would have been aware of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials before the earliest priority date of the '609 patent as evidenced by the disclosures of *Pogge* and *Edelstein*. In my opinion, a POSITA would have found it obvious that *Cooney*'s TSV with a void enclosed in the conductor layer would also cause a reduction in the thermal stress in the surrounding substrate consistent with the voids in *Pogge* and *Edelstein*.

132. Moreover, as I discussed above, during prosecution of the '609 patent, the Examiner cited *Edelstein* and *Beyne* for the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate. Section VII.C. Patent Owner acquiesced to the rejection and did not rebut the Examiner's statement. Section VII.C.

133. In view of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*'s TSV to cause a reduction in the thermal stress in the surrounding substrate. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*'s express teaching of including the void.

134. It is my opinion, therefore, that a POSITA would have found limitation [1b-2] obvious over *Cooney* in view of the POSITA's knowledge of the state of the art.

- e. [1b-3]: “said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;”

135. In my opinion, *Cooney* discloses (**Ground 1A**) or alternatively would have rendered obvious (**Ground 1B**) said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward.

136. For example, as I discussed for limitation [1b-2], *Cooney* discloses “a liner layer 22 located and formed conformally upon the semiconductor structure” and “incompletely filling the extended aperture.” *Cooney*, ¶[0055]; Section XI.A.1.d. *Cooney* also discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]; Section XI.A.1.d. Further, *Cooney* discloses that the aperture formed in its semiconductor substrate for the formation of each TSV has varying widths and comprises four regions R1, R2, R3, and R4. Annotated Figure 5 of *Cooney*, below, illustrates the four regions in *Cooney*'s TSV.

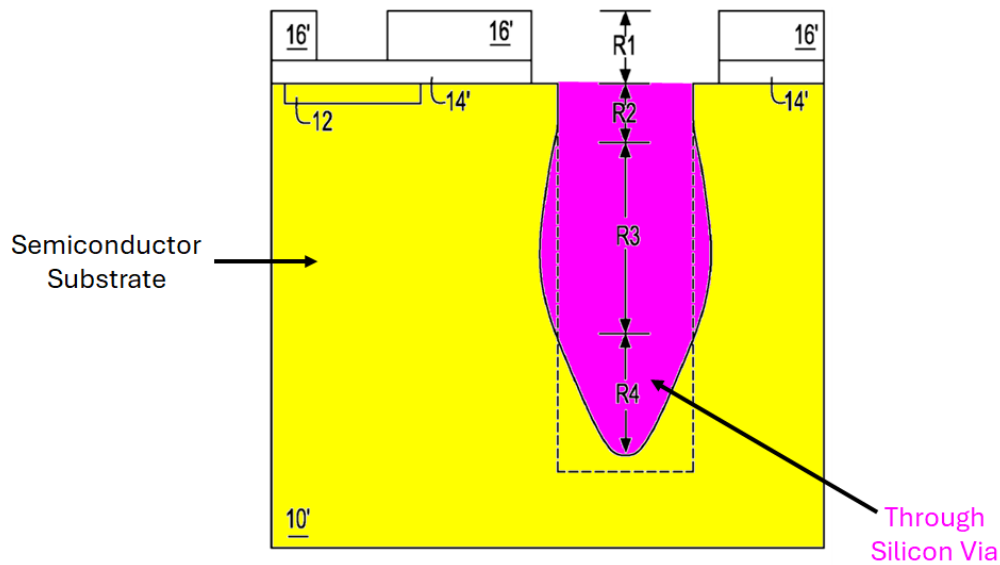


FIG. 5

Cooney, Fig. 5 (annotated).

137. *Cooney* explains that “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3 and to localize that void to the third region R3.” *Cooney*, ¶[0051]. Because *Cooney*’s conductor layer 24 “completely fill[s] the extended aperture” and because the void is completely sealed off and localized in the third region R3, it is my opinion that the conductor layer 24 of *Cooney* entirely surrounds void 25.

Annotated Figure 6 of *Cooney* illustrates this configuration in which the conductive filler (e.g., conductor layer 24) completely surrounds the hollow center (e.g., void 25) disposed in region R3 of *Cooney*’s TSV extending through semiconductor substrate 10.

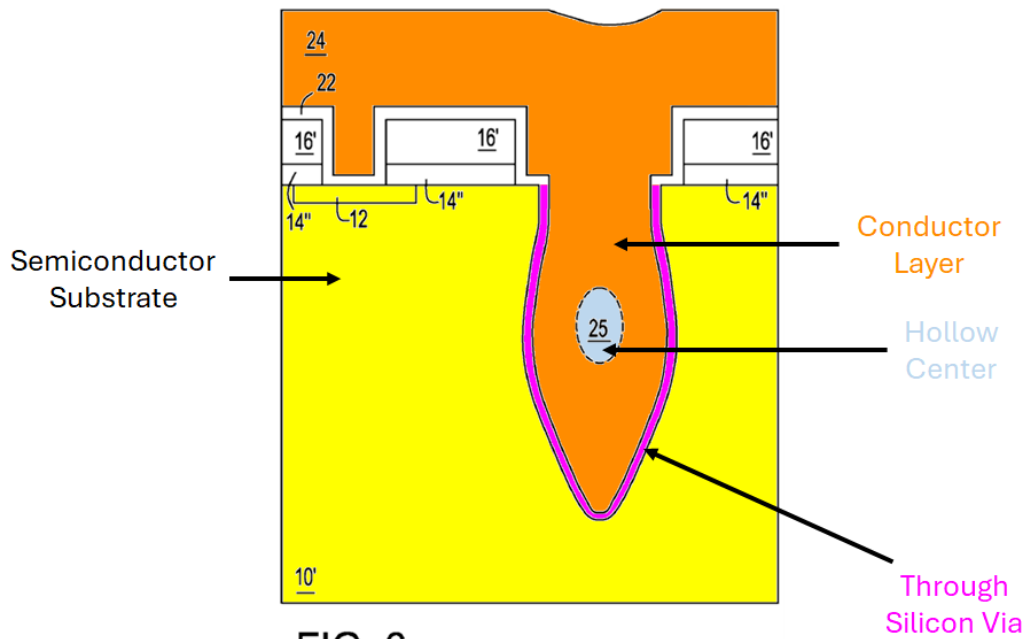


FIG. 6

Cooney, Fig. 6 (annotated).

138. In my opinion, therefore, *Cooney* discloses that the **hollow center** in each of *Cooney*'s **TSVs** is entirely surrounded by said **conductive filler**.

139. **Ground 1A:** Because *Cooney* discloses the presence of the hollow center or void 25, *Cooney*'s void 25 would allow conductor layer 24 to expand inward. As I discussed for limitation [1b-2], the '609 patent discloses that "hollow center portion 432 and pinched off region 438 are formed in through silicon via 402." Ex. 1001, 4:49-50; Section XI.A.1.d. Although the '609 patent states that hollow center portion 432 provides many beneficial features, the '609 patent does not identify any characteristics or properties of the hollow center that contribute to the inward expansion of the conductive filler. Ex. 1001, 4:60-61; *see generally* Ex. 1001. *Cooney*'s TSV also includes a hollow center (e.g., void 25). In my

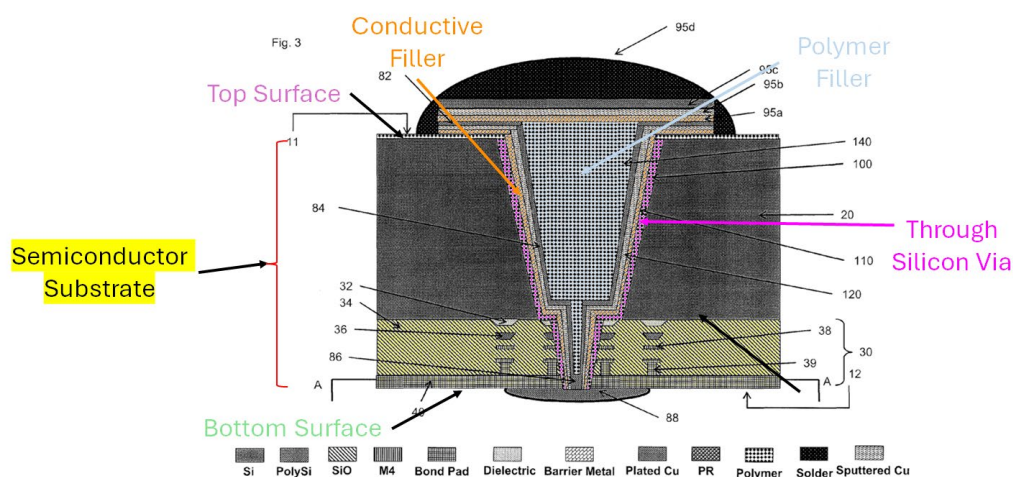
opinion, a POSITA would have understood that void 25 in *Cooney*'s TSV would allow the conductor layer 24 of *Cooney* to expand inward into void 25, *see supra* VI.C.1, consistent with the hollow center of the '609 patent allowing the conductive filler of the '609 patent to expand inward into the hollow center.

140. **Ground 1B:** To the extent the Patent Owner argues otherwise, a POSITA would have found it obvious to include *Cooney*'s purposeful void 25 to "provide space for said conductive filler to expand inward," based on the POSITA's knowledge of the state of the art.

141. A POSITA would have recognized that it was well known that when a relatively compliant material is enclosed by metal in a TSV, the metal expands inward into the compliant material when the temperature of the TSV and surrounding substrate increases. For example, U.S. Patent Publication No. 2011/0304026 to Tsui et al. ("*Tsui*," Ex. 1007) explains this feature. *Tsui* published on December 15, 2011, from an application that was filed on June 14, 2010, before the earliest priority date of the '609 patent. *Tsui* is directed to "a via and a method of via forming and method of via filling, especially but not limited to a through-silicon-via (TSV)." *Tsui*, ¶[0001]. With reference to its Figures 2(a) through 2(d), and 3, *Tsui* discloses a "via that extends all the way through a substrate from a first surface 11 to an opposite second surface 12." *Tsui*, ¶¶[0029], [0037]. *Tsui* further discloses: "Preferably the via comprises an electroplated metal layer surrounding a

polymer filler.” *Tsui*, ¶[0036]. *Tsui* explains that “the via has an outer polymer layer 100, a barrier layer 110, a sputtered metal (e.g. copper) layer 120, an electroplated (e.g. copper) layer 84 and an inner polymer layer 140.” *Tsui*, ¶[0039]. *Tsui* also discloses that barrier layer 110 may be a metal layer. *Tsui*, ¶[0045].

142. *Tsui* also discloses that “a barrier layer 95a and sputtered metal layer 95b are added to the first surface 11” and that “a further electroplated layer 95c is added on top of the sputtered metal layer 95b.” *Tsui*, ¶[0047]. *Tsui* explains that layers 95a-c are metal layers. *Tsui*, ¶[0047]. Annotated Figure 3 of *Tsui*, below, illustrates *Tsui*’s TSV extending through the substrate from a top surface (e.g., first surface 11) to a bottom surface (e.g., second surface 12), and including a metallic conductive filler (e.g., layers 84, 94a-c, 110, and 120) surrounding polymer filler 140. Thus, *Tsui*’s TSV includes a polymer filled center surrounded by a conductive filler.



Tsui, Fig. 3 (annotated).

143. *Tsui* explains that the “metal-polymer-metal structure helps to compensate for the different coefficients of thermal expansion of the non-active region 20 of the substrate (usually formed of silicon) and the electroplated metal layer (usually made of copper).” *Tsui*, ¶[0036]. *Tsui* further explains that “the coefficient of thermal expansion of the electroplated metal is much greater than the coefficient of thermal expansion of the non-active region 20.” *Tsui*, ¶[0036]. *Tsui* discloses that the “simple presence of the filler helps to reduce the problems caused by the differences in coefficients of thermal expansion, first by reducing the volume of the electroplated layer and second by having an intermediate coefficient of thermal expansion itself.” *Tsui*, ¶[0036]. Further, *Tsui* discloses that “the filler layer has a degree of resilience” and “if the electro-plated layer expands, due to a change in temperature, this expansion can be accommodated by a ‘squashing’ of the filler layer.” *Tsui*, ¶[0036]. A skilled artisan would have understood from *Tsui*’s disclosure that the metal layers of *Tsui*’s via would expand inward into the polymer filler to “squash” the filler layer when temperature of *Tsui*’s via increases. Resilience as disclosed by *Tsui* refers to how elastic or compressible a material is when exposed to external stresses.

144. One skilled in the art would further recognize that a void (e.g., void 25 of *Cooney*) filled with a gas is significantly more resilient (elastic or compressible) than the polymer filler included in the TSV of *Tsui*. Thus, the conductive filler

material in *Cooney*'s TSV would more readily expand inward into void 25 as compared to the expansion of *Tsui*'s metal layers into the polymer filler. It would, therefore, have been obvious to a POSITA that when *Cooney*'s TSV and substrate are subjected to an increase in temperature, the conductive filler in *Cooney* would expand inwardly, squashing the gas-filled void.

145. In view of the well-known inward expansion behavior of a conductive filler in a TSV including a void (filled with polymer or gas), a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*'s TSV to allow *Cooney*'s conductor layer to expand inward into the void. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*'s express teaching of including a void in its conductor layer.

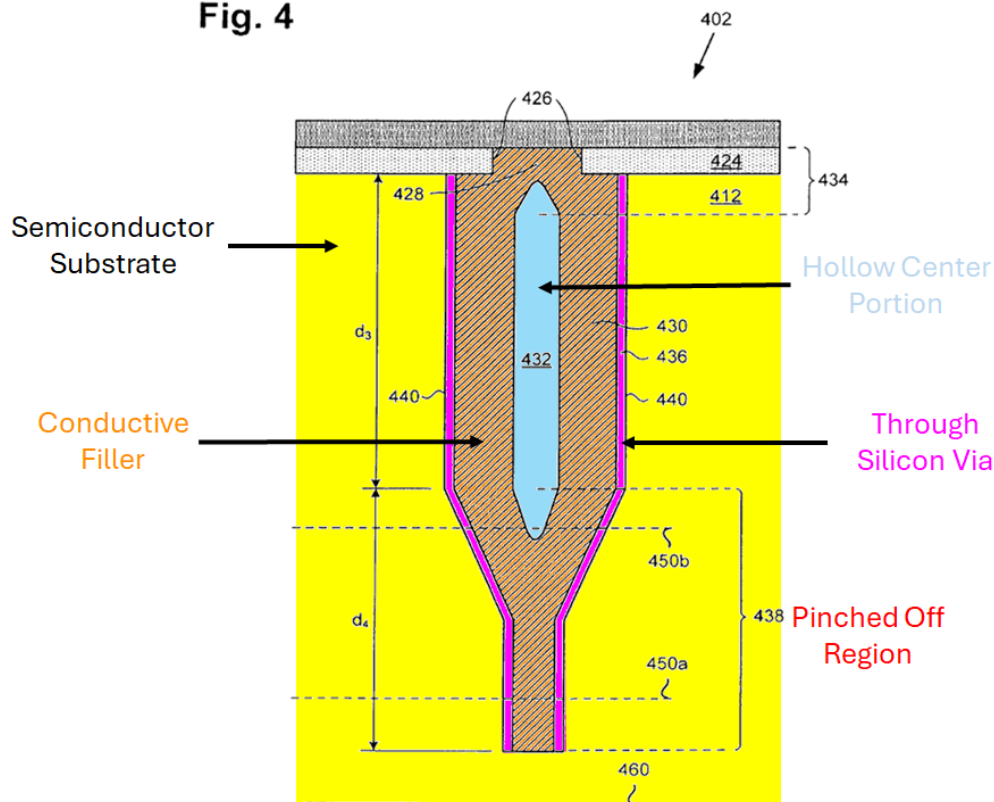
146. It is my opinion, therefore, that a POSITA would have found limitation [1b-3] obvious over *Cooney* in view of the POSITA's knowledge of the state of the art.

- f. [1c-1]: “wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**, and”

147. In my opinion, *Cooney* discloses (**Ground 1A**), or alternatively would have rendered obvious (**Ground 1B**) each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

148. Before discussing the disclosure of *Cooney*, it is helpful to review the disclosure of the '609 patent relative to the claimed “pinched off region at a bottom portion.” For example, the '609 patent simply discloses “hollow center portion 432 and pinched off region 438 are formed in through silicon via 402.” Ex. 1001, 4:49-50. The '609 patent also discloses “pinched off region 438 at a bottom portion of TSV 402.” Ex. 1001, 5:3-4. The '609 patent does not expressly disclose or claim the extent or height of pinched off region 438 other than displaying it in Figure 4 of the '609 patent. Ex. 1001, Fig. 4. Annotated Figure 4, below, illustrates the disclosed **pinched off region 438** at the bottom portion of **TSV 402** of the '609 patent.

Fig. 4



Ex. 1001, Fig. 4 (annotated).

149. As I illustrate below, the pinched off region at the bottom portion of *Cooney's* TSV is mirrors the pinched off region 438 in the '609 patent. For example, *Cooney* discloses an extended aperture having a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶[0042]. Figure 5 of *Cooney*, excerpted below illustrates regions R1, R2, R3, and R4 of the extended aperture corresponding to each TSV in *Cooney's* substrate. *Cooney*, ¶¶[0049]-[0054].

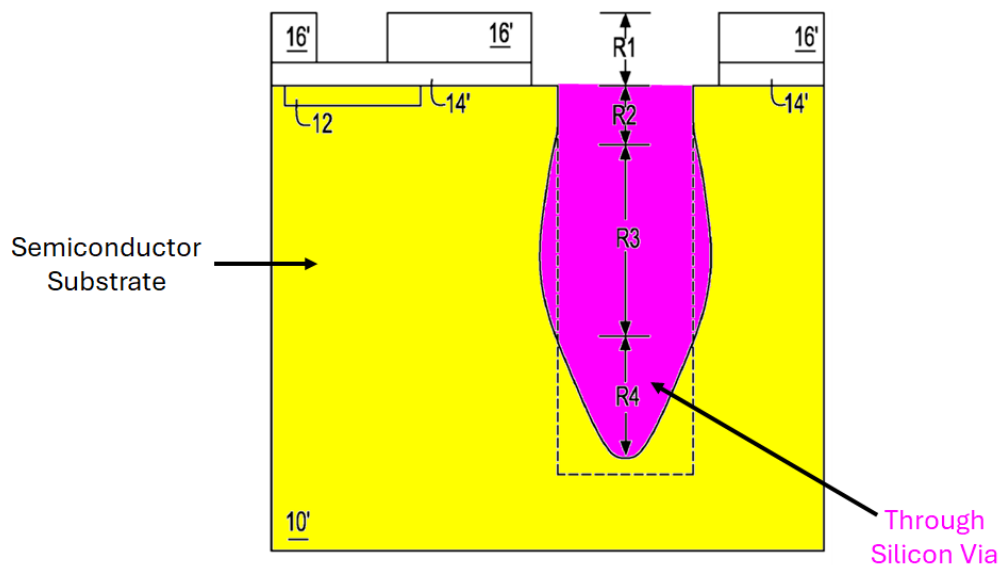


FIG. 5

Cooney, Fig. 5 (annotated).

150. *Cooney* discloses “a liner layer 22 located and formed conformally upon the semiconductor structure” and “incompletely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* also discloses “a conductor layer 24 with an

optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]; *see also Cooney*, Abstract, ¶[0051]. Further, *Cooney* discloses that “the conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.” *Cooney*, ¶[0060].

151. *Cooney* discloses that “the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture.” *Cooney*, ¶[0051]. Further, *Cooney* discloses that “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3.” *Cooney*, ¶[0051]. As a result, the extended aperture is “completely” filled by “a conductor layer 24 with an optional void 25 located therein.” *Cooney*, ¶[0055] (The conductor layer 24 is “formed upon the liner layer 22” within the extended aperture.); *see also Cooney*, Abstract, ¶[0051].

152. According to *Cooney*, “due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.” *Cooney*, ¶[0060]. In my opinion, by localizing void 25, to region R3, *Cooney* discloses a TSV having a pinched off region at a

bottom portion of the TSV. Annotated Figure 6 of *Cooney*, below, illustrates the **pinched off region** of *Cooney*'s TSV. As illustrated in Figure 6, below, the **pinched off region** extends over the narrowing portion of the torpedo shaped **aperture** of *Cooney*. A comparison of *Cooney*'s Figure 6 with Figure 4 of the '609 patent illustrates that the **pinched off region** of *Cooney* extends over the narrowing portion of the torpedo shaped aperture in *Cooney* and is just like the **pinched off region 438** of Fig. 4 of the '609 patent (above).

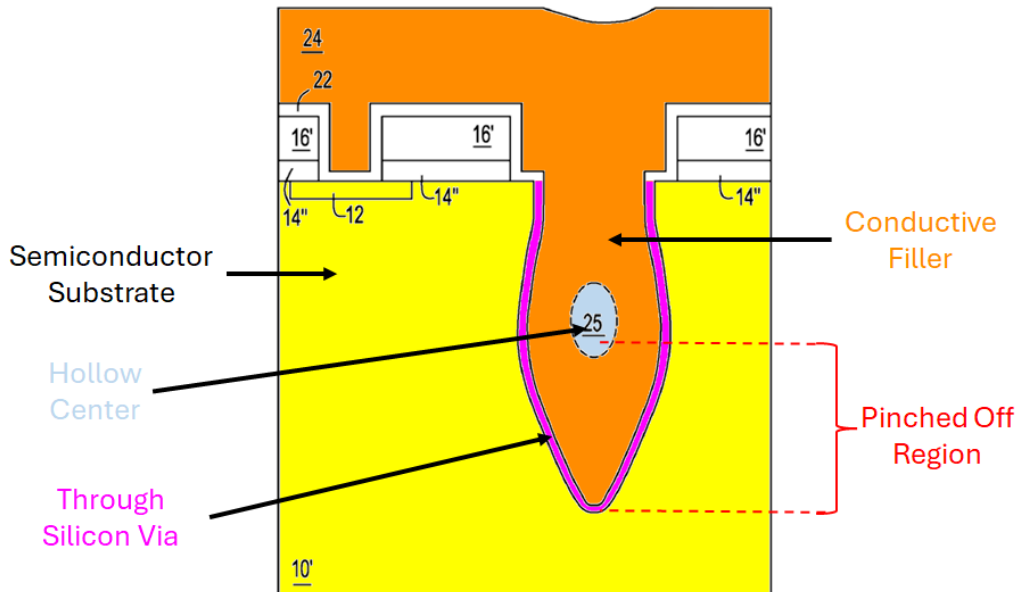


FIG. 6

Cooney, Fig. 6 (annotated).

153. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single TSV, *Cooney*'s **substrate 10** includes a plurality of similar TSVs. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. Each

of the plurality of TSVs of *Cooney* has a pinched off region at a bottom portion of the TSV.

154. **Ground 1A:** Because *Cooney* discloses the presence of a pinched off region at the bottom portion of *Cooney*'s TSV, *Cooney* still teaches claim limitation [1c-1]. The '609 patent discloses "pinched off regions at the bottom and/or the top portions of the through silicon vias, which prevent contamination during processing of the semiconductor substrate." Ex. 1001, Abstract. The '609 patent also discloses that "filling a bottom portion of TSV 402 with conductive filler 430 may ensure that no contamination of TSV 402 occurs during polish action 540." Ex. 1001, 5:31-33. I note that other than disclosing that the presence of pinched off regions prevents contamination, the '609 patent does not identify any other characteristics or properties of the pinched off region that may contribute to preventing contamination. As I discussed above, *Cooney*'s TSVs include a pinched off region at the bottom portion of each TSV. In my opinion, a skilled artisan would have understood that the pinched off region at the bottom portion of each of *Cooney*'s TSVs would prevent contamination during semiconductor processing operations, consistent with the pinched off regions of TSVs 402 of the '609 patent.

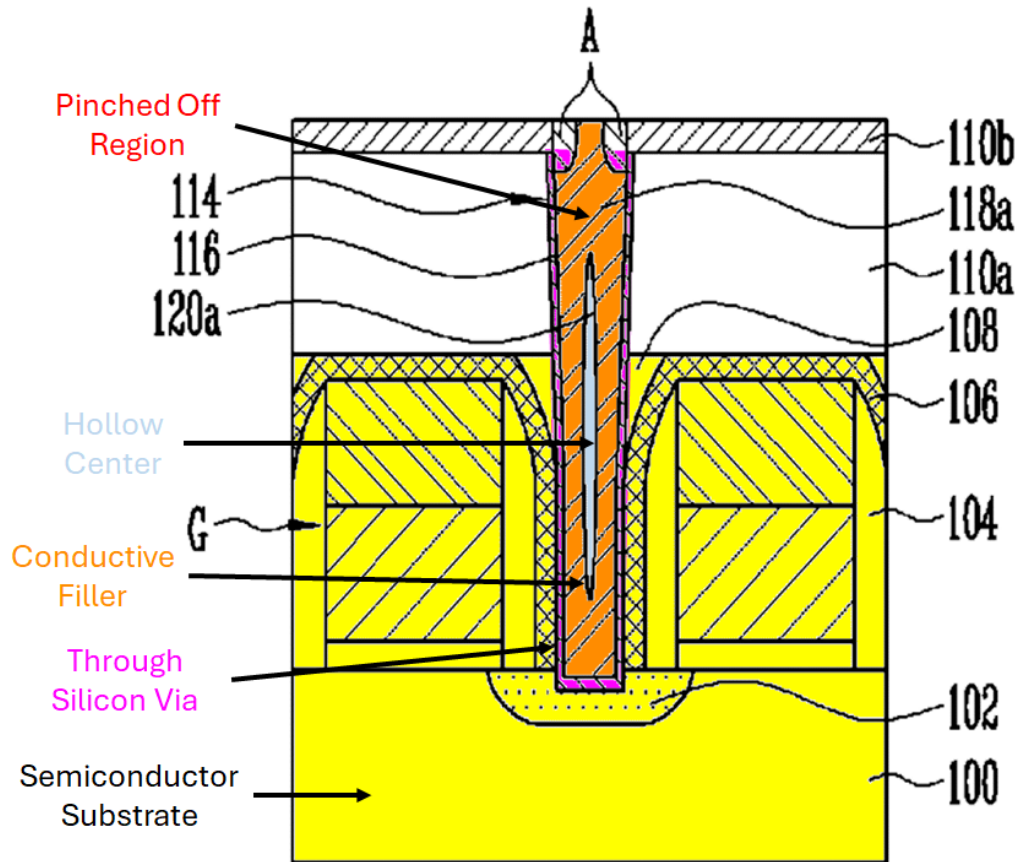
155. **Ground 1B:** To the extent the Patent Owner argues otherwise, a POSITA would have found it obvious to include the pinched off region in

Cooney's TSV to "prevent contamination during processing of said semiconductor substrate."

156. A POSITA would have recognized that it was well known in the art before the earliest priority date of the '609 patent that a via closed at both ends prevents contamination of the via during subsequent semiconductor manufacturing processes. For example, Korean Application No. 10-2010-0011480 to Kim ("*Kim*," Ex. 1013)⁴ published on February 3, 2010, discloses this feature. *Kim* is directed "to a method for manufacturing a semiconductor device" in which a tungsten plug is used for electrical connection between a junction and a gate in a semiconductor substrate. *Kim*, ¶[0001].

157. With reference to its Figs. 1a to 1d, *Kim* discloses forming insulating films 110 on top of a semiconductor substrate. *Kim*, ¶¶[0015]-[0018]. *Kim* further discloses forming a contact hole or via 114 extending through the insulating films and at least a portion of the substrate 100 to expose junction 102 in substrate 100. *Kim*, ¶[0022]. *Kim* discloses filling contact hole 114 with tungsten with a void 120. *Kim*, ¶¶[0027]-[0029]. *Kim* also discloses etching at least a portion of the insulating films 110. *Kim*, ¶[0030]. Annotated Figure 1h of *Kim*, below, illustrates *Kim*'s semiconductor device after the etching step. As shown in the figure, a contact plug 118a is formed at the top of *Kim*'s via.

⁴ Citations to KR 10-2010-0011480 are to the certified English translation.



Kim, Fig. 1h (annotated).

158. *Kim* explains that when “a seam of a tungsten film is present on the top of a tungsten plug, the size of the seam increases during the pre-chemical mechanical polishing (CMP) cleaning process, the CMP process, and the post-CMP cleaning process.” *Kim*, ¶[0002]. As a result, “foreign matter, such as CMP residue or particles, becomes trapped in the seam, [and] the resistance of the contact plug increases due to the effect of these CMP residue or particles, and thereby bridging between contact plugs may occur.” *Kim*, ¶[0002]. To solve this issue, *Kim* discloses that “the seam (120 of FIG. 1g) ... is closed in the vicinity of

the overhang (A),” so “the seam (120 of FIG. 1g) is not exposed when performing the CMP process to form the contact plug (118a).” *Kim*, ¶[0032]. Further, because “the seam (120 in FIG. 1g) in the metal layer (118 in FIG. 1g) is not exposed during the CMP process,” *Kim* explains that after “lower seam (120a) inside the contact plug (118a) can be prevented from becoming exposed and increasing in size during the subsequent post-CMP cleaning process.” *Kim*, ¶[0033].

Accordingly, it is possible to prevent “the intrusion of foreign matter such as CMP residue or particles into the lower seam (120a),” during any of the pre-chemical mechanical polishing (CMP) cleaning process, the CMP process, and the post-CMP cleaning process. *Kim*, ¶[0033]. This occurs because the “seam . . . is closed in the vicinity where the overhang occurred.” *Kim*, ¶[0029], Figs. 1g-1h.

159. Thus, *Kim* explains that by closing off the seam, the seam is prevented from becoming exposed during subsequent CMP process, which thereby inhibits “foreign matter becoming caught inside the seam.” *Kim*, ¶¶[0012], [0027]-[0033], Fig. 1h.

160. Thus, a skilled artisan would have POSITA would have understood that, like *Kim*’s closed seam, the conductor layer in *Cooney* completely surrounds the void on all sides, so the pinched off region of *Cooney*’s TSV would also prevent metal contamination or particle contamination during any subsequent processes such as polishing or etching of the substrate.

161. *Kim* illustrates that it was well known in the art before the earliest priority date of the '609 patent that pinched off regions at the top portion and/or bottom portion of a metal filled via help to prevent contamination of the via during subsequent semiconductor manufacturing processes. In view of this well-known function of pinched portions of a via, in my opinion, a POSITA would have found it obvious to include the pinched off region in *Cooney's* TSV to prevent contamination during subsequent processing of *Cooney's* semiconductor substrate. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney's* express teaching of including the pinched off region.

162. Indeed, consistent with the teachings of the '609 patent, *Cooney's* TSV has no unwanted gaps between the conductor layer 24" and the liner layer 22", or between the liner layer 22" and/or the substrate 10 either at the top surface or bottom surface of substrate 10. For example, in its "BACKGROUND" section, the '609 patent discloses that "conventional fabrication methods result in incomplete filling of the TWVs, especially at their top and bottom portion" that "result in unwanted gaps in the top and bottom portions of the TWVs ." Ex. 1001, 1:45-48. The '609 patent discloses that these unwanted gaps "lead to contamination of the TWVs during subsequent processes." Ex. 1001, 1:49-50. *Cooney* discloses that the shape of its extended aperture "aids in efficiently filling the aperture with the through substrate via 24." *Cooney*, ¶[0066]. And as I have

discussed above, *Cooney* also discloses a conductor layer 24 completely filling the extended aperture. *Cooney*, ¶[0055]. Because the conductor layer 24 of *Cooney* efficiently and completely fills *Cooney*'s extended aperture, a POSITA would recognize that there are no unwanted gaps in the top and bottom portions of *Cooney*'s TSV. For example, as seen in Figure 9 of *Cooney*, below, there are no unwanted gaps between conductor layer 24" and liner layer 22", or between liner layer 22" and/or substrate 10 either at the top surface or bottom surface of substrate 10.

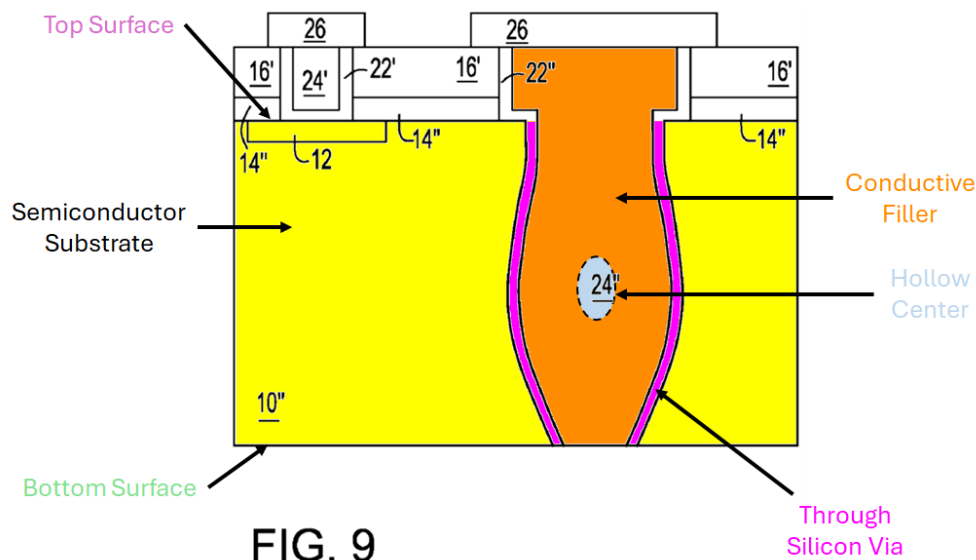


FIG. 9

Cooney, Fig. 9 (annotated).

163. In my opinion, therefore, consistent with the '609 patent, in the absence of any unwanted gaps in *Cooney*, a POSITA would have found it obvious that there would be no contamination of *Cooney*'s TSV during subsequent semiconductor manufacturing processes.

164. Accordingly, a POSITA would have found limitation [1c-1] obvious over Cooney in view of the POSITA's knowledge of the state of the art.

g. [1c-2]: “wherein said hollow center is tapered in said pinched off region.”

165. In my opinion, *Cooney* teaches (**Ground 1A**) or alternatively would have rendered obvious (**Ground 1B**) that said hollow center is tapered in said pinched off region.

166. As I discussed above for claim [1c-1], and as illustrated in Figure 5, below, *Cooney* discloses an extended aperture having a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶¶[0042], [0049]-[0054]. As illustrated in Figure 5 of *Cooney* below, the walls of the aperture are tapered towards the bottom of the substrate (e.g., in regions R3 and R4) due to the disclosed “downward pointing torpedo shape” of the aperture.

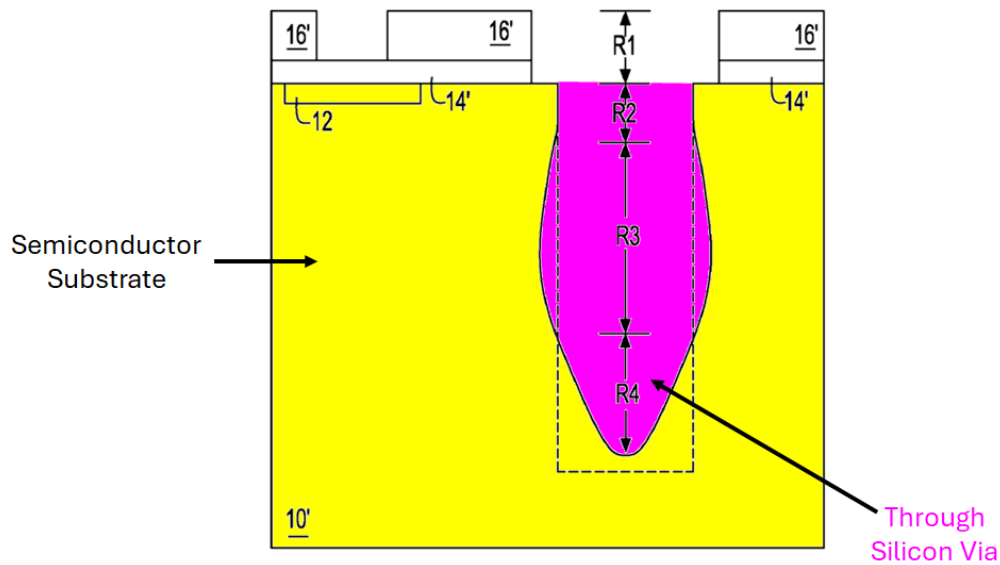


FIG. 5

Cooney, Fig. 5 (annotated).

167. *Cooney* discloses “a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* explains that the liner layer 22 “may be deposited with enhanced adhesion using an atomic layer chemical vapor deposition,” consistent with the ’609 patent.⁵ *Cooney*, ¶[0058]. Further, *Cooney* discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* explains that “the conductor layer 24 typically comprises

⁵ The ’609 patent discloses that depositing conductive filler on sidewalls of through silicon via “may be accomplished using any appropriate deposition technique, such as chemical vapor deposition (CVD) or atomic layer deposition (ALD), for example.” ’609 patent, 4:47-59.

a tungsten material” and that “[s]uch a tungsten material is preferably deposited using a chemical vapor deposition method[.]” *Cooney*, ¶[0059].

168. A skilled artisan would have understood that conformal deposition would cause the deposited material layer to conform to and take the shape of the underlying structure. Therefore, a skilled artisan would have understood that chemical vapor deposition of conductor layer 24 in *Cooney*’s aperture would cause the conductor layer 24 to conformally follow the underlying tapered shape of the aperture walls.

169. Because the conductor layer 24 defines the boundary of void 25, the conformal deposition of conductor layer 24 would cause void 25 to also have a tapered bottom portion to match the tapered shape of the aperture in the semiconductor substrate 10, as shown below in Figure 6.

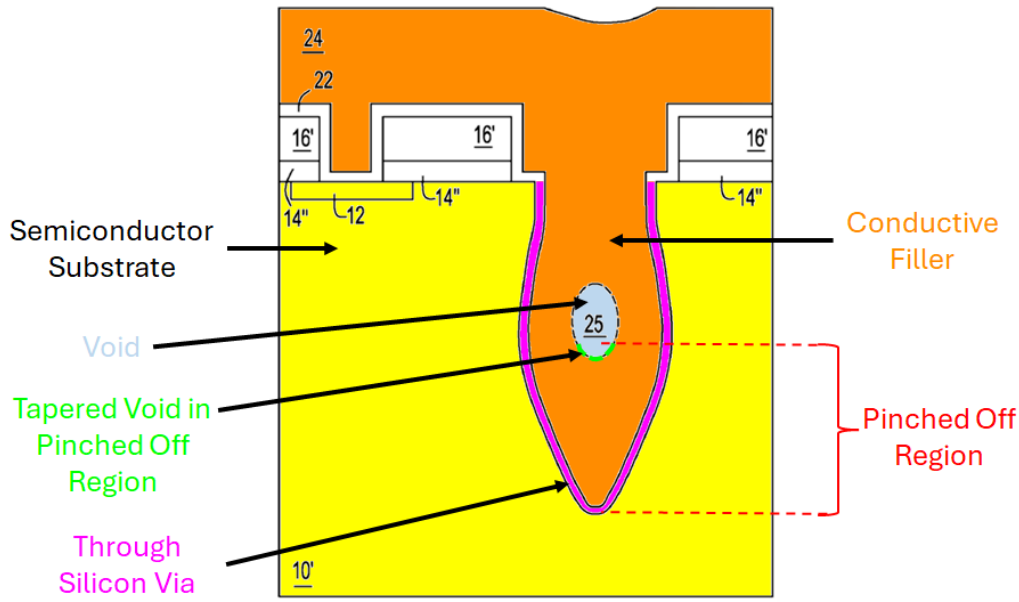


FIG. 6

Cooney, Fig. 6 (annotated).

170. To the extent the Patent Owner argues otherwise, a skilled artisan would have found this feature to be obvious based on the skilled artisan's knowledge of the state of the art. It was well known in the art that conformal deposition processes like chemical vapor deposition cause the deposited material to follow the shape of the underlying surface. For example, U.S. Patent Publication No. 2011/0159690 to Chandrashekar et al. ("*Chandrashekar*," Ex. 1008) discloses this feature. *Chandrashekar* published on June 30, 2011, from an application filed on January 28, 2011 and claiming priority to an application filed July 9, 2010. *Chandrashekar* is directed to methods and apparatuses for filling high aspect ratio features with tungsten-containing materials." *Chandrashekar*, ¶[0004]. *Chandrashekar* discloses "a semiconductor substrate containing a high aspect ratio

feature.” *Chandrashekar*, ¶[0029]. Further, *Chandrashekar* discloses depositing an under-layer lining the feature hole. *Chandrashekar*, ¶[0030]. *Chandrashekar* also discloses filling the feature hole with tungsten-containing materials.

Chandrashekar, ¶[0031]. *Chandrashekar* discloses that the “deposition process may result in a conformal layer of the materials [] built-up over the under-layer.”

Chandrashekar, ¶[0031]. *Chandrashekar* explains that the “deposition layer follows the shape of the under-layer.” *Chandrashekar*, ¶[0031].

171. As another example, U.S. Patent Publication No. 2011/0193241 to Yen et al. (“*Yen*,” Ex. 1009) also discloses material deposited via a conformal deposition process follows the shape of the underlying surface. *Yen* published on August 11, 2011, from an application filed on February 9, 2011, and claiming priority to a provisional application filed on May 5, 2010. *Yen* is directed to “a chip package having a through substrate hole and formation method thereof.” *Yen*, ¶[0003]. *Yen* discloses “a hole 108 having an ‘inverted angle’ structure” formed in the substrate. *Yen*, ¶[0061]. *Yen* discloses that “an insulating layer 112 capable of being exposed and developed is formed on a sidewall and a bottom of the hole 108.” *Yen*, ¶[0061]. Further, *Yen* discloses “an insulating layer 110 is formed on the sidewall and the bottom of the hole 108.” *Yen*, ¶[0063]. *Yen* also discloses that “a conducting layer 114 is formed in the hole 108.” *Yen*, ¶[0064]. *Yen* explains: “Because the insulating layer 110 is conformally formed on the insulating layer

112a, a profile of the insulating layer 110 may also help the following formation of a conducting layer.” *Yen*, ¶[0063]. Annotated Fig. 3C of *Yen*, below, illustrates the conducting layer 114 formed conformally and taking the shape of the underlying insulating layer 110.

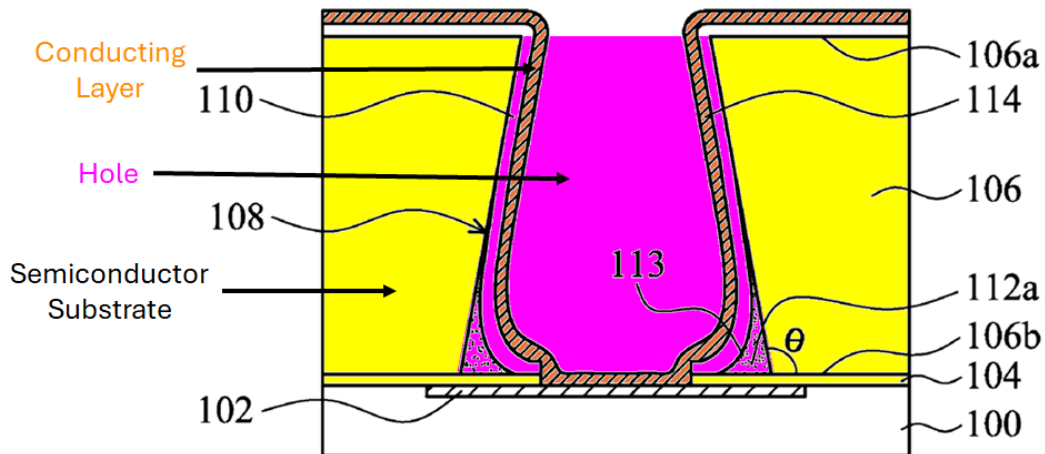


FIG. 3C

Yen, Fig. 3C (annotated).

172. A skilled artisan would have understood that material deposited using a conformal deposition process causes the deposited material to take the shape of the underlying layer. A POSITA would have recognized that *Cooney*’s conformal deposition processes would have caused the deposited layer to take the shape of the underlying surface. Accordingly, a POSITA would have recognized that the surface of the conductor layer, which forms the void in *Cooney*’s TSV, would take on a tapered shape similar to the underlying tapered shape of the aperture in *Cooney*. Annotated Figure 6 of *Cooney*, below, illustrates the tapered shape of the

Diagram illustrating a cross-section of a semiconductor device structure, showing a void in a conductive filler region.

Labels and Dimensions:

- Semiconductor Substrate:** Indicated by an arrow pointing to the yellow region.
- Void:** Indicated by an arrow pointing to the central void in the conductive filler.
- Tapered Void in Pinched Off Region:** Indicated by an arrow pointing to the tapered void in the conductive filler.
- Through Silicon Via:** Indicated by an arrow pointing to the central void in the conductive filler.
- Conductive Filler:** Indicated by an arrow pointing to the orange region.
- Pinched Off Region:** Indicated by a bracket on the right side of the diagram.
- Dimensions:**
 - 24 (Top layer thickness)
 - 22 (Layer thickness below 24)
 - 16' (Layer thickness below 22)
 - 14" (Layer thickness below 16')
 - 12 (Layer thickness below 14")
 - 14" (Layer thickness below 12)
 - 10' (Bottom layer thickness)
 - 25 (Central void diameter)

Cooney, Fig. 6 (annotated).

2. **Claim 2:** “The **semiconductor substrate** of claim 1, wherein said **pinched off region** is formed by **tapering** a bottom portion of each of said plurality of **through silicon vias.**”

174. In my opinion, *Cooney* also discloses said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

175. As I discussed above with respect to claim 1, Cooney discloses forming an extended aperture having a “downward pointing torpedo shape” in a semiconductor substrate 10. Cooney, ¶[0042]; Section XI.A.1. Cooney discloses forming an extended aperture that includes “sequentially contiguous” regions such as a first region R1 at the top portion that is “comparatively wide region,” a second region R2 “that is a constricted region,” a third region R3 that is “comparatively wide region,” and a fourth region R4 at the bottom portion that has a generally “pointed inward taper,” as shown below. Cooney, ¶¶[0049]-[0054]. Figure 5 of Cooney, excerpted below illustrates regions R1, R2, R3, and R4 of the extended aperture. Cooney, ¶¶[0049]-[0054]; Fig. 5.

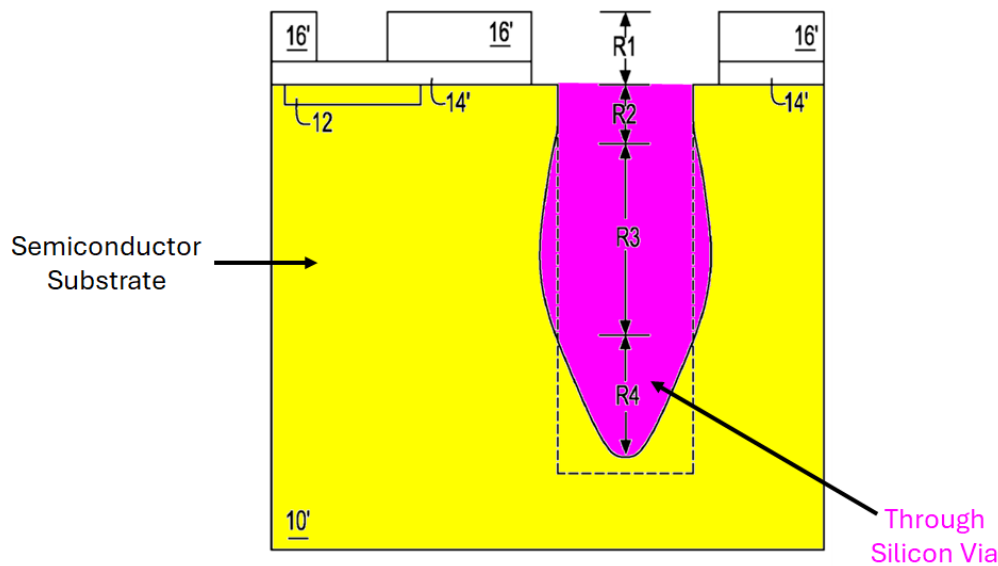


FIG. 5

Cooney, Fig. 5 (annotated).

176. The extended aperture thus has a “downward pointing torpedo shape” at the bottom portion of *Cooney*’s TSV. *Cooney*, ¶[0042].

177. *Cooney* explains that “the comparatively wide linewidth of the first region R1, the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture.” *Cooney*, ¶[0051]. *Cooney* further explains that “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3.” *Cooney*, ¶[0051]. *Cooney* also discloses that “the conductor layer 24 is deposited conformally to follow the extended aperture’s sidewall, “due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.” *Cooney*, ¶[0060].

178. In my opinion, these disclosures of *Cooney* illustrate that “substantially bowed sidewalls” in region R3 help to ensure that a void is formed while the aperture is filled with a conductor layer, and the “inward taper” within the region R4, similar to the constriction within the second region R2, helps to seal off and completely enclose the void in the conductor layer at the bottom portion, and to localize any void to region R3. Thus, tapering the bottom portion of the TSV as disclosed by *Cooney*, forms the pinched off region at the bottom portion of the extended aperture. Figure 6 of *Cooney*, below, illustrates the **pinched off region**

formed because of the **tapered walls** of the bottom portion of *Cooney's* extended **aperture or TSV** that help to localize the **hollow center portion** (e.g., **void 25**) to region R3.

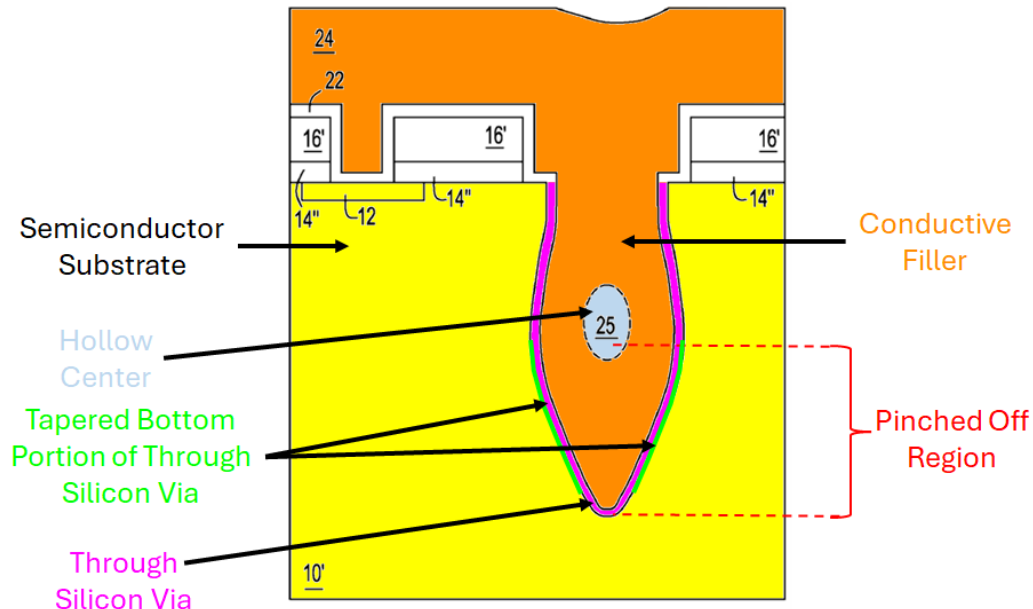


FIG. 6

Cooney, Fig. 6 (annotated).

179. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single **TSV**, *Cooney's* **substrate 10** includes a plurality of similar **TSVs**. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. Thus, in my opinion, *Cooney* includes a plurality of **TSVs**, each of which includes a **tapered bottom portion** that helps to form the **pinched off region** at the bottom portion of the **extended aperture** for each respective **TSV**.

3. Claim 3: “The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.”

180. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

181. In my opinion, *Cooney* further discloses said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

182. As I discussed above for claim limitation [1c-1], *Cooney* discloses that the pinched off region at the bottom portion of *Cooney*’s TSV prevents contamination during processing of said semiconductor substrate. *Cooney* discloses “backside planarizing of the semiconductor substrate 10’, the liner layer 22’ and the conductor layer 24’[.]” *Cooney*, ¶[0063]. *Cooney* explains that “[s]uch a backside planarizing is intended to remove a thickness from about 0.1 to about 10 microns from the semiconductor substrate 10’ while leaving exposed portions of both the liner layer 22” and the conductor layer 24”.” *Cooney*, ¶[0063]. *Cooney* also discloses that the backside planarizing may use methods such as “mechanical polish planarizing methods and chemical mechanical polish planarizing methods.” *Cooney*, ¶[0063]. Figure 9 of *Cooney* illustrates the semiconductor substrate 10”, liner layer 22” and conductor layer 24” that result from a backside planarizing.

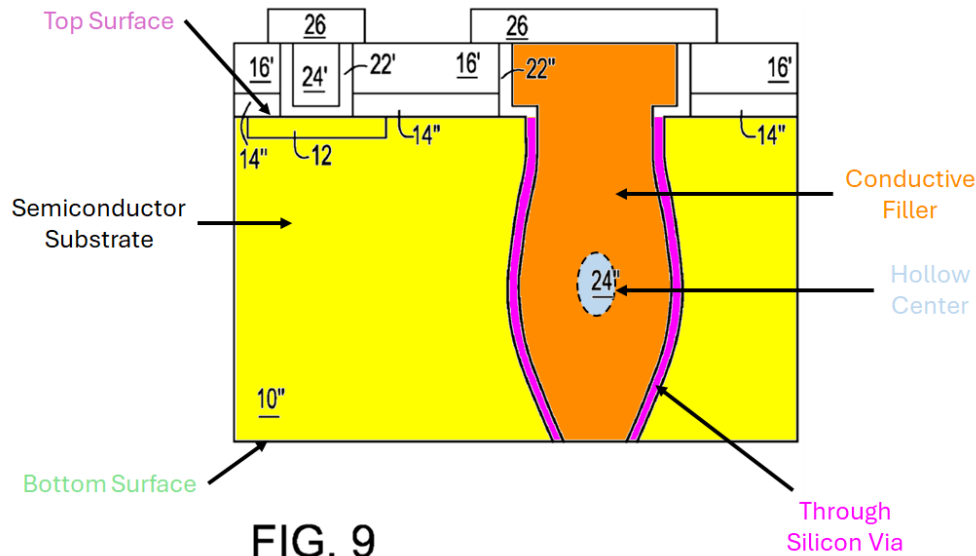


FIG. 9

Cooney, Fig. 9 (annotated and modified to include the void as shown in Fig. 6).

183. As Figure 9 of *Cooney* illustrates, there are no unwanted gaps between conductor layer 24" and liner layer 22", or between liner layer 22" and/or substrate 10 either at the top surface or bottom surface of substrate 10. As I discussed for claim limitation [1c-1], because there are no gaps, any contamination or debris generated during mechanical polish planarizing methods and/or chemical mechanical polish planarizing methods used to perform the backside planarizing would not be able to enter the TSV in *Cooney*. In my opinion, therefore, *Cooney* discloses preventing contamination during polishing of the bottom surface of the substrate. Furthermore, as I discussed for limitation [1c-1], a POSITA would have found it obvious to include the pinched off region in *Cooney*'s TSV to prevent contamination during subsequent processing of *Cooney*'s semiconductor substrate. Moreover, because the conductor layer in *Cooney* completely fills the TSV and

surrounds the void on all sides, the **pinched off region** of *Cooney*'s **TSV** would also prevent metal contamination or particle contamination during any subsequent processes such as polishing or etching of the substrate, including during polishing said bottom surface of said substrate. Section XI.A.1.f; *Kim*, ¶¶[0012], [0027]-[0033], Fig. 1h.

4. Claim 4: “The semiconductor substrate of claim 1, wherein said **conductive filler comprises a **metallic filler**.”**

184. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

185. In my opinion, *Cooney* also discloses said conductive filler comprises a metallic filler.

186. For example, as I discussed for claim limitation [1b-1], *Cooney* discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* explains that “the conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys.” *Cooney*, ¶[0059]; Section XI.A.1.c.

187. In my opinion, because the **conductor layer 24** constitutes the **conductive filler** in *Cooney*'s **TSV** and because **conductor layer 24** includes metals or metal alloys, *Cooney* discloses that the **conductive filler** (e.g., **conductor layer 24**) in *Cooney*'s **TSVs** is a **metallic filler**.

5. Claim 5: “The semiconductor substrate of claim 1, wherein said **conductive filler comprises **tungsten**.”**

188. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

189. In my opinion, *Cooney* also discloses said conductive filler comprises tungsten.

190. For example, as I discussed for claim 4, *Cooney* teaches a conductor layer 24 that comprises comprise any of several conductor materials, including but not limited to any of several metals and metal alloys.” See Section XI.A.4. *Cooney* also discloses “the conductor layer 24 typically comprises a **tungsten** material.” *Cooney*, ¶[0059].

191. In my opinion, because the **conductor layer 24** constitutes the **conductive filler** in *Cooney*’s **TSV** and because **conductor layer 24** includes **tungsten**, *Cooney* discloses that the **conductive filler** (e.g., **conductor layer 24**) in *Cooney*’s **TSVs** comprises **tungsten**.

6. Claim 6: “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.”

192. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

193. In my opinion, *Cooney* also discloses each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

194. As I discussed for claim 2, *Cooney* discloses that the “substantially bowed sidewalls” in region R3 helps to ensure that a void is formed while the aperture is filled with a conductor layer, and the “inward taper” within the region R4 helps to seal off and completely enclose the void in the conductor layer at the bottom portion, and to localize any void to region R3. *See* Section XI.A.2. Thus, the tapered bottom portion of the TSV as disclosed by *Cooney*, helps to seal off or pinch the “hollow center” (e.g., void 25) formed within the “conductive filler” (e.g., conductor layer 24) as illustrated in Figure 6 of *Cooney*, below.

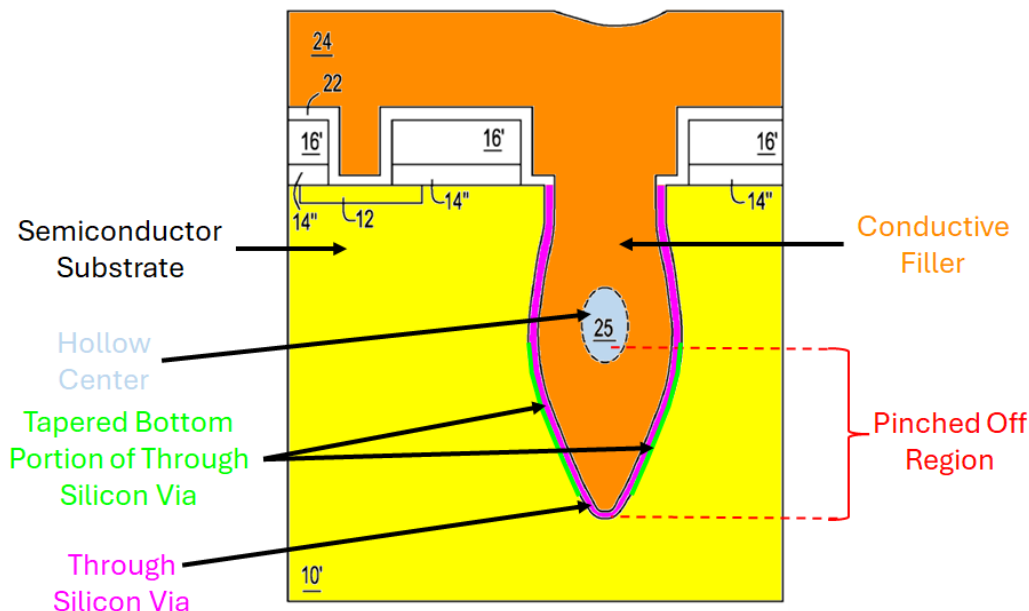


FIG. 6

Cooney, Fig. 6 (annotated).

195. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single TSV, *Cooney*'s substrate 10 includes a plurality of similar TSVs. *Cooney*, ¶[0066]; *see also Cooney*, Abstract, ¶¶[0018], [0020]. In my opinion, therefore, the tapered bottom portion of each of *Cooney*'s TSVs help to seal off or pinch the “hollow center” (e.g., void 25) formed within the “conductive filler” (e.g., conductor layer 24) as illustrated in Figure 6 of *Cooney*, above.

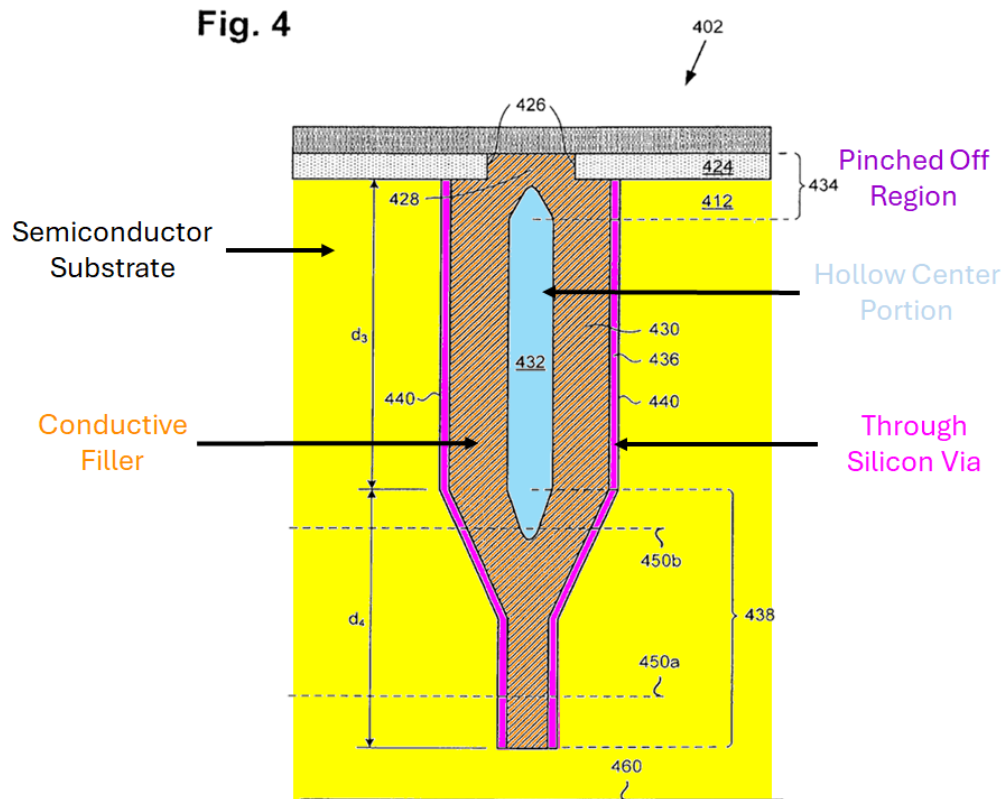
7. Claim 9: “The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.”

196. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

197. In my opinion, *Cooney* also discloses a pinched off region at a top of each of said plurality of through silicon vias.

198. Before discussing the disclosure of *Cooney*, it is instructive to review the disclosure of the '609 patent relative to the claimed “pinched off region at a top of each of said plurality of through silicon vias.” For example, the '609 patent discloses “forming pinched off region 434 at a top portion of TSV 402.” Ex. 1001, 5:4-5. The '609 patent also discloses “forming opening 428 ensures pinched off region 434 is formed in the top region of TSV 402.” Ex. 1001, 5:14-16. The '609 patent does not expressly disclose the extent or height of pinched off region 434

other than displaying it in Figure 4 of the '609 patent. Ex. 1001, Fig. 4. Annotated Figure 4 of the '609 patent, below, illustrates the disclosed **pinched off region 434** formed in the top region of **TSV 402**.



Ex. 1001, Fig. 4 (annotated).

199. As I illustrate below, the pinched off region at the top of *Cooney*'s TSV is similar to the pinched off region 434 in the '609 patent. For example, *Cooney* discloses an extended aperture having a "downward pointing torpedo shape" for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶[0042]. Figure 5 of *Cooney*, excerpted below illustrates regions R1, R2,

R3, and R4 of the extended aperture corresponding to each TSV in *Cooney's* substrate. *Cooney*, ¶¶[0049]-[0054].

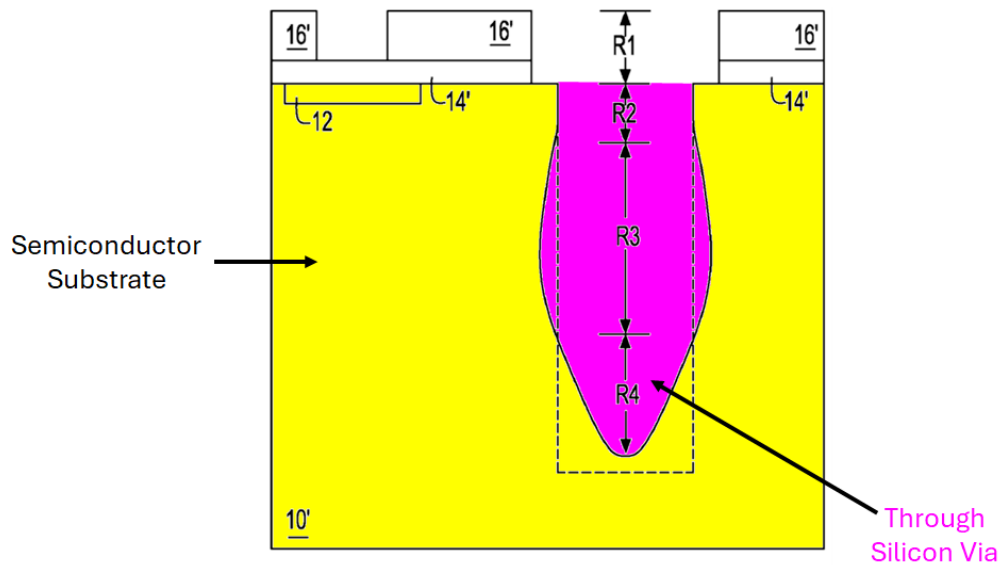


FIG. 5

Cooney, Fig. 5 (annotated)

200. *Cooney* explains that “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3.” *Cooney*, ¶[0051]. Specifically, *Cooney* discloses “a liner layer 22 located and formed conformally upon the semiconductor structure” and “incompletely filling the extended aperture.” *Cooney*, ¶[0055]. *Cooney* also discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]; *see also Cooney*, Abstract, ¶[0051]. Further, *Cooney* discloses that “the conductor layer 24 may be deposited

or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.” *Cooney*, ¶[0060].

201. In my opinion, the portion between the top surface of the **TSV** and the area where the void is *sealed off with the conductor layer 24* forms the **pinched off region** at the top of the **TSV**. A comparison of *Cooney*’s Figure 6 with Figure 4 of the ’609 patent illustrates that the **pinched off region** of *Cooney*, Fig. 6 (below) is just like the **pinched off region 434** of Fig. 4 of the ’609 patent (above).

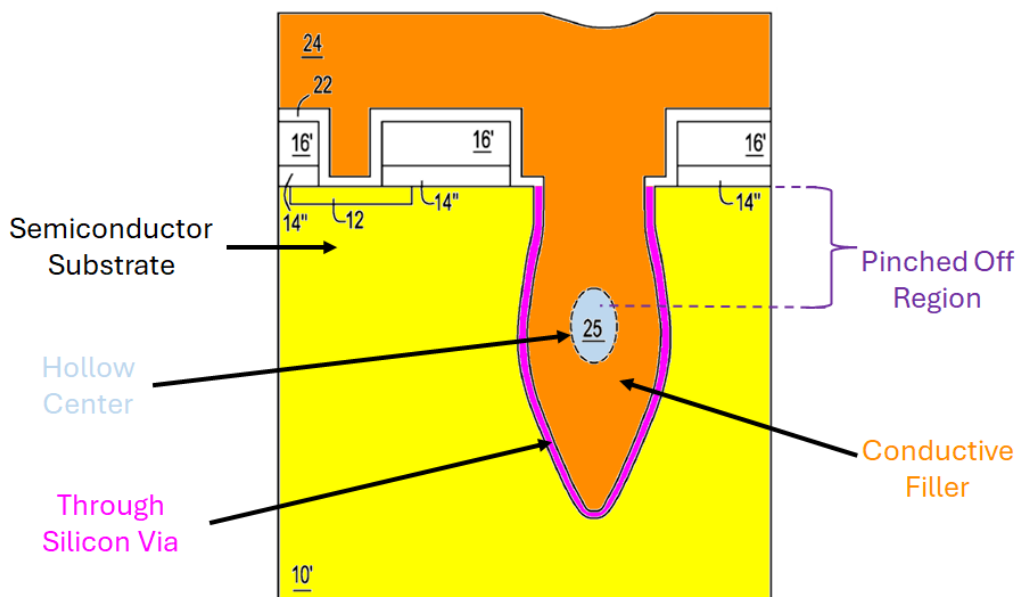


FIG. 6

Cooney, Fig. 6 (annotated).

202. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single **TSV**, *Cooney*’s **substrate 10** includes a plurality of similar **TSVs**. *Cooney*, ¶[0066]; *see also Cooney*, Abstract, ¶¶[0018], [0020]. In

my opinion, therefore, each of the plurality of TSVs in *Cooney*'s substrate 10 has a pinched off region at a top of the TSV as shown in annotate Figure 6 above.

8. Claim 10: “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills bottom portion, narrowing said hollow center.”

203. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 1.

204. In my opinion, *Cooney* also discloses that each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills bottom portion, narrowing said hollow center.

205. As I discussed above for claim limitation [1c-1], and as illustrated in Fig. 5, below, *Cooney* discloses an extended aperture having a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶¶[0042], [0049]-[0054]. As illustrated in Figure 5 of *Cooney*, below, the walls of the aperture are tapered towards the bottom of the substrate due to the disclosed “downward pointing torpedo shape” of the aperture.

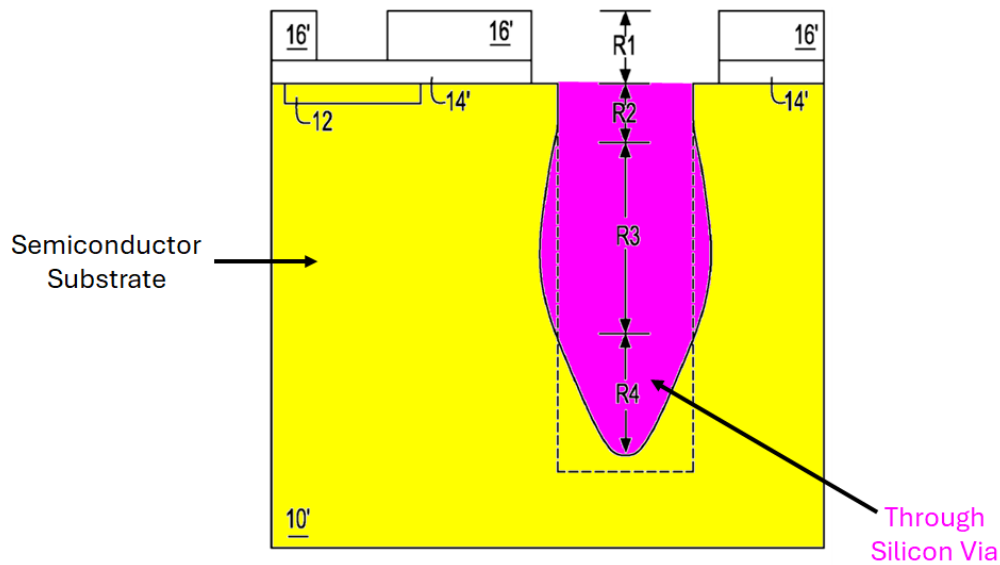


FIG. 5

Cooney, Fig. 5 (annotated).

206. Further, as *Cooney* discloses, when a conductor layer 24 completely fills the extended aperture, the conductor layer 24 would conformally take the shape of the underlying surface of the extended aperture. *Cooney*, ¶[0055]. As a result, the conformal deposition of conductor layer 24 would cause the conductor layer 24 to follow the underlying tapered shape at the bottom portion of the extended aperture. *Cooney*, ¶[0055]. A POSITA reading *Cooney* would have recognized that the tapered shape at the bottom further causes the conductive filler to incompletely fill at the bottom portion of the void, thus narrowing the void 25, to correspond to the tapered shape of the aperture in *Cooney*'s semiconductor substrate 10. As illustrated in Figure 6 of *Cooney*, below, *Cooney* discloses a TSV tapered at the bottom portion such that conductive filler (e.g. "conductor layer 24")

incompletely fills the bottom portion of the TSV, narrowing the “hollow center” (e.g., void 25).

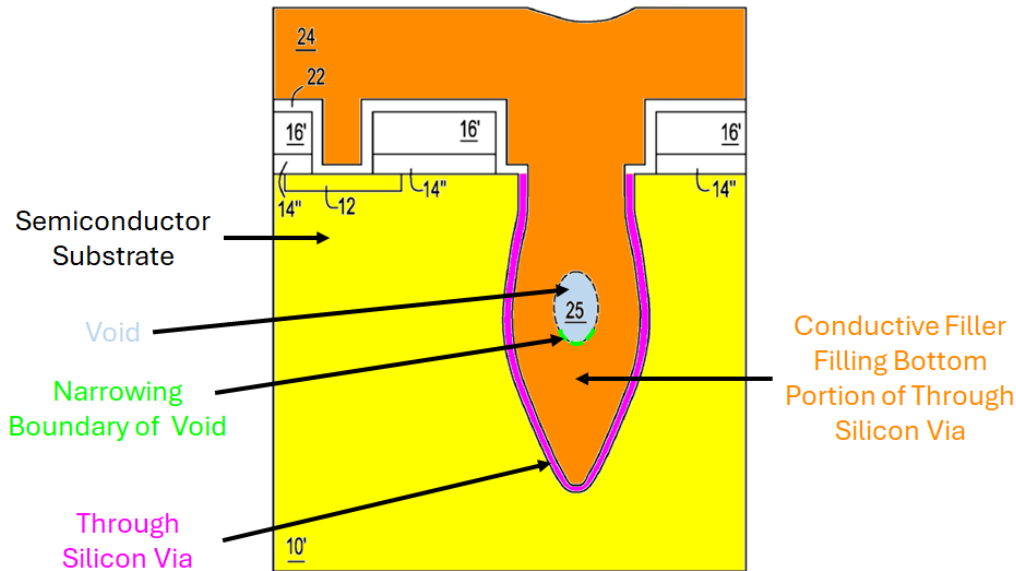


FIG. 6

Cooney, Fig. 6 (annotated).

207. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single TSV, *Cooney*'s substrate 10 includes a plurality of similar TSVs. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. In my opinion, therefore, each of *Cooney*'s plurality of TSVs is tapered at a bottom portion such that the conductive filler incompletely fills bottom portion, narrowing the hollow center in each of *Cooney*'s TSVs.

9. Claim 11:

208. *Cooney* discloses or would have rendered obvious every element of independent claim 11 in the same manner as explained above for independent claim 1. *See* Section XI.A.1.

- a. [11pre]: “A **semiconductor substrate** having a plurality of **devices**, said semiconductor substrate comprising:”
[11a]: “a plurality of **through silicon vias** disposed in said **substrate** extending from a **top surface** of said substrate to a **bottom surface** of said substrate;”
[11b]: “a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;”

209. Claim limitations [11pre]-[11b] are substantively identical to limitations [1pre]-[1b-3]. In my opinion, *Cooney* anticipates or renders obvious limitations [11pre]-[11b] for reasons similar to those I discussed for claim limitations [1pre]-[1b-3]. *See* Sections XI.A.1.a-XI.A.1.e.

- b. [11c]: “wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.”

210. Claim limitation [11c] includes recitations substantially identical to the recitations in claim limitations [1c-1] and [1c-2], and claim 9. The primary

difference is that claim limitation [11c] refers to the pinched off region at a bottom portion as “another pinched off region at a bottom portion.” Ex. 1001, claim 11. In my opinion, *Cooney* anticipates or would have rendered obvious, claim limitation [11c] for reasons similar to those I discussed for claim limitations [1c-1] and [1c-2], and claim 9. *See* Sections XI.A.1.f, XI.A.1.g, and XI.A.7.

211. A combination of the annotations of *Cooney*’s Figure 6 from Sections XI.A.1.f and XI.A.7 is illustrated below to show the **pinched off region** at a top portion and **another pinched off region** at a bottom portion of *Cooney*’s TSV. A comparison of the **pinched off region** and **another pinched off region** of *Cooney*, Fig. 6 (below) with Figure 4 of the ’609 patent illustrates that the **pinched off region** and **another pinched off region** of *Cooney* are just like **pinched off region 434** and **pinched off region 438**, respectively, of Fig. 4 of the ’609 patent.

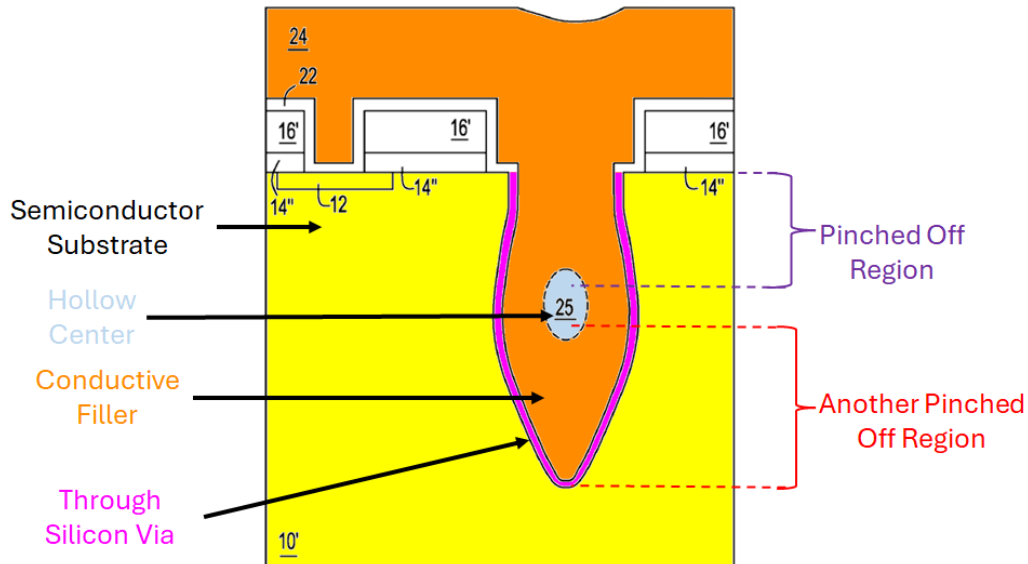


FIG. 6

Cooney, Fig. 6 (annotated).

212. Furthermore, as I discussed in Section IX.A, although Figure 6 of *Cooney* illustrates a single TSV, *Cooney*'s substrate 10 includes a plurality of similar TSVs. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. In my opinion, therefore, each of the plurality of *Cooney*'s TSVs has a pinched off region at a top of the TSV and another pinched off region at a bottom portion of the TSV.

10. **Claim 12:** “The semiconductor substrate of claim 11, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.”

213. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 11.

214. In my opinion, *Cooney* also discloses a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

215. For example, *Cooney* discloses an “etch stop layer 14 is located upon the semiconductor substrate 10” and a “capping layer 16 is located upon the etch stop layer.” *Cooney*, ¶[0026]. *Cooney* also discloses that “etch stop layer 14 will typically comprise a dielectric etch stop material[.]” *Cooney*, ¶[0034]. Because the etch stop layer 14 is made of dielectric material, in my opinion, *Cooney* discloses a dielectric layer (e.g., etch stop layer 14) disposed on the top surface of its substrate 10.

216. *Cooney* discloses the dielectric etch stop layer 14 has an aperture such as “a first region R1 that is a first comparatively wide region” that is situated directly above *Cooney*’s TSV as shown in Figure 5 of *Cooney* below.

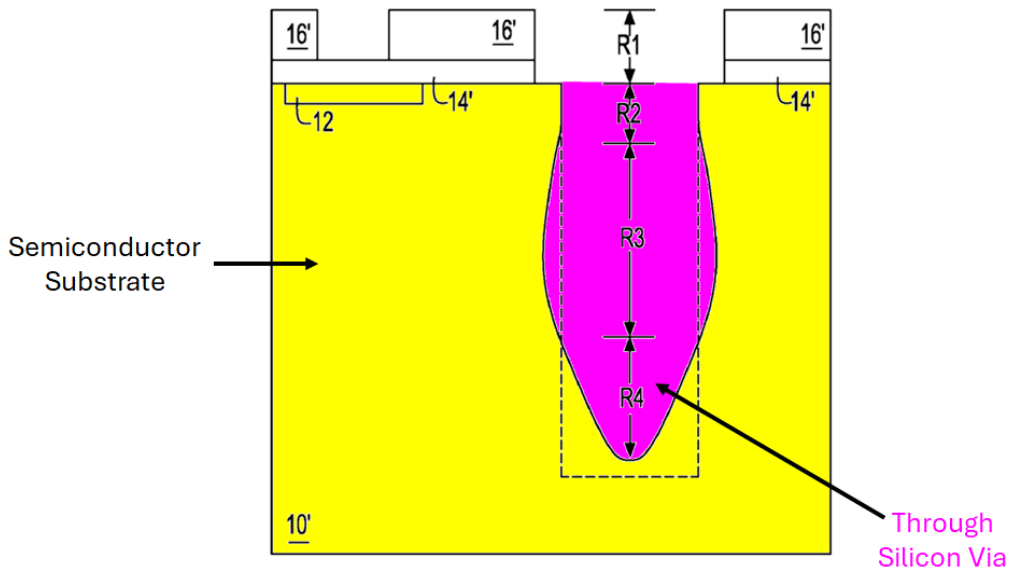


FIG. 5

Cooney, Fig. 5 (annotated).

217. As seen in the above figure, region R1 of *Cooney*'s **aperture** (or **TSV**) extends through the dielectric etch stop layer 14. As also illustrated in the above figure, the region R1 is situated directly above *Cooney*'s **TSV**.

218. *Cooney* discloses that “the linewidth of the third region R3 is preferably greater than the linewidth of the first region R1.” *Cooney*, ¶[0054]. In my opinion, therefore, *Cooney* discloses that the opening in the dielectric etch stop layer 14 in the region R1 has a width that is smaller than a width of *Cooney*'s TSV, specifically smaller than a width of region R3 of *Cooney*'s TSV.

219. Furthermore, as I discussed in Section IX.A, although Figure 5 of *Cooney* illustrates a single **TSV**, *Cooney*'s **substrate 10** includes a plurality of similar **TSVs**. *Cooney*, ¶[0066]; see also *Cooney*, Abstract, ¶¶[0018], [0020]. In

my opinion, therefore, each of the plurality of *Cooney*'s TSVs includes the aperture with regions R1, R2, R3, and R4 as described above. Thus, *Cooney* discloses a dielectric layer disposed on said top surface of said substrate and having a plurality of openings (e.g., region R1) corresponding to the plurality of TSVs. Moreover, as discussed above, each of the openings (e.g., region R1) is situated directly above one of the TSVs. Further, *Cooney* discloses that a width of the opening in region R1 is smaller than a width of the opening in region R3. In my opinion, therefore, *Cooney* includes a plurality of TSVs, each of which includes the opening in the dielectric etch stop layer 14 in the region R1 having a width that is smaller than a width of *Cooney*'s TSV. Thus, *Cooney* discloses the limitations of claim 12.

11. Claims 13, 14, and 18

- a. **Claim 13: "The semiconductor substrate of claim 11, wherein said conductive filler comprises a metallic filler."**

Claim 14: "The semiconductor substrate of claim 11, wherein said conductive filler comprises tungsten."

Claim 18: "The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center."

220. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 11.

221. In my opinion, *Cooney* also discloses the limitations of claims 13, 14, and 18.

222. Claims 13, 14, and 18 include recitations that are substantively identical to the recitations in claims 4, 5, and 10, respectively. In my opinion, *Cooney* anticipates or renders obvious claims 13, 14, and 18 for reasons similar to those I discussed for claims 4, 5, and 10, respectively. *See* Sections XI.A.4, XI.A.5, and XI.A.8.

12. Claim 17: “The semiconductor substrate of claim 11, wherein said another pinched off region is tapered at said bottom of each of said plurality of through silicon vias.”

223. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claim 11.

224. In my opinion, *Cooney* also discloses the limitations of claim 17.

225. Claim 17 includes recitations substantively identical to those of claim 2. In my opinion, *Cooney* anticipates or renders obvious claim 17 for reasons similar to those I discussed for claim 2. *See* Section XI.A.2.

B. Claims 7 and 15 Are Obvious over Cooney and Dean (Ground 2)**1. Claims 7 and 15**

- a. Claim 7: “The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.”**
Claim 15: “The semiconductor substrate of claim 11, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.”

226. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claims 1 and 11.

227. In my opinion, *Cooney* in view of *Dean* also discloses or suggests the recitations of claims 7 and 15.

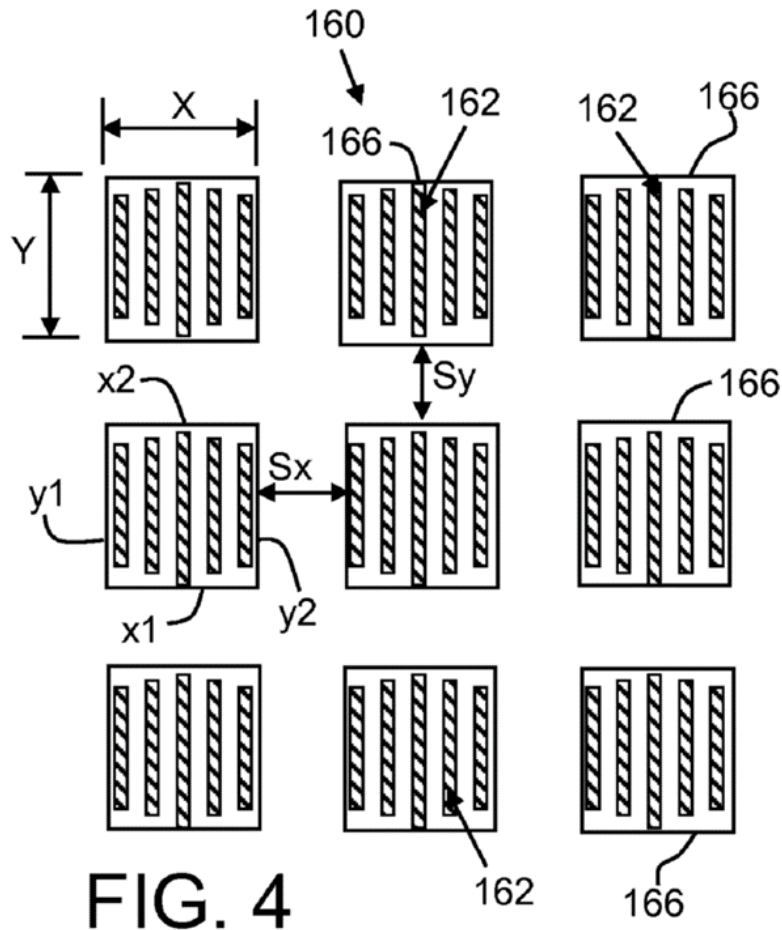
228. It would have been obvious to lay out a first group of *Cooney*’s TSV a in a width direction and a second group of *Cooney*’s TSV in a length direction, as *Dean* teaches, to reduce or eliminate wafer breakage. *Cooney* discloses that TSVs have “a comparatively narrow linewidth (i.e., in a range from about 5 to 0.1 microns).” *Cooney*, ¶¶[0007]. In describing its TSVs, *Cooney* discloses dimensions of an aperture etched in the semiconductor substrate as ranging between about 3 and 50 microns. *Cooney*, ¶[0050]. A POSITA reading *Cooney* would have understood that *Cooney*’s TSVs have a generally narrow elongated shape. Thus, when *Cooney*’s TSVs are arranged “in a single, given direction, i.e., an x-direction

or a y-direction,” there is a high chance of breakage in the wafer substrate during semiconductor processing.

229. *Dean* also discloses that “[t]hrough silicon vias (TSVs) are typically elongated vias” that may be “3 mm wide by 50 mm long.” *Dean*, ¶[0017]. Given the prevalence of elongated TSVs and given *Cooney*’s disclosures regarding the dimensions of its TSVs, a skilled artisan would have understood that *Cooney*’s vias are elongated vias.

230. *Dean* explains that “when TSVs are aligned they act like perforations making it easy to break a wafer into which they are formed.” *Dean*, ¶[0017].

Figure 4 of *Dean*, below, illustrates a set of TSVs all aligned in the vertical or Y direction.

**FIG. 4**

Dean, Fig. 4.

231. It is apparent from the figure above, that because the TSVs 162 or 166 are all aligned in the same direction (e.g., Y direction), before TSVs 162 or 166 are filled with conductive material, they would behave like perforations aligned along the Y direction. And as *Dean* discloses, the presence of a plurality of such perforations all aligned in the same direction makes it likely that the substrate would break along the length of the aligned TSVs.

232. As disclosed by *Cooney*, formation of TSVs requires etching a deep groove (e.g., extended aperture of *Cooney*) in the substrate material. *Cooney*,

¶¶[0042]-[0054]. Subsequently, the extended aperture is filled with conductor layer 24. *Cooney*, ¶¶[0055]-[0060]. Thus, prior to the filling step, *Cooney*'s substrate would likely have a plurality of extended apertures etched into *Cooney*'s substrate. A POSITA would have recognized that manufacturing semiconductor substrates with *Cooney*'s TSVs would face a similar problem related to wafer breakage, as *Dean* teaches.

233. A POSITA reading *Cooney* would have understood that *Cooney*'s TSVs are narrow elongated vias having a width ranging from 0.1 to 5 microns and a length ranging from 3 to 50 microns. For example, *Cooney* discloses that TSVs have "a comparatively narrow linewidth (i.e., in a range from about 5 to 0.1 microns)." *Cooney*, ¶[0007]. *Cooney* further discloses that the TSVs have an aperture etched in the semiconductor substrate ranging between about 3 and 50 microns. *Cooney*, ¶[0050]; *Dean*, ¶[0017] ("Through silicon vias (TSVs) are typically elongated vias" that may be "3 μm wide by 50 μm long."); Thus, given the prevalence of elongated TSVs and given *Cooney*'s disclosures regarding the dimensions of its TSVs, a POSITA would have understood that *Cooney*'s vias are elongated vias.

234. A POSITA would have recognized that if a plurality of elongated TSVs were aligned with each other on *Cooney*'s substrate, those TSVs would act like perforations, as *Dean* teaches. But even if *Cooney*'s TSVs are not elongated

TSVs, the same concern regarding wafer breakage remains. A POSITA would have understood that circular TSVs are perforations in the wafer substrates as well. As such, *Cooney*'s TSVs—when arranged “in a single, given direction, i.e., an x-direction or a y-direction,” as *Dean* explains—would potentially cause breakage of *Cooney*'s substrate during semiconductor processing. *Dean*, ¶[0031]. Thus, regardless if the TSVs are elongated or circular, a POSITA would have been motivated to use alternating elongated TSVs, as *Dean* teaches, to “reduce or eliminate wafer breakage.” *Dean*, ¶[0039].

235. A POSITA would have recognized that such an aligned arrangement of elongated TSVs in *Cooney*'s substrate would also make it easy to break *Cooney*'s substrate during manufacturing of *Cooney*'s substrate as disclosed by *Dean*. A POSITA would have, therefore, looked to *Dean*'s teachings to address the problem of substrate breakage.

236. *Dean* discloses rotating alternate TSV sets 162 to be non-aligned to the given direction. *Dean*, ¶[0033], Fig. 6. As *Dean* explains, such an arrangement of the TSVs, as shown below, “reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing.” *Dean*, ¶[0039].

237. Annotated Figure 6 of *Dean*, below, illustrates the rotation of vias 162 in this manner such that a first group of vias remains aligned in a first direction X (see X direction indicated in Fig. 4 of *Dean*, above) and another group of vias is rotated to be aligned in a second direction Y (see Y direction indicated in Fig. 4 of *Dean*, above) perpendicular to the first direction.

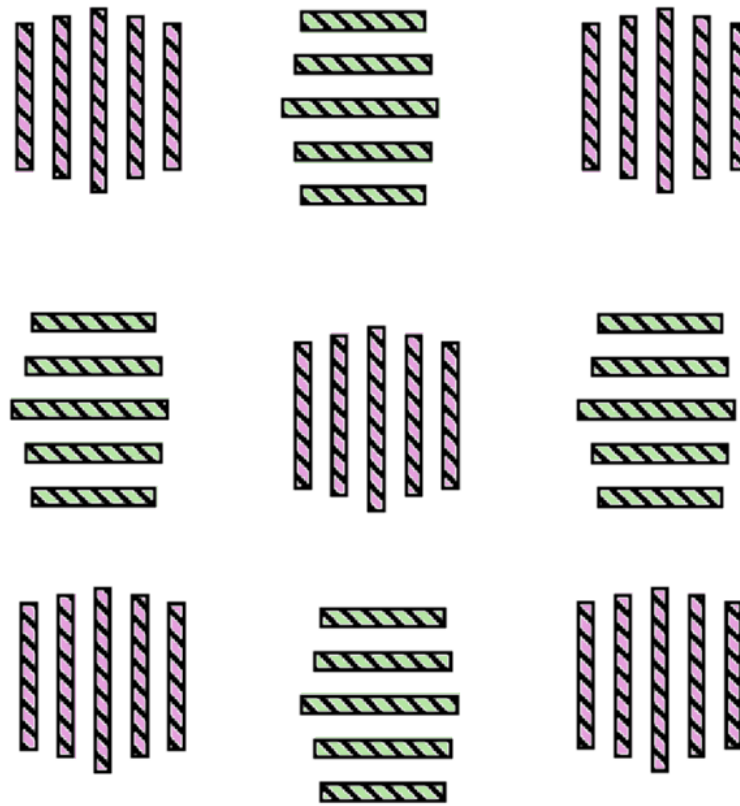


FIG. 6

Dean, Fig. 6 (annotated).

238. A skilled artisan would readily understand, for example, that if the X direction corresponds to a length direction, the Y direction, which is perpendicular to the X direction would correspond to the width direction. Thus, when one of the

X or Y directions is a length direction, the other of the X or Y directions would correspond to a width direction, or vice-versa. *Dean* discloses laying out a first group of vias in width direction and a second group of vias in the length direction to minimize the problem of substrate breakage caused by aligned vias.

239. *Cooney* and *Dean* are both directed to manufacturing semiconductor substrates with TSVs. *Cooney* discloses “a semiconductor structure [that] includes a through substrate via 24” that penetrates from a front side of a semiconductor substrate 10” to a backside of the semiconductor substrate 10.” *Cooney*, ¶[0065]. In *Cooney*, “backside planarizing” such as “mechanical polish planarizing methods and chemical mechanical polish planarizing methods” may be used to remove the backside of the substrate. *Cooney*, ¶[0063]. *Cooney* makes clear that “a multiplicity of dimensionally similar or dimensionally identical apertures and corresponding vias may also be used within a single substrate.” *Cooney*, ¶[0066].

240. As discussed above, *Dean* similarly discloses “a plurality of through silicon vias (TSVs)” in an integrated circuit (IC) layout. *Dean*, Abstract, ¶[0001]. *Dean* further explains that “at a subsequent process step, the bottom of the TSV is exposed by removing the backside of the substrate by, for example, mechanically grinding or etching,” but “when TSVs are aligned they act like perforations [within a wafer, and thus] making it easy to break a wafer into which they are formed.” *Dean*, ¶[0017], Fig. 4. To address this issue, *Dean* teaches “arranging through

silicon vias (TSVs) in an integrated circuit (IC) layout to reduce linearly aligned TSVs” in order to reduce wafer breakage. *Dean*, ¶[0002], Abstract. Accordingly, a POSITA would have appreciated that *Dean*’s technique of avoiding alignment of TSVs would be useful for arranging the plurality of TSVs on *Cooney*’s substrate to reduce wafer breakage.

241. A POSITA would have recognized that an aligned arrangement of elongated TSVs in *Cooney*’s substrate would make it easy to break *Cooney*’s substrate during manufacturing of *Cooney*’s substrate as disclosed by *Dean*. A POSITA would have, therefore, looked to *Dean*’s teachings to address the problem of substrate breakage. A POSITA would have been motivated to implement the TSV arrangement scheme, as *Dean* teaches, in *Cooney*’s substrate to ensure that the TSVs in *Cooney*’s substrate do not line up and do not create high stress points as taught by *Dean*. A POSITA would have recognized that doing so would have minimized the likelihood of breakage of *Cooney*’s substrate during semiconductor processing.

242. Fabricating semiconductor devices on a wafer is an expensive and time-consuming process. Because a broken wafer is typically discarded and because a wafer may have hundreds of dice, wafer breakage has the potential to cause significant economic loss to the semiconductor manufacturer. Furthermore, typically several semiconductor wafers are processed together in a batch through

the various manufacturing steps. As a result, debris generated due to breakage of one or more wafers during semiconductor processing can contaminate other wafers in the batch, or may even contaminate the equipment being used to manufacture the wafers. Cleaning of the undamaged wafers and/or equipment can further increase the manufacturing time and consequently increase manufacturing costs. In my opinion, therefore, a POSITA would have been motivated to reduce or eliminate the likelihood of breakage during the manufacture of *Cooney*'s substrate with TSVs to minimize substrate wastage and to minimize contamination of associated substrates and/or equipment.

243. As taught by *Dean*, it was well known in the art to orient TSVs along the width and length directions to reduce the likelihood of wafer breakage. A POSITA would have found the modification of the TSV arrangement on *Cooney* based on *Dean*'s teaching obvious because it would have involved nothing more than the use of a known technique—lengthwise and widthwise orientation of TSVs—to improve a similar device—*Cooney*'s semiconductor substrate—in the same way, namely, by reducing the likelihood of breakage of *Cooney*'s semiconductor substrate during manufacturing.

244. In my opinion, a POSITA would have had a reasonable expectation of success in implementing the teachings of *Dean* for the manufacture of the TSVs of *Cooney*. As I discussed above, both *Cooney* and *Dean* disclose semiconductor

substrates with a plurality of TSVs. Therefore, arranging the TSVs on *Cooney's* substrate using the via arrangement techniques taught by *Dean* would have been well within the skill of a POSITA. Indeed, *Dean* provides a detailed discussion of the criteria for rotation of one or more TSVs. Specifically, *Dean* discloses expanding a bounding box surrounding a via by half of the spacing between adjacent TSVs. *Dean*, ¶[0032]. When adjacently located bounding boxes touch each other, *Dean* discloses rotating one of the TSVs to be non-aligned to the direction of the immediately adjacent TSV. *Dean*, ¶[0033]. *Dean* also discloses that when the adjacently located bounding boxes do not touch or overlap each other, “no rotation is performed.” *Dean*, ¶[0033]. Thus, the TSV realignment technique disclosed by *Dean* relies on simple geometrical relationships between adjacently located TSVs. In my opinion, a POSITA would have had the requisite skill to understand the simple geometrical considerations underlying *Dean's* technique and implement it on *Cooney's* substrate.

245. In my opinion, the application of *Dean's* via layout principles on *Cooney's* substrate would also have been simple implementation of the TSV arrangement of *Cooney* with the TSV arrangement of *Dean*. A POSITA would have had a reasonable expectation of success for the combination of *Dean's* teachings with *Cooney* because it merely requires combining well-known prior

elements (e.g., simple geometrical rotations of TSVs) according to known methods.

246. Therefore, in my opinion, a POSITA would have found it obvious to combine the teachings of *Dean* with *Cooney*, and the result would be a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The combination of *Cooney* and *Dean* renders claims 7 and 15 obvious.

C. Claims 8 and 16 Are Obvious over *Cooney* and *Farooq* (Ground 3)

1. Claims 8 and 16

- a. Claim 8: “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.”**
Claim 16: “The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias has at least one chamfered corner.”

247. For the reasons discussed above, *Cooney* anticipates (Ground 1A) or would have rendered obvious (Ground 1B) claims 1 and 11.

248. In my opinion, *Cooney* in view of *Farooq* would have rendered obvious the additional recitations of claims 8 and 16.

249. It would have been obvious to modify *Cooney*’s TSVs to include flat edges with truncated corners, *as Farooq teaches*, to ensure uniform current densities along any of the edges where current may flow.

250. *Farooq* discloses the electromigration through the TSV causes a gap to form in the material, leading to higher resistance or even circuit failure. *Farooq*, 1:62-2:5, 4:10-26. As *Farooq* explains, electromigration damage occurs when current crowding in a region causes the current density to exceed a certain value. *Farooq*, 3:65-4:5. To reduced “electromigration in a circuit containing a through-silicon via (TSV),” *Farooq* provides a “novel structure for the TSV,” such as a truncated square” or “octagonal” shaped TSV structure. *Farooq*, Abstract; 4:29-34. According to *Farooq*, a “truncated square” or “octagonal” shaped TSV structure would allow the current to be “evenly distributed over the length of the edge.” *Farooq*, 4:29-34. Thus, as current enters the TSV, “relatively uniform current densities can be seen” along the flat edge of the truncated square, as shown below. *Id.*, 5:15-17, 5:40-42.

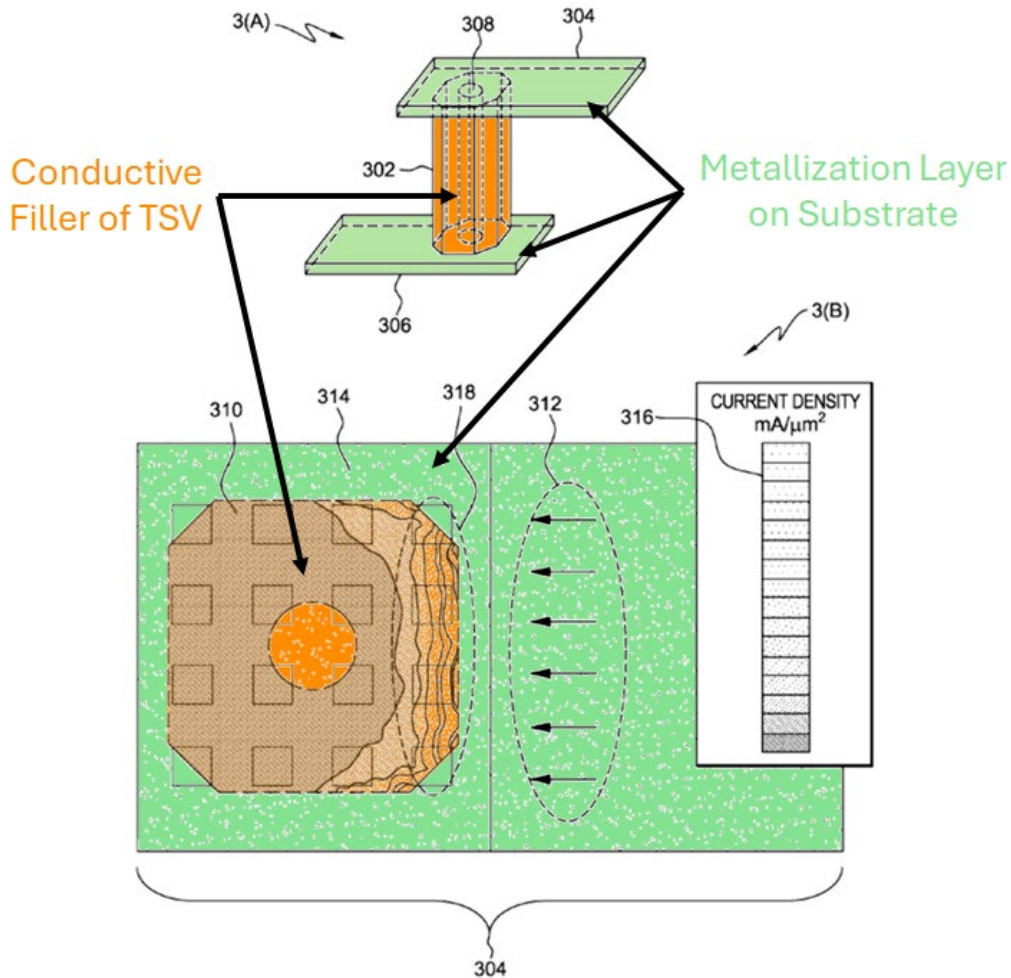


FIG. 3

Farooq, Fig. 3 (annotated).

251. In my opinion, a POSITA would have been motivated to ensure uniform current densities among any of the edges where current may flow. As I explained earlier in ground 2, a POSITA would have understood that *Cooney*'s TSVs are generally elongated TSVs. A POSITA would have been motivated to ensure that *Cooney*'s elongated vias have flat edges with truncated corners for at least two reasons. First, having a flat edge with truncated corners, as *Farooq* teaches, would ensure that "there is no leading edge ... in which current may

crowd into when flowing into or out of the TSV” and would thereby minimize current crowding while ensuring uniform current densities along the flat edge of the truncated square. *Farooq*, 6:20-25, Fig. 3. Second, truncating the corners would allow for more uniform current flow, and thus, there would have less peak current density. *See Farooq*, Fig. 3. Moreover, in my opinion, a POSITA would have also been motivated to truncate the corners to reduce the stress at the corners. As *Farooq* explains, corners introduce “local stresses” in the area, and a POSITA reading *Farooq* would have understood that truncating the corners would help to reduce the stress at the corners. *See Stiffler* (Ex. 1014), 561 (“beveling the outside corner with a 45° cut” reduces the local stress at the corners). But even if *Cooney*’s TSVs are not elongated TSVs, the same concern regarding current crowding or current density remains. For example, a POSITA would have understood that any substantially circular TSVs would cause current to crowd at the leading edge. *Farooq*, 4:17-23. Thus, in my opinion, regardless if the TSVs are elongated or circular, a POSITA would have been motivated to use flat edges with truncated corners, as *Farooq* teaches, to minimize current crowding and electromigration damage.

252. In my opinion, the modification of *Cooney*’s TSVs based on *Farooq*’s teaching would have been obvious because it would have involved nothing more than the use of a known technique of forming TSV with flat edges with truncated

corners, as *Farooq* teaches, to improve a similar device (*Cooney*'s semiconductor device in the same way, namely, by reducing the likelihood of electromigration damage of *Cooney*'s semiconductor device.

253. Furthermore, a POSITA would have had a reasonable expectation of success in implementing the teachings of *Farooq* during the manufacture of the TSVs of *Cooney* because both *Cooney* and *Farooq* disclose forming TSV through a semiconductor substrate. In my opinion, creating flat edges with truncated corners, as *Farooq* teaches, would have been well within the skill of a person of ordinary skill in the art. The application of *Farooq*'s principles on *Cooney*'s TSV would also have been a simple implementation of the TSV shape. In my opinion, a POSITA would have had a reasonable expectation of success for the combination of *Farooq* with *Cooney* because it merely requires combining well-known prior elements according to known methods.

254. Accordingly, when *Cooney*'s TSVs are fabricated to create flat edges with truncated corners, the resulting TSVs would have had chamfered corners, as *Farooq* teaches, (*Farooq*, 4:29-34, 6:4-19), and the combination of *Cooney* and *Farooq* would have rendered claims 8 and 16 obvious.

D. Claims 8 and 16 Are Obvious over *Chen* and *Cooney* (Ground 4)**1. Claims 8 and 16**

- a. **Claim 8: “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.”**
Claim 16: “The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias has at least one chamfered corner.”

255. In my opinion, *Chen* in view of *Cooney* would have rendered obvious the additional recitations of claims 8 and 16.

256. *Chen* discloses forming a plurality of TSVs directly under a UBM to reduce the total real estate taken on the surface of a semiconductor die, as shown below. *Chen*, ¶¶[0004], [0041]. Specifically, *Chen* notes that a semiconductor die can be connected to other die or devices through bumps. *Chen*, ¶[0002]. Further, *Chen* discloses that the bumps themselves are normally connected to the semiconductor die by layers or conductive material collectively known as under bump metallization (UBM). *Chen*, ¶[0002]. *Chen* recognizes that while the interconnects such as TSVs are relatively small in size, the bump and its UBM are much, much larger. *Chen*, ¶[0003]. *Chen* notes that as devices are further scaled down, this large footprint on the surface of the semiconductor die becomes even more of a liability, because multiple UBMs compete for valuable real estate with other features such as trace lines on the surface of the die. *Id.* To alleviate this problem, *Chen* discloses a system and method of forming the TSVs under the

UBM. *Chen*, ¶¶[0041]-[0042]. *Chen* explains that by placing the TSVs under the UBM, “less space on the surface of the die needs to be taken up by trace lines,” so that “die may be spaced closer together” and help to “reduce the size of circuit components in general, leading to smaller devices overall.” *Chen*, ¶[0044].

257. *Chen* discloses an exemplary embodiment in which the UBM is formed in an octagonal shape and the TSVs under the UBM are formed with chamfered corners to substantially match the UBM shape. *Chen*, ¶[0042]; Fig. 8B.

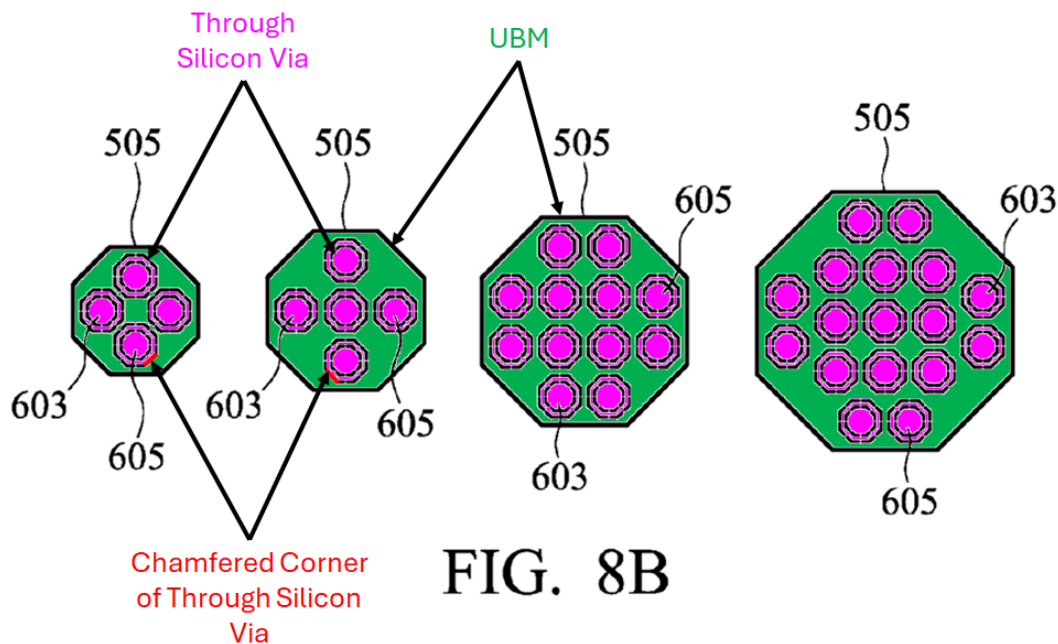


FIG. 8B

Chen, Fig. 8B (annotated).

258. I note that the use of rectangular TSVs with chamfered corners was well known in the art. For example, *Farooq* discloses using truncated squares (e.g., square shaped TSVs with chamfered corners) to minimize electromigration. *Farooq* explains: “Electromigration can take place in any conductive material

carrying a current, such as a TSV structure or a metallization layer.” *Farooq*, 1:62-64. *Farooq* discloses that “[e]lectromigration is the transport of material caused by the gradual movement of ions in a conductor” and that this “transport of material may eventually cause a gap, or a void, in the conductive material leading to higher resistance . . . or an open circuit failure.” *Farooq*, 1:64-2:2. *Farooq* explains that “[b]y providing a flat edge in the TSV structure where current enters and exits . . . , the current is evenly distributed over the length of the edge.” *Farooq*, 2:29-32. *Farooq* proposes a “preferred embodiment” that has “eight sides,” (*Farooq*, 4:40-43), which as I explained earlier would help allow for more uniform current flow and less peak current density. According to *Farooq*, such designs with chamfered edges for the TSV “mitigate electromigration concerns.” *Farooq*, 4:9. A POSITA would have understood that the use of rectangular TSVs with chamfered corners, as *Chen* teaches, was well known in the art to help minimize electromigration of the conductive material in the TSVs. *Farooq*, 1:62-2:3, 3:65-4:5, 4:29-43.

259. When *Chen*’s TSVs are fabricated using the particular sidewall profile, as *Cooney* teaches, the resulting TSVs either anticipate or alternately would have rendered obvious claims 1 and 11 in the same manner as explained above for claims 1 and 11. See Sections XI.A.1 and XI.A.9. *Chen* and *Cooney* are both directed to manufacturing semiconductor substrates with TSVs. *Chen* discloses “a system and method for manufacturing through silicon vias.” *Chen*,

¶[0001]. *Chen* discloses that when “devices are scaled down,” multiple TSVs are preferably located under the UBM with the layout of the TSVs substantially matching the UBM shape, as shown below. *Chen*, Fig. 8B.

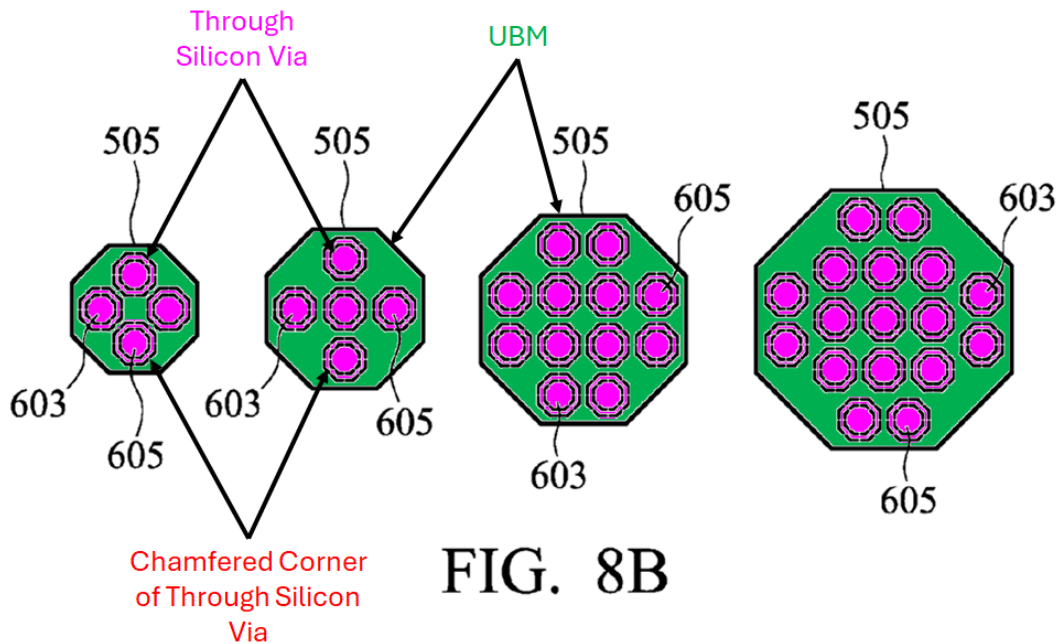


FIG. 8B

Chen, Fig. 8B (annotated).

260. *Cooney* discloses that as “microelectronic structure dimensions decrease,” the aperture’s particular sidewall profile “provides for ease in filing the via into the aperture, while providing for desirable geometric localization of any voids that form when filing the via into the aperture.” *Cooney*, ¶[0018].

261. A POSITA would have recognized the benefits of using the specific aperture and sidewall profile, as *Cooney* teaches, when the vias are arranged close together to reduce real estate in a semiconductor die, as *Chen* teaches. As *Cooney* explains, as “microelectronic structure dimensions decrease,” TSVs having

enhanced performance are needed. Cooney, ¶[0017]. A POSITA would have been motivated to use the “irregular sidewall curvature of the extended aperture,” as *Cooney* teaches, for aiding the filling of each TSV’s aperture and to localize any void within the TSV. Cooney, ¶¶[0018], [0060], [0066]. Moreover, implementing *Cooney*’s TSVs in *Chen* would have involved nothing more than the use of a known technique—using a particular sidewall profile for the TSVs—to improve a similar device—*Chen*’s TSV—in the same way, namely, to provide ease of filling the via and optimally localizing the void in the TSVs.

262. A POSITA would have had a reasonable expectation of success in implementing *Cooney*’s design, including the aperture with the particular sidewall profile, for the TSVs of *Chen*. Implementing *Chen*’s vias to take advantage of *Cooney*’s particular sidewall profile, as *Cooney* teaches, would have involved a simple geometric design that would have been well within the skill of a POSITA. Moreover, the application of *Cooney*’s vias in *Chen*’s substrate would have been a simple implementation of the TSV shape of *Cooney* in *Chen*. A POSITA would have had a reasonable expectation of success for the combination of *Cooney*’s teachings with *Chen* because it merely requires combining well-known prior art elements according to known methods.

263. Therefore, in my opinion, *Cooney* in view of *Chen* would have rendered obvious claims 8 and 16.

XII. CONCLUSION

264. For the reasons set forth in Section XI, it is my opinion that one skilled in the art would have found claims 1-18 of the '609 patent anticipated by or obvious. My opinion would remain the same even if the level of skill in the art was slightly lower (e.g., requiring only a bachelor's degree instead of a master's degree).

265. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

266. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 24, 2024

Respectfully submitted,

A handwritten signature in black ink that reads "Scott E. Thompson". The signature is written in a cursive, flowing style. Below the signature is a horizontal line.

Scott E. Thompson, Ph.D.

APPENDIX A

SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

- 1992 Ph.D. (Electrical Engineering), University of Florida
- 1988 Master of Science in Electrical Engineering, University of Florida
- 1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- ❑ Tenured Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- ❑ Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
 - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- ❑ Researcher on advanced chip technology at University of Florida totaling \$4M worth of research contracts.
 - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- ❑ Consultant (non litigation) last 5 years: Xperi Corporation
- ❑ **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- ❑ Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- ❑ Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- ❑ Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- ❑ National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

C. Legal cases

- ❑ Bold is the client
 - Godo Kaisha IP Bridge v/ **Xilinx/TSMC**
 - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017

- **KAIST IP v. Apple**
 - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
 - Case in Korea : Intellectual Property Trial and Appeal Board (“IPTAB”) regarding Korean Patent No. 10-0458288 (hereinafter, “KR ‘288 patent”).
- **Godo Kaisha IP Bridge, Inc. v. NVIDIA**
 - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1
- **Chinese Academy of Sciences v. Intel**
 - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
 - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
 - Beijing Court Testimony IME vs Lenovo 11/21/2021
 - Beijing court Testimony IME vs Intel China 1/12/2022
- **IFT v. TSMC (ITC case)**
 - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
 - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- **NXP v. Impinj**
 - 9,495,631, IPR2020-00543 - filed 2/10/2020
 - 9,633,302, IPR2020-00516 - filed 2/5/2020
 - 6,680,523, IPR2020-01630 - filed 9/17/2020
 - 7,538,444, IPR2021-00003 - filed 10/5/2020
 - Oakland District Court Case No. 4:19-cv-03161-YGR
- **Katana Silicon Technology LLC v. GlobalFoundries 2022**
 - IPR2022-01083
- **Ericsson v. Apple** Brazil Patent BRPI 9811639-8 filed 2022
- **Greenthread v. Intel** Case 6:22-cv-105-ADA filed 12/2022
- **ITC Daedalus v. TSMC** Case 337-TA-1336 filed 10/2022
- **Oasis Tooling, Inc v. GlobalFoundries** C.A. No. 22-312-CJB 3/2023
- **BiTMICRO LLC v. Intel** IPR2023-00781 filed 3/31/2023
- **Longitude Licensing LTD, v Western Digital Technologies, Inc.** IPR2023-01286 filed 8/08/2023

D. Honors and Awards

- ❑ 100 granted US patents, 60 publications and 1 book on semiconductors
- ❑ Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- ❑ Elected to Intel Fellow in 2003
- ❑ Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- ❑ 2008 SEMI award North American Recipient
- ❑ 2014 TiE 50: Top Startup (SuVolta)

- ❑ 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- ❑ 2011 EuroAsia IC Industry Award for start-up
- ❑ 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

E. Publications/Patents

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- [2] C.-H. Kuo, T. A. Weingartner, M. E. Law, S. E. Thompson, and A. Appaswamy, *Effect of Stress on Bipolar Transistor*, SRC TECHCON 2021
- [3] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent 10,250,257, 2019.
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