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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,744	03/08/2012	Hadi Jebory	0150167

CONFIRMATION NO. 9194

IMPROPER CPOA LETTER

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OC000000086049841

Date Mailed: 09/27/2016

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the power of attorney filed 09/14/2016. The power of attorney in this application is not accepted for the reason(s) listed below:

- The power of attorney is from an assignee and the statement required by 37 CFR 3.73(c) has not been received.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,744	03/08/2012	Hadi Jebory	0150167

CONFIRMATION NO. 9194

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

MISCELLANEOUS NOTICE

OC000000085967973

Date Mailed: 09/23/2016

A communication which cannot be delivered in electronic form has been mailed to the applicant.

Doc Code: N572

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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,744	03/08/2012	Hadi Jebory	0150167

CONFIRMATION NO. 9194

OC000000085967973

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Cc: BEVER HOFFMAN & HARMS, LLP
39500 STEVENSON PLACE, SUITE 209
FREMONT, CA 94539

Date: Mailed: **09/22/2016**

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed **09/14/2016** is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☑ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(c) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____, co-inventor(s) in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.
- ☐ Only one Customer Number can be designated for the Power of Attorney in an application. The Customer Number that was captured is the first Customer Number provided on the Power of Attorney document.

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- ☐ A request under 37 CFR 1.48 to add an inventor was granted in this application, however, no power of attorney consistent with the power of attorney granted by the originally named inventive entity has been received. Thus, the addition of the inventor has resulted in the loss of power of attorney in the application. See 37 CFR 1.32(e).
- ☐ The power of attorney has not been accepted because the party who is giving power of attorney has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A patent owner who was not the applicant must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).
- ☐ The power of attorney from the inventors has not been accepted because it is a copy from a prior national application for which benefit is claimed and the continuing application names an inventor who was not named as an inventor in the prior application.
- ☐ The power of attorney from the inventors has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).
- ☐ Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Any inquiries regarding this notice should be directed to the Application Assistance Unit at 571-272-4200.

AB

Application Assistance Unit
571-272-4200

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 22888

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Newport Fab, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Ronit Vardi	Date (Optional)	1/11/2016
Name	Ronit Vardi		
Title	Chief Financial Officer		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of ONE forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/47 (03-09)
Approved for use through 05/31/2015. OMB 0651-0016
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
9,147,609	13/415,744

Completed by (check one):

☐ Applicant/Inventor — /E. Eric Hoffman/ (Signature)

☑ Attorney or Agent of record 38,186 (Reg. No.) — E. Eric Hoffman (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — (925) 895-3545 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame_____ — September 14, 2016 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of _____forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	26922565
Application Number:	13415744
International Application Number:	
Confirmation Number:	9194
Title of Invention:	THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE
First Named Inventor/Applicant Name:	Hadi Jebory
Customer Number:	25700
Filer:	Edward Eric Hoffman/Carrie Reddick
Filer Authorized By:	Edward Eric Hoffman
Attorney Docket Number:	0150167
Receipt Date:	14-SEP-2016
Filing Date:	08-MAR-2012
Time Stamp:	14:05:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150167-PTO-CHG-Adrs-POA-MF-CHG-Adrs-TO-FILE.pdf	555331 709aa2d3251d350149a8099154f8f3838fe61695	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Change of Address	1	1
	Power of Attorney	2	2
	Maintenance Fee Address Change	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	555331	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/123 (04-15)
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CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
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Alexandria, VA 22313-1450

Patent Number	9,147,609
Issue Date	09/29/2015
Application Number	13/415,744
Filing Date	03/08/2012
First Named Inventor	Hadi Jebory
Attorney Docket Number	TSJ-0150167

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ **Firm *or* Individual Name**

Address

City	**State**	**ZIP**

Country

Telephone	**Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38,186.

Signature	/E. Eric Hoffman/
Typed or Printed Name	E. Eric Hoffman
Date	September 14, 2016
Telephone	(925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	09/29/2015	9147609	0150167	9194

25700 7590 09/09/2015

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 173 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Best Available Copy

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 07/09/2015
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

OPAP AKIMA-18 AUG 25 2015 PATENT & TRADEMARK OFFICE

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Azin Bakhtiari	(Depositor's name)
Azin Bakhtiari	(Signature)
8/25/15	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

TITLE OF INVENTION: THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BACHNER, ROBERT G	2898	257-621000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively.
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 FARJAMI & FARJAMI LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: **Newport Fab, LLC dba Jazz Semiconductor**

(B) RESIDENCE: (CITY and STATE OR COUNTRY): **Newport Beach, CA**

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-0731 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date August 25, 2015
Typed or printed name Michael Farjami Registration No. _____

08/26/2015 AVUONG2 00000015 13415744
01 FC:1501 960.00 OP

PAGE 6/6 * RCVD AT 8/25/2015 1:31:09 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-30



Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Jebory et al.**	Group Art Unit: 2898
Application Serial No.: **13/415,744**	Examiner: Bachner, Robert G.
Filed: **3/8/2012**	Notice of Allowance: July 9, 2015
Title: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

ISSUE FEE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Enclosed, please find the completed "Issue Fee Transmittal" form and a "Payment by Credit Card" form (PTO-2038) in the amount of $960.00 to cover the issue fee. The drawings filed in the present application have been accepted as formal drawings by the Examiner.

PAGE 3/6 * RCVD AT 8/25/2015 1:31:09 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-30

COMMENTS ON STATEMENTS OF REASONS FOR ALLOWANCE

The Applicant recognizes that in accordance with M.P.E.P. § 1302.14, the reasons for allowance provided by the Examiner do not necessarily include all of the reasons why the claims are allowed. The Applicant does not concede that the stated reasons for allowance are the only grounds for patentability of the allowed claims or that any element excluded from the Examiner's Reasons for Allowance is taught or suggested by the art of record.

Further, the Applicant does not concede that all of the elements identified by the Examiner are required to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the Examiner does not assert, and the Applicant would not agree, that the stated reasons for allowance have any bearing on the patentability of claims in any other applications.

Each dependent claim stands on its own and is allowable based on its own elements or in combination with one or more elements recited in its base claim(s). The combination of elements need not include all of the elements identified in the stated reasons for allowance.

The Commissioner is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0731.

PAGE 4/6 * RCVD AT 8/25/2015 1:31:09 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-30

An early issuance of the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 08/25/2015

By: _____
Michael Farjami
Reg. No. 38,135
Attorneys for Applicants

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

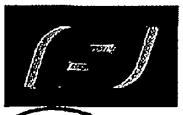
CERTIFICATE OF MAILING OR TRANSMISSION
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop Issue Fee, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, or being facsimile transmitted to the USPTO at **(571) 273-2885**, on the date indicated below.

Date: 8/25/2015

Azin Bakhtiari
Name of Person Mailing or Transmitting Paper and/or Fee

_____
Signature

PAGE 5/6 * RCVD AT 8/25/2015 1:31:09 PM [Eastern Daylight Time] * SVR:W-PTOFAX-001/12 * DNIS:2732885 * CSID:949 282 1002 * DURATION (mm-ss):01-30



FARJAMI & FARJAMI LLP

AN INTELLECTUAL PROPERTY LAW FIRM

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fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: August 25, 2015

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-2885

Re: **Application Serial No.: 13/415,744**
Filing Date: 3/8/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 6

Message:

Enclosed please find the Issue Fee.

Payment in the Amount of $960.00 is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account No. **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

25700 7590 07/09/2015

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
BACHNER, ROBERT G	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 07/09/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

TITLE OF INVENTION: THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/09/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 07/09/2015
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

TITLE OF INVENTION: THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BACHNER, ROBERT G	2898	257-621000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 07/09/2015

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MISSION VIEJO, CA 92691

EXAMINER	
BACHNER, ROBERT G	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 07/09/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/415,744	Applicant(s) JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/22/15*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-10 and 13-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ROBERT BACHNER/
Primary Examiner, Art Unit 2898

DETAILED ACTION

Response to Amendment

Applicants' amendment filed 6/22/15 has been entered and considered. The Examiner agrees that Applicants' amendment overcomes the art rejections contained in the Non-Final Office Action mailed on 2/20/15. A new search was conducted based on the amended claims, and no new art was found. Thus, this application is hereby allowed.

Allowable Subject Matter

Claims 1-10 and 13-20 are hereby allowed.

The following is the Examiner's Reasons for Allowance:

the prior art fails to disclose and would not have rendered obvious:

each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region, as recited in claim 1; and

each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region, as recited in claim 13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BACHNER whose telephone number is (571)270-3888. The examiner can normally be reached on Mon-Thurs 8:30-5 alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio J. Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROBERT BACHNER/
Primary Examiner, Art Unit 2898

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L2	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L3	689	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L4	11851	(through near silicon near via$2 TSV)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L5	0	(through near silicon near via$2 TSV) and tapper	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L6	101	(through near silicon near via$2 TSV) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L7	113	(through near silicon near via$2 TSV) and pinch$3 near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L8	2	"13744864"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L9	6	("20090098737" | "20090206416" | "20110081753" | "20120061773" | "7241700" | "7575991").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L10	8	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L11	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:49
L12	57	(through near silicon near via$2 TSV) and pinch near off and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49

L13	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L14	877	(through near silicon near via$2 TSV) and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L15	57	(through near silicon near via$2 TSV) and void and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L16	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L17	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:49
L18	24	("20060273455" | "20070085198" | "20070152194" | "20070228546" | "5424245" | "5493096" | "5501893" | "5599744" | "5679978" | "6150252" | "6333265" | "6589865" | "6821896" | "6861312" | "6908841" | "6919255").PN. OR ("7772123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:49
L19	64	(through near silicon near via$2 TSV) and (void hollow) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L20	1260	(through near silicon near via$2 TSV) and (void hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L21	151	(through near silicon near via$2 TSV) and (void hollow) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L22	16	(through near silicon near via$2 TSV) and (void hollow) same (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L23	51	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L24	114	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L25	181	newport near fab	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L26	19	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49

L27	279	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L28	6	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L29	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L30	280	(through near silicon near via$2 TSV) and (taper pinch near off narrow) and contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L37	513	("20010020739" | "20020005583" | "20020006687" | "20020020898" | "20020027293" | "20020057468" | "20020059722" | "20020060208" | "20020089025" | "20020094607" | "20020096729" | "20020113296" | "20020130390" | "20020145676" | "20020190371" | "20030014895" | "20030042564" | "20030062601" | "20030119308" | "20030148597" | "20030216023" | "20040004280" | "20040012698" | "20040018712" | "20040023447" | "20040023469" | "20040038442" | "20040041261" | "20040043607" | "20040046251" | "20040073607" | "20040082094" | "20040087441" | "20040094389" | "20040137661" | "20040137701" | "20040141536" | "20040159668" | "20040159958" | "20040178491" | "20040180539" | "20040188260" | "20040192033" | "20040198033" | "20040198040" | "20040214373" | "20040219342" | "20040219763" | "20040222082" | "20040245649" | "20040255258" | "20040262753" | "20040265562" | "20050026443" | "20050037608" | "20050046002" | "20050052751" | "20050064707" | "20050067620" | "20050069782" | "20050101054" | "20050101116" | "20050104228" | "20050106834" | "20050110095" | "20050110889" | "20050127478" | "20050136646" | "20050139390" | "20050150683" | "20050151228" | "20050164500" | "20050189637" | "20050191861" | "20050194169" | "20050208766" | "20050227382" | "20050236708" | "20050247894" | "20050254133" | "20050258530" | "20050272221" | "20050277293" | "20050282374" | "20060003566" | "20060011809" | "20060038272" | "20060040428" | "20060043569" | "20060046438" | "20060046468" | "20060046537" | "20060057776").PN. OR ("20060057836" | "20060071347" | "20060151880" | "20060154153" | "20060160367" | "20060180941" | "20060186097"	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:49

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		"20060199363"	"20060204651"					
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		"20060223301"	"20060240687"					
		"20060249849"	"20060252254"					
		"20060252262"	"20060255443"					
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		"20060278979"	"20060278980"					
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		"20070004079"	"20070012655"					
		"20070020805"	"20070020935"					
		"20070023121"	"20070032061"					
		"20070035033"	"20070037379"					
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		"20070045388"	"20070045779"					
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		"20070077753"	"20070082427"					
		"20070096263"	"20070099395"					
		"20070111386"	"20070122940"					
		"20070138562"	"20070145563"					
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		"20090283898"	"20090315154"					
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		"3345134"	"3865298"	"3902036"				
		"4040168"	"4368106"	"4534100"				
		"4581301"	"4608480"	"4614427"				
		"4627971"	"4660063"	"4756765"				
		"4768291"	"4818728"	"4906314"				
		"4907127"	"4959705"	"4964212"				
		"4984597"	"5006922"	"5024966"				
		"5026964"	"5027184"	"5037782"				
		"5098864"	"5102829"	"5123902"				
		"5130783"	"5144412"	"5145099"				
		"5158911"	"5200366"	"5219344"				
		"5233448"	"5237148"	"5289631"				
		"5291062"	"5292686"	"5294568"				
		"5304743"	"5371397"	"5378312"				
		"5378313"	"5380681"	"5402435"				

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		"6203539" | "6221769" | "6222136" |						
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L38	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L39	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L40	28	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L41	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L42	1	(US-7795134-$).did.	USPAT	OR	OFF	2015/06/29 15:49
L43	354	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49

L44	4060	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L45	1497	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L46	302	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L47	158	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L48	212	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L49	2	"8039386"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L50	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L51	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L52	0	L51 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L53	54	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:49
L54	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L55	8	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L56	89	(through near silicon near via$2 TSV contact near hole) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L57	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.				
L58	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L59	689	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L60	11851	(through near silicon near via$2 TSV)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L61	0	(through near silicon near via$2 TSV) and tapper	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L62	101	(through near silicon near via$2 TSV) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L63	113	(through near silicon near via$2 TSV) and pinch$3 near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L64	2	"13744864"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L65	6	("20090098737" | "20090206416" | "20110081753" | "20120061773" | "7241700" | "7575991").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L66	8	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L67	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L68	57	(through near silicon near via$2 TSV) and pinch near off and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L69	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L70	877	(through near silicon near via$2 TSV) and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L71	57	(through near silicon near via$2 TSV) and void and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L72	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

L73	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L74	24	("20060273455" | "20070085198" | "20070152194" | "20070228546" | "5424245" | "5493096" | "5501893" | "5599744" | "5679978" | "6150252" | "6333265" | "6589865" | "6821896" | "6861312" | "6908841" | "6919255").PN. OR ("7772123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50
L75	64	(through near silicon near via$2 TSV) and (void hollow) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L76	1260	(through near silicon near via$2 TSV) and (void hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L77	151	(through near silicon near via$2 TSV) and (void hollow) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L78	16	(through near silicon near via$2 TSV) and (void hollow) same (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L79	51	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L80	114	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L81	181	newport near fab	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L82	19	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L83	279	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L84	6	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L85	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L86	280	(through near silicon near via$2 TSV) and (taper pinch near off narrow) and contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L93	513	("20010020739" | "20020005583" | "20020006687" | "20020020898" | "20020027293" | "20020057468" | "20020059722" | "20020060208" | "20020089025" | "20020094607" |	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50

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		"20020130390"	"20020145676"					
		"20020190371"	"20030014895"					
		"20030042564"	"20030062601"					
		"20030119308"	"20030148597"					
		"20030216023"	"20040004280"					
		"20040012698"	"20040018712"					
		"20040023447"	"20040023469"					
		"20040038442"	"20040041261"					
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		"20050037608"	"20050046002"					
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		"20060199363"	"20060204651"					
		"20060208360"	"20060216862"					
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		"20060249849"	"20060252254"					
		"20060252262"	"20060255443"					
		"20060264041"	"20060270108"					
		"20060278979"	"20060278980"					
		"20060278988"	"20060278989"					
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		"20070020805"	"20070020935"					
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		"20070035033"	"20070037379"					
		"20070042598"	"20070045120"					
		"20070045388"	"20070045779"					
		"20070045806"	"20070045812"					
		"20070045826"	"20070045834"					

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L94	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L95	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L96	28	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L97	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L98	1	(US-7795134-$).did.	USPAT	OR	OFF	2015/06/29 15:50
L99	354	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L100	4060	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L101	1497	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L102	302	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L103	158	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L104	212	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L105	2	"8039386"	US-PGPUB;	OR	OFF	2015/06/29 15:50

			USPAT			
L106	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L107	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L108	0	L107 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L109	54	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L110	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L111	8	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L112	89	(through near silicon near via$2 TSV contact near hole) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L113	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L114	0	("2012/0139127").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L115	0	("2012/0139127").URPN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L116	0	("2012/0139127").URPN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L117	8	("20120013022" | "20090001502" | "20010038128" | "7959819" | "20080171432" | "20120280381" | "20100264538" | "20110291287").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

L118	128	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4 and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L119	211	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L120	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L121	4	"8569156"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L122	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L123	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L124	10	("20010048166" | "20020110645" | "6239496" | "20080230898" | "5656550" | "6239496" | "20020047200" | "20040245608" | "5864178" | "7105424" | "20040032013").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L125	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

L126	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L127	8	("20120013022" | "20090001502" | "20010038128" | "7959819" | "20080171432" | "20120280381" | "20100264538" | "20110291287").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L128	27	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$ or US-20080171432-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L129	27	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$ or US-20080171432-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L130	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L131	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L132	689	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L133	11851	(through near silicon near via$2 TSV)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L134	0	(through near silicon near via$2 TSV) and	US-	OR	OFF	2015/06/29

		tapper	PGPUB; USPAT			15:50
L135	101	(through near silicon near via$2 TSV) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L136	113	(through near silicon near via$2 TSV) and pinch$3 near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L137	2	"13744864"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L138	6	("20090098737" | "20090206416" | "20110081753" | "20120061773" | "7241700" | "7575991").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L139	8	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L140	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L141	57	(through near silicon near via$2 TSV) and pinch near off and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L142	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L143	877	(through near silicon near via$2 TSV) and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L144	57	(through near silicon near via$2 TSV) and void and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L145	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L146	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L147	24	("20060273455" | "20070085198" | "20070152194" | "20070228546" | "5424245" | "5493096" | "5501893" | "5599744" | "5679978" | "6150252" | "6333265" | "6589865" | "6821896" | "6861312" | "6908841" | "6919255").PN. OR ("7772123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50
L148	64	(through near silicon near via$2 TSV) and (void hollow) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L149	1260	(through near silicon near via$2 TSV) and (void hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L150	151	(through near silicon near via$2 TSV) and	US-	OR	OFF	2015/06/29

		(void hollow) and (taper pinch near off)	PGPUB; USPAT			15:50
L151	16	(through near silicon near via$2 TSV) and (void hollow) same (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L152	51	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L153	114	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L154	181	newport near fab	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L155	19	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L156	279	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L157	6	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L158	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L159	280	(through near silicon near via$2 TSV) and (taper pinch near off narrow) and contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L166	513	("20010020739" | "20020005583" | "20020006687" | "20020020898" | "20020027293" | "20020057468" | "20020059722" | "20020060208" | "20020089025" | "20020094607" | "20020096729" | "20020113296" | "20020130390" | "20020145676" | "20020190371" | "20030014895" | "20030042564" | "20030062601" | "20030119308" | "20030148597" | "20030216023" | "20040004280" | "20040012698" | "20040018712" | "20040023447" | "20040023469" | "20040038442" | "20040041261" | "20040043607" | "20040046251" | "20040073607" | "20040082094" | "20040087441" | "20040094389" | "20040137661" | "20040137701" | "20040141536" | "20040159668" | "20040159958" | "20040178491" | "20040180539" | "20040188260" | "20040192033" | "20040198033" |	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50

		"20040198040"	"20040214373"				
		"20040219342"	"20040219763"				
		"20040222082"	"20040245649"				
		"20040255258"	"20040262753"				
		"20040265562"	"20050026443"				
		"20050037608"	"20050046002"				
		"20050052751"	"20050064707"				
		"20050067620"	"20050069782"				
		"20050101054"	"20050101116"				
		"20050104228"	"20050106834"				
		"20050110095"	"20050110889"				
		"20050127478"	"20050136646"				
		"20050139390"	"20050150683"				
		"20050151228"	"20050164500"				
		"20050189637"	"20050191861"				
		"20050194169"	"20050208766"				
		"20050227382"	"20050236708"				
		"20050247894"	"20050254133"				
		"20050258530"	"20050272221"				
		"20050277293"	"20050282374"				
		"20060003566"	"20060011809"				
		"20060038272"	"20060040428"				
		"20060043569"	"20060046438"				
		"20060046468"	"20060046537"				
		"20060057776").PN. OR ("20060057836"					
		"20060071347"	"20060151880"				
		"20060154153"	"20060160367"				
		"20060180941"	"20060186097"				
		"20060191882"	"20060195729"				
		"20060199363"	"20060204651"				
		"20060208360"	"20060216862"				
		"20060223301"	"20060240687"				
		"20060249849"	"20060252254"				
		"20060252262"	"20060255443"				
		"20060264041"	"20060270108"				
		"20060278979"	"20060278980"				
		"20060278988"	"20060278989"				
		"20060281224"	"20060281243"				
		"20060289967"	"20060292877"				
		"20070004079"	"20070012655"				
		"20070020805"	"20070020935"				
		"20070023121"	"20070032061"				
		"20070035033"	"20070037379"				
		"20070042598"	"20070045120"				
		"20070045388"	"20070045779"				
		"20070045806"	"20070045812"				
		"20070045826"	"20070045834"				
		"20070048896"	"20070048994"				
		"20070049019"	"20070057028"				
		"20070077753"	"20070082427"				
		"20070096263"	"20070099395"				
		"20070111386"	"20070122940"				
		"20070138562"	"20070145563"				
		"20070152342"	"20070155997"				
		"20070158839"	"20070158853"				
		"20070161235"	"20070166991"				
		"20070166997"	"20070167004"				
		"20070170574"	"20070178694"				
		"20070182020"	"20070190803"				
		"20070197013"	"20070202617"				
		"20070222050"	"20070222054"				
		"20070228576"	"20070228926"				
		"20070262424"	"20070267138"				
		"20070281473"	"20070293040"				

		"20080006850" | "20080050904" | "20080050911" | "20080054444" | "20080057620" | "20080079120" | "20080079121" | "20080081386" | "20080081398" | "20080265933" | "20080299759" | "20080299762" | "20080318361" | "20090007934").PN. OR ("20090014859" | "20090057912" | "20090091962" | "20090127668" | "20090146312" | "20090166846" | "20090180257" | "20090224405" | "20090283898" | "20090315154" | "20090321947" | "2821959" | "3006318" | "3345134" | "3865298" | "3902036" | "4040168" | "4368106" | "4534100" | "4581301" | "4608480" | "4614427" | "4627971" | "4660063" | "4756765" | "4768291" | "4818728" | "4906314" | "4907127" | "4959705" | "4964212" | "4984597" | "5006922" | "5024966" | "5026964" | "5027184" | "5037782" | "5098864" | "5102829" | "5123902" | "5130783" | "5144412" | "5145099" | "5158911" | "5200366" | "5219344" | "5233448" | "5237148" | "5289631" | "5291062" | "5292686" | "5294568" | "5304743" | "5371397" | "5378312" | "5378313" | "5380681" | "5402435" | "5406630" | "5424573" | "5435887" | "5438212" | "5447871" | "5464960" | "5481483" | "5485039" | "5496755" | "5505804" | "5515167" | "5518956" | "5550403" | "5585308" | "5585675" | "5593913" | "5605783" | "5614743" | "5618752" | "5624437" | "5627106" | "5646067" | "5654221" | "5672519" | "5673846" | "5684642" | "5690841" | "5694246" | "5708293" | "5718791" | "5723904" | "5726493" | "5734555" | "5771158" | "5776824" | "5807439" | "5811799" | "5821532" | "5825080" | "5826628" | "5847454" | "5851845" | "5857963" | "5861654" | "5870289" | "5870823" | "5877040" | "5893828" | "5897338" | "5904499" | "5914488" | "5969422" | "5977535" | "5998240" | "5998292" | "5998862" | "6004867" | "6008070" | "6008914" | "6080291" | "6097087" | "6103547" | "6104086").PN. OR ("6107186" | "6107679" | "6110825" | "6114240" | "6119335" | "6124634" | "6133622" | "6137163" | "6137182" | "6140604" | "6143588" | "6148509" | "6159764" | "6180518" | "6184060" | "6184465" | "6187615" | "6191487" | "6203539" | "6221769" | "6222136" | "6222270" | "6228687" | "6229202" | "6235552" | "6236046" | "6246108" | "6252300" | "6259083" | "6266197" | "6271580" | "6274927" | "6277757" | "6285064" | "6291894" | "6294837" | "6297155" | "6324253" | "6326689" | "6326697" | "6329632" | "6341009" | "6344976" | "6351027" | "6359254" |				

		"6359328" | "6372548" | "6388208" | "6391770" | "6406636" | "6407381" | "6411439" | "6432821" | "6433303" | "6433304" | "6437284" | "6437441" | "6444576" | "6448106" | "6455425" | "6457515" | "6459039" | "6459150" | "6468889" | "6483652" | "6486083" | "6486549" | "6503780" | "6521516" | "6521530" | "6534192" | "6541762" | "6545563" | "6555782" | "6560047" | "6566745" | "6569711" | "6569777" | "6572606" | "6576531" | "6580174" | "6582987" | "6582992" | "6593644" | "6599436" | "6603183" | "6606251" | "6617623" | "6620031" | "6620731" | "6621045" | "6638410" | "6653236" | "6658818" | "6660622" | "6660630" | "6661047" | "6664129" | "6664485" | "6667551" | "6670986" | "6680459" | "6686588" | "6699787" | "6703310" | "6708405" | "6734419" | "6746971" | "6750144" | "6756564" | "6759266" | "6774486" | "6777244" | "6778046" | "6780749" | "6790775" | "6791076" | "6795120" | "6797616" | "6800943" | "6809025" | "6809421" | "6813154" | "6818464" | "6825127").PN. OR ("6825458" | "6825557" | "6828175" | "6828223" | "6828663" | "6828674" | "6838377" | "6841849" | "6844978" | "6847109" | "6852621" | "6856023" | "6858891" | "6864172" | "6864457" | "6867390" | "6873054" | "6882021" | "6882030" | "6885107" | "6903012" | "6903442" | "6903443" | "6910268" | "6913952" | "6916725" | "6934065" | "6936536" | "6939343" | "6943056" | "6946325" | "6951627" | "6953748" | "6962867" | "6970775" | "6982487" | "7022609" | "7023090" | "7029937" | "7033927" | "7037836" | "7041598" | "7045015" | "7084073" | "7091124" | "7092284" | "7094677" | "7109068" | "7111149" | "7129112" | "7151009" | "7164565" | "7166247" | "7170183" | "7183176" | "7183653" | "7186650" | "7190061" | "7199050" | "7214615" | "7217596" | "7217888" | "7223634" | "7256073" | "7262134" | "7262495" | "7265052" | "7271482" | "7279776" | "7300857" | "7317256" | "7378726" | "7408265" | "7449098" | "7491582" | "7498661").PN. OR ("7795134").URPN.				
L167	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.				
L168	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L169	28	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L170	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L171	1	(US-7795134-$).did.	USPAT	OR	OFF	2015/06/29 15:50
L172	354	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L173	4060	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L174	1497	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L175	302	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L176	158	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L177	212	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L178	2	"8039386"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L179	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L180	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.				
L181	0	L180 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L182	54	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L183	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L184	8	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L185	89	(through near silicon near via$2 TSV contact near hole) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L186	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L187	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L188	689	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L189	11851	(through near silicon near via$2 TSV)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L190	0	(through near silicon near via$2 TSV) and tapper	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L191	101	(through near silicon near via$2 TSV) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L192	113	(through near silicon near via$2 TSV) and pinch$3 near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L193	2	"13744864"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L194	6	("20090098737" | "20090206416" | "20110081753" | "20120061773" | "7241700" | "7575991").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L195	8	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-	US-PGPUB;	OR	OFF	2015/06/29 15:50

		20110151659-$ or US-20100230818-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$).did.	USPAT			
L196	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L197	57	(through near silicon near via$2 TSV) and pinch near off and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L198	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L199	877	(through near silicon near via$2 TSV) and void	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L200	57	(through near silicon near via$2 TSV) and void and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L201	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L202	13	("2010/0230818").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L203	24	("20060273455" | "20070085198" | "20070152194" | "20070228546" | "5424245" | "5493096" | "5501893" | "5599744" | "5679978" | "6150252" | "6333265" | "6589865" | "6821896" | "6861312" | "6908841" | "6919255").PN. OR ("7772123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50
L204	64	(through near silicon near via$2 TSV) and (void hollow) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L205	1260	(through near silicon near via$2 TSV) and (void hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L206	151	(through near silicon near via$2 TSV) and (void hollow) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L207	16	(through near silicon near via$2 TSV) and (void hollow) same (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L208	51	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L209	114	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L210	181	newport near fab	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L211	19	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-	US-PGPUB;	OR	OFF	2015/06/29 15:50

		20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$).did.	USPAT			
L212	279	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L213	6	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L214	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L215	280	(through near silicon near via$2 TSV) and (taper pinch near off narrow) and contaminat$	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L222	513	("20010020739" | "20020005583" | "20020006687" | "20020020898" | "20020027293" | "20020057468" | "20020059722" | "20020060208" | "20020089025" | "20020094607" | "20020096729" | "20020113296" | "20020130390" | "20020145676" | "20020190371" | "20030014895" | "20030042564" | "20030062601" | "20030119308" | "20030148597" | "20030216023" | "20040004280" | "20040012698" | "20040018712" | "20040023447" | "20040023469" | "20040038442" | "20040041261" | "20040043607" | "20040046251" | "20040073607" | "20040082094" | "20040087441" | "20040094389" | "20040137661" | "20040137701" | "20040141536" | "20040159668" | "20040159958" | "20040178491" | "20040180539" | "20040188260" | "20040192033" | "20040198033" | "20040198040" | "20040214373" | "20040219342" | "20040219763" | "20040222082" | "20040245649" | "20040255258" | "20040262753" | "20040265562" | "20050026443" | "20050037608" | "20050046002" | "20050052751" | "20050064707" | "20050067620" | "20050069782" | "20050101054" | "20050101116" | "20050104228" | "20050106834" | "20050110095" | "20050110889" | "20050127478" | "20050136646" | "20050139390" | "20050150683" | "20050151228" | "20050164500" | "20050189637" | "20050191861" | "20050194169" | "20050208766" | "20050227382" | "20050236708" | "20050247894" | "20050254133" |	US-PGPUB; USPAT; USOCR	OR	OFF	2015/06/29 15:50

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		"20060003566"	"20060011809"						
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		"20060208360"	"20060216862"						
		"20060223301"	"20060240687"						
		"20060249849"	"20060252254"						
		"20060252262"	"20060255443"						
		"20060264041"	"20060270108"						
		"20060278979"	"20060278980"						
		"20060278988"	"20060278989"						
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		"20060289967"	"20060292877"						
		"20070004079"	"20070012655"						
		"20070020805"	"20070020935"						
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		"20070197013"	"20070202617"						
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		"4581301"	"4608480"	"4614427"					
		"4627971"	"4660063"	"4756765"					
		"4768291"	"4818728"	"4906314"					

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L223	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L224	7	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L225	28	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L226	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.				
L227	1	(US-7795134-$).did.	USPAT	OR	OFF	2015/06/29 15:50
L228	354	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L229	4060	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L230	1497	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L231	302	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L232	158	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L233	212	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L234	2	"8039386"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L235	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L236	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L237	0	L236 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L238	54	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L239	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L240	8	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L241	89	(through near silicon near via$2 TSV contact near hole) and (round$3	US-PGPUB;	OR	OFF	2015/06/29 15:50

		chamfer$2) with corner same stress	USPAT			
L242	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L243	0	("2012/0139127").URPN.	USPAT	OR	OFF	2015/06/29 15:50
L244	0	("2012/0139127").URPN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L245	0	("2012/0139127").URPN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L246	8	("20120013022" | "20090001502" | "20010038128" | "7959819" | "20080171432" | "20120280381" | "20100264538" | "20110291287").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L247	128	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4 and polish$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L248	211	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L249	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L250	4	"8569156"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L251	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L252	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.				
L253	10	("20010048166" | "20020110645" | "6239496" | "20080230898" | "5656550" | "6239496" | "20020047200" | "20040245608" | "5864178" | "7105424" | "20040032013").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L254	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L255	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L256	8	("20120013022" | "20090001502" | "20010038128" | "7959819" | "20080171432" | "20120280381" | "20100264538" | "20110291287").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L257	27	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$ or US-20080171432-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L258	27	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$ or US-20080171432-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

		8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.				
L259	0	"14251296"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L260	719	(through near silicon near via$2 tsv) and (air near gap airgap hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L261	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L262	64	(through near silicon near via$2 tsv) and (air near gap airgap hollow) and expand	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L263	110838	(air near gap airgap hollow) and expand	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L264	9250	(air near gap airgap hollow) and expand and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L265	849	(air near gap airgap hollow) same expand and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L266	7	("5686171" | "20040129451" | "6214703" | "20100090304" | "20070111390" | "20100120227" | "20070222037").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L267	689	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L268	135	L267 and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L269	0	(air near gap airgap hollow) same expand and semiconductor and pinchoff	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L270	10	(air near gap airgap hollow) same expand and semiconductor and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L271	95	(air near gap airgap hollow) same expand and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L272	230	(air near gap airgap hollow) same expand and thermal near stress	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L273	74174	((257/774 OR 257/416 OR 257/737 OR 257/432 OR 257/531 OR 257/E21.502 OR 257/E23.021 OR 257/330 OR 257/415 OR 257/417 OR 257/434 OR 257/443 OR 257/446 OR 257/48 OR 257/532 OR 257/621 OR 257/678 OR 257/684 OR 257/741 OR 257/762 OR 257/773 OR 257/783 OR 257/94 OR 257/98 OR 257/99).CCLS.)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L274	6	L273 and (hollow air near gap) same (conductive near fill)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

L275	1991	L273 and (hollow air near gap) same (conductive fill metal)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L276	0	L273 and (hollow air near gap) same (conductive near fill) and pinch near oof	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L277	4	L273 and (hollow air near gap) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L278	6	(hollow air near gap) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L279	8	(hollow air) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L280	334	(hollow air) same (conductive) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L281	73	(hollow air) same (conductive) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L282	114	(hollow air) same (conductive metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L283	73	(hollow air) same (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L284	38	(hollow air) with (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L285	73	(hollow air) same (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L286	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L287	1809	(through near silicon near via tsv) and (air hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L288	729	(through near silicon near via tsv) and (air hollow) and (thermal near stress expan$4)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
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		Y10T29/4935 OR G02B6/4416).CPC.)				
L290	133291	((257/774 OR 257/415 OR 257/43 OR 257/531 OR 257/777 OR 257/E21.211 OR 257/E21.506 OR 257/E23.145 OR 257/209 OR 257/369 OR 257/421 OR 257/432 OR 257/437 OR 257/48 OR 257/499 OR 257/618 OR 257/675 OR 257/690 OR 257/692 OR 257/737 OR 257/762 OR 257/773 OR 257/783 OR 257/84 OR 257/88 OR 257/98 OR 257/99 OR 333/239 OR 333/21R OR 333/254 OR 333/1 OR 333/248 OR 333/256 OR 333/26 OR 333/260 OR 438/109 OR 438/667 OR 438/104 OR 438/107 OR 438/126 OR 438/455 OR 438/51 OR 438/613 OR 438/106 OR 438/108 OR 438/113 OR 438/118 OR 438/119 OR 438/121 OR 438/125 OR 438/17 OR 438/25 OR 438/26 OR 438/3 OR 438/424 OR 438/458 OR 438/459 OR 438/618 OR 438/637 OR 438/64 OR 438/660 OR 438/780).CCLS.)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
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L292	34104	L291 and (hollow air) same (conductive metal)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L293	6852	L291 and (hollow air) same (conductive metal) same (thermal stress)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
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L295	1	"13370400"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L296	313	Adamovich	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L297	6	("20090053488" | "7161294" | "7161294" | "20050168137" | "20070037010" | "20100244002" | "20040100190").PN.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L298	31	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$ or US-20080171432-$ or US-20140374916-$ or US-20130256843-$ or US-20130161826-$ or US-20050121768-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

L299	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
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L302	4439	L301 and (tsv via$3) and substrate and silicon and (air near gap hollow)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L303	143	L301 and (tsv via$3) and substrate and silicon and (air near gap hollow) and pinch$3	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L304	28	L301 and (tsv via$3) and substrate and silicon and (air near gap hollow) and pinch$3 and taper$3	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L305	857	L301 and (tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3)	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L306	2	"13183315"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L307	3	"20120013022"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50
L308	2	"8647920"	US-PGPUB; USPAT	OR	OFF	2015/06/29 15:50

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L309	1671	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50

L310	1618	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3) and (fill$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L311	75	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3) and conductive near (fill$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L312	1671	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L313	1501	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3) and thermal.clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L314	323	(tsv via$3) and substrate and silicon and (air near gap hollow) and (pinch$3 taper$3) and stress.clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L315	135	(tsv via$3) and substrate and silicon and air near gap and (hollow) and (pinch$3 taper$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L316	822	(tsv via$3) and substrate and silicon and air and (hollow) and (pinch$3 taper$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50
L317	1072	(tsv via$3) and substrate and silicon and air and (empty hollow) and (pinch$3 taper$3).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2015/06/29 15:50

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C:\Users\rbachner\Documents\EAST\Workspaces\13415744.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	**Art Unit**
	ROBERT BACHNER	2898

CPC						
Symbol					**Type**	**Version**
H01L		21	/	76898	F	2013-01-01
H01L		23	/	481	I	2013-01-01
H01L		2924	/	0002	A	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
H01L		2924	/	0002	A	1	1	2013-01-01
H01L		2924	/	00	A	1	2	2013-01-01

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/ROBERT BACHNER/ Primary Examiner.Art Unit 2898	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	**Art Unit**
	ROBERT BACHNER	2898

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	621	H	0	1	L	29 / 40 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
438	667				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/ROBERT BACHNER/ Primary Examiner.Art Unit 2898	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	**Art Unit**
	ROBERT BACHNER	2898

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
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14	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/ROBERT BACHNER/ Primary Examiner.Art Unit 2898	06/29/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	**Art Unit**
	ROBERT BACHNER	2898

CPC- SEARCHED		
Symbol	**Date**	**Examiner**
((H01L2924/00 OR H01L2224/73204 OR H01L2924/014 OR H01L2224/16225 OR H01L2924/0002 OR H01L2224/32225 OR H01L2924/1461 OR H01L2224/48091 OR H01L2924/00012 OR H01L2224/245 OR H01L2924/00015 OR H01L2924/	6/29/2015	/RGB/

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
	((257/774 OR 257/415 OR 257/43 OR 257/531 OR 257/777 OR 257/E21.211 OR 257/E21.506 OR 257/E23.145 OR 257/209 OR 257/369 OR 257/421 OR 257/432 OR 257/437 OR 257/48 OR 257/499 OR 257/618 OR 257/675 OR 257/690 OR 257/692 OR 257/737 OR 257/762 OR 257/773 OR 257/783 OR 257/84 OR 257/88 OR 257/98 OR 257/99 OR 333/239 OR 333/21R OR 333/254 OR 333/1 OR 333/248 OR 333/256 OR 333/26 OR 333/260 OR 438/109 OR 438/667 OR 438/104 OR 438/107 OR 438/126 OR 438/455 OR 438/51 OR 438/613 OR 438/106 OR 438/108 OR 4	6/29/2015	/RGB/

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Searched as detailed in the attached EAST SEARCH REPORT.	4/2/2014	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	8/15/2014	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	2/10/2015	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	6/29/2015	/RGB/

	/ROBERT BACHNER/ Primary Examiner.Art Unit 2898

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
	Searched as detailed in the attached EAST SEARCH REPORT.	6/29/2015	/RGB/

	/ROBERT BACHNER/ Primary Examiner.Art Unit 2898

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JUN 22 2015

Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**	Art Unit: 2898
Serial No.: 13/415,744	Examiner: Bachner, Robert G.
Filing Date: 03/08/2012	
For: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

AMENDMENT AND RESPONSE TO *NON-FINAL* OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Non-Final* Office Action dated February 20, 2015 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

06/23/2015 JVONG1 00000004 13415744
01 FC:1251 200.00 OP

PAGE 3/17 * RCVD AT 6/22/2015 7:55:18 PM [Eastern Daylight Time] * SVR:W-PTOFAX-003/20 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):03-06

In the Claims:

Claim 1 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region.

Claim 2 (original): The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

Claim 3 (original): The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

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Claim 4 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

Claim 5 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

Claim 6 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

Claim 7 (original): The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 8 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 9 (original): The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

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Claim 10 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Claims 11-12 (canceled)

Claim 13 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.

Claim 14 (original): The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric

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layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

Claim 15 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

Claim 16 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

Claim 17 (original): The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 18 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 19 (currently amended): The semiconductor substrate of claim 13, ~~further comprising a~~ wherein said another pinched off region is tapered at [[a]] said bottom of each of said plurality of through silicon vias.

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Claim 20 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

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REMARKS

Prior to the present amendment and response, claims 1-10 and 13-20 were pending in the present application. By the present amendment and response, Applicants have amended claims 1, 13 and 19. Thus, after the present amendment and response, claims 1-10 and 13-20 remain pending in the present application. Applicants respectfully request reconsideration and allowance of claims 1-10 and 13-20 in view of the above amendments and the following remarks.

A. Rejection of Claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a)

In the *Non-Final* Office Action, dated February 20, 2015 (hereinafter "Office Action"), the Examiner rejects claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over alleged Applicants' Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent Application Publication Number 2012/0139127 A1 by Eric Beyne (hereinafter "Beyne"), and further in view of U.S. Patent Application Publication Number 2005/0121768 A1 by Edelstein et al. (hereinafter "Edelstein"). *See* page 2 of the Office Action. For the reasons discussed below, Applicants respectfully submit that amended independent claim 13 is patentably distinguishable over the alleged AAPA, Beyne and Edelstein, either singly or in any combination thereof.

As disclosed in the present application, in one implementation, flowchart 500 in Figure 5 presents an exemplary method of fabricating a through silicon via having a

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pinched off region such as, for example, TSV 402 in Figure 4 of the present application. *See*, e.g., page 10, lines 4-6 of the present application. For example, "action 510 of flowchart 500 includes performing a first etch into substrate 412 to first depth d_3 to form sidewalls 440 of through silicon via 402." *Id.*, e.g., at lines 7-8 with Figures 4 and 5. Thereafter, "action 520 includes performing a second etch in through silicon via 402 to second depth d_4 such that through silicon via 402 tapers from first depth d_3 to second depth d_4." *Id.*, e.g., at lines 10-12. Action 530 of flowchart 500 "includes depositing conductive filler 430 on sidewalls 440 of through silicon via 402 such that hollow center portion 432 and pinched off region 438 are formed in through silicon via 402." *See*, e.g., *id.* at page 11, lines 6-8. As illustrated in Figure 4, hollow center portion 432 extends below first depth d_3 into second depth d_4 in pinched off region 438, and is tapered off in pinched off region 438.

By the present amendment and response, Applicants have amended independent claim 13 to recite, in part,

> wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region. *See* claim 13 above.

Support for amended independent claim 13 can be found at least page 11, lines 6-21 and Figure 4 of the present application. Applicants have also amended claim 19 to harmonize its recitation with changes introduced to independent claim 13, from which it depends. *See* claim 19 above.

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In the Office Action, the Examiner asserts that the alleged AAPA discloses various features of independent claim 13 of the present application. *See* pages 2-3 of the Office Action. The Examiner concedes:

> AAPA does not disclose:
>
> each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward; to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate. *Id.*

In an attempt to cure the acknowledged deficiencies of the alleged AAPA, the Examiner suggests combining the alleged AAPA with Edelstein and Beyne. *Id.* Specifically, the Examiner asserts:

> In related art, Edelstein discloses Fig. 2b and 6d-f:
> Said hollow center (220) being entirely surrounded by said conductive filler (225) to provide space fro said conductive filler to expand inward, (See [0041]). Edelstein discloses that providing the hollow portion 220 provides the benefit of reducing thermal stresses on the substrate. See [0041]. Thus, it would have been obvious to one having ordinary skill in the art o provide the hollows as taut by Edelstein for the thermal benefits that by Edelstein. *Id.*

Turning to Edelstein, Figure 2B of Edelstein depicts a through-via having "an annular ring of insulating material 223 within which is disposed a conductive via of metal (e.g., copper) 225 having a void 220 at its core." *See* page 4, paragraph [0041] with Figure 2B of Edelstein. However, Applicants respectfully submit that Edelstein does not disclose or suggest, for example, "wherein each of said plurality of through silicon vias has [...] another pinched off region at a bottom portion," and "wherein said hollow center

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is tapered in said another pinched off region," as recited in amended independent claim 13 of the present application.

Turning to Beyne, Beyne describes a specific method of "forming airgaps in isolating structures whereby **the structures are situated *around* a TSV interconnect structure** in order to reduce the mechanical stress, the electric field and capacitance effects in the surrounding areas of the large TSV interconnect structure." *See* page 1, paragraph [0015] of Beyne (emphases added by Applicants).

With reference to Figures 2A and 2B, Beyne provides:

> Turning now to FIG. 2A and FIG. 2B illustrating side views of a particular example of an embodiment, wherein the semiconductor substrate S has a 3D-TSV 10. **The semiconductor substrate S comprises a 3D-TSV 10** in the present example having a depth in the substrate S of around 50 μm and a diameter (width) around 2 μm and **further comprises isolating trench-like structures 3 having at least one airgap 4.** The trench-like structure 3 thus is a hollow trench-like structure comprising at least one airgap 4. A liner 2*a* may be deposited onto the substrate S and on the inner sidewalls 2*b* of TSV. In the present example, the liner 2*b* has a thickness of around 200 nm on the inner sidewalls of said TSV, although embodiments are not limited thereto. The liner further may pinch of the isolating trench-like structures 3 thereby creating an airgap 4 in the trench-like structures. FIG. 2A illustrates a side view and FIG. 2B illustrates a more detailed side view combined with a top view. *See id.* at page 4, paragraph [0064] with Figures 2A and 2B (emphases added by Applicants).

With reference to Figures 10A-10H, Beyne depicts various steps of fabricating "a Through Silicon Via (TSV) interconnect based on **the via middle approach whereby said TSV interconnects are surrounded by isolating trenches with airgaps.**" *See id.*

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at page 6, paragraph [0079] (emphasis added by Applicants). As illustrated in Figure 10A, TSV hole 1 and isolating trench 3 are formed in substrate S. *Id.* with Figure 10A.

With reference to Figure 10B, Beyne further states:

> FIG. 10B illustrates a detailed view of the substrate S with a patterned photoresist 12, PMD and STI layer(s) 11 and a liner 2*a* deposited in the TSV hole and isolating trenches. The liner is deposited on the horizontal parts of the substrate 2*a* and onto the sidewalls of the TSV hole 2*b* and within the isolating trenches 2*c* FIG. 10B clearly illustrates the closure of the opening (top) of the isolating trenches 3 thereby pinching-off the trench and forming an airgap 4 within said trench. *Id.* at paragraph [0088] with Figure 10B.

As expressly stated in Beyne, the deposited liner 2a is a tetraethyl orthosilicate (TEOS) liner, which is a dielectric liner lining the sidewalls of isolating trench 3. Although Figure 10B of Beyne illustrates that the top of isolating trench 3 is pinched off by TEOS liner 2a, airgap 4 is not entirely enclosed by TEOS liner 2a in isolating trench 3 since the bottom of isolating trench 3 remains open. Thus, Applicants respectfully submit that Beyne also fails to disclose or suggest, for example, "wherein each of said plurality of through silicon vias has [...] another pinched off region at a bottom portion," and "wherein said hollow center is tapered in said another pinched off region," as recited in amended independent claim 13 of the present application.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 13 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA, Edelstein and Beyne, either singly or in any combination thereof. Consequently, Applicants respectfully submit that independent claim 13 is patentably distinguishable over the alleged AAPA, Edelstein and Beyne. As such, claims

14 and 17 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

B. Rejection of Claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejects 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne and Edelstein, and further in view of U.S. Patent Application Publication Number 2011/0237073 by Dao et al. (hereinafter "Dao"). *See* page 6 of the Office Action.

With regard to claims 1-7, 9 and 10, by the present amendment and response, Applicants have amended independent claim 1 to include features similar to those in amended independent claim 13. *See* claim 1 above. For at least similar reasons presented above, Applicants respectfully assert that none of the alleged AAPA, Beyne and Edelstein discloses or suggests, for example, "wherein said hollow center is tapered in said pinched off region," as recited in amended independent claim 1 of the present application. Applicants respectfully assert that the above-cited feature is also not disclosed by Dao.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 1 is neither anticipated by, nor is obvious in light of, the disclosures

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provided by the alleged AAPA, Beyne, Edelstein and Dao, either singly or in any combination thereof. Consequently, Applicants respectfully submit that independent claim 1 is patentably distinguishable over the alleged AAPA, Beyne, Edelstein and Dao. As such, claims 2-7, 9 and 10 depending from and further limiting patentable independent claim 1 are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne, Edelstein and Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

With regard to claims 15, 16, 19 and 20, as discussed above, amended independent claim 13 is patentably distinguishable over the alleged AAPA, Beyne and Edelstein. As such, claims 15, 16, 19 and 20 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne and Edelstein, and the alleged AAPA, Beyne and Edelstein in combination with any other cited references, such as Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

C. **Rejection of Claims 8 and 18 under pre-AIA 35 U.S.C. § 103(a)**

In the Office Action, the Examiner rejects claims 8 and 18 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne, Edelstein and Dao, and further in view of U.S. Patent Application Publication Number 2008/0258307 by Ito et al. (hereinafter "Ito"). *See* page 16 of the Office Action. However, as discussed above, independent claims 1 and 13 are patentably

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distinguishable over the alleged AAPA, Beyne, Edelstein and Dao. As such, claim 8 depending from and further limiting patentable independent claim 1, and claim 18 depending from and further limiting patentable independent claim 13, are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne, Edelstein and Dao, and the alleged AAPA, Beyne, Edelstein and Dao in combination with any other cited reference, such as Ito, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

D. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claims 1 and 13, and claims depending therefrom, are patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all of the reasons presented above, an early allowance of claims 1-10 and 13-20 pending in the present application is respectfully requested.

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Attorney Docket No.: 0150167

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 06/22/2015

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FACSIMILE TRANSMISSION COVER SHEET

Date: June 22, 2015

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-8300

Re: **Application Serial No.: 13/415,744**
Filing Date: 03/08/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 17

Message:

Enclosed, please find the Amendment and Response to Non-Final Office Action dated February 20, 2015.

Payment for First Month Extension of Time in the Amount of **$200.00** is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731.**

Thank you.

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☒ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/22/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/NICHELE PETERSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 02/20/2015

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EXAMINER	
BACHNER, ROBERT G	

ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
02/20/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 13/415,744	Applicant(s) JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/27/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10 and 13-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10 and 13-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7/8/14* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicants' amendment filed 1/27/15 with RCE has been entered and considered. Applicant's arguments with respect to claims 1 and 13 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 14 and 17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA) citations referring to applicants' U.S. Application Publication No. 2013/0087893, in view of Beyne U.S. Provisional Patent Application No. 61/420,653 (copy attached), citations refer to U.S. Patent Application Publication No. 2012/0139127 further in view of Edelstein (U.S. Patent Application No. 2005/0121768).

Regarding Claim 13.

AAPA discloses (AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said semiconductor substrate comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (conductive fill shown as shaded area),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward; to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

In related art, Edelstein discloses Fig. 2b and 6d-f:

Said hollow center (220) being entirely surrounded by said conductive filler(225) to provide space for said conductive filler to expand inward, (See [0041]). Edelstein discloses that providing the hollow portion 220 provides the benefit of reducing thermal stresses on the substrate. See [0041]. Thus, it would have been obvious to one having ordinary skill in the art to provide the hollows as taught by Edelstein for the thermal benefits taught by Edelstein.

In related art, Beyne discloses (10B-H)

each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070],

disclosing that the airgaps help reduce stress in the substrate TSV interface); wherein each of said plurality of through silicon vias (Fig. 10b) has a pinched off region (Pinch-off trench) at a top portion to prevent contamination during processing of said semiconductor substrate. (See Abstract, [0017], [0066]-[0068], [0078].

Beyne discloses that the pinch off trench top provides good TSV. the airgap and via is formed of good quality, and does not contain contamination. Thus, it would have been obvious to modify AAPA by including the pinch-off top portion to include the air-gap for the benefit of avoiding stress in the VIA and obtaining good quality TSV. The modified AAPA would result the hollow center being surrounded by said conductive filler, because AAPA is relied on for the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. Thus, the features of claim 13 would have been obvious to one having ordinary skill in the art.

Regarding Claim 14.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

Beyne disclose that the pinched off portion that is overhanging the trench forms the airgap. Beyne discloses that the pinch off may be formed by a dielectric. See Abstract,

The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a

width smaller than a width of said through silicon vias. (See Beyne Fig. 10b-h, and Abstract, [0017], [0070] [0078], [0093] [0094] and claim 1). Beyne discloses that the use dielectric layer can be used to form the pinch off, which creates the airgaps which reduces stress in the TSV. Thus, it would have been obvious to form a dielectric pinch off as taught by Beyne in the device of AAPA for the benefit of reducing stress in the TSV.

Regarding Claim 17. The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.
The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held

unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 17 would have been obvious to one having ordinary skill in the art.

Claims 1-7, 9, 10, 15, 16, 19 and 20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA), in view of Beyne in view of Edelstein (U.S. Patent Application No. 2005/0121768) further in view of Dao (U.S. Patent Application No. 2011/0237073)

Regarding Claim 1.

(AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said semiconductor substrate (110) comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (fill disposed in 118 figs. 1A & 1B),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward.

In related art, Edelstein discloses Fig. 2b and 6d-f:

Said hollow center (220) being entirely surrounded by said conductive filler(225) to provide space for said conductive filler to expand inward, (See [0041]). Edelstein discloses that providing the hollow portion 220 provides the benefit of reducing thermal stresses on the substrate. See [0041]. Thus, it would have been obvious to one having ordinary skill in the art to provide the hollows as taught by Edelstein for the thermal benefits taught by Edelstein.

In related art, Beyne discloses (Fig. 10B-H):

each of said plurality of through silicon vias (2c through S) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface). Beyne discloses that the airgaps help reduce stress in the TSV. Thus, it would have been obvious to modify AAPA to incorporate the airgap as taught by Beyne for the benefit of reducing the thermal stress in further processing of the device;

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. The modified AAPA would result the hollow center being surrounded by said conductive filler, because AAPA is relied on for the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Regarding Claim 2.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

Modified AAPA of claim 1 results in the features of claim 2. Namely,

The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further

processing as taught by Dao. Thus, the features of claim 2 would have been obvious to one having ordinary skill in the art.

Regarding Claim 3.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill during polishing. See [0017], [0025] [0028], See Figs 5-10. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 3 would have been obvious to one having ordinary skill in the art.

Regarding Claims 4 and 5

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S. 327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill for a TSV, With no unexpected results. Thus, the features of claims 4-5 would have been obvious.

Regarding Claim 6.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center. (See Dao Fig. 9, disclosing that bottom of Taper 16 is filled with 44.) Thus, modified AAPA would result in this feature, because the teaching of Beyne would include the pinched off hollow center, with the bottom filled as taught by Dao. Thus, the features of claim 6 would have been obvious to one having ordinary skill in the art.

Regarding Claim 7.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.

The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read

on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 7 would have been obvious to one having ordinary skill in the art.

Regarding Claim 9.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

Beyne discloses:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias. (See fig. 10b-H, pinch off trench, and Abstract and [0017] [0061] [0064]). Beyne discloses that the pinched off top portions creates air gap 4, which helps reduce stress in the substrate/via. Thus, it would have been obvious to provide a top pinch off for the benefit of obtaining the airgap 4 which reduces stress in AAPA.

Regarding Claim 10.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Modified AAPA results in this features, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled. See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA as done in regards to claim 1.

Regarding Claims 15 and 16.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S. 327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill for a TSV, with no unexpected results. Thus, the features of claims 15-16 would have been obvious.

Regarding Claim 19.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the

TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 18 would have been obvious to one having ordinary skill in the art.

Regarding Claim 20.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

AAPA does not disclose:

Dao discloses a taper bottom portion at (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Modified AAPA results in this feature, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled. See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA for the

benefits of obtaining an airgap to prevent stress as taught by Beyne and tapering to avoid contamination as taught by Dao. Thus, the features of claim 20 would have been obvious to one having ordinary skill in the art.

Claims 8 and 18 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA) Beyne in view of Edelstein (U.S. Patent Application No. 2005/0121768)in view of Dao further in view of Ito (U.S. Patent Application No. 2008/0258307)

Regarding Claim 8 and 18.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

In related art, Ito discloses:

The semiconductor substrate of claim 1/13, wherein each of said plurality of through silicon vias has at least one chamfered corner. (See Ito Figs. 2B, 3B, and [0051]) Ito discloses that the chamfered corners help avoid a stress concentration in the corners. Thus, it would have been obvious to chamfer the corners of the Vias of AAPA for the benefit of avoiding stress concentrations as taught by Ito.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BACHNER whose telephone number is (571)270-3888. The examiner can normally be reached on Mon-Thurs 8:30-5 alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio J. Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROBERT BACHNER/
Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 13/415,744	Applicant(s)/Patent Under Reexamination JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0121768	06-2005	Edelstein et al.	257/698
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	642	(through near silicon near via$2 tsv) and (air near gap airgap hollow)	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:39
L2	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:40
L3	60	(through near silicon near via$2 tsv) and (air near gap airgap hollow) and expand	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:47
L4	107841	(air near gap airgap hollow) and expand	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:47
L5	8936	(air near gap airgap hollow) and expand and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:47
L6	806	(air near gap airgap hollow) same expand and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:53
L7	7	("5686171" | "20040129451" | "6214703" | "20100090304" | "20070111390" | "20100120227" | "20070222037").PN.	US-PGPUB; USPAT	OR	OFF	2015/02/10 18:58
L8	680	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:03
L9	129	8 and semiconductor	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:04
L10	0	(air near gap airgap hollow) same expand and semiconductor and pinchoff	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:12
L11	10	(air near gap airgap hollow) same expand and semiconductor and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:12
L12	94	(air near gap airgap hollow) same expand and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:13
L13	229	(air near gap airgap hollow) same expand and thermal near stress	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:15
L14	71642	((257/774 OR 257/416 OR 257/737 OR 257/432 OR 257/531 OR 257/E21.502 OR 257/E23.021 OR 257/330 OR 257/415 OR 257/417 OR 257/434 OR 257/443 OR 257/446 OR 257/48 OR 257/532 OR 257/621 OR 257/678 OR 257/684 OR 257/741 OR 257/762 OR 257/773 OR 257/783 OR 257/94 OR 257/98 OR 257/99).CCLS.)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:21

L15	6	14 and (hollow air near gap) same (conductive near fill)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:22
L16	1904	14 and (hollow air near gap) same (conductive fill metal)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:22
L17	0	14 and (hollow air near gap) same (conductive near fill) and pinch near oof	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:23
L18	4	14 and (hollow air near gap) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:23
L19	6	(hollow air near gap) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:25
L20	8	(hollow air) same (conductive near fill) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:28
L21	324	(hollow air) same (conductive) and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:28
L22	70	(hollow air) same (conductive) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:28
L23	110	(hollow air) same (conductive metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:29
L24	72	(hollow air) same (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:29
L25	37	(hollow air) with (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:29
L26	72	(hollow air) same (metal) same via and pinch near off	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:33
L27	4	("20080258307" | "20110237073" | "20120139127" | "7795134").PN.	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:35
L28	1631	(through near silicon near via tsv) and (air hollow)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:36
L29	664	(through near silicon near via tsv) and (air hollow) and (thermal near stress expan$4)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:37
L30	252658	((H01L2924/00 OR H01L2224/73204 OR H01L2924/014 OR H01L2224/16225 OR H01L2924/0002 OR H01L2224/32225 OR H01L2924/1461 OR H01L2224/48091 OR H01L2924/00012 OR H01L2224/245 OR H01L2924/00015 OR H01L2924/10253 OR H01L2924/12041 OR H01L2224/16145 OR H01L2924/15311 OR H01P3/121 OR H01P3/16 OR H01P11/001 OR H01P11/002 OR H01P3/165 OR H01P5/00 OR H01P5/087 OR H01P5/107 OR Y10T29/49826 OR Y10T29/49016 OR Y10T156/10 OR Y10T428/24942 OR Y10T428/26 OR	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:38

		Y10T29/49908 OR Y10T29/49002 OR Y10T29/4902 OR Y10T29/49071 OR Y10T29/49117 OR Y10T29/49155 OR Y10T29/49165 OR Y10T29/4935 OR G02B6/4416).CPC.)				
L31	128776	((257/774 OR 257/415 OR 257/43 OR 257/531 OR 257/777 OR 257/E21.211 OR 257/E21.506 OR 257/E23.145 OR 257/209 OR 257/369 OR 257/421 OR 257/432 OR 257/437 OR 257/48 OR 257/499 OR 257/618 OR 257/675 OR 257/690 OR 257/692 OR 257/737 OR 257/762 OR 257/773 OR 257/783 OR 257/84 OR 257/88 OR 257/98 OR 257/99 OR 333/239 OR 333/21R OR 333/254 OR 333/1 OR 333/248 OR 333/256 OR 333/26 OR 333/260 OR 438/109 OR 438/667 OR 438/104 OR 438/107 OR 438/126 OR 438/455 OR 438/51 OR 438/613 OR 438/106 OR 438/108 OR 438/113 OR 438/118 OR 438/119 OR 438/121 OR 438/125 OR 438/17 OR 438/25 OR 438/26 OR 438/3 OR 438/424 OR 438/458 OR 438/459 OR 438/618 OR 438/637 OR 438/64 OR 438/660 OR 438/780).CCLS.)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:38
L32	334620	14 31 30	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:38
L33	32937	32 and (hollow air) same (conductive metal)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:39
L34	6657	32 and (hollow air) same (conductive metal) same (thermal stress)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:39
L35	38	32 and (hollow air) same (conductive metal) same (thermal stress) and (pinch near off)	US-PGPUB; USPAT	OR	OFF	2015/02/10 19:39

EAST Search History (Interference)

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2/ 10/ 2015 7:43:07 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Searched as detailed in the attached EAST SEARCH REPORT.	4/2/2014	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	8/15/2014	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	2/10/2015	/RGB/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/ROBERT BACHNER/ Examiner.Art Unit 2898	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	**Art Unit**
	ROBERT BACHNER	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/11/2013	04/02/2014	08/15/2014	02/10/2015					
	1	÷	✓	✓	✓					
	2	÷	✓	✓	✓					
	3	÷	✓	✓	✓					
	4	÷	✓	✓	✓					
	5	÷	✓	✓	✓					
	6	÷	✓	✓	✓					
	7	÷	✓	✓	✓					
	8	÷	✓	✓	✓					
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	10	÷	✓	✓	✓					
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	12	÷	-	-	-					
	13	÷	✓	✓	✓					
	14	÷	✓	✓	✓					
	15	÷	✓	✓	✓					
	16	÷	✓	✓	✓					
	17	÷	✓	✓	✓					
	18	÷	✓	✓	✓					
	19	÷	✓	✓	✓					
	20	÷	✓	✓	✓					

JAN 27 2015

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Application Number	13/415,744
Filing Date	03/8/2012
First Named Inventor	Jebory
Group Art Unit	2898
Examiner Name	Bachner, Robert G.
Attorney Docket Number	0150167

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat Office 47 (Apr. 11, 2000), which established RCE practice.

1. Submission required under 37 C.F.R. § 1.114
   - a. ☐ Previously submitted
     - i. ☐ Consider the amendment(s)/reply under 37 C.F.R. § 1.116 previously filed on _____ (Any unentered amendment(s) referred to above will be entered).
     - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - iii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Amendment/Reply
     - ii. ☐ Affidavit(s)/Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____

01/28/2015 APEREZAM 00000008 13415744
01 FC:1801 1200.00 OP

2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R.§ 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months. Fee under 37 C.F.R. § 1.17(i) required)
   - b. ☐ Other _____
3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-0731
     - i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
     - ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
     - iii. ☒ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed.
   - c. ☒ Payment by credit card for the amount of $ 1,800.00 (Form PTO-2038 enclosed).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Michael Farjami, Esq.	Registration No. (Attorney/Agent)	38135
Signature		Date	Jan. 27, 2015

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name (Print/Type)	EVAN C. GUNDERZMAN		
Signature		Date	1/27/15

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JAN 27 2015

Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**	Art Unit: 2898
Serial No.: 13/415,744	Examiner: Bachner, Robert G.
Filing Date: 03/08/2012	
For: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

AMENDMENT AND RESPONSE TO *ADVISORY ACTION*

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Advisory Action* dated December 5, 2014 in the above-referenced patent application. Please enter and consider the following amendments and remarks in light of the attached ***Request for Continued Examination*** filed under 37 CFR § 1.114 in the above-identified application.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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In the Claims:

Claim 1 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

Claim 2 (original): The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

Claim 3 (original): The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

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Claim 4 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

Claim 5 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

Claim 6 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

Claim 7 (original): The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 8 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 9 (original): The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

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Claim 10 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Claims 11-12 (canceled)

Claim 13 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing ~~reduce~~ thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

Claim 14 (original): The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

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Claim 15 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

Claim 16 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

Claim 17 (original): The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 18 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 19 (original): The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

Claim 20 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

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REMARKS

Prior to the present amendment and response, claims 1-10 and 13-20 were pending in the present application. By the present amendment and response, Applicants have amended claims 1 and 13. Thus, after the present amendment and response, claims 1-10 and 13-20 remain pending in the present application. Applicants respectfully request reconsideration and allowance of claims 1-10 and 13-20 in view of the above amendments and the following remarks.

A. Rejection of Claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a)

In the *Advisory Action* dated December 5, 2014 (hereinafter "Advisory Action"), the Examiner affirms rejection of claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over alleged Applicants' Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent Application Publication Number 2012/0139127 A1 by Eric Beyne (hereinafter "Beyne"). *See* page 1 of the Advisory Action; *and see* page 3 of the *Final* Office Action dated August 28, 2014 (hereinafter "Office Action"). For the reasons discussed below, Applicants respectfully submit that amended independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne, either singly or in combination.

The present application is directed, in part, to through silicon via (TSV) structures. *See*, e.g., page 4, lines 2-5 of the present application. For example, in one implementation, as shown in described in Figure 4 of the present application, exemplary

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TSV 402 may correspond to TSV 202 of Figure 2. *See*, e.g., *id.* at page 10, lines 3-4 with Figure 4. As illustrated in Figure 4, TSV 402 includes first depth d_3 and second depth d_4 in substrate 412, where TSV 402 tapers from first depth d_3 to second depth d_4. *Id.*, e.g., at lines 7-12 with Figure 4. Conductive filler 430 is deposited on sidewalls 440 of TSV 402 such that hollow center portion 432 and pinched off region 438 are formed in TSV 402. *See*, e.g., *id.* at page 11, lines 6-8 with Figure 4. For example, "hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402." *Id.*, e.g., at lines 15-21. "Hollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions." *Id.* "Such reduction in thermal and mechanical stress reduces cracking in substrate 412." *Id.*

By the present amendment and response, Applicants have amended independent claim 13 to recite, in part, "each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate." *See* claim 13 above. Support for amended independent claim 13 can be found at least page 11, lines 6-21 and Figure 4 of the present application.

In the Office Action, the Examiner asserts that the alleged AAPA discloses various features of independent claim 13 of the present application. *See* pages 3-4 of the Office Action. The Examiner concedes:

> AAPA does not disclose:

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> each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate. *Id.*

In an attempt to cure the acknowledged deficiencies of the alleged AAPA, the Examiner suggests combining the alleged AAPA with Beyne. *Id.* In the Advisory Action, the Examiner further asserts:

> Beyne teaches forming trenches around TSV. In the trenches, Beyne teaches using an airgap in the fill to reduce the thermal stresses on the substrate. This is evidenced in Beyne [0070]-[0076], [0083]-[0094] and Figs. 5and 10. Fig. 5 expressly teaches that the use of airgaps in filled features that are deposited in a silicon substrate reduces the stress on the substrate, which reduces cracking in the substrate from stress from the TSV, or thermal processing stress. Based on at least this teaching of Beyne, one having ordinary skill in the art would have been motivated to modify AAPA to include a airgap in the TSV for the benefit of reducing stress on the substrate, which prevents cracking. *See* page 1 of the Advisory Action.

As acknowledged by the Examiner above, Beyne merely describes "forming trenches *around* TSV." As depicted in Figure 2B of Beyne, isolating trench-like structure 3 having airgap 4 surrounds TSV 10 in the center. By contrast, previously unamended independent claim 13 requires "each of said plurality of through silicon vias having a hollow center being *surrounded by* said conductive filler." Applicants respectfully maintain that neither the alleged AAPA nor Beyne discloses or suggests, for example, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being

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surrounded by said conductive filler," as recited in previously unamended independent claim 13. Furthermore, even assuming, *ad arguendo*, that the Examiner's assertions above are proper, Applicants respectfully assert that Beyne does not disclose or suggest, for example, "each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate," as recited in amended independent claim 13.

Turning to Beyne, Beyne describes a specific method of "forming airgaps in isolating structures whereby **the structures are situated *around* a TSV interconnect structure** in order to reduce the mechanical stress, the electric field and capacitance effects in the surrounding areas of the large TSV interconnect structure." *See* page 1, paragraph [0015] of Beyne (emphases added by Applicants).

With reference to Figures 2A and 2B, Beyne provides:

> Turning now to FIG. 2A and FIG. 2B illustrating side views of a particular example of an embodiment, wherein the semiconductor substrate S has a 3D-TSV 10. **The semiconductor substrate S comprises a 3D-TSV 10** in the present example having a depth in the substrate S of around 50 μm and a diameter (width) around 2 μm and **further comprises isolating trench-like structures 3 having at least one airgap 4.** The trench-like structure 3 thus is a hollow trench-like structure comprising at least one airgap 4. A liner 2*a* may be deposited onto the substrate S and on the inner sidewalls 2*b* of TSV. In the present example, the liner 2*b* has a thickness of around 200 nm on the inner sidewalls of said TSV, although embodiments are not limited thereto. The liner further may pinch of the isolating trench-like structures 3 thereby creating an airgap 4 in the trench-like structures. FIG. 2A illustrates a side view and FIG. 2B illustrates a more detailed side view combined with a

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top view. *See id.* at page 4, paragraph [0064] with Figures 2A and 2B.

With reference to Figures 10A-10H, Beyne depicts various steps of fabricating "a Through Silicon Via (TSV) interconnect based on **the via middle approach whereby said TSV interconnects are surrounded by isolating trenches with airgaps**." *See id.* at page 6, paragraph [0079] (emphasis added by Applicants). As illustrated in Figure 10A, TSV hole 1 and isolating trench 3 are formed in substrate S. *Id.* with Figure 10A.

With reference to Figure 10B, Beyne further states:

> FIG. 10B illustrates a detailed view of the substrate S with a patterned photoresist 12, PMD and STI layer(s) 11 and a liner 2*a* deposited in the TSV hole and isolating trenches. The liner is deposited on the horizontal parts of the substrate 2*a* and onto the sidewalls of the TSV hole 2*b* and within the isolating trenches 2*c* FIG. 10B clearly illustrates the closure of the opening (top) of the isolating trenches 3 thereby pinching-off the trench and forming an airgap 4 within said trench. *Id.* at paragraph [0088] with Figure 10B.

As expressly stated in Beyne, the deposited liner 2a is a tetraethyl orthosilicate (TEOS) liner, which is a dielectric liner lining the sidewalls of isolating trench 3. Although Figure 10B of Beyne illustrates that the top of isolating trench 3 is pinched off by TEOS liner 2a, airgap 4 is not entirely enclosed by TEOS liner 2a in isolating trench 3 since the bottom of isolating trench 3 remains open. Moreover, since airgap 4 is not surrounded by a conductive material, Beyne does not disclose or suggest reducing stress in a substrate by providing space within a conductive material to allow it to expand inward. Thus, Applicants respectfully assert that the combination of the alleged AAPA and Beyne does not disclose or suggest, for example, "each of said plurality of through

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silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate," as recited in amended independent claim 13.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 13 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA and Beyne, either singly or in combination. Consequently, Applicants respectfully submit that independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne. As such, claims 14 and 17 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

B. Rejection of Claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. § 103(a)

In the Advisory Action, the Examiner affirms rejection of claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne, and further in view of U.S. Patent Application Publication Number 2011/0237073 by Dao et al. (hereinafter "Dao"). *See* page 1 of the Advisory Action; *and see* page 6 of the Office Action.

With regard to claims 1-7, 9 and 10, by the present amendment and response, Applicants have amended independent claim 1 to include features similar to those in

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amended independent claim 13. *See* claim 1 above. For at least similar reasons presented above, Applicants respectfully assert that neither the alleged AAPA nor Beyne discloses or suggests, for example, "said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward," as recited in amended independent claim 1 of the present application. Applicants respectfully assert that the above-mentioned features are also not disclosed by Dao.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 1 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA, Beyne and Dao, either singly or in any combination thereof. Consequently, Applicants respectfully submit that independent claim 1 is patentably distinguishable over the alleged AAPA, Beyne and Dao. As such, claims 2-7, 9, 10 depending from and further limiting patentable independent claim 1 are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne and Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

With regard to independent claims 15, 16, 19 and 20, as discussed above, amended independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne. As such, claims 15, 16, 19 and 20 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, and the alleged AAPA and Beyne in combination with any other cited

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references, such as Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

C. Rejection of Claims 8 and 18 under pre-AIA 35 U.S.C. § 103(a)

In the Advisory Action, the Examiner affirms rejection of claims 8 and 18 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne and Dao, and further in view of U.S. Patent Application Publication Number 2008/0258307 by Ito et al. (hereinafter "Ito"). *See* page 1 of the Advisory Action; *and see* page 15 of the Office Action. However, as discussed above, independent claims 1 and 13 are patentably distinguishable over the alleged AAPA, Beyne and Dao. As such, claim 8 depending from and further limiting patentable independent claim 1, and claim 18 depending from and further limiting patentable independent claim 13, are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne and Dao, and the alleged AAPA, Beyne and Dao in combination with any other cited references, such as Ito, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

D. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claims 1 and 13, and claims depending therefrom, are patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all

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of the reasons presented above, an early allowance of claims 1-10 and 13-20 pending in the present application is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: Jan. 27, 2015

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FACSIMILE TRANSMISSION COVER SHEET

Date: January 27, 2015

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-8300

Re: **Application Serial No.: 13/415,744**
Filing Date: 03/08/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 17

Message:

Enclosed please find:

1. Request for Continued Examination;
2. Amendment and Response to Advisory Action.

Payment for Request for Continued Examination and Second Month Extension Fee in the Amount of $1,800.00 is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account 50-0731.

Thank you.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/27/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/AMANDA FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 12/05/2014

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EXAMINER	
BACHNER, ROBERT G	

ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
12/05/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
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Advisory Action Before the Filing of an Appeal Brief	**Application No.** 13/415,744	**Applicant(s)** JEBORY ET AL.	
	Examiner ROBERT BACHNER	**Art Unit** 2898	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 November 2014 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;
(2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): (a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
Applicants argue that AAPA could not reasonably be modified in view of Beyne without "impremissible hindsight" from Applicants' specification to arrive at the features of claims 1 and 13. The Examiner disagrees. Beyne teaches forming tenches around TSV. In the trenches, Beyne teaches use of an airgap in the fill to reduce the thermal stresses on the substrate. This is evidenced in Beyne [0070]-[0076], [0083]-[0094] and Figs. 5 and 10. Fig. 5 expressly teaches that use of airgaps in filled features that are deposited in a silicon substrate reduces the stress on the substrate, which reduces cracking in the substrate from stress from the TSV, or thermal processing stress. Based on at least this teaching of Beyne, one having ordinary skill in the art would have been motivated to modify AAPA to include a airgap in the TSV for the benefit of reducing stress on the substrate, which prevents cracking. Thus, the well-made rejection is hereby maintained.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

/ROBERT BACHNER/
Examiner, Art Unit 2898

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Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**	Art Unit: 2898
Serial No.: 13/415,744	Examiner: Bachner, Robert G.
Filing Date: 03/08/2012	
For: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

RESPONSE TO *FINAL* OFFICE ACTION

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Final* Office Action dated August 28, 2014 in the above-referenced patent application. Please enter and consider the following remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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In the Claims:

Claim 1 (previously presented): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being surrounded by said conductive filler;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

Claim 2 (original): The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

Claim 3 (original): The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

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Claim 4 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

Claim 5 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

Claim 6 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

Claim 7 (original): The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 8 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 9 (original): The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

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Claim 10 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Claims 11-12 (canceled)

Claim 13 (previously presented): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

Claim 14 (original): The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

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Claim 15 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

Claim 16 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

Claim 17 (original): The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 18 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 19 (original): The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

Claim 20 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

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REMARKS

Prior to the present response, claims 1-10 and 13-20 were pending in the present application. No claims are amended by the present response. Thus, after the present response, claims 1-10 and 13-20 remain pending in the present application. Applicants respectfully request reconsideration and allowance of claims 1-10 and 13-20 in view of the following remarks.

A. Rejection of Claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a)

In the *Final* Office Action dated August 28, 2014 (hereinafter "Office Action"), the Examiner rejects claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over alleged Applicants' Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent Application Publication Number 2012/0139127 A1 by Eric Beyne (hereinafter "Beyne"). *See* page 3 of the Office Action. For the reasons discussed below, Applicants respectfully submit that previously presented independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne, either singly or in combination.

The present application is directed, in part, to through silicon via structures. *See*, e.g., page 4, lines 2-5 of the present application. For example, in one implementation, as shown in described in Figure 4 of the present application, exemplary TSV 402 may correspond to TSV 202 of Figure 2. *See*, e.g., *id.* at page 10, lines 3-4 with Figure 4. As illustrated in Figure 4, TSV 402 includes first depth d_3 and second depth d_4 in substrate

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412, where TSV 402 tapers from first depth d_3 to second depth d_4. *Id.*, e.g., at lines 7-12 with Figure 4. Conductive filler 430 is deposited on sidewalls 440 of TSV 402 such that hollow center portion 432 and pinched off region 438 are formed in TSV 402. *See*, e.g., *id.* at page 11, lines 6-8 with Figure 4. For example, "hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402." *Id.*, e.g., at lines 15-21. "Hollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions." *Id.* "Such reduction in thermal and mechanical stress reduces cracking in substrate 412." *Id.*

Previously presented independent claim 13 recites, in part, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate." *See* claim 13 above.

In the Office Action, the Examiner asserts that the alleged AAPA discloses various features of independent claim 13 of the present application. *See* pages 3-4 of the Office Action. The Examiner concedes:

> AAPA does not disclose:
>
> each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate. *Id.*

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In an attempt to cure the acknowledged deficiencies of the alleged AAPA, the Examiner suggests combining the alleged AAPA with Beyne. *Id.* Specifically, the Examiner asserts:

> In related art, Beyne discloses (10B-H)
>
> each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface); wherein each of said plurality of through silicon vias (Fig. 10b) has a pinched off region (Pinch-off trench) at a top portion to prevent contamination during processing of said semiconductor substrate. (See Abstract, [0017], [0066]-[0068], [0078]. Beyne discloses that the pinch off trench top provides good TSV. The airgap and via is formed of good quality, and does not contain contamination). Thus, it would have been obvious to modify AAPA by including the pinch-off top portion to include the air-gap for the benefit of avoiding stress in the VIA and obtaining good quality TSV. The modified AAPA would result the hollow center being surrounded by said conducive filler, because AAPA is relied on for the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. Thus, the features of claim 13 would have been obvious to one having ordinary skill in the art. *Id.*

Applicants respectfully disagree with the Examiner's assertions above.

Turning to Beyne, Beyne describes a specific method of "forming airgaps in isolating structures whereby **the structures are situated *around* a TSV interconnect structure** in order to reduce the mechanical stress, the electric field and capacitance effects in the surrounding areas of the large TSV interconnect structure." *See* page 1, paragraph [0015] of Beyne (emphases added by Applicants).

With reference to Figures 2A and 2B, Beyne provides:

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> Turning now to FIG. 2A and FIG. 2B illustrating side views of a particular example of an embodiment, wherein the semiconductor substrate S has a 3D-TSV 10. **The semiconductor substrate S comprises a 3D-TSV 10** in the present example having a depth in the substrate S of around 50 μm and a diameter (width) around 2 μm and **further comprises isolating trench-like structures 3 having at least one airgap 4.** The trench-like structure 3 thus is a hollow trench-like structure comprising at least one airgap 4. A liner 2*a* may be deposited onto the substrate S and on the inner sidewalls 2*b* of TSV. In the present example, the liner 2*b* has a thickness of around 200 nm on the inner sidewalls of said TSV, although embodiments are not limited thereto. The liner further may pinch of the isolating trench-like structures 3 thereby creating an airgap 4 in the trench-like structures. FIG. 2A illustrates a side view and FIG. 2B illustrates a more detailed side view combined with a top view. *See id.* at page 4, paragraph [0064] with Figures 2A and 2B.

With reference to Figures 10A-10H, Beyne depicts various steps of fabricating "a Through Silicon Via (TSV) interconnect based on the via middle approach whereby said TSV interconnects are surrounded by isolating trenches with airgaps." *See id.* at page 6, paragraph [0079]. As illustrated in Figure 10A, TSV hole 1 and isolating trench 3 are formed in substrate S. *Id.* with Figure 10A. With reference to Figure 10B, Beyne further states:

> FIG. 10B illustrates a detailed view of the substrate S with a patterned photoresist 12, PMD and STI layer(s) 11 and a liner 2*a* deposited in the TSV hole and isolating trenches. The liner is deposited on the horizontal parts of the substrate 2*a* and onto the sidewalls of the TSV hole 2*b* and within the isolating trenches 2*c* FIG. 10B clearly illustrates the closure of the opening (top) of the isolating trenches 3 thereby pinching-off the trench and forming an airgap 4 within said trench. *Id.* at paragraph [0088] with Figure 10B.

As further stated in Beyne, "FIG. 10C illustrates the deposition of barrier material and conductive material 21 onto the substrate S thereby filling the TSV hole with

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conductive material in order to create a TSV interconnect 10." *Id.* at paragraph [0090] with Figure 10C.

Thus, Beyne describes forming an isolating trench-like structure surrounding a TSV, where the isolating trench-like structure includes an airgap to help isolate high mechanical stress in the substrate. As depicted in Figure 2B of Beyne, isolating trench-like structure 3 having airgap 4 surrounds TSV 10 in the center. As described in Beyne, by concentrating and capturing the stress in the ring of substrate material in between the isolating trench-like structure and the TSV, cracking in the substrate between closely spaced TSVs can be avoided. *See id.* at page 5, paragraph [0070]. However, neither the alleged AAPA nor Beyne describes or suggests, for example, forming a hollow center *within* the conductive material in a through silicon via to reduce thermal stress in a semiconductor substrate. Rather, the Examiner has apparently relied upon Applicants' own disclosure stating that after said modification,

> The modified AAPA would result the hollow center being surrounded by said conducive filler, because AAPA is relied on for the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. *See* page 4 of the Office Action.

Applicants respectfully submit that the combination of the alleged AAPA and Figures 10B-H of Beyne is improper because the Examiner relies on information gleaned solely from the present application. MPEP § 2142 states that "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Consequently, Applicants respectfully submit that the

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Examiner has not pointed to a teaching, suggestion, or motivation in either the alleged AAPA or Figures 10B-H of Beyne which would prompt one of ordinary skill in the art to combine these references for the purpose of forming "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate," as recited in previously presented independent claim 13 of the present application.

For all of the reasons set forth above, Applicants respectfully submit that previously presented independent claim 13 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA and Beyne, either singly or in combination. Consequently, Applicants respectfully submit that independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne. As such, claims 14 and 17 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

B. Rejection of Claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejects claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over

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the alleged AAPA in view Beyne, and further in view of U.S. Patent Application Publication Number 2011/0237073 by Dao et al. (hereinafter "Dao"). *See* page 6 of the Office Action.

With regard to claims 1-7, 9 and 10, previously presented independent claim 1 includes features similar to those in previously presented independent claim 13. *See* claim 1 above. For at least similar reasons presented above, Applicants respectfully assert that neither the alleged AAPA nor Beyne discloses or suggests, for example, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being surrounded by said conductive filler," as recited in previously presented independent claim 1 of the present application. Applicants respectfully assert that the above-mentioned features are also not disclosed by Dao.

For all of the reasons set forth above, Applicants respectfully submit that previously presented independent claim 1 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA, Beyne and Dao, either singly or in any combination thereof. Consequently, Applicants respectfully submit that independent claim 1 is patentably distinguishable over the alleged AAPA, Beyne and Dao. As such, claims 2-7, 9, 10 depending from and further limiting patentable independent claim 1 are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne and Dao, for at

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least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

With regard to independent claims 15, 16, 19 and 20, as discussed above, previously presented independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne. As such, claims 15, 16, 19 and 20 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, and the alleged AAPA and Beyne in combination with any other cited references, such as Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

C. **Rejection of Claims 8 and 18 under pre-AIA 35 U.S.C. § 103(a)**

In the Office Action, the Examiner rejects claims 8 and 18 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne and Dao, and further in view of U.S. Patent Application Publication Number 2008/0258307 by Ito et al. (hereinafter "Ito"). *See* page 15 of the Office Action. However, as discussed above, independent claims 1 and 13 are patentably distinguishable over the alleged AAPA, Beyne and Dao. As such, claim 8 depending from and further limiting patentable independent claim 1, and claim 18 depending from and further limiting patentable independent claim 13, are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne and Dao, and the alleged AAPA, Beyne and Dao in

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combination with any other cited references, such as Ito, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

D. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claims 1 and 13, and claims depending therefrom, are patentably novel and inventive. Thus, for all of the reasons presented above, an early allowance of claims 1-10 and 13-20 pending in the present application is respectfully requested.

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Attorney Docket No.: 0150167

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: Nov. 20, 2014

Michael Farjami, Esq.
Reg. No. 38,135

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FACSIMILE TRANSMISSION COVER SHEET

Date: November 20, 2014

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-8300

Re: **Application Serial No.: 13/415,744**
Filing Date: 03/08/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 16

Message:

Enclosed please find the Response to Final Office Action dated August 28, 2014.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)		(Column 2)		
FOR	NUMBER FILED		NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A		N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A		N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A		N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =		*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =		*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	11/20/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/AMANDA FORD/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 08/28/2014

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EXAMINER	
BACHNER, ROBERT G	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
08/28/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 13/415,744	Applicant(s) JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/8/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10 and 13-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10 and 13-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7/8/14* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicants' amendment filed 7/8/14 has been entered and considered. Applicants' amendment of the drawings overcomes the objections to the drawings detailed in the previous Office Action. Applicants have amended claims 1 and 13, and argue that these claims are patentable over the cited references. The Examiner disagrees. AAPA teaches a conductive filler in figs. 1a and b. The proposed modification of AAPA is to include Beyne's pinch off, and hollow 4 in the conductive material of AAPA. This modified AAPA would result in the feature "said hollow center being surrounded by said conductive filler", as recited in claim 1 and similarly recited in claim 13, because the proposed modification would include the hollow as taught by Beyne in the conductive filled TSV of AAPA. Including the pinch off and hollow in the device of AAPA would provide the benefit of reducing mechanical stress on the substrate, as taught by Beyne at least at [0013]-[0015], [0037], [0069]-[0086]. For at least these reasons, the features of claims 1 and 13 are properly read on AAPA in view of Beyne. This rejection is hereby made **FINAL**.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

> obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 14 and 17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA) citations referring to applicants' U.S. Application Publication No. 2013/0087893, in view of Beyne U.S. Provisional Patent Application No. 61/420,653 (copy attached), citations refer to U.S. Patent Application Publication No. 2012/0139127.

Regarding Claim 13.

AAPA discloses (AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said semiconductor substrate comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (conductive fill shown as shaded area),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

In related art, Beyne discloses (10B-H)

each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface); wherein each of said plurality of through silicon vias (Fig. 10b) has a pinched off region (Pinch-off trench) at a top portion to prevent contamination during processing of said semiconductor substrate. (See Abstract, [0017], [0066]-[0068], [0078].

Beyne discloses that the pinch off trench top provides good TSV. the airgap and via is formed of good quality, and does not contain contamination. Thus, it would have been obvious to modify AAPA by including the pinch-off top portion to include the air-gap for the benefit of avoiding stress in the VIA and obtaining good quality TSV. The modified AAPA would result the hollow center being surrounded by said conductive filler, because AAPA is relied on for the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. Thus, the features of claim 13 would have been obvious to one having ordinary skill in the art.

Regarding Claim 14.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

Beyne disclose that the pinched off portion that is overhanging the trench forms the airgap. Beyne discloses that the pinch off may be formed by a dielectric. See Abstract,

The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias. (See Beyne Fig. 10b-h, and Abstract, [0017], [0070] [0078], [0093] [0094] and claim 1). Beyne discloses that the use dielectric layer can be used to form the pinch off, which creates the airgaps which reduces stress in the TSV. Thus, it would have been obvious to form a dielectric pinch off as taught by Beyne in the device of AAPA for the benefit of reducing stress in the TSV.

Regarding Claim 17. The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.
The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular

arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 17 would have been obvious to one having ordinary skill in the art.

Claims 1-7, 9, 10, 15, 16, 19 and 20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA), in view of Beyne further in view of Dao (U.S. Patent Application No. 2011/0237073).

Regarding Claim 1.

(AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said semiconductor substrate (110) comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (fill disposed in 118 figs. 1A & 1B),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, said hollow center being surrounded by said conductive filler.

In related art, Beyne discloses (Fig. 10B-H):

each of said plurality of through silicon vias (2c through S) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface). Beyne discloses that the airgaps help reduce stress in the TSV. Thus, it would have been obvious to modify AAPA to incorporate the airgap as taught by Beyne for the benefit of reducing the thermal stress in further processing of the device;

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. The modified AAPA would result the hollow center being surrounded by said conductive filler, because AAPA is relied on for

the conductive filler. That is, the hollow center, and pinch off would be provided in the device of AAPA for the benefit of reducing stress on the substrate of AAPA. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Regarding Claim 2.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

Modified AAPA of claim 1 results in the features of claim 2. Namely,

The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 2 would have been obvious to one having ordinary skill in the art.

Regarding Claim 3.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination

during polishing said bottom surface of said substrate. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill during polishing. See [0017], [0025] [0028], See Figs 5-10. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 3 would have been obvious to one having ordinary skill in the art.

Regarding Claims 4 and 5

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S.

327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill for a TSV, With no unexpected results. Thus, the features of claims 4-5 would have been obvious.

Regarding Claim 6.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center. (See Dao Fig. 9, disclosing that bottom of Taper 16 is filled with 44.) Thus, modified AAPA would result in this feature, because the teaching of Beyne would include the pinched off hollow center, with the bottom filled as taught by Dao. Thus, the features of claim 6 would have been obvious to one having ordinary skill in the art.

Regarding Claim 7.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.

The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 7 would have been obvious to one having ordinary skill in the art.

Regarding Claim 9.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

Beyne discloses:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias. (See fig. 10b-H, pinch off trench, and Abstract and [0017] [0061] [0064]). Beyne discloses that the pinched off top portions creates air gap 4, which helps reduce stress in the substrate/via. Thus, it would have been obvious to provide a top pinch off for the benefit of obtaining the airgap 4 which reduces stress in AAPA.

Regarding Claim 10.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Modified AAPA results in this features, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled.

See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA as done in regards to claim 1.

Regarding Claims 15 and 16.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S. 327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill

for a TSV, with no unexpected results. Thus, the features of claims 15-16 would have been obvious.

Regarding Claim 19.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 18 would have been obvious to one having ordinary skill in the art.

Regarding Claim 20.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

AAPA does not disclose:

Dao discloses a taper bottom portion at (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Modified AAPA results in this feature, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled. See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA for the benefits of obtaining an airgap to prevent stress as taught by Beyne and tapering to avoid contamination as taught by Dao. Thus, the features of claim 20 would have been obvious to one having ordinary skill in the art.

Claims 8 and 18 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA) Beyne in view of Dao further in view of Ito (U.S. Patent Application No. 2008/0258307)

Regarding Claim 8 and 18.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

In related art, Ito discloses:

The semiconductor substrate of claim 1/13, wherein each of said plurality of through silicon vias has at least one chamfered corner. (See Ito Figs. 2B, 3B, and [0051]) Ito discloses that the chamfered corners help avoid a stress concentration in the corners. Thus, it would have been obvious to chamfer the corners of the Vias of AAPA for the benefit of avoiding stress concentrations as taught by Ito.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BACHNER whose telephone number is (571)270-3888. The examiner can normally be reached on Mon-Thurs 8:30-5 alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio J. Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROBERT BACHNER/
Examiner, Art Unit 2898

/JULIO J. MALDONADO/

Supervisory Patent Examiner, Art Unit 2898

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Searched as detailed in the attached EAST SEARCH REPORT.	4/2/2014	/RGB/
Searched as detailed in the attached EAST SEARCH REPORT.	8/15/2014	/RGB/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/ROBERT BACHNER/ Examiner.Art Unit 2898	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"13415744"	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L2	652	Jebory near Hadi Howard near David	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L3	8928	(through near silicon near via$2 TSV)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L4	0	(through near silicon near via$2 TSV) and tapper	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L5	79	(through near silicon near via$2 TSV) and pinch near off	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L6	87	(through near silicon near via$2 TSV) and pinch$3 near off	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L7	1	"13744864"	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L8	6	("20090098737" | "20090206416" | "20110081753" | "20120061773" | "7241700" | "7575991").PN.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L9	8	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$).did.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L10	11	("2010/0230818").URPN.	USPAT	OR	OFF	2014/08/15 16:47
L11	40	(through near silicon near via$2 TSV) and pinch near off and void	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L12	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$).did.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L13	681	(through near silicon near via$2 TSV) and void	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L14	40	(through near silicon near via$2 TSV) and void and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L15	10	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$).did. or (US-7829976-$ or US-7772123-$ or	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47

		US-7749899-$ or US-8178950-$).did.				
L16	11	("2010/0230818").URPN.	USPAT	OR	OFF	2014/08/15 16:47
L17	23	("20060273455" | "20070085198" | "20070152194" | "20070228546" | "5424245" | "5493096" | "5501893" | "5599744" | "5679978" | "6150252" | "6333265" | "6589865" | "6821896" | "6861312" | "6908841" | "6919255").PN. OR ("7772123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/08/15 16:47
L18	47	(through near silicon near via$2 TSV) and (void hollow) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L19	955	(through near silicon near via$2 TSV) and (void hollow)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L20	106	(through near silicon near via$2 TSV) and (void hollow) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L21	14	(through near silicon near via$2 TSV) and (void hollow) same (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L22	38	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (tapper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L23	79	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L24	167	newport near fab	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L25	19	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$).did.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L26	210	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L27	5	(through near silicon near via$2 TSV) and (void hollow) and (thermal stress) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L28	6	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same contaminat$	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L29	216	(through near silicon near via$2 TSV) and (taper pinch near off narrow) and contaminat$	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L36	513	("20010020739" | "20020005583" | "20020006687" | "20020020898" | "20020027293" | "20020057468" | "20020059722" | "20020060208" | "20020089025" | "20020094607" | "20020096729" | "20020113296" |	US-PGPUB; USPAT; USOCR	OR	OFF	2014/08/15 16:47

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L38	6	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L39	21	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L40	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L41	1	(US-7795134-$).did.	USPAT	OR	OFF	2014/08/15 16:47
L42	279	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L43	3030	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L44	1146	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L45	238	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L46	111	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L47	162	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L48	1	"8039386"	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L49	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47

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L51	0	L50 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L52	35	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L53	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L54	6	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L55	86	(through near silicon near via$2 TSV contact near hole) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
L56	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2014/08/15 16:47
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L61	110	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4 and polish$4	US-PGPUB; USPAT	OR	OFF	2014/08/15 17:08
L62	178	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) same conduct$4	US-PGPUB; USPAT	OR	OFF	2014/08/15 17:08
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EAST Search History (Interference)

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8/ 15/ 2014 5:46:16 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/11/2013	04/02/2014	08/15/2014						
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Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**	Art Unit: 2898
Serial No.: 13/415,744	Examiner: Bachner, Robert G.
Filing Date: 03/08/2012	
For: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

AMENDMENT AND RESPONSE TO *NON-FINAL* OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Non-Final* Office Action dated April 8, 2014 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

PAGE 2/19 * RCVD AT 7/8/2014 6:50:06 PM [Eastern Daylight Time] * SVR:W-PTOFAX-002/6 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):06-13

In the Drawings:

Please enter replacement Figures 1A, 1B and 4 in the present application. Applicants amend Figures 1A and 1B to include the legend "Prior Art." Applicants amend Figure 4 to remove reference numeral 422. No new matter is introduced by replacement Figures 1A, 1B and 4. Two drawing replacement sheets, marked as such, are provided at the end of the present amendment and response.

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In the Claims:

Claim 1 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being surrounded by said conductive filler;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

Claim 2 (original): The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

Claim 3 (original): The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

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Claim 4 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

Claim 5 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

Claim 6 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

Claim 7 (original): The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 8 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 9 (original): The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

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Claim 10 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Claims 11-12 (canceled)

Claim 13 (currently amended): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

Claim 14 (original): The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

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Claim 15 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

Claim 16 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

Claim 17 (original): The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 18 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 19 (original): The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

Claim 20 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

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REMARKS

Prior to the present amendment and response, claims 1-10 and 13-20 were pending in the present application. By the present amendment and response, Applicants have amended Figures 1A, 1B and 4, and claims 1 and 13. Thus, after the present amendment and response, claims 1-10 and 13-20 remain pending in the present application. Applicants respectfully request reconsideration and allowance of claims 1-10 and 13-20 in view of the above amendments and the following remarks.

A. Objection to the Drawings

In the *Non-Final* Office Action, dated April 8, 2014 (hereinafter "Office Action"), the Examiner objects to Figures 1A, 1B and 4 of the present application. *See* page 2 of the Office Action. By the present amendment and response, Applicants have amended Figures 1A and 1B to include the legend "Prior Art." Applicants have also amended Figure 4 to remove reference numeral 422. Two replacement sheets including the amended Figures 1A, 1B and 4 are enclosed and filed herewith. Applicants respectfully submit that the objection to Figures 1A, 1B and 4 has now been overcome.

B. Rejection of Claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejects claims 13, 14 and 17 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over alleged Applicants' Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent Application Publication

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Number 2012/0139127 A1 by Eric Beyne (hereinafter "Beyne"). *See* page 3 of the Office Action. For the reasons discussed below, Applicants respectfully submit that amended independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne, either singly or in combination.

The present application is directed, in part, to through silicon via structures. *See*, e.g., page 4, lines 2-5 of the present application. For example, in one implementation, as shown in described in Figure 2 of the present application, exemplary semiconductor structure 200 includes semiconductor devices 208 and 210, and narrow through-silicon vias (TSVs) 202, 204 and 206 in substrate 212. *See*, e.g., *id.* at page 7, lines 15-22 with Figure 2. "The novel features of narrow TSVs 202, 204 and 206 [...] allow exemplary semiconductor devices 208 and 210 to be placed much closer to TSVs 202, 204 and 206 than conventional TWV designs." *See*, e.g., *id.* at page 8, lines 6-9. "In addition, because TSVs 202, 204 and 206 may be placed much closer to each other than in conventional TWV designs, uniform thermal dissipation and heatsinking through TSVs 202, 204 and 206 becomes more practical." *Id.*, e.g., at lines 14-16 with Figure 2.

As disclosed in the present application, "Figure 4 presents an exemplary magnified view of TSV 402, which may correspond to TSV 202 of Figure 2, for example." *See*, e.g., *id.* at page 10, lines 3-4 with Figure 4. As illustrated in Figure 4, TSV 402 includes first depth d_3 and second depth d_4 in substrate 412, where TSV 402 tapers from first depth d_3 to second depth d_4. *Id.*, e.g., at lines 7-12 with Figure 4. Conductive filler 430 is deposited on sidewalls 440 of TSV 402 such that hollow center portion 432 and pinched

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off region 438 are formed in TSV 402. *See*, e.g., *id.* at page 11, lines 6-8 with Figure 4. For example, "hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402." *Id.*, e.g., at lines 15-21. "Hollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions." *Id.* "Such reduction in thermal and mechanical stress reduces cracking in substrate 412." *Id.*

By the present amendment and response, Applicants have amended independent claim 13 to recite, in part, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate." *See* claim 13 above. Support for amended independent claim 13 can be found at least in page 11, lines 6-21 and Figure 4 of the present application.

In the Office Action, the Examiner asserts that the alleged AAPA discloses various features of independent claim 13 of the present application. *See* pages 3-4 of the Office Action. The Examiner concedes:

> AAPA does not disclose:
>
> each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate. *Id.*

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In an attempt to cure the acknowledged deficiencies of the alleged AAPA, the Examiner suggests combining the alleged AAPA with Beyne. *Id.* Specifically, the Examiner asserts:

> In related art, Beyne discloses (10B-H)
>
> each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface); wherein each of said plurality of through silicon vias (Fig. 10b) has a pinched off region (Pinch-off trench) at a top portion to prevent contamination during processing of said semiconductor substrate. (See Abstract, [0017], [0066]-[0068], [0078]. Beyne discloses that the pinch off trench top provides good TSV. The airgap and via is formed of good quality, and does not contain contamination). *Id.*
>
> Turning to Beyne, with reference to Figure 10B,
>
> FIG. 10B illustrates a detailed view of the substrate S with a patterned photoresist 12, PMD and STI layer(s) 11 and a liner 2*a* deposited in the TSV hole and isolating trenches. The liner is deposited on the horizontal parts of the substrate 2*a* and onto the sidewalls of the TSV hole 2*b* and within the isolating trenches 2*c* FIG. 10B clearly illustrates the closure of the opening (top) of the isolating trenches 3 thereby pinching-off the trench and forming an airgap 4 within said trench. *See* page 6, paragraph [0088] with Figure 10B of Beyne.

As described in the Beyne, the liner deposited in isolating trench 2c is a tetraethyl orthosilicate (TEOS) liner, which is a dielectric material. *See id.* at paragraph [0023]. Thus, airgap 4 is formed in a dielectric liner in isolating trench 2c. As further depicted in Figure 10C of Beyne, conductive material 21 is deposited over the dielectric liner in TSV hole 2*b* above isolating trench 2c. In other words, Beyne describes depositing a dielectric liner in an isolating trench, where an airgap may be formed in the dielectric liner. Thus,

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Applicants respectfully assert that neither the alleged AAPA nor Beyne discloses or suggests, for example, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being surrounded by said conductive filler to reduce thermal stress in said semiconductor substrate," as recited in amended independent claim 13 of the present application.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 13 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA and Beyne, either singly or in combination. Consequently, Applicants respectfully submit that independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne. As such, claims 14 and 17 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

C. Rejection of Claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejects claims 1-7, 9, 10, 15, 16, 19 and 20 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne and further in view of U.S. Patent Application Publication Number 2011/0237073 by Dao et al. (hereinafter "Dao"). *See* page 6 of the Office Action.

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With regard to claims 1-7, 9 and 10, by the present amendment and response, Applicants have amended independent claim 1 to include features similar to those in amended independent claim 13. *See* claim 1 above. For at least similar reasons presented above, Applicants respectfully assert that neither the alleged AAPA nor Beyne discloses or suggests, for example, "a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being surrounded by said conductive filler," as recited in amended independent claim 1 of the present application. Applicants respectfully assert that the above-mentioned features are also not disclosed by Dao.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claim 1 is neither anticipated by, nor is obvious in light of, the disclosures provided by the alleged AAPA, Beyne, and Dao either singly or in any combination thereof. Consequently, Applicants respectfully submit that independent claim 1 is patentably distinguishable over the alleged AAPA, Beyne, and Dao. As such, claims 2-7, 9, 10 depending from and further limiting patentable independent claim 1 are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne, and Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

With regard to independent claims 15, 16, 19 and 20, as discussed above, amended independent claim 13 is patentably distinguishable over the alleged AAPA and Beyne.

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As such, claims 15, 16, 19 and 20 depending from and further limiting patentable independent claim 13 are, *a fortiori*, also patentably distinguishable over the alleged AAPA and Beyne, and the alleged AAPA and Beyne in combination with any other cited references, such as Dao, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

D. Rejection of Claims 8 and 18 under pre-AIA 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejects claims 8 and 18 under pre-AIA 35 U.S.C. §103(a) as being unpatentable for purported obviousness over the alleged AAPA in view Beyne and Dao, and further in view of U.S. Patent Application Publication Number 2008/0258307 by Ito et al. (hereinafter "Ito"). *See* page 16 of the Office Action. However, as discussed above, independent claims 1 and 13 are patentably distinguishable over the alleged AAPA, Beyne, and Dao. As such, claim 8 depending from and further limiting patentable independent claim 1, and claim 18 depending from and further limiting patentable independent claim 13, are, *a fortiori*, also patentably distinguishable over the alleged AAPA, Beyne, and Dao, and the alleged AAPA, Beyne, and Dao in combination with any other cited references, such as Ito, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

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E. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claims 1 and 13, and claims depending therefrom, are patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all of the reasons presented above, an early allowance of claims 1-10 and 13-20 pending in the present application is respectfully requested.

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Attorney Docket No.: 0150167

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 7/8/2014

Michael Farjami, Esq.
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Date of Facsimile: 7/8/14

Diane Arnett
Name of Person Performing Facsimile Transmission

Diane Arnett 7/8/14
Signature Date

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DRAWING REPLACEMENT SHEETS

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REPLACEMENT SHEET

Fig. 1A (Prior Art)

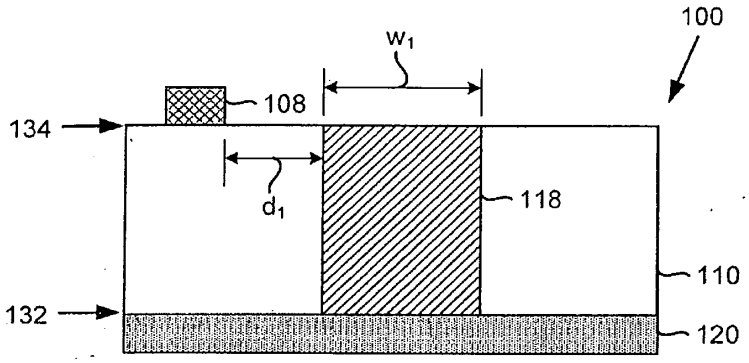
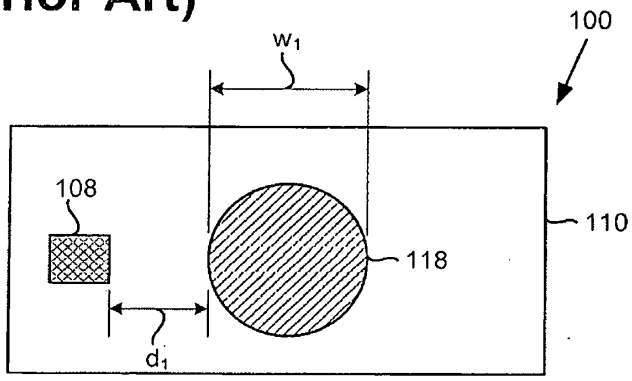
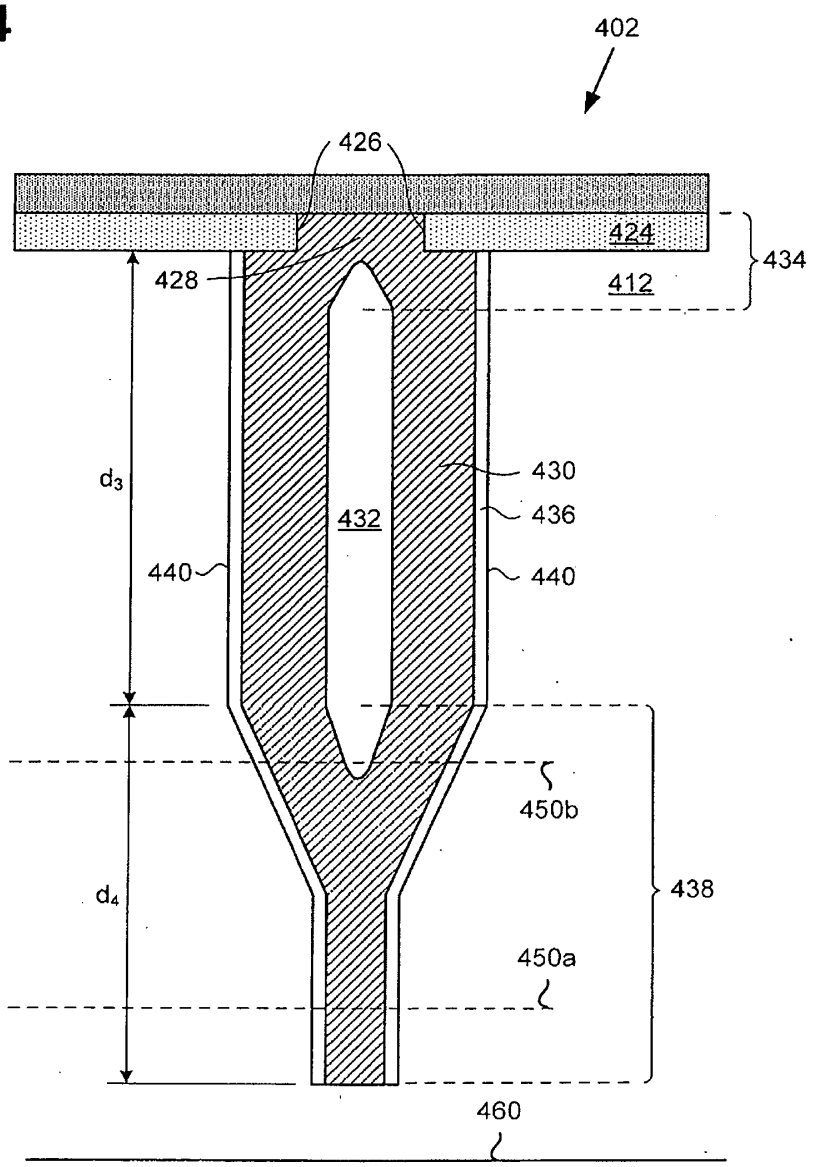


Fig. 1B (Prior Art)



REPLACEMENT SHEET

Fig. 4



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FACSIMILE TRANSMISSION COVER SHEET

Date: July 8, 2014

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-8300

Re: **Application Serial No.: 13/415,744**
Filing Date: 03/08/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 19

Message:

Enclosed please find the Amendment and Response to Non-Final Office Action dated April 8, 2014.

Also enclosed, please find Two (2) Drawing Replacement Sheets.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account 50-0731.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **07/08/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/KIM WATSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 04/08/2014

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EXAMINER	
BACHNER, ROBERT G	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
04/08/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 13/415,744	Applicant(s) JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/19/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10 and 13-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10 and 13-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *3/8/12* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicants' amendment filed 2/19/14 has been entered and considered. Applicants have elected Group I, claims 1-10 and 13-20, without traverse. Non-elected claims 11-12 are canceled.

Drawings

Figures 1A and 1B should be designated by a legend such as --Prior Art—because based on applicants' specification page 5, lines 1-5 and page 6 line 11- page7 line 5 only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p) (5) because they include the following reference character(s) not mentioned in the description: 422. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures

appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 14 and 17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA) citations referring to applicants' U.S. Application Publication No. 2013/0087893, in view of Beyne U.S. Provisional Patent Application No. 61/420,653 (copy attached), citations refer to U.S. Patent Application Publication No. 2012/0139127.

Regarding Claim 13.

AAPA discloses (AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said

semiconductor substrate comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (conductive fill shown as shaded area),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate; wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

In related art, Beyne discloses (10B-H)

each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface); wherein each of said plurality of through silicon vias (Fig. 10b) has a pinched off region (Pinch-off trench) at a top portion to prevent contamination during processing of said semiconductor substrate. (See Abstract, [0017], [0066]-[0068], [0078]. Beyne discloses that the pinch off trench top provides good TSV. the airgap and via is formed of good quality, and does not contain contamination. Thus, it would have been obvious to modify AAPA by including the pinch-off top portion to include the air-gap for the benefit of avoiding stress in the VIA and obtaining good quality TSV. Thus, the features of claim 13 would have been obvious to one having ordinary skill in the art.

Regarding Claim 14.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

Beyne disclose that the pinched off portion that is overhanging the trench forms the airgap. Beyne discloses that the pinch off may be formed by a dielectric. See Abstract,

The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias. (See Beyne Fig. 10b-h, and Abstract, [0017], [0070] [0078], [0093] [0094] and claim 1). Beyne discloses that the use dielectric layer can be used to form the pinch off, which creates the airgaps which reduces stress in the TSV. Thus, it would have been obvious to form a dielectric pinch off as taught by Beyne in the device of AAPA for the benefit of reducing stress in the TSV.

Regarding Claim 17. The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make

interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.

The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 17 would have been obvious to one having ordinary skill in the art.

Claims 1-7, 9, 10, 15, 16, 19 and 20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereafter: AAPA), in view of Beyne further in view of Dao (U.S. Patent Application No. 2011/0237073).

Regarding Claim 1.

(AAPA Figs. 1A and 1B and [0013]-[0014])

A semiconductor substrate (110) having a plurality of devices (108, [0002]), said semiconductor substrate (110) comprising: a plurality of through silicon vias (118, plurality: [0002] and [0014]) disposed in said substrate (118 disposed in 110) extending from a top surface (134) of said substrate (110) to a bottom surface (132) of said substrate (110); a conductive filler (conductive fill shown as shaded area) disposed within each of said plurality of through silicon vias (fill disposed in 118 figs. 1A & 1B),

AAPA does not disclose:

each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

In related art, Beyne discloses (Fig. 10B-H):

each of said plurality of through silicon vias (2c through S) having a hollow center (4) to reduce thermal stress in said semiconductor substrate (4 reduces thermal stress, [0070], disclosing that the airgaps help reduce stress in the substrate TSV interface). Beyne discloses that the airgaps help reduce stress in the TSV. Thus, it would have been obvious to modify AAPA to incorporate the airgap as taught by Beyne for the benefit of reducing the thermal stress in further processing of the device;

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Regarding Claim 2.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

Modified AAPA of claim 1 results in the features of claim 2. Namely,

The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 2 would have been obvious to one having ordinary skill in the art.

Regarding Claim 3.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate. Dao discloses that the taper at the bottom prevents contamination of the Via conductive fill during polishing. See [0017], [0025] [0028], See Figs 5-10. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 3 would have been obvious to one having ordinary skill in the art.

Regarding Claims 4 and 5

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S. 327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill for a TSV, With no unexpected results. Thus, the features of claims 4-5 would have been obvious.

Regarding Claim 6.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

In related art, Dao discloses:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center. (See Dao Fig. 9, disclosing that bottom

of Taper 16 is filled with 44.) Thus, modified AAPA would result in this feature, because the teaching of Beyne would include the pinched off hollow center, with the bottom filled as taught by Dao. Thus, the features of claim 6 would have been obvious to one having ordinary skill in the art.

Regarding Claim 7.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA discloses [0002], that semiconductor substrates have a plurality of TSV's in semiconductor substrates. AAPA discloses that the TSV's are used to make interconnections through semiconductors. AAPA discloses that the TSV's are used where needed to make interconnections through the semiconductors.

The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction. The recited feature would have resulted from an obvious matter of design choice. One having ordinary skill in the art would be motivated to make the vias as recited to accommodate a particular arrangement of contacts required by a die. See MPEP 2144.04 VI C. *In re Japikse,* 181 F.2d 1019, 86 USPQ 70 (CCPA1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); *In re Kuhle,* 526 F.2d 553, 188 USPQ 7 (CCPA

1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice). Thus, the broadly recited features recited in claim 7 would have been obvious to one having ordinary skill in the art.

Regarding Claim 9.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

Beyne discloses:

The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias. (See fig. 10b-H, pinch off trench, and Abstract and [0017] [0061] [0064]). Beyne discloses that the pinched off top portions creates air gap 4, which helps reduce stress in the substrate/via. Thus, it would have been obvious to provide a top pinch off for the benefit of obtaining the airgap 4 which reduces stress in AAPA.

Regarding Claim 10.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Modified AAPA results in this features, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled. See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA as done in regards to claim 1.

Regarding Claims 15 and 16.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

In related art, Dao discloses:

The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler. (Dao [0028], 44 comprising tungsten, copper)

The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten. (Dao [0028], 44 comprising tungsten, copper). The selection of a known

material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair &Carroll Co. v. Interchemical Corp.,* 325 U.S. 327,65 USPQ 297 (1945) See MPEP 2144.07. Here, the selection of metal, specifically tungsten would have been obvious because it is known to be used as a fill for a TSV, with no unexpected results. Thus, the features of claims 15-16 would have been obvious.

Regarding Claim 19.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

IN related art Dao discloses:

wherein each of said plurality of through silicon vias (fig. 10, 16) has a pinched off region at a bottom portion (taper ending at bottom) to prevent contamination during processing of said semiconductor substrate (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 18 would have been obvious to one having ordinary skill in the art.

Regarding Claim 20.

AAPA in view of Beyne disclose all of the features of claim 13 as addressed above.

AAPA does not specifically disclose:

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

AAPA does not disclose:

Dao discloses a taper bottom portion at (taper preventing contamination as described at [0017], [0021]. Dao discloses that the taper prevents contamination of the Via conductive fill. See [0017], [0025]. Thus, it would have been obvious to make the TSV of AAPA tapered as taught by Dao for the benefit of preventing contamination of the TSV in further processing as taught by Dao. Thus, the features of claim 1 would have been obvious to one having ordinary skill in the art.

Modified AAPA results in this feature, because Beyne discloses that the air gap is created by the top pinch off region and Dao discloses that the tip of the taper is filled. See Beyne fig 10b, and Dao Fig. 6 and 9. Dao's fill narrows the hollow center, by providing more fill material to close the airgap. Thus, the features recited are met by modified AAPA by applying the teachings of both Beyne and Dao to AAPA for the benefits of obtaining an airgap to prevent stress as taught by Beyne and tapering to avoid contamination as taught by Dao. Thus, the features of claim 20 would have been obvious to one having ordinary skill in the art.

Claims 8 and 18 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over AAPA) Beyne in view of Dao further in view of Ito (U.S. Patent Application No. 2008/0258307)

Regarding Claim 8 and 18.

AAPA in view of Beyne further in view of Dao disclose all of the features of claim 1 as addressed above.

AAPA does not disclose:

The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

In related art, Ito discloses:

The semiconductor substrate of claim 1/13, wherein each of said plurality of through silicon vias has at least one chamfered corner. (See Ito Figs. 2B, 3B, and [0051]) Ito discloses that the chamfered corners help avoid a stress concentration in the corners. Thus, it would have been obvious to chamfer the corners of the Vias of AAPA for the benefit of avoiding stress concentrations as taught by Ito.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BACHNER whose telephone number is

(571)270-3888. The examiner can normally be reached on Mon-Thurs 8:30-5 alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio J. Maldonado can be reached on 571-272-1864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROBERT BACHNER/
Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 13/415,744	Applicant(s)/Patent Under Reexamination JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0258307 A1	10-2008	Ito, Hiroyasu	257/771
*	B	US-7,795,134 B2	09-2010	Sulfridge, Marc	438/637
*	C	US-2011/0237073 A1	09-2011	Dao et al.	438/654
*	D	US-2012/0139127 A1	06-2012	Beyne, Eric	257/774
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Beyne, U.S. Provisional Patent Application Serial No. 61/420,653
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 9194

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/415,744	03/08/2012 RULE	257	2898	0150167

APPLICANTS

INVENTORS

Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 61/545,003 10/07/2011

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

03/20/2012

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ROBERT G BACHNER/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	4	20	3

ADDRESS

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691
UNITED STATES

TITLE

Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
1250	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/11/2013	04/02/2014							
	1	÷	✓							
	2	÷	✓							
	3	÷	✓							
	4	÷	✓							
	5	÷	✓							
	6	÷	✓							
	7	÷	✓							
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	10	÷	✓							
	11	÷	-							
	12	÷	-							
	13	÷	✓							
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	16	÷	✓							
	17	÷	✓							
	18	÷	✓							
	19	÷	✓							
	20	÷	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Searched as detailed in the attached EAST SEARCH REPORT.	4/2/2014	/RGB/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/ROBERT BACHNER/ Examiner.Art Unit 2898	

Method for forming isolation trenches with airgaps behind Through Silicon Via 3D-interconnect structures and devices obtained thereof

Field of the invention

[0001] The invention relates to the field of forming isolation trenches comprising airgaps and to the field of forming interconnect structures such as Through Silicon Vias (TSV) to be used in the stacking of semiconductor devices.

[0002] More particularly, the present invention relates to methods of forming airgaps in isolating structures whereby said structures are situated around a TSV interconnect structure in order to reduce the mechanical stress, the electric field and capacitance effects in the surrounding areas of the large TSV interconnect structure.

[0003] The invention further relates to devices thus obtained.

Background of the invention

[0004] With the continued scaling of IC technology, due to the large amount of electronic circuits on a small area, the density of chip input/output connection pads (I/O's) continues to increase. This leads to an increasing bandwidth of interconnects between integrated circuits (IC's) and/or other system elements. For short interconnects, electrical signal lines maintain the highest capacity and speed. In order to keep up with the increasing speed and density requirements, system in a package (SIP) technology is increasingly used. This creates the need for 3-dimensional interconnects.

[0005] 3D integration requires the realization of electrical interconnections that go through the bulk of the substrate (wafer) on (or into) which the active devices are realized. These are the so-called Through-Si-Via (TSV) connections. One particular approach to realizing TSV connections is the so-called via-middle approach, where the

TSV is realized after the fabrication of the active devices (the front-end-of-line, FEOL), just before the integration of the multilayer chip interconnect stack (the back-end-of-line, BEOL). The electrically conductive material of the TSV is typically copper or tungsten metal.

[0006] However in the state of the art there are still key issues which need to be resolved in order to integrate these TSV in a reliable way with good device performances:

- The use of a metallic connection through the Si substrate results in large mechanical stress levels in the Si, causing mobility variations in the Si resulting in performance degradation of neighboring devices.
- The presence of a relatively large metallic structure through the bulk of the substrate causes a relatively large electrical capacitance that degrades circuit performance.
- Electrostatic field due to TSV potential and charging current of the TSV-substrate capacitor during transient operation may affect the device performance of neighboring devices

Detailed description of illustrative embodiments

[0007] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

[0008] Moreover, the term top and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the preferred embodiments described herein are capable of operation in other orientations than described or illustrated herein.

[0009] It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0010] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0011] Similarly it should be appreciated that in the description of exemplary preferred embodiments, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

[0012] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0013] In the description provided herein, numerous specific details are set forth. However, it is understood that preferred embodiments may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0014] The invention will now be described by a detailed description of several preferred embodiments. It is clear that other preferred embodiments can be configured according to the knowledge of persons skilled in the art without departing from the true spirit or technical teaching of the invention as defined by the appended claims.

[0015] It is an object of embodiments of the present invention to provide Through Substrate Via (TSV) interconnects, such as Through Silicon Via interconnects for use in 3D stacked semiconductor devices, thereby reducing the negative impact of these 3D-TSV towards neighboring devices. It is therefore a goal to provide isolating trenches around said TSV interconnect structures, said trenches comprising airgaps.

[0016] It is a further goal to provide a method for manufacturing said 3D-TSV semiconductor devices making use of existing processing technology.

[0017] The present invention significantly reduces the negative impact caused by the relative large 3D-TSV interconnect structures. Said negative impact may be mechanical stress created in the substrate around said 3D-TSV structure thereby causing mobility variations in the surrounding substrate and hence resulting in performance degradation of neighboring devices. Said negative impact may be caused by inducing a relatively large electrical capacitance that degrades neighboring circuit performance. Furthermore said negative impact caused by the large 3D-TSV

structures may be due to the creation of an electrostatic field and potential within the 3D-TSV thereby creating a charging current in the surrounding substrate which may during transient operation affect the device performance of neighboring devices.

[0018] The present invention solves the above mentioned problems by forming isolating trenches with airgaps during the processing of said 3D-TSV interconnect structure. It is the aim of the invention to provide said isolating trenches without adding additional processing steps and making use of processing steps required to fabricate the 3D-TSV.

[0019] The above objective is accomplished by a method and device according to the present invention.

[0020] The present invention relates to a semiconductor device and a method for making said device, the semiconductor device comprising at least one 3D-TSV interconnect and isolating trench-like structure, said isolating trench-like structure comprising at least one airgap. Said 3D-TSV interconnect is preferably a pillar made of conductive material which can be connected to the interconnect structures of for example another semiconductor substrate or another semiconductor device and/or another level of interconnect structures within the same semiconductor device.

[0021] The method of the present invention for making the 3D-TSV interconnect is based on the so-called "via-middle" approach, wherein the TSV is realized after the fabrication of the active devices (the front-end-of-line, FEOL), just before the integration of the multilayer chip interconnect stack (the back-end-of-line, BEOL). The electrically conductive material of the TSV is typically copper or tungsten metal.

[0022] According to a first aspect of the invention, a substrate, preferably a semiconductor substrate comprising semiconductor active devices, is disclosed which comprises at least an interconnect Through Substrate (Si) Via (TSV) structure which is surrounded by at least one isolating trench-like structure comprising an airgap. Said interconnect structure is preferably a 3D-TSV in the form of a conductive pillar. Said at least one isolating trench-like structure comprises at least an airgap and a sealing which pinches off the airgap.

[0023] Figure 1 illustrates side views of a state of a state of the art semiconductor substrate having 3D-TSV interconnects **10**, said 3D-TSV having a depth in the substrate **S** of around 50 µm and a diameter around 5 µm (Figure 1A). Figure 1B illustrates a 3D-TSV **10** having a diameter of around 2 µm thereby responding to further device scaling requirements. Both TSV structures **10** have a liner **2b** deposited onto the inner sidewalls of TSV, said liner **2b** having a width of around 200nm in said TSV **10**.

[0024] Figure 2 illustrates side views of a semiconductor substrate **S** having a 3D-TSV **10** having a depth in the substrate **S** of around 50 µm and a diameter (width) around 2 µm and further comprising isolating trench-like structures **3** having at least one airgap **4**. A liner **2a** is deposited onto the substrate **S** and on the inner sidewalls **2b** of TSV, said liner **2b** having a thickness of around 200nm on the inner sidewalls of said TSV. Said liner further pinches of the isolating trench-like structures **3** thereby creating an airgap **4** in said trench-like structures. Figure 2A illustrates a side view and Figure 2B illustrates a more detailed side view combined with a top view. Figure 2A further illustrates the portion of the (backside) substrate **S2** to be removed in order to open the TSV **10** structure when the device is finalized.

[0025] According to preferred embodiments of the invention said at least one isolating trench-like structure is etched at the same time (simultaneous) as the interconnect TSV structure and hence requiring no additional processing. Due to aspect-ratio-dependent etching it is possible to etch the isolating trench-like structure having a diameter in the order of 200-500nm at the same time of the interconnect TSV structure having a diameter in the order of 2-10µm. In general, the isolating trench-like structure has a depth which is around 1/5 to 2/3 the via depth. A state of the art anisotropic Bosch etch process may be used to perform said simultaneous etching.

[0026] According to embodiments of the invention the airgap in said at least one isolating trench-like structure is formed through depositing a liner onto the substrate whereby said liner pinches off the trench-like structure, thereby forming at least one airgap in said trench-like structure. The pinch-off is preferably realized during the

deposition of a liner within the TSV structure and hence requiring almost no additional processing. A liner deposition within the TSV structure is preferred to realize a smoothening of the sidewalls (to reduce the scalloped surface) after etching the TSV structure.

[0027] According to embodiments of the invention the liner material used to smoothen the sidewalls of the TSV structure and at the same time pinching off the airgap in the trench like structure is made of a liner material selected from an oxide and/or nitride and/or polymer such as CVD oxide, CVD nitride, SA-CVD TEOS oxide, plasma enhanced CVD oxide. Figure 8 is a SEM picture illustrating the TSV interconnect structure **10** filled with copper and having a SA-CVD deposited TEOS liner **2b**. The TEOS liner is clearly smoothening the scalloped surface of the inner sidewalls of the TSV **10**.

[0028] According to embodiments of the invention the isolating trench-like structure is narrow such that during TSV liner deposition (typically oxide or nitride) forms an airgap in the trench due to the pinch-off of the liner deposited on the field area. To realize the pinch-off, the at least one trench-like structure typically has a diameter (width) smaller than 2 times the average thickness of the deposited liner on the Si-sidewall near the top of the via (which is typically 40% less than the thickness of the deposited liner on the field area). This means that for a deposited liner on the TSV sidewall having a thickness of e.g. 200nm, the average diameter of the trench-like structure has to be smaller than 400nm. The at least one trench-like structure typically has a diameter around 200-500 nm and a liner deposition of e.g. 200 to 300 nm thickness on the TSV sidewalls is sufficient to pinch-off the trench surrounding the TSV.

[0029] According to embodiments of the invention the isolating trench-like structure may have any closed form shape, such as a polygon, circle or oval, with the TSV structure situated within said closed form trench separated by a minimum amount of substrate material. Mechanical stresses in the substrate material that are caused by the different materials used inside the TSV will be concentrated in this narrow silicon ring-like structure around the TSV structure. The diameter of which has to be

optimized in order to minimize and to avoid loss in TSV density over the whole device substrate. The separation between the outside of the TSV and inner dimension of the air-gap trench surrounding the TSV is in the range of 1μm to one or two times the TSV diameter.

[0030] High mechanical stress in the substrate surrounding the TSV may result in mobility changes in the channels of surrounding (MOSFET) devices thereby causing cracks in the substrate between closely spaced TSV's which may be avoided be concentrating and capturing the stress in said substrate material (ring) in between the isolating trench-like structure and the TSV. An isolating trench-like structure comprising an airgap thereby significantly helps to isolate the stress. Furthermore high mechanical stress in TSV (copper) may cause TSV (Cu)-"pumping" and thereby cause damage to the low-k dielectric in the BEOL. Figure 4 illustrates the stress concentration in the (Si) substrate surrounding the TSV as a function of the diameter of the substrate (Si) ring in between the isolating trenches and the TSV. Figure 5 illustrates a first order analytical model illustrating the stress in the substrate (Si) ring around the TSV due to stress in TSV for different TSV diameters and diameter of the Si ring between the TSV and the air-gap.

[0031] According to embodiments of the invention the TSV structure has a diameter/width between 1 and 30 μm. According to particular embodiments said TSV has an average diameter/width in the range 2 μm up to 5 μm, more particular said TSV has an average diameter of around 2 μm.

[0032] According to embodiments of the invention the depth of the trench-like structure is significantly less than the depth of the TSV structure, the depth of the trench-like structure may be only 5 to 10 μm.

[0033] According to embodiments of the invention the TSV structure has a depth around 50 μm in the substrate, which results after thinning the substrate in order to expose the conductive part of the TSV in a depth of around 47 μm.

[0034] According to preferred embodiments of the invention said TSV structure is made of a material selected from copper (Cu), aluminum (Al), tungsten (W) or any other metals used in the field. The conductive material can also be an alloy, an

implanted semiconductor, conductive silicon, conducting polymers. Alternatively a metal paste, e.g. Cu paste, can be applied. Also combinations of above mentioned materials can be used. The step of depositing a conductive material possibly creates an interconnect with an external contact. This step can comprise various sub-steps. Extra layers underlying the conductive material or intermediate layers can be used. This can be for example improve the filling of the holes, improve adhesion of the conductive material, further reduce the stress within the TSV, prevent inter-diffusion of materials,...

[0035] In particular embodiments of the present invention, the TSV structure may be made of conductive material, and further comprises a barrier layer and/or a seed layer which is deposited before filling the TSV structure with conductive material e.g. by electroplating. Said seed layer may cover the whole surface of the side walls and bottom wall of the TSV structure. Said barrier layer is preferably made of a material selected from Ta, Ti, TaN, TiN, RuTa, Mn and combinations thereof and is deposited by state of the art deposition techniques such as PVD and CVD and combinations thereof. A seed layer is preferably made of a material selected from Cu, Ni, Co, W, Mn and may be applied for instance by Chemical Vapor Deposition (CVD), Physical Vapor Deposition (sputtering) (PVD), Atomic Layer Deposition (ALD), Electro Chemical Deposition (ECD), as well as by any other method known in the art.

[0036] It is also possible that more than one electrical interconnect TSV structure (conductive pillar) is formed within a single surrounding trench-like structure. This means that parallel TSV are formed within the same trench-like (ring) structure.

[0037] According to a second aspect of the invention a method for the fabrication of at least one Through Substrate Via (TSV) interconnect with surrounding isolating trench like structure is disclosed, whereby said trench-like structures comprise at least one airgap to further improve its insulating properties. Said method is characterized and differentiated towards state of the art methods in the fact that the isolating trench-like structures are fabricated at the same time as the fabrication of the TSV holes thereby reducing the number of processing steps significantly. The method is further differentiated by the formation of airgaps in said isolating trench-

like structures. No process steps are added to the process flow to create and seal the airgap trenches. No additional masks are required.

[0038] Figures 10A-10F illustrate different processing steps according to embodiments of the invention to fabricate a Through Silicon Via (TSV) interconnect based on the via middle approach whereby said TSV interconnects are surrounded by isolating trenches with airgaps.

[0039] According to embodiments, the method of the invention to provide TSV interconnect structures surrounded by isolating trench-like structures, said trench-like structures having at least one airgap comprises at least the steps of:

- providing a substrate having a first main surface and then,
- producing at the same time (simultaneous) at least one a TSV hole having a diameter in the order of 2 μm up to 20μm and a trench-like structure having a diameter (width) smaller than 1000nm surrounding said TSV hole and separated by remaining substrate material, and then
- depositing a dielectric liner in order to smoothen the sidewalls of the etched TSV hole and to pinch-off the opening of the trench-like structure at the first main surface of the substrate in order to create at least one airgap in said trench-like structure, and then
- depositing a conductive material in said TSV hole in order to create a TSV interconnect.

[0040] According to embodiments, the substrate is a silicon wafer having active devices on its first main surface material, said active device being produced during the preceding FEOL processing. After completion of the TSV interconnect BEOL processing is performed in order to create BEOL interconnects

[0041] According to embodiments the step of producing at the same time (simultaneous) at least one a TSV hole and a trench-like structure is performed using an aspect-ratio-dependent etching such that it is possible to etch the isolating trench-like structure having a diameter (width) in the order of 100-500nm at the same time of the TSV hole having a diameter (width) in the order of 2-20μm. In general, the isolating trench-like structure has a depth which is around 1/5 to 2/3 the via depth. A

state of the art anisotropic Bosch etch process may be used to perform said simultaneous etching.

[0042] Figure 3 illustrates the aspect-ratio-dependent- etch-rate effect (ARDE), the Figure illustrates the etched trench depth as a function of the trench diameter (width) when simultaneously a 50 µm deep TSV hole having a diameter (width) of around 5 µm for a typical Bosch type etch process (tool dependent).

[0043] Figure 9 and Figure 10A illustrate a detailed view of the substrate **S** with a photoresist **12**, PMD and STI layer(s) **11** after patterning in order to define the TSV hole (to be etched) and the isolating trenches or ring (to be etched).

[0044] According to embodiments the trench-like structure is a trench-like ring structure having a diameter (width) below 100-500nm. The outer diameter of the trench-like ring structure may be in the order of 10-15 µm, for example 10.4-10.8 µm. The inner diameter of the trench-like ring structure may be in the order of 10 µm.

[0045] According to embodiments the TSV hole is having a diameter (width) in the order of 2 µm up to 20µm. The TSV hole (interconnect structure) may have a diameter (width) smaller than 10 µm, or smaller than 7 µm, or smaller than 6 µm or below 5 µm or below 4µm. According to particular embodiments said TSV hole may have an average diameter (width) in the range 2 µm up to 5 µm, more particular said TSV hole has an average diameter (width) of around 2 µm.

[0046] According to embodiments the distance between the TSV and the trench-like structure comprising an airgap is such that it allows for a sufficiently low stress layer in this Si sidewall (Stress is more concentrated when using an airgap), typically this will be a diameter (width) between 1 µm and 1 or 2 times the via diameter, most typically around half of the via diameter.

[0047] According to embodiments the step of providing TSV holes (interconnect structures) in said first main surface of the substrate may be performed using an etch process which is optimized to obtain undercut free etch with limited scallops on the sidewalls during etching. This may be a pulsed etching technique comprising alternating steps of isotropic etching and passivation (Bosch process). Said alternating etching – passivation process is preferably using an SF_6 based plasma

etching step alternated with a C_4F_8 based plasma passivation step, optionally further comprising oxygen and/or inert gases in either or both steps. Figure 6 illustrates the TSV hole **1** with an undercut **20** after performing a standard deep via etch process (Figure 6A) and after applying an optimized deep via etch process to obtain undercut free etch with limited scallops (Figure 6B).

[0048] Figure 10B illustrates a detailed view of the substrate **S** with a patterned photoresist **12**, PMD and STI layer(s) **11** and a liner **2a** deposited in the TSV hole and isolating trenches. The liner is deposited on the horizontal parts of the substrate **2a** and onto the sidewalls of the TSV hole **2b** and within the isolating trenches **2c**. Figure 10B clearly illustrates the closure of the opening (top) of the isolating trenches **3** thereby pinching-off the trench and forming an airgap **4** within said trench.

[0049] According to embodiments the thickness of the deposited liner is such that it pinches off the trench-like (ring) structure at the surface of the substrate such that an airgap is created in the center of said structure. The thickness of the liner is much thicker on the horizontal parts compared to the thickness on the vertical parts (sidewalls of the TSV hole). This is illustrated in Figure 7A which shows the thickness of a TEOS liner using a SA-CVD O3-TEOS process (at 400°C) on a substrate (300mm wafer) having TSV of 5µm diameter (width) and having an aspect ratio 1:1, 3:1 and 5:1. Figure 7B illustrates a SEM picture of the bottom and sidewall of a TSV **1** having an aspect ratio 10:1. For a 200 nm thick liner on the bottom sidewall **2b**, a 500nm thick layer **2a** is deposited on the top surface of the substrate (wafer).

[0050] According to embodiments the step of depositing a conductive material in said TSV hole in order to create a TSV interconnect structure is such that said TSV hole is at least partly filled with a conductive material thereby creating an electrical interconnect structure suitable for forming an electrical path from the bottom surface of the hole up until the surface of the substrate. Figure 10C illustrates the deposition of barrier material and conductive material **21** onto the substrate **S** thereby filling the TSV hole with conductive material in order to create a TSV interconnect **10**.

[0051] According to preferred embodiments of the invention the step of at least partly filling the TSV hole with a conductive material is performed using

electrochemical deposition (ECD) techniques or alternatively Chemical Vapor deposition (CVD). Said conductive material may be a metal such as Copper (Cu), Nickel (Ni), tungsten (W) or any other metals and/or alloy of metals. Also alternative conductive materials may be used such as an implanted semiconductor, conductive silicon, conducting polymers, carbon nanotubes. Alternatively a metal paste consisting of metallic particles and organic binders, e.g. Ag paste, can be applied. Alternatively Carbon nano tubes (CNT) and combination of CNT and Cu can be applied.

[0052] Figure 10D illustrates the step of performing a planarization of the conductive material in order to remove the overburden of conductive material **20** on the horizontal parts. Said planarization may be performed using Chemical Mechanical Planarization (CMP). A residual part of conductive material may be left above the isolating trenches

[0053] After performing the TSV processing steps the device may then be further finalized by providing metal contacts onto said TSV interconnect and furthermore several BEOL interconnect layers. Figure 10E indicates the metal contacts and dielectric layer surrounding said metal contact. Figure 10F illustrates further BEOL layers for the first (M1) and second metal (M2) layers in combination with Dielectric layers.

[0054] Figure 10G illustrates the passivation step after finalizing the BEOL processing.

[0055] Finally the substrate may be thinned on the backside in order to open the TSV interconnects from the backside of the substrate in order to make a 3D stacking possible. Said TSV interconnect structure may therefore be further provided with a solder ball or bump. Thinning of the substrate may be performed down to a substrate thickness of 50µm-100µm. The thinning may be performed by for instance mechanical operations such as grinding or other state of the art techniques. According to alternative embodiments of the present invention, the thinning may comprise chemically thinning, e.g. by dry etching or plasma etching the substrate (1) from the backside, the thinning being halted when the interconnect structure (5) is reached. The chemical thinning, e.g. plasma etching, may not stop at the level where

the conductive structure **10** is reached, but may continue above that level (thus slightly over etching the substrate **S** e.g. silicon wafer). The interconnect structure (the conducting material 10 or the combined conductive material and dielectric will then stick out of the etched-back surface, which is advantageous for the addition of a solder volume such as a solder ball or bump. A solder volume as for instance a solder ball or solder bump can further be applied to the conductive structure on the second surface.

[0056] According to preferred embodiments of the invention the circumferential (hoop-)stress or in other words the stress originating from the TSV interconnect structure towards the substrate behind said TSV structure is dependent on the diameter of the TSV interconnect structure and the width of the remaining substrate (W_{Si}) in between the TSV interconnect structure and the isolating trench-like structure. Figure 11A illustrates a 3D-TSV with a diameter $Ø_{Cu}$ having isolating trench-like structures having at least one airgap and remaining (Si) substrate (Si ring) having a width W_{Si} in between the isolating trench-like structure (ring) and the TSV structure according to embodiments of the invention. Figure 11B illustrates the circumferential (hoop-)stress as a function of the width of the remaining substrate (W_{Si}) as a function of the diameter of the Cu TSV ($Ø_{Cu}$).

[0057] While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive. The invention is not limited to the disclosed embodiments.

[0058] Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a

combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

[0059] The foregoing description details certain embodiments of the invention. It will be appreciated, however, that no matter how detailed the foregoing appears in text, the invention may be practiced in many ways, and is therefore not limited to the embodiments disclosed. It should be noted that the use of particular terminology when describing certain features or aspects of the invention should not be taken to imply that the terminology is being re-defined herein to be restricted to include any specific characteristics of the features or aspects of the invention with which that terminology is associated.

Brief description of the drawings

[0060] Figure 1 illustrates side views of a state of a state of the art semiconductor substrate having 3D-TSV interconnects, said 3D-TSV having a depth in the substrate of around 50 µm and a diameter (width) around 5 µm (Figure 1A). Figure 1B illustrates a 3D-TSV having a diameter (width) of around 2 µm thereby responding to further device scaling requirements. Both TSV structures have a liner deposited onto the inner sidewalls of TSV, said liner having a width of around 200nm in said TSV.

[0061] Figure 2 illustrates side views of a semiconductor substrate having a 3D-TSV according to Figure 1 and further comprising isolating trench-like structures having at least one airgap according to embodiments of the invention. Figure 2A illustrates a side view and Figure 2B illustrates a more detailed side view combined with a top view.

[0062] Figure 3 illustrates the trench depth in function of the trench diameter (width) when performing the Bosch etch process in order to etch simultaneously a 50µm deep and 5 µm wide TSV according to embodiments of the invention. The Figure illustrates the aspect-ratio-dependent- etch-rate effect (ARDE).

[0063] Figure 4 illustrates the stress in the (Si) substrate surrounding the TSV, relative to the stress in the TSV, as a function of the diameter (width) of the substrate (Si) ring in between the isolating trenches and the TSV.

[0064] Figure 5 illustrates a first order analytical model illustrating the stress in the substrate (Si) ring around the TSV due to stress in TSV.

[0065] Figure 6 illustrates the TSV after performing a standard deep via etch process (Figure 6A) and after applying an optimized deep via etch process to obtain undercut free etch with limited scallops (Figure 6B).

[0066] Figure 7A illustrates the thickness of a TEOS liner using a SA-CVD O3-TEOS process (at 400°C) on a substrate (300mm wafer) having TSV of 5µm diameter (width) and having an aspect ratio 1:1, 3:1 and 5:1. Figure 7B illustrates a SEM picture of the bottom and sidewall of a TSV having an aspect ratio 10:1. For a 200 nm thick liner on the bottom sidewall, a 500nm thick layer is deposited on the top surface of the substrate (wafer).

[0067] Figure 8 is a SEM picture illustrating the TSV interconnect structure filled with copper and having a SA-CVD deposited TEOS liner according to embodiments of the invention. The TEOS liner clearly smoothening the scalloped surface of the inner sidewalls of the TSV hole.

[0068] Figure 9 illustrates a detailled view of the substrate with a photoresist , PMD and STI layer after patterning in order to define the TSV hole (to be etched) and the isolating trenches or ring (to be etched) according to embodiments of the invention.

[0069] Figures 10A-10F illustrate different processing steps according to embodiments of the invention to fabricate a Through Silicon Via (TSV) interconnect based on the via middle approach whereby said TSV interconnects are surrounded by isolating trenches with airgaps.

[0070] Figure 11A illustrates a 3D-TSV with a diameter $Ø_{Cu}$ having isolating trench-like structures having at least one airgap and remaining (Si) substrate (Si ring) having a width W_{Si} in between the isolating trench-like structure (ring) and the TSV structure according to embodiments of the invention. Figure 11B illustrates the circumferential (hoop-)stress as a function of the width of the remaining substrate (W_{Si}) as a function of the diameter of the Cu TSV ($Ø_{Cu}$).

[0071] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0072] Any reference signs in the claims shall not be construed as limiting the scope. In the different drawings, the same reference signs refer to the same or analogous elements.

Definitions

[0073] Where reference is made in embodiments of the present invention to isolating "trench-like structure" this may refer to a structure with any geometrical shape having a specific diameter (width) W_G that is surrounding a TSV structure. Examples of suitable shapes for the trench-like structure are a circular ring, polygonal rings or square rings,.... In between said "trench-like structure" and the TSV structure there is substrate material. In embodiments the isolating trench-like structure is separated from the TSV by remaining substrate (e.g. Si) material having at least a critical diameter (width) W_G, which is in the order of one μm up to 2 times the via diameter, with ½ the via diameter more optimal.

[0074] Where in embodiments of the present invention reference is made to a pulsed etching it refers to a process in which an etching step is alternated with a deposition step and this is repeated to achieve nearly vertical structures. It is also referred to as the "The Bosch process". The plasma contains some ions, which attack the wafer from a nearly vertical direction. For silicon, this pulsed etching preferably uses sulfur hexafluoride source gas [SF_6], while for the deposition of a chemically inert passivation layer, preferably a C_4F_8 source gas is used and each pulsed phase preferably lasts for several seconds. The passivation layer protects the entire substrate from further chemical attack and prevents further (lateral) etching. However, during the etching phase, the directional ions that bombard the substrate attack the passivation layer at the bottom of the trench (but not along the sides. The etch/deposition steps are repeated many times over resulting in a large number of very small isotropic etch steps taking place only at the bottom of the etched pits. To

etch through a 0.5 mm silicon wafer, for example, 100–1000 etch/deposit steps are needed. Typically this etching process results in sidewalls having a scalloped surface.

Claims

1. A method for providing at least one TSV interconnect structure surrounded by at least one isolating trench-like structure, said trench-like structure having at least one airgap and said method comprising at least the steps of:
   - providing a substrate having a first main surface, and then
   - producing simultaneous at least one a TSV hole having a diameter (width) in the order of 2 µm up to 20µm and a trench-like structure having a diameter (width) smaller than 1000nm surrounding said TSV hole and separated by remaining substrate material, and then
   - depositing a dielectric liner in order to smoothen the sidewalls of the etched TSV hole and to pinch-off the opening of the trench-like structure at the first main surface of the substrate in order to create at least one airgap in said trench-like structure, and then
   - depositing a conductive material in said TSV hole in order to create a TSV interconnect.
2. A method according to claim 1 wherein the substrate is a silicon wafer having active devices on its first main surface material, said active device being produced during a preceding FEOL processing.
3. A method according to claim 1 or 2 wherein the step of producing simultaneous at least one TSV hole and a trench-like structure is performed using an aspect-ratio-dependent etching such that the isolating trench-like structure has a diameter (width) of 100-500nm and the TSV hole has a diameter (width) of 2-20µm and the isolating trench-like structure has a depth around 1/5 to 2/3 the via depth.
4. A method according to foregoing claims wherein the aspect-ratio-dependent etching is a pulsed etching comprising alternating steps of isotropic etching and passivation such as an SF_6 based plasma etching step alternated with a C_4F_8 based plasma passivation step, optionally further comprising oxygen and/or inert gases in either or both steps.

5. A method according to foregoing claims wherein the deposited liner is a TEOS liner deposited using a process such as a SA-CVD.
6. A method according to foregoing claims wherein the step of depositing a conductive material in said TSV hole in order to create a TSV interconnect structure is performed using electrochemical deposition (ECD) techniques or Chemical Vapor deposition (CVD) and wherein the conductive material is selected from a metal such as Copper (Cu), Nickel (Ni), tungsten (W) or any other metals and/or alloy of metals or selected from alternative conductive materials such as an implanted semiconductor, conductive silicon, conducting polymers, carbon nanotubes.
7. A method according to foregoing claims further comprising after the step of creating a TSV interconnect a planarization step such as Chemical Mechanical Planarization (CMP) of the conductive material in order to remove the overburden of conductive material on the horizontal parts of the substrate.
8. A method according to foregoing claims further comprising after the step of creating a TSV interconnect a thermal anneal step in order to initiate grain growth of the metal.
9. A method according to foregoing claims further comprising after the step of creating a TSV interconnect the step of providing metal contacts onto said TSV interconnect and furthermore several BEOL interconnect layers.
10. Use of a method according to foregoing claims for the 3D stacking of semiconductor substrates and further comprising the step thinning the backside of the substrate using mechanical operations such as grinding and/or chemical thinning in order to open the TSV interconnects from the backside and to make a 3D stacking possible.
11. Use according to claim 10 wherein said TSV interconnect structure is further provided with a solder ball or bump.
12. A substrate comprising at least one interconnect Through Substrate (Si) Via (TSV) structure which is surrounded by at least one isolating trench-like structure

comprising an airgap fabricated using the method according to any of claims 1 to 9 and wherein said interconnect TSV structure is a 3D-TSV.

Abstract

Method for forming isolation trenches with airgaps behind Through Silicon Via 3D-interconnect structures and devices obtained thereof

A method is disclosed for providing at least one TSV interconnect structure surrounded by at least one isolating trench-like structure, said trench-like structure having at least one airgap. Said method comprising at least the steps of:

- providing a substrate having a first main surface, and then
- producing simultaneous at least one a TSV hole having a diameter (width) in the order of 2 μm up to 20μm and a trench-like structure having a diameter (width) smaller than 1000nm surrounding said TSV hole and separated by remaining substrate material, and then
- depositing a dielectric liner in order to smoothen the sidewalls of the etched TSV hole and to pinch-off the opening of the trench-like structure at the first main surface of the substrate in order to create at least one airgap in said trench-like structure, and then
- depositing a conductive material in said TSV hole in order to create a TSV interconnect.

Figure 1

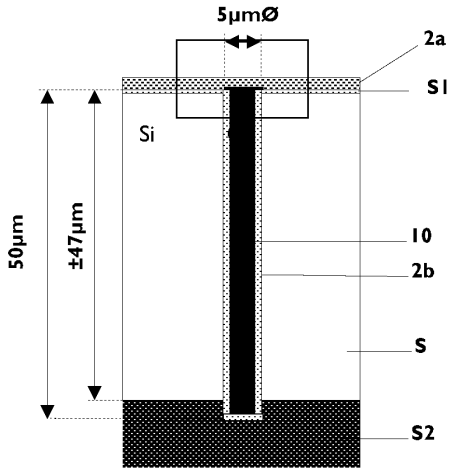


Figure 1A

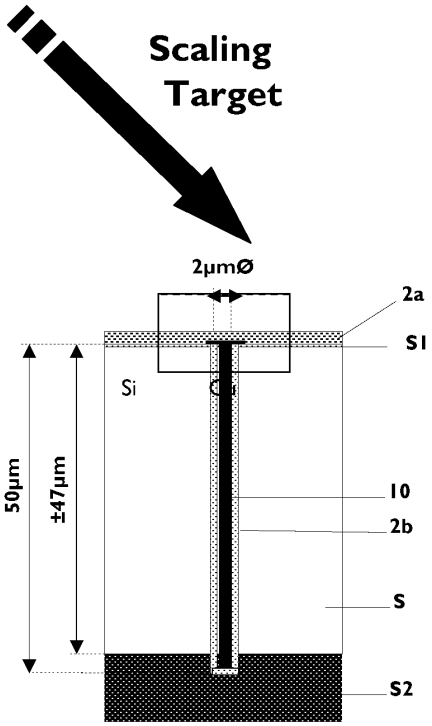


Figure 1B

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Figure 2

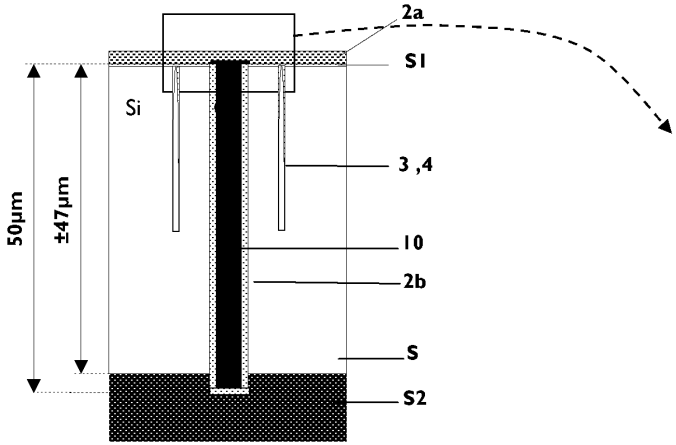


Figure 2A

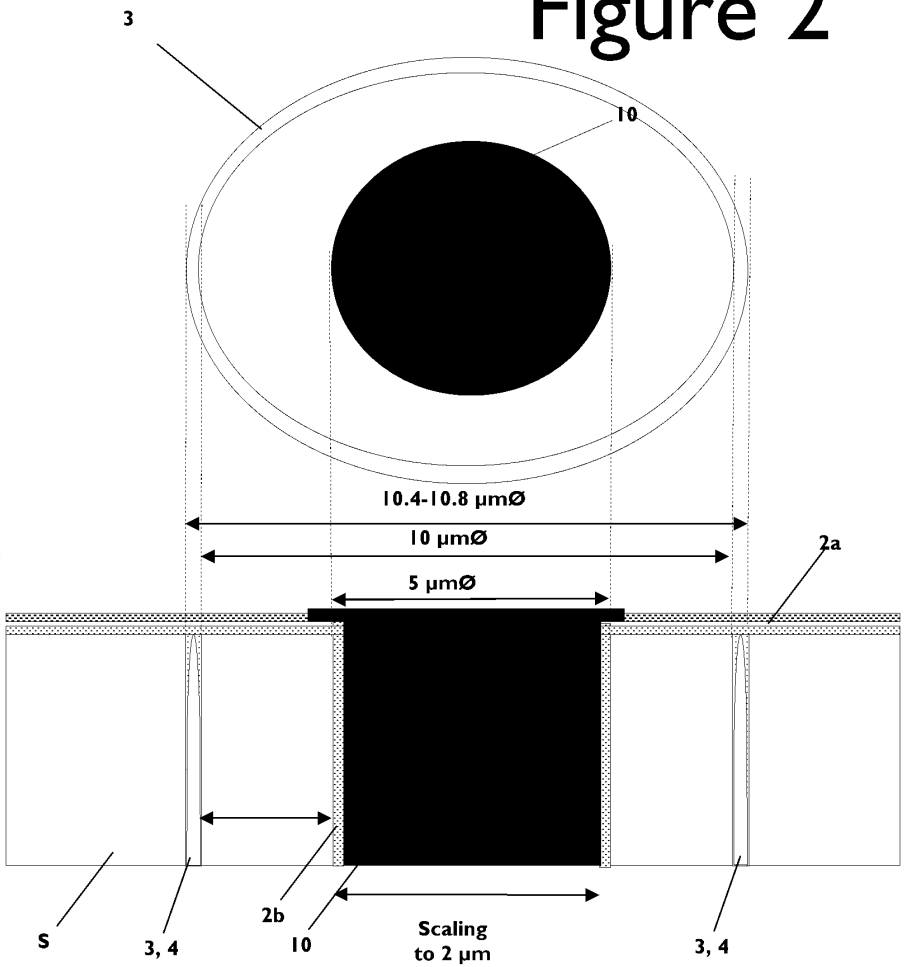


Figure 2B

Figure 3

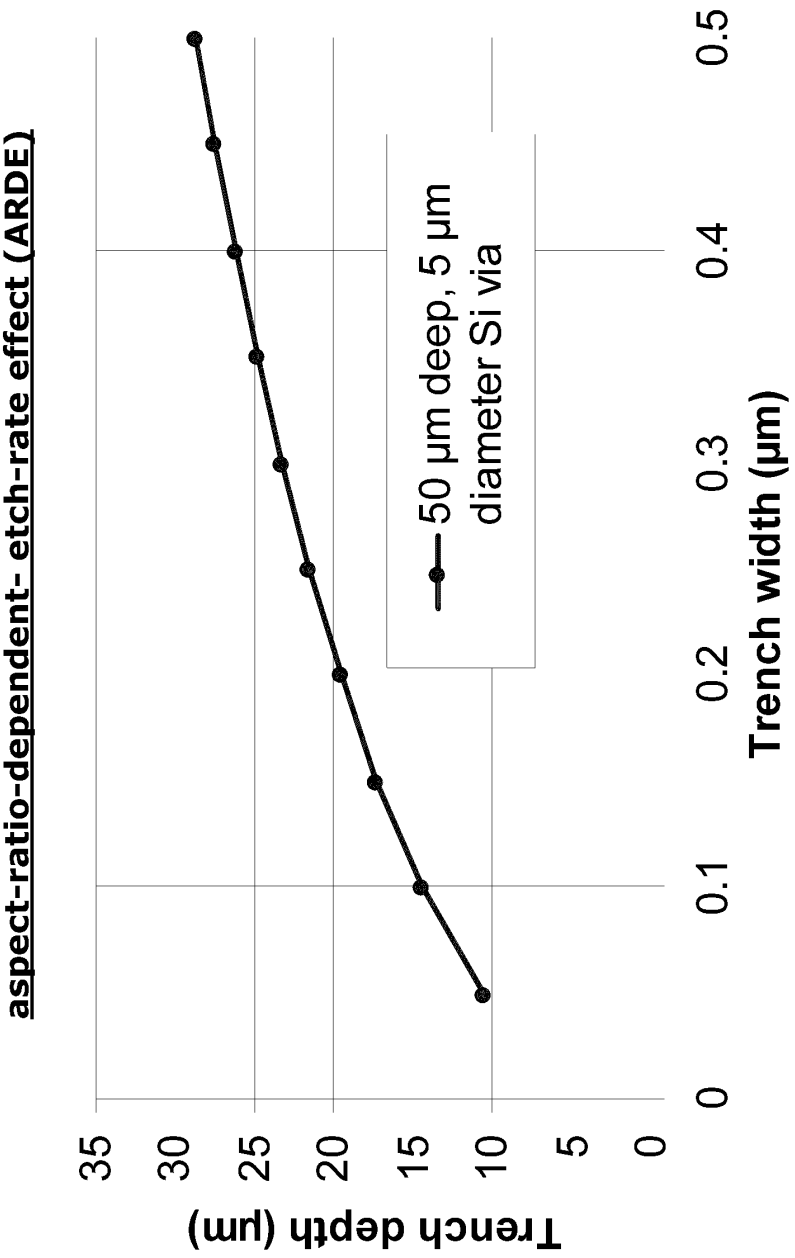

aspect-ratio-dependent- etch-rate effect (ARDE)
Trench depth (μm)
0
5
10
15
20
25
30
35
0
0.1
0.2
0.3
0.4
0.5
Trench width (μm)
50 μm deep, 5 μm diameter Si via

Figure 4

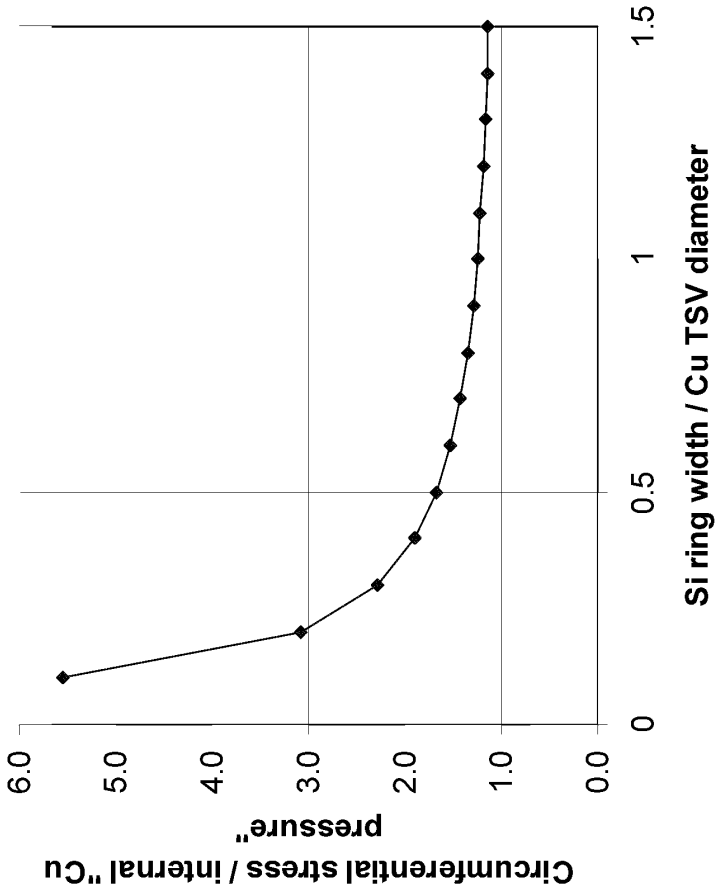

Circumferential stress / internal "Cu pressure"
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0
0.5
1
1.5
Si ring width / Cu TSV diameter

Figure 5

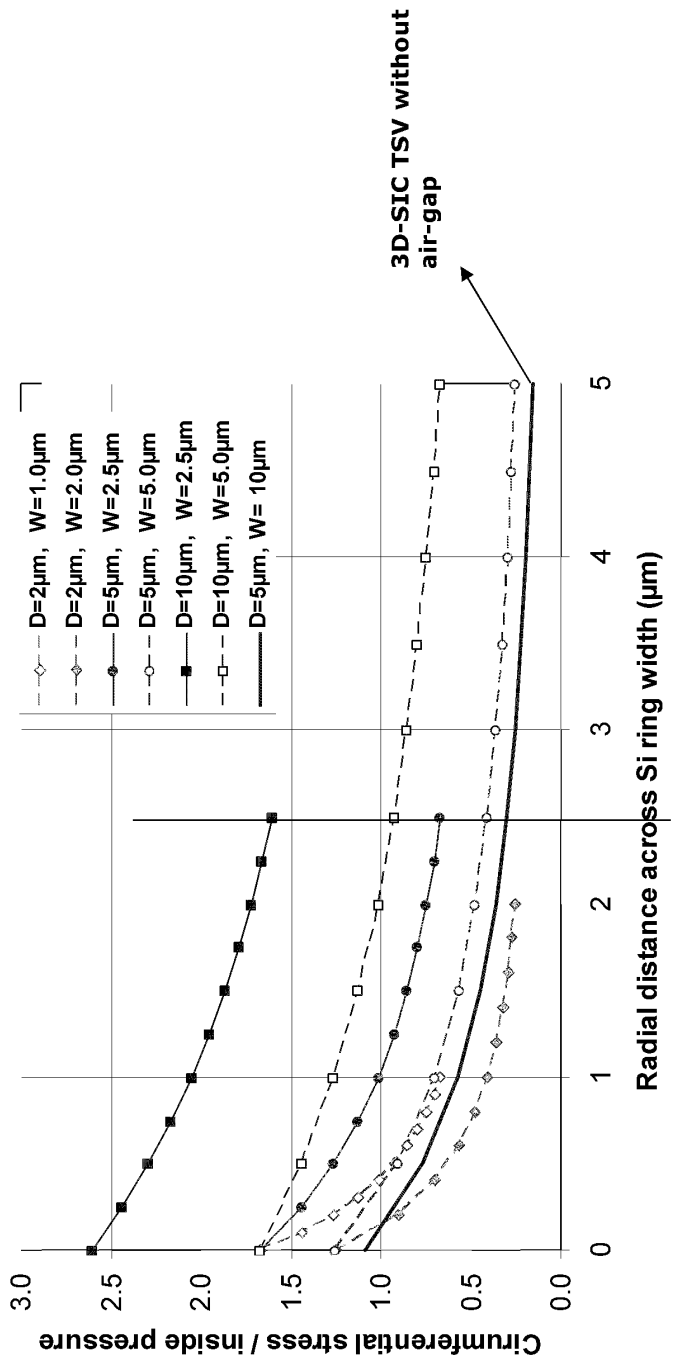

Circumferential stress / inside pressure
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
1
2
3
4
5
Radial distance across Si ring width (µm)
D=2µm, W=1.0µm
D=2µm, W=2.0µm
D=5µm, W=2.5µm
D=5µm, W=5.0µm
D=10µm, W=2.5µm
D=10µm, W=5.0µm
D=5µm, W= 10µm
3D-SIC TSV without air-gap

Figure 6

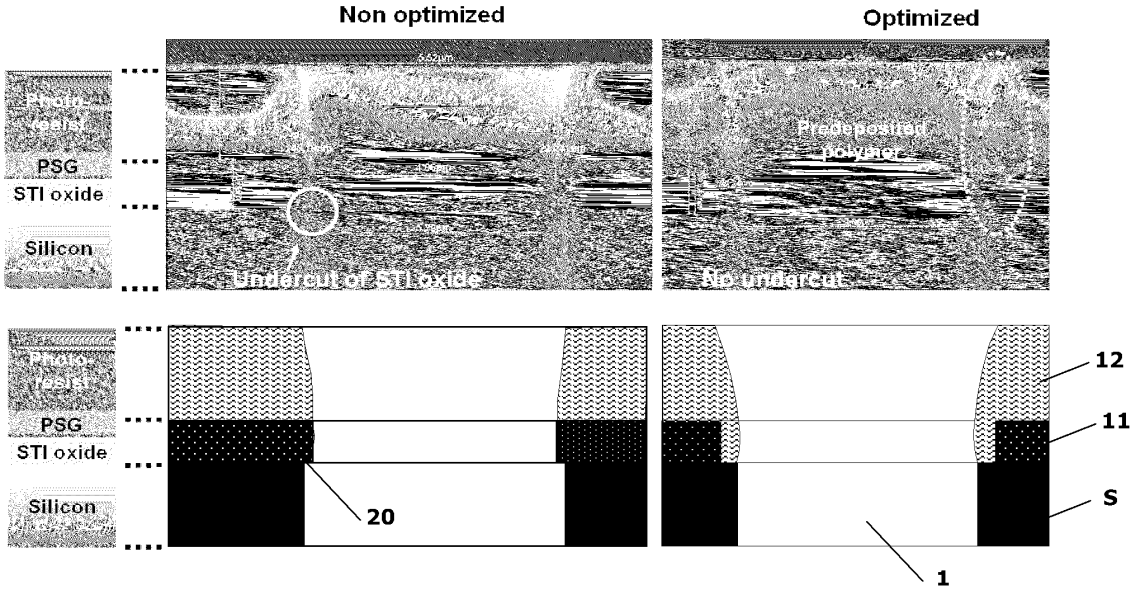


Figure 6A

Figure 6B

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Figure 7

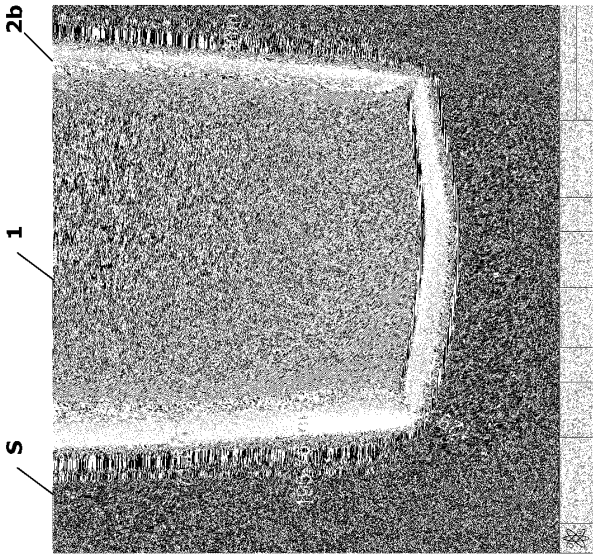


Figure 7B

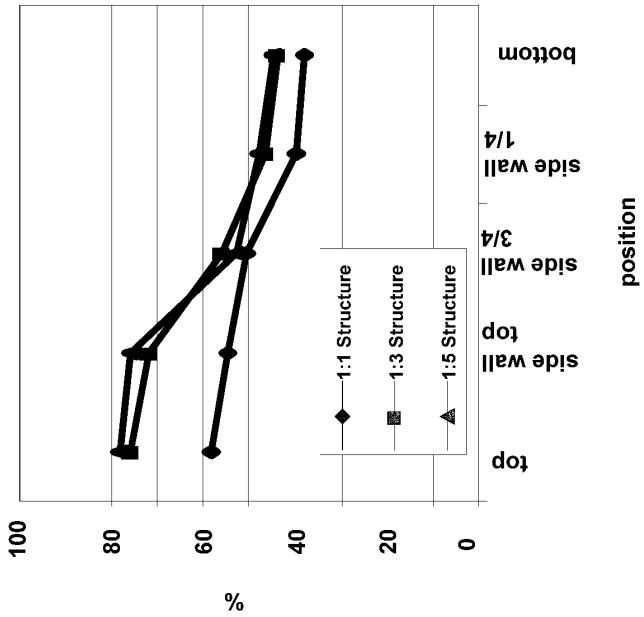


Figure 7A

Figure 8

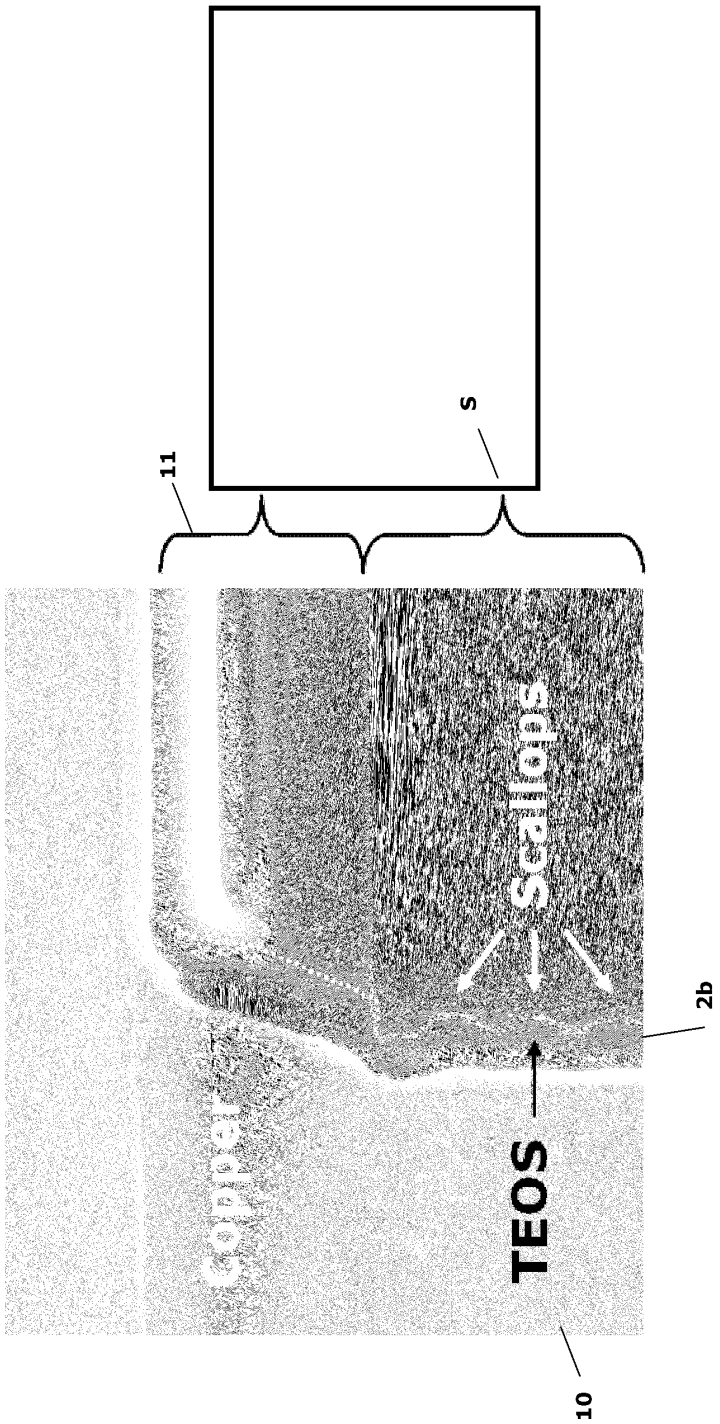


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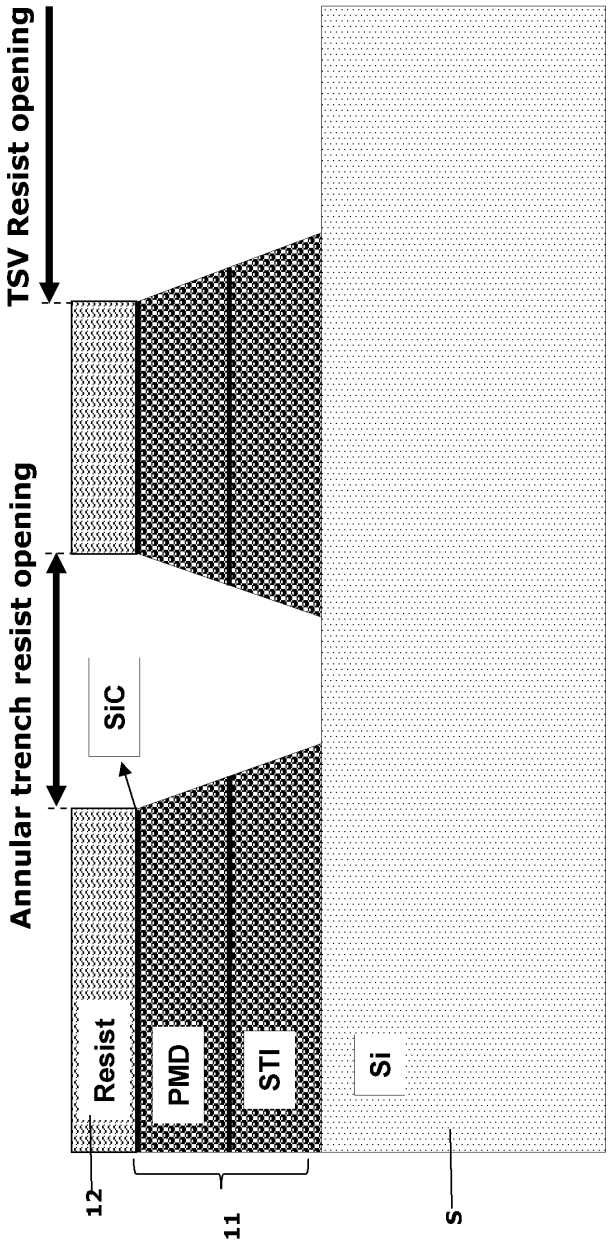

TSV Resist opening
Annular trench resist opening
SiC
Resist
PMD
STI
Si
12
11
S

Figure 10A

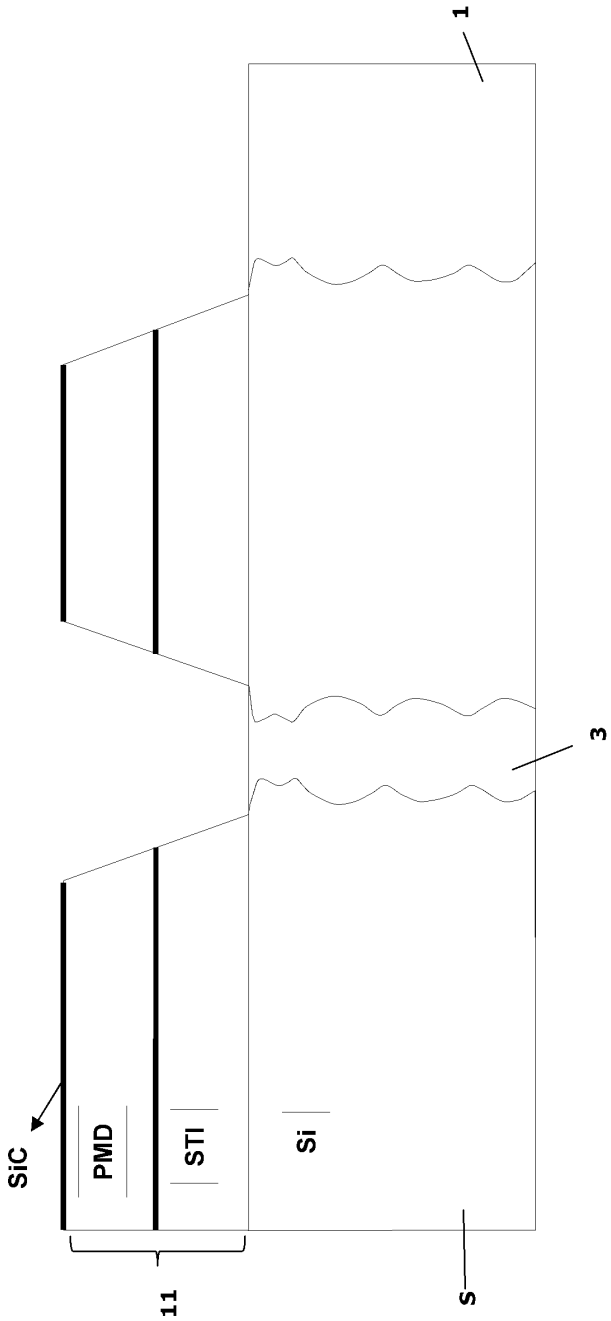


Figure 10B

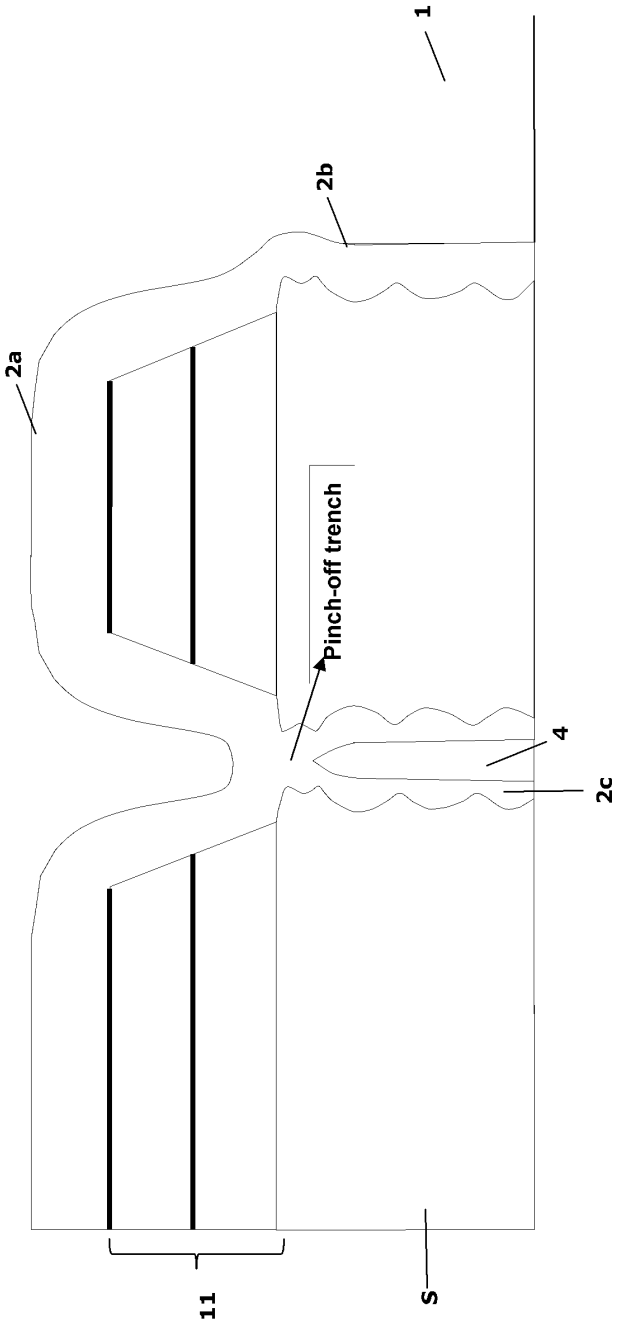


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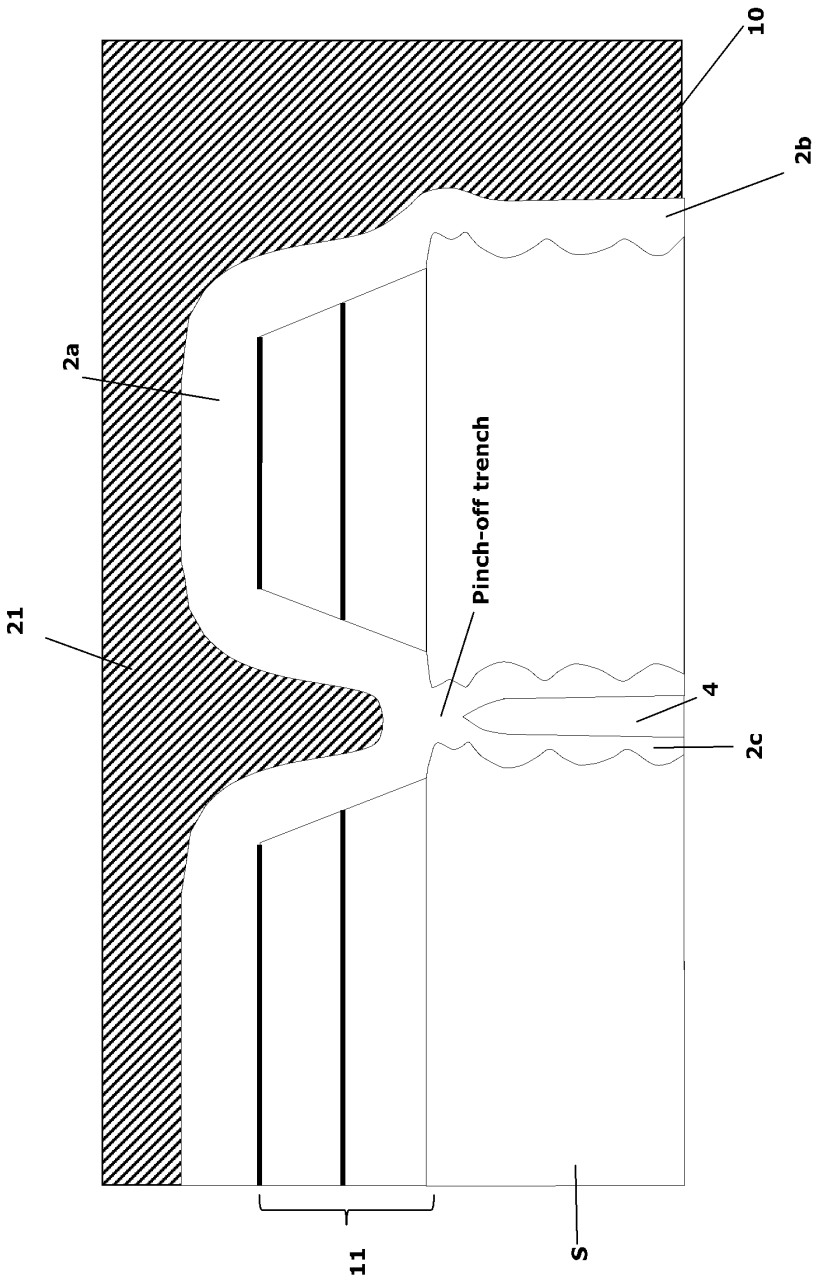


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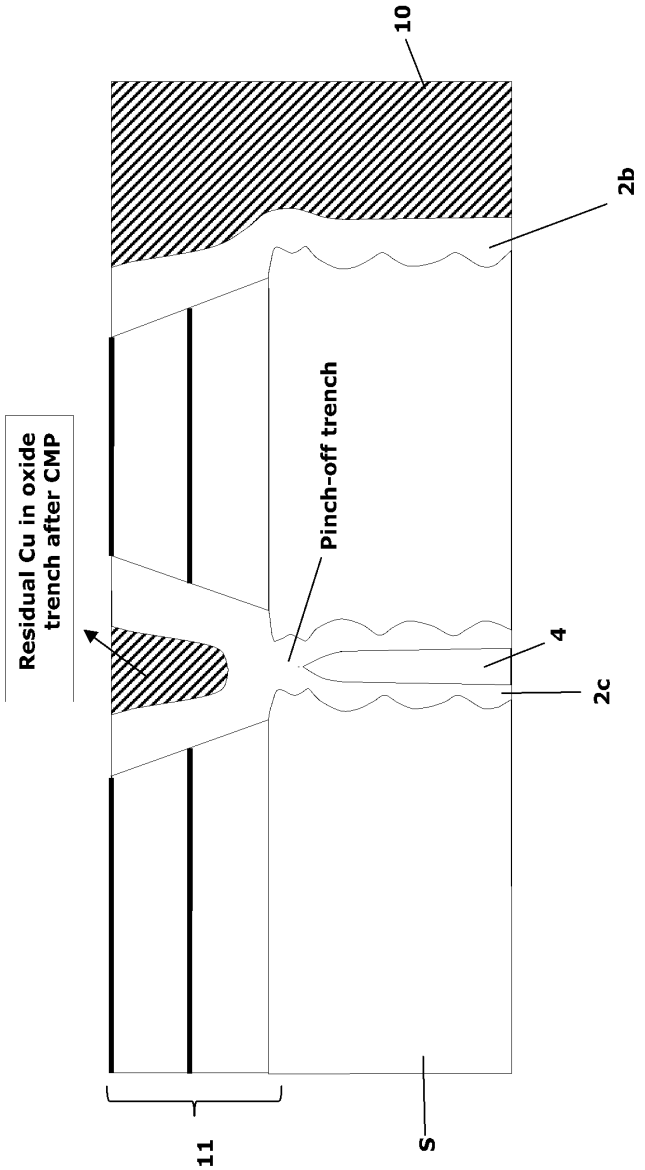

10
2b
Pinch-off trench
Residual Cu in oxide trench after CMP
4
2c
11
S

Figure 10E

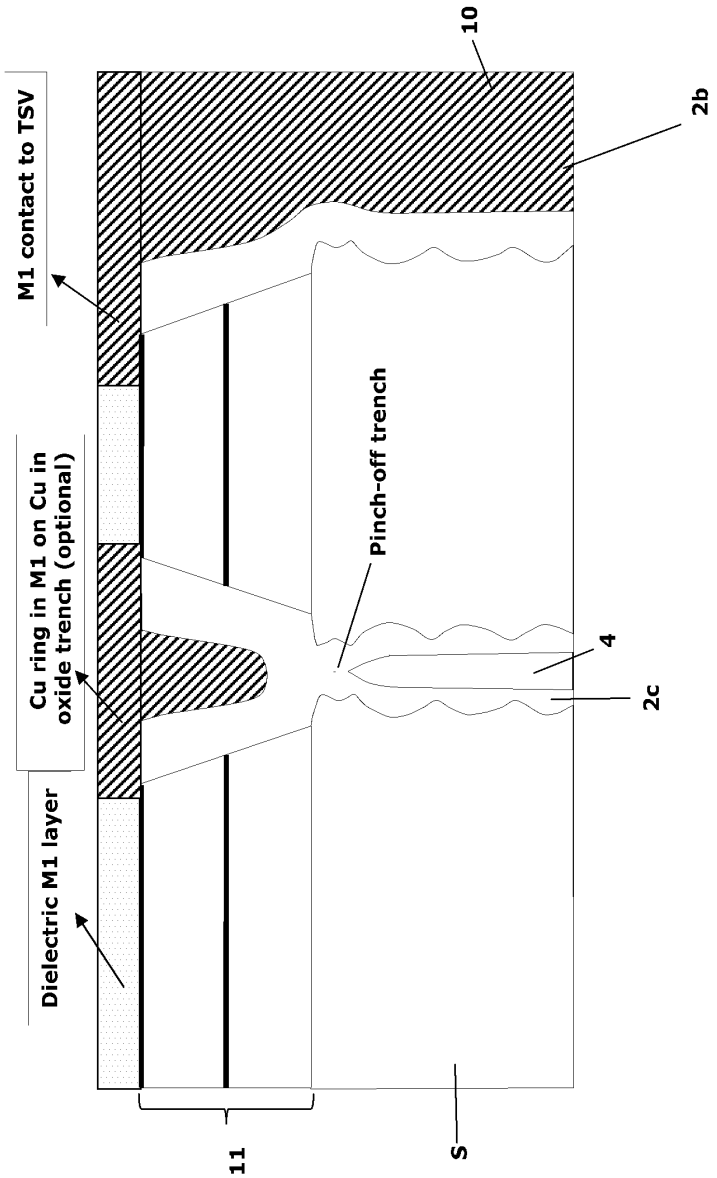

10
2b
M1 contact to TSV
Pinch-off trench
Cu ring in M1 on Cu in oxide trench (optional)
4
2c
Dielectric M1 layer
11
S

Figure 10F

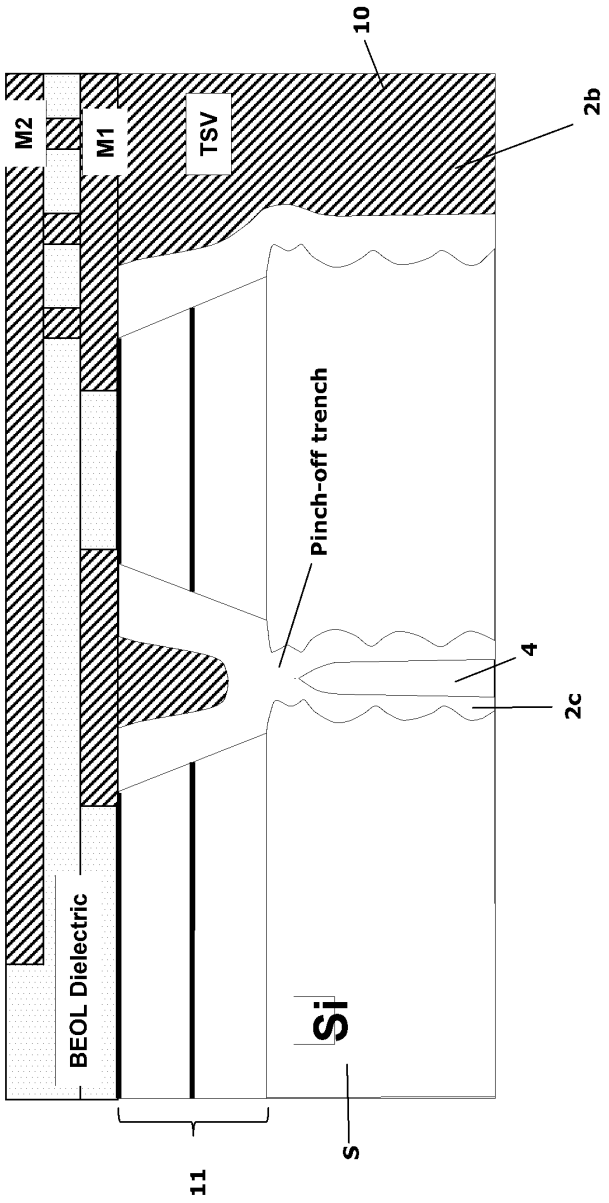


Figure 10G

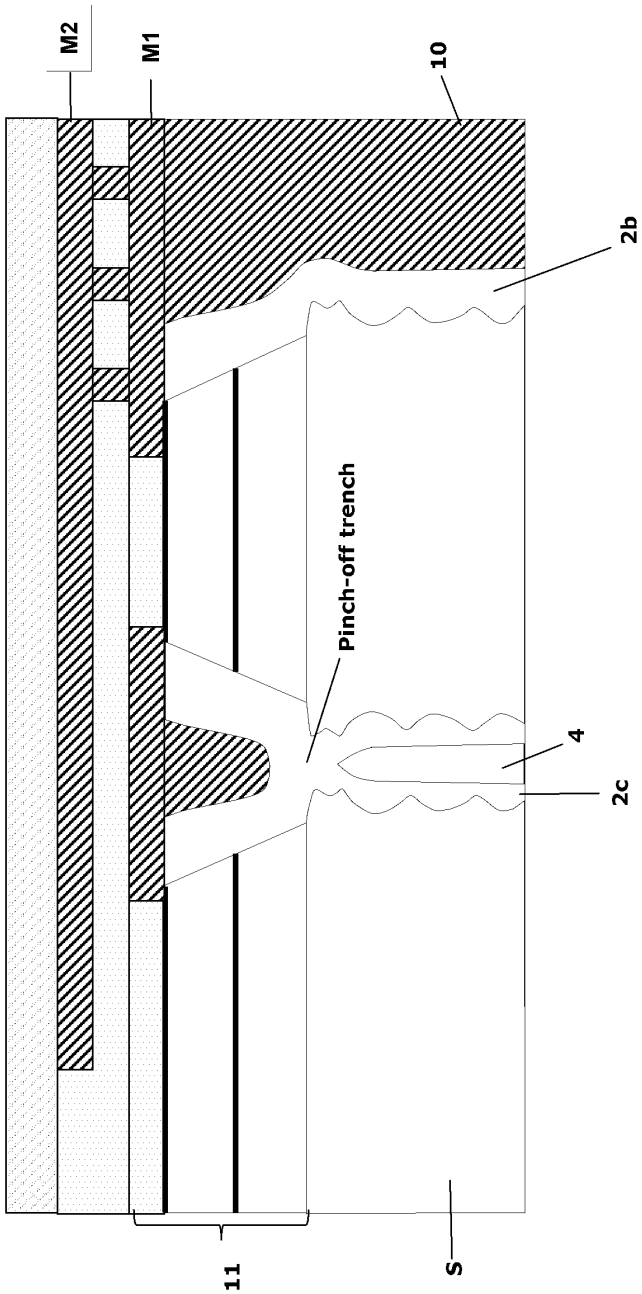


Figure 10H

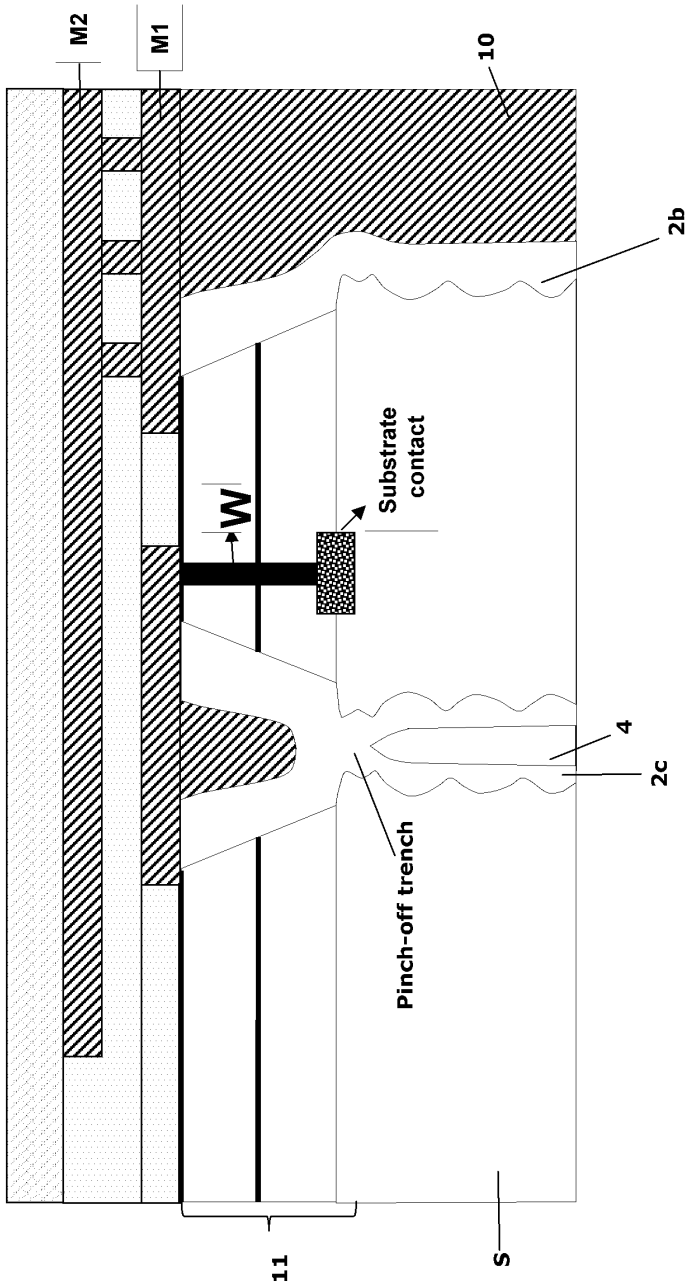


Figure 11

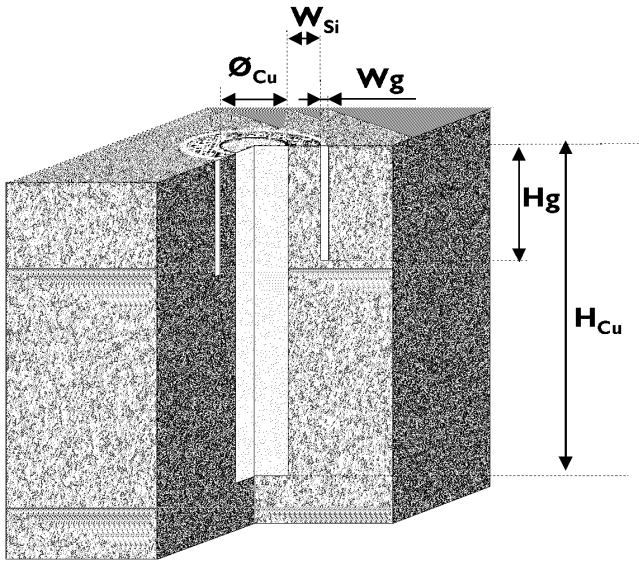


Figure 11A

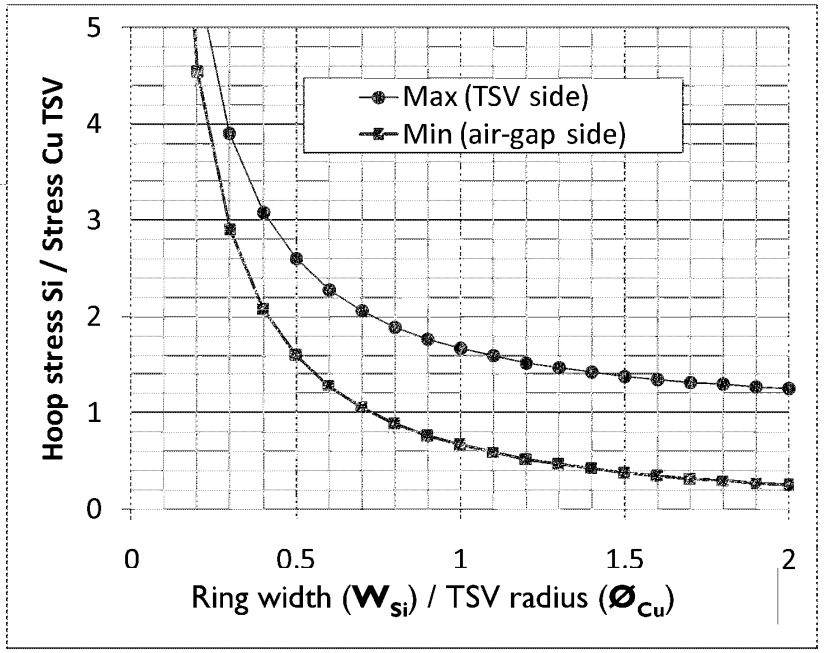


Figure 11B

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EAST Search History

EAST Search History (Prior Art)

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L37	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2014/04/02 10:42
L38	6	(through near silicon near via$2 TSV) and (taper pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2014/04/02 10:42
L39	21	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish	US-PGPUB; USPAT	OR	OFF	2014/04/02 10:42
L40	23	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$).did.	US-PGPUB; USPAT	OR	OFF	2014/04/02 11:07
L41	1	(US-7795134-$).did.	USPAT	OR	OFF	2014/04/02 11:14
L42	244	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish	US-PGPUB; USPAT	OR	OFF	2014/04/02 11:37
L43	2641	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow)	US-PGPUB; USPAT	OR	OFF	2014/04/02 11:54
L44	1003	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2014/04/02 11:54
L45	211	(through near silicon near via$2 TSV) same (tap$4 pinch near off narrow) and polish$4	US-PGPUB; USPAT	OR	OFF	2014/04/02 11:54
L46	95	(through near silicon near via$2 TSV) and (tap$4 pinch near off narrow) same polish$4	US-PGPUB; USPAT	OR	OFF	2014/04/02 12:04
L47	137	(through near silicon near via$2 TSV) with (taper$4 pinch near off contaminat$)	US-PGPUB; USPAT	OR	OFF	2014/04/02 12:13
L48	1	"8039386"	US-PGPUB; USPAT	OR	OFF	2014/04/02 12:19
L49	2	"12748101"	US-PGPUB; USPAT	OR	OFF	2014/04/02 12:19

L50	25	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:46
L51	0	50 and chamfer$2	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:46
L52	33	(through near silicon near via$2 TSV) and chamfer$2	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:48
L53	1	(through near silicon near via$2 TSV) and chamfer$2 with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:49
L54	5	(through near silicon near via$2 TSV) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:49
L55	83	(through near silicon near via$2 TSV contact near hole) and (round$3 chamfer$2) with corner same stress	US-PGPUB; USPAT	OR	OFF	2014/04/02 13:50
L56	26	(US-20090298285-$ or US-20120013022-$ or US-20110240481-$ or US-20110151659-$ or US-20100230818-$ or US-20100219513-$ or US-20130302980-$ or US-20120139127-$ or US-20140070339-$ or US-20110159690-$ or US-20120175789-$ or US-20100130002-$ or US-20110304026-$ or US-20110237073-$ or US-20080258307-$).did. or (US-7829976-$ or US-7772123-$ or US-7749899-$ or US-8178950-$ or US-8647920-$ or US-7531453-$ or US-8587126-$ or US-7955972-$ or US-8232626-$ or US-7795134-$ or US-8039386-$).did.	US-PGPUB; USPAT	OR	OFF	2014/04/02 14:09

EAST Search History (Interference)

<This search history is empty>

4/2/2014 3:43:32 PM
C:\Users\rbachner\Documents\EAST\Workspaces\13415744.wsp

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FEB 19 2014

Attorney Docket No.: 0150167

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**	Art Unit: 2898
Serial No.: 13/415,744	Examiner: Bachner, Robert G.
Filing Date: 03/08/2012	
For: **Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate**	

AMENDMENT AND RESPONSE TO OFFICE ACTION

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the Office Action dated December 19, 2013 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

02/20/2014 APEREZAM 00000005 13415744
01 FC:1251 200.00 OP

08JAZ0006

PAGE 5/11 * RCVD AT 2/19/2014 8:49:47 PM [Eastern Standard Time] * SVR:W-PTOFAX-003/14 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-17

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In the Claims:

Claim 1 (original): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

Claim 2 (original): The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

Claim 3 (original): The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

PAGE 6/11 * RCVD AT 2/19/2014 8:49:47 PM [Eastern Standard Time] * SVR:W-PTOFAX-003/14 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-17

Claim 4 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

Claim 5 (original): The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

Claim 6 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

Claim 7 (original): The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 8 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 9 (original): The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

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Claim 10 (original): The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

Claims 11-12 (canceled)

Claim 13 (original): A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion to prevent contamination during processing of said semiconductor substrate.

Claim 14 (original): The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

PAGE 8/11 * RCVD AT 2/19/2014 8:49:47 PM [Eastern Standard Time] * SVR:W-PTOFAX-003/14 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-17

Claim 15 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

Claim 16 (original): The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

Claim 17 (original): The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Claim 18 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

Claim 19 (original): The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

Claim 20 (original): The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

PAGE 9/11 * RCVD AT 2/19/2014 8:49:47 PM [Eastern Standard Time] * SVR:W-PTOFAX-003/14 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-17

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REMARKS

Prior to the present amendment and response, claims 1-20 were pending in the present application. It is noted that the present Office Action dated December 19, 2013 has a typographical error in that it has listed claims 11-20 as being "drawn to a method of forming a semiconductor device." However, only claims 11-12 are method claims, while claims 13-20 are "drawn to a semiconductor device," as are claims 1-10 that have been correctly listed as device claims in the present Office Action.

By the present amendment and response, the present application has been restricted to claims 1-10 and 13-20 for prosecution, while claims 11-12 have been canceled. Thus, claims 1-10 and 13-20 are now pending in the present application.

Applicant requests an early examination and/or allowance of claims 1-10 and 13-20 pending in the present application.

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Attorney Docket No.: 0150167

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 2/19/2014

Michael Farjami, Esq.
Reg. No. 38,135

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Date of Facsimile: 2/19/14

EVAN C. GANDERMAN
Name of Person Performing Facsimile Transmission

Signature 2/19/14
Date

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FACSIMILE TRANSMISSION COVER SHEET

Date: February 19, 2014

To: United States Patent and Trademark Office
Examiner: Bachner, Robert G.; Art Unit: 2898

Fax: (571) 273-8300

Re: **Application Serial No.: 13/415,744**
Filing Date: 03/08/2012; First-Named Inventor: Jebory
Attorney Docket No.: 0150167

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 11

Message:

Enclosed please find the Amendment and Response to Office Action dated December 19, 2013.

Payment for First Month Extension Fee in the amount of $200.00 is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

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Attorney Docket No.: 0150167

AMENDMENT COVER SHEET

IN RE APPLICATION OF: Jebory et al.

SERIAL NO.: 13/415,744 FILED: 03/08/2012

FOR: Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate

HONORABLE COMMISSIONER FOR PATENTS
P.O. Box 1450, Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith is a paper in the above-identified application. Any necessary extension of time period set for this paper is hereby requested.

☐ No additional fee is required.

☒ The fee has been calculated as shown below:

☒ EXTENSION FEE	RATE Non-Small Entity	RATE Small-Entity	FEE
FIRST MONTH AFTER TIME PERIOD SET	200.00	100.00	$200.00
SECOND MONTH AFTER TIME PERIOD SET	600.00	300.00	$
THIRD MONTH AFTER TIME PERIOD SET	1,400.00	700.00	$
FOURTH MONTH AFTER TIME PERIOD SET	2,200.00	1,100.00	$

☒ TOTAL EXTENSION FEE $200.00

☐ FEE FOR EXTRA CLAIMS added by Amendment in this response:

	Column 1 Number of Claims after Amendment	Column 2 Number Previously Paid for	Column 3 Number of Extra Claims	RATE Non-Small Entity	RATE Small Entity	FEE
TOTAL CLAIMS	18	MINUS **20	* = 0	x 80	x 40	$
INDEPENDENT	2	MINUS ***3	* = 1	x 420	x 210	$
First presentation of multiple dependent claim				+ 780	+ 390	$

TOTAL FEE FOR EXTRA CLAIMS $

* If the entry in Column 1 is less than the entry of Column 2, write "0" in Column 3.
** If the number of Total Claims previously paid for is less than 20, write "20" in this space.
*** If the number of Independent Claims previously paid for is less than 3, write "3" in this space.

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Attorney Docket No.: 0150167

☐ Total fee for Terminal Disclaimer $

☒ Enclosed is the total fee of **$200.00** (Payment by Credit Card, Form PTO-2038 Enclosed).

☐ Please charge Deposit Account No. 50-0731 in the amount of $ 0.00

☒ The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. **50-0731**.

Date: 2/19/2014

By: _____
Michael Farjami, Reg. No. 38,135

Michael Farjami, Esq.
Farjami & Farjami LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

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Signature

Evan C. Gunderman
Name of Person Performing Facsimile Transmission

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **02/19/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LAJUAN HICKSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/415,744	Filing Date 03/08/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **01/24/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/KIM WATSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/415,744	03/08/2012	Hadi Jebory	0150167	9194

25700 7590 12/19/2013

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
BACHNER, ROBERT G	
ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
12/19/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 13/415,744	Applicant(s) JEBORY ET AL.	
	Examiner ROBERT BACHNER	Art Unit 2898	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/8/12*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☒ Other: *Detailed Action*.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. **Claims 1-10** drawn to a semiconductor device, classified in class 257, and subclass 621.

II. **Claims 11-20** drawn to a method of forming a semiconductor device, classified in class 438, and subclass 667.

The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

In the instant case, the through silicon vias as recited in claim 1 could be formed by a materially different than that recited in claim 11. For example, the through silicon vias of claim 1 could be formed with a process of selectively depositing the materials as opposed to the deposition and removal (etching) of material as recited in claim 11. That is, apparatus of claim 1 could be formed using a materially different process than that recited in claim 11 and restriction is proper. Thus, a serious burden exists because the Examiner would be required to search in at least two different classes for the respective inventions.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or a grouping of patentably indistinct species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either

instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply:

The Examiner would be required to conduct a search in several classes and subclasses.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement

will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder**. Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BACHNER whose telephone number is (571)270-3888. The examiner can normally be reached on Mon-Thurs 8:30-5 alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio J. Maldonado can be reached on 571-272-1864. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROBERT G. BACHNER/
Examiner, Art Unit 2898

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13415744	JEBORY ET AL.
	Examiner	Art Unit
	ROBERT BACHNER	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/11/2013								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
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	20	÷								

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/415,744	03/08/2012	Hadi Jebory	0150167

CONFIRMATION NO. 9194

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

PUBLICATION NOTICE



Title: Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate

Publication No.US-2013-0087893-A1
Publication Date:04/11/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/415,744

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/415,744	03/08/2012	2812	1250	0150167	20	3

CONFIRMATION NO. 9194

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

FILING RECEIPT

OC000000053248005

Date Mailed: 03/30/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;

Assignment For Published Patent Application

NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR, NEWPORT BEACH, CA

Power of Attorney: The patent practitioners associated with Customer Number 25700

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/545,003 10/07/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 03/20/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/415,744**

Projected Publication Date: 04/11/2013

Non-Publication Request: No

Early Publication Request: No

Title

Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/415,744

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/415,744	03/08/2012	2812	1250	0150167	20	3

CONFIRMATION NO. 9194

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

FILING RECEIPT

OC000000053248005

Date Mailed: 03/23/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;

Assignment For Published Patent Application

NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR, NEWPORT BEACH, CA

Power of Attorney: The patent practitioners associated with Customer Number 25700

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/545,003 10/07/2011

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If Required, Foreign Filing License Granted: 03/20/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/415,744**

Projected Publication Date: Perfected

Non-Publication Request: No

Early Publication Request: No

Title

Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate

Preliminary Class

438

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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PATENT APPLICATION COVER SHEET

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Transmitted herewith is the patent application of:

ASSIGNEE: NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR (NEWPORT BEACH, CA)

Inventor(s): Hadi Jebory and David J. Howard

For: "Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate"

This application is a ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____.

Enclosed are:

☒ Four (4) Sheets of drawings

☐ Request for Non-Publication (Form PTO/SB/35 (11-00))

☐ Separate Payment Form PTO-2038 for $40.00 is Attached for Assignment of the invention to:

_____

☐ The enclosed payment includes $____for the recording of the assignment

☐ Information Disclosure Statement

☐ Preliminary Amendment

☒ Combined Declaration and Power of Attorney

☒ The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY		OTHER THAN A SMALL ENTITY	
FOR:	No. Filed	No. Extra	RATE	FEE	RATE	FEE
BASIC FEE				$190.00		$380.00
SEARCH FEE				$310.00		$620.00
EXAMINATION FEE				$125.00		$250.00
APPLICATION SIZE FEE (Total Number of Sheets)	(23 -100)/50=	0	x $155.00=	$	x $310.00=	$
TOTAL CLAIMS	20 -20 =	0	x $30.00=	$	x $60.00=	$
INDEPENDENT CLAIMS	3 -3 =	0	x $125.00=	$	x $250.00 =	$
MULTIPLE DEPENDENT CLAIMS PRESENTED			+$225.00=	$	+$450.00 =	$
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Date: March 8, 2012

/Michael Farjami Reg. # 38,135/

MICHAEL FARJAMI, ESQ.

Reg. No.: 38,135

Customer No.: 25700

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CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office through the EFS Filing System, on 3/8/12.

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Jembier Davalos — Signature

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE.

The specification of which
a. ☒ is attached hereto
b. ☐ was filed on _____ as application serial no. _____ and was amended on _____ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed _____ and as amended on _____ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, Sections 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications has been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC Section 119

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, Sections 119 and 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information material to patentability, as defined in Section 1.56 of Title 37, Code of Federal Regulations, which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING	STATUS
61/545,003	**October 7, 2011**	**Pending**

I hereby appoint the attorneys associated with the Customer Number below to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Customer Number 25700

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them to the contrary.

Please direct all correspondence in this case to **FARJAMI & FARJAMI LLP** at the address associated with the Customer Number below:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF INVENTOR: **Hadi Jebory**

MAILING/RESIDENCE ADDRESS: 36 Valente; Irvine, CA 92602

COUNTRY OF CITIZENSHIP: U.S.A.

SIGNATURE OF INVENTOR: _____ DATE: 03/01/2012

FULL NAME OF INVENTOR: **David J. Howard**

MAILING/RESIDENCE ADDRESS: 19 Springwater; Irvine, CA 92604

COUNTRY OF CITIZENSHIP: U.S.A.

SIGNATURE OF INVENTOR: _____ DATE: 2012.03.1ST

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A *prima facie* case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Attorney Docket No.: 0150167

UNITED STATES PATENT APPLICATION

FOR

THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

INVENTORS:

HADI JEBORY
DAVID J. HOWARD

PREPARED BY:
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(949) 282-1000

Customer No.: 25700

08JAZ0006

BACKGROUND

The present application claims the benefit of and priority to a pending provisional patent application entitled "Through Silicon Via with a Pinched Off Region and Related Method," Serial Number 61/545,003 filed on October 7, 2011. The disclosure in that pending provisional application is hereby incorporated fully by reference into the present application.

Semiconductor die density has continuously increased, and continues to increase. Further miniaturization and increased density in semiconductor dies require an increasing number of signal, ground and power electrical interconnects and connections. To make efficient use of limited surface area on semiconductor dies, conventional methods have included forming interconnects within the semiconductor dies using through wafer vias (TWVs). Conventional TWVs may, for example, connect a ground plane on a bottom surface of a semiconductor die with circuitry on a top surface of a semiconductor die. However, such conventional TWVs are typically very wide, for example, 50 μm (micrometers) in diameter. Such large widths result in undesirable characteristics in semiconductor dies and their semiconductor substrates. For example, placement of numerous conventional TWVs within a semiconductor substrate can result in a significant reduction in mechanical stability of the semiconductor substrate. Thus, the number and density of such conventional TWVs placed within a semiconductor substrate must be limited. Such limitations result in large minimum distances between TWVs and semiconductor devices, such as transistors, situated in a semiconductor die.

Moreover, utilizing a small number of conventional TWVs results in an uneven

thermal dissipation within the semiconductor substrate, especially during high power operation. The uneven thermal dissipation can result in increased thermal stress in the semiconductor substrate, thus reducing mechanical stability and reliability of the semiconductor die.

Further, although it is desirable to completely fill TWVs with conductive material, conventional fabrication methods result in incomplete filling of the TWVs, especially at their top and bottom portions. The incomplete filling can result in unwanted gaps in the top and bottom portions of the TWVs which can, for example, lead to contamination of the TWVs during subsequent processes.

SUMMARY

The present application is directed to through silicon via structure, method of formation, and integration in semiconductor substrate, substantially as shown in and/or described in connection with at least one of the figures, and as set forth more completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates an exemplary cross-sectional view of a portion of a semiconductor substrate including a conventional through wafer via.

Figure 1B illustrates an exemplary top view of a portion of a semiconductor substrate including a conventional through wafer via.

Figure 2 illustrates an exemplary perspective view of a portion of a semiconductor substrate including through silicon vias in accordance with one implementation of the present application.

Figure 3 illustrates an exemplary top view of a semiconductor substrate including through silicon vias having chamfered corners in accordance with one implementation of the present application.

Figure 4 illustrates an exemplary cross-sectional view of a through silicon via within a semiconductor substrate in accordance with one implementation of the present application.

Figure 5 presents an exemplary flowchart illustrating a method of fabricating a through silicon via in accordance with one implementation of the present application.

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. One skilled in the art will recognize that the present disclosure may be implemented in a manner different from that specifically discussed herein. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual relative dimensions.

Figure 1A presents an exemplary cross-section of conventional semiconductor structure 100 including exemplary through-wafer via 118 disposed in substrate 110, exemplary semiconductor device 108 disposed on top surface 134 of substrate 110, and ground plane 120 disposed on bottom surface 132 of substrate 110. Similarly, Figure 1B presents an exemplary top view of conventional semiconductor structure 100. In conventional semiconductor structure 100, through-wafer via 118 may extend from bottom surface 132 of substrate 110 to top surface 134 of substrate 110 and may generally have a uniform width w_1. By way of one specific example, width w_1 may be approximately 50 μm, where through-wafer via 118 has a circular cross-section. Because through-wafer via 118 extends the entire depth of substrate 110, both through-wafer via 118 and substrate 110 can generally have a depth of, for example, approximately 200 μm. Through-wafer via 118 is also typically contacted at the bottom surface of substrate 110

by ground plane 120. Semiconductor device 108, which may be a transistor for example, is also shown in Figures 1A and 1B and may be connected to ground plane 120 by through-wafer via 110. However, due to the very wide cross section of through-wafer via 118, semiconductor device 108 typically requires placement at a distance d_1 from through-wafer via 118, which may be, for example, at least 15 μm to 20 μm.

In addition, the very large width of through-wafer via 118 typically limits the number of through-wafer vias that may be formed in a substrate of a particular dimension. For example, in a typical substrate it is common for multiple through-wafer vias to be spaced hundreds of micrometers (μm) apart. Such large spacing between through-wafer vias results in uneven thermal dissipation within the substrate. Differences in the thermal coefficients of substrate 110 and through-wafer via 118 may cause high levels of mechanical stress in substrate 110 when heated, which can lead to cracking of substrate 110. The very large width of exemplary through wafer via 118 can increase such thermally induced mechanical stress in substrate 110.

Figure 2 presents an exemplary perspective view of semiconductor structure 200 including top surface 220 of substrate 212 and cross-section 230 of substrate 212, taken at edge 224, for example. Substrate 212 may include narrow through-silicon vias (TSVs) 202, 204 and 206, for example. Substrate 212 may also include various semiconductor devices such as exemplary semiconductor devices 208 and 210. Exemplary semiconductor devices 208 and 210 may be any type of semiconductor device, such as various transistors, for example, NPN bipolar transistors, or any other device without limitation.

Narrow TSVs 202, 204 and 206 may be arranged in arrays, such as array 240 for example, disposed in substrate 212, to suit the needs of a particular application. For example, each of narrow TSVs 202, 204 and 206 may provide a ground connection to exemplary semiconductor devices 208 and 210, for example. In addition, all TSVs in a particular array may be connected to one another by an overlying metal 1 or metal 2 layer (not shown), for example. The novel features of narrow TSVs 202, 204 and 206, which will be discussed in greater detail below, allow exemplary semiconductor devices 208 and 210 to be placed much closer to TSVs 202, 204 and 206 than conventional TWV designs. Figure 2 shows such a reduced distance d_2, which may be 5-10 μm, for example. Thus, as one specific example, exemplary semiconductor devices 208 and 210 may be placed as much as 2 to 3 times closer, in one dimension, to TSVs 202, 204 and 206 as compared to conventional via designs. This allows the present implementation to greatly reduce the amount of wasted substrate area.

In addition, because TSVs 202, 204 and 206 may be placed much closer to each other than in conventional TWV designs, uniform thermal dissipation and heatsinking through TSVs 202, 204 and 206 becomes more practical. Furthermore, the resistance and ground path length of narrow TSVs 202, 204, and 206 are still improved relative to conventional wire bonds, or even relative to through-wafer vias since a greater number of TSVs can be used, which can also be placed closer to ground terminal connections of semiconductor devices, such as semiconductor devices 208 and 210, of semiconductor structure 200.

Turning to Figure 3, Figure 3 presents an exemplary top view 340 of a portion of

TSV array 240 of Figure 2. TSVs 302, 304 and 306 may each correspond to TSVs 202, 204 and 206 of Figure 2, respectively. As shown in Figure 3, each of TSVs 302, 304 and 306 may have a rectangular shape and may, in one particular example, be oriented such that TSVs 302 and 306 have a longer side oriented parallel to a Y-axis (also referred to as being laid out in a "length direction" in the present application) and TSV 304, disposed between TSVs 302 and 306, has a longer side oriented parallel to an X-axis (also referred to as being laid out in a "width direction" in the present application). Thus, according to the implementation presented by Figure 3, each TSV in an array may be oriented at a 90° angle relative to an adjacent TSV. Such orientation may reduce cracking in the substrate by interrupting naturally forming cleavage planes 312 caused by thermal and mechanical stresses in the substrate.

To further reduce thermal and mechanical stress in the substrate, at least one corner of each of TSVs 302, 304 and 306 may be a chamfered corner 314. Preferably, however, each corner of each TSV may be chamfered. Chamfering each corner of TSVs 302, 304 and 306 may also help to complete the narrow, deep etch required by the present implementation. Each of TSVs 302, 304 and 306 may have the same dimensions. In one specfic example, each of TSVs 302, 304 and 306 may have a short side width w_2 of 2-5 μm and a long side width w_3 of 6-10 μm, for example. Thus, TSVs 302, 304 and 306 allow for greater flexibility in their placement in the substrate due to their significantly smaller size and cleavage plane impeding orientations. Each of TSVs 302, 304 and 306 may be etched into the substrate to a depth of, for example, 100 μm. The finished depth of the TSVs and substrate may then be accurately controlled by polishing the bottom

surface of the substrate, as will be discussed in further detail below.

The fabrication of one or more TSVs in a semiconductor substrate will be further described by reference to Figures 4 and 5. Figure 4 presents an exemplary magnified view of TSV 402, which may correspond to TSV 202 of Figure 2, for example. Figure 5 presents an exemplary flowchart implementing a method of fabricating a through silicon via having a pinched off region such as, for example, TSV 402.

Action 510 of flowchart 500 includes performing a first etch into substrate 412 to first depth d_3 to form sidewalls 440 of through silicon via 402. The first etch to first depth d_3 may be controlled by, for example, adjusting the time of first etch action 510.

Continuing with action 520 of flow chart 500, action 520 includes performing a second etch in through silicon via 402 to second depth d_4 such that through silicon via 402 tapers from first depth d_3 to second depth d_4. Action 520 may be carried out by varying the etchant power during action 520. As a specific example, etchant power may be varied from 50 watts to 20 watts during etch action 520. Reducing the etchant power allows the formation of a narrowing portion of TSV 402 from first depth d_3 to second depth d_4. Alternatively, or in addition, adding O_2 during action 520 may make the etch more selective, effectively reducing the width of the etch during action 520. Though specific etch techniques are disclosed, action 520 may be achieved by other appropriate etching methods. Thus, action 520 may result in a contouring of the shape of TSV 402 such that a bottom portion (i.e. the portion generally below first depth d_3) of TSV 402 tapers. In one specific example, TSV 402 may taper to a width of approximately 1 μm and second depth d_4 may be approximately 15 μm.

Once TSV 402 has been etched to second depth d_4, optional insulation layer 436 may be deposited on silicon sidewalls 440 of TSV 402. However, preferentially, such an optional insulation layer 436 may not be included to ensure that conductive filler 430 is in contact with silicon sidewalls 440 of TSV 402 and a ground plane on the bottom surface of the substrate, for example.

Action 530 of Figure 5 includes depositing conductive filler 430 on sidewalls 440 of through silicon via 402 such that hollow center portion 432 and pinched off region 438 are formed in through silicon via 402. The tapered portion of TSV 402 (i.e. the portion generally below depth d_3), allows conductive filler 430 to completely fill the bottom portion of TSV 402. In the alternative, conductive filler 430 may by deposited to incompletely fill the bottom portion of TSV 402. In a preferred implementation, conductive filler 430 is a metallic filler, for example, tungsten. Action 530 may be accomplished using any appropriate deposition technique, such as chemical vapor deposition (CVD) or atomic layer deposition (ALD), for example.

Hollow center portion 432 provides many beneficial features. For instance, hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402. Hollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions. Such reduction in thermal and mechanical stress reduces cracking in substrate 412. In addition, hollow center portion 432 in TSV 402 can be formed using present manufacturing tools and without increasing production costs.

In addition to pinched off region 438 at a bottom portion of TSV 402, the present

implementation may include forming pinched off region 434 at a top portion of TSV 402. A natural loading effect exists when depositing fillers, which causes an increased deposition at the top of vias. However, to ensure that hollow center portion 432 does not extend to the top of TSV 402, oxide layer 424 may be deposited over the top surface of substrate 412. An opening 428 may be formed in oxide layer 424, over TSV 402, such that sides 426 of opening 428 remain within sidewalls 440 of TSV 402, thus resulting in the width of opening 428 to be smaller than the width of TSV 402. Depositing oxide layer 424 and forming opening 428 ensures pinched off region 434 is formed in the top region of TSV 402, and that hollow center portion 432 does not extend to the top of TSV 402.

Turning to action 540 of flow chart 500, action 540 includes polishing bottom surface 460 of substrate 412 to expose conductive filler 430 from the bottom surface of the substrate. Polish action 540 may be performed until polish line 450a is reached in substrate 412 (i.e. until bottom surface 460 becomes the same as polish line 450a). Polish line 450a may represent a bottom surface of processed substrate 412. Alternatively, polish action 540 may be performed until polish line 450b is reached in substrate 412 (i.e. until bottom surface 460 becomes the same as polish line 450b), which may represent an alternative bottom surface of processed substrate 412 where an incomplete filling of the bottom portion of TSV 402 is desired.

Carrying out prior action 530 and filling a bottom portion of TSV 402 with conductive filler 430 may ensure that no contamination of TSV 402 occurs during polish action 540, for example. In addition, due to the narrow width of the bottom of TSV 402,

a subsequent rough polish will not cause damage to the via, unlike conventional TWV fabrication methods. Consequently, only a rough polish is required at bottom surface 460 to achieve a good contact with a ground plane metal layer which may be subsequently applied to bottom surface 460 of substrate 412. Thus, according to the present implementation, a subsequent fine polish or dry etch at this point in fabrication is avoided.

Thus, various implementations disclosed in the present application provide through silicon vias with a pinched off region which reduce thermal and mechanical stress in semiconductor substrates, as compared to conventional TWVs. Such through silicon vias further reduce the amount of wasted semiconductor substrate area as well as prevent contamination of the through silicon vias during semiconductor substrate processing.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the spirit and the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described herein, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

CLAIMS

1. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate.

2. The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

3. The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.

4. The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.

5. The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.

6. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.

7. The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

8. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.

9. The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.

10. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

11. A method of forming a through silicon via in a semiconductor substrate,

said method comprising:

performing a first etch into said substrate to a first depth to form sidewalls of said through silicon via;

performing a second etch in said through silicon via to a second depth such that said through silicon via tapers from said first depth to said second depth;

depositing a conductive filler on said sidewalls of said through silicon via such that a hollow center and a pinched off region are formed in said through silicon via;

wherein said pinched off region prevents contamination during processing of said semiconductor substrate, and said hollow center reduces thermal stress in said semiconductor substrate.

12. The method of claim 11, further comprising polishing a bottom surface of said substrate to expose said conductive filler from said bottom surface of said substrate.

13. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a

top portion to prevent contamination during processing of said semiconductor substrate.

14. The semiconductor substrate of claim 13, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.

15. The semiconductor substrate of claim 13, wherein said conductive filler comprises a metallic filler.

16. The semiconductor substrate of claim 13, wherein said conductive filler comprises tungsten.

17. The semiconductor substrate of claim 13, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

18. The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias has at least one chamfered corner.

19. The semiconductor substrate of claim 13, further comprising a pinched off region at a bottom of each of said plurality of through silicon vias.

20. The semiconductor substrate of claim 13, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

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ABSTRACT

Various implementations of through silicon vias with pinched off regions are disclosed. A semiconductor substrate includes a plurality of the through silicon vias disposed in the substrate and extending from a top surface of the substrate to a bottom surface of the substrate. A conductive filler is disposed within each of the plurality of through silicon vias, each of the plurality of through silicon vias having a hollow center which reduces thermal stress in the semiconductor substrate. The plurality of through silicon vias also have pinched off regions at the bottom and/or the top portions of the through silicon vias, which prevent contamination during processing of the semiconductor substrate.

Fig. 1A

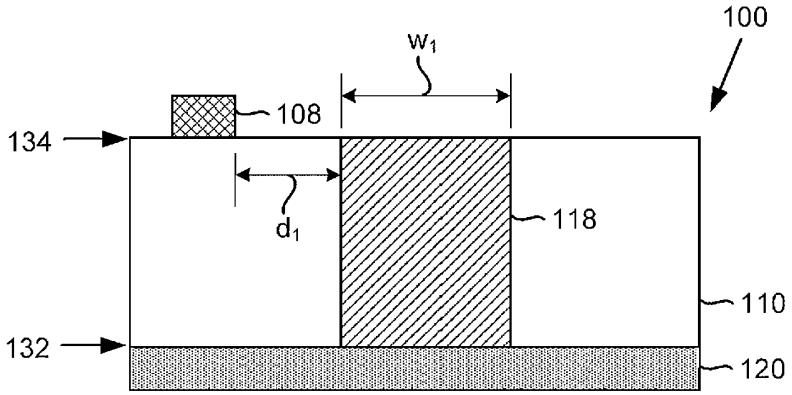


Fig. 1B

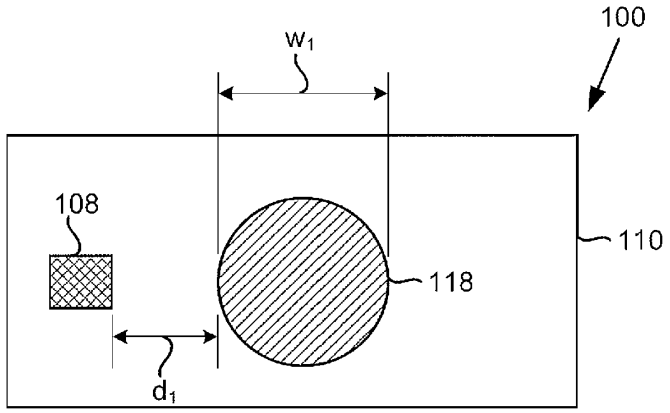


Fig. 2

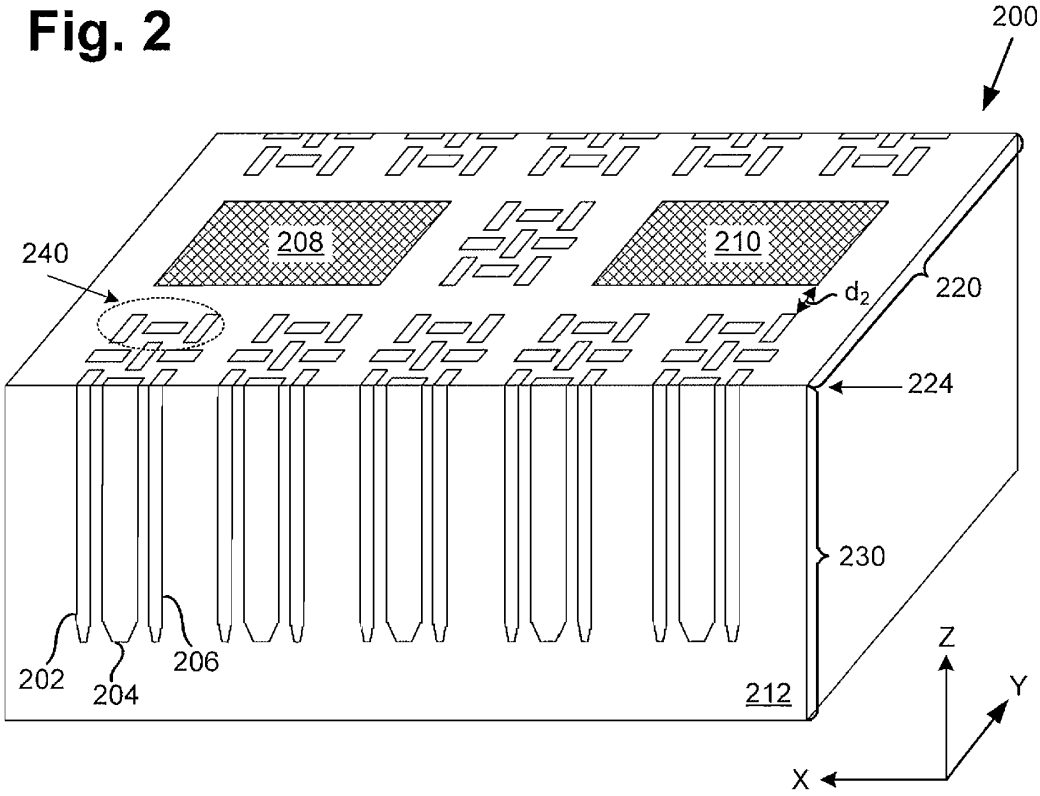

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240
208
210
220
d_2
224
230
202
204
206
212
Z
Y
X

Fig. 3

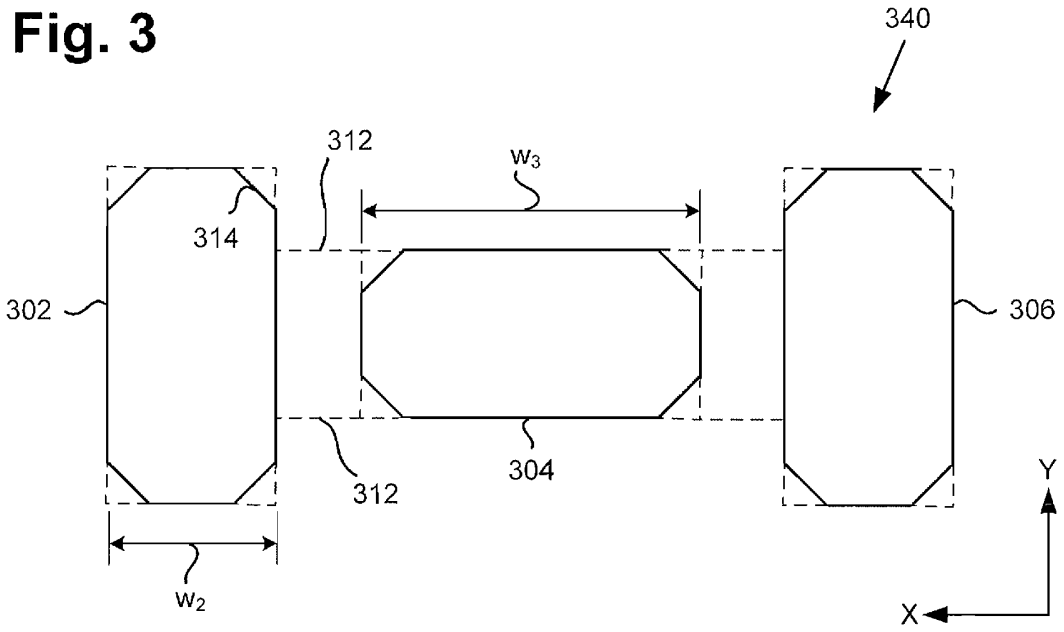

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312
w_3
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304
312
w_2
Y
X

Fig. 4

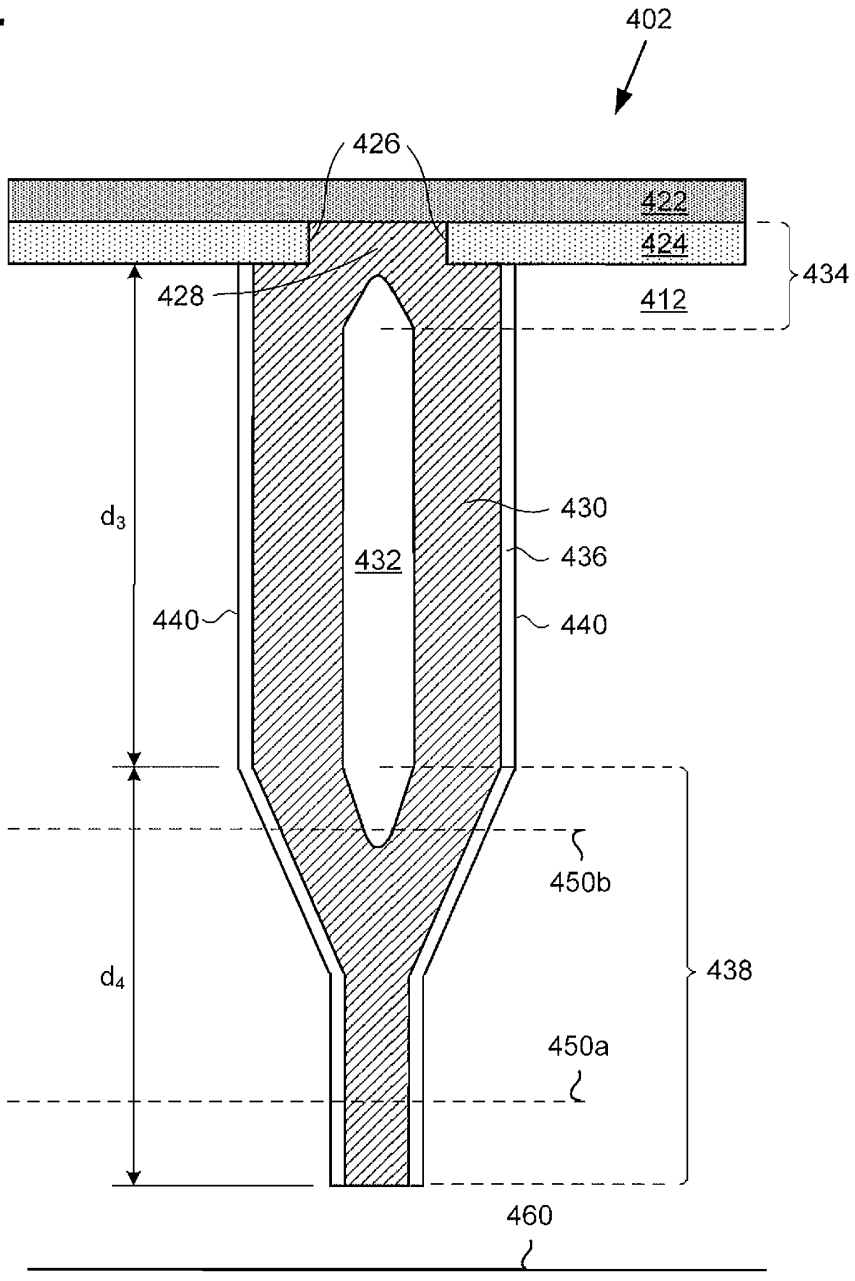
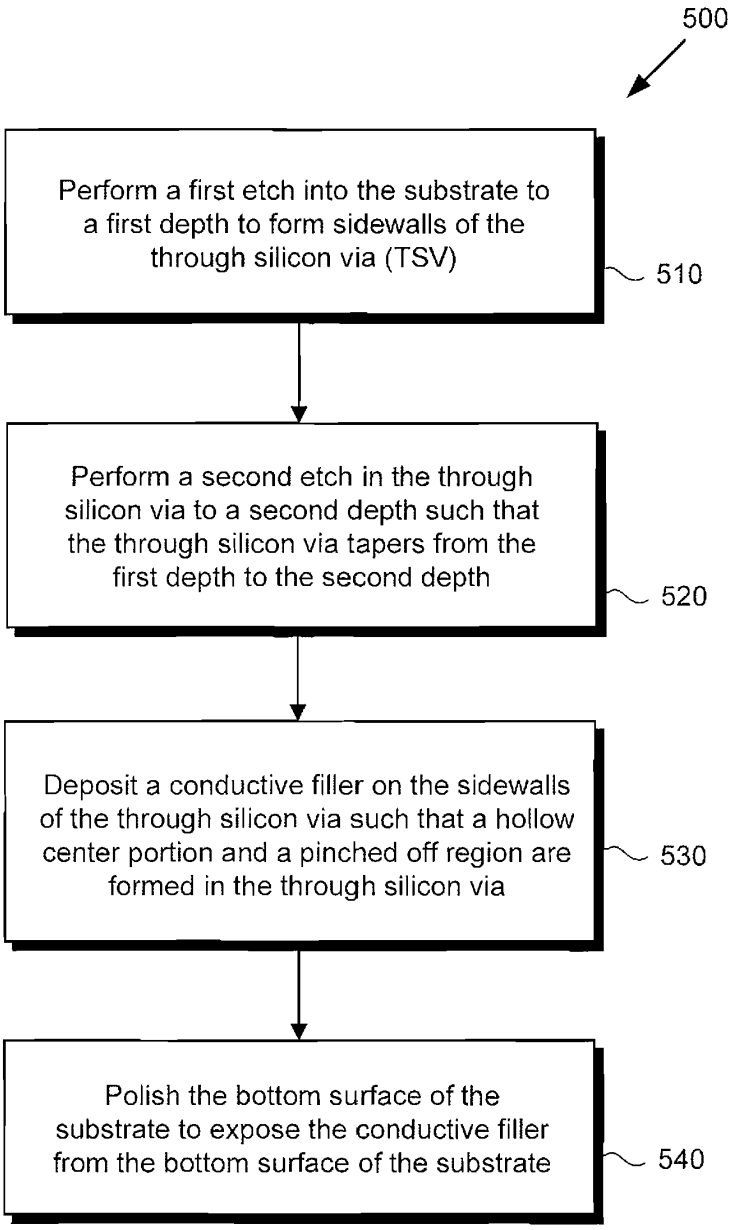

402
426
422
424
434
428
412
d_3
430
432
436
440
440
450b
438
d_4
450a
460

Fig. 5


500
Perform a first etch into the substrate to a first depth to form sidewalls of the through silicon via (TSV)
510
Perform a second etch in the through silicon via to a second depth such that the through silicon via tapers from the first depth to the second depth
520
Deposit a conductive filler on the sidewalls of the through silicon via such that a hollow center portion and a pinched off region are formed in the through silicon via
530
Polish the bottom surface of the substrate to expose the conductive filler from the bottom surface of the substrate
540

Electronic Patent Application Fee Transmittal	
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Filing Date:	
Title of Invention:	Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate
First Named Inventor/Applicant Name:	Hadi Jebory
Filer:	Michael Farjami/Jembier Davalos
Attorney Docket Number:	0150167
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Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

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Extension-of-Time:				
Miscellaneous:				
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	Transmittal of New Application		1	2	
	Oath or Declaration filed		3	5	
	Specification		6	18	
	Claims		19	23	
	Abstract		24	24	
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