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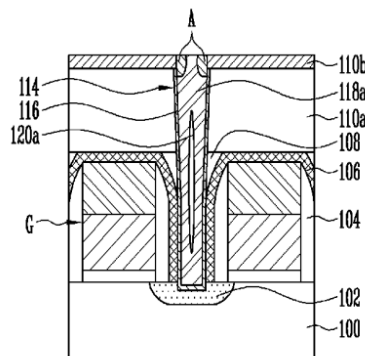
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(54) METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE**(57) Abstract**

The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a method of manufacturing a semiconductor device comprising: a step of forming an interlayer insulating film by sequentially forming first, second, and third insulating films on a semiconductor substrate, wherein the first and third insulating films have an etching selectivity that differs from that of the second insulating film; a step in which a contact hole is formed that penetrates through the interlayer insulating film and has a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films; a step in which a metal barrier layer is formed in the contact hole along the surfaces of the contact hole and the interlayer insulating film, the metal barrier layer having an overhang on the sidewall of the protruding second insulating film; a step in which a metal layer is formed that fills the contact hole but has a seam that is closed in the vicinity where the overhang occurs; and a step in which a contact plug is formed by etching the metal layer, the metal barrier layer, and the interlayer insulating film so as to expose the second insulating film.

Representative Drawing - FIG. 1h

CLAIMS

Claim 1

A method of manufacturing a semiconductor device, comprising:

- a step of forming an interlayer insulating film by sequentially forming first, second, and third insulating films on a semiconductor substrate, wherein the first and third insulating films have an etching selectivity that differs from that of the second insulating film;
- a step in which a contact hole is formed that penetrates through the interlayer insulating film and has a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films;
- a step in which a metal barrier layer is formed in the contact hole along the surfaces of the contact hole and the interlayer insulating film, the metal barrier layer having an overhang on the sidewall of the protruding second insulating film;
- a step in which a metal layer is formed that fills the contact hole but has a closed seam in the vicinity where the overhang is created; and
- a step in which a contact plug is formed by etching the metal layer, the metal barrier layer, and the interlayer insulating film so as to expose the second insulating film.

Claim 2

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the first and third insulating films are formed as oxide films.

Claim 3

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the second insulating film is formed as a nitride film.

Claim 4

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the step in which a contact hole is formed having a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films further comprises:
 - a step of forming the contact hole by etching a partial region of the interlayer insulating film; and
 - a step of performing a cleaning process on the semiconductor substrate prior to depositing the metal barrier layer, so that the sidewall of the second insulating film is etched to a lesser degree than the first and third insulating films.

Claim 5

The method of manufacturing a semiconductor device according to claim 4, wherein:

- the cleaning process prior to depositing the metal barrier layer deposition uses BOE or HF.

Claim 6

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the metal barrier layer is formed as a Ti/TiN laminated structure using a physical vapor deposition method.

Claim 7

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the metal layer is formed of tungsten (W).

Claim 8

The method of manufacturing a semiconductor device according to claim 1, wherein:

- the contact plug is formed by etching the metal layer using a chemical mechanical polishing process.

SPECIFICATION***Detailed Description of the Invention******Technical Field***

[0001] The present invention relates to a method of manufacturing a semiconductor device, and more particularly to a method of manufacturing a semiconductor device whereby, when forming a contact plug with a large aspect ratio, the shape of a seam formed in a tungsten film for the contact plug can be improved so as to prevent the seam from being exposed in a subsequent process.

Background Art

[0002] In the situation of a tungsten plug (W plug) used to fill a deep contact hole in a memory device, a seam will unavoidably be created inside the plug due to the increase in aspect ratio due to increased device integration. The seam that forms inside the tungsten plug acts to increase the resistance of the conductor itself, and also causes further problems depending on where the seam is located. When a seam of a tungsten film is present on the top of a tungsten plug, the size of the seam increases during the pre-chemical mechanical polishing (CMP) cleaning process, the CMP process, and the post-CMP cleaning process; as foreign matter, such as CMP residue or particles, becomes trapped in the seam, the resistance of the contact plug increases due to the effect of these CMP residue or particles, and thereby bridging between contact plugs may occur.

Summary of the Invention***Problem to be Solved***

[0003] An object of the present invention is to provide a method of manufacturing a semiconductor device that, when forming a contact plug having a large aspect ratio, improves the shape in which a seam is formed in a tungsten film for use in the contact plug, thereby preventing the seam from becoming exposed in a subsequent CMP process and a post-CMP cleaning process, thus making it possible to inhibit increased resistance of the contact plug and the occurrence of bridging between contact plugs due to foreign matter becoming caught in the seam.

Means of Solving the Problem

[0004] The method of manufacturing a semiconductor device according to an embodiment of the present invention comprises: a step of forming an interlayer insulating film by sequentially forming first, second, and third insulating films on a semiconductor substrate, wherein the first and third insulating films have an etching selectivity that differs from that of the second insulating film; a step in which a contact hole is formed that penetrates through the interlayer insulating film and has a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films; a step in which a metal barrier layer is formed in the contact hole along the surfaces of the contact hole and the interlayer insulating film, the metal barrier layer having an overhang on the sidewall of the protruding second insulating film; a step in which a metal layer is formed that fills the contact hole but has a closed seam in the vicinity where the overhang is created; and a step in which a contact plug is formed by etching the metal layer, the metal barrier layer, and the interlayer insulating film so as to expose the second insulating film.

[0005] Above, the first and third insulating films are formed as oxide films.

[0006] The second insulating film is formed as a nitride film.

[0007] The step in which a contact hole is formed having a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films further comprises a step of forming the contact hole by etching a partial region of the interlayer insulating film; and a step of performing a cleaning process on the semiconductor substrate prior to depositing the metal barrier layer, so that the sidewall of the second insulating film is etched to a lesser degree than the first and third insulating films.

[0008] In the cleaning process prior to metal barrier layer deposition, BOE (Buffered Oxide Etchant) or HF is used.

[0009] The metal barrier layer is formed as a Ti/TiN laminated structure using a physical vapor deposition (PVD) method.

[0010] The metal layer is formed of tungsten (W).

[0011] The contact plug is formed by etching the metal layer using a chemical mechanical polishing (CMP) process.

Effects

[0012] In the present invention, by the formation of the interlayer insulating film in which the second insulating film, which has an etching selectivity different from those of the first and third insulating films, is inserted between the first and third insulating films, a contact hole is formed to have a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films due to a difference between the films in etch rate during the metal barrier layer pre-cleaning process, so that when the metal barrier layer is subsequently formed, an overhang is formed on the protruding sidewall of the second insulating film in the contact hole; and when a tungsten film is subsequently deposited for filling the contact hole, a seam in the tungsten film is closed in the vicinity where the overhang occurred, so that the seam is prevented from becoming exposed in the subsequent CMP process and CMP post-cleaning process; thereby, bridging between contact plugs and increased contact plug resistance due to foreign matter becoming caught inside the seam can be inhibited.

[0013] In accordance with the method described above, process yield and device reliability can be improved.

Best Mode of Implementing the Invention

[0014] Below, an embodiment of the present invention will be explained in greater detail with reference to the attached drawings.

[0015] FIGS. 1a through 1h are process cross-sections illustrating the method of manufacturing a semiconductor device according to an embodiment of the present invention.

[0016] Referring to FIG. 1a, a semiconductor substrate (100) is provided on which gates (G) and gate spacers (104) are formed by a known manufacturing method under an etch stop film (106) and a planarized first interlayer insulating film (108); in a lower portion between the gates (G), a predetermined resultant is formed, such as a junction region (102). In the situation of a semiconductor device such as a DRAM, the gates (G) can be formed as a laminated structure having a gate insulating film and a gate electrode; in this situation, the gate electrode can be formed as a laminated structure having a polysilicon film and a metal layer. In the situation of a flash memory device, the gates (G) may be gates of a drain select transistor, in which situation each of the gates (G) can be formed as a laminated structure having a tunnel insulating film, a first conductive film, a dielectric film, and a second conductive film. In the situation of the gate (G) of a drain select transistor, the first conductive film and the second conductive film are electrically connected via a contact hole formed in the dielectric film; alternatively, the dielectric film may be omitted. The junction region (102) can be formed by implanting impurities using a conventional ion implantation process. In the situation of a DRAM, the junction region (102) becomes the source/drain; in the situation of a flash memory device, the junction region (102) becomes the drain.

[0017] The etch stop film (106) is formed on the semiconductor substrate (100) along the surface of the gates (G) and the gate spacers (104), and may be formed as a nitride film. For that reason, the etch stop film (106) is conventionally called an SAC (Self Align Contact) nitride film. The first interlayer insulating film (108) can be formed as an oxide film and is formed by depositing the first interlayer insulating film (108) on top of the etch stop film (106) and then performing planarization etching until the etch stop film (106) is exposed. The planarization etching can be performed by a chemical mechanical polishing (CMP) process.

[0018] Referring to FIG. 1b, a second interlayer insulating film (110) is formed above the etch stop film (106) and the first interlayer insulating film (108). The second interlayer insulating film (110) can be formed as a laminated structure in which a middle insulating film that has an etching selectivity different from those of the upper and lower insulating films is inserted between these insulating films and preferably can be formed as a laminated structure having a lower oxide film (110a), a nitride film (110b), and an upper oxide film (110c).

[0019] The nitride film (110b) is subsequently formed so as to have a sidewall profile in which the nitride film (110b) protrudes farther than the lower and upper oxide films (110a, 110c) as a result of the difference in etch rates between the films, which creates an overhang on the sidewall of the nitride film (110b) in the contact hole when the metal barrier layer is deposited, thereby closing the seam inside the tungsten film in the vicinity of the overhang that is created when the tungsten (W) film is deposited to fill the contact hole; its purpose is to serve as a polishing stop film during the subsequent CMP process.

[0020] The interlayer insulating film (110) is formed by sequentially depositing a lower oxide film (110a), a nitride film (110b), and an upper oxide film (110c). When forming the second interlayer insulating film (110) having the structure described above, rather than the oxide film being deposited all at once as in the past, instead it is deposited in two separate stages.

[0021] Referring to FIG. 1c, a hard mask film (112) is formed above the second interlayer insulating film (110). The hard mask film (112) is intended to be used as an etching mask when forming a subsequent contact hole, and can be formed of an oxide, a nitride, or the like.

[0022] Referring to FIG. 1d, a hard mask film (112 in FIG. 1c) is etched by an etching process using a mask (not shown) to form a hard mask film pattern (not shown). The mask is then removed. Then, using the hard mask film pattern as a mask, the second interlayer insulating film (110), the first interlayer insulating film (108), and the etch stop film (106) are each etched in sequence to form a contact hole (114) that exposes the junction region (102) between the gates (G). In this situation, the contact hole (114) has a large aspect ratio because it is formed penetrating through the first and second interlayer insulating films (110, 108). In the situation of a flash memory device, the contact hole (114) becomes a drain contact hole. In the course of forming a contact hole (114), the hard mask film pattern can also be removed by etching; if residue remains, it is removed.

[0023] The contact hole (114) can also be formed without removing the mask after etching the hard mask film (112 in FIG. 1c); in such a situation, the mask can be removed or part of it can be etched in the course of forming the contact hole (114), and part of the hard mask film pattern can be etched. If any portions of the mask and the hard mask film pattern remain, they are removed.

[0024] Referring to FIG. 1e, a metal barrier layer deposition pre-cleaning process is performed. The metal barrier layer deposition pre-cleaning process can be performed using a buffered oxide etchant (BOE) or a hydrofluoric acid (HF) solution.

[0025] During the metal barrier layer deposition pre-cleaning process, the sidewall of the nitride film (110b) inside the contact hole (114) is etched to a lesser extent than the sidewalls of the lower and upper oxide films (110a, 110c), owing to the difference in the wet etch rate between the nitride film (110b) and the lower and upper oxide films (110a, 110c). Accordingly, the contact hole (114) has a sidewall profile in which the nitride film (110b) protrudes farther than the lower and upper oxide films (110a, 110c).

[0026] Referring to FIG. 1f, the metal barrier layer (116) is formed on the second interlayer insulating film (110), which has the contact hole (114) having a sidewall profile in which the nitride film (110b) protrudes farther than the lower and upper oxide films (110a, 110c). The metal barrier layer (116) can be formed as a Ti/TiN laminated structure in the manner of a liner, using a conventional physical vapor deposition (PVD) method or the like. In this situation, owing to the protruding nitride film (110b) on the sidewall of the contact hole (114), the metal barrier layer (116) has an overhang (A) on the sidewall in the contact hole (114) corresponding to the protruding nitride film (110b).

[0027] Referring to FIG. 1g, the metal layer (118) is formed on top of the metal barrier layer (116) having the contact hole (114), so that the contact hole (114) is filled. Preferably, the metal layer (118) can be formed of tungsten (W).

[0028] In general, if a contact hole with a large aspect ratio is filled with tungsten, an overhang is created due to the characteristics of the deposition, and the tungsten film comes into contact with the opposite sidewalls of the contact hole, thereby creating a seam inside the tungsten film.

[0029] However, in an embodiment of the present invention, the seam (120) in the tungsten film is closed near the overhang (A) of the sidewall of the protruding nitride film (110b) in the contact hole (114), and therefore the seam (120) in the tungsten film is ultimately formed with a separate lower seam (120a) and upper seam (120b), respectively above and below the overhang formed in the metal barrier layer (116).

[0030] Referring to FIG. 1h, the metal layer (118 in FIG. 1g), the metal barrier layer (116), and the upper oxide film (110c of FIG. 1g) of the second interlayer insulating film (110) have been etched so that the nitride film (110b) of the second interlayer insulating film (110) is exposed. The etching process can be performed by a CMP process.

[0031] Thereby, the metal layer (not shown) remaining inside the contact hole (114) is formed into a contact plug (118a), and only the lower seam (120a) is present inside the contact plug (118a). In other words, the upper seam (120b) is removed in the course of etching the upper oxide film (110c in FIG. 1g) and the metal layer (118 in FIG. 1g) to form the contact plug (118a). Additionally, the metal barrier layer (116) remains on the sidewall and on the bottom surface of the contact hole (114).

[0032] In particular, according to an embodiment of the present invention, because the seam (120 in FIG. 1g) in the metal layer (118 in FIG. 1g) is closed in the vicinity of the overhang (A) of the sidewall of the protruding nitride film (110b) in the contact hole (114), the seam (120 in FIG. 1g) is not exposed when performing the CMP process to form the contact plug (118a).

[0033] After the CMP process is performed, it is common to perform post-CMP cleaning to remove foreign matter such as CMP residue or particles; as described above, if the seam (120 in FIG. 1g) in the metal layer (118 in FIG. 1g) is not exposed during the CMP process, the lower seam (120a) inside the contact plug (118a) can be prevented from becoming exposed and increasing in size during the subsequent post-CMP cleaning process. Accordingly, it is possible to inhibit an increase in the resistance of the contact plug (118a) and bridging between contact plugs (118a) due to the intrusion of foreign matter such as CMP residue or particles into the lower seam (120a), thereby improving process yield and device reliability.

[0034] The method of manufacturing a semiconductor device according to an embodiment of the present invention is applicable to all devices that use tungsten in manufacturing a plug having a large aspect ratio.

[0035] The present invention is not limited to the embodiments set forth above, but can be realized in various different forms; the above embodiments are presented only to complete the disclosure of the present invention and to fully inform a person of ordinary skill in the art of the scope of the invention. Accordingly, the scope of the present invention must be construed in accordance with the claims in the present application.

Brief Description of the Drawings

[0036] FIGS. 1a through 1h are process cross-sections illustrating a method of manufacturing a semiconductor device according to an embodiment of the present invention.

- [0037] <Explanation of Principal Elements of the Drawings>
 [0038] 100: Semiconductor substrate 102: Junction region
 [0039] 104: Gate spacer 106: Etch stop film
 [0040] 108: First interlayer insulating film 110: Second interlayer insulating film
 [0041] 110a: Lower oxide film 110b: Nitride film
 [0042] 110c: Upper oxide film 112: Hard mask film
 [0043] 114: Contact hole 116: Metal barrier layer
 [0044] 118: Metal layer 118a: Contact plug
 [0045] 120: Seam 120a: Lower seam
 [0046] 120b: Upper seam

Drawings

FIG. 1a

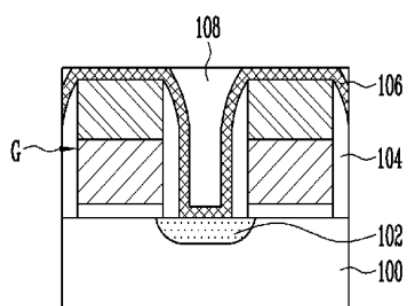


FIG. 1b

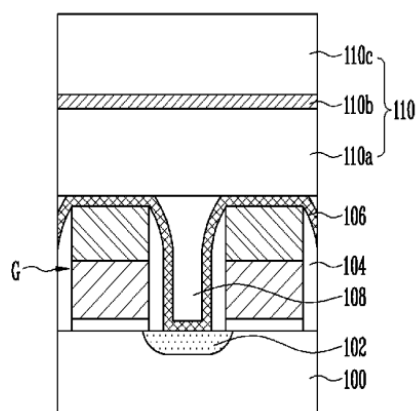


FIG. 1c

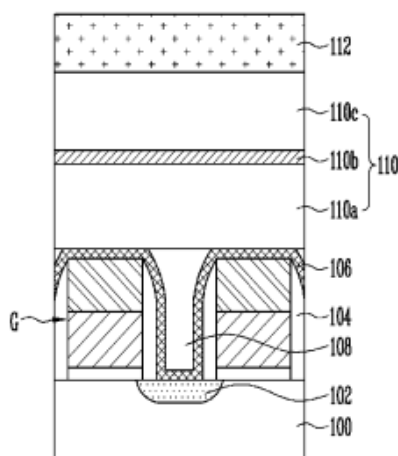


FIG. 1d

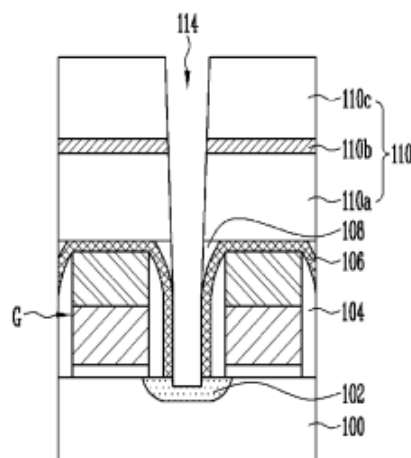


FIG. 1e

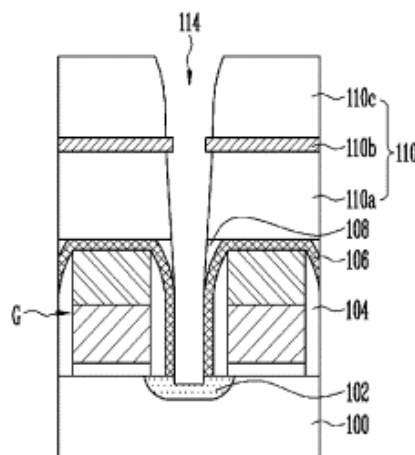


FIG. 1f

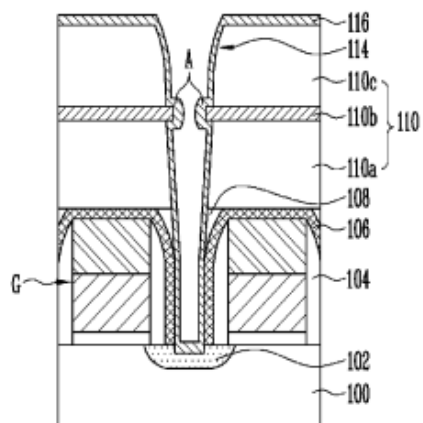


FIG. 1g

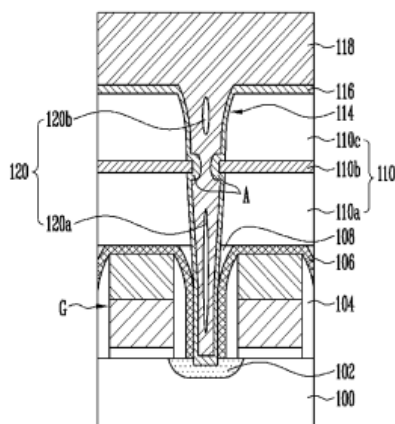
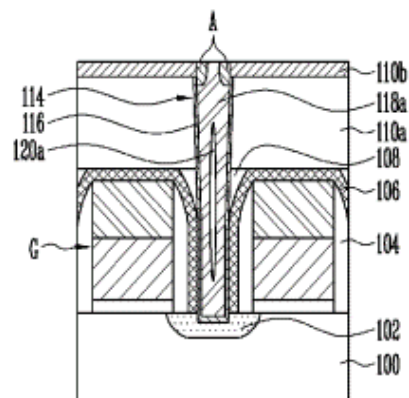


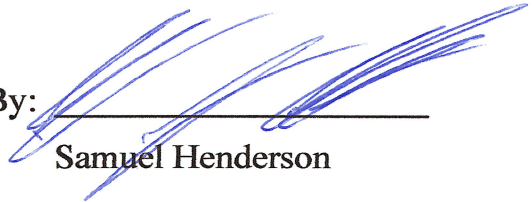
FIG. 1h



I, Samuel Henderson, declare as follows:

1. I am over 21 years of age and am competent to make this declaration.
2. I am a native speaker of English.
3. I am fluent in Korean.
4. I have 13 years of experience translating Korean to English.
5. I translated the attached patent document "KR20100011480A" from Korean to English.
6. I certify that the translation of the document "KR20100011480A" is, to the best of my knowledge, a true and accurate translation from Korean to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed: September 11, 2024

By: 

Samuel Henderson