

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

Case IPR2024-01404
Patent No. 9,147,609

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,147,609 to Jebory et al. (“’609 patent”)
Ex. 1002	Declaration of Scott Thompson, Ph.D. (“Thompson”)
Ex. 1003	Prosecution History of the ’609 patent (downloaded from Public PAIR)
Ex. 1004	U.S. Patent Publication No. 2009/0278237 to Cooney, III et al., filed May 6, 2008, and published November 12, 2009 (“ <i>Cooney</i> ”)
Ex. 1005	U.S. Patent Publication No. 2003/111733 to Pogge et al., filed December 19, 2001, and published June 19, 2003 (“ <i>Pogge</i> ”)
Ex. 1006	U.S. Patent Publication No. 2006/0027934 to Edelstein et al., filed October 3, 2005, and published February 9, 2006 (“ <i>Edelstein</i> ”)
Ex. 1007	U.S. Patent Publication No. 2011/0304026 to Tsui et al., filed June 14, 2010, and published December 15, 2011 (“ <i>Tsui</i> ”)
Ex. 1008	U.S. Patent Publication No. 2011/0159690 to Chandrashekar et al., filed January 28, 2011, and published June 30, 2011 (“ <i>Chandrashekar</i> ”)
Ex. 1009	U.S. Patent Publication No. 2011/0193241 to Yen et al., filed February 9, 2011, and published August 11, 2011 (“ <i>Yen</i> ”)
Ex. 1010	U.S. Patent Publication No. 2011/0057319 to Dean, Jr. et al., filed September 9, 2009, and published March 10, 2011 (“ <i>Dean</i> ”)
Ex. 1011	U.S. Patent Publication No. 2010/0032843 to Chen et al., filed August 5, 2008, and published February 11, 2010 (“ <i>Chen</i> ”)
Ex. 1012	KR 10-2010-0011480, filed on July 25, 2008, and published February 3, 2010
Ex. 1013	Certified English language translation of KR 10-2010-0011480, filed on July 25, 2008, and published February 3, 2010 (“ <i>Kim</i> ”)
Ex. 1014	Scott R. Stiffler et al., The Effect of Trench Corner Shapes on Local Stress Fields: A Three-Dimensional Finite Element Modeling Study, IEEE Transactions on Electron Devices, March 1993 (“ <i>Stiffler</i> ”)
Ex. 1015	Reserved
Ex. 1016	U.S. Patent No. 8,237,288 to Farooq et al. (“ <i>Farooq</i> ”)
Ex. 1017	U.S. Patent Publication No. 2012/0139127 to Beyne, filed December 2, 2011, and published June 7, 2012 (“ <i>Beyne</i> ”)
Ex. 1018	U.S. Patent Publication No. 2011/0237073 to Dao et al., filed March 26, 2010, and published September 29, 2011 (“ <i>Dao</i> ”)

Exhibit	Description
Ex. 1019	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Plaintiff’s Infringement Contentions Cover Pleading (July 18, 2024)
Ex. 1020	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)
Ex. 1021	U.S. Patent Publication No. 2009/0140395 to Davis et al., filed December 4, 2007, and published June 4, 2009 (“ <i>Davis</i> ”)
Ex. 1022	U.S. Patent Publication No. 2009/0302480 to Birner et al., filed June 6, 2008, and published December 10, 2009 (“ <i>Birner</i> ”)
Ex. 1023	U.S. Patent Publication No. 2008/0318361 to Han et al., filed July 13, 2007, and published December 25, 2008 (“ <i>Han</i> ”)
Ex. 1024	U.S. Patent Publication No. 2010/0171226 to West et al., filed December 29, 2009, and published July 8, 2010 (“ <i>West</i> ”)

I. PRELIMINARY STATEMENT

Petitioner, Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively “Samsung”), requests *inter partes* review of U.S. Patent No. 9,147,609 (“the ’609 patent”) (Ex. 1001), assigned to Patent Owner Harbor Island Dynamic, LLC (“HID”), and cancellation of claims 1-18.

The ’609 patent relates to semiconductor substrates, and specifically the structure of through silicon vias in a semiconductor substrate. ’609 patent, 1:54-56. The purported invention is a through silicon via (TSV) that includes a “hollow center portion” that serves to provide space for a conductive filler in the TSV “to expand inward rather than outward in high temperature conditions” and thus reduce potential thermal and mechanical stress in the substrate. *Id.*, 4:47-66. The ’609 patent also includes claims directed to orienting adjacent TSVs perpendicular to each other to purportedly reduce substrate cracking and to having chamfered corners in the TSVs to purportedly reduce thermal and mechanical stress in the substrate. *Id.*, 3:44-57.

Notably, the Examiner did not allow the claims based on the above-identified features. Ex. 1003, 21, 83-97. Instead, after a lengthy prosecution, the Examiner allowed the claims because the prior art allegedly failed to disclose the “pinched off region[s],” as recited in independent claims 1 and 13. *Id.*, 21. All these features, including those noted by the Examiner, were known in the prior art,

however. For example, U.S. Patent Publication No. 2009/0278237 (“*Cooney*”) (Ex. 1004) discloses TSVs with pinched off regions at the top and bottom portions, along with an enclosed void that is tapered in the bottom portion of the TSV. U.S. Patent Publication No. 2011/0057319 (“*Dean*”) (Ex. 1010) discloses arranging adjacently located sets of TSVs perpendicular to each other to reduce substrate cracking. And U.S. Patent Publication No. 2010/0032843 (“*Chen*”) (Ex. 1011) discloses TSVs with chamfered corners. None of these references were before the Examiner during prosecution of the ’609 patent.

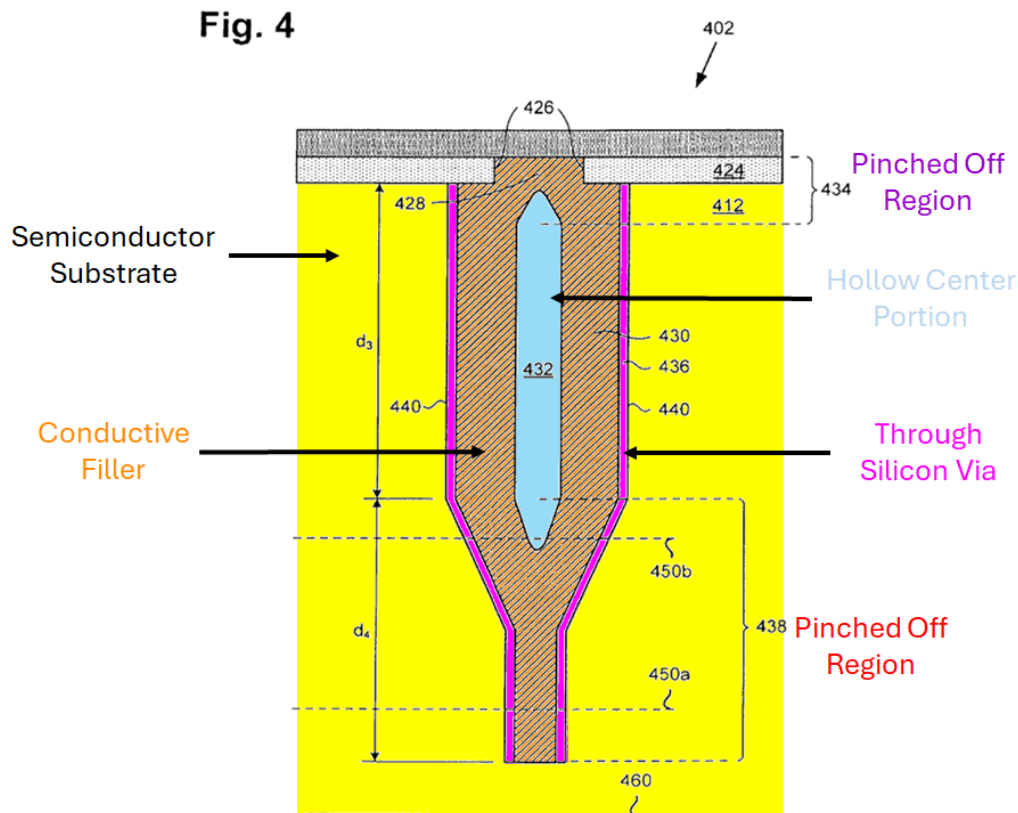
As detailed below and in the supporting declaration of Scott Thompson, Ph.D., Thompson, ¶¶1-266, Claims 1-6, 9-14, 17, and 18 of the ’609 patent are anticipated by or would have been obvious over *Cooney*, and the remaining claims 7, 8, 15, and 16 would have been obvious over *Cooney* in view of *Dean* or *Chen* in view of *Cooney*. The Board should thus institute review and cancel all challenged claims.

II. THE ’609 PATENT

A. Alleged Invention

The ’609 patent relates to “through silicon via structure, method of formation, and integration in semiconductor substrate.” ’609 patent, 1:54-56. Specifically, the ’609 patent discloses “a through silicon via having a pinched off region such as, for example, TSV 402,” formed in **substrate 412**. *Id.*, 4:14-18.

Annotated Figure 4 of the '609 patent, below, illustrates some of the disclosed features of TSV 402. *Id.*, Fig. 4; Thompson, ¶¶51-55, 57.



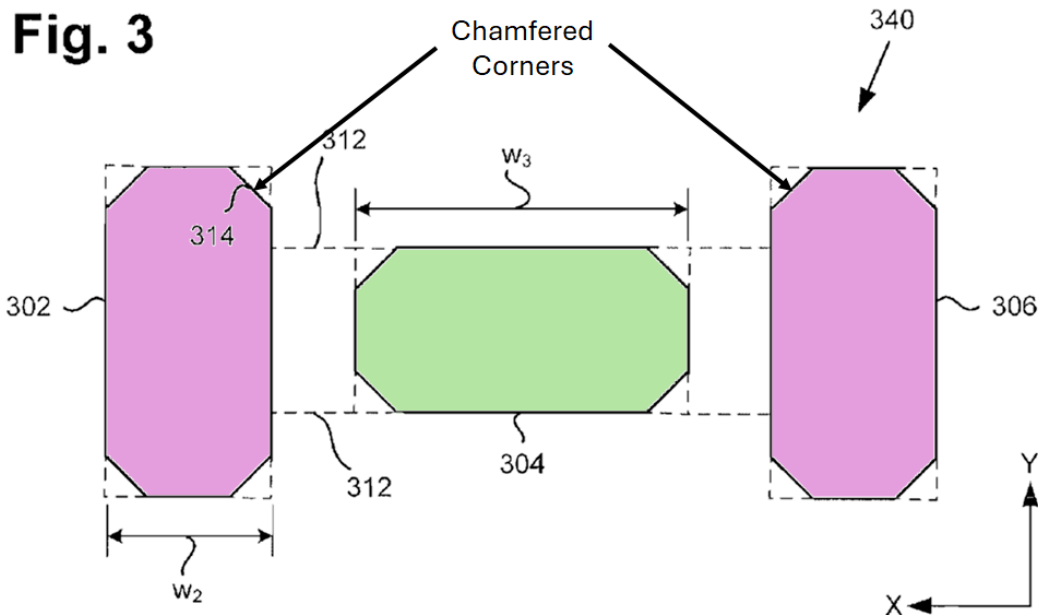
'609 patent, Fig. 4 (annotated)

As illustrated in Figure 4, the '609 patent's **through silicon via (TSV) 402** (from top to bottom) includes a "**pinched off region 434**," a "**hollow center portion 432**," and a "**pinched off region 438**." '609 patent, 4:47-50, 5:3-5.

In fabricating such a **TSV 402**, sidewalls 440 are first formed to a first depth d_3 , then the **pinched off region 438** is formed "from first depth d_3 to second depth d_4 ." *Id.*, 4:23-25. A "**conductive filler 430**" is next deposited on the sidewalls 440 of the **TSV 402** to form the "**hollow center portion 432** and **pinched off region**

438.” *Id.*, 4:47-50. An “oxide layer 424 may be deposited over the top surface of substrate 412” to form an “opening 428 . . . over TSV 402, such that . . . the width of opening 428 [is] smaller than the width of TSV 402.” *Id.*, 5:9-14. “Depositing oxide layer 424 and forming opening 428 ensures pinched off region 434 is formed in the top region of TSV 402, and that hollow center portion 432 does not extend to the top of TSV 402.” *Id.*, 5:14-16; Thompson, ¶55.

According to the ’609 patent, the hollow center portion 432 “reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions,” which further “reduces cracking in substrate 412.” *Id.*, 4:62-67; Thompson, ¶56. To further reduce thermal and mechanical stress in the substrate, the ’609 patent discloses arranging the TSVs, as shown below, so “each TSV in an array may be oriented at a 90° angle relative to an adjacent TSV” to “interrupt[] naturally forming cleavage planes [] caused by thermal and mechanical stresses in the substrate.” *Id.*, 3:53-57.



'609 patent, Fig. 3 (annotated)

Annotated Figure 3 of the '609 patent illustrates such arrangement where the TSVs 302 and 306 are arranged in a “width direction” while the TSV 304 is disposed between the TSVs 302 and 306 in a “length direction.” *Id.*, 3:46-52; Thompson, ¶¶58-60. Further, the '609 patent discloses chamfering “at least one corner of each of TSVs” and preferably “each corner of each TSV” to further reduce thermal and mechanical stress. *Id.*, 3:58-61.

B. Prosecution History

U.S. Application No. 13/415,744, which issued as the '609 patent, was filed on March 8, 2012, with 20 claims and claimed priority to U.S. Provisional Application No. 61/545,003, which was filed on October 7, 2011. Ex. 1003, 286, 295, 307-311. During prosecution, the '744 application initially received a

restriction requirement. *Id.*, 273-277. In response, Applicant cancelled two claims. *Id.*, 260-264; Thompson, ¶63.

Subsequently, the remaining claims were twice rejected over Applicant's Admitted Prior Art ("AAPA") based on Figures 1A and 1B of the as-filed application in view of U.S. Patent Publication No. 2012/0139127 ("*Beyne*") (Ex. 1017) alone or in further view of U.S. Patent Publication No. 2011/0237073 ("*Dao*") (Ex. 1018). Ex. 1003, 193-206, 144-157. Without disputing that "Beyne discloses (10B-H) each of said plurality of through silicon vias (10b) having a hollow center (4) to reduce thermal stress in said semiconductor substrate," (*id.*, 194, 176-183, 144-145, 129-137, 111-119), Applicant first amended independent application claims 1 and 13 to recite "said hollow center being surrounded by said conductive filler" (*id.*, 172, 174) and subsequently amended those claims to additionally require the hollow center being "entirely" surrounded by the conductive filler "to provide space for said conductive filler to expand inward" (*id.*, 107, 109). Thompson, ¶¶64-65

The Examiner remained unconvinced and rejected application claims 1-10 and 13-20 based on AAPA in view of *Beyne* and U.S. Patent Publication No. 2005/0121768 ("*Edelstein*") (Ex. 1006), or further in view of *Dao*. Ex. 1003, 83-97. Again, without disputing that "Edelstein discloses Fig. 2b and 6d-f: Said hollow center (220) being entirely surrounded by said conductive filler (225) to

provide space for said conductive filler to expand inward” or that “Edelstein discloses that providing the hollow portion 220 provides the benefit of reducing thermal stresses on the substrate,” (*id.*, 88, 70-77), Applicant instead amended independent application claim 1 to additionally recite “said hollow center is tapered in said pinched off region” and independent application claim 13 to additionally recite that each of the plurality of through silicon vias has a pinched off region at a top portion “and another pinched off region at a bottom portion” and “said hollow center is tapered in said another pinched off region.” *Id.*, 65, 67; Thompson, ¶66.

As a result, the Examiner allowed application claims 1-10 and 13-20, (*id.*, 21), and provided the following reasons for allowance based on the prior art then known to the Examiner:

[T]he prior art fails to disclose and would not have rendered obvious:

each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region, as recited in claim 1;

and

each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region, as recited in claim 13.

Id.; Thompson, ¶67.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.¹

III. STATEMENT OF PRECISE RELIEF REQUESTED

A. Prior Art

- Ex. 1004, U.S. Patent Application Publication No. 2009/0278237 (“*Cooney*”), published November 12, 2009, is prior art to the ’609 patent under §§ 102(a), (b), and (e).

¹ Petitioner reserves the right to argue in an appropriate forum that certain limitations in the challenged claims are indefinite.

- Ex. 1010, U.S. Patent Application Publication No. 2011/0057319 (“*Dean*”), published March 10, 2011, is prior art to the ’609 patent under §§ 102(a) and (e).
- Ex. 1011, U.S. Patent Application Publication No. 2010/0032843 (“*Chen*”), published February 10, 2010, is prior art to the ’609 patent under §§ 102(a), (b), and (e).
- Ex. 1016, U.S. Patent No. 8,237,288 (“*Farooq*”), filed February 9, 2011, and issued August 7, 2012, is prior art to the ’609 patent under §§ 102(a) and (e).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1A	1-6, 9-14, 17, and 18	§102	<i>Cooney</i>
1B	1-6, 9-14, 17, and 18	§103	<i>Cooney</i>
2	7 and 15	§103	<i>Cooney and Dean</i>
3	8 and 16	§103	<i>Cooney and Farooq</i>
4	8 and 16	§103	<i>Chen and Cooney</i>

IV. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) at the time of the purported invention of the ’609 patent (October 7, 2011) would have had at least a master’s degree in electrical engineering or a similar field and at least two years of

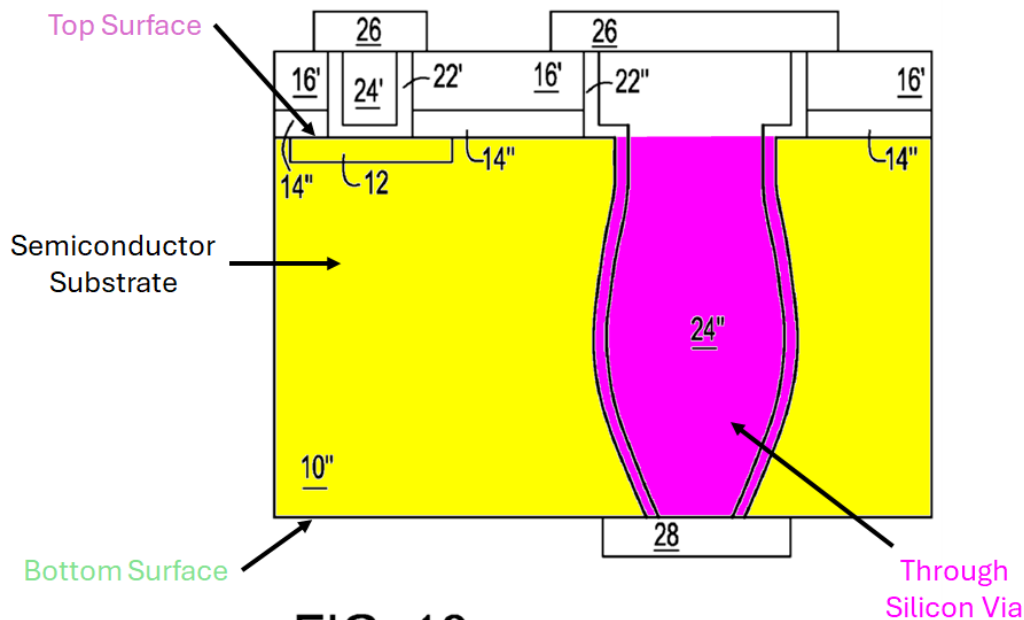
experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and *vice versa*. Thompson, ¶¶72-74.

V. CLAIMS 1-18 ARE UNPATENTABLE

A. Claims 1-6, 9-14, 17, and 18 Are Anticipated (Ground 1A) or Rendered Obvious by *Cooney* (Ground 1B)

1. Overview of *Cooney*

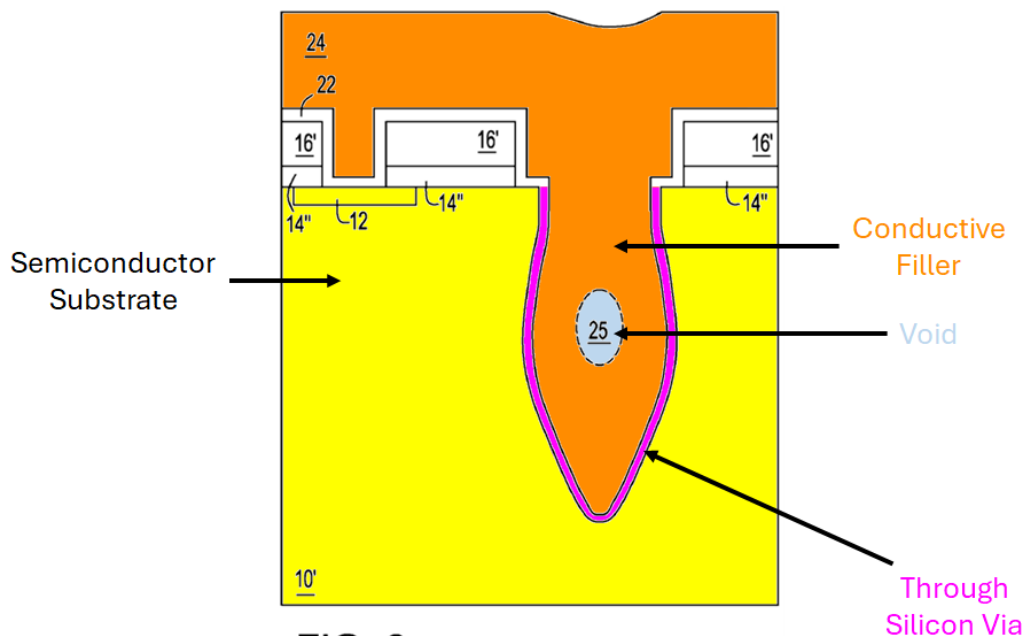
Cooney discloses a “microelectronic structure, such as a semiconductor structure, and a method for fabricating the microelectronic structure[.]” *Cooney*, Abstract. Specifically, *Cooney* discloses a semiconductor substrate 10 that includes a contact region 12. *Cooney*, ¶[0026]; Fig. 1.



Cooney, Fig. 10 (annotated).

In addition to the contact region, *Cooney*'s "substrate 10 will also include located and formed therein semiconductor devices that are appropriate for a semiconductor circuit"; such semiconductor devices may include, but are not necessarily limited to, resistors, transistors, diodes and capacitors. *Cooney*, ¶[0032]. As illustrated in Figure 10, *Cooney* discloses a through substrate via 24" that penetrates from a front side (e.g., top surface) of a semiconductor substrate 10" to a backside (e.g., bottom surface) of the semiconductor substrate 10". *Id.*, ¶[0065]; Fig. 10.

Cooney discloses that the through substrate via 24" has "a downward pointing torpedo shape." *Cooney*, ¶[0042]. A liner layer 22 is "formed conformally" upon the semiconductor structure, "incompletely filling the extended aperture." *Id.*, ¶[0055]. As illustrated in Figure 6, below, *Cooney* further discloses "a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture." *Id.*



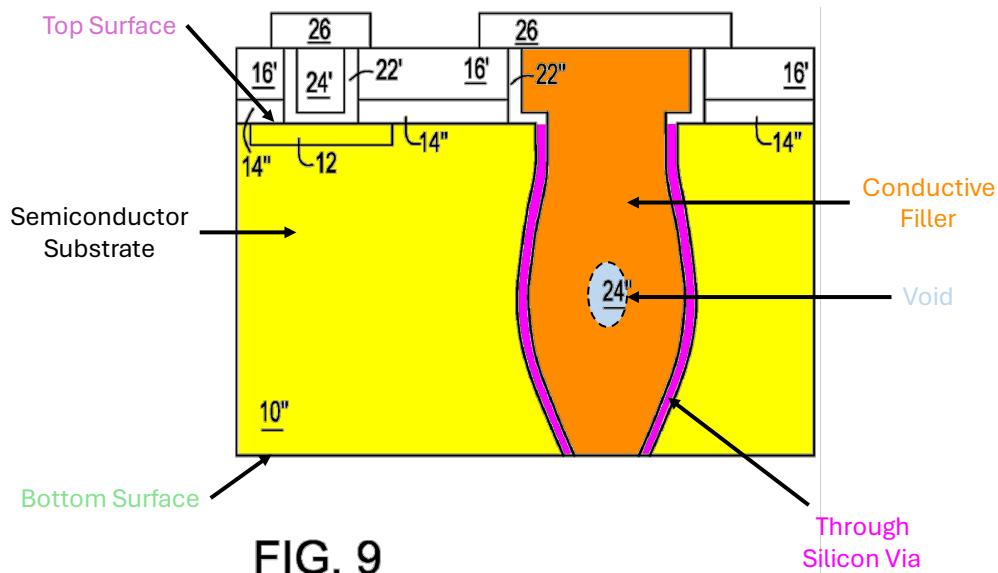
Cooney, Fig. 6 (annotated).

The “conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys,” and “typically comprises a tungsten material.” *Cooney*, ¶[0059]; Thompson, ¶¶76-84.

Cooney further discloses “backside planarizing of the semiconductor substrate 10', the liner layer 22' and the conductor layer 24' ... to remove a thickness from about 0.1 to about 10 microns from the semiconductor substrate 10' while leaving exposed portions of both the liner layer 22'' and the conductor layer 24''.” *Cooney*, ¶[0063]. *Cooney*'s backside planarizing may include “mechanical polish planarizing methods and chemical mechanical polish planarizing methods.” *Id.* Figure 9 of *Cooney*, below, illustrates the semiconductor substrate 10'', liner

layer 22" and conductor layer 24" that result from a backside planarizing. *Id.*;

Thompson, ¶85.



Cooney, Fig. 9 (annotated and modified to include the void as shown in Fig. 6).

Cooney's "FIG. 1 to FIG. 10 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in fabricating a microelectronic structure in accordance with a particular embodiment of the invention." *Cooney*, ¶[0025]. Thus, features such as a substrate, TSV, conductor layer, void, shown in one figure of *Cooney* correspond to similar structures shown in other figures of *Cooney*. Thompson, ¶86. For example, elements labeled 10, 10', 10'' correspond to the same substrate, and similarly, elements labelled 24, 24', and 24'' correspond to the same conductor layer. *Id.* Moreover, because Figures 4-8 illustrate intermediate steps in fabricating *Cooney*'s TSV, the TSV shown in

Figures 4-8 does not extend from the top surface to the bottom surface of the semiconductor substrate. *Id.* This is similar to Figure 4 of the '609 patent, in which TSV 402 does not extend from the top surface of substrate 412 to a bottom surface of substrate 412. '609 patent, Fig. 4; Thompson, ¶87. Instead, the '609 patent discloses “polishing bottom surface 460 of substrate 412 to expose conductive filler 430 from the bottom surface of the substrate” as the final step 540 in manufacturing substrate 412. '609 patent, 5:18-21, Fig. 5. Similarly, Figures 9 and 10 of *Cooney* illustrate *Cooney*'s TSV extending from the top surface to the bottom surface of substrate 10 after backside planarizing to expose the TSV. *Cooney*, ¶[0063]; Thompson, ¶87.

Moreover, according to *Cooney*, “a multiplicity of dimensionally similar or dimensionally identical apertures and corresponding **vias** may also be used within a single substrate[.]” *Cooney*, ¶[0066]; *see also id.*, Abstract, ¶¶[0018], [0020]; Thompson, ¶79. Thus, while each of Figures 1-10 of *Cooney* illustrates a single **TSV**, *Cooney*'s **substrate 10** may include a plurality of **TSVs**. *Id.* Accordingly, the features discussed in *Cooney* with reference to Figures 1-10 as discussed below apply to each of the TSVs in *Cooney*.

Cooney is analogous art to the '609 patent because *Cooney*, like the '609 patent, discloses a method of fabricating a microelectronic structure such as a TSV in a substrate. *Compare Cooney*, Abstract, ¶¶[0018]-[0020], [0023], [0026],

[0042]-[0043], [0051]-[0055], [0058]-[0060], *with* the '609 patent, Abstract, 1:54-56, 3:1-5, 4:9-5:24; Thompson, ¶88.

2. Independent Claim 1

Cooney discloses or would have rendered obvious every element of independent claim 1.

- a. [1pre]: “A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:”

To the extent the preamble is limiting, *Cooney* discloses a semiconductor substrate 10 that includes a contact region 12. *Cooney*, ¶[0026]; Fig. 1. In addition to the contact region, *Cooney*’s “substrate 10 will also include located and formed therein semiconductor devices that are appropriate for a semiconductor circuit ... such semiconductor devices may include, but are not necessarily limited to, resistors, transistors, diodes and capacitors.” *Id.*, ¶[0032]; Thompson, ¶¶110-111.

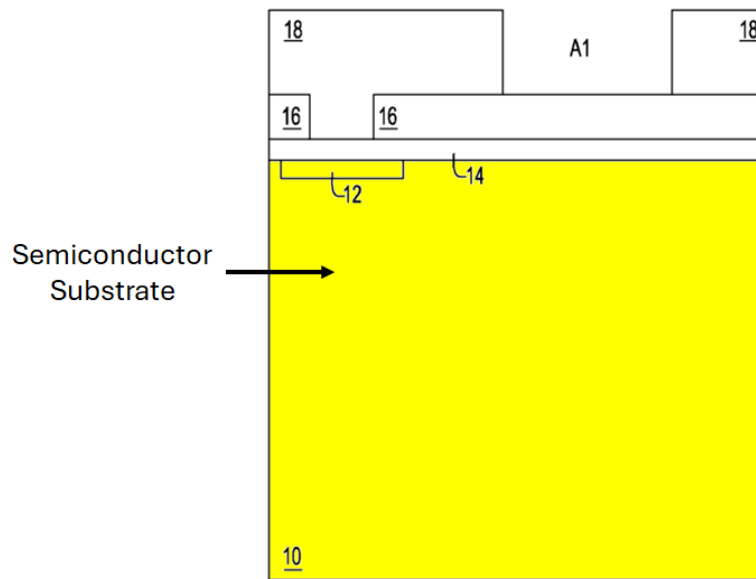
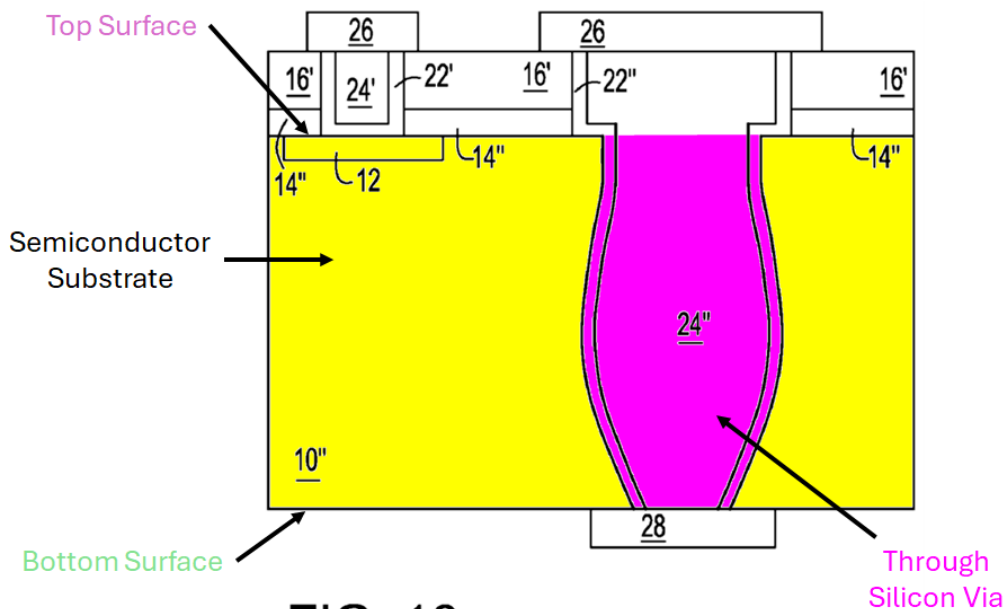


FIG. 1

Cooney, Fig. 1 (annotated).

- b. [1a]: “a plurality of **through silicon vias** disposed in said **substrate** extending from a **top surface** of said substrate to a **bottom surface** of said substrate;”

Cooney discloses a semiconductor structure that includes a **through substrate via 24** that penetrates from a **front side** (e.g., “**top surface**”) of a **semiconductor substrate 10** to a **backside** (e.g., “**bottom surface**”) of the **semiconductor substrate 10**. *Cooney*, ¶[0065]; Fig. 10. As discussed *supra* in § V.A.1, *Cooney* discloses a multiplicity of **TSVs** may be used within a single substrate, each of which extends from a **top surface** of said **substrate** to a **bottom surface** of the **substrate**. *Cooney*, ¶[0066]; Thompson, ¶¶112-115.



Cooney, Fig. 10 (annotated).

- c. [1b-1]: “a **conductive filler** disposed within each of said plurality of **through silicon vias**,”

Cooney discloses a **conductor layer** disposed within and filling the TSVs. Thompson, ¶¶116-119. *Cooney* discloses a liner layer 22 located and formed conformally and incompletely filling the extended aperture, (*Cooney*, ¶[0055]), and formed upon the liner layer 22, “a **conductor layer 24** with an optional void 25 located therein ... completely filling the **extended aperture**.” *Id.* Figure 6 of *Cooney* illustrates **conductor layer 24** that constitutes the conductive filler within the **TSV**, along with the void 25. Thompson, ¶118.

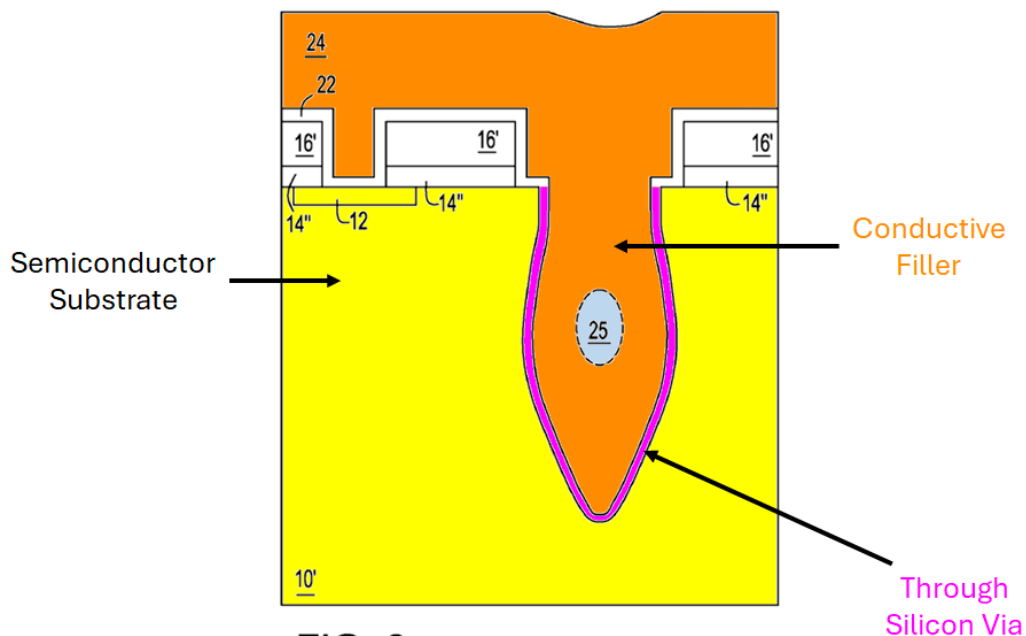


FIG. 6

Cooney, Fig. 6 (annotated).

Cooney explains that “the conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys.” *Cooney*, ¶[0059]. Because *Cooney*’s conductor layer 24 is made of metals or metal alloys, the conductor layer 24 is conductive. Thompson, ¶118. Further, *Cooney*’s conductor layer 24 is disposed within *Cooney*’s TSV because the conductor layer 24 fills the TSV in *Cooney*’s semiconductor substrate 10.

Thompson, ¶117. As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, each of which includes conductive filler (e.g., conductor layer 24) disposed within the respective TSV. Thompson, ¶119.

- d. [1b-2]: “each of said plurality of **through silicon vias** having a **hollow center** to reduce thermal stress in said **semiconductor substrate**,”

As discussed earlier for limitation [1b-1], *Cooney* teaches that each of the plurality of TSVs has a hollow center. Thompson, ¶¶120-134. For example, *Cooney* discloses that each **TSV** has “an optional **void 25** located therein.” *Cooney*, ¶[0055]; *see also id.*, Abstract, ¶[0051]. As *Cooney* explains, “the **conductor layer 24** may be deposited or formed with a **void 25**,” as illustrated by the **phantom line enclosure** within the below schematic diagram of FIG. 6. *Id.*, ¶[0060].

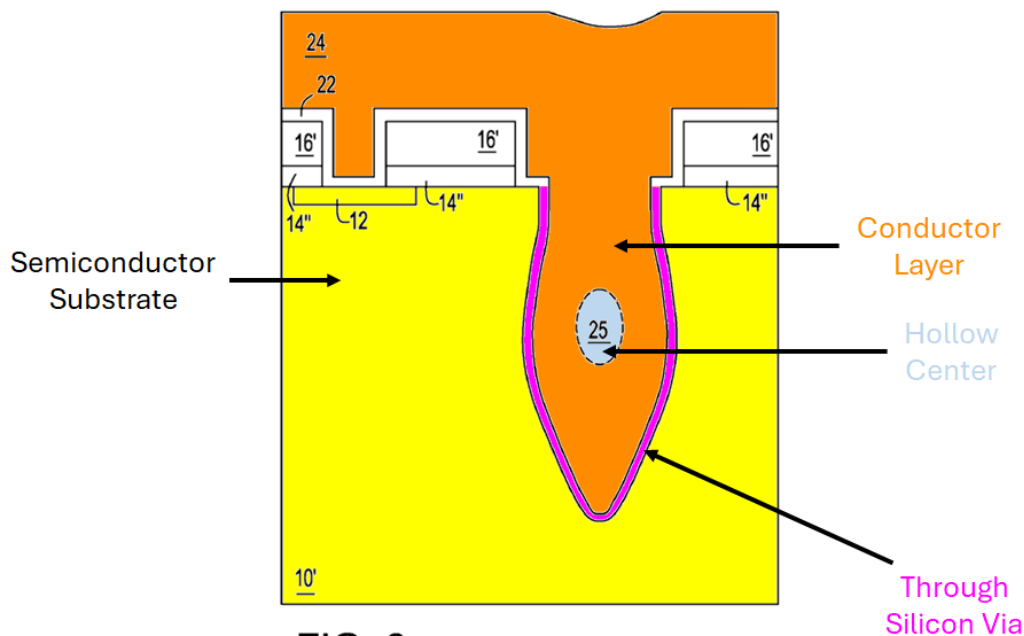


FIG. 6

Cooney, Fig. 6 (annotated).

Cooney's void 25 constitutes the claimed hollow center. Thompson, ¶121.

Moreover, as discussed in § V.A.1, *supra*, each of the plurality of TSVs of *Cooney* may include void 25. Thompson, ¶122.

The phrase “to reduce thermal stress in said semiconductor substrate” states the use of or explanation for the hollow center and should be entitled to no patentable weight over the prior art. *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999) (holding that “a scientific explanation for the prior art’s functioning, does not render the old composition patentably new”); *In re Sinex*, 309 F.2d 488, 492 (C.C.P.A. 1962) (“The expression ‘for reconcentrating liquid dehydrating agents’ is merely a statement of intended use and does not qualify or distinguish the structural apparatus claimed over the reference.”); *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“[T]he recitation of a new intended use for an old product does not make a claim to that old product patentable.”). Other than disclosing the presence of a hollow center in the TSV, the ’609 patent does not identify any features of the hollow center that contribute to thermal stress reduction in the semiconductor substrate. *See generally* ’609 patent. Thompson, ¶123. This failing further supports the conclusion that this claim language should be entitled to no patentable weight over the prior art.

Even if HID argues otherwise, the analysis would still need to take into account *Cooney*'s TSV and its inclusion of a purposeful void 25 that mirrors the hollow center, in limitation [1b-2]. *Cooney*'s void 25, like the claimed hollow center would similarly reduce thermal stress in the semiconductor substrate.

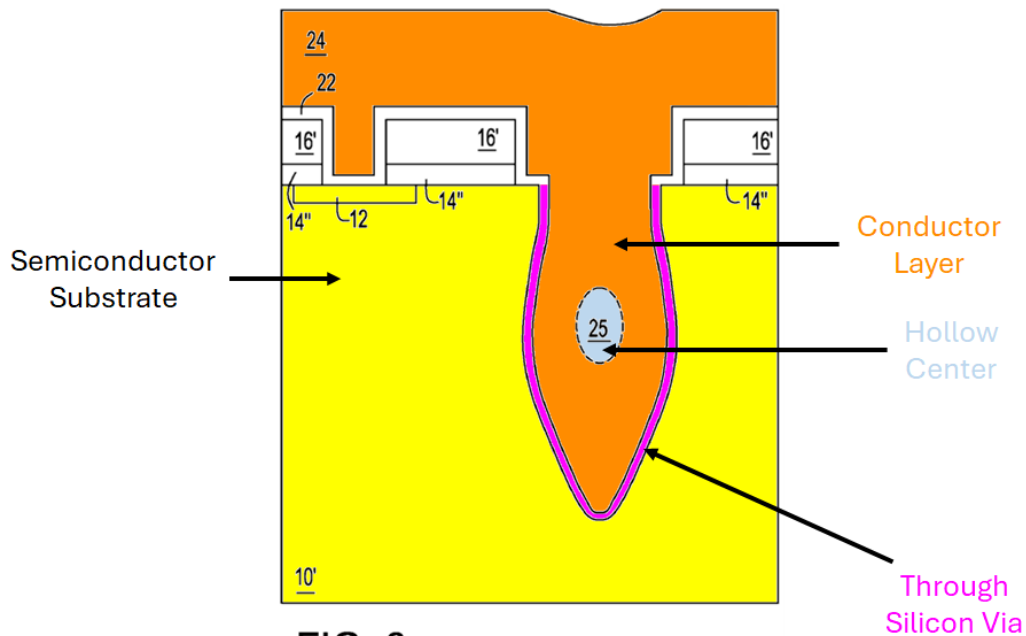
Thompson, ¶123. And at a minimum, a POSITA would have found it obvious to include *Cooney*'s void 25 to “reduce thermal stress in said semiconductor substrate,” as recited in limitation [1b-2], based on the POSITA's knowledge of the state of the art. *KSR Int'l. Co. v. Teleflex, Inc.*, 550 U.S. 398, 420-21 (2007) (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”); Thompson, ¶124. As Dr. Thompson explains, it was well known that the presence of a void in a filled TSV results in a lower amount of thermal stress in the surrounding substrate. Thompson, ¶125. For example, *Pogge* discloses that a void in a copper filled TSV “has an important function in relieving stress caused by differences in thermal coefficient of expansion (TCE) of the various materials in and around the feature.” *Pogge*, ¶[0027]; Thompson, ¶¶126-127. Similarly, *Edelstein* discloses that a “through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures.” *Edelstein*, ¶[0047]; Thompson, ¶¶128-131. And these very teachings were recognized during prosecution of the '609 patent. There, the Examiner cited *Edelstein* and *Bejne* for

the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate, and Patent Owner acquiesced to the rejection and did not rebut the Examiner’s statement. Section II.B; Thompson, ¶¶132.

In view of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials, if not explicitly disclosed, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*’s TSV to cause a reduction in the thermal stress in the surrounding substrate. Thompson, ¶133. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including the void. *Id.* Thus, *Cooney* discloses or at least would have rendered obvious limitation [1b-2] in view of the knowledge of a POSITA. *Id.*, ¶134.

- e. [1b-3]: “said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;”

In *Cooney*, the void 25 is entirely surrounded by the conductor layer 24 as illustrated in Figure 6, below. Thompson, ¶¶135-146.



Cooney, Fig. 6 (annotated).

As discussed earlier for limitation [1b-2], *Cooney* teaches “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Cooney*, ¶[0055]; *see also id.*, Abstract, ¶[0051]. *Cooney* discloses that the aperture has varying widths and comprises four regions R1, R2, R3, and R4 as illustrated in *Cooney*’s Figure 5 (below). *Cooney*, ¶¶[0049]-[0054], Fig. 5; Thompson, ¶136.

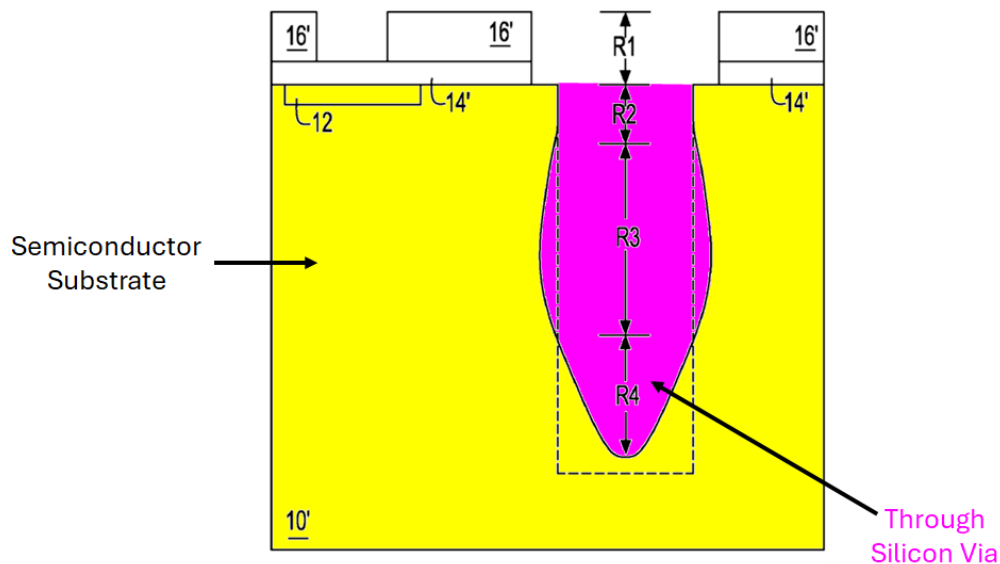


FIG. 5

Cooney, Fig. 5 (annotated).

Specifically, “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3 and to localize that void to the third region R3.” *Cooney*, ¶[0051]. Because *Cooney*’s conductive layer 24 fills the TSV and because the void is completely sealed off and localized in region R3, *Cooney* discloses a “hollow center” (e.g., void 25) that is entirely surrounded by the “conductive filler” (e.g., conductor layer 24). *Id.*; Thompson, ¶¶137-138.

The phrase “to provide space for said conductive filler to expand inward” states another use for the functioning of the hollow center and should be entitled to no patentable weight over the prior art. *Atlas Powder*, 190 F.3d at 1347; *Sinex*, 309 F.2d at 492; *Arctic Cat*, 919 F.3d at 1328. Again, other than disclosing the

presence of a hollow center in the TSV, the '609 patent does not identify any features of the hollow center in the TSV that purportedly allows the conductive filler in the TSV to expand inward. *See generally* '609 patent. Thompson, ¶139. Thus, the patent itself recognizes that this functional language should not be entitled to patentable weight.

Regardless, because *Cooney*'s TSV includes a purposeful void 25 akin to hollow center in limitation [1b-3], *Cooney*'s void 25, like the claimed hollow center would provide space for said conductive filler to expand inward. Thompson, ¶139. And even if HID were to contend otherwise, a POSITA would have found it obvious to include *Cooney*'s void 25 to “provide space for said conductive filler to expand inward,” as recited in limitation [1b-3], based on the POSITA's knowledge of the state of the art. *KSR*, 550 U.S. at 420-21; Thompson, ¶140. As Dr.

Thompson explains, it was well known that a via surrounded by substrate material expands inward. Thompson, ¶¶141-143. For example, *Tsui* discloses a TSV that is filled with a polymer material surrounded by copper on all sides. *Tsui*, ¶[0036] (“Preferably the via comprises an electroplated metal layer surrounding a polymer filler.”). *Tsui* further explains that “the filler layer has a degree of resilience”² and

² Resilience refers to how elastic a material is when exposed to various external stresses. Thompson, ¶143.

that when “the electro-plated layer expands, due to a change in temperature, this expansion can be accommodated by a ‘squashing’ of the filler layer.” *Id.*

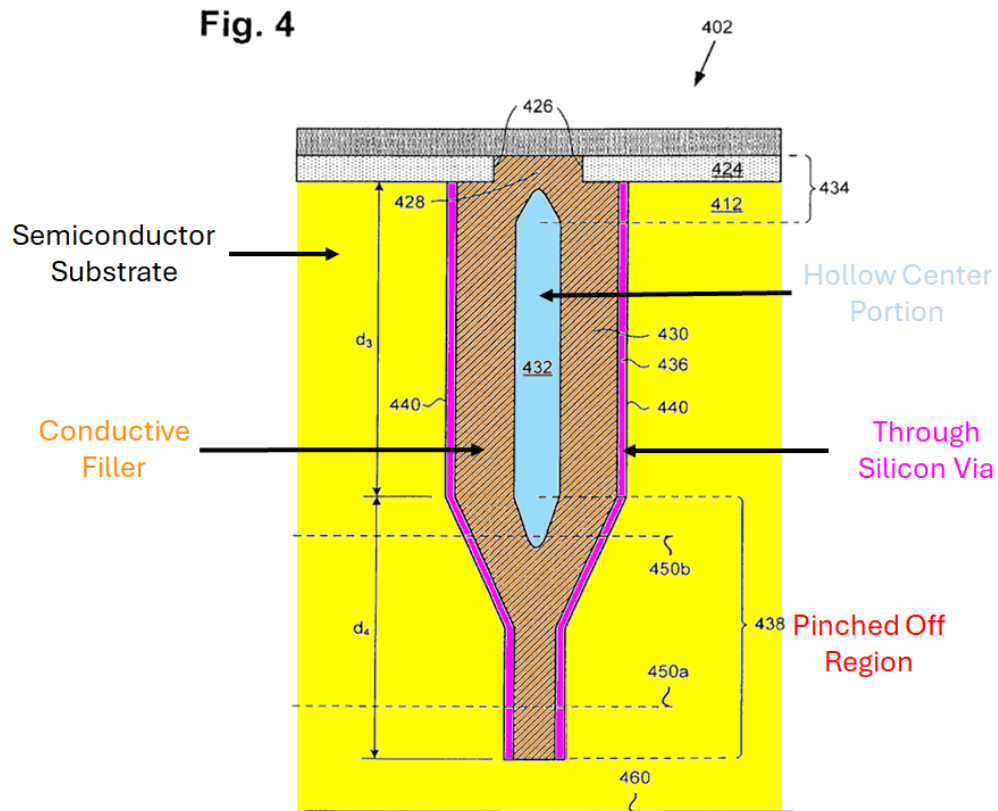
Given these teachings, a POSITA would recognize that a void (e.g., void 25 of *Cooney*) filled with gas would be significantly more resilient or elastic than *Tsui*’s polymer filler. Thompson, ¶144. Thus, *Cooney*’s conductive filler material in the TSV would more readily expand inward into the void 25 as compared to the expansion of the copper into *Tsui*’s polymer filler. Thompson, ¶144. According to Dr. Thompson, it would, therefore, have been obvious to a POSITA to include *Cooney*’s void 25 such that when *Cooney*’s TSV and substrate are subjected to an increase in temperature, the conductive filler in *Cooney* would expand inwardly, squashing the gas-filled void. *Id.*

In view of the well-known expansion behavior of conductive fillers, if not explicitly stated, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*’s TSV to allow *Cooney*’s conductor layer to expand inward into the void. Thompson, ¶145. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including a void in its conductor layer. *Id.* Thus, *Cooney* discloses or would have rendered obvious limitation [1b-3] in view of the knowledge of a POSITA. *Id.*, ¶146.

- f. [1c-1]: “wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**, and”

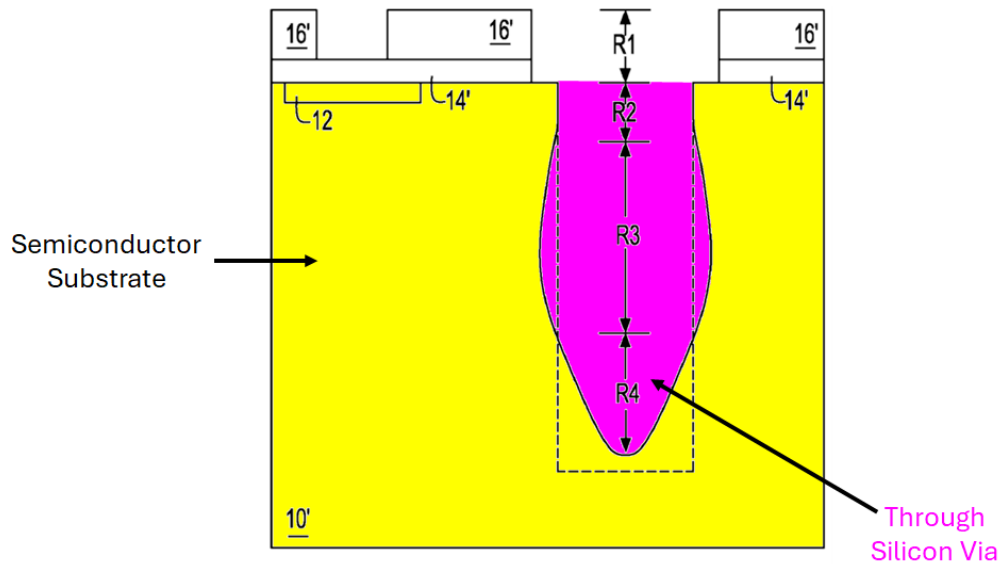
Cooney discloses that each of the plurality of TSVs has a pinched off region at a bottom portion. Thompson, ¶¶147-164.

The '609 patent simply discloses that the “hollow center portion 432 and pinched off region 438 are formed in through silicon via 402” ('609 patent, 4:49-50) and that the “pinched off region 438 [is] at a bottom portion of TSV 402” (*id.*, 5:3-4). The '609 patent does not expressly disclose or claim the extent or height of the pinched off region 438 other than displaying it in Figure 4, which is shown below. '609 patent, Fig. 4. Thompson, ¶148.



'609 patent, Fig. 4 (annotated).

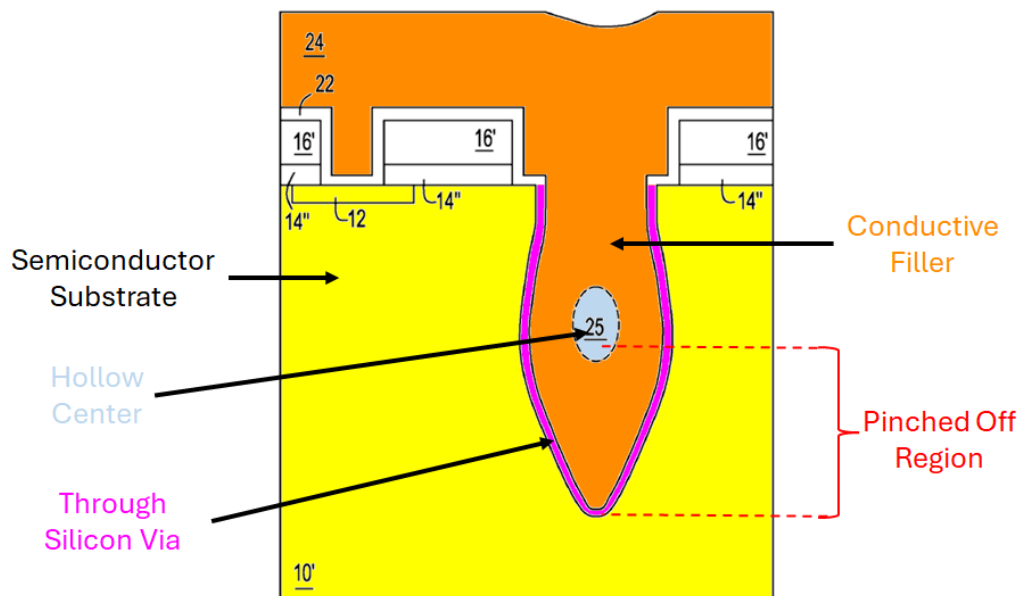
In similar fashion, *Cooney*'s pinched off region at the bottom portion of the TSV mirrors the pinched off region 438 in the '609 patent. Thompson, ¶149. As *Cooney* explains, an extended aperture having a “downward pointing torpedo shape” is etched to form the TSV through a semiconductor substrate 10. *Cooney*, ¶[0042].



Cooney, Fig. 5 (annotated).

Cooney's Figure 5 illustrates regions R1, R2, R3, and R4 of the extended aperture in *Cooney*'s substrate. *Cooney*, ¶¶ [0049]-[0054]; Fig. 5. In *Cooney*, “the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture.” *Id.*, ¶[0051]. “In addition, the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3.” *Id.* As a result, the extended aperture is “completely” filled by “a conductor layer 24 with an optional void 25 located therein.” *Id.*, ¶[0055] (The conductor layer 24 is “formed upon the liner layer 22” within the extended aperture.); *see also id.*, Abstract, ¶[0051]. According to *Cooney*, “due to the irregular sidewall curvature of the extended

aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.” *Id.*, ¶[0060]. By localizing void 25, to region R3, *Cooney* discloses a TSV having a pinched off region at a bottom portion of the TSV, as illustrated in Figure 6 below. Thompson, ¶¶149-152.



Cooney, Fig. 6 (annotated).

In the figure, the **pinched off region** extends over the narrowing portion of the torpedo shaped **aperture** in *Cooney* and is similar to the pinched off region 438 at the bottom portion of TSV 402 of the '609 patent. Thompson, ¶152; *compare Cooney*, Fig. 6 (**pinched off region**), *with* '609 patent, Fig. 4 (**pinched off region 438**). Moreover, as discussed in § V.A.1, *supra*, each of the plurality of **TSVs**

would include a **pinched off region** at a bottom portion of a respective **TSV**.

Thompson, ¶152.

The phrase “to prevent contamination during processing of said semiconductor substrate” states yet another use for the functioning of the pinched off region and should be entitled to no patentable weight over the prior art. *Atlas Powder*, 190 F.3d at 1347; *Sinex*, 309 F.2d at 492; *Arctic Cat*, 919 F.3d at 1328. Other than disclosing the presence of the pinched off region in the TSV, the ’609 patent does not identify any features of the pinched off region that contribute to preventing contamination. *See generally* ’609 patent. Thompson, ¶154. Thus, this functional language should not be entitled to any patent weight, but even if it were, *Cooney*’s TSV includes a **pinched off region** similar to that recited in limitation [1c-1], *Cooney*’s **pinched off region**, like the claimed pinched off region, would prevent contamination during processing of the semiconductor substrate. Thompson, ¶154.

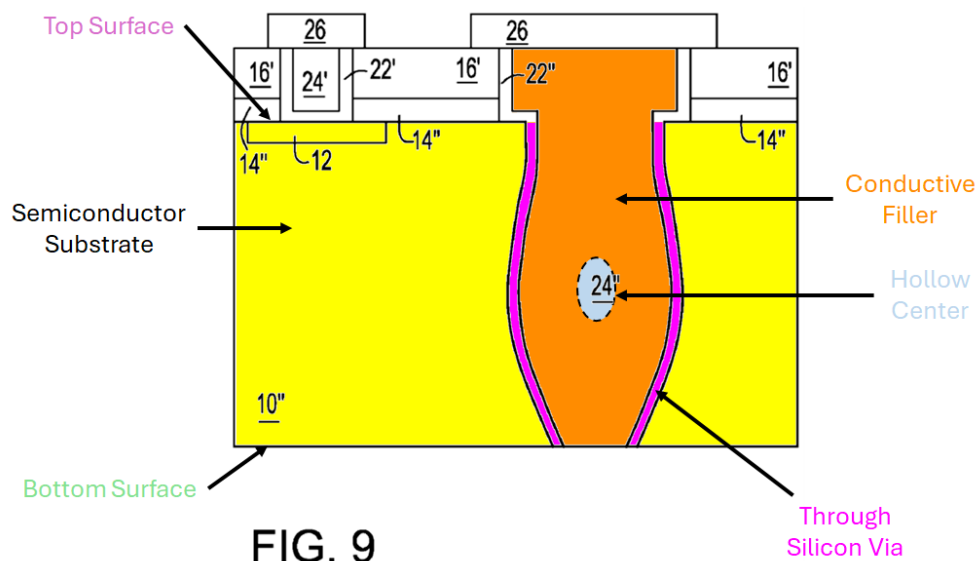
To the extent HID contends otherwise, a POSITA would have found it obvious to include the **pinched off region** in *Cooney*’s **TSV** to “prevent contamination during processing of said semiconductor substrate,” as recited in limitation [1c-1]. Thompson, ¶155. According to Dr. Thompson, it was well known that a via closed at both ends prevents contamination of the via during subsequent processes. Thompson, ¶156. As Dr. Thompson explains, by closing off

the seam, for example, as *Kim* (Ex. 1013) discloses, the seam is prevented from becoming exposed during subsequent CMP process, which thereby inhibits “foreign matter becoming caught inside the seam.” *Kim*, ¶¶[0012], [0027]-[0033], Fig. 1h; Thompson, ¶¶156-159. This occurs because the “seam ... is closed in the vicinity where the overhang occurred.” *Kim*, ¶[0029], Figs. 1g-1h. A POSITA would understand that, like *Kim*’s closed seam, the conductor layer in *Cooney* completely surrounds the void on all sides, so the pinched off region of *Cooney*’s TSV would also prevent metal contamination or particle contamination during any subsequent processes such as polishing or etching of the substrate. Thompson, ¶160. Thus, a POSITA would have found it obvious to include the **pinched off region** in *Cooney*’s TSV to prevent contamination during subsequent processing of *Cooney*’s semiconductor substrate. Thompson, ¶161. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including the **pinched off region**. *Id.*

Indeed, consistent with the teachings of the ’609 patent,³ *Cooney*’s TSV has no unwanted gaps between the **conductor layer 24** and the liner layer 22”, or

³ According to the ’609 patent’s “BACKGROUND” section, “conventional fabrication methods result in incomplete filling of the TWVs [(through wafer

between the liner layer 22" and/or the substrate 10 either at the top surface or bottom surface of substrate 10, as shown below. Thompson, ¶162; Cooney, ¶[0066] (disclosing that the shape of the extended aperture "aids in efficiently filling the aperture with the through substrate via 24").



Cooney, Fig. 9 (annotated and modified to include the void as shown in Fig. 6). Therefore, given the lack of any unwanted gaps, there would have been no contamination of Cooney's TSV during subsequent processes.

vias)], especially at their top and bottom portion," which further "result in unwanted gaps in the top and bottom portions of the TWVs." '609 patent, 1:45-48. These unwanted gaps then "lead to contamination of the TWVs during subsequent processes." *Id.*, 1:49-50.

Thompson, ¶¶162-163. Thus, if not explicitly disclosed, *Cooney* at a minimum have rendered obvious limitation [1c-1] in view of the knowledge of a POSITA.

Thompson , ¶164.

- g. [1c-2]: “wherein said hollow center is tapered in said pinched off region.”

Cooney discloses this limitation. Thompson, ¶165-172. As discussed above for claim [1c-1], and as illustrated below in Figure 5, *Cooney* discloses an extended aperture having a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶¶[0042], [0049]-[0054].

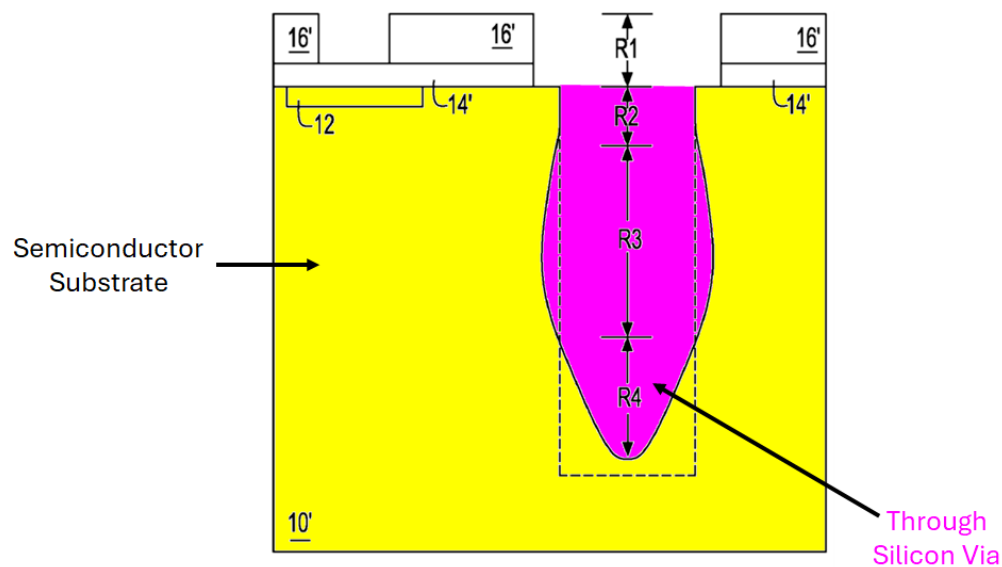


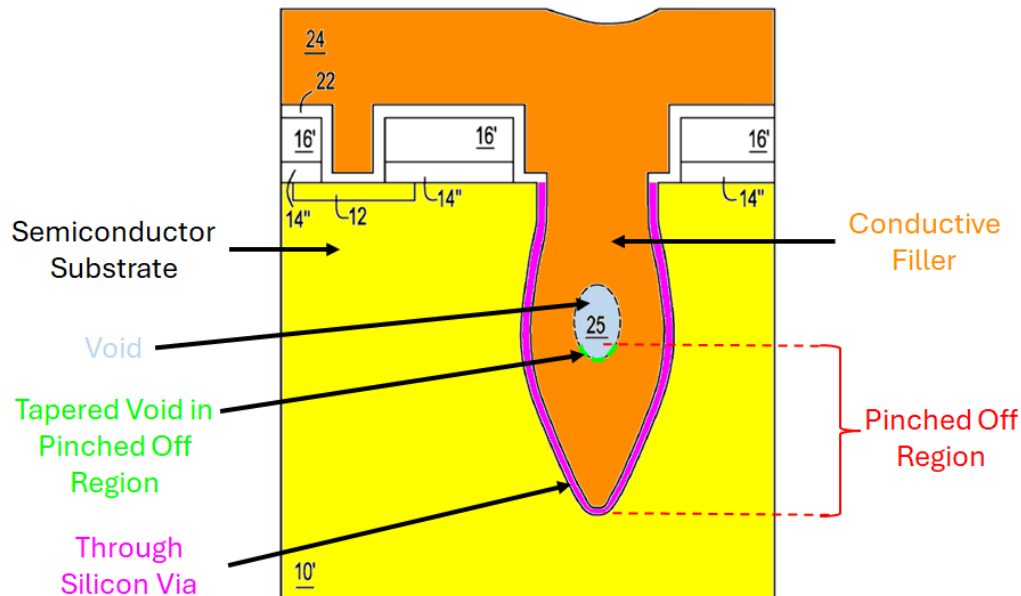
FIG. 5

Cooney, Fig. 5 (annotated).

In Figure 5, the walls of the aperture are tapered towards the bottom of the substrate (e.g., in regions R3 and R4) due to the disclosed “downward pointing torpedo shape” of the aperture. *Id.*, ¶[0042]; Thompson, ¶166.

Cooney discloses that “a liner layer 22” is “located and formed *conformally* upon the semiconductor structure of FIG. 5,” (*Cooney*, ¶[0055], emphasis added), and “may be deposited with enhanced adhesion using an atomic layer chemical vapor deposition[.]” *Id.*, ¶[0058]. Further, *Cooney* discloses “a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Id.*, ¶[0055]. As *Cooney* explains, “the conductor layer 24 typically comprises a tungsten material,” and “[s]uch a tungsten material is preferably deposited using a chemical vapor deposition method[.]” *Id.*, ¶[0059]. As *Cooney* teaches, chemical vapor deposition causes conformal deposition, which by its plain terms indicates that the conductor layer 24 would take the shape of the underlying surface. Thompson, ¶167. Because the underlying surface has tapered walls due to the aperture’s downward facing torpedo shape, the chemical vapor deposition of the conductor layer 24 would cause the conductor layer 24 to conformally follow the underlying tapered shape. Thompson, ¶168. Moreover, because the conductor layer 24 defines the boundary of void 25, the conformal deposition of conductor layer 24 would cause void 25 to

also have a tapered bottom portion to match the tapered shape of the aperture in the semiconductor substrate 10, as shown below in Figure 6. Thompson, ¶169.



Cooney, Fig. 6 (annotated).

According to Dr. Thompson, it was well known in the art that conformal deposition processes like chemical vapor deposition cause the deposited material to follow the shape of the underlying surface. Thompson, ¶170. As Dr. Thompson explains, for example, *Chandrashekar* (Ex. 1008) discloses that a “deposition process may result in a conformal layer of the materials [] built-up over the under-layer” and this “deposited layer follows the shape of the under-layer.”

Chandrashekar, ¶[0031]; Thompson, ¶170. Dr. Thompson further explains that, according to *Yen*, a profile of an underlying insulating layer may help the

following formation of a conducting layer because the underlying insulating layer is conformally deposited to follow the profile the bottom layer. *Yen*, ¶[0063]; Thompson, ¶171. Therefore, a POSITA would have recognized that *Cooney*'s conformal deposition processes would have caused the deposited layer to take the shape of the underlying surface. Thompson, ¶172. Accordingly, a POSITA would have recognized that the surface of the conductor layer, which forms the void in *Cooney*'s TSV, would take on a tapered shape similar to the underlying tapered shape of the aperture in *Cooney*. Indeed, this is illustrated below in Figure 6 of *Cooney*. Thompson, ¶172.

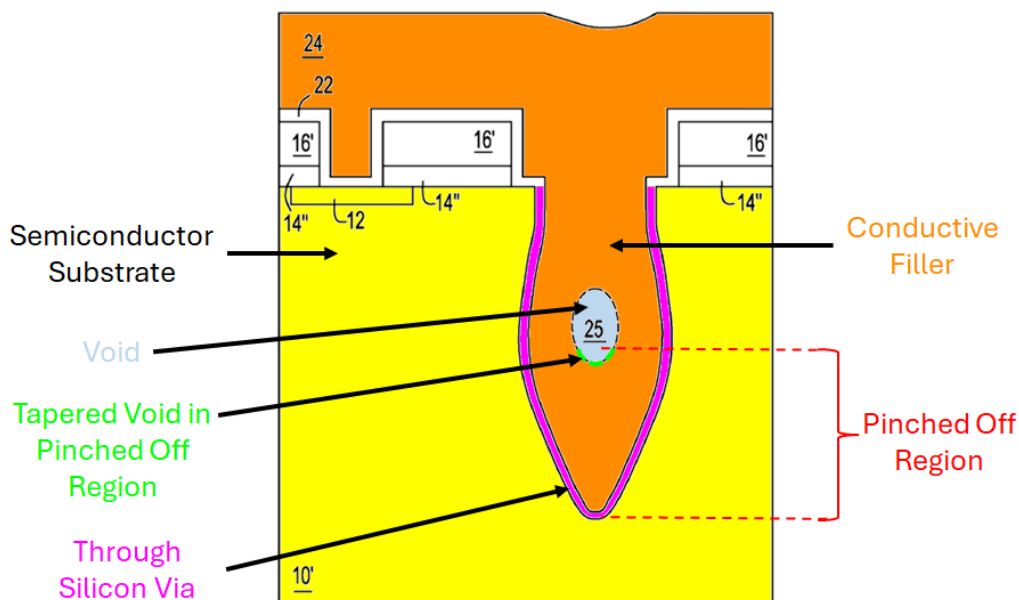


FIG. 6

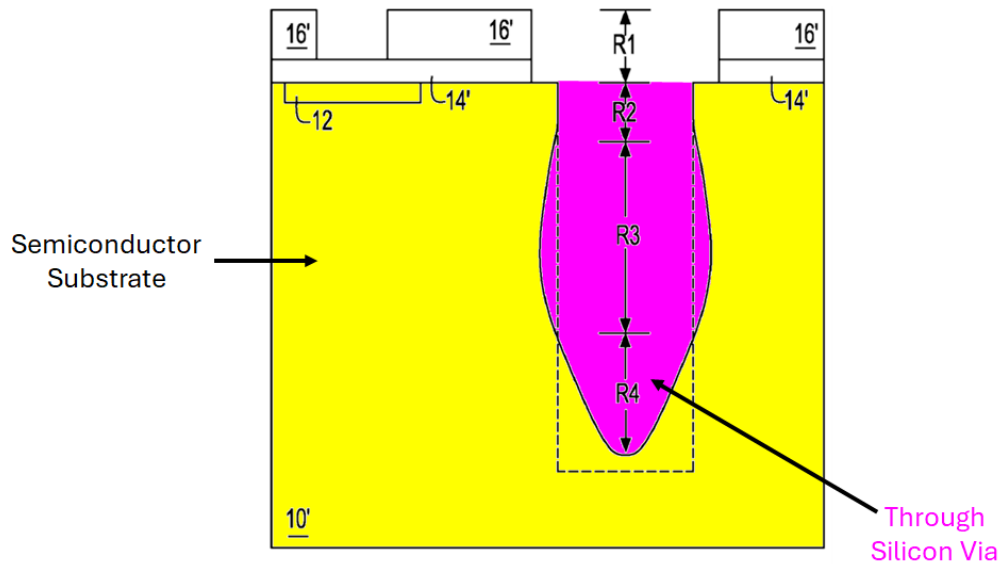
Cooney, Fig. 6 (annotated).

As a result, *Cooney*'s void 25 would also have a tapered shape towards its bottom portion. Thompson, ¶172. Thus, *Cooney* discloses that the “hollow center” (e.g., void 25) in *Cooney*'s TSV is tapered in the pinched off region. *Id.*

3. **Claim 2: “The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.”**

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitation of claim 2. Thompson, ¶¶173-179.

Cooney discloses forming an extended aperture that includes “sequentially contiguous” regions such as a first region R1 at the top portion that is “comparatively wide region,” a second region R2 “that is a constricted region,” a third region R3 that is “comparatively wide region,” and a fourth region R4 at the bottom portion that has a generally “pointed inward taper,” as shown below. *Cooney*, ¶¶[0049]-[0054]; Fig. 5.



Cooney, Fig. 5 (annotated).

The extended aperture thus has a “downward pointing torpedo shape” at the bottom portion of *Cooney*’s TSV. *Cooney*, ¶¶0042]; Thompson, ¶¶175-176.

Cooney further explains that, while “the comparatively wide linewidth of the first region R1, the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture,” (*Cooney*, ¶¶0051]), “the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3 [at the top portion], and to localize that void to the third region R3.” *Id.* Because the conductor layer 24 is deposited conformally to follow the extended aperture’s sidewall, “due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region

R3 of the extended aperture.” *Id.*, ¶[0060]. In other words, *Cooney* discloses that the “substantially bowed sidewalls” in region R3 help to ensure that a void is formed while the aperture is filled with a conductor layer, while the “inward taper” within the region R4, similar to the constriction within the second region R2, helps to seal off and completely enclose the void in the conductor layer at the bottom portion, and to localize any void to region R3. Thompson, ¶¶177-178. Thus, tapering the bottom portion of the TSV as disclosed by *Cooney*, forms the pinched off region at the bottom portion of the extended aperture as illustrated in Figure 6 of *Cooney*, below, by allowing the aperture to be filled by the conductor layer 24. Thompson, ¶178.

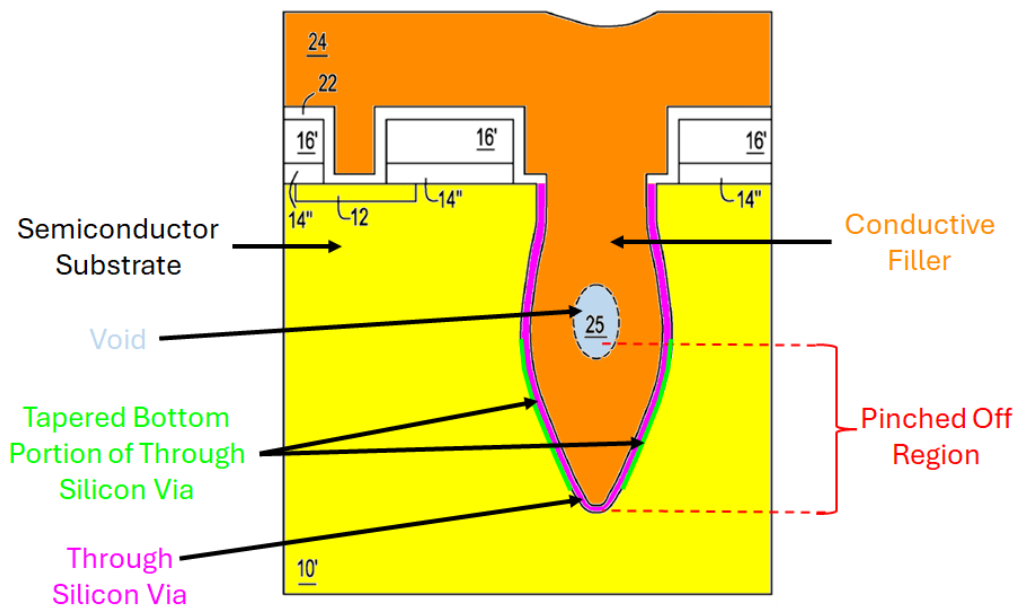


FIG. 6

Cooney, Fig. 6 (annotated).

As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, each of which includes a tapered bottom portion that helps to form the pinched off region at the bottom portion of the extended aperture for each respective TSV. Thompson, ¶179.

4. Claim 3: “The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.”

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitation of claim 3. Thompson, ¶¶180-183.

As discussed for claim limitation [1c-1], *Cooney* discloses that the pinched off region at the bottom portion of *Cooney*’s TSV prevents contamination during processing of said semiconductor substrate. Thompson, ¶¶181-183. *Cooney* discloses “backside planarizing of the semiconductor substrate 10’, the liner layer 22’ and the conductor layer 24’[.]” *Cooney*, ¶[0063]. *Cooney* explains that “[s]uch a backside planarizing is intended to remove a thickness from about 0.1 to about 10 microns from the semiconductor substrate 10’ while leaving exposed portions of both the liner layer 22” and the conductor layer 24”.” *Id.* *Cooney* also discloses that the backside planarizing may use methods such as “mechanical polish planarizing methods and chemical mechanical polish planarizing methods.”

Id. Figure 9 of *Cooney* illustrates the semiconductor substrate 10", liner layer 22" and conductor layer 24" after backside planarizing. *Id.*

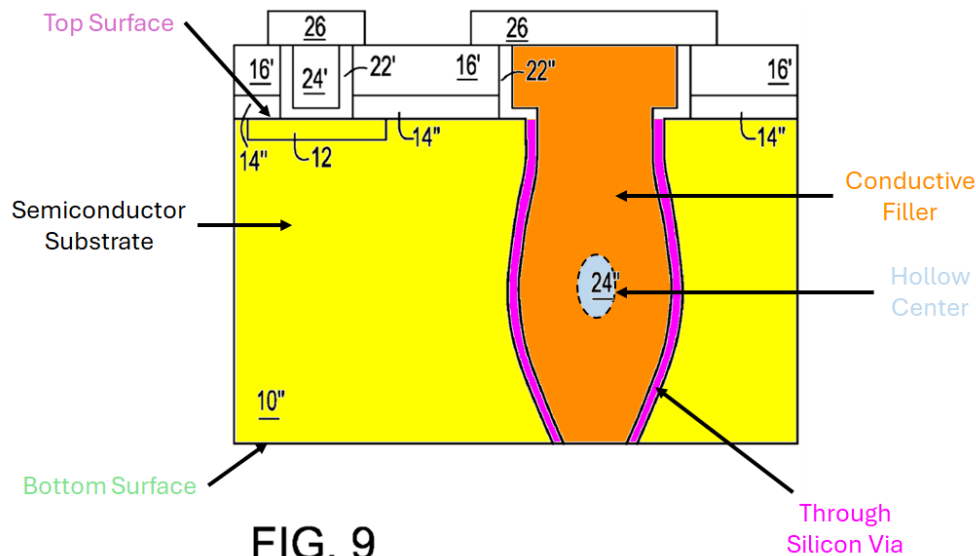


FIG. 9

Cooney, Fig. 9 (annotated and modified to include the void as shown in Fig. 6). As seen above in Figure 9 of *Cooney*, there are no unwanted gaps between conductor layer 24" and liner layer 22", or between liner layer 22" and/or substrate 10 at the bottom surface of substrate 10. As discussed for claim limitation [1c-1], because there are no gaps, any contamination or debris generated during mechanical polish planarizing methods and/or chemical mechanical polish planarizing methods used to perform the backside planarizing would not be able to enter the TSV in *Cooney*. Thompson, ¶183. Accordingly, *Cooney* discloses preventing contamination during polishing of the bottom surface of the substrate. *Id.* Furthermore, as discussed for limitation [1c-1], a POSITA would have found it

obvious to include the **pinched off region** in *Cooney*'s TSV to prevent contamination during subsequent processing of *Cooney*'s semiconductor substrate. Thompson, ¶183. And because the conductor layer in *Cooney* completely fills the TSV and surrounds the void on all sides due to the **pinched off region**, a POSITA would recognize that the pinched off region of *Cooney*'s TSV would prevent metal contamination or particle contamination during any subsequent processes such as polishing or etching of the substrate, including during polishing said bottom surface of said substrate. *Supra*, § V.A.2.f; *Kim*, ¶¶[0012], [0027]-[0033], Fig. 1h; Thompson, ¶183.

5. Claim 4: “The semiconductor substrate of claim 1, wherein said **conductive filler comprises a **metallic filler**.”**

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitation of claim 4. Thompson, ¶¶184-187.

For example, as discussed for claim [1b-1], *Cooney* discloses that “the **conductor layer 24** may comprise any of several conductor materials, including but not limited to any of several **metals and metal alloys**[.]” *Id.*, ¶[0059]; *see also supra* Section V.A.2.c; Thompson, ¶186. Thus, *Cooney*'s **conductor layer 24** (e.g., “**conductive filler**”) comprises a **metal or metal alloy** (e.g., “**metallic filler**”). Thompson, ¶187.

6. Claim 5: “The semiconductor substrate of claim 1, wherein said **conductive filler comprises **tungsten**.”**

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitation of claim 5. Thompson, ¶¶188-191.

For example, as discussed for claim 4, *Cooney* teaches a **conductor layer 24** that comprises “any of several conductor materials, including but not limited to any of several metals and metal alloys.” *See supra* Section V.A.5; Thompson, ¶191. *Cooney* further discloses “the **conductor layer 24** typically comprises a **tungsten** material.” *Cooney*, ¶[0059]; Thompson, ¶191. Thus, *Cooney*’s **conductor layer 24** (e.g., “**conductive filler**”) comprises **tungsten**. Thompson, ¶191.

7. Claim 6: “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.”

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitations of claim 6. Thompson, ¶¶192-195.

As discussed for claim 2, *Cooney* discloses that the “substantially bowed sidewalls” in region R3 helps to ensure that a void is formed while the aperture is filled with a conductor layer, while the “inward taper” within the region R4 helps to seal off and completely enclose the void in the conductor layer at the bottom

portion, and to localize any void to region R3. *Supra* V.A.3; Thompson, ¶194. As a result of the tapered bottom portion of the TSV as disclosed by Cooney, the “conductive filler” (e.g., conductor layer 24) fills the tapered bottom portion, sealing or pinching off the “hollow center” (e.g., void 25) formed within as illustrated in Figure 6 of Cooney, below. Thompson, ¶194.

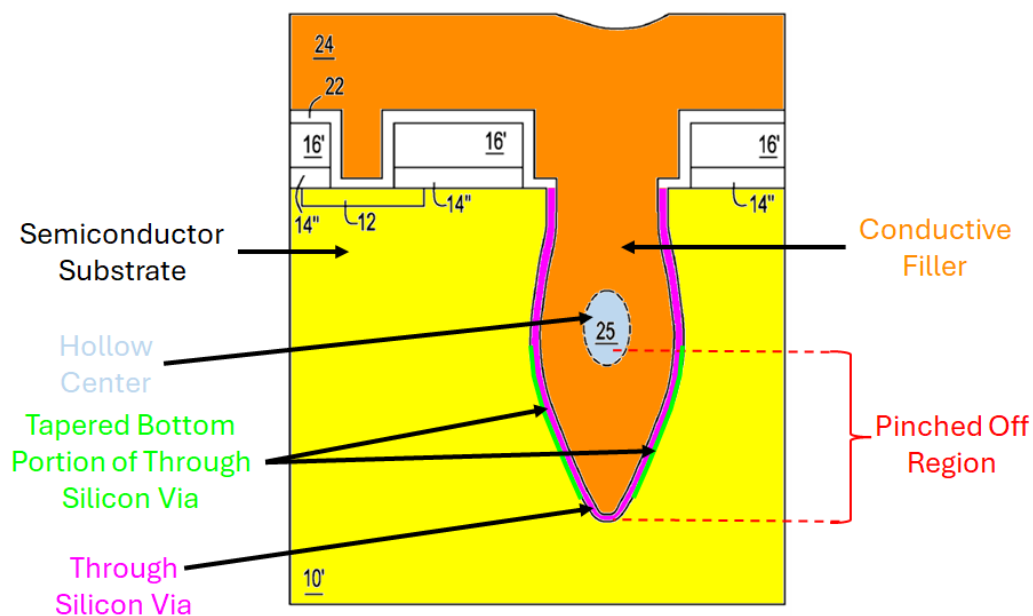


FIG. 6

Cooney, Fig. 6 (annotated).

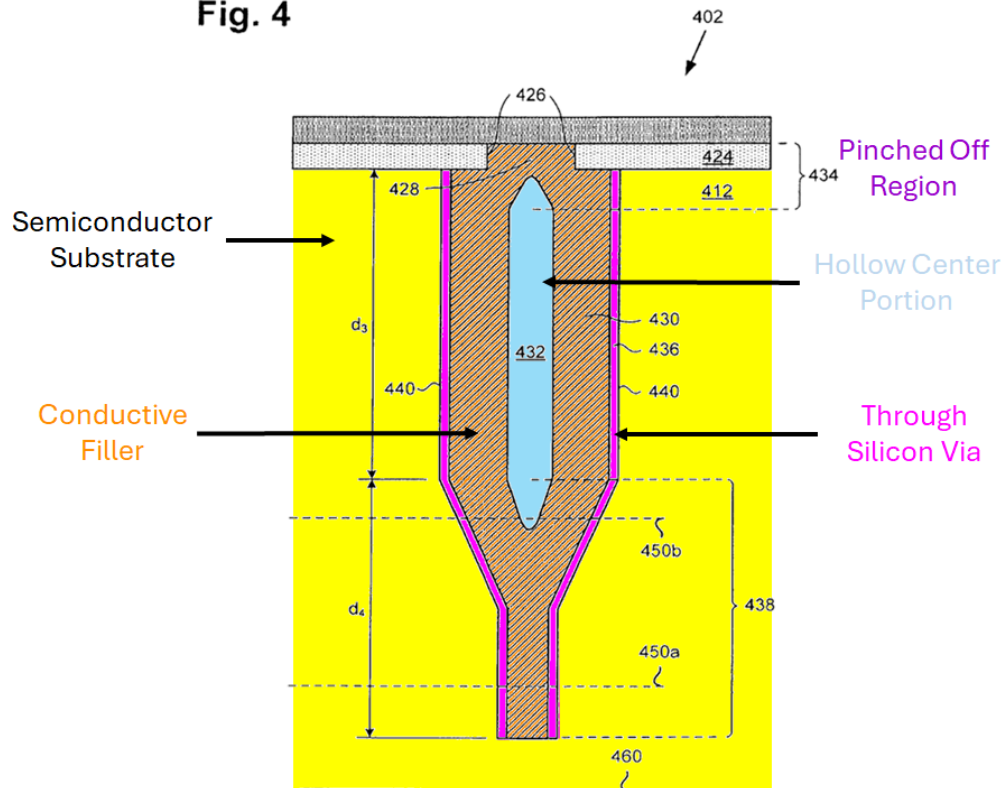
Moreover, as discussed in § V.A.1, *supra*, Cooney includes a plurality of TSVs, the tapered bottom portion of each of which results in the “conductive filler” (e.g., conductor layer 24) sealing off or pinching the “hollow center” (e.g., void 25) formed within as illustrated in Figure 6 of Cooney, above. Thompson, ¶195.

8. Claim 9: “The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.”

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitations of claim 9. Thompson, ¶¶196-202.

The '609 patent generally discloses “forming pinched off region 434 at a top portion of TSV 402” and that “forming opening 428 ensures pinched off region 434 is formed in the top region of TSV 402.” '609 patent, 5:4-5, 5:14-16. But the '609 patent does not expressly disclose the extent or height of pinched off region 434 other than displaying it in Figure 4, as shown below. *Id.*, Fig. 4; Thompson, ¶198.

Fig. 4



'609 patent, Fig. 4 (annotated)

In *Cooney*, the pinched off region at the top of the TSV is similar to the pinched off region 434 in the '609 patent. As discussed for claims [1b-3] and 2, *Cooney* discloses that an extended aperture corresponding to its TSV has varying widths and comprises four regions R1, R2, R3, and R4. *Cooney*, ¶¶[0049]-[0054]; Fig. 5, below; Sections V.A.2.e and V.A.3; Thompson, ¶199.

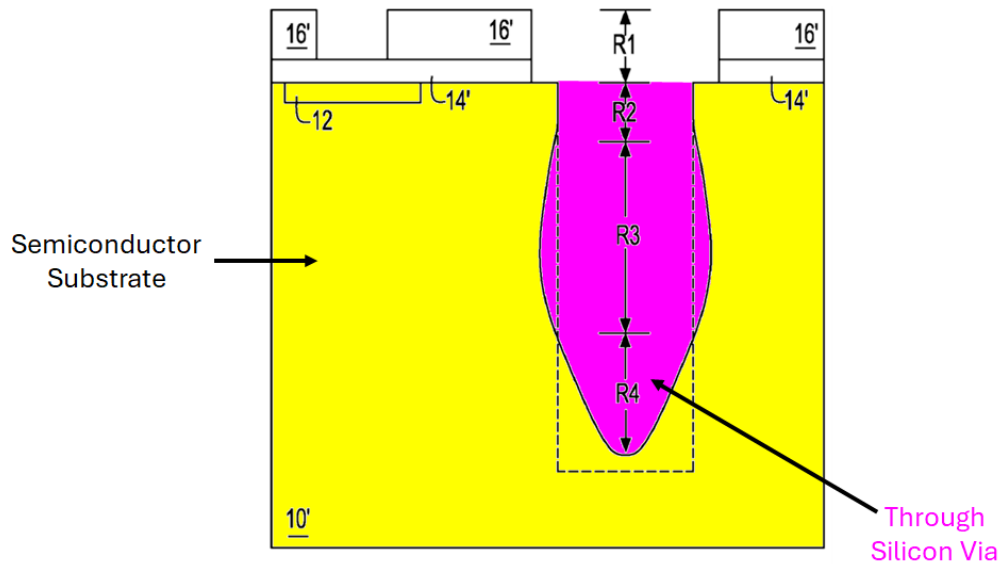


FIG. 5

Cooney, Fig. 5 (annotated).

As also previously discussed, *Cooney* explains that “the constriction within the second region R2 is intended to *completely seal off* any void that may form within the third region R3, and to localize that void to the third region R3.” *Id.*, ¶[0051] (emphasis added), ¶[0060] (“[T]he conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.”). Thus, the portion between the top surface of the TSV and the area where the void is *sealed off with the conductor layer 24* forms the *pinched off region* at the top of the TSV. Thompson, ¶200. This is illustrated in annotated Fig. 6 of *Cooney*, below. Thompson, ¶201; *Compare Cooney*, Fig. 6 (pinched off region), *with* ’609 patent, Fig. 4 (pinched off region 434). Thompson, ¶201.

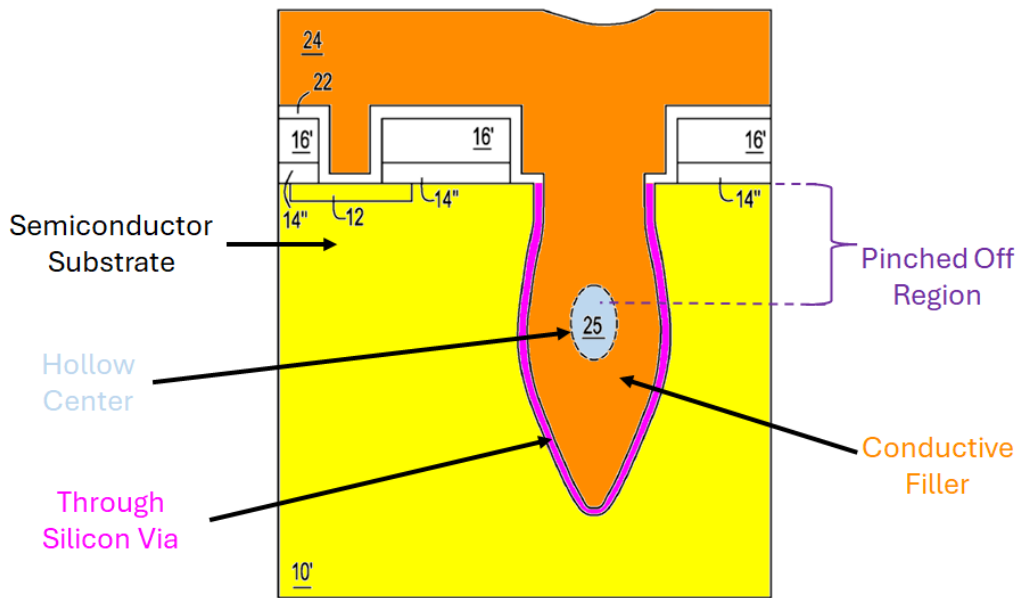


FIG. 6

Cooney, Fig. 6 (annotated).

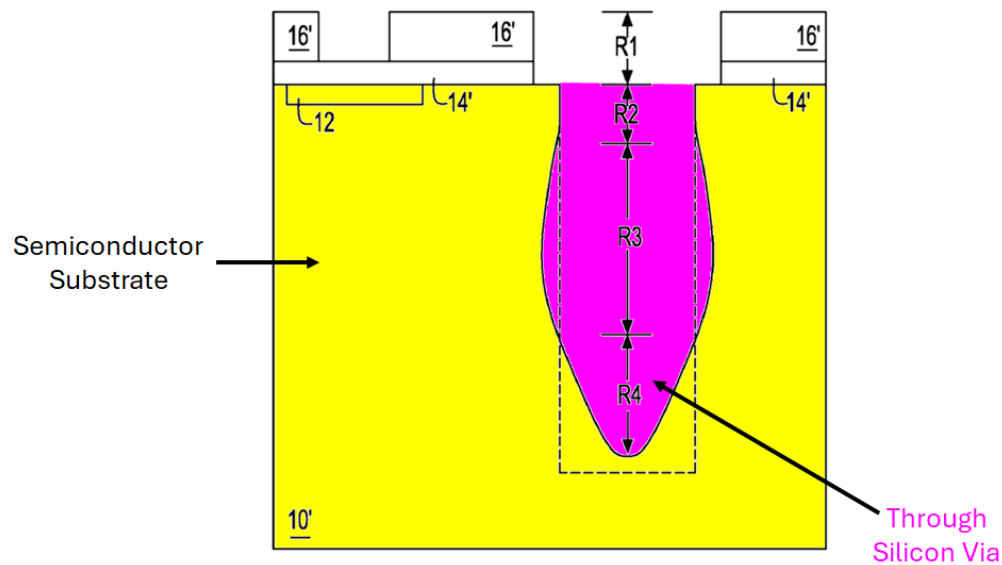
As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, and as discussed above, by localizing void 25 in region R3, conductor layer 24 of *Cooney* forms the pinched off region at the top of each of the TSVs in a similar manner.

Thompson, ¶202.

9. **Claim 10:** “The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills bottom portion, narrowing said hollow center.”

As discussed above, *Cooney* anticipates or would have rendered obvious claim 1. *Cooney* also teaches the additional limitations of claim 10. Thompson, ¶¶203-207.

As discussed above for claim [1c-1], and as illustrated in Fig. 5, below, *Cooney* discloses an extended aperture having a “downward pointing torpedo shape” for forming one or more TSVs through a semiconductor substrate 10. *Cooney*, ¶¶[0042], [0049]-[0054].



Cooney, Fig. 5 (annotated).

As illustrated above in Figure 5 of *Cooney*, the walls of the aperture are inwardly tapered towards the bottom of the substrate due to the disclosed “downward pointing torpedo shape” of the aperture. *Id.*, ¶¶[0042], [0049]-[0054]; Thompson, ¶205.

Further, as *Cooney* discloses, when a conductor layer 24 completely fills the extended aperture, the conductor layer 24 would conformally take the shape of the underlying surface of the extended aperture. *Cooney*, ¶[0055]; *supra* V.A.2.g;

Thompson, ¶206. As a result, the conformal deposition of conductor layer 24 would cause the conductor layer 24 to follow the underlying tapered shape at the bottom portion of the extended aperture. *Cooney*, ¶[0055]; Thompson, ¶206. A POSITA reading *Cooney* would have recognized that the tapered shape at the bottom further causes the conductive filler to incompletely fill at the bottom portion of the void, thus narrowing the void 25 to correspond to the tapered shape of the aperture in *Cooney*'s semiconductor substrate 10, as shown below.

Thompson, ¶206.

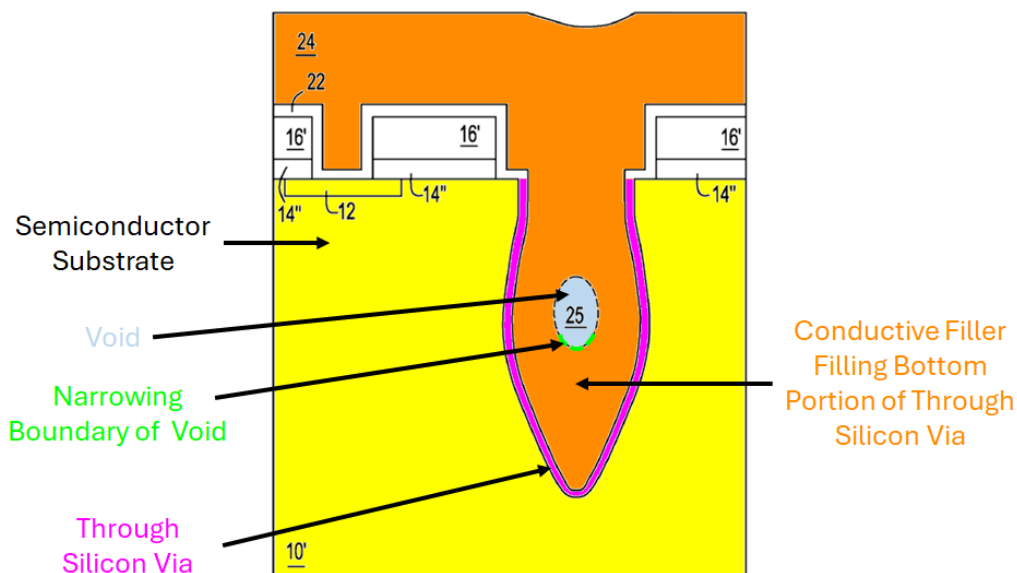


FIG. 6

Cooney, Fig. 6 (annotated).

See, e.g., Acoustic Tech., Inc. v. Itron Networked Sols. Inc., 949 F.3d 1366, 1373-74 (Fed. Cir. 2020) (affirming anticipation ground as supported by expert testimony of what a skilled artisan would have recognized the prior art reference as

disclosing); *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (finding “a reference can anticipate a claim ... if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.”). Thus, *Cooney* discloses a TSV tapered at the bottom portion such that conductive filler (e.g. “conductor layer 24”) incompletely fills the bottom portion of the TSV, narrowing the “hollow center” (e.g., void 25). Thompson, ¶206.

As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, each of which is tapered at the bottom portion such that conductive filler (e.g. “conductor layer 24”) incompletely fills the bottom portion of a respective TSV, narrowing the “hollow center” (e.g., void 25) in a similar manner. Thompson, ¶207.

10. Independent Claim 11

Cooney discloses or would have rendered obvious every element of independent claim 11 in the same manner as explained above for independent claim 1. Thompson ¶¶208-212.

- a. [11pre]: “A **semiconductor substrate** having a plurality of **devices**, said semiconductor substrate comprising:”
[11a]: “a plurality of **through silicon vias** disposed in said **substrate** extending from a **top surface** of said substrate to a **bottom surface** of said substrate;”
[11b]: “a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;”

Limitations [11pre]-[11b] are substantively identical to limitations [1pre]-[1b-3]. *Cooney* anticipates or would have rendered obvious limitations [11pre]-[11b] as discussed above for limitations [1pre]-[1b-3]. *Supra* §§ V.A.2.a-V.A.2.e; Thompson ¶209.

- b. [11c]: “wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.”

Limitation [11c] includes recitations substantially identical to the recitations in claim limitations [1c-1] and [1c-2] and claim 9, the primary difference being that limitation [11c] refers to the pinched off region at a bottom portion as “another pinched off region at a bottom portion.” Thompson, ¶210. *Cooney* anticipates or would have rendered obvious limitation [11c] in the same manner as explained

above for limitations [1c-1] and [1c-2] and claim 9. *Supra* §§ V.A.2.f, V.A.2.g, and V.A.8; Thompson ¶¶210-211.

Moreover, a combination of the annotations of *Cooney*'s Figure 6 from §§ V.A.2.f and V.A.8 is illustrated below to show the pinched off region at a top portion and another pinched off region at a bottom portion of *Cooney*'s TSV.

Thompson, ¶211; *compare Cooney*, Fig. 6 (pinched off region and another pinched off region), with '609 patent, Fig. 4 (pinched off region 434 and pinched off region 438); § II.A, *supra*.

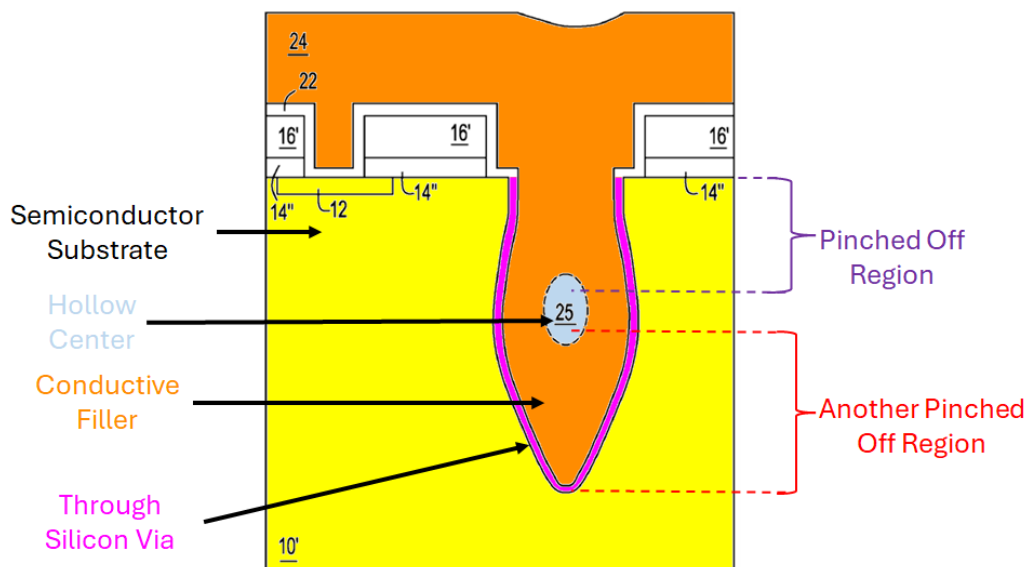


FIG. 6

Cooney, Fig. 6 (annotated).

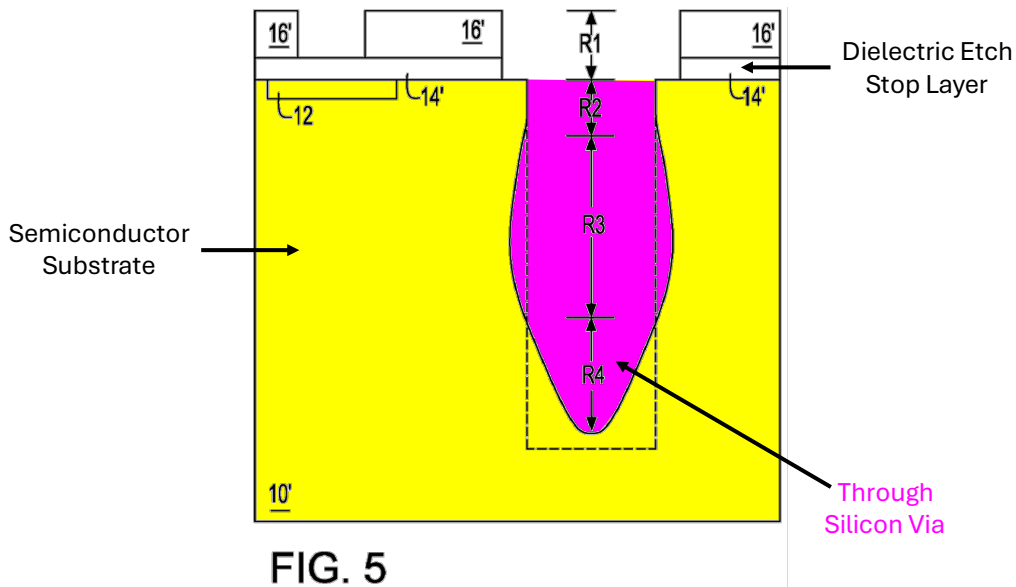
As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, each of which includes a pinched off region and another pinched off region as discussed above. Thompson, ¶212.

- 11. Claim 12: “The semiconductor substrate of claim 11, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.”**

As discussed above, *Cooney* anticipates or would have rendered obvious claim 11. *Cooney* also teaches the additional limitations of claim 12. Thompson, ¶¶213-219.

Cooney discloses that an “etch stop layer 14 is located upon the semiconductor substrate 10[.]” *Cooney*, ¶[0026]. *Cooney* discloses that “etch stop layer 14 will typically comprise a dielectric etch stop material[.]” *Id.*, ¶[0034]. Thus, *Cooney* discloses a dielectric layer (e.g., etch stop layer 14) disposed on the top surface of its substrate 10.

Further, *Cooney* discloses the dielectric etch stop layer 14 has an aperture such as “a first region R1 that is a first comparatively wide region” that is situated directly above *Cooney*’s TSV, as shown below. *Cooney*, ¶[0050].



Cooney, Fig. 5 (annotated).

Cooney further discloses that “the linewidth of the third region R3 is preferably greater than the linewidth of the first region R1.” *Cooney*, ¶[0054]. That is, *Cooney* discloses that the opening in the dielectric etch stop layer 14 in the region R1 has a width that is smaller than a width of *Cooney*’s TSV, specifically smaller than a width of region R3 of *Cooney*’s TSV. Thompson, ¶¶215-218.

As discussed in § V.A.1, *supra*, *Cooney* includes a plurality of TSVs, each of which includes the opening in the dielectric etch stop layer 14 in the region R1 having a width that is smaller than a width of *Cooney*’s TSV. Thompson, ¶219. Thus, *Cooney* discloses the limitations of claim 12.

12. Claims 13, 14, and 18

As discussed above, *Cooney* anticipates or alternately would have rendered obvious claim 11. Claims 13, 14, and 18 add substantively the same limitations as claims 4, 5, 10, respectively. Thompson ¶¶220-222. *Cooney* teaches or suggests the additional limitations of claims 13, 14, and 18 in the same manner as explained above for the additional limitations of claims 4, 5, and 10. Thompson ¶222.

13. Claim 17: “The semiconductor substrate of claim 11, wherein said another pinched off region is tapered at said bottom of each of said plurality of through silicon vias.”

As discussed above, *Cooney* anticipates or alternately would have rendered obvious claim 11. Claim 17 adds substantively the same limitations as claim 2. *Cooney* teaches or suggests these limitations in the same manner as explained above for the additional limitations of claim 2. Thompson ¶¶223-225.

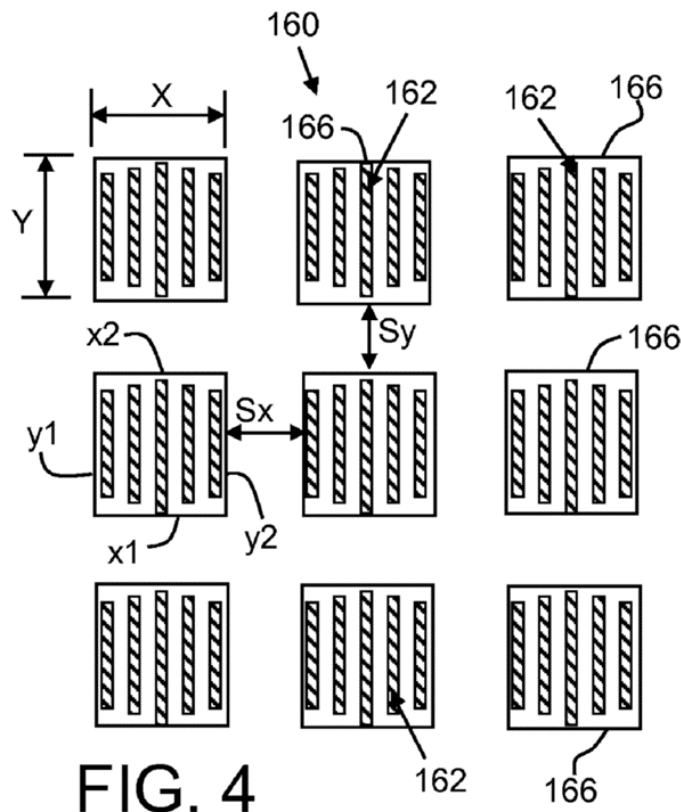
B. Claims 7 and 15 Are Obvious over *Cooney* and *Dean* (Ground 2)

1. Overview of *Dean*

Like *Cooney*, *Dean* relates to TSVs and, more particularly, to arranging TSVs in an integrated circuit (IC) layout to reduce or eliminate wafer breakage. *Dean*, Abstract, ¶[0002]. *Dean* recognizes that “[t]hrough silicon vias (TSVs) are typically elongated vias,” and “when TSVs are aligned they act like perforations [in the wafer,] making it easy to break a wafer into which they are formed.” *Id.*, ¶[0017] (“In particular, wafers having aligned, regularly repeating TSV arrays

break at an approximately 66% rate[.]”). To alleviate this problem, *Dean* discloses a system for “identifying linearly aligned through silicon vias (TSVs) in a portion of an integrated circuit (IC) layout that includes a plurality of TSVs” and “modifying at least the portion of the IC layout to reduce a number of the linearly aligned TSVs.” *Id.*, ¶[0006], Abstract; Thompson ¶¶89-90.

Dean discloses, for example, an “IC layout 90 including array 160 having nine TSV sets 162” in which “all of the TSVs ... initially extend in a single, given direction[.]” *Dean*, ¶[0031]. Figure 4 of *Dean* illustrates this example layout with TSV sets 162 aligned in the Y direction. *Id.*, Fig. 4.



Dean, Fig. 4.

Dean discloses rotating alternate TSV sets 162 to be non-aligned to the given direction (e.g., the Y direction). *Dean*, ¶[0033]. Figure 6 of *Dean*, below, illustrates the results of such rotation of the TSV sets 162 in which some TSV sets 162 are aligned with a vertical direction, whereas other TSV sets 162 are aligned in a horizontal direction. Thompson, ¶¶91-93.

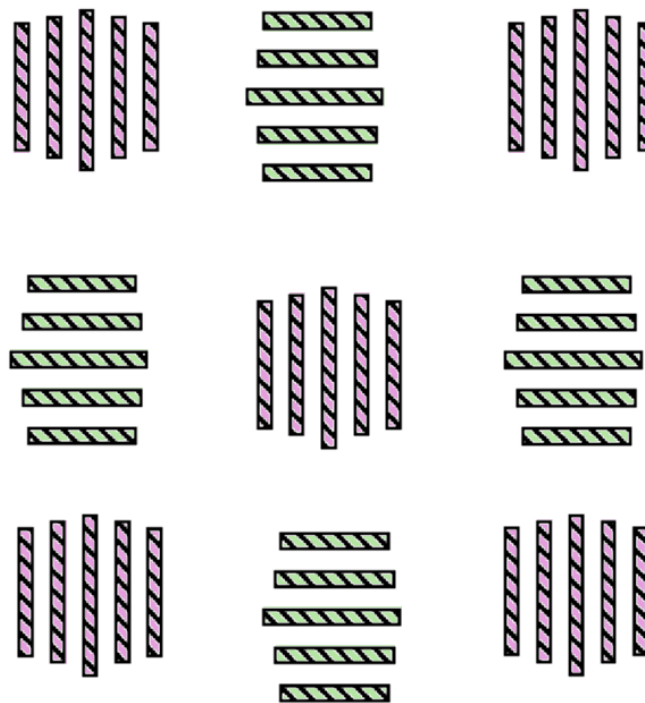


FIG. 6

Dean, Fig. 6 (annotated).

According to *Dean*, the rotation of the TSV sets “reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing.” *Dean*, ¶[0039]; Thompson, ¶94.

Dean is analogous art to the '609 patent because *Dean*, like the '609 patent, discloses methods of formation of TSVs in a semiconductor substrate. *Compare Dean*, Abstract, ¶¶[0002], [0005]-[0007], [0042], *with* the '609 patent, Abstract, 1:54-56, 3:1-5, 4:9-5:24; Thompson, ¶95.

2. Rationale for combining *Cooney* with *Dean*

a. Motivation to combine

A POSITA would have been motivated to combine the arrangement of TSVs, as *Dean* teaches, with the semiconductor manufacturing process of *Cooney*. Thompson, ¶¶227-246.

Cooney and *Dean* are both directed to manufacturing semiconductor substrates with TSVs. Thompson, ¶239. *Cooney* discloses “a semiconductor structure [that] includes a through substrate via 24” that penetrates from a front side of a semiconductor substrate 10” to a backside of the semiconductor substrate 10.” *Cooney*, ¶[0065]. In *Cooney*, “backside planarizing” such as “mechanical polish planarizing methods and chemical mechanical polish planarizing methods” may be used to remove the backside of the substrate. *Id.*, ¶[0063]. *Cooney* makes clear that “a multiplicity of dimensionally similar or dimensionally identical apertures and corresponding vias may also be used within a single substrate.” *Id.*, ¶[0066]. *Dean* similarly discloses “a plurality of through silicon vias (TSVs)” in an integrated circuit (IC) layout. *Dean*, Abstract, ¶[0001]. *Dean* further explains that

“at a subsequent process step, the bottom of the TSV is exposed by removing the backside of the substrate by, for example, mechanically grinding or etching,” but “when TSVs are aligned they act like perforations [within a wafer, and thus] making it easy to break a wafer into which they are formed.” *Id.*, ¶[0017], Fig. 4. To address this issue, *Dean* teaches “arranging through silicon vias (TSVs) in an integrated circuit (IC) layout to reduce linearly aligned TSVs” in order to reduce wafer breakage. *Id.*, ¶[0002], Abstract. Accordingly, a POSITA would have appreciated that *Dean*’s technique of avoiding alignment of TSVs would be useful for arranging the plurality of TSVs on *Cooney*’s substrate to reduce wafer breakage. Thompson, ¶240.

A POSITA would have recognized that manufacturing semiconductor substrates with *Cooney*’s TSVs would face a similar problem related to wafer breakage, as *Dean* teaches. Thompson, ¶241. A POSITA reading *Cooney* would have understood that *Cooney*’s TSVs are narrow elongated vias having a width ranging from 0.1 to 5 microns and a length ranging from 3 to 50 microns. Thompson, ¶233. For example, *Cooney* discloses that TSVs have “a comparatively narrow linewidth (i.e., in a range from about 5 to 0.1 microns).” *Cooney*, ¶[0007]. *Cooney* further discloses that the TSVs have an aperture etched in the semiconductor substrate ranging between about 3 and 50 microns. *Cooney*, ¶[0050]; *Dean*, ¶[0017] (“Through silicon vias (TSVs) are typically elongated

vias” that may be “3 μm wide by 50 μm long.”); Thompson, ¶233. Thus, given the prevalence of elongated TSVs and given Cooney’s disclosures regarding the dimensions of its TSVs, a POSITA would have understood that *Cooney*’s vias are elongated vias. Thompson, ¶233. A POSITA would have recognized that if a plurality of elongated TSVs were aligned with each other on *Cooney*’s substrate, those TSVs would act like perforations, as *Dean* teaches. Thompson, ¶234. But even if *Cooney*’s TSVs are not elongated TSVs, the same concern regarding wafer breakage remains. Thompson, ¶234. A POSITA would have understood that circular TSVs are perforations in the wafer substrates as well. Thompson, ¶234. As such, *Cooney*’s TSVs—when arranged “in a single, given direction, i.e., an x-direction or a y-direction,” as *Dean* explains—would potentially cause breakage of *Cooney*’s substrate during semiconductor processing. *Dean*, ¶[0031]; Thompson, ¶234. Thus, regardless if the TSVs are elongated or circular, a POSITA would have been motivated to use alternating elongated TSVs, as *Dean* teaches, to “reduce or *eliminate* wafer breakage.” *Dean*, ¶[0039] (emphasis added); Thompson, ¶234.

A POSITA would have recognized that such an aligned arrangement of elongated TSVs in *Cooney*’s substrate would also make it easy to break *Cooney*’s substrate during manufacturing of *Cooney*’s substrate as disclosed by *Dean*.

Thompson, ¶235. A POSITA would have, therefore, looked to *Dean*'s teachings to address the problem of substrate breakage. *Id.*

Dean discloses rotating alternate TSV sets 162 to be non-aligned to the given direction. *Dean*, ¶[0033], Fig. 6; Thompson, ¶236. As *Dean* explains, such an arrangement of the TSVs, as shown below, “reduces or eliminates wafer breakage by arranging and design rule checking TSVs to avoid alignment, i.e., parallel edges from lining up, and creating high stress points, which cause wafer breakage during IC processing.” *Dean*, ¶[0039].

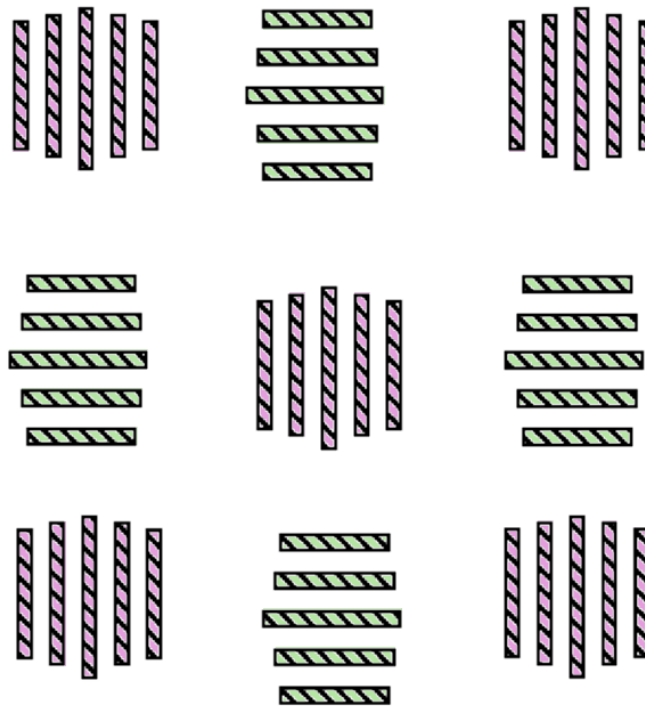


FIG. 6

Dean, Fig. 6 (annotated).

A POSITA would have been motivated to implement the TSV arrangement scheme, as *Dean* teaches, in *Cooney*'s substrate to ensure that the TSVs in *Cooney*'s substrate do not line up and do not create high stress points as taught by *Dean*. Thompson, ¶¶240-241. A POSITA would have recognized that doing so would have minimized the likelihood of breakage of *Cooney*'s substrate during semiconductor processing. Thompson, ¶241.

Moreover, as Dr. Thompson explains, fabricating semiconductor devices on a wafer is an expensive and time-consuming process. Thompson, ¶242 Because a broken wafer is typically discarded and because a wafer may have hundreds of dice, wafer breakage has the potential to cause significant economic loss to the semiconductor manufacturer. Thompson, ¶242. Furthermore, debris generated due to breakage of one or more wafers during semiconductor processing can contaminate other wafers and/or the equipment being used to manufacture the wafers. *Id.* Cleaning of the wafers and/or equipment can further affect the manufacturing time and increase manufacturing costs. *Id.* Accordingly, a POSITA would have been motivated to reduce or eliminate the likelihood of wafer breakage during the manufacture of *Cooney*'s substrate to minimize wafer wastage and to minimize contamination of associated wafers and/or equipment. *Id.*; *Dean*, ¶[0017] (noting a reduction of breakage from approximately 66% to approximately 4%); *Dome Patent L.P. v. Lee*, 799 F.3d 1372, 1380 (Fed. Cir. 2015) (affirming

obviousness where “a person of ordinary skill understood that [the feature resulting from the alteration] was desirable”).

As *Dean* teaches, it was well known in the art to orient elongated TSVs along the width and length directions to reduce the likelihood of wafer breakage. Thompson, ¶243. A POSITA would have found the modification of the TSV arrangement on *Cooney* based on *Dean*’s teaching obvious because it would have involved nothing more than the use of a known technique—lengthwise and widthwise orientation of elongated TSVs—to improve a similar device—*Cooney*’s semiconductor substrate—in the same way, namely, by reducing the likelihood of breakage of *Cooney*’s semiconductor substrate during manufacturing. *Id.*; *KSR*, 550 U.S. at 401 (stating “a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”); *KSR*, 550 U.S. at 419-20.

b. Expectation of Success

A POSITA would have had a reasonable expectation of success in implementing the teachings of *Dean* for the manufacture of the TSVs of *Cooney*. Thompson, ¶244. Given that both *Cooney* and *Dean* disclose semiconductor substrates with a plurality of TSVs, designing the arrangement of the TSVs on *Cooney*’s substrate using the via arrangement techniques taught by *Dean* would have been well within the skill of a person of ordinary skill in the art. *Id.* The

application of *Dean*'s via layout principles on *Cooney*'s substrate would also have been a simple implementation of the TSV arrangement of *Cooney* with the TSV arrangement of *Dean*. Thompson, ¶245. A POSITA would have had a reasonable expectation of success for the combination of *Dean* with *Cooney* because it merely requires combining well-known prior elements according to known methods. *Id.*; *See, e.g., In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001) (finding when the prior art identifies a problem and provides explicit guidance on how to fix the problem, it is reasonable to conclude that the skilled artisan would have had a reasonable expectation of success in combining the prior art.).

3. Claims 7 and 15

- a. **Claims 7 and 15: “The semiconductor substrate of claim [1 or 11], wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.”**

As discussed above, *Cooney* anticipates or alternately would have rendered obvious claims 1 and 11. *Cooney* in view of *Dean* would have rendered obvious the additional limitations of claims 7 and 15. Thompson, ¶¶226-227.

It would have been obvious to lay out a first group of *Cooney*'s TSV a in a width direction and a second group of *Cooney*'s TSV in a length direction, as *Dean* teaches, to reduce or eliminate wafer breakage. Thompson, ¶228. *Cooney* discloses that TSVs have “a comparatively narrow linewidth (i.e., in a range from about 5 to

0.1 microns)” with an aperture etched in the semiconductor substrate as ranging between about 3 and 50 microns. *Cooney*, ¶¶[0007], [0050]. A POSITA reading *Cooney* would have understood that *Cooney*’s TSVs have a generally narrow elongated shape. Thompson, ¶228; § V.B.2.a. As explained above, when *Cooney*’s TSVs are arranged “in a single, given direction, i.e., an x-direction or a y-direction,” there is a high chance of breakage in the wafer substrate during semiconductor processing. Thompson, ¶228; § V.B.2.a. A POSITA would have been motivated to implement *Dean*’s TSV arrangements to avoid alignment of TSVs and to reduce or eliminate wafer breakage. Thompson, ¶233-235; *Dean*, ¶[0039].

As *Dean* explains, “[t]hrough silicon vias (TSVs) are typically elongated vias” that may be “3 µm wide by 50 µm long,” and “when TSVs are aligned they act like perforations making it easy to break a wafer into which they are formed.” *Dean*, ¶[0017]. Such aligned TSVs are illustrated in Fig. 4 of *Dean*, which shows TSVs aligned with each other along the Y direction.

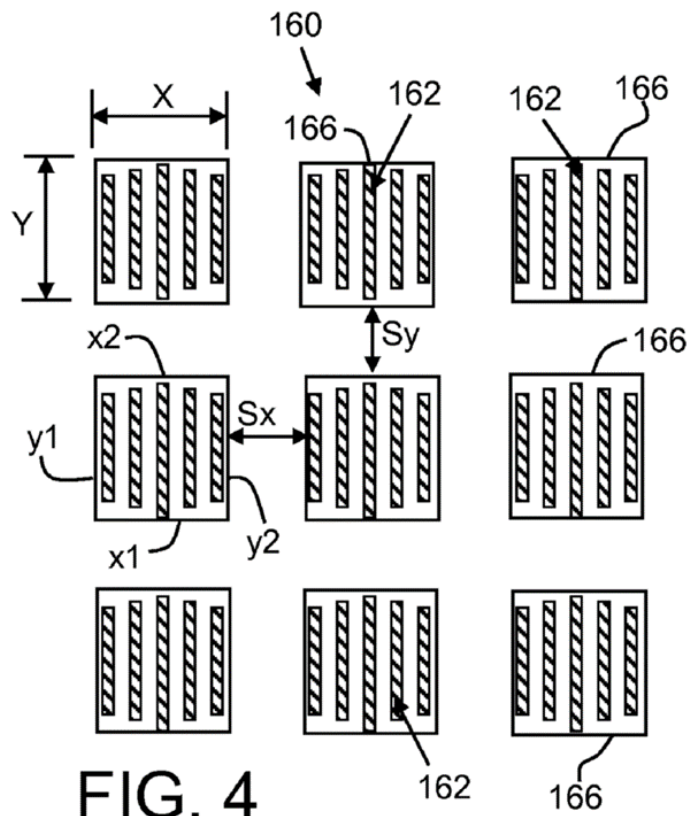


FIG. 4

Dean, Fig. 4.

To solve the problem of wafer breakage, *Dean* discloses rotating a set of vias 162 so as to be perpendicular to the original direction. *Dean*, ¶[0033]. As illustrated in Fig. 6 of *Dean* below, rotation of vias 162 in this manner results in a first group of vias aligned in a first direction X (see X direction indicated in Figure 4, above) and another group of vias aligned in a second direction Y (see Y direction indicated in Figure 4, above) perpendicular to the first direction.

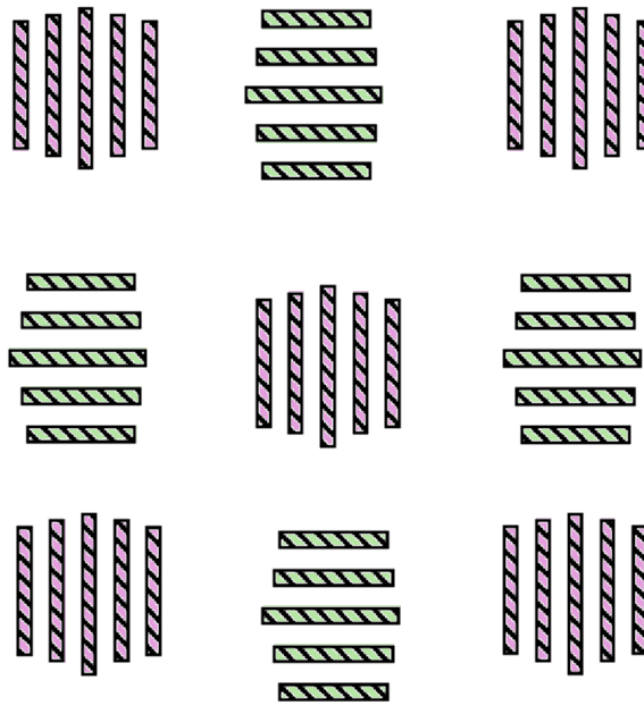


FIG. 6

Dean, Fig. 6 (annotated).

As Dr. Thompson explains, when one of the X or Y directions is a length direction, the other of the X or Y directions would correspond to a width direction, or vice-versa. Thompson, ¶238. Thus, *Dean* discloses laying out a first group of vias in width direction and a second group of vias in the length direction. *Id.*

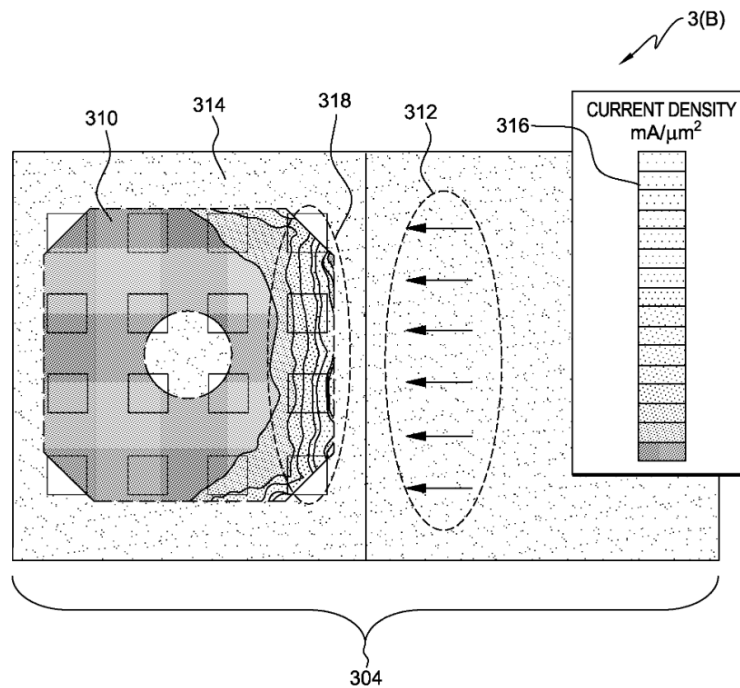
As explained above, a POSITA would have found it obvious to combine the teachings of *Dean* with *Cooney*, and the result would be a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

Thompson, ¶¶228-245. Thus, the combination of *Cooney* and *Dean* renders claims 7 and 15 obvious. Thompson, ¶246.

C. Claims 8 and 16 Are Obvious over *Cooney* and *Farooq* (Ground 3)

1. Overview of *Farooq*

Farooq discloses “a method for reducing electromigration in a circuit containing a through-silicon via (TSV) and the resulting novel structure for the TSV.” *Farooq*, Abstract. According to *Farooq*, electromigration through the TSV causes a gap to form in the material, leading to higher resistance or even circuit failure. *Id.*, 1:62-2:5, 4:10-26. Electromigration damage occurs when current crowding in a region causes the current density to exceed a certain value. *Id.*, 3:65-4:5. To reduce electromigration, *Farooq* discloses using a “truncated square” or “octagonal” shaped TSV structure, so “the current is evenly distributed over the length of the edge.” *Id.*, 4:29-34. As current (312) enters the TSV, “relatively uniform current densities can be seen” along the flat edge of the truncated square, as shown below. *Id.*, 5:15-17, 5:40-42.



Farooq, Fig. 3 (excerpted).

Farooq is analogous art to the '609 patent because *Farooq*, like the '609 patent, discloses methods of formation of TSVs in a semiconductor substrate. Compare *Farooq*, 1:18-37, 5:6-12, 6:4-19, with '609 patent, Abstract, 1:54-56, 3:1-5, 4:9-5:24; Thompson, ¶¶101-105.

2. Rationale for combining *Cooney* and *Farooq*

a. Motivation to combine

A POSITA would have been motivated to modify *Cooney*'s TSVs to include flat edges with truncated corners, as *Farooq* teaches, to ensure uniform current densities along any of the edges where current may flow. Thompson, ¶¶248-254.

As discussed earlier, a POSITA would have understood that *Cooney*'s TSVs are elongated TSVs. Thompson, ¶251. A POSITA would have ensured that *Cooney*'s elongated vias have flat edges with truncated corners, as *Farooq* teaches, because truncating the corners allow for more uniform current flow, and thus, would have less peak current density. *Id.*; *Farooq*, Fig. 3. Using a flat edge with truncated corners, as *Farooq* teaches, would ensure that “there is no leading edge ... in which current may crowd into when flowing into or out of the TSV,” thereby minimizing current crowding and ensuring uniform current densities along the flat edge of the truncated square. Thompson, ¶251; *Farooq*, 6:20-25, Fig. 3. Moreover, a POSITA would have desired to truncate the corners to reduce the stress at the corners. Thompson, ¶251 *see also* *Farooq*, 4:44-46 (noting that corners introduce “local stresses”); *Stiffler* (Ex. 1014), 561 (“beveling the outside corner with a 45° cut” reduces the local stress at the corners). But even if *Cooney*'s TSVs are not elongated TSVs, the same concern regarding current crowding or current density remains. Thompson, ¶251. A POSITA would have understood that any substantially circular TSVs would cause current to crowd at the leading edge. *Farooq*, 4:17-23. Thus, regardless if the TSVs are elongated or circular, a POSITA would have been motivated to use flat edges with truncated corners, as *Farooq* teaches, to minimize current crowding and electromigration damage. Thompson, ¶251; *Farooq*, 4:2-5.

A POSITA would have found the modification of *Cooney*'s TSVs based on *Farooq*'s teaching obvious because it would have involved nothing more than the use of a known technique—forming TSV with flat edges with truncated corners—to improve a similar device—*Cooney*'s semiconductor device—in the same way, namely, by reducing the likelihood of electromigration damage of *Cooney*'s semiconductor device. Thompson, ¶252; *KSR*, 550 U.S. at 401 (stating “a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”); *KSR*, 550 U.S. at 419-20.

a. Expectation of Success

A POSITA would have had a reasonable expectation of success in implementing the teachings of *Farooq* during the manufacture of the TSVs of *Cooney*. Thompson, ¶253. Given that both *Cooney* and *Farooq* disclose forming TSVs through a semiconductor substrate, creating flat edges with truncated corners, as *Farooq* teaches, would have been well within the skill of a person of ordinary skill in the art. *Id.* The application of *Farooq*'s principles on *Cooney*'s TSV would also have been a simple implementation of the TSV shape. *Id.* A POSITA would have had a reasonable expectation of success for the combination of *Farooq* with *Cooney* because it merely requires combining well-known prior elements according to known methods. *Id.*; *Inland Steel*, 265 F.3d at 1364 (finding

when the prior art identifies a problem and provides explicit guidance on how to fix the problem, it is reasonable to conclude that the skilled artisan would have had a reasonable expectation of success in combining the prior art.).

1. Claims 8 and 16

- a. Claims 8 and 16: “The semiconductor substrate of claim [1 or 11], wherein each of said plurality of through silicon vias has at least one chamfered corner.”**

Cooney in view of *Farooq* would have rendered obvious the additional limitations of claims 8 and 17. Thompson, ¶¶248-254. *Farooq* discloses using a “truncated square” (or flat edges with truncated corners), so “the current is evenly distributed over the length of the edge” to ensure uniform current densities and to reduce electromigration damages. *Farooq*, 4:29-34. When *Cooney*’s TSVs are fabricated to create flat edges with truncated corners, as *Farooq* teaches, the resulting TSVs have chamfered corners. *Id.*, 4:29-34, 6:4-19. Thus, the combination of *Cooney* and *Farooq* would have rendered claims 8 and 16 obvious. Thompson, ¶¶251-254.

D. Claims 8 and 16 Are Obvious over *Chen* and *Cooney* (Ground 4)

1. Overview of *Chen*

Chen relates to TSV layout to reduce the overall footprint and save space on a die’s surface. *Chen*, Abstract, ¶¶[0001], [0005]-[0008]. Specifically, *Chen* is

directed to “a system and method for manufacturing through silicon vias.” *Id.*, ¶[0001]. *Chen* notes that a semiconductor die can be connected to other die or devices through bumps. *Id.*, ¶[0002]. These bumps are “normally connected to the semiconductor die ... by layers of conductive material collectively known as under bump metallization [UBM].” *Id.* *Chen* explains that by placing the TSVs under the UBM, “less space on the surface of the die needs to be taken up by trace lines,” so that the “die may be spaced closer together,” which helps to “reduce the size of circuit components in general, leading to smaller devices overall.” *Id.*, ¶[0044]. *Chen* further explains that different layouts of the TSVs are used depending on the UBM shape, as shown below. *Id.*, ¶[0042].

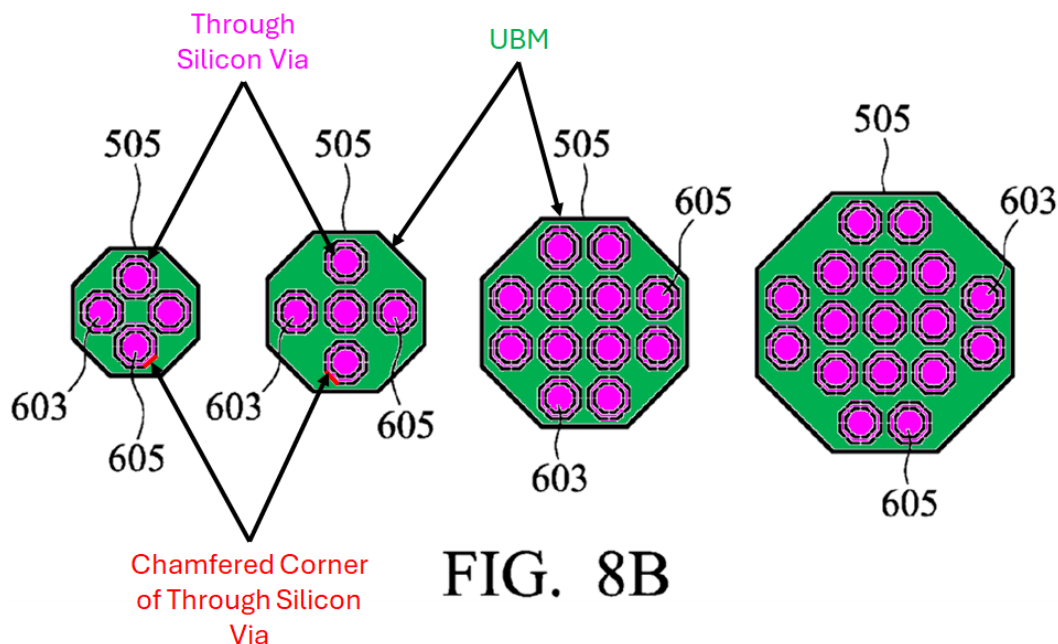


FIG. 8B

Chen, Fig. 8B (annotated).

For example, when the UBM is formed in an octagonal shape, the TSVs under the UBM are formed with chamfered corners and arranged to fit them under the UBM.

Chen, ¶[0042], Fig. 8B.

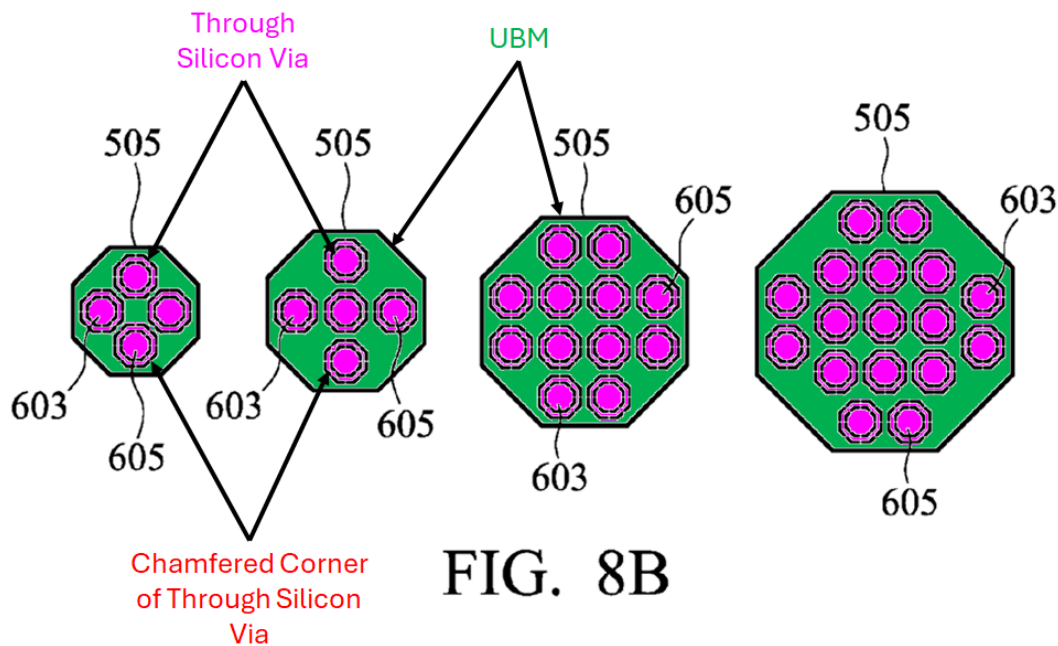
Chen is analogous art to the '609 patent because *Chen*, like the '609 patent, discloses methods of formation of TSVs in a semiconductor substrate. Compare *Chen*, Abstract, ¶¶[0001], [0006]-[0008], [0024]-[0027], with '609 patent, Abstract, 1:54-56, 3:1-5, 4:9-5:24; Thompson, ¶¶96-100.

2. Rationale for combining *Chen* with *Cooney*

a. Motivation to combine

A POSITA would have been motivated to combine *Chen*'s TSVs with *Cooney*'s aperture and sidewall profile. Thompson, ¶¶255-263. *Chen* and *Cooney* are both directed to manufacturing semiconductor substrates with TSVs.

Thompson, ¶259. *Chen* discloses "a system and method for manufacturing through silicon vias." *Chen*, ¶[0001]. *Chen* discloses that when "devices are scaled down," multiple TSVs are preferably located under the UBM with the layout of the TSVs substantially matching the UBM shape, as shown below. *Chen*, Fig. 8B.



Chen, Fig. 8B (annotated).

Cooney further discloses that as “microelectronic structure dimensions decrease,” the aperture’s particular sidewall profile “provides for ease in filing the via into the aperture, while providing for desirable geometric localization of any voids that form when filing the via into the aperture.” *Cooney*, ¶[0018].

A POSITA would have recognized the benefits of using the specific aperture and sidewall profile, as *Cooney* teaches, when the vias are arranged close together to reduce real estate in a semiconductor die, as *Chen* teaches. Thompson, ¶261. As *Cooney* explains, as “microelectronic structure dimensions decrease,” TSVs having enhanced performance are needed. *Id.*; *Cooney*, ¶[0017]. A POSITA would have been motivated to use the “irregular sidewall curvature of the extended aperture,”

as *Cooney* teaches, for aiding the filling of each TSV's aperture and to localize any void within the TSV. Thompson, ¶261; *Cooney*, ¶¶[0018], [0060], [0066].

Moreover, implementing *Cooney*'s TSVs in *Chen* would have involved nothing more than the use of a known technique—using a particular sidewall profile for the TSVs—to improve a similar device—*Chen*'s TSV—in the same way, namely, to provide ease of filling the via and optimally localizing the void in the TSVs.

Thompson, ¶261; *KSR*, 550 U.S. at 419-20; *id.* at 401.

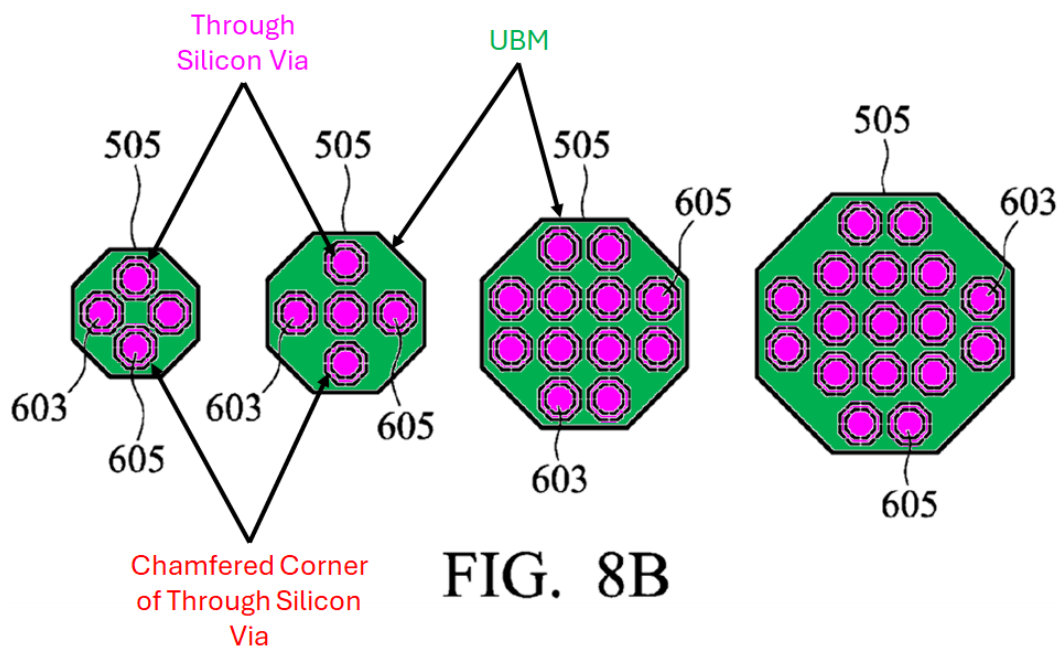
b. Expectation of Success

A POSITA would have had a reasonable expectation of success in implementing *Cooney*'s design, including the aperture with the particular sidewall profile, for the TSVs of *Chen*. Thompson, ¶262. Implementing *Chen*'s vias to take advantage of *Cooney*'s particular sidewall profile, as *Cooney* teaches, would have involved a simple geometric design that would have been well within the skill of a POSITA. *Id.* Moreover, the application of *Cooney*'s vias in *Chen*'s substrate would have been a simple implementation of the TSV shape of *Cooney* in *Chen*. *Id.* A POSITA would have had a reasonable expectation of success for the combination of *Cooney*'s teachings with *Chen* because it merely requires combining well-known prior art elements according to known methods. *Id.*; *Inland Steel*, 265 F.3d at 1364.

3. Claims 8 and 16

- a. Claims 8 and 16: “The semiconductor substrate of claim [1 or 11], wherein each of said plurality of through silicon vias has at least one chamfered corner.”

Chen in view of *Cooney* would have rendered obvious the additional limitations of claims 8 and 17. Thompson, ¶¶255-263. *Chen* discloses forming a plurality of TSVs directly under a UBM to reduce the total real estate taken on the surface of a semiconductor die, as shown below. *Chen*, ¶¶[0004], [0041].



Chen, Fig. 8B (annotated).

When *Chen*’s TSVs are fabricated using the particular sidewall profile, as *Cooney* teaches, the resulting TSVs either anticipate or alternately would have rendered obvious claims 1 and 11 in the same manner as explained above for claims 1

and 11. Thompson, ¶259. *Chen* additionally discloses, as shown in Figure 8B, that the TSVs have chamfered corners to substantially match the UBM shape. *Chen*, Fig. 8B, ¶[0042]. The use of rectangular TSVs with chamfered corners, as *Chen* teaches, was well known in the art to help minimize electromigration of the conductive material in the TSVs. Thompson, ¶258 (citing *Farooq*, 1:62-2:3, 3:65-4:5, 4:29-43). Because *Chen*'s TSVs have chamfered corners, the combination of *Chen* and *Cooney* would have rendered claims 8 and 16 obvious. Thompson, ¶¶258-263.

VI. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office's interim guidelines dated June 21, 2022 ("Interim Procedures") require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions only on July 18, 2024. Ex. 1019. Fact discovery opened only last month, and will not close until August 18, 2025, with expert discovery closing September 22, 2025. Ex. 1020, 3. The parties will not begin claim construction until March 4, 2025, and the hearing will not take place until July 8, 2025. *Id.*, 3-4.

Factor 4 favors institution because this Petition additionally challenges claims 3 and 6-18, which are not involved in the litigation. Moreover, Petitioner has not served invalidity contentions, so no overlap currently exists. Petitioner reserves the right to submit a stipulation after serving invalidity contentions.

Regarding Factors 1, 2, and 5, no stay has been requested, and trial is currently scheduled for January 5, 2026, (Ex. 1020), two months before the anticipated FWD in March 2026. In these circumstances, Factors 1, 2, and 5 are at worst neutral. *Protect Animals with Satellites v. OnPoint Sys.*, IPR2021-01483, Paper 11 at 12-13, 17 (Mar. 4, 2022). Indeed, the Board has instituted with far more time between trial and FWD. *See NetNut v. Bright Data*, IPR2021-01492, Paper 12 at 9-16 (Mar. 21, 2022) (instituting IPR without stipulation and patent owner arguing trial date six months before FWD); *Protect Animals*, IPR2021-01483, Paper 11 at 18-19 (same with patent owner arguing trial date two months before FWD); Interim Procedures, 8.

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under 35 U.S.C. §325(d)

No other proceedings involving the '609 patent are currently pending or have been brought before the Patent Office. Additionally, none of the asserted prior art references (*Cooney*, *Dean*, and *Chen*) were before the Examiner during prosecution. Thus, the same or substantially the same prior art or arguments have

not been previously presented to the Patent Office and denial of institution is not warranted under §325(d).

VII. MANDATORY NOTICES

A. Real Party-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.

B. Related Matters

HID asserted the '609 Patent in *Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al*, Case No. 2:24-cv-00140 (E.D. Tex).

The '609 Patent is not related to any known pending applications.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. GROUNDS FOR STANDING

Petitioner certifies that the '609 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. CONCLUSION

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 24, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CLAIMS APPENDIX

1. **[1pre]** A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:
 - [1a]** a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;
 - [1b-1]** a conductive filler disposed within each of said plurality of through silicon vias,
 - [1b-2]** each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,
 - [1b-3]** said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;
 - [1c-1]** wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and
 - [1c-2]** wherein said hollow center is tapered in said pinched off region.
2. The semiconductor substrate of claim 1, wherein said pinched off region is formed by tapering a bottom portion of each of said plurality of through silicon vias.

3. The semiconductor substrate of claim 1, wherein said preventing contamination during said processing is achieved by preventing contamination during polishing said bottom surface of said substrate.
4. The semiconductor substrate of claim 1, wherein said conductive filler comprises a metallic filler.
5. The semiconductor substrate of claim 1, wherein said conductive filler comprises tungsten.
6. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler fills said bottom portion, pinching off said hollow center.
7. The semiconductor substrate of claim 1, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second group of said plurality of through silicon vias are laid out in a length direction.

8. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias has at least one chamfered corner.
9. The semiconductor substrate of claim 1, further comprising a pinched off region at a top of each of said plurality of through silicon vias.
10. The semiconductor substrate of claim 1, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills bottom portion, narrowing said hollow center.
11. **[11pre]** A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:
 - [11a]** a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;
 - [11b]** a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;

[11c] wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.

12. The semiconductor substrate of claim 11, further comprising a dielectric layer disposed on said top surface of said substrate, wherein said dielectric layer has a plurality of openings, each situated over one of said plurality of through silicon vias, and having a width smaller than a width of said through silicon vias.
13. The semiconductor substrate of claim 11, wherein said conductive filler comprises a metallic filler.
14. The semiconductor substrate of claim 11, wherein said conductive filler comprises tungsten.
15. The semiconductor substrate of claim 11, wherein a first group of said plurality of through silicon vias are laid out in a width direction and a second

group of said plurality of through silicon vias are laid out in a length direction.

16. The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias has at least one chamfered corner.
17. The semiconductor substrate of claim 11, wherein said another pinched off region is tapered at said bottom of each of said plurality of through silicon vias.
18. The semiconductor substrate of claim 11, wherein each of said plurality of through silicon vias is tapered at a bottom portion such that said conductive filler incompletely fills said bottom portion, narrowing said hollow center.

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,106.

Dated: September 24, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on September 24, 2024, a copy of the foregoing Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1014 and 1016-1024 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 9,147,609:

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Date: September 24, 2024

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