

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,147,609

Filing Date: March 8, 2012

Issue Date: September 29, 2015

Inventors: Hadi Jebory and David J. Howard

Title: THROUGH SILICON VIA STRUCTURE, METHOD OF
FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

PATENT OWNER'S RESPONSE

Case No. IPR2024-01404

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung’s Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants’ Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	Merriam-Webster Dictionary definition for the word “taper.”
2005	Dictionary.com definition for the word “tapered.”
2006	Oxford English Dictionary definition for the word “tapered.”
2007	Transcript of June 17, 2025 Deposition of Dr. Scott E. Thompson
2008	<i>Thermal Stresses around Void in Through Silicon Via in 3D SiP</i> by T. Kinoshita, et al., published in the 2014 International Conference on Electronics Packaging (April 2014)
2009	<i>3D-interconnect: Visualization of Extrusion and Voids Induced in Copper-Filled Through-Silicon Vias (TSVs) at Various Temperatures Using X-Ray Microscopy</i> , by Kong et al., published in <i>Microelectronic Engineering</i> 92 (2012),
2010	<i>TSV Cu Filling Failure Modes and Mechanisms Causing the Failures</i> , by J.W. Choi, et al., published in <i>IEEE Transactions on Components, Packaging, and Manufacturing Technology</i> , Vol. 4, No. 4 (April 2014)

Exhibit No.	Description of Document
2011	<i>Low Stress TSV Arrays for High-Density Interconnection</i> , by Jiao, et al. (2022)
2012	Declaration of Mr. John Berg

I. INTRODUCTION

On September 24, 2024, Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) submitted a Petition (Paper 1, “Petition” or “Pet.”) to institute *inter partes* review (“IPR”) of U.S. Patent No. 9,147,609 (Ex. 1001, the “’609 Patent”), challenging Claims 1-18 (the “Challenged Claims”). The Petition asserts that: (i) Claims 1-6, 9-14, 17, and 18 would have been anticipated or rendered obvious over U.S. Patent Application Publication No. US 2009/0278237 to Cooney, III et al. (“Cooney” or Ex. 1004); (ii) Claims 7 and 15 are obvious over Cooney and U.S. Patent Application Publication No. US 2011/0057319 to Dean, Jr. et al. (“Dean” or Ex. 1010); (iii) Claims 8 and 16 are rendered obvious over Cooney and U.S. Patent No. 8,237,288 to Farooq et al. (“Farooq” or Ex. 1016); and (iv) Claims 8 and 16 are rendered obvious over U.S. Patent Application Publication No. US 2010/0032843 to Chen et al. (“Chen”) or Ex. 1011) and Cooney. The Board should confirm patentability of all Challenged Claims for the following reasons:

Every claim of the ’609 Patent requires through-silicon via with a hollow center that reduces thermal stress in the surrounding silicon substrate, which the Petition does not demonstrate is present in the prior art. First, the Petition argues that

the functional limitation should be completely ignored. But basic tenets of claim construction require each limitation of the claims to be given patentable weight. The Petition next argues that the prior art anticipates this claim element, despite an admitted lack of disclosure in that prior art regarding the function of an “optional void” in a through-silicon via. Finally, the Petition claims that this claim element can be backfilled with the knowledge of a person of ordinary skill in the art that all voids in through-silicon vias necessarily reduce thermal stress in the surrounding substrate. But this assumption regarding the knowledge of the person of ordinary skill in the art is faulty—indeed, contemporary extrinsic evidence shows that in certain circumstances the presence of a void in a through-silicon via can *increase* thermal stress. Neither Petitioner nor its expert provide any analysis of the characteristics of the optional void in the prior art, instead merely relying on the flawed assumption that all voids decrease thermal stress. Therefore, the Petition fails to show that the person of ordinary skill in the art would have found it obvious that the “optional void” disclosed in the prior art is a hollow center that reduces thermal stress in the surrounding semiconductor substrate.

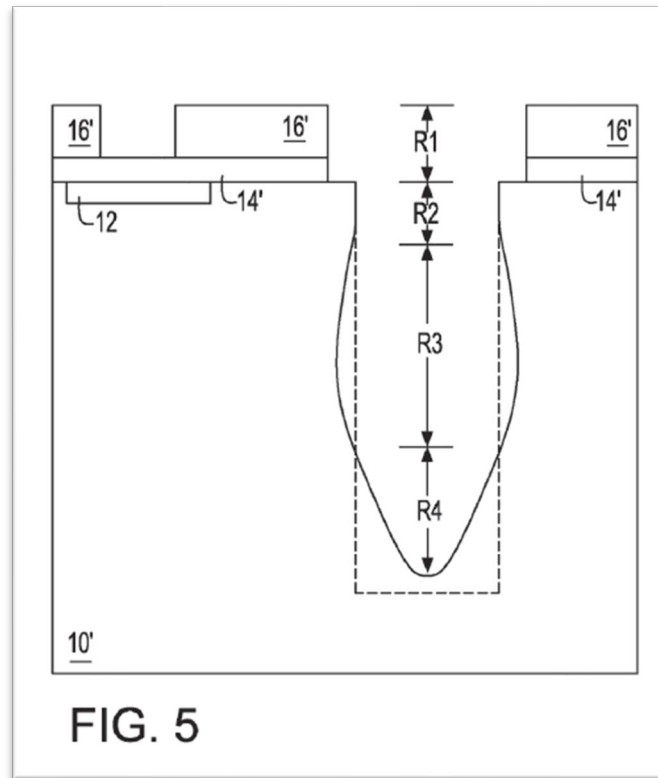
The Board should, therefore, confirm patentability of all of the Challenged Claims.

Fig. 4 illustrates an embodiment of the '609 Patent's claimed invention. *Id.*, 4:9-5:2. The pinched off region 438 includes a tapered portion that allows the conductive filler to completely fill the bottom of the TSV. *Id.*, 4:48-54. The hollow center 432 includes a section that tapers conically within the pinched off region. *Id.*, 4:48-5:2; Fig. 4.

III. THE RELEVANT ALLEGED PRIOR ART

A. Cooney

U.S. Patent Application Publication No. US 2009/0278237 to Cooney, III et al. (Ex. 1004) is titled "Through Substrate Via Including Variable Sidewall Profile" and published on November 12, 2009. *Cooney* is directed to forming a via in a semiconductor substrate. Ex. 1004, Abstract, ¶ [0002]. *Cooney's* via is torpedo shaped, and composed of four regions. *Id.*, ¶¶ [0042], [0050]-[0055], FIGS. 4-6. The regions include comparatively wide linewidth regions R1 and R3, as well as a tapered region R4. *Id.*, ¶ [0051], FIG. 5.



Ex. 1004, FIG. 5. The geometries of the various regions aid in filling the aperture with a conductor layer, and in confining any voids to the R3 region. *Id.*, ¶¶ [0051] (“the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3”), [0055], [0060], FIG. 6.

FIG. 6 of *Cooney* shows a “conductor layer 24 with an **optional void** 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.” *Id.*, ¶ [0055] (emphasis added).

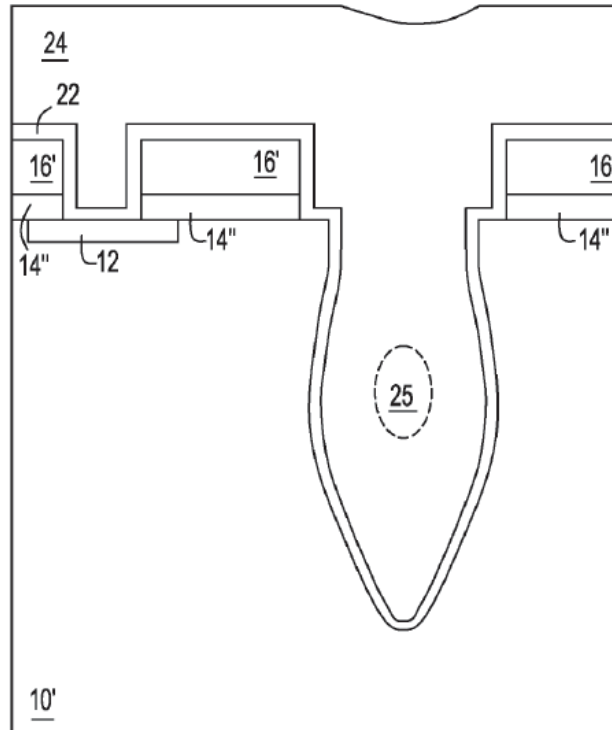


FIG. 6

Cooney, FIG. 6, showing “optional void” 25

Cooney notes that the optional void 25 is “localized to the second comparatively wide region R3 of the extended aperture.” *Id.*, ¶ [0060]. It also notes that “[t]he constricted region provides for surface closure of any voids that may form in the second comparatively wide region.” *Id.*, ¶ [0066]. *Cooney* does not describe or mention the purpose of the “optional void 25.”

B. Dean

U.S. Patent Application Publication No. US 2011/0057319 to Dean, Jr., et al. (Ex. 1010) published on March 10, 2011. *Dean* relates to arranging through silicon vias in an IC layout to result in less wafer breakage. Ex. 1010, Abstract.

C. Farooq

U.S. Patent No. 8,237,288 to Farooq et al. (Ex. 1016) is titled “Enhanced Electromigration Resistance in TSV Structure and Design” and issued on August 7, 2012. Farooq relates to structures and connections of TSVs. Ex. 1016, Abstract.

D. Chen

U.S. Patent Application Publication No. US 2010/0032843 to Chen et al. (Ex. 1011) published on February 11, 2010. Chen relates to a particular layout of TSVs. Ex. 1011, Abstract.

IV. LEVEL OF ORDINARY SKILL IN THE ART

As Mr. Berg explains, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. Additional formal education (such as Master of Science degrees) would compensate for less technical experience and vice versa. Ex. 2012 (Berg Declaration), ¶¶ 22-26.

Petitioner’s proposed level of skill in the art – “at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems”—imposes a requirement of a master’s degree. Pet., 9-10. As Mr. Berg explains, engineers working in this field, and implementing designs such as that described in the ’609 Patent, typically have bachelor’s degrees. Ex. 2012, ¶ 24. Such engineers are the target audience for the ’609 Patent, and thus, a POSITA need not have a master’s degree. *Id.*

V. CLAIM CONSTRUCTION

Petitioner states that “no terms need construction to resolve the controversy in this forum” and, therefore, proposes no claim terms or proposed constructions. Pet. at 8. However, Petitioner claims that certain functional limitations in the Challenged Claims can be ignored as statements of intended use. *See id.* at 20, 24–25. Patent Owner contends that these limitations should not be ignored and, therefore, Patent Owner believes that claim construction disputes exist regarding the terms “to reduce thermal stress in said semiconductor substrate,” “to provide space for said conductive filler to expand inward,” and “to prevent contamination during processing of said semiconductor substrate.” Petitioner also claims that the prosecution history should be interpreted in a manner that disavows claim scope

regarding the function of the claimed void. Patent Owner addresses each of these in turn.

A. Functional Limitations

1. “to reduce thermal stress in said semiconductor substrate”

Claim 1 of the '609 Patent requires, *inter alia*, “a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center *to reduce thermal stress in said semiconductor substrate*. '609 Patent, cl. 1 (emphasis added). Claim 11 requires “each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward *for reducing thermal stress in said semiconductor substrate*.” *Id.*, cl. 11 (emphasis added). Petitioner claims that these phrases “state[] the use of or explanation for the hollow center and should be entitled to no patentable weight over the prior art.” Pet. at 20.

Patent Owner disagrees that the reduction of thermal stress is a statement of the use or explanation for the hollow center; rather, the claim should be properly interpreted to give weight to this limitation. Ex. 2012, ¶¶ 49-54. Not all hollow centers and not all configurations of vias reduce thermal stress in all semiconductor

substrates, and evidence cited by Petitioner supports this. For example, U.S. Patent Application Publication No. 2009/0302480 to Birner et al. (Ex. 1022) states that “the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum defectivity arising from thermal or other stress related defects.” Ex. 1022, ¶ [0037]. *Birner* also provides a discussion regarding how to select the size and shape of the fill material in order to create a void that reduces thermal stress. *Id.* ¶ [0038]. *Birner* notes that:

As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material 50 is selected relative to the dimension of the tailored void 90. For example, a fraction of the fill material 50 (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1 *b*, this fraction of the fill material 50 (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} . The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material 50 (α_{FM}) and the tailored void (α_V) as $f_{FM} = (\alpha_{Si} - \alpha_V) / (\alpha_{FM} - \alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM} \approx 0$, the fraction $f_{FM} = \alpha_{Si} / \alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening $250 r_{TSV}$. In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments, thicker fill material can be used as stress up to a certain critical limit (e.g., critical shear stress) can be safely accommodated. For example, the stress produced during a small increase in temperature may not be significant.

Hence, in various embodiments, a numerical simulator is used to design the shape of the voids. In such embodiments, a suitable thickness is calculated numerically to minimize, for example, stress concentrations during subsequent processing. In some embodiments, a more sophisticated analysis utilizing 2D or 3D simulations using finite element simulators determines the appropriate shape and structure of the tailored void 90 relative to the fill material 50. Such numerical calculations can account for changes in stress in different regions, for example, in the corners. Suitable metrics, such as Von Misses criterion, based on the stress tensor may be used to monitor the stress in the structure.

Id. The POSITA would have understood from this reference that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur. Ex. 2012, ¶ 49.

As another example, shown in the paper *Thermal Stresses around Void in Through Silicon Via in 3D SiP* by T. Kinoshita, et al., which was published in the 2014 International Conference on Electronics Packaging (April 2014) (Ex. 2008, “Kinoshita”), under operational conditions the presence of a void can increase thermal stresses inside the TSV, which could in turn increase thermal stresses in the silicon substrate. Ex. 2012, ¶¶ 50-53.

Figure 5 of *Kinoshita* is shown below:

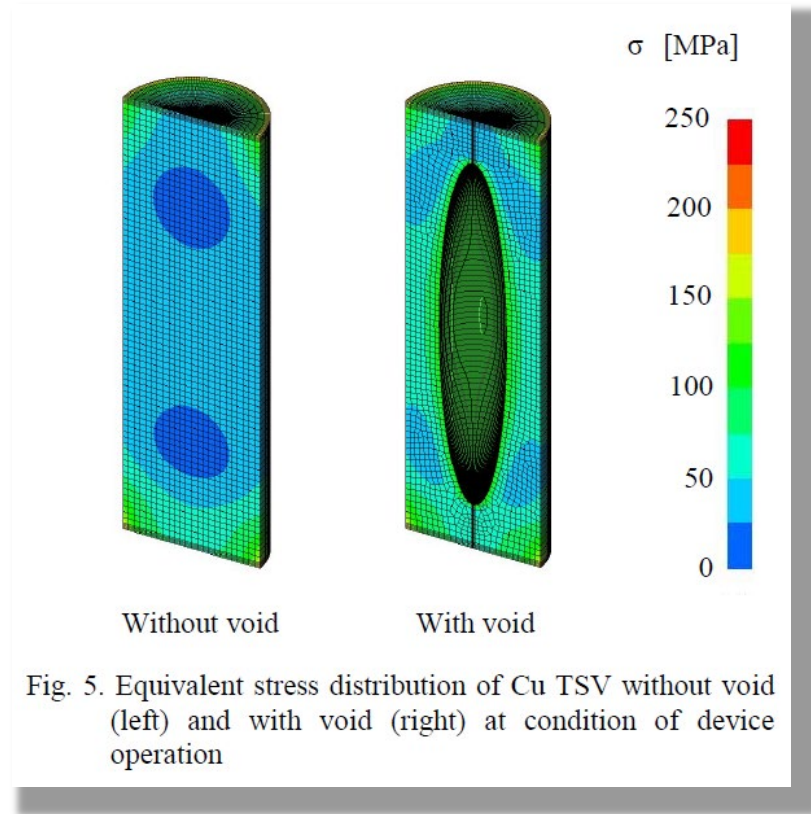


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

As shown in Figure 5 and explained by Kinoshita:

In the case of the TSV structure without voids, the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa.

...

In case of the TSV structure with a void, the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa. It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper.

Ex. 2008, at 107 (emphasis added). Because *Birner* and *Kinoshita* show that the presence of a void in a through-silicon via does not inherently mean that the thermal stress on the semiconductor substrate is reduced, Petitioner's argument that the functional language is merely a statement of intended use for the hollow center and entitled to no patentable weight is improper.

The claim language in the '609 Patent is intended to convey the purpose of the hollow center: to reduce thermal stress in the substrate.

Functional language generally limits the claim to a structure when the functional language describes something about the structure of the apparatus rather than merely listing its intended or preferred uses. *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1363–64 (Fed. Cir. 1999) (holding that claim term “for substantially preventing movement therebetween at least in a horizontal plane” dictates the meaning of “permanently affixed” to mean that it prevents movement in a horizontal plane.). Here, Petitioner does not present any evidence that *all* voids reduce thermal stress in semiconductor substrates, nor can it. Rather, Petitioner states that the '609 Patent “does not identify any features of the hollow center that contribute to thermal stress reduction in the semiconductor substrate.” Pet. at 20. This is not the standard by which to evaluate the functional limitation. The '609 Patent does state that the

hollow center “reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions” and that “[s]uch reduction in thermal and mechanical stress reduces cracking in substrate 412.” ’609 Patent, 4:60-67. The hollow center portion in Claim 1 must therefore be sufficient to reduce thermal stress in the semiconductor substrate, or it will not be the claimed “hollow center.” *See Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 381 F.3d 1111, 1117–20 (Fed. Cir. 2004) (holding that functional relationship “operatively connected” means that the claimed components must be “connected in a way to perform a designated function.”).

Petitioner’s case law is unavailing. First, Petitioner cites to *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999) for the proposition that “a scientific explanation for the prior art’s functioning, does not render the old composition patentably new.” Pet. at 20. In that case, the claim term at issue was “sufficient aeration . . . to enhance sensitivity.” The trial record was clear and the inventor himself testified that air from any source would enhance sensitivity and, thus, the district court’s construction that the “sufficient aeration” term would

include both interstitial and porous air was not error.¹ *Id.* at 1347. Petitioner next cites to *In re Sinex*, 309 F.2d 488 (C.C.P.A. 1962), but this case merely holds that a preamble is not limiting because it is merely a statement of intended use and “does not qualify or distinguish the structural apparatus claimed over the reference.” *Id.* at 492. Petitioner’s final case, *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019) is even less compelling. In that case, a preamble was also held to be not limiting and the court merely recited the well-known legal principle that intended-use preamble language cannot be given defining effect. But here, the functional limitation “to prevent thermal stress in said semiconductor substrate” is not in the preamble, and does significantly more than just state a scientific explanation. It specifically claims that the hollow center must cause a reduction in thermal stress in the semiconductor substrate. Therefore, contrary to Petitioner’s assertion, this claim term should be given patentable weight, and should be construed to require the hollow center to cause reduction in thermal stress.

¹ Notably, the court in *Atlas Powder*, 190 F.3d at 1346, did not hold that all air increased sensitivity, as Petitioner in this case contends on a much thinner record that all voids regardless of their size or configuration reduce thermal stress in the substrate.

The remaining functional limitations should be given patentable weight for the same reasons.

B. Prosecution History Acquiescence

Petitioner also claims that the prosecution history should be interpreted to mean that the Applicant admitted that all hollow centers reduce thermal stress in the semiconductor substrate. Pet. at 21-22 (“And these very teachings were recognized during prosecution of the ’609 patent. There, the Examiner cited *Edelstein* and *Beyne* for the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate, and Patent Owner acquiesced to the rejection and did not rebut the Examiner’s statement.”). Although it cites no cases, Patent Owner interprets this argument to be one under the doctrine of acquiescence. But a patentee is “not required to fight tooth and nail every possibly adverse thought an examiner commits to paper, nor to advance redundant arguments for patentability.” *TorPharm, Inc. v. Ranbaxy Pharms., Inc.*, 336 F.3d 1322, 1330 (Fed. Cir. 2003). That the applicant chose to amend its claim to recite additional limitations rather than argue every position advanced by the Examiner is not an acquiescence that *all* hollow centers in *all* TSVs reduce thermal stress in the surrounding substrate, as apparently advocated by Petitioner.

VI. PETITIONER’S CITED ART DOES NOT ANTICIPATE OR RENDER OBVIOUS THE CHALLENGED CLAIMS

To anticipate a claimed invention, a prior art reference must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “However, a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (C.C.P.A. 1962)).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole

would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983).

The Board has held that a failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. *See, Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Decision Denying Institution of *Inter Partes* Review, Paper 9 at 9-10 (P.T.A.B. June 26, 2015) (denying institution for failure to identify the differences between the claimed subject matter and the prior art).

In arriving at an obviousness determination, the Board must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims and a relevant, skilled artisan not only could have made, but would have been motivated to combine all the prior art references in the way the patent claims and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have the motivation to combine those references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical*

Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co., 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual finding as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a person of skill in the art would have had a reasonable expectation of success from such a combination). This combinability determination, as supported by an articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references” *Innogenetics, N.V. v. Abbott Lab’ys.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

To demonstrate inherent obviousness, an inherent limitation must necessarily be present in the combination of references. *See Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376 (Fed. Cir. 2019); *LBT IP I LLC v. Apple Inc.*, No. 2022-1613,

2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023). It is not enough to merely show that it is likely to be present. *Id.*

A. Grounds 1A and 1B Fail Because the “Optional Void” in *Cooney* Does Not Reduce Thermal Stress in the Substrate

Claims 1 and 11 each require a plurality of through-silicon vias that have “a hollow center [] to reduce thermal stress in said semiconductor substrate.”² The “optional void” in *Cooney* does not reduce thermal stress in the semiconductor substrate. Petitioner and Dr. Thompson’s analysis of the “optional void” in *Cooney* is not sufficient to determine whether it decreases thermal stress. Grounds 1A and 1B can be analyzed together, because they are both based on Petitioner’s foundational assumption that *all* voids decrease thermal stress in *all* configurations of *all* TSV’s, which is incorrect.

² Claim 1 requires “each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward” while Claim 11 requires “each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate.” The functional result of both of these claims is that the hollow center must have certain properties that reduce thermal stress in the substrate and, therefore, these claims can be analyzed together.

At the outset, *Cooney* cannot anticipate any claim of the '609 Patent as contended by Petitioner because, as admitted by its expert, *Cooney* does not mention “thermal stress” and does not discuss the purpose of the “optional void” in its disclosure. Ex. 2007 (Thompson transcript), 30:25-31:11 (“A void that’s buried obviously reduces stress as the tungsten expand [sic] and squashes – squashes the void and expands inward into the void.”) *Net MoneyIN, Inc.*, 545 F.3d at 1369 (“Because the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983))).

Petitioner attempts to backfill this missing limitation with a statement that “*Cooney*’s void 25, like the claimed hollow center would similarly reduce thermal stress in the semiconductor substrate.” Pet., 21 (citing Ex. 1002, ¶ 123). But Dr. Thompson’s opinion is merely that thermal stress is reduced because of the presence of the optional void in *Cooney*. Ex. 1002, ¶ 123. This is not only incorrect, but it is improper in an anticipation ground to use the knowledge of a person of skill in the art to fit prior art that is missing limitations into the claim language. For

Cooney to anticipate based on this disclosure, Petitioner would need to show that *Cooney*'s void ***necessarily*** reduces thermal stress. *Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382 (Fed. Cir. 2019) (“Inherency . . . may not be established by probabilities or possibilities.” (quoting *Par Pharm., Inc. v. TWI Pharm., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014))).

The “optional void” in *Cooney* does not anticipate or render obvious any claim for several reasons. First, Petitioner and Dr. Thompson rely on a foundational assumption that all voids in all TSVs reduce thermal stress in the substrate, and this assumption is flatly contradicted by extrinsic evidence. Second, a POSITA would understand that a “void” is different from a hollow center, and is too small to reduce thermal stress. Third, the torpedo shape used to create *Cooney*'s void actually increases thermal stress by requiring additional metal filler and focusing forces on a smaller part of the silicon, as compared to a typical straight TSV.

1. All Voids Do Not Decrease Thermal Stress

According to Petitioner and Dr. Thompson, all voids in a through-silicon via would reduce the required thermal stress. *See* Ex. 1002, ¶ 123 (“Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney*'s void 25 reduces thermal stress in *Cooney*'s substrate”); Ex. 2007, 30:25-31:11 (“A

void that's buried obviously reduces stress as the tungsten expand [sic] and squashes – squashes the void and expands inward into the void.”). But this is wrong.

According to Mr. Berg, not all voids or all hollow centers in through-silicon vias decrease thermal stress. Ex. 2012, ¶¶ 47-53; 63-69. Evidence relied upon by Petitioner supports this. For example, U.S. Patent Application Publication No. 2009/0302480 to Birner et al. (Ex. 1022) states that “the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum defectivity arising from thermal or other stress related defects.” Ex. 1022, ¶ [0037]. *Birner* also provides a discussion regarding how to select the size and shape of the fill material in order to create a void that reduces thermal stress. *Id.* ¶ [0038]. *Birner* notes that:

As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material 50 is selected relative to the dimension of the tailored void 90. For example, a fraction of the fill material 50 (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1 *b*, this fraction of the fill material 50 (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} . The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material 50 (α_{FM}) and the tailored void (α_V) as $f_{FM}=(\alpha_{Si}-\alpha_V)/(\alpha_{FM}-\alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM}\approx 0$, the fraction $f_{FM}=\alpha_{Si}/\alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening r_{TSV} . In other words, a partial fill that covers about

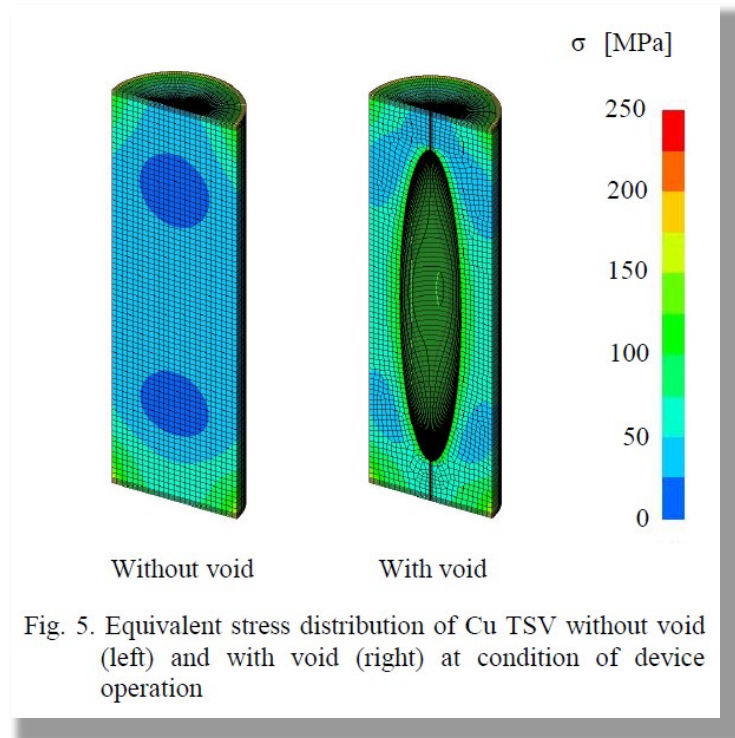
15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments, thicker fill material can be used as stress up to a certain critical limit (e.g., critical shear stress) can be safely accommodated. For example, the stress produced during a small increase in temperature may not be significant. Hence, in various embodiments, a numerical simulator is used to design the shape of the voids. In such embodiments, a suitable thickness is calculated numerically to minimize, for example, stress concentrations during subsequent processing. In some embodiments, a more sophisticated analysis utilizing 2D or 3D simulations using finite element simulators determines the appropriate shape and structure of the tailored void 90 relative to the fill material 50. Such numerical calculations can account for changes in stress in different regions, for example, in the corners. Suitable metrics, such as Von Mises criterion, based on the stress tensor may be used to monitor the stress in the structure.

Id. The POSITA would have understood from this reference that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur. Ex. 2012, ¶ 49.

Additionally, as shown in the paper *Thermal Stresses around Void in Through Silicon Via in 3D SiP* by T. Kinoshita, et al., which was published in the 2014 International Conference on Electronics Packaging (April 2014) (Ex. 2008, “Kinoshita”), under operational conditions the presence of a void can increase thermal stresses inside the TSV, which would in turn increase thermal stresses in the

silicon substrate. Ex. 2012, ¶ 64.

FIG. 5 of *Kinoshita* is shown below:



Ex. 2008, FIG. 5.

As shown in FIG. 5 and explained by *Kinoshita*:

In the case of the TSV structure without voids, the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa.

...

In case of the TSV structure with a void, the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa. It was larger than the stress obtained for the case

of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper.

Ex. 2008, at 107 (emphasis added).

As can be seen, the “with void” TSV structure in *Kinoshita* exhibits higher stress levels along the edges of the TSV as compared to the non-voided TSV, and this stress is transferred directly to the substrate. Ex. 2012, ¶¶ 54, 66. *Kinoshita* also notes that “[i]n the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa,” indicating that the presence of a void does not reduce the stress on the inside of the substrate. Ex. 2008, at 107; Berg Decl., ¶ 67. Due to the POSITA’s knowledge of void characteristics at least through *Birner* and *Kinoshita*, Dr. Thompson’s assumption that thermal stress is reduced merely through the presence of the void is incorrect, and insufficient. *Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382-83 (Fed. Cir. 2019).

In order to determine whether the optional void in *Cooney* decreases thermal stress in the substrate, Dr. Thompson would have needed to perform *some* analysis of the specific features in *Cooney*, rather than simply relying on the incorrect assumption that all voids decrease thermal stress in the substrate. Ex. 2012, ¶ 68. *Cooney* does not provide the POSITA with the information necessary to determine whether the optional void decreases thermal stress, at least because the relative size

of the void as compared to the size of the TSV and the size of the liner layer is not given. *Id.* Because of this lack of analysis, Petitioner and Dr. Thompson have not shown that the optional void in *Cooney* decreases thermal stress.

Additionally, *Cooney's* use of the term “void” implies a very small imperfection in the filling of the torpedo shaped TSV, and not a large hollow center that reduces thermal stress. According to Mr. Berg, the POSITA when presented with the teachings in *Cooney* would have known that a “void” is generally understood to be a very small “pinhole” type of defect that occurs when a TSV is incompletely filled. *Id.*, ¶ 69. For example, a paper contemporary to the '609 Patent discusses voids as “defect[s]” that need to be further studied. Ex. 2009, Kong et al., *3D-Interconnect: Visualization of Extrusion and Voids Induced in Copper-Filled Through-Silicon Vias (TSVs) at Various Temperatures Using X-Ray Microscopy*, Microelectronic Engineering 92 (2012), at 27 (“voids and other defects in the TSVs on the extrusion phenomenon should be made a topic of further study”). Figs. 3-6 of this paper show the size of typical voids in a 4 micrometer TSV:³

³ See also Ex. 2010, J.W. Choi, et al., *TSV Cu Filling Failure Modes and Mechanisms Causing the Failures*, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: “If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed.”

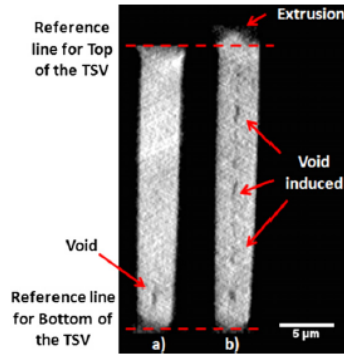


Fig. 3. XY plane at the center of 4 μm TSV before (a) and after 225 °C annealing (b).

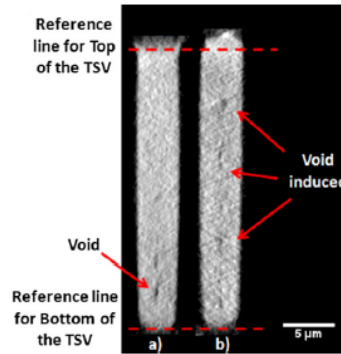


Fig. 5. XY plane at the center of 4 μm TSV before (a) and after 300 °C annealing (b).

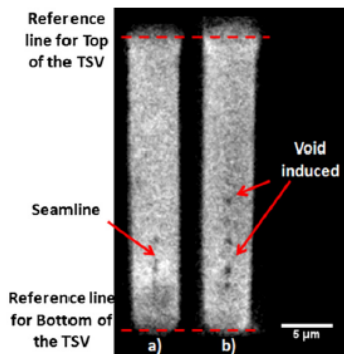


Fig. 4. XY plane at the center of 5 μm TSV before (a) and after 225 °C annealing (b).

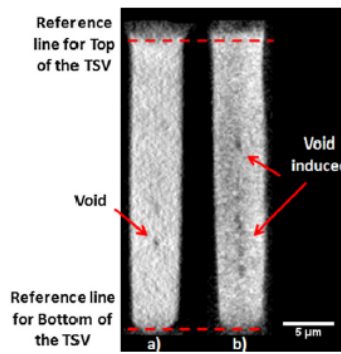


Fig. 6. XY plane at the center of 5 μm TSV before (a) and after 300 °C annealing (b).

Aside from the Figure in *Cooney*, the reference provides the POSITA with no additional information or guidance regarding the size of the void. Ex. 2012, ¶ 70. Therefore, the POSITA would not have understood *Cooney's* use of the term “void” to mean a hollow center that reduces thermal stress, as required by Claims 1 and 11 of the '609 Patent. *Id.*

2. The Shape of Cooney's TSV Increases Thermal Stress

The optional void in *Cooney* is created by incompletely filling *Cooney's*

TSV.⁴ Ex. 1004, ¶ [0055]. According to Mr. Berg, the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV. Ex. 2012, ¶ 71. This is because filling this bulge requires additional metal to fill the TSV. *Id.* Because there is more metal, it will increase by a greater factor at a given temperature than a straight TSV with less metal. *Id.* And the torpedo shape itself can increase thermal stresses, by focusing stress on certain portions of the substrate rather than spreading them out along the entire TSV. *Id.* Dr. Thompson did not analyze the shape of the void in *Cooney*, merely relying on the discredited assumption that all voids decrease thermal stress, which is contradicted by *Birner* and *Kinoshita*. Therefore, for this additional reason, Petitioner has not met its burden to show that *Cooney* anticipates or renders obvious any Challenged Claim.

3. Dr. Thompson Does Not Analyze the Size of Cooney's Void

Cooney provides no basis to make a conclusion regarding the size of the optional void aside from the Figures themselves. And consulting such Figures is

⁴ Ex. 2010, J.W. Choi, et al., *TSV Cu Filling Failure Modes and Mechanisms Causing the Failures*, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: “If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed.”

improper. Petitioner’s analysis of the Figures in *Cooney* also fails because it interprets dimensionality from an exemplary figure. Absent disclosure in the specification to the contrary, patent drawings cannot be used to show specific sizes of elements. *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“The [] patent is devoid of any indication that the proportions of the groove and fins are drawn to scale. . . . Under our precedent . . . patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”). The Petition makes no attempt to analyze the size of the optional void in relation to the size or shape of the torpedo shaped via, and therefore an attempt to interpret this size from the Figures is improper.

According to Mr. Berg, the POSITA would have recognized that a “void” in a TSV is typically an artifact of processing caused by incomplete filling of the TSV. Ex. 2012, ¶ 72. Rather than desirable features, voids are typically to be avoided.⁵ *Id.* Voids, as typically understood by the POSITA, are not large enough to have any

⁵ Ex. 2010, J.W. Choi, et al., *TSV Cu Filling Failure Modes and Mechanisms Causing the Failures*, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: “If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed.”

appreciable impact on the reduction of thermal stress in the semiconductor substrate. *Id.* (citing Ex. 2011). A “void” is different from a hollow center. Aside from the Figure in *Cooney*, *Cooney* does not present any data or information necessary to inform the POSITA as to whether the optional void is large enough to decrease thermal stress in the substrate, and therefore Dr. Thompson did not have sufficient information upon which to base his opinions.

For this additional reason, *Cooney* does not anticipate or render obvious any asserted claims.

4. The References Allegedly Disclosing the Knowledge of a POSITA Are Insufficient

Dr. Thompson, in an apparent recognition of the weakness in *Cooney*, opines that the POSITA “would have recognized that it was well known in the art that the presence of a void in a TSV reduces thermal stress in the surrounding substrate.” Ex. 1002, ¶ 125. Dr. Thompson also cites to two references that apparently explain this feature, U.S. Patent Application Publication No. 2003/0111733 to Pogge et al. (Ex. 1005) and U.S. Patent Application Publication No. 2006/0027934 to Edelstein et al. (Ex. 1006) *Id.* Neither *Pogge* nor *Edelstein* disclose that voids reduce thermal stresses in the semiconductor substrate. Ex. 2012, ¶¶ 73-77.

Pogge discloses a through-silicon via structure filled with copper and surrounded by several additional layers. *Pogge*'s vias include an oxide layer 21, a trench liner 22, and a layer of copper 23, then another layer of copper 24 that fills the void. Ex. 1005, ¶¶ [0026]-[0027]. *Pogge* does state that the void "has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature." *Id.*, ¶ [0027]. However, *Pogge* does not mention or state that the stresses would be borne by the semiconductor substrate. Ex. 2012, ¶ 74. Even if *Pogge* does teach that thermal stresses are relieved by the void in the particular device disclosed in *Pogge*, it does not teach that the POSITA would have known that all voids decrease thermal stress in all TSVs because, as discussed above, that assumption by Dr. Thompson is not correct in view of the disclosures of *Birner* and *Kinoshita*. *Id.*, ¶ 74.

Edelstein similarly does not inform the POSITA that a void in a TSV can be used to protect the substrate from thermal stresses. *Id.*, ¶ 75. *Edelstein*, rather, discloses that a "through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures." Ex. 1006, ¶ 47. *Edelstein*'s discussion is entirely centered around removing mechanical stresses, not thermal

stresses, and in any event, *Edelstein* also never discloses the reduction of stress (whether mechanical or thermal) in the substrate itself. Ex. 2012, ¶ 75. And, even if *Edelstein* does teach that thermal stresses are relieved by the void in the particular device disclosed in *Edelstein*, it does not teach that the POSITA would have known that all voids decrease thermal stress in all TSVs because, as discussed above, that assumption by Dr. Thompson is not correct in view of *Birner* and *Kinoshita*. *Id.*, ¶ 75.

The Petition's attempt to create disclosure in the prior art where none exists through the knowledge of a POSITA is, at best, incomplete. While the POSITA may have understood that some voids in some circumstances can decrease thermal stress in the surrounding substrate, this does not alone render the Challenged Claims of the '609 Patent obvious without further analysis.

The Petition also states that "if not explicitly disclosed, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*'s TSV to cause a reduction in the thermal stress in the surrounding substrate." Pet., 22. But aside from repeating the same arguments that voids *can* relieve thermal stress in the substrate, the Petition makes no attempt to show that the particular void in *Cooney* reduces thermal stress except for repeating the flawed assumption that there were

“well-known thermal stress relieving behavior of voids in TSVs.” *Id.* Because this assumption is not correct, the Petition fails to show that the optional void in *Cooney* reduces thermal stress in the substrate.

Therefore, *Cooney* does not anticipate or render obvious any of the Challenged Claims, and Grounds 1A and 1B both fail.

B. Ground 2 Fails Because it Does Not Cure the Deficiencies of Ground 1

Ground 2 asserts obviousness based on *Cooney* and *Dean* as to dependent Claims 7 and 15. Pet., 57-70. Ground 2 explicitly relies on the flawed Ground 1 analysis and does not assert that including *Dean* overcomes the deficiencies of Ground 1. Pet., 66; Ex. 2012, ¶ 77. Accordingly, Ground 2 also fails.

C. Ground 3 Fails Because it Does Not Cure the Deficiencies in Ground 1

Ground 3 asserts obviousness based on *Cooney* and *Farooq* as to dependent Claims 8 and 16. Pet., 70-74. Ground 3 does not assert that including *Farooq* overcomes the deficiencies of Ground 1. Pet., 74; Ex. 2012, ¶ 77. Accordingly, Ground 3 also fails.

**D. Ground 4 Fails Because it Does Not Cure the Deficiencies
in Ground 1**

Ground 4 asserts obviousness based on *Cooney* and *Chen* as to dependent Claims 8 and 16. Pet., 74-80. Ground 4 does not assert that including *Farooq* overcomes the deficiencies of Ground 1. Pet., 80; Ex. 2012, ¶ 77. Accordingly, Ground 4 also fails.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding all Challenged Claims not shown to be unpatentable.

Respectfully submitted,

Dated: June 27, 2025

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S PRELIMINARY RESPONSE specified in 37 C.F.R. § 42.24 has 6,627 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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June 27, 2025

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