

UNITED STATES PATENT & TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

- against- Patent No. 9,147,609

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

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DATE: June 17, 2025

TIME: 11:48 a.m.

DEPOSITION of SCOTT E. THOMPSON, Ph.D.,
held via Zoom videoconference, taken by the
Patent Owner, pursuant to a notice, held
remotely via Zoom Videoconference, before
Roberta Caiola, a Notary Public of the State
of New York.

Scott E. Thompson, Ph.D.
June 17, 2025

Page 2 1 A P P E A R A N C E S : 2 3 FABRICANT LLP Attorneys for the Patent Owner 4 411 Theodore Fremd Avenue, #206 South Rye, New York 10580 5 646.797.4343 BY: JOSEPH MERCADANTE, ESQ. 6 jmercadante@fabricantllp.com 7 8 FINNEGAN HEDERSON FARABOW GARRETT & DUNNER LLP 9 Attorneys for the Petitioner SAMSUNG 901 New York Avenue, NW 10 Washington, D.C. 20001 202.408.4324 11 BY: CHEN ZANG, Ph.D., ESQ. chen.zang@finnegan.com 12 JOSHUA L. GOLDBERG, ESQ. joshua.goldberg@finnegan.com 13 ABHAY A. WATWE, Ph.D., ESQ. abhay.watwe@finnegan.com 14 15 16 17 18 19 20 21 22 23 24 25	Page 3 1 S. Thompson 2 THE REPORTER: The parties and 3 counsel participating in this deposition 4 acknowledge that I am not physically 5 present and will be reporting this 6 deposition remotely. 7 They further acknowledge that, in 8 lieu of an oath administered in person, the 9 witness will be sworn in remotely. 10 The parties and their counsel 11 consent to this arrangement and waive any 12 objections to this manner of reporting. 13 Dr. Thompson, would you please raise 14 your right hand. 15 (Witness complies.) 16 THE REPORTER: Do you swear that the 17 testimony that you are about to give will 18 be the truth, the whole truth, and nothing 19 but the truth? 20 THE WITNESS: I do. 21 SCOTT E. THOMPSON, Ph.D., having been first 22 duly sworn by a Notary Public of the State of 23 New York, was examined and testified as 24 follows: 25
Page 4 1 S. Thompson 2 EXAMINATION BY 3 MR. MERCADANTE: 4 Q. Good morning, again, Dr. Thompson. 5 A. Good morning. 6 Q. As previously, my name is Joseph 7 Mercadante, and I will be taking your 8 deposition today. 9 Earlier today we conducted another 10 deposition in which I went over some ground 11 rules. 12 Do you understand those ground rules 13 to also apply to this deposition? 14 A. Yes. 15 Q. Has anything changed since this 16 morning about your mental state or your ability 17 to conduct this deposition? 18 A. No. 19 Q. Do you continue to not have access 20 to any chat or email programs at this time? 21 A. That's correct. 22 Q. I've put four exhibits into the 23 chat, which will be Exhibits 1, 2, 3 and 4 to 24 this deposition. 25 (Exhibit 1, United States Patent	Page 5 1 S. Thompson 2 Number 9,147,609 B2, marked for 3 identification.) 4 (Exhibit 2, Declaration of Dr. Scott 5 E. Thompson, Ph.D. in Support of Petition 6 for Inter Partes Review of United States 7 Patent No. 9,147,609, marked for 8 identification.) 9 (Exhibit 3, Excerpts from the 10 prosecution history of the '609 patent, 11 marked for identification.) 12 (Exhibit 4, U.S. Patent Application 13 Publication 2009/0278237, marked for 14 identification.) 15 Q. Exhibit 1 is the '609 patent, 16 9,147,609. Exhibit 2 is your declaration 17 submitted in this proceeding. Exhibit 3 are 18 excerpts from the prosecution history of the 19 '609 patent. And Exhibit 4 is U.S. Patent 20 Application Publication 2009/0278237 to Cooney, 21 which you refer to, and I will refer to, as 22 Cooney. 23 Do you see those documents? 24 A. I do. 25 Q. And you have those documents locally

Page 6 1 S. Thompson 2 in the room with you; is that correct? 3 A. I do. 4 Q. I'd like to first start with 5 Exhibit 1, the '609 patent. 6 Could you open that for me, please? 7 A. I have it open. 8 Q. Do you see there are two inventors' 9 names, Mr. Jebory and Mr. Howard? 10 A. Yes. 11 Q. Do you know those individuals, 12 either personally or professionally? 13 A. I do not. 14 Q. Have you ever heard of them? 15 A. I have not. 16 Q. And this patent, like the patent we 17 talked about earlier today, originated at 18 Newport Fab LLC, which is a d/b/a of Tower 19 Semiconductor. 20 Do you see that? 21 A. I see that. 22 Q. Since I asked you questions earlier 23 today about Tower, has anything else come to 24 mind that you know about Tower Semiconductor? 25 A. No.	Page 7 1 S. Thompson 2 Q. Could you please open up your 3 declaration, which is Exhibit 2? 4 A. I have it open. 5 Q. In this declaration, like the other 6 one we discussed earlier today, you have a 7 section titled "Technology Background and State 8 of the Prior Art," which begins on page 23. 9 Do you see that? 10 A. I do. 11 Q. And in this section, you rely on 12 some documents to show your general 13 understanding of the state-of-the-art that are 14 not relied on in the body of your report; is 15 that correct? 16 MR. ZANG: Objection. Form. 17 A. I am just showing what a POSITA 18 would know in this time frame. I'm teaching 19 the technology; that's what I'm doing in the 20 background section. 21 Q. Okay. And so, aside from Cooney and 22 the other references specifically identified in 23 the body of your report, you are not relying on 24 any of these background or 25 state-of-the-prior-art references to form your
Page 8 1 S. Thompson 2 invalidity opinions; is that correct? 3 MR. ZANG: Objection. Form. 4 A. I use Cooney, Dean, Chen and Farooq 5 in the grounds. The other ones are just 6 support material. 7 Q. Okay. I have some questions about 8 the level of ordinary skill in the art that you 9 proposed for this patent, which is in paragraph 10 73 of your declaration. 11 Let me know when you're there. 12 A. I'm here. 13 Q. In this paragraph, you state that 14 it's your opinion that "a person of ordinary 15 skill in the art, pertinent to the '609 patent, 16 would have had at least a master's degree in 17 electrical engineering or a similar field and 18 at least two years of experience working on 19 semiconductor systems." 20 Is that correct? 21 A. That's correct. 22 Q. And do you see where you mention a 23 similar field here? 24 A. I do. 25 Q. And your testimony earlier today	Page 9 1 S. Thompson 2 about fields that would be similar enough to 3 electrical engineering would also apply here; 4 is that correct? 5 A. Correct. 6 Q. And in paragraph 74, you state that 7 you were a person of ordinary skill in the art 8 as of October 7, 2011; is that correct? 9 A. Can you repeat that? 10 Q. Sure. 11 In paragraph 74 of your report right 12 here, you state that you were at least a person 13 of ordinary skill in the art as of October 7, 14 2011; is that correct? 15 A. That's correct. 16 Q. And, as of that date, you were 17 likely a person of extraordinary skill in the 18 art; is that correct? 19 MR. ZANG: Objection. Form. 20 A. I had credentials, such as the IEEE 21 fellow, so I'm not -- I'm not scoring myself in 22 any way. 23 Q. But you have credentials -- in 2011, 24 you had credentials beyond that of the person 25 of ordinary skill in the art; is that correct?

Page 10 1 S. Thompson 2 A. Correct. 3 Q. You had additional education and 4 experience, correct? 5 A. Correct. 6 Q. So you have one ground in this 7 declaration, but you've broken it up into an 8 anticipation ground, which you label 1A, and 9 then an obviousness ground, which you label 1B; 10 is that correct? 11 And I'm sorry, I misspoke, that was 12 a bad question, because there is more than one 13 ground in the declaration. 14 In the ground that you've labeled A, 15 or ground 1, you state that "the claims are 16 anticipated by Cooney or alternatively obvious 17 over Cooney." 18 Is that correct? 19 A. For ground 1, right. I have other 20 grounds for some other claims. 21 Q. Okay. With respect to the 22 anticipation ground, 1-A, are you relying at 23 all on inherent anticipation? 24 MR. ZANG: Objection. Form. 25 A. So, again, the same; I'm -- I'm	Page 11 1 S. Thompson 2 saying a POSITA reading Cooney knows all the 3 elements are present. That's all I'm doing for 4 the anticipated ground. 5 Q. And in the obviousness ground, 1B, 6 you were relying on Cooney in combination with 7 the knowledge of a person of skill in the art; 8 is that correct? 9 MR. ZANG: Objection. Form. 10 A. So, ground 1B is there in case the 11 patent owner wants to argue ground 1A had 12 misnomers. 13 I'm saying a single reference of 14 Cooney and an understanding a POSITA would make 15 the invention obvious. 16 Q. Here, as in -- strike that. 17 Could you turn to the claim 18 construction section, please? It starts on 19 page 41. Goes to 42. 20 A. I'm there. 21 Q. In paragraph 70, you state that you 22 were "not asked to expressly construe any terms 23 at this time but was asked for purposes of this 24 declaration to apply the plain and ordinary 25 meaning of the claim terms as they would have
Page 12 1 S. Thompson 2 been understood by a person of ordinary skill 3 in the art at the earliest claimed priority 4 date of the '609 patent." 5 Do you see that? 6 A. I do. 7 Q. And was it counsel who asked you to 8 apply the plain and ordinary meaning of the 9 claim terms? 10 A. It was. 11 Q. On the last page of this 12 declaration, it's dated September 24, 2024. 13 Since you signed this declaration, 14 has any material come to your attention that 15 changes your ultimate opinions regarding 16 validity in this case? 17 A. No. 18 Q. Have you reviewed any additional 19 materials, such as the institution decision? 20 A. I have. 21 Q. Aside from the institution decision, 22 what did you review, if anything? 23 A. Nothing. 24 Q. So the claims of the '609 patent 25 talk about a pinched-off region; is that	Page 13 1 S. Thompson 2 correct? 3 A. In claim -- well, looking at 1C-1, 4 it says: "Silicon vias have a pinched-off 5 region at the bottom." 6 Q. It says "at a bottom portion," 7 correct? 8 A. "At a bottom portion." Correct. 9 Q. What do you understand a pinched-off 10 region to mean? 11 A. Please go to page 3 of 3 of my 12 report, where I show page 4 of the '609 patent. 13 Let me know when you're there. 14 Q. I'm there. 15 A. The spec didn't -- of the '609 did 16 not put requirements on the height of the 17 pinched-off region, but it did give us a figure 18 to guide us of what a pinched-off region is. 19 In Figure 4, they label 438 the 20 pinched-off region, and you can see why they 21 did that. 22 The through silicon via narrows 23 right at the line below the top of the 24 pinched-off region, and also the -- that 25 narrowing of the TSV causes the void to taper.

Page 14 1 S. Thompson 2 So it is with this diagram, I 3 understand a pinched-off region to be where, at 4 least for the -- the bottom pinched-off region 5 near the TSV is narrowing and the void is being 6 sealed off. 7 Q. Does the term or the phrase 8 "pinched-off region" have any particular 9 special meaning in the semiconductor arts or is 10 that just a plain English term? 11 MR. ZANG: Objection. Form. 12 A. Again, it would depend on what 13 semiconductor document you're referring to. In 14 the through silicon via, a POSITA would 15 understand this as being a narrowing of the -- 16 of the TSV. 17 Q. In your opinion, would any narrowing 18 of the TSV qualify as pinched-off region? 19 MR. ZANG: Objection. Form. 20 A. So I don't have to study that case 21 or the invalidity, but I know, based on what 22 they're teaching me in Figure 4, the 23 pinched-off region is being labeled that 24 because the TSV is narrowing and the void is 25 being sealed off.	Page 15 1 S. Thompson 2 Q. So the point at which the TSV 3 becomes narrower than where it starts at the 4 top is the point at which the pinched-off 5 region begins? 6 MR. ZANG: Objection to form. 7 A. If you look at Figure 4, right at 8 the line where the top of the pinched-off 9 region is labeled, two things are happening. 10 One is the -- through a silicon via 11 is getting narrower, and because there's 12 conformal deposition, that starts the process 13 of the void getting sealed off. So as the TSV 14 narrows more and more the void gets sealed off, 15 and then gets completely sealed off. 16 Q. And when you talk about the void, 17 you're talking about the label 432 in this 18 Figure 4 of the patent? 19 A. I'm referring to the hollow center 20 in this figure. At Intel, we would call this 21 a -- a buried void; that's terminology I will 22 sometimes refer this to, because it's a void 23 that's sealed off top and bottom, and, like 24 most companies, if you don't have a -- if you 25 have a void exposed, it causes yield problems.
Page 16 1 S. Thompson 2 Q. What kind of problems? 3 A. Well-known problems such as chemical 4 power slurry getting into the void and 5 contaminating the via. 6 Q. So your understanding of the 7 pinched-off re -- the proper interpretation of 8 a pinched-off region is any area of the via 9 where the via narrows as compared to the top of 10 the via; is that correct? 11 MR. ZANG: Objection. Form. 12 A. So, that's not what I said. It's 13 where the via is narrowing and sealing off the 14 void. 15 Q. Well, you keep bringing the void in, 16 and we're not there yet. 17 Would you agree with me that, if a 18 via does not have a void, that if it's 19 completely full, that it could still have a 20 pinched-off region? 21 MR. ZANG: Objection. Form. 22 A. That's not a case I had to analyze 23 for this -- for this invalidity. 24 Q. So, all right, we'll jump ahead a 25 little bit.	Page 17 1 S. Thompson 2 Let's talk about Cooney. Again, I 3 like a lot of your annotations, so I would like 4 to talk about Figure 10 of Cooney, which you've 5 got annotated on page 45 of your declaration. 6 Let me know when you're there. 7 A. I'm here. 8 Q. So in Cooney, Cooney discloses a TSV 9 with an optional void. 10 Would you agree with me? 11 A. I would agree with you. 12 Q. And your opinion is that the via in 13 Cooney, which we see here in Figure 10, that 14 you've annotated in either pink or purple, has 15 a pinched-off region; is that correct? 16 A. Yes, this via has a pinched-off 17 region. I don't label it in this diagram. 18 There's other diagrams where I do label this. 19 Q. But this via disclosed in Cooney has 20 a pinched-off region, regardless of whether the 21 void is there or not; is that correct? 22 MR. ZANG: Objection. Form. 23 A. Again, that's not a case I've had to 24 analyze. In -- on page 49 in my report, I 25 analyze this case where it is only relevant to

Page 18 1 S. Thompson 2 have a void for the invalidity raised to the 3 claims. 4 Q. Well, whether the TSV in Cooney is 5 completely filled or not, its shape does not 6 change; is that correct? 7 MR. ZANG: Objection. Form. 8 A. Well, the hollow center is changing 9 the shape of the TSV. It's changing the 10 resistance and inductance of the TSV. 11 Q. But whether the -- the TSV is 12 completely filled or not, it doesn't change the 13 external shape of the TSV, does it? 14 MR. ZANG: Same objection. 15 A. The etched apparatus would still 16 have the same shape. 17 Q. Right. And that shape, in your 18 opinion, has a pinched-off region; is that 19 correct? 20 A. So, again, I don't analyze that 21 case. I analyze the case where there is a -- a 22 void where the via is narrowing and it's also 23 sealing off the void. 24 Q. But you do analyze the case, because 25 you said that the shape of the etched apparatus	Page 19 1 S. Thompson 2 does not change whether the void is there or 3 not. 4 So would you agree with me that, 5 regardless of the presence of the void, the TSV 6 in Cooney, in your opinion, has a pinched-off 7 region? 8 MR. ZANG: Objection. Form. 9 A. So, again, I'm only analyzing the 10 case where there is a void, and the pinched-off 11 region is where the via narrows, and it's also 12 sealing off the void. 13 THE REPORTER: I think 14 Mr. Mercadante is gone. He just logged 15 back in. 16 MR. MERCADANTE: I don't know if you 17 are still on the record. The Zoom froze 18 and I dropped off. 19 Q. It looks like there was an answer 20 that I didn't hear because I'm frozen. And the 21 answer was: "So, again, I'm only analyzing the 22 case where there is a void, and the pinched-off 23 region is where the via narrows, and it's also 24 sealing off the void." So I will just -- I'll 25 just go from there.
Page 20 1 S. Thompson 2 So, Dr. Thompson, you can't tell me 3 that -- you can't tell me whether the etched 4 apparatus in Cooney has a pinched-off region if 5 there is no void inside the TSV? 6 MR. ZANG: Objection. Form. 7 A. That's not a case I've analyzed for 8 my report. So, at this point, I would want to 9 study that before giving you an opinion. 10 Q. Would you please turn to paragraph 11 154 -- no, I'm sorry, 152 of your report, on 12 page 83. 13 A. Paragraph 152? 14 Q. 152, yes, that's correct. 15 At the bottom of it, you'll see an 16 annotated version of Figure 6 at Cooney. 17 A. I'm here. 18 Q. In Figure 6, as annotated in 19 paragraph 152 of your declaration, you added in 20 the hollow center inside the TSV; is that 21 correct? 22 I will withdraw the question. That 23 hollow center is in Figure 6. My fault. 24 A. That's what I thought. I was just 25 going to triple-check myself before I answered.	Page 21 1 S. Thompson 2 Q. You also applied the plain and 3 ordinary meaning of the term "tapered," in 4 performing your analysis; is that correct? 5 A. I did. 6 Q. Does the term "tapered" have a 7 particular meaning in the semiconductor arts or 8 did you just apply the plain English 9 understanding of that term? 10 MR. ZANG: Objection to form. 11 A. Taper is a word that would be used 12 in different contexts, but, in the context of 13 the '609, it's referring to how the hollow 14 center closes off. 15 Q. So if something is tapered, it is 16 somehow reducing in thickness, going in one 17 direction; is that generally correct? 18 MR. ZANG: Objection. Form. 19 A. In Figure 4 of the '609 patent, the 20 width of the hollow center is narrowing, so 21 that's why it's tapered. 22 Q. Is the tapering of the TSV in Cooney 23 synonymous with becoming pinched off? 24 MR. ZANG: Objection. Form. 25 A. Can you -- I don't quite understand

Page 22 1 S. Thompson 2 the question. Can you break it up? 3 Q. Sure. 4 Well, how about this: Let's point 5 you to your report. 6 Could you turn to paragraph 166 of 7 your declaration, please, it's on page 90? 8 A. Okay. 9 Q. In paragraph 166, you say: "As 10 illustrated in Figure 5 of Cooney below, the 11 walls of the aperture are tapered towards the 12 bottom of the substrate (e.g., in regions R3 13 and R4) due to the disclosed 'downward pointing 14 torpedo shape' of the aperture." 15 Do you see that? 16 A. I do. 17 Q. And then, in the annotated version 18 of Figure 5, which is on the next page, you 19 state that the -- well, you just colored in 20 Figure 5. 21 But, is it your opinion that the 22 tapering in the bottom portion of the TSV in 23 Cooney, that you're talking about in Figure 24 166, is synonymous with the pinched-off region 25 that you annotated earlier?	Page 23 1 S. Thompson 2 MR. ZANG: Objection. Form. 3 A. The pinched-off region is referring 4 to the narrowing of the TSV, and the tapering 5 you're referring to, the narrowing of the void; 6 so they're different, but they are related in 7 the sense Cooney had the same aperture, a TSV. 8 They're filling it the same way with conformal 9 tungsten. 10 And so, as the TSV narrows, the 11 width of the void is also going to narrow and 12 taper. 13 Q. So in this case, in Cooney, the 14 pinched-off region of the TSV causes the 15 tapering of the void; is that accurate? 16 MR. ZANG: Objection. Form. 17 A. So I think it's helpful to look at 18 the -- again, the Figure 4 of the '609 patent. 19 Focus on the hollow center, where it has a 20 constant uniform width. 21 That width remains constant until 22 the width of the TSV narrows; and once the 23 width of the TSV narrows, then the width of the 24 void narrows. 25 Q. So it's the narrowing of both the
Page 24 1 S. Thompson 2 TSV and the void that causes both the 3 pinched-off region and the tapering; is that 4 correct? 5 MR. ZANG: Objection. Form. 6 A. That's not what I said. It's the 7 narrowing of the TSV that causes the void then 8 to become narrow and taper. 9 Q. And would you agree with me that 10 when you use conformal deposition, the shape of 11 the void is always going to mirror the shape of 12 the aperture? 13 MR. ZANG: Objection. Form. 14 A. Conformal deposition means the 15 deposition follows the shape of the aperture, 16 and then there's a resulting void from that 17 which, in the Figure 4 of the patent, in the 18 middle part of the void where the width of the 19 TSV is not being changed, the void width 20 remains constant. 21 But, as the width of the TSV 22 narrows, then the width of the void is also 23 going to narrow. 24 Q. The challenged claims of the '609 25 patent require a reduction in thermal stress in	Page 25 1 S. Thompson 2 the semiconductor substrate; is that correct? 3 MR. ZANG: Objection. Form. 4 A. It says in claim element 1B-2, vias 5 having a hollow center to reduce thermal stress 6 in the semiconductor substrate. 7 Q. And could you please explain to me 8 what thermal stress is? 9 A. It's stress that results from 10 temperature because materials have different 11 CTE; that stands for coefficient of thermal 12 expansion. 13 Q. So you've got a via -- at least in 14 Cooney, you've got a via full of tungsten, 15 correct? 16 A. In Cooney, the film material is 17 tungsten, and then there's a buried void that's 18 -- that's hollow. 19 Q. Right. And generally speaking, 20 tungsten will expand more when it gets hot than 21 silicon does; is that correct? 22 A. The CTE is larger for tungsten than 23 the CTE for silicon. And so, if we just have 24 both material sitting on a table, that means 25 tungsten would expand more than silicon or bulk

Page 26 1 S. Thompson 2 material sitting on a table, with temperature. 3 Q. And so when -- would the person of 4 ordinary skill in the art understand that, when 5 semiconductors get hot, that thermal stress is 6 caused by the mismatch of CTE in the various 7 materials? 8 MR. ZANG: Objection. Form. 9 A. So we're now talking about, in 10 general, there's many different materials used 11 in the semiconductor, and it's understood that 12 they have different values for coefficient of 13 thermal expansion, and it's understood the 14 semiconductor materials, throughout their life, 15 change; they see different temperatures. 16 It's a combination of changing 17 temperature and having different CTEs causes 18 stress in the integrated circuits. 19 Q. What kinds of stresses does it 20 cause? 21 A. It can cause very large stresses. 22 Q. Thermal stress can lead to failure 23 at certain temperatures; is that correct? 24 MR. ZANG: Objection. Form. 25 A. Again, we're just talking in	Page 27 1 S. Thompson 2 general. I've seen cases in my career where 3 you had large thermal stress that caused 4 delamination of layers, or even cracking of the 5 silicon itself. 6 Q. And in those cases that you've seen 7 in your career that caused delamination or 8 cracking, did that occur because of a via that 9 was creating the thermal stress or was it 10 another element? 11 MR. ZANG: Objection. Form. 12 A. In my career, I've seen stresses 13 from vias, from source drains, from nitride 14 layers. I've seen, you know, many, many 15 different types of elements. 16 Q. And does this thermal stress tend to 17 occur during fabrication or use, or both? 18 MR. ZANG: Objection. Form. 19 A. If we're just talking in general for 20 integrated circuits, it's whenever the 21 temperature changes; so that's both during 22 processing and during use. 23 Q. Could you open up Cooney for me, 24 it's Exhibit 4. 25 A. I have it open.
Page 28 1 S. Thompson 2 Q. Can you turn to paragraph 55 of 3 Cooney? 4 A. I'm here. 5 Q. So paragraph 5 states: "Figure 6 6 shows a liner layer 22 located and formed 7 conformally upon the semiconductor structure of 8 Figure 5 and incompletely filling the extended 9 aperture. Figure 6 also shows a conductor 10 layer 24 with an optional void 25 located 11 therein, located and formed upon the liner 12 layer 22 and completely filling the extended 13 aperture." 14 Did I read that correctly? 15 A. You did. 16 Q. So if the conductor layer 24 17 completely fills the extended aperture, would 18 you agree with me that the optional void in 19 Cooney would not exist? 20 MR. ZANG: Objection to form. 21 A. So what this means is, there can be 22 a case where there's no void, and the aperture 23 is completely filled, or there's a case where 24 there is a void, and the aperture is completely 25 filled, except where the void is.	Page 29 1 S. Thompson 2 Q. And when the -- when the aperture is 3 filled using conformal deposition, and the 4 optional void does exist, what is inside the 5 void; is it a vacuum? 6 MR. ZANG: Objection. Form. 7 A. It could be. It's generally just 8 air. 9 Q. And regardless of whether the void 10 is air or a vacuum, your opinion is that the 11 void would reduce thermal stress in Cooney; is 12 that correct? 13 MR. ZANG: Objection. Form. 14 A. It's well-known that the coefficient 15 of thermal expansion of a void that's buried is 16 much, much, much, much lower than tungsten or 17 silicon, and so, based on the references that 18 I -- I include as support, it was obvious to a 19 POSITA that the presence of a void there 20 reduces stress when it's a -- when it's a 21 buried void, as defined in Cooney or the '609. 22 Q. Does the size of the void matter at 23 all to your analysis? Would a void of any size 24 reduce thermal stress in the TSV in Cooney? 25 MR. ZANG: Objection. Form.

Page 30 1 S. Thompson 2 A. I only analyzed the case of Cooney, 3 not every possible sized void. 4 Cooney's void is a typically shaped 5 void, as you would expect from conformal 6 deposition, where you have a bowed TSV, and 7 Cooney's void would reduce stress. 8 Q. And you say Cooney's void is 9 typically shaped. I assume you also mean it's 10 of a typical size, based on your review of the 11 figures? 12 A. Yeah, I think Cooney's void is a 13 typical void, just like the '609 void is a 14 typical void. 15 Q. Does Cooney state the purpose of the 16 optional void 25 in his apparatus? 17 MR. ZANG: Objection to form. 18 A. By allowing for the optional void, 19 these are well-known -- exceptionally 20 well-known features in the semiconductor 21 processing for tungsten vias. It has different 22 benefits. 23 A POSITA would know that it would 24 reduce stress and other properties, too. 25 Q. But the Cooney reference, Exhibit 4,	Page 31 1 S. Thompson 2 does not explicitly discuss thermal stress; is 3 that correct? 4 MR. ZANG: Same objection. 5 A. Cooney doesn't use the word 6 "stress," but things that are obvious don't 7 need to be said. 8 A void that's buried obviously 9 reduces stress as the tungsten expand and 10 squashes -- squashes the void and expands 11 inward into the void. 12 Q. Cooney is an IBM patent; is that 13 correct? 14 A. It is. 15 Q. Do you know any of the individuals 16 listed as inventors of the Cooney patent? 17 A. I don't know them, but I've seen 18 some of their work at conferences. 19 Q. Did you have any contact with these 20 individuals during your career, either at Intel 21 or otherwise? 22 A. Not that I know of, but I have 23 visited IBM Electronics and I have given talks 24 there. 25 I don't know if they were in the
Page 32 1 S. Thompson 2 audience. I don't remember any contact with 3 these individuals. 4 Q. The Cooney patent also discloses a 5 liner layer, which they label as 22; is that 6 correct? 7 A. Yes, it includes a liner layer 22. 8 Q. Do you know what a liner layer is 9 used for in a TSV, like the one disclosed in 10 Cooney? 11 A. I do. 12 Q. What? 13 A. So Cooney says that liner layer can 14 be conductor or a dielectric layer. So when 15 it's a dielectric layer, it's tended to be used 16 for some insulation. 17 When it's a conductor, it's 18 generally used for adhesion, because tungsten 19 doesn't tend to adhere to silicon very well. 20 So at Intel, we used tungsten-filled 21 devices. We would use a liner layer of 22 titanium or titanium nitride to help it adhere 23 to silicon. 24 Q. And you said when you use a 25 dielectric as a liner, it's generally used for	Page 33 1 S. Thompson 2 insulation. 3 You mean electrical insulation; is 4 that correct? 5 A. Yes, to electrically insulate the 6 tungsten from the bulk wafer. 7 MR. MERCADANTE: I don't believe I 8 have any more questions. I would just like 9 to take a five-minute break, because my 10 notes have turned into a disaster. 11 MR. ZANG: Sounds good. 12 (Whereupon, a recess was taken.) 13 Q. Dr. Thompson, I actually do have a 14 couple of more questions about Cooney. 15 So Cooney discloses a TSV that it 16 refers to as a torpedo shape. 17 Would you agree with that? 18 A. A downward-pointing torpedo shape, 19 correct. 20 Q. How does one go about etching a 21 torpedo shape in silicon, like the one shown in 22 Cooney? 23 MR. ZANG: Objection. Form. 24 A. You would typically use reactive ion 25 etches for that.

Page 34 1 S. Thompson 2 Q. And that would help you make the 3 walls of the torpedo shape wider at one point 4 than the opening at the top of the TSV? 5 MR. ZANG: Objection to form. 6 A. That would be one way to do it with 7 the reactive ion etch and how you passivate the 8 walls during the etch. 9 Q. Are there any other ways that you 10 would use to create the torpedo shape shown in 11 Cooney? 12 A. There could be. 13 Q. Would the person of ordinary skill 14 in the art have been aware of those at the time 15 of the invention of the '609 patent? 16 A. Yeah, at the time of the '609, a 17 POSITA would understand that there's different 18 ways to etch that. 19 Q. Some of these references, including 20 Cooney, use the term semiconductor on 21 insulator. 22 In your view, is that synonymous 23 with silicon on insulator? 24 MR. ZANG: Objection. Form. 25 A. It would depend on the -- on the	Page 35 1 S. Thompson 2 context. Semiconductor is broader. Silicon is 3 one type of semiconductor. But you could do 4 germanium on silicon, and that would be a 5 semiconductor on silicon -- a semiconductor on 6 insulator. 7 Q. But that would not be a silicon 8 insulator, because it's not silicon? 9 A. Right. 10 Q. I'm not sure if I asked you this at 11 the beginning of this deposition, but, in the 12 course of your preparation for this deposition, 13 did you encounter any errors or typos in your 14 report -- I'm sorry, in your declaration in 15 this case that need to be corrected or 16 addressed? 17 A. Not that I -- not that I saw. 18 MR. MERCADANTE: Subject to any 19 additional questions by your attorney, I 20 have nothing further. 21 MR. ZANG: Counsel, can we ask for 22 five minutes? 23 MR. MERCADANTE: Sure. 24 MR. ZANG: Thank you. 25 (Whereupon, a recess was taken.)
Page 36 1 S. Thompson 2 MR. ZANG: Counsel, we have no other 3 questions. 4 MR. MERCADANTE: Just one thing I 5 thought of during the break, which was that 6 I introduced four exhibits into this 7 deposition, but I only talked about three 8 of them; I didn't talk about the 9 prosecution history. 10 Are you guys fine leaving that as an 11 exhibit to the deposition? 12 MR. GOLDBERG: That's fine. 13 And go off the record. 14 MR. MERCADANTE: I'm done, if you 15 guys are done? 16 MR. ZANG: Yes. 17 18 (Time Noted: 12:50 p.m..) 19 20 21 22 23 24 25	Page 37 1 DECLARATION 2 3 I HEREBY CERTIFY that having been 4 first duly sworn to testify to the truth, I 5 gave the above testimony. 6 7 I FURTHER CERTIFY that the foregoing 8 transcript is a true and correct transcript 9 of the testimony given by me at the time 10 and place specified hereinbefore. 11 12 13 _____ 14 SCOTT E. THOMPSON, Ph.D. 15 16 17 Subscribed and sworn to before me 18 this _____ day of _____ 20__. 19 20 21 _____ 22 NOTARY PUBLIC 23 24 25

Scott E. Thompson, Ph.D.
June 17, 2025

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1 CERTIFICATE		1 INDEX	
2		2 WITNESS: SCOTT E. THOMPSON, Ph.D. PAGE	
3 STATE OF NEW YORK)		3 MR. MERCADANTE 4	
4 : ss		4	
5 COUNTY OF BRONX)		5 E X H I B I T S	
6		6 NUMBER DESCRIPTION PAGE	
7 I, ROBERTA CAIOLA, a Certified		7 Exhibit 1 United States Patent Number 4	
8 Shorthand Reporter, do hereby certify:		8 9,147,609 B2	
9 That SCOTT E. THOMPSON, Ph.D., the		9 Exhibit 2 Declaration of Dr. Scott E. 5	
10 witness whose deposition is hereinbefore set		10 Thompson, Ph.D. in Support of	
11 forth, was duly sworn by me and that such		11 Petition for Inter Partes Review	
12 deposition is a true record of the testimony		12 of united States Patent No.	
13 given by the witness.		13 9,147,609	
14 I further certify that I am not		14 Exhibit 3 Excerpts from the prosecution 5	
15 related to any of the parties to this action by		15 history of the '609 patent	
16 blood or marriage, and that I am in no way		16 Exhibit 4 U.S. Patent Application 5	
17 interested in the outcome of this matter.		17 Publication 2009/0278237	
18 IN WITNESS WHEREOF, I have hereunto		18	
19 set my hand on June 18, 2025.		19 (Exhibits forwarded to U.S. Legal for production.)	
20		20	
21 <u>Roberta Caiola</u>		21	
22 ROBERTA CAIOLA		22	
23		23	
24		24	
25		25	

Page 40	
1 ERRATA SHEET	
2 CASE NAME: SAMSUNG vs. HARBOR	
3 DATE OF DEPOSITION: June 17, 2025	
4 WITNESS: SCOTT E. THOMPSON, Ph.D.	
5 PAGE	LINE FROM TO
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20	____ ____ ____ ____
21 Subscribed and sworn to before me	
22 this ____ day of _____, 20____.	
23	
24	
25 Notary Public	Commission Expires

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