

Thermal Stresses around Void in Through Silicon Via in 3D SiP

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Abstract— Thermal stresses around void in TSV (Through Silicon Via) structure in 3D SiP were discussed under the conditions of device operation and reflow process by using FEM (Finite Element Method). In case of the condition of device operation, equivalent stress around void inside Cu TSV was estimated at around 100 MPa. It showed the low possibility for low cycle fatigue of Cu TSV under device operation because that the stress was lower than yield stress of copper, 210MPa. Maximum principal stress of Si was estimated around 100 MPa. It was lower than bending stress of Si. In case of the condition of reflow process, the equivalent stress of TSV with void was higher than yield stress of Cu. However temperature elevation due to reflow process was once or twice during the process. It showed the low possibility for fracture by low cycle fatigue under reflow process. In case without void, maximum principal stress of Si was estimated around 400 MPa. It was almost similar to the bending strength of Si. Stress concentrations were occurred at parts of corner and interface of materials. It has possibility that singular stress field was formed at the parts, and we should discuss fracture induced by singular stress field.

Keywords—Thermal Stresses, Void, TSV(Through Silicon Via), 3D SiP, FEM(Finite Element Method)

I. INTRODUCTION

Recently, the high density 3D packaging technology has been developed to reduce the size and to improve the performance of semiconductor devices [1-8]. Through silicon via (TSV) technique has enabled faster electrical-signal communication between semiconductor chips. The delay time of the signals, which depends on circuit lengths, is become short in 3D packaging structures as compared to the existing 2D packaging structures. Due to above advantages, 3D SiP (Three Dimensional System in Package) with TSV technique has been widely investigated for cooling systems, manufacturing systems and device designs.

The cross-sectional photograph of a 3D stacked structure is shown in Fig. 1. The TSVs are arranged in full area array configuration in this system. The structure was developed by ASET (Association of Super-Advanced Electronics Technology) [9]. In complex device structures which were shown in Fig. 1, the thermal stresses generated in the systems are mainly caused by the mismatch of coefficients of thermal expansion (CTE) and temperature variations of the materials constituting the systems. Several studies on 3D device

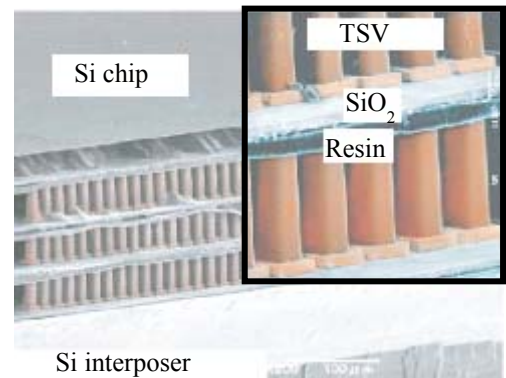


Fig. 1. Cross section of stacked structure and its enlarged figure around TSV (courtesy of ASET)

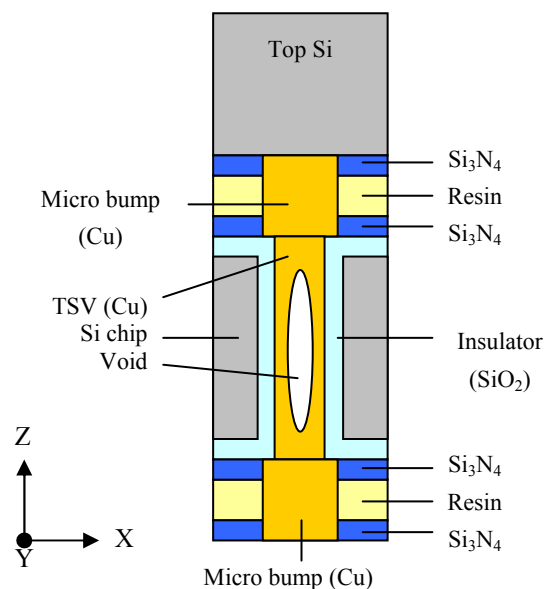


Fig. 2. Schematic image of simulation model of the TSV structure with void in TSV

fabrication reported that some voids are formed in solder bump, under fill and TSVs. These voids are the potential factors for initiations and propagations of cracks and lowering the fatigue life time of integrated materials. Experimental and computational studies on effects of void have been previously performed to ensure the reliability of electronics devices [10-14].

In this study, the effects of the presence of voids inside the TSVs in a 3D SiP structure on the thermal stresses in the TSV structure under device operating condition are analyzed using the large scale simulator, ADVENTUREcluster [15]. The mechanical stresses in the Cu TSVs and in the Si chips are obtained from the simulations.

II. SIMULATION METHOD

A. Simulation model and dimension

The schemes of simulation model (two Si chips and one column) with the TSV structure with a void in the TSV structure was shown in Fig. 2. Periodic boundary conditions were assumed for both models. The model is two Si chips structure and it consists of a TSV (Cu), a micro bump (Cu), a semiconductor chip (Si), an insulator layer (SiO_2), a nitride layer (Si_3N_4) and an inter chip fill resin. TSV structure was not modeled in top Si chip and top Si chip and Si chip with TSV structure were connected by micro bump. Micro bump was surrounded by inter chip fill resin and nitride layer. The void was modeled as a spheroid and it was arranged at the center part of the TSV. Material properties used in this study were shown in Table 1. It is assumed that Cu is elastic-plastic material and Si is anisotropic material.

The dimensions of the simulation model were shown in Fig. 3. The width of the model along the X and Y axes were 50 micro meters. It means that the pitch of the TSVs was 50 micro meters and they are modeled as the square arrangement. The total height was 159 micro meters along the Z direction. The height of top Si chip was 70 micro meters along the Z direction. The diameter of the TSV was 24 micro meters and its height was 75 micro meters. The thickness of the insulator was 1 micro meter and it was arranged between the TSV and the Si chip and between the nitride layer and the Si chip. The thickness of the nitride layer was 1 micro meter. The diameter of the micro bump was 30 micro meters and its height was 7 micro meters. Micro bump was surrounded by inter chip fill resin. Nitride layers are arranged top and bottom surfaces of inter chip fill resin. For the model with a void inside the TSV structure, the length of the major axis and minor axis of the spheroid void were 60 and 12 micro meters, respectively.

B. FEM model

The appearance of FEM model was shown in Fig. 4. The model was built by importing the CAD data to the FEM simulator, ADVENTUREcluster. In this study, all of materials were modeled by Solid Works and mesh was generated by mesh generator of Hyper Mesh.

In building of FEM model, the mesh for thin layer materials with 1 micro meter thickness (insulator and nitride layers) was generated by two layers along the thickness

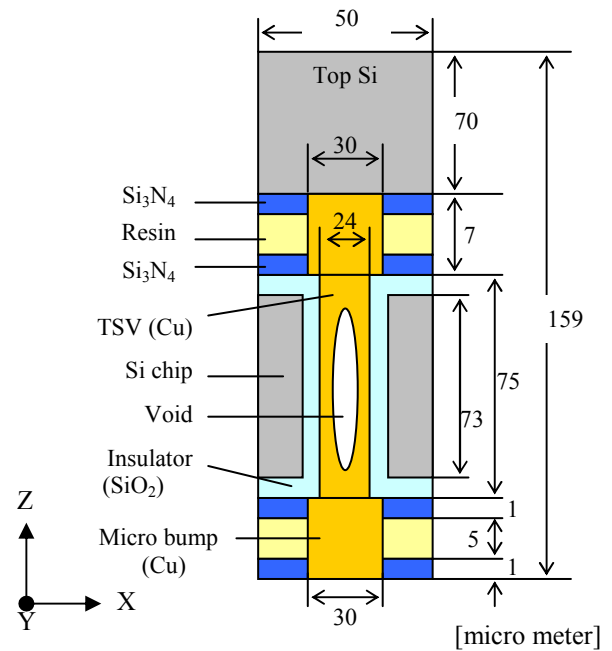


Fig. 3. Dimensions of simulation model with void

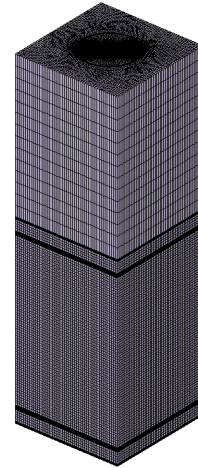


Fig. 4. Appearance of FEM model

Table 1 Material properties

	Young's modulus E [GPa]	Poisson's ratio ν	Yield stress σ_y [MPa]	Hardening coefficient H [GPa]	CTE α [ppm/K]
Cu	110.0	0.30	210	1.7	16.2
Si	131.0	0.28	-	-	2.6
SiO_2	70.0	0.16	-	-	0.5
ICF	3.2	0.30	-	-	71.0
Si_3N_4	302.0	0.28	-	-	2.4

direction to show more accurate stresses. The distance between elementary nodes was 0.5 micro meters. Quadratic hexahedral elements were adopted in this study. In the case of the TSV

structure without void, the number of elements and the degree of freedom (DOF) for the model were 741,730 and 9,596,448, respectively. In the case of the TSV structure with a void, number of elements and degree of freedom (DOF) of the model were 704,290 and 9,246,189, respectively.

C. Thermal stress simulation

In this study, an inelastic thermal stress simulation was carried out to discuss the effect of the presence of void inside the TSVs on the thermal stresses in the Cu TSV and the Si chip under the device operating condition and the reflow process. It was assumed that the temperature of the model was uniformly changed under both conditions. The stress free temperature was assumed to be the room temperature of 25 deg. C., which corresponds to the power OFF state of the devices. In case of device operation, temperature was elevated up to 85 deg. C. In case of reflow process, temperature was elevated up to 260 deg. C. in the simulations.

There are a lot of TSVs in semiconductor chip and they are built in square arrangement in inner plane along X and Y axes direction. Lateral faces, X and Y planes, of the model are constrained by keeping flat and by not rotating along the Z axis direction due to periodic boundary of the model along the X and Y axes direction.

III. RESULTS

The results of the inelastic thermal stress simulation, the equivalent stress distributions in the cross-sections of the models without and with a void inside the TSVs were shown in Fig. 5. In the case of the TSV structure without voids, the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa. The magnitude of the equivalent stress was lower than the yield stress of bulk copper which is 230 MPa. It was insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation. In case of the TSV structure with a void, the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa. It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper. It was also insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation.

In case of reflow process, the equivalent stress distribution was shown in Fig. 6. The equivalent stress with void was estimated around 200 MPa, it showed that TSV was yielded at the condition. However temperature elevation in reflow process was once or twice during the process. It showed the low possibility for fracture by low cycle fatigue under reflow process.

Maximum principal stress distributions at device operation in the cross-section of one chip model without voids and with a void were shown in Fig. 7. The TSV and the SiO₂ insulator layers were removed in the figure and only the cylindrical inner surfaces of Si were shown. In the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa.

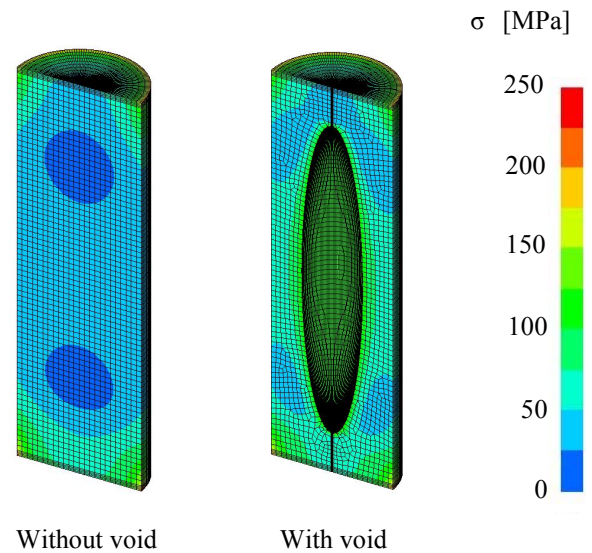


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

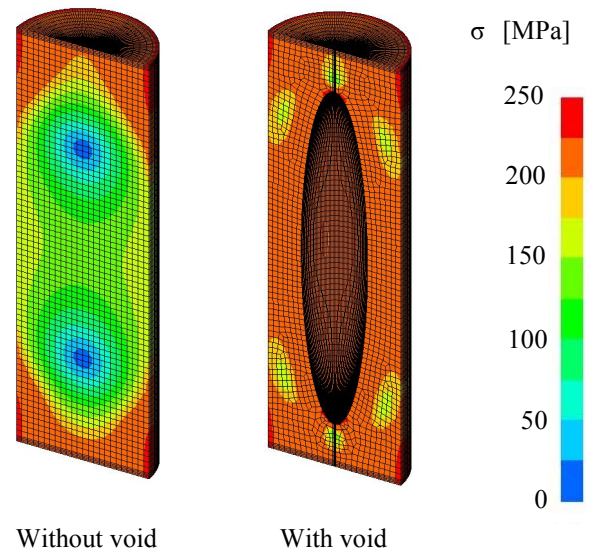


Fig. 6. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of reflow process

Maximum principal stress distributions at reflow process in the cross-section of one chip model without voids and with a void were shown in Fig. 8. The stress without void was estimated around 400 MPa in center part of Si. It was almost similar level of bending strength of Si. The level should not be negligible for crack generation of Si ships.

IV. CONCLUSIONS

In this study, mechanical stress analyses for a TSV structure including the TSVs and Si chips in 3D SiP was discussed with a large scale simulator based on FEM to ensure the reliability of electronics devices for the cases of the TSV structures without voids and with a void inside the TSVs. In the results of inelastic thermal stress simulation, it was shown that the low possibility for fracture of TSV by low cycle fatigue under both conditions. The maximum principal stress of Si without voids in TSV was estimated to be about 400 MPa on the inner surfaces of Si chip under reflow process. It was almost similar level to bending strength of Si. It suggested that the stress level should not be negligible for damages in Si chips.

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REFERENCES

- [1] J. Lau and H. Kong, "TSV and Other Enabling Technologies for 4D IC Integration and WLP – Part1", IneterPACK'09, 2009
- [2] M. Koyanagi, *et al.*, "Future System-on-Silicon LSI chips", IEEE MICRO, Vol. 18, p.17
- [3] J. Lau and H. Kong, 2009, "TSV and Other Enabling Technologies for 4D IC Integration and WLP – Part2", IneterPACK'09.
- [4] S.J. Koester, "3D Integration – Technology, Applications, and New opportunities", IMPACT 2009.
- [5] S.G. Singh and C.S. Tan, "Thermal mitigation using thermal through silicon via (TTSV) in 3-D ICs", IMPACT 2009, 182-185.
- [6] S.P. Shen and *et al.*, "A Novel Cu Plating Formula for Filling Through Silicon Vias", IMPACT 2009, 186-189.
- [7] Journal of Japan Institute of Electronics Packaging, Vol.8, No.7, p. 434
- [8] T. Kinoshita, T. Kawakami, *et al.*, "Thermal Stresses of Through Silicon Vias and Si Chips in Three Dimensional System in Package", Journal of Electronic Packaging, 134, p. 020903(1-4)
- [9] Association of Super-Advanced Electronics Technologies (http://www.aset.or.jp/kenkyu/kenkyu_seika_comp_7.html).
- [10] L. J. Ladani and A. Dasgupta, 2007, "Effect of Voids on Thermomechanical Durability of Pb-Free BGA Solder Joints: Modeling and Simulation", Journal of Electronic Packaging, 129, pp. 273-277
- [11] R. L. Panton *et al.*, 2003, "Simulation of Void Growth in Molten Solder Bumps", Journal of Electronic Packaging, 125, pp. 329-334
- [12] D. Wang and R. L. Panton, 2006, "Experimental Study of Void Formation in Eutectic and Lead-Free Solder Bumps of Flip-Chip Assemblies", Journal of Electronic Packaging, 128, pp. 202-207
- [13] S. Lee, M. J. Yim and D. Baldwin, 2009, "Void Formation Mechanism of Flip Chip Package Using No-Flow Underfill", Journal of Electronic Packaging, 131, pp. 031014 (1-5)
- [14] L. J. Ladani and A. Dasgupta, 2008, "Damage Initiation and Propagation in Voids Joints: Modeling and Simulation", Journal of Electronic Packaging, 130, pp. 011008 (1-11)
- [15] Allied Engineering Corporation (<http://www.alde.co.jp/>)

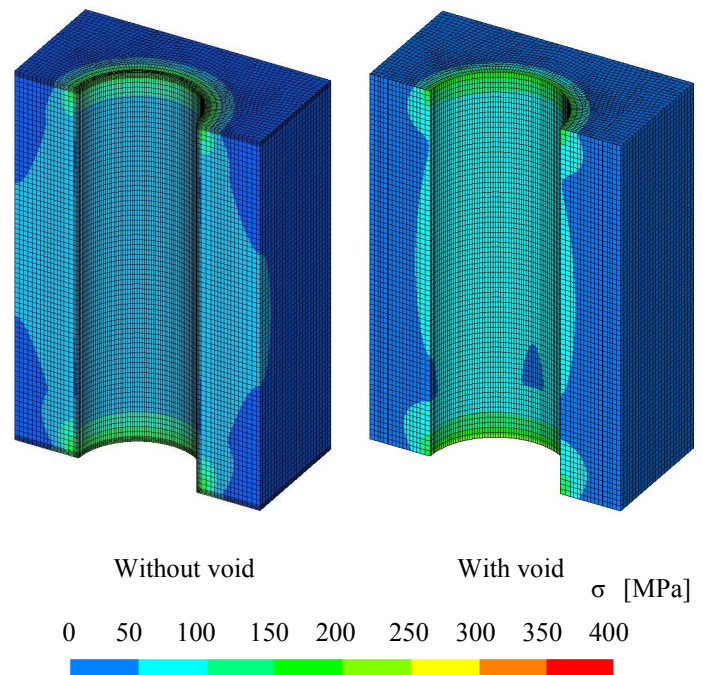


Fig. 7. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of device operation

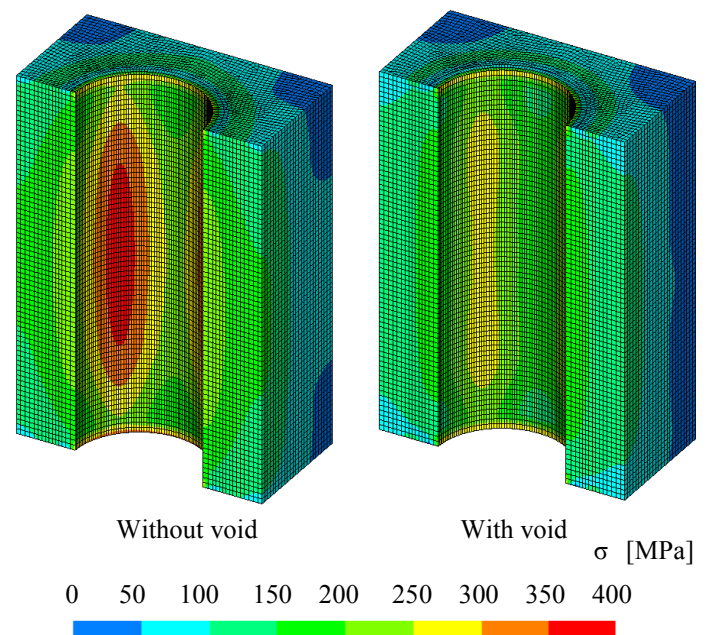


Fig. 8. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of reflow process