

TSV Cu Filling Failure Modes and Mechanisms Causing the Failures

Jae Woong Choi, Ong Lee Guan, Mao Yingjun, Hilmi B. Mohamad Yusoff, Xie Jieli, Chow Choi Lan, Woon Leng Loh, Boon Long Lau, Linda Liew Hwee Hong, Lau Guan Kian, Ramana Murthy, and Eugene Tan Swee Kiat

Abstract—In this paper, we report through-silicon via (TSV) Cu filling failure modes and categorize them into three major regions based on their causes. First, Si etch-related region for the TSV defining. Si etch defects, such as bottom corner notch, Si grass at the bottom, surface roughness, and sponge-like defect, cause Cu seed layer loss at the defect areas. It causes electrical disconnection resulting in the TSV Cu filling failure. Second, Cu seed layer-related region. Defects include poor Cu seed layer step coverage and oxidation of the Cu seed layer from the Cu seed layer deposition until the TSV Cu electroplating from the Cu seed layer deposition. They result in aggrandizing terminal effect, which makes Cu ion reduction at the TSV bottom difficult. Third, Cu electroplating-related region. The most important factor in this region is chemical concentration control because the TSV Cu filling by bottom up filling mainly depends on the cooperation of three additives of suppressor, accelerator, and leveler. Another important factor in the region is current density ramp up rate. It is critical to ramp up the current density with an appropriate rate to prevent pinchoff plating causing voids inside the TSVs. These regions are closely connected with each other and the relationship needs to be understood to overcome the TSV Cu filling failure.

Index Terms—Cu electroplating, Cu filling defects, Cu seed layer, failure modes, Si etch, through-silicon via (TSV).

I. INTRODUCTION

THROUGH-silicon via (TSV) is generally considered as a breakthrough to achieve 3-D IC packaging to satisfy market requirements with high performance, low cost, and form factor [1]. As well-known [2], Si dry etch, dielectric layer deposition, Cu seed layer deposition, Cu electroplating, and Cu chemical mechanical polishing are widely used to produce the TSV contained wafers. Although the TSV has great potential to be used for 3-D IC packaging, it still has a lot of problems to overcome for mass production with low cost. Largely, there are five categories of the obstacles on the way to the mass production [3]. The first category is

about the TSV formation, including Si etch, isolation, and Cu filling. The second category is the wafer thinning, such as grinding and TSV revealing process. The other categories are bonding/debonding, assembly, and testing. In the first category of the TSV wafer fabrication, commonly we can observe several types of the Cu filling failures after Cu electroplating with nondestructive X-ray microscopy [4]–[6]. If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed. Fig. 1 shows the conventional model of bottom up filling for void-free TSV Cu filling when all processes are controlled well. From process integration point of view, a lot of researches have shown the Cu filling failures but a few have addressed the root cause of such failures. It is also considered that the overall understanding about the mechanisms causing the failures is needed to realize low-cost 3-D IC based on the TSV.

In this paper, we report the Cu filling failure modes observed as voids inside the TSVs, which are caused by each unit process. In addition, we discuss the mechanisms how the defects cause the Cu filling failures

II. EXPERIMENTAL PROCEDURE

In this paper, all the TSVs were dry etched at inductively coupled plasma type Si etcher with a Bosch process using SF₆ for Si etch and C₄F₈ for sidewall passivation, respectively. We used 300-mm wafers for interposer application with 10 μm $\times$ 100 μm TSV and 200-mm wafers for micro-electromechanical systems application with 30 μm $\times$ 150 μm TSV and 60 μm $\times$ 250 μm TSV, respectively. Si etch was done at AMAT Centura Siliva Si etch for 300-mm wafers and SPTS OMEGA for 200-mm wafers. Dielectric liner deposition after Si etch was done at Producer InVia chemical vapor deposition (CVD) for 300-mm wafers and thermal oxide deposition for 200-mm wafers, respectively. The Cu seed layer for Cu electroplating was done at AMAT Endura CuBS RFX physical vapor deposition for 300-mm wafers and Tango Systems for 200-mm wafers, respectively. The Cu seed layers were examined by transmission electron microscope (TEM). All the TSV Cu fillings were done at Semitool Raider-S with vacuum prewetting to avoid any air trapped inside the TSVs. We used virgin makeup solution from JCU Corp for the TSV Cu electroplating with the conventional three additives of leveler, accelerator, and suppressor. In this paper, we maintained the concentration of the three additives to avoid the

Manuscript received August 20, 2013; revised December 17, 2013; accepted December 30, 2013. Date of publication January 24, 2014; date of current version March 28, 2014. Recommended for publication by Associate Editor B. Dang upon evaluation of reviewers' comments.

The authors are with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore 117685 (e-mail: choijw@ime.a-star.edu.sg; onglg@ime.a-star.edu.sg; maoy@ime.a-star.edu.sg; hilmi@ime.a-star.edu.sg; xieji@ime.a-star.edu.sg; chowcl@ime.a-star.edu.sg; lohwl@ime.a-star.edu.sg; laubl@ime.a-star.edu.sg; liewhhl@ime.a-star.edu.sg; laugk@ime.a-star.edu.sg; ramana@ime.a-star.edu.sg; tanske@ime.a-star.edu.sg).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TCPMT.2014.2298031

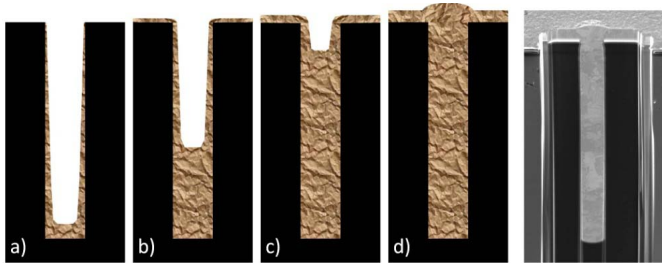


Fig. 1. Cu filling procedure to form a void-free TSV. (a) Initial stage. (b) Intermediate stage. (c) Final stage. (d) Void-free Cu filling and the image of actual TSV after Cu filling.

chemical concentration effect on Cu electroplating with cyclic voltametric stripping (CVS) method (ECI QL-10EX CVS). We used direct current wave forms to fill the TSVs and the current densities for each Cu electroplating were ramped up gradually. After the TSV Cu filling, we inspected the wafers with a nondestructive X-ray method and a cross-sectional inspection to examine the voids was done by focused ion beam.

III. RESULTS AND DISCUSSION

A. Si Etch-Related Region

1) *Sidewall Scallop*: Sidewall scallop is one of the crucial factors to achieve defect-free Cu filling. If the sidewall scallop is too deep laterally, it is impossible to make a good coverage of the Cu seed layer. In addition, the deeper sidewall scallop increases the electrical resistance from the top of the TSVs to the bottom of the TSVs by increasing electron path. It means that it will require lower current density to overcome its high-terminal effect [7], [8] at the beginning stage of the TSV Cu electroplating for the initiation of the bottom up filling. Fig. 2(a) shows one of the TSV Cu filling failure modes due to a Cu loss at the bottom of the TSV. As shown in the image, the TSV does not have any Cu deposit electroplated at the bottom of the TSV at all and a very huge void is observed in the TSV. With the result, we can simulate how the filling failure mode occurred during the Cu electroplating process as shown in Fig. 2(b)–(e). At the beginning of the Cu electroplating process, low-current density, which is low enough to minimize the terminal effect is applied and it helps to have conformal Cu electroplated layer from the top to the bottom of the TSV. Since the initiating process depends on the electrical resistance from the top to bottom of the TSV, the process can be varied according to the performance of sidewall roughness, dielectric liner sidewall smoothening performance, and seed layer step coverage. In this failure mode, Cu electroplating occurred on the sidewall and the Cu deposits grew laterally. Pinchoff plating occurs when the Cu layer on the sidewall starts to grow and close off at the mouth of the TSV. It means that there was no electrical connection between the sidewall and bottom of the TSV although the Cu seed layer was on the bottom of the TSV. As can be observed in Fig. 3, we were able to observe the discontinuity of the Cu seed layer because of the sidewall roughness (bottom corner notch) caused by Si etch. As shown in the TEM image, because the discontinuity is narrow, the electroplated Cu grown from the bottom corner at the side of

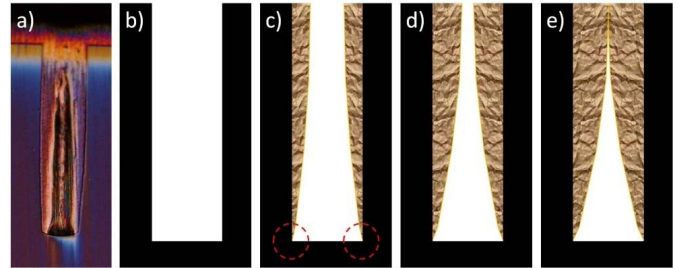


Fig. 2. Cu filling failure mode due to Cu loss at the bottom of the $60\ \mu\text{m} \times 250\ \mu\text{m}$ TSV. (a) Actual void inside TSV. (b)–(d) Method showing the formation of the void inside the TSV.

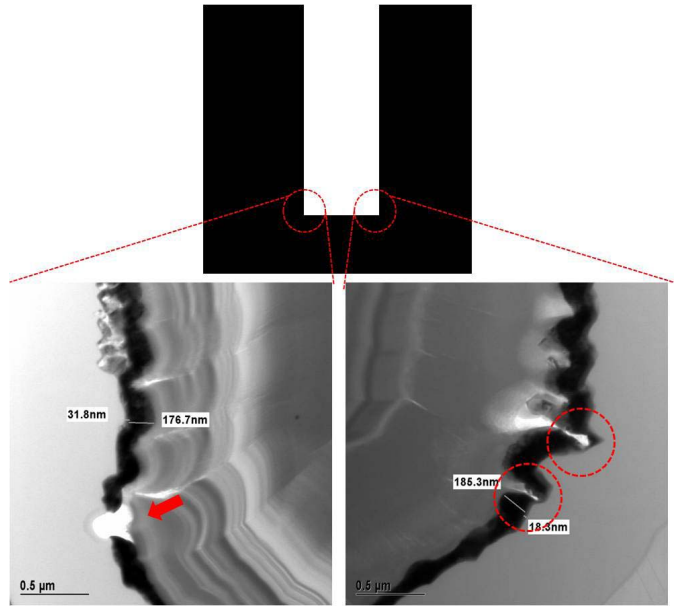


Fig. 3. TEM images at the bottom corners of $60\ \mu\text{m} \times 250\ \mu\text{m}$ TSV.

sidewall may get connected to the bottom Cu seed layer to form electrical connection as the Cu electroplating continues. However, the Cu seed layer at the bottom will be etched away in the Cu electroplating chemical before the Cu grown from the bottom corner makes the electrical connection with the Cu seed layer at the bottom of the TSV.

If the rate of the current density ramping up is slowed down after the initiation stage, it is possible to achieve less volume of the void inside the TSV by retarding the pinchoff plating as shown in Fig. 4(c). However, the bottom up filling may not occur because of the Cu seed layer discontinuity caused by the bottom corner notch and the TSV will be filled with only the Cu grown from the sidewall, as can be observed in Fig. 4.

The sidewall roughness issue caused by Si etch can be minimized using ozone tetraethylorthosilicate (O_3 TEOS) dielectric layer deposition, as shown in Fig. 5. It helps to have a good continuity of the Cu seed layer by smoothening the sidewall roughness. Although the sidewall roughness can be smoothened by the oxide deposition, the scallop peaks can be the sources of fracture due to the stress focusing as reported in [9] and [10]. Therefore, the sidewall roughness should be improved to solve both the Cu seed layer discontinuity and the stress focused fracture for more reliable TSVs.

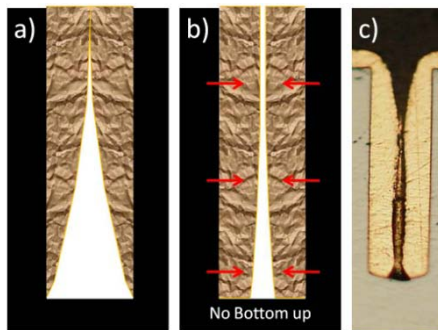


Fig. 4. Less volumetric void inside TSV by lowering down the rate of current density ramp up. (a) High rate of current density ramp up. (b) Low rate of current density ramp up. (c) Actual TSV by low rate of current density at $60\ \mu\text{m} \times 250\ \mu\text{m}$.

2) *Si Grass*: When we use the Bosch process using the repetitive cycles of etch and sidewall passivation, the balance between etch step and sidewall passivation step is very critical to achieve defect-free TSVs. We can observe the Si etch defects such as profile tilting, undercut, bowing, sidewall scallop, and Si grass. To minimize the sidewall scallop, each step is controlled in hundreds of milliseconds. Among Si etch defects, Si grass is considered the most crucial defect causing Cu filling failure, as can be observed in Fig. 6.

It is reported that the Si grass is formed by micromasking due to Si-O [11]. Because oxygen added in the plasma saturates dangling bonds on the Si surface forms a passivating Si-O layer inhibiting Si etch by fluorine radicals. It is recommended to add Si-O scavenger, such as CHF_3 , to avoid Si-O micromasking at the bottom of the TSV. However, Si grass defect is observed even in the case of nonoxygen contained process, as shown in Fig. 6. Leopold *et al.* [12] reported that the cluster acting as micromasking was not Si containing compound, such as SiF_xO_y , SiO_x , or SiC, analyzed by X-ray photoelectron spectroscopy, and it consisted of residues of fluorinated carbon. It means that the micromasking resulting in Si grass defect can occur in the process without oxygen forming Si-O.

If there is Si grass at the bottom of the TSVs, the area will not be filled with Cu during the TSV Cu electroplating. Then, it will leave voids after backside TSV revealing and it may affect on the electrical performance.

3) *Sponge-Like Defect*: As we reported [13], sponge-like defect can be observed mainly at the interface between each cycle of etch, as shown in Fig. 7. It is considered that there are two mechanisms causing the sponge-like defect. One mechanism is thought that a poor polymer deposition for sidewall passivation caused by surface defects formed during the previous etch steps, as shown in Fig. 8. If there are surface defects formed during etch steps before the sidewall passivation steps, the sidewall passivation may fail to deposit a polymer on the surface at the defect areas to protect Si surface from the etchant during the subsequent etch steps and it will make the surface condition worse.

The other mechanism causing the sponge-like defect is thought to be voids inside the sidewall polymer. To verify the voids effects on the sponge-like defect, we deposited

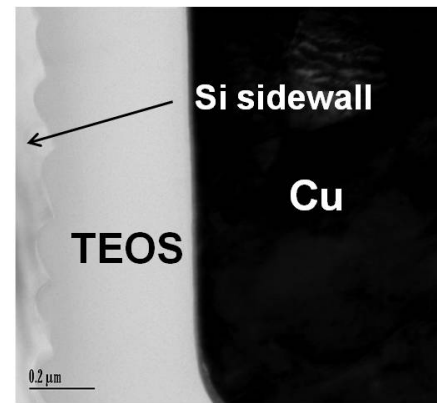


Fig. 5. TEM image of Si sidewall roughness smoothed by O_3 TEOS.

a thick polymer on the sidewall after the TSV formation. We were able to observe voids in the sidewall polymer, as shown in Fig. 9. With the observation, the sponge-like defect is considered to be formed as the suggested mechanism in Fig. 10. If the voids are formed inside the sidewall polymer, the polymer at the void areas will be thinner than the other areas. Thus, the sidewall polymer at the areas will be too thin to protect the Si surface during the subsequent etch steps. The repetitive failure of the sidewall protection will make the sponge-like defect worse. Since Si etch is an isotropic etching by the etchant, we will see isotropically etched surface defects.

As shown in Fig. 11, we can observe the mechanism how the Cu seed layer missing occurs because of the sponge-like defect. As explained, there are some sponge-like defects formed during Si etch process as shown in Fig. 11(a). The sponge-like defects at area A are smaller and shallower than the defect at area B. The Si etch will be followed by dielectric layer deposition using either thermal oxidation or CVD. During the dielectric layer deposition process, the sponge-like defects at the area A can be filled with the dielectric material of Si-O but the sponge-like defect at the area B cannot be fully filled because of the size and the depth of the defect. Therefore, we will have the Cu seed layer missing at the area B, as shown in Fig. 11(b) and (c), shows the microscopic image taken after the Cu seed layer deposition and we can observe the Cu seed layer missing due to the sponge-like defect and the deep sidewall scalloping. This Cu seed layer missing results in the Cu filling failure, as shown in Fig. 12. Fig. 12 shows the TSVs without Cu filling failure and the TSVs with the failure caused by the Cu seed layer missing due to the sponge-like defect formed during the Si etch process.

B. Cu Seed Layer-Related Region

1) *Step Coverage*: A step coverage is widely used to show the capability of the Cu seed layer deposition for the TSVs. The Cu seed layer with higher step coverage means thicker Cu seed layer at the weakest point in the TSVs than the Cu seed layer with lower step coverage when the Cu seed layer thickness at the field area is the same. In other words, the Cu seed layer with higher step coverage can reduce the terminal effect bothering the reduction of Cu ions at the

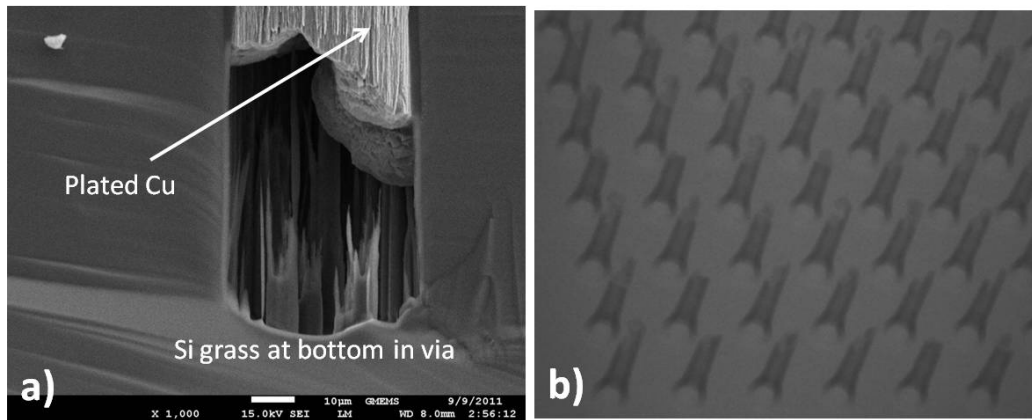


Fig. 6. SEM image of the Cu filling failure mode caused by (a) Si grass and (b) its X-ray image.

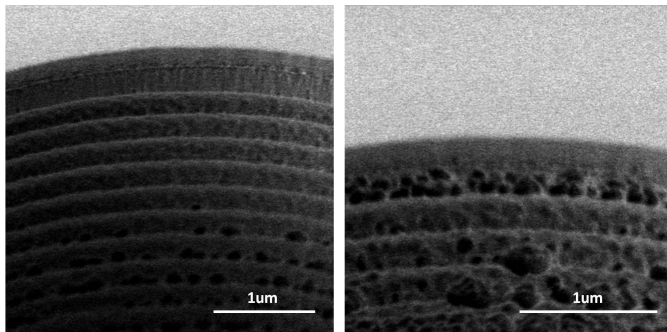


Fig. 7. DR-SEM images of the sponge-like defects formed during Si etch process at $10\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ TSV [13].

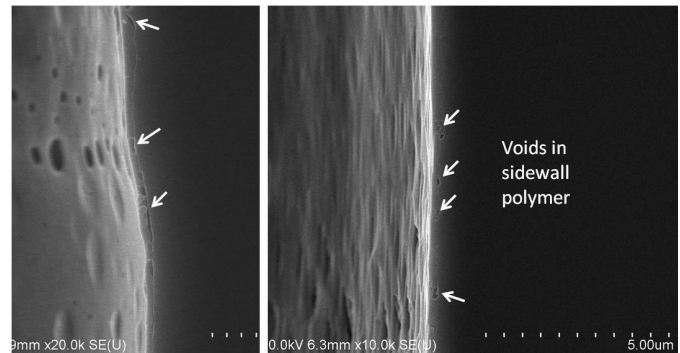


Fig. 9. Voids in sidewall polymer causing the sponge-like defects [13].

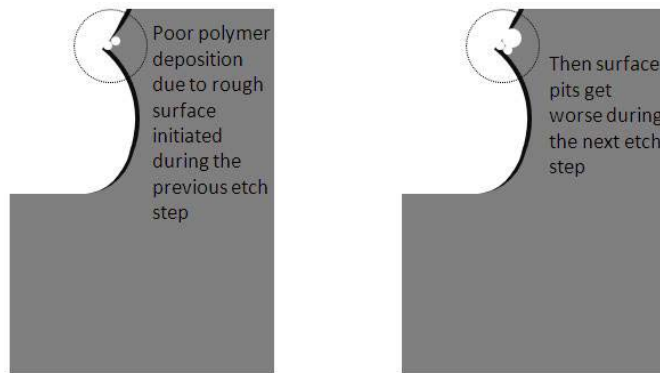


Fig. 8. First mechanism causing the sponge-like defect during Si etch process [13].

weakest point in the TSVs. Therefore, the Cu seed layer with lower step coverage will result in either the failure of bottom up filling or pinchoff plating due to higher terminal effect if the TSV Cu electroplating for two different step coverage layers is the same.

To observe the effect of the Cu seed layer step coverage on the TSV Cu filling behavior, we prepared the TSV wafers with two different step coverage Cu seed layers, as shown in Table I. As shown in Fig. 13, while the void-free filling was achieved at the Cu seed layer with higher step coverage,

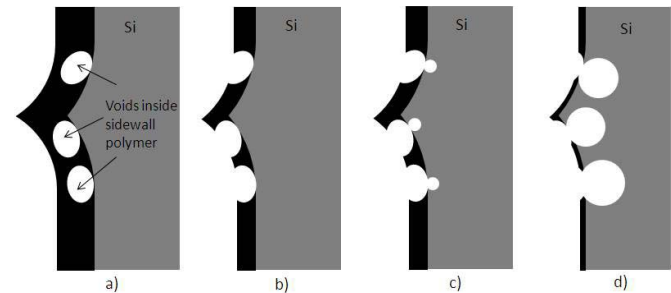


Fig. 10. Second mechanism causing the sponge-like defects during Si etch process [13]. (a) Voids inside sidewall polymer after passivation, (b) initial stage of etch step, (c) mid-stage of etch step, and (d) final stage of etch step.

the voids in the TSVs were observed at the Cu seed layer with lower step coverage.

The voids due to the lower step coverage of the Cu seed layer, it can be solved by lowering the current density for the initiation of the bottom up filling at the TSV Cu filling stage. However, it will increase the overall TSV Cu electroplating process time.

2) *Oxidation of Cu Seed Layer*: The oxidation of Cu seed layer is one of the critical factors to be controlled to achieve void-free TSV Cu filling [14]. Since the oxidation of metal is a surface reaction regardless of its thickness, the oxidation rate of Cu seed layer will be consistent all over the seed layer if the microstructure of the Cu seed layer is uniform.

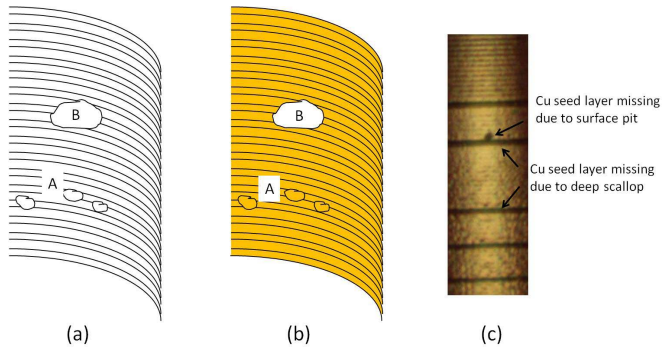


Fig. 11. Mechanism causing the Cu seed layer missing due to sponge-like defects and deep scallops. (a) After Si etch. (b) After Cu seed layer deposition. (c) Microscopic image of the Cu seed layer deposited at $60\ \mu\text{m} \times 250\ \mu\text{m}$.

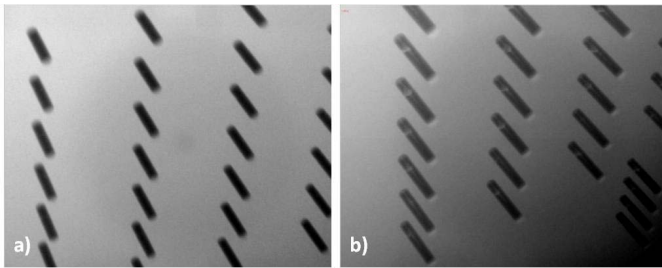


Fig. 12. X-ray images of TSVs after Cu electroplating. (a) TSVs without Cu filling failure. (b) TSVs with Cu filling failure caused by the Cu seed layer loss due to the sponge-like defects at $30\ \mu\text{m} \times 150\ \mu\text{m}$ TSV.

TABLE I
STEP COVERAGE OF TWO DIFFERENT Cu SEED LAYERS

Location	Cond. A	Cond. B
Field	100%	100%
Bottom Corner	3.31%	2.16%
Bottom Center	12.54%	10.64%

It will make the step coverage of Cu seed layer changed, as shown in Fig. 14, because the Cu oxide is etched away in the Cu electroplating chemical. Therefore, it will show the same result with the Cu seed layer step coverage effect on the TSV Cu filling result as explained in Section III-B.1.

To verify the Cu seed layer oxidation effect on the TSV Cu filling, we prepared Cu seed layer deposited wafers at the same time and stored them in a clean room atmosphere. Then, each wafer was Cu electroplated one by one and inspected by X-ray. As shown in Fig. 15, the voids at the top area in the TSVs began to be observed at the wafer of Cu electroplated after 10 days from the Cu seed layer deposition.

It means that the Cu seed layer oxidation aggrandizes the terminal effect by changing the Cu seed layer step coverage. As a result, the current density for the initiation of the bottom up filling was not appropriate at the oxidized Cu seed layer wafers to achieve the void-free filling. The voids due to the oxidation of the Cu seed layer can be overcome by lowering

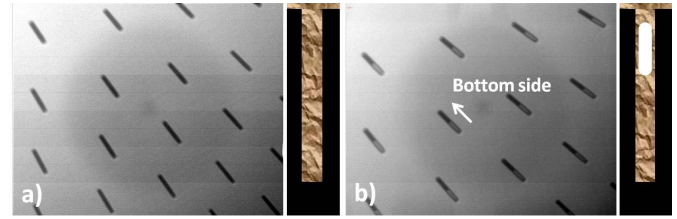


Fig. 13. X-ray comparison of TSVs after Cu electroplating. (a) Higher step coverage of Cond. A, no voids inside TSVs. (b) Lower step coverage of Cond. B, voids inside TSVs due to slow bottom up filling.

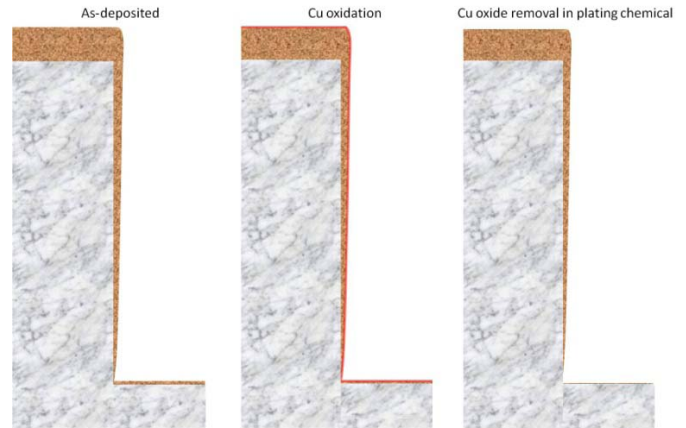


Fig. 14. Model of the Cu seed layer oxidation effect on the Cu seed layer step coverage.

the current density for the initiation of the bottom up filling like the method for the lower step coverage of the Cu seed layer.

C. Cu Electroplating-Related Region

1) *Chemical Composition*: To achieve a bottom up filling without any voids inside the TSVs, generally three different additives of accelerator, suppressor, and leveler are used. Owing to the molecular diffusivity difference among each additive, the relative concentration of each additive is different at the bottom of the TSVs and at the opening of the TSVs. The well combined additives concentration helps to achieve bottom up filling [15], [16] by suppressing the Cu deposition at the opening of the TSVs. To achieve the bottom up filling, the ratio of three different additives should be controlled very carefully. A lot of researches have reported the importance of not only additives concentration but also the inorganic concentration in Cu electroplating chemical, including Cu ions and Cl^- ions [17]–[21]. These researches have focused on achieving an optimum chemical concentration to improve the Cu ion reduction at the bottom of the TSVs and disturbing the reaction at the opening of the TSVs using charge transfer and mass transport. The development direction of the additives is to avoid the pinchoff plating for the bottom up filling with void-free and thin overburden for less wafer level warpage. In this paper, we used a best known method chemical concentration condition rather than diversifying the concentration to eliminate the chemical concentration effect on the TSV Cu filling defects.

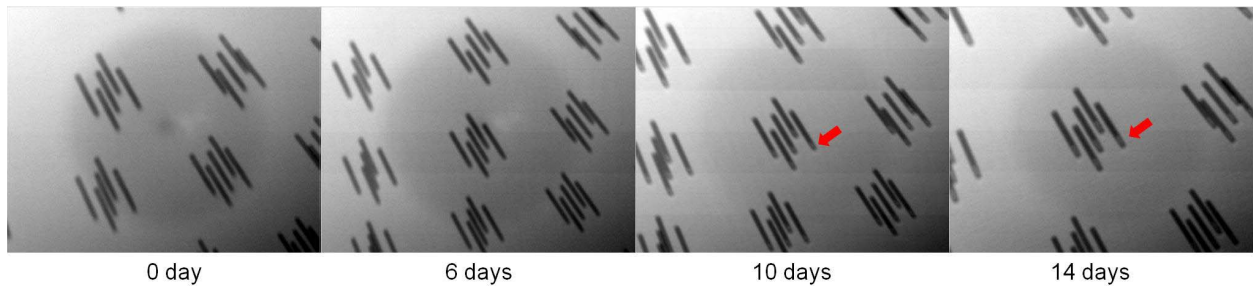


Fig. 15. X-ray inspection results from Cu electroplated wafers according to queue time after Cu seed layer deposition at $10\ \mu\text{m} \times 100\ \mu\text{m}$ TSVs.

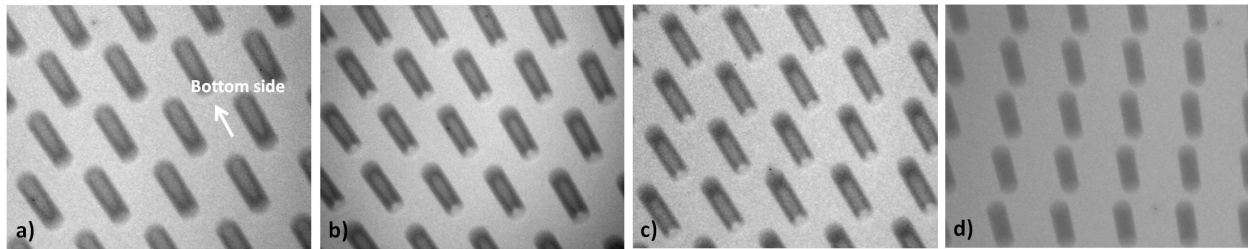


Fig. 16. X-ray images showing the current density ramping up rate on TSV Cu filling failure. (a) Initiation at $1.5\ \text{mA}/\text{cm}^2$. (b) Initiation at $1.0\ \text{mA}/\text{cm}^2$ then switched to $1.5\ \text{mA}/\text{cm}^2$. (c) Longer duration at $1.0\ \text{mA}/\text{cm}^2$ then switched to $1.5\ \text{mA}/\text{cm}^2$. (d) Completely fully filled TSVs.

D. Current Density Ramping Up Rate

We used direct current wave forms but the current density was gradually ramped up from low-current density to high-current density to achieve bottom up without any voids inside the TSVs as fast as possible. Largely, there are three stages for the TSV Cu electroplating: 1) an initial stage, initiating the bottom up at low-current density; 2) an intermittent stage, developing Cu from the bottom while minimizing Cu growth at the opening of TSVs; and 3) a final stage, filling the TSVs completely. The pinchoff plating is the most common Cu filling defect. Although the Cu seed layer step coverage is sufficient and the additives concentration is in the optimum condition, the pinchoff plating defect is inevitable when the current density ramping rate and the current density for the initiation of the bottom up filling are not appropriate.

As shown in Fig. 16(a), the TSV Cu electroplating was started at the current density of $1.5\ \text{mA}/\text{cm}^2$ and the current density was switched to $2\ \text{mA}/\text{cm}^2$. The X-ray image shows that even the bottom up was not initiated but the opening of the TSV was already closed. Therefore, we lowered the current density for the initiation of the bottom up filling from 1.5 to $1\ \text{mA}/\text{cm}^2$. Then, the current density was switched to $1.5\ \text{mA}/\text{cm}^2$. Although the current densities were different for the TSV of Fig. 16(a) and the TSV of Fig. 16(b), the Ampere-minute for two different conditions was the same. As can be observed in Fig. 16(b), the bottom up filling was initiated but the opening of the TSV began to be closed because of the rapid current density ramping up from 1 to $1.5\ \text{mA}/\text{cm}^2$. To retard the closing at the opening of the TSV, the current density was switched to $1.5\ \text{mA}/\text{cm}^2$ after longer duration at $1\ \text{mA}/\text{cm}^2$ (from 10 to $15\ \text{A min}$; 1.5 times longer plating at $1\ \text{mA}/\text{cm}^2$). As shown in Fig. 16(c), slower current density ramping up was able to keep the opening of the TSV open. With the initiation of the bottom up filling, the current density was ramped up to $5\ \text{mA}/\text{cm}^2$ gradually to completely fill the TSVs, as shown in Fig. 16(d).

IV. CONCLUSION

In this paper, we reported the TSV Cu filling failure modes and mechanisms causing the failures based on each unit process in a TSV process integration procedure. We categorized the root causes resulting in the TSV Cu filling failures into three major regions of Si etch related, Cu seed layer related, and Cu electroplating related. There were Si sidewall roughness (bottom corner notch), Si grass, and sponge-like defect in Si etch-related region, and they caused Cu seed layer loss resulting in the Cu filling failure observed as voids. In the Cu seed layer-related region, there were Cu seed layer step coverage variation and Cu seed layer oxidation. The Cu seed layer oxidation caused degradation of the Cu seed layer step coverage. Both of them resulted in aggrandizing the terminal effect, which affected on the efficiency of Cu ion reduction at the bottom of the TSVs. There were Cu electroplating chemical composition, including three additives of accelerator, suppressor and leveler, current density for the initiation of bottom-up filling, and the rate of current density ramp up to fill the TSVs completely without any voids in the TSVs in the Cu electroplating-related region. Although the chemical composition was at the optimum condition, we were able to observe voids in the TSVs if the current density for the initiation and the rate of the current density ramp up were not appropriate. Since these three major regions causing the TSV Cu filling failures are closely connected with each other, it is considered that understanding the mechanisms can help to the reliability and repeatability of the TSV formation without the Cu filling failures.

REFERENCES

- [1] E. Mounier, "3D IC & TSV report (cost, technologies & markets)," Yole Development, Villeurbanne, France, Tech. Rep., 2007.
- [2] J. Van Olmen, C. Huyghebaert, J. Coenen, J. Van Aelst, E. Slecckx, A. Van Ammel, *et al.*, "Integration challenges of copper through silicon via (TSV) metallization for 3D-stacked IC integration," *Microelectron. Eng.*, vol. 88, no. 5, pp. 745–748, 2011.

- [3] J.-M. Yannou, P. Garrou, J. Baron, and C. Zinck, "3D glass & interposer," Yole Development, Villeurbanne, France, Tech. Rep., Sep. 2010.
- [4] K. Sueoka, F. Yamada, A. Horibe, H. Kikuchi, K. Minami, and Y. Orii, "TSV diagnostics by X-ray microscopy," in *Proc. IEEE 13th EPTC*, Dec. 2011, pp. 695–698.
- [5] L. W. Kong, J. R. Lloyd, K. B. Yeap, E. Zschech, A. Rudack, M. Liehr, *et al.*, "Applying X-ray microscopy and finite element modeling to identify the mechanism of stress-assisted void growth in through-silicon vias," *J. Appl. Phys.*, vol. 110, no. 5, 2011.
- [6] L. W. Kong, J. R. Lloyd, A. C. Rudack, and A. C. Diebold, "Thermally induced void growth in through-silicon vias," *J. Micro/Nanolith MEMS MOEMS*, vol. 12, no. 2, p. 023010, 2013.
- [7] S. Armini and P. M. Vereecken, "Impact of 'terminal effect' on Cu plating: Theory and experimental evidence," *ECS Trans.*, vol. 25, no. 27, pp. 185–194, 2010.
- [8] S. Armini, A. Tokei, H. Volders, Z. El-Mekki, A. Radisic, G. Beyer, *et al.*, "Impact of 'terminal effect' on Cu electrochemical deposition: Filling capability for different metallization options," *Microelectron. Eng.*, vol. 88, no. 5, pp. 754–759, 2011.
- [9] N. Ranganathan, D. Y. Lee, L. Youhe, G.-Q. Lo, K. Prasad, and K. L. Pey, "Influence of Bosch etch process on electrical isolation of TSV structures," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 10, pp. 1497–1507, Oct. 2011.
- [10] T. Nakamura, H. Kitada, Y. Mizushima, N. Maeda, K. Fujimoto, and T. Ohba, "Comparative study of side-wall roughness effects on leakage currents in through-silicon via interconnects," in *Proc. IEEE Int. 3D Syst. Integr. Conf.*, Jan./Feb. 2012, pp. 1–4.
- [11] F. Laermer, *Comprehensive Microsystems*. New York, NY, USA: Elsevier, 2008, pp. 217–233.
- [12] S. Leopold, C. Kremin, A. Ulbrich, S. Krischok, and M. Hoffmann, "Formation of silicon grass: Nanomasking by carbon clusters in cyclic deep reactive ion etching," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 29, no. 1, pp. 011002-1–011002-7, Jan. 2011.
- [13] J. W. Choi, W. L. Loh, S. K. Praveen, R. Murphy, and E. T. K. Swee, "A study of the mechanisms causing surface defects on sidewalls during Si etching for TSV (through Si via)," *J. Micromech. Microeng.*, vol. 23, no. 6, pp. 065005-1–065005-7, Jun. 2013.
- [14] J. Reid, S. Mayer, E. Broadbent, E. Klawuhn, and K. Ashtiani, "Factors influencing damascene feature fill using copper PVD and electroplating," *Solid State Technol.*, vol. 43, no. 7, pp. 86–103, Jul. 2000.
- [15] P. C. Andricacos, *Electrochem. Soc. Inter.*, vol. 8, no. 1, p. 32, 1999.
- [16] P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, "Damascene copper electroplating for chip interconnections," *IBM J. Res. Develop.*, vol. 42, no. 5, pp. 567–574, Sep. 1998.
- [17] M. Arnold, C. Emnet, A. Flugel, M. Hahn, A. Wagner, D. Mayer, *et al.*, "New concept for advance 3D TSV copper plating additives," in *Proc. 218th ECS Meeting*, 2010.
- [18] E. Delbos, L. Omnès, and A. Etcheberry, "Bottom-up filling optimization for efficient TSV metallization," *Microelectron. Eng.*, vol. 87, no. 3, pp. 514–516, Mar. 2010.
- [19] A. Radisic, O. Lühn, H. G. G. Philipsen, Z. El-Mekki, M. Honore, S. Rodet, *et al.*, "Copper plating for 3D interconnects," *Microelectron. Eng.*, vol. 88, no. 5, pp. 701–704, May 2011.
- [20] S. Miura and H. Honma, "Advanced copper electroplating for application of electronics," *Surf. Coat. Technol.*, vols. 169–170, pp. 91–95, Jun. 2003.
- [21] T.-H. Tsai and J.-H. Huang, "Electrochemical investigations for copper electrodeposition of through-silicon via," *Microelectron. Eng.*, vol. 88, no. 2, pp. 195–199, Feb. 2011.



Jae Woong Choi received the Ph.D. degree in materials science from Hanyang University, Seoul, Korea, in 2005.

He was involved in process development and integration for semiconductor, microsystems, and equipments. He has been with the Institute of Microelectronics, Singapore, since 2011, where he is involved in process development and integration for advanced packaging.

Ong Lee Guan, photograph and biography not available at the time of publication.

Mao Yingjun, photograph and biography not available at the time of publication.

Hilmi B. Mohamad Yusoff, photograph and biography not available at the time of publication.

Xie Jielin, photograph and biography not available at the time of publication.

Chow Choi Lan, photograph and biography not available at the time of publication.

Woon Leng Loh, photograph and biography not available at the time of publication.



Boon Long Lau received the B.S. degree from the National University of Singapore, Singapore, in 2005.

He was with ST Microelectronics, Singapore, in process engineering. Since 2012, he has been with the Institute of Microelectronics, A*STAR, Singapore. His current research interests include micro-channel and through-silicon-via process integration.



Linda Liew Hwee Hong received the B.Sc. degree in chemistry from the National University of Singapore, Singapore, in 2004.

She has four years of experience as a Process Engineer in chemical vapor processes in backend wafer device fabrication and one year of experience in wet etch process and thermal treatment in frontend silicon wafer fabrication. She is currently a Research Engineer with the Institute of Microelectronics, Singapore, where she is involved in 3-D TSV process integration.



Lau Guan Kian received the M.Sc. degree from the National University of Singapore, Singapore.

She is a Research Engineer with the Institute of Microelectronics, Singapore. Her current research interests include through silicon via process integration and thin wafer handling.



Ramana Murthy was involved in ultra high vacuum technologies, plasma research, surface studies and elemental analysis, semiconductor MESFET technologies in India, where he worked in UHV systems and surface analysis techniques, metallization, wet chemical processing (acid and solvent), wafer thinning and polishing and gold electroplating. He has joined the A-STAR Institute of Microelectronics (IME), Singapore, in 2001, and is currently a Senior Research Engineer (Dry Etch module) for Cu-low-k/Cu-ultralow-k interconnects, photonics, 3-D-Integration, bio/nano/MEMS, and TSV fabrication processes. He is currently a Senior Manager of fabrication with IME. He was conferred various awards based on technical performance and research work. He has published several international conference/journal papers and has several patents as co-inventor. He has reviewed several technical research papers for international journals.

Eugene Tan Swee Kiat, photograph and biography not available at the time of publication.