UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,147,609
Filing Date: March 8, 2012
Issue Date: September 29, 2015

Inventors: Hadi Jebory and David J. Howard
Title: THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

DECLARATION OF MR. JOHN BERG

Case No. IPR2024-01404

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I. INTRODUCTION

1. I am over eighteen years of age and I would be competent to testify as to the matters set forth herein if I am called upon to do so.

2. I have been retained by Fabricant LLP, counsel for the Patent Owner Harbor Island Dynamic LLC to review U.S. Patent No. 9,147,609 ("the '609 Patent") entitled THROUGH SILICON VIA STRUCTURE, METHOD OF FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE, and to provide my technical review, analysis, insights, and opinions regarding the '609 Patent in view of the prior art cited by Petitioners Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively "Samsung" or "Petitioner"). I submit this Declaration in support of Patent Owner's Response in this IPR proceeding. I have personal knowledge of the matters stated herein and would be competent to testify to them if required.

II. BACKGROUND AND QUALIFICATIONS

3. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below.

4. This section summarizes my career history, education, publications, and other relevant qualifications. My full *curriculum vitae* ("CV") is included as

Appendix A.

5. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980, and now I am focusing on analog CMOS circuit design, simulation, modeling, and processing.

6. I am currently an expert consultant in semiconductor design and manufacturing. Since 2010, I have performed this work as a Principal at Berg-Attenborough, Inc., a consulting firm that provides technical consulting and expert witness services to semiconductor companies and law firms. My work as an expert consultant has included developing advanced CMOS processes and multi-chip modules that incorporate logic circuits using SOI, memory devices such as dynamic random-access memory ("DRAM") and flash memory, as well as performing device analysis and testing using scanning electron microscope ("SEM") and transmission electron microscopy ("TEM") technology. In addition to my work as an expert consultant, I have over 35 years of experience as an executive and as an engineer in the semiconductor industry.

7. As the Chief Technologist at American Semiconductor, I developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using 45nm double-gate FET technology. Before joining ASI, I developed

automated tools for the nano-imprint industry at Transfer Devices.

8. Prior to Transfer Devices, I was a Managing Director at Cypress Semiconductor, where I managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, I was Vice President of Technology Development at Zilog, where I managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier.

9. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

III. COMPENSATION

10. My compensation for time worked on this proceeding is not dependent on any issues related to the '609 Patent, the outcome of this proceeding, or the substance of my opinions. My compensation for time worked on this proceeding is at my customary rate of $560 per hour. I have no financial interest in, or affiliation with, the Patent Owner or any of the real parties in interest.

IV. LEGAL PRINCIPLES

A. Claim Construction

11. I understand that claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e., the meaning that the term would have to a person of ordinary skill in the art ("POSITA") in question at the time of the invention in light of what the patent teaches, unless it appears that the inventors were using them to mean something else. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as his/her own lexicographer (i.e., provided special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope).

12. I understand that a POSITA is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but also in the context of the entire patent, including the specification and the prosecution history. The prosecution file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower

interpretation. For these reasons, the words of the claim must be interpreted in view of, and be consistent with, the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

13. I understand that, to determine how a POSITA would have understood a claim term, one should look to those sources available that show what a POSITA would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that one looks primarily to the intrinsic patent evidence, but extrinsic evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

14. Additionally, the context in which a term is used in the Asserted Claim can be highly instructive. Likewise, other claims of the patent in question, both

asserted and not asserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

15. I understand that, while intrinsic evidence is of primary importance, extrinsic evidence, e.g., all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may help one better understand the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, I understand that it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

B. Anticipation

16. I understand that to anticipate a claim, a prior art reference must disclose all elements of the claim within the four corners of the document, and it must disclose those elements arranged as in the claim. I understand that a reference may anticipate even if it does not expressly disclose all the elements if a POSITA reading the reference would at once envisage the claimed arrangement or combination.

17. I understand that if a reference fails to disclose even one element, it does not anticipate that claim. I understand that references that must be modified to disclose a claim element do not anticipate that claim.

C. Obviousness

18. I understand that a patent claim is unpatentable as "obvious" if the subject matter of the claim as a whole would have been obvious to a POSITA as of the time of the invention at issue.

19. I understand that the question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence.

20. I further understand that the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

V. LEVEL OF ORDINARY SKILL IN THE ART

21. It is my understanding that I must address the issues set forth in this Declaration, from the viewpoint of a POSITA at the time of the invention to which the Asserted Patent pertains.

22. I understand that this hypothetical POSITA is considered to have the normal skills of a person in a certain technical field. I understand that factors that may be considered in determining the level of ordinary skill in the art include: (1) the education level of the inventor; (2) the types of problems encountered in the art; (3) the prior art solutions to those problems; (4) rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the education level of active workers in the field.

23. Considering the above factors, in my opinion, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. I also agree that a person

could also have qualified as a POSITA with some combination of (1) more formal education (such as Master of Science degrees) and less technical experience, or (2) less formal education and more technical or professional experience in the fields listed above.

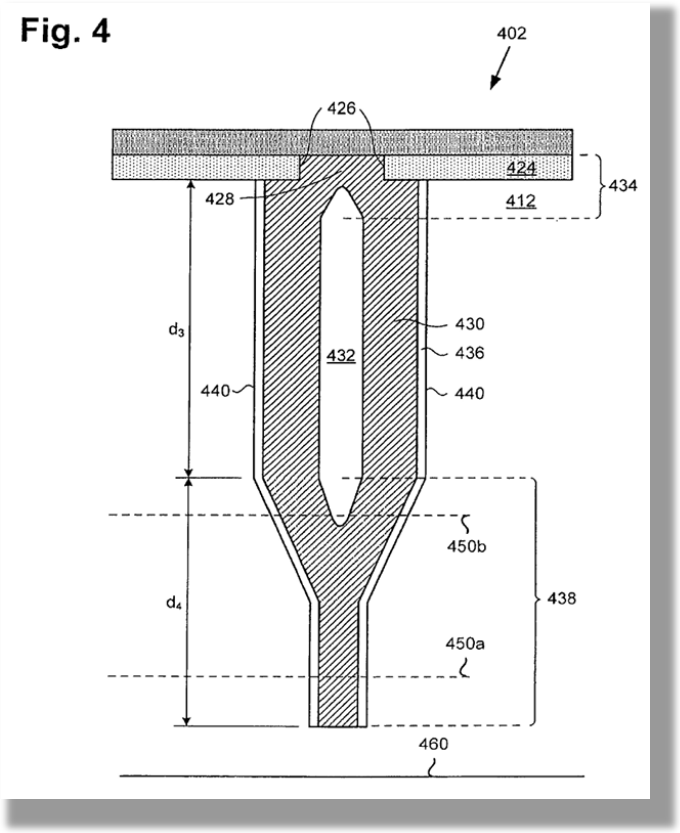
24. I understand that Dr. Thompson has opined that a POSITA would have at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Ex. 1002, ¶ 73. While our contentions are similar, I disagree that a master's degree represents the ordinary level of skill. The '609 Patent is directed to an audience of engineers working to design through-silicon vias. In the industry, it is typical for such engineers to have a bachelor's degree. Indeed, I myself implemented such designs with a bachelor's degree.

25. I understand that the '609 Patent is entitled to an October 7, 2011, priority date, and that is the relevant time period from which a POSITA would evaluate its disclosure and any prior art.

26. My qualifications and experience exceed those of a POSITA, under both my and Dr. Thompson's opinions. Nonetheless, my analysis and opinions herein regarding the Asserted Patent are given from the perspective of a POSITA.

VI. THE ’609 PATENT

27. The ’609 Patent (Ex. 1001) is titled “Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate” and issued on September 29, 2015. The ’609 Patent relates to through silicon vias (TSVs) having pinched off regions. ’609 Patent, Abstract, 1:54-59. 4:9-15. In particular, the ’609 Patent teaches manufacturing TSVs with hollow centers. *Id.*, 4:47-59. The pinched off regions and hollow centers provide significant advantages, such as reducing the TSV’s inductance, and reducing thermal and mechanical stresses. *Id.* 4:60-5:2.



28. Fig. 4 illustrates an embodiment of the '609 Patent's claimed invention. *Id.*, 4:9-5:2. The pinched off region 438 includes a tapered portion that allows the conductive filler to completely fill the bottom of the TSV. *Id.*, 4:48-54. The hollow center 432 includes a section that tapers conically within the pinched off region. *Id.*, 4:48-5:2; Fig. 4.

29. The '609 Patent discloses how through silicon vias (TSVs) are designed to reduce thermal and mechanical stress in semiconductor substrates:

> Thus, various implementations disclosed in the present application provide through silicon vias with a pinched off region which reduce thermal and mechanical stress in semiconductor substrates, as compared to conventional TWVs.

'609 Patent, 5:43-46.

30. The hollow center of the TSVs provides space for the conductive filler to expand inward during high-temperature conditions, minimizing outward expansion that could lead to substrate cracking:

> Hollow center portion 432 provides many beneficial features. For instance, hollow center portion 432 may serve to reduce intrinsic inductance of TSV 402. Hollow center portion 432 also reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions. Such reduction in thermal and mechanical stress reduces cracking in substrate 412.

’609 Patent, 4:60-67.

31. Additionally, the pinched-off regions at the top and bottom of the TSVs prevent contamination during processing, further enhancing the reliability of the substrate. *Id.*, 6:11-15.

32. I understand that the Challenged Claims in this proceeding are Claims 1-18. Claims 1 and 11 of the ’609 Patent are independent claims.

VII. THE ALLEGED PRIOR ART

A. Cooney

33. U.S. Patent Application Publication No. US 2009/0278237 to Cooney, III et al. (Ex. 1004) is titled “Through Substrate Via Including Variable Sidewall Profile” and published on November 12, 2009. *Cooney* is directed to forming a via in a semiconductor substrate. Ex. 1004, Abstract, ¶ [0002]. *Cooney’s* via is torpedo shaped, and composed of four regions. *Id.*, ¶¶ [0042], [0050]-[0055], FIGS. 4-6. The regions include comparatively wide linewidth regions R1 and R3, as well as a tapered region R4. *Id.*, ¶ [0051], FIG. 5.

34. *Cooney* is directed to “through substrate vias within microelectronic substrates.” *Id.* ¶ [0002]. *Cooney* describes a microelectronic structure, specifically a semiconductor structure, and a method for fabricating it. *Id.*, Abstract. The

structure includes an aperture within a substrate, which is designed to accommodate a through substrate via with an irregular sidewall profile:

> The through substrate via 24" is located and formed into an aperture within the semiconductor substrate 10" of FIG. 10 that has an irregular sidewall profile.

Ex. 1004, ¶ [0065].

35. This profile consists of sequential regions: a first wide region, a constricted region, a second wide region, and a tapered region:

> The particular sidewall profile includes, downwardly progressing through the substrate: (1) a first comparatively wide region at a surface of the substrate; (2) a constricted region contiguous with the first comparatively wide region; (3) a second comparatively wide region contiguous with the constricted region; and (4) an inward tapered region contiguous with the second comparatively wide region.

Ex. 1004, ¶ [0018].

36. *Cooney* specifies the fabrication process, including etching methods, material choices, and the integration of liner and conductor layers.

37. *Cooney* is silent on a method of reducing stress caused by through silicon vias. *Cooney* is silent on a method to reduce cracks or delamination in the silicon substrate due to the stress induced by the CTE mismatch of the silicon TSV material and the silicon substrate.

B. Dean

38. U.S. Patent Application Publication No. US 2011/0057319 to Dean, Jr., et al. (Ex. 1010) published on March 10, 2011. *Dean* relates to arranging through silicon vias in an IC layout to result in less wafer breakage. Ex. 1010, Abstract.

C. Farooq

39. U.S. Patent No. 8,237,288 to Farooq et al. (Ex. 1016) is titled "Enhanced Electromigration Resistance in TSV Structure and Design" and issued on August 7, 2012. *Farooq* relates to structures and connections of TSVs. Ex. 1016, Abstract.

D. Chen

40. U.S. Patent Application Publication No. US 2010/0032843 to Chen et al. (Ex. 1011) published on February 11, 2010. *Chen* relates to a particular layout of TSVs. Ex. 1011, Abstract.

VIII. CLAIM CONSTRUCTION

41. I understand that Dr. Thompson was not asked to opine on the construction of any claim terms in the '609 Patent. Ex. 1002, ¶¶ 70–71.

42. I also understand that Petitioner has taken the position that certain phrases should not be entitled to patentable weight. For example, the Petition states that "[t]he phrase 'to reduce thermal stress in said semiconductor substrate' states

the use of or explanation for the hollow center and should be entitled to no patentable weight over the prior art." Pet. at 20. The Petition also states that "[t]he phrase 'to provide space for said conductive filler to expand inward' states another use for the functioning of the hollow center and should be entitled to no patentable weight over the prior art." *Id.* at 24. Finally, the Petition states that "[t]he phrase 'to prevent contamination during processing of said semiconductor substrate' states yet another use for the functioning of the pinched off region and should be entitled to no patentable weight over the prior art." *Id.* at 31.

43. I have been instructed by counsel to consider the plain meaning of all claim terms, including the phrases that the Petitioner claims are not entitled to patentable weight.

44. I disagree with Dr. Thompson that no claim terms need express construction to resolve the disputes in this proceeding, because he is apparently interpreting the claims to merely require the existence of the claimed hollow center, not a hollow center that reduces thermal stress.

45. In my opinion, the parties appear to have a differing view of the scope of the term "each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate," as recited in the independent

claims of the ’609 Patent.

46. According to Petitioner and Dr. Thompson, all voids in a through-silicon via would reduce the required thermal stress. *See* Ex. 1002, ¶ 123 (“Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney’s* void 25 reduces thermal stress in *Cooney’s* substrate”); Ex. 2007 (Thompson transcript)Ex. 2007, 30:25-31:11 (“A void that’s buried obviously reduces stress as the tungsten expand [sic] and squashes – squashes the void and expands inward into the void.”).

47. I disagree with Petitioner and Dr. Thompson that all voids (or all hollow centers) in through-silicon vias reduce thermal stress in the substrate.

48. In my opinion, the terms “each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate” in Claim 1 and “each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate” in Claim 11 should be construed to mean that the hollow center has the function of reducing thermal stress in the substrate. In my opinion, the POSITA would understand this to be the plain and ordinary meaning of the claim term.

49. Contrary to Dr. Thompson's analysis, in my opinion, the POSITA would have understood that in certain circumstances, the presence of a hollow center or void in a TSV may increase thermal stress in the substrate, rather than reduce it, even when it provides space for the TSV fill material to expand inward. Evidence relied upon by Dr. Thompson supports this. For example, U.S. Patent Application Publication No. 2009/0302480 to Birner et al. (Ex. 1022) states that "the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum deflectivity arising from thermal or other stress related defects." Ex. 1022, ¶ [0037]. *Birner* also provides a discussion regarding how to select the size and shape of the fill material in order to create a void that reduces thermal stress. *Id.* ¶ [0038]. *Birner* notes that:

> As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material **50** is selected relative to the dimension of the tailored void **90**. For example, a fraction of the fill material **50** (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1 *b*, this fraction of the fill material **50** (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV}. The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material **50** (α_{FM}) and the tailored void (α_V) as $f_{FM}=(\alpha_{Si}-\alpha_V)/(\alpha_{FM}-\alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM}\approx 0$, the fraction $f_{FM}=\alpha_{Si}/\alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening **250** r_{TSV}. In other words, a partial

> fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments, thicker fill material can be used as stress up to a certain critical limit (e.g., critical shear stress) can be safely accommodated. For example, the stress produced during a small increase in temperature may not be significant. Hence, in various embodiments, a numerical simulator is used to design the shape of the voids. In such embodiments, a suitable thickness is calculated numerically to minimize, for example, stress concentrations during subsequent processing. In some embodiments, a more sophisticated analysis utilizing 2D or 3D simulations using finite element simulators determines the appropriate shape and structure of the tailored void **90** relative to the fill material **50**. Such numerical calculations can account for changes in stress in different regions, for example, in the corners. Suitable metrics, such as Von Misses criterion, based on the stress tensor may be used to monitor the stress in the structure.

Id. The POSITA would have understood from this reference that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur.

50. As another example, as shown in the paper *Thermal Stresses around Void in Through Silicon Via in 3D SiP* by T. Kinoshita, et al., which was published in the 2014 International Conference on Electronics Packaging (April 2014) (Ex. 2008, "Kinoshita"), under operational conditions the presence of a void can actually increase thermal stresses inside the TSV, which would in turn increase thermal stresses in the silicon substrate.

51. Fig. 5 of *Kinoshita* is shown below:

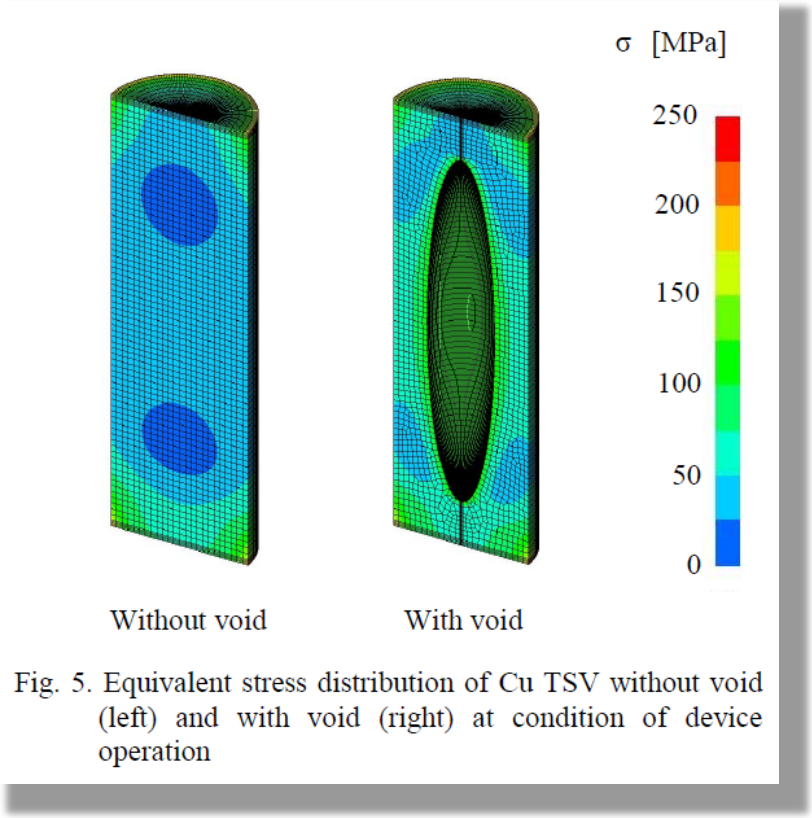


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

52. As shown in Fig. 5 and explained by *Kinoshita*:

> *In the case of the TSV structure without voids, the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa.*
>
> . . .
>
> *In case of the TSV structure with a void, the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa.* It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper.

Ex. 2008, at 107 (emphasis added). The "with void" TSV structure in *Kinoshita* exhibits higher stress levels than the non-voided TSV, including on the edges of the TSV. In *Kinoshita*, without additional thermal considerations present, this thermal stress is transferred to the semiconductor substrate. *Kinoshita* also notes that "In the cases the TSV structure without voids and with a void, the stress on the inner surface of Si was estimated to be about 100 MPa," indicating that the presence of a void does not reduce the stress on the inside of the substrate.

53. Therefore, it is my opinion that Petitioner and Dr. Thompson are incorrect in their assumption that, simply because of the presence of a void, that thermal stress is reduced in the silicon substrate.

54. The POSITA would have understood that, to meet this claim limitation, the hollow center must serve the purpose of reducing thermal stress in the silicon substrate, and that is what the plain meaning of this claim limitation requires.

IX. ALL GROUNDS FAIL

55. Claims 1 and 11 each require a plurality of through-silicon vias that

have "a hollow center [] to reduce thermal stress in said semiconductor substrate."[1] Dr. Thompson contends that this claim element is anticipated or rendered obvious by *Cooney*. Ex. 1002, ¶¶ 120-134. I disagree. The "optional void" in *Cooney* does not reduce thermal stress in the semiconductor substrate.

A. Grounds 1A and 1B: Cooney Does Not Disclose or Render Obvious a Hollow Center to Reduce Thermal Stress in the Semiconductor Substrate

56. The Petition presents in Ground 1A that Claims 1-6, 9-14, 17, and 18 are anticipated by *Cooney* and in Ground 1B that the same claims are rendered obvious by *Cooney*. I disagree.

57. As admitted by Dr. Thompson, *Cooney* does not mention "thermal stress" and does not discuss the purpose of the "optional void" in its disclosure. Ex. 2007, 30:15-31:11. This, in my opinion, is sufficient to show that *Cooney* does not anticipate any '609 Patent claim.

[1] Claim 1 requires "each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward" while Claim 11 requires "each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate." The functional result of both of these claims is that the hollow center must have certain properties that reduce thermal stress in the substrate and, therefore, these claims can be analyzed together.

58. According to *Cooney*, the conductor layer 24 has an "optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture." Ex. 1004, ¶ [0055].

59. In my opinion, *Cooney's* "optional void" is not the same as the hollow center claimed in the '609 Patent. Whereas *Cooney's* "optional void" is merely an artifact of processing with encompassing a volume that is much less than 15% of the total via height per *Cooney's* Figure, the hollow center represents greater than ~40% of the via's height.

60. Further, *Cooney* creates a trench with a bulge in the profile:

> FIG. 4 shows an aperture A4 that is etched into a semiconductor substrate 10' derived from the semiconductor substrate 10 that is illustrated in FIG. 3, while using the second photoresist layer 20 as a mask. As is illustrated within the schematic cross-sectional diagram of FIG. 4, the aperture A4 is formed with a downward pointing torpedo shape. Within FIG. 4, the phantom lines correspond with a theoretical straight sided aperture that may alternatively be formed into the semiconductor substrate 10' while using the second photoresist layer 20 as an etch mask. As is illustrated in FIG. 4, the aperture A4 is wider at the widest point thereof in comparison with the theoretical straight sided aperture and narrower at the inward pointed tip thereof in comparison with the theoretical straight sided aperture.

Ex. 1004, ¶ [0042].

61. FIG. 8 shows the aperture, A4, filled with the TSV metal 24". The bulge in the TSV means that there is more metal in the TSV, than there would otherwise be without the bulge. Most TSV's today do not have this bulge, because that additional metal being in the TSV due to the bulge will increase stresses in the silicon substrate.

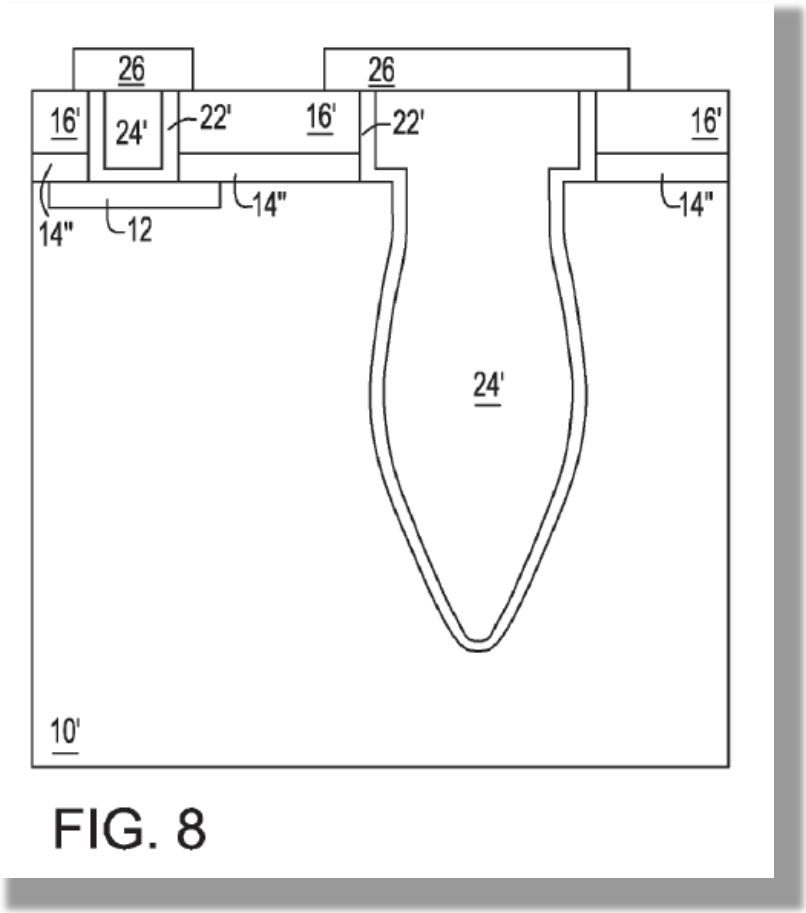


FIG. 8

Ex. 1004, FIG. 8.

62. It is my opinion that the "optional void" in *Cooney* does not reduce thermal stress in the substrate for several reasons. First, the torpedo shape used to create it actually increases thermal stress by requiring additional metal filler and focusing forces on a smaller part of the silicon. Second, a POSITA would understand that a "void" is different from a hollow center, and is too small to reduce thermal stress. Third, a void as disclosed in *Cooney* can often increase thermal stress, as disclosed in *Kinoshita*. Dr. Thompson does not analyze any of these features, and merely relies upon the mistaken assumption that all voids in TSV's reduce thermal stress in the surrounding substrate.

1. All Voids Do Not Decrease Thermal Stress

63. As I explained earlier, the foundational assumption by Petitioner and Dr. Thompson that *all* voids and hollow centers in *all* TSV's reduce thermal stress is incorrect. For example, U.S. Patent Application Publication No. 2009/0302480 to Birner et al. (Ex. 1022) states that "the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum deflectivity arising from thermal or other stress related defects." Ex. 1022, ¶ [0037]. *Birner* also provides a discussion regarding how to select the size and shape of the fill material in order to create a void that reduces thermal stress. *Id.* ¶ [0038]. *Birner* notes that:

As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material **50** is selected relative to the dimension of the tailored void **90**. For example, a fraction of the fill material **50** (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1 *b*, this fraction of the fill material **50** (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV}. The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material **50** (α_{FM}) and the tailored void (α_V) as $f_{FM}=(\alpha_{Si}-\alpha_V)/(\alpha_{FM}-\alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM}\approx 0$, the fraction $f_{FM}=\alpha_{Si}/\alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening **250** r_{TSV}. In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments, thicker fill material can be used as stress up to a certain critical limit (e.g., critical shear stress) can be safely accommodated. For example, the stress produced during a small increase in temperature may not be significant. Hence, in various embodiments, a numerical simulator is used to design the shape of the voids. In such embodiments, a suitable thickness is calculated numerically to minimize, for example, stress concentrations during subsequent processing. In some embodiments, a more sophisticated analysis utilizing 2D or 3D simulations using finite element simulators determines the appropriate shape and structure of the tailored void **90** relative to the fill material **50**. Such numerical calculations can account for changes in stress in different regions, for example, in the corners. Suitable metrics, such as Von Misses criterion, based on the stress tensor may be used to monitor the stress in the structure.

Id. The POSITA would have understood from this reference that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur.

64. For example, as shown in the paper *Thermal Stresses around Void in Through Silicon Via in 3D SiP* by T. Kinoshita, et al., which was published in the 2014 International Conference on Electronics Packaging (April 2014) (Ex. 2008, "Kinoshita"), under operational conditions the presence of a void can increase thermal stresses inside the TSV, which would in turn increase thermal stresses in the silicon substrate.

65. Fig. 5 of *Kinoshita* is shown below:

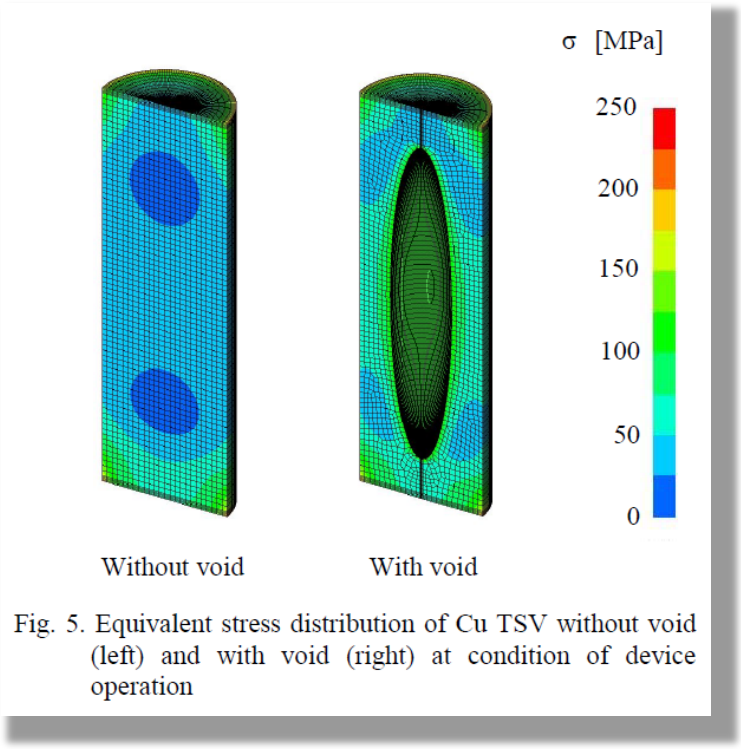


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

66. As shown in Fig. 5 and explained by *Kinoshita*:

> *In the case of the TSV structure without voids, the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa.*
> . . .
> *In case of the TSV structure with a void, the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa.* It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper.

67. Ex. 2008, at 107 (emphasis added). The "with void" TSV structure in *Kinoshita* exhibits higher stress levels than the non-voided TSV, including on the

edges of the TSV. In *Kinoshita*, without additional thermal considerations present, this thermal stress is transferred to the semiconductor substrate. *Kinoshita* also notes that "In the cases the TSV structure without voids and with a void, the stress on the inner surface of Si was estimated to be about 100 MPa," indicating that the presence of a void does not reduce the stress on the inside of the substrate. Therefore, it is my opinion that Petitioner and Dr. Thompson are incorrect in their assumption that, simply because of the presence of a void, that thermal stress is reduced in the silicon substrate.

68. In my opinion, Dr. Thompson's analysis of the void in *Cooney* is insufficient. In order to determine whether the optional void in *Cooney* decreases thermal stress in the substrate, Dr. Thompson would have needed to perform *some* analysis of the specific features in *Cooney*, rather than simply relying on the incorrect assumption that all voids decrease thermal stress in the substrate. I do not believe that *Cooney* provides me (or the POSITA) with the information necessary to determine whether the optional void decreases thermal stress, at least because the relative size of the void as compared to the size of the TSV and the size of the liner layer is not given.

69. Additionally, the POSITA when presented with the teachings in

Cooney would have known that a "void" is generally understood to be a very small "pinhole" type of defect that occurs when a TSV is incompletely filled. For example, a paper contemporary to the '609 Patent discusses voids as "defect[s]" that need to be further studied. Ex. 2009, Kong et al., *3D-Interconnect: Visualization of Extrusion and Voids Induced in Copper-Filled Through-Silicon Vias (TSVs) at Various Temperatures Using X-Ray Microscopy*, Microelectronic Engineering 92 (2012), at 27 ("voids and other defects in the TSVs on the extrusion phenomenon should be made a topic of further study"). Figs. 3-6 of this paper show the size of typical voids in a 4 micrometer TSV:[2]

[2] *See also* Ex. 2010, J.W. Choi, et al., TSV Cu Filling Failure Modes and Mechanisms Causing the Failures, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: "If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed."

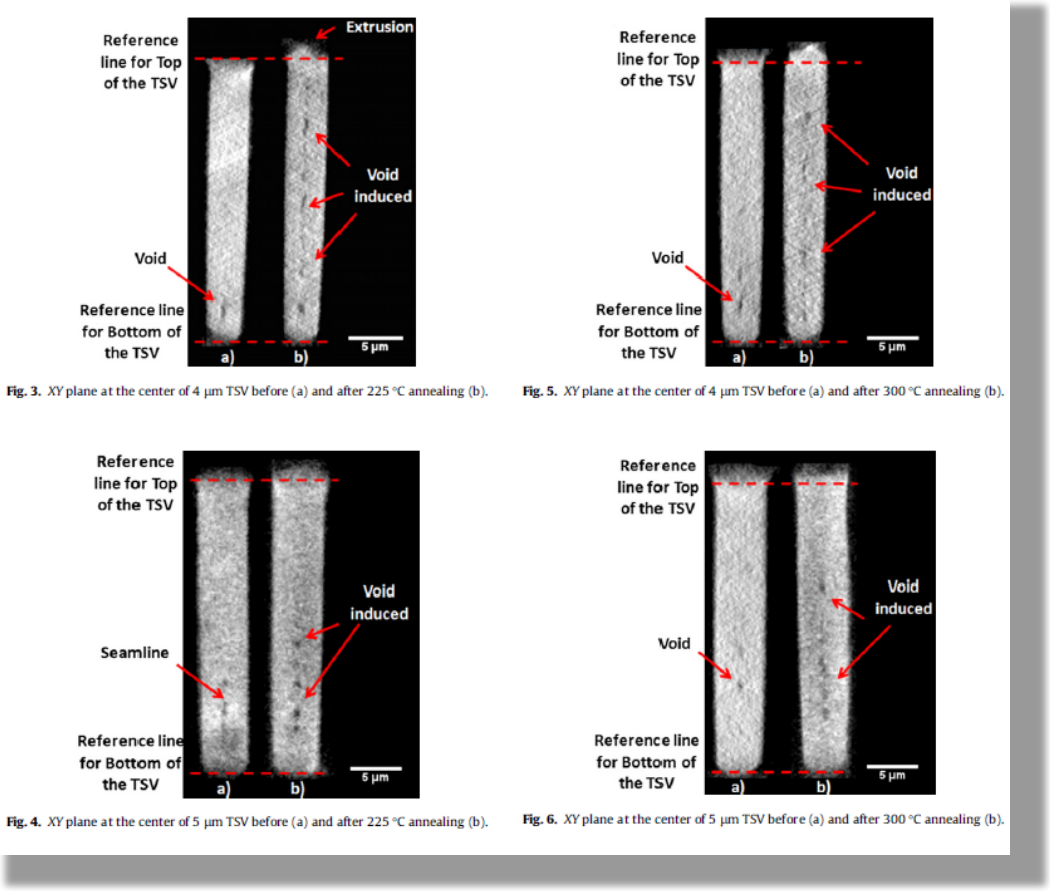


Fig. 3. *XY* plane at the center of 4 μm TSV before (a) and after 225 °C annealing (b).

Fig. 5. *XY* plane at the center of 4 μm TSV before (a) and after 300 °C annealing (b).

Fig. 4. *XY* plane at the center of 5 μm TSV before (a) and after 225 °C annealing (b).

Fig. 6. *XY* plane at the center of 5 μm TSV before (a) and after 300 °C annealing (b).

70. Aside from the Figure in *Cooney*, it provides the POSITA no additional information or guidance regarding the size of the void. Therefore, the POSITA would not have understood *Cooney's* use of the term "void" to mean a hollow center of sufficient size to reduce thermal stress.

2. The Shape of Cooney's TSV Increases Thermal Stress

71. The optional void in *Cooney* is created by incompletely filling *Cooney's* TSV.[3] Ex. 1004, ¶ [0055]. In my opinion, the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV. This is because filling this bulge requires additional metal to fill the TSV. Because there is more metal, it will increase by a greater factor at a given temperature than a straight TSV with less metal. And the torpedo shape itself can increase thermal stresses, by focusing stress on certain portions of the substrate rather than spreading them out along the entire TSV. Dr. Thompson did not analyze the shape of the void in *Cooney*.

3. Dr. Thompson Does Not Analyze the Size of Cooney's Void

72. As I explained earlier, *Cooney's* "optional void" is merely an artifact of processing with encompassing a volume that is much less than 15% of the total via height per *Cooney's* Figure, the hollow center represents greater than ~40% of the via's height. Although I understand that it can be improper to rely on Figures in a

[3] Ex. 2010, J.W. Choi, et al., TSV Cu Filling Failure Modes and Mechanisms Causing the Failures, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: "If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed."

patent for scale, *Cooney* provides no other basis by which to measure the size or volume of the optional void. Therefore, to the extent that Dr. Thompson appears to use the Figures to interpret the size of *Cooney's* optional void, I will do the same. The POSITA would have recognized that a "void" in a TSV is typically an artifact of processing caused by incomplete filling of the TSV. Rather than desirable features, voids are typically to be avoided.[4] Voids, as typically understood by the POSITA, are not large enough to have any appreciable impact on the reduction of thermal stress in the semiconductor substrate. *See* Ex. 2011, *Low Stress TSV Arrays for High-Density Interconnection*, Jiao et al. at 201-205 (distinguishing a "hollow" TSV from a void). A "void" is different from a hollow center. Aside from the Figure in *Cooney*, *Cooney* does not present any data or information necessary to inform the POSITA as to whether the optional void is large enough to decrease thermal stress in the substrate, and therefore it is my opinion that Dr. Thompson did not have sufficient information on which to base his opinions.

[4] Ex. 2010, J.W. Choi, et al., TSV Cu Filling Failure Modes and Mechanisms Causing the Failures, IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 4, April 2014, p. 581: "If there are any issues in the process integration procedure, Cu filling defects, observed as voids, and inside the TSVs will be observed."

4. The References Allegedly Disclosing the Knowledge of a POSITA Are Insufficient

73. Dr. Thompson, in an apparent recognition of the weakness in *Cooney*, opines that the POSITA "would have recognized that it was well known in the art that the presence of a void in a TSV reduces thermal stress in the surrounding substrate." Ex. 1002, ¶ 125. I disagree. Dr. Thompson also cites to two references that apparently explain this feature, U.S. Patent Application Publication No. 2003/0111733 to Pogge et al. and U.S. Patent Application Publication No. 2006/0027934 to Edelstein et al. *Id.* In my opinion, neither *Pogge* nor *Edelstein* disclose that voids reduce thermal stresses in the semiconductor substrate.

74. *Pogge* discloses a through-silicon via structure filled with copper and surrounded by several additional layers. *Pogge's* vias include an oxide layer 21, a trench liner 22, and a layer of copper 23, then another layer of copper 24 that fills the void. Ex. 1005, ¶¶ [0026]-[0027]. *Pogge* does state that the void "has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature." *Id.*, ¶ [0027]. However, *Pogge* does not mention or state that the stresses would be borne by the semiconductor substrate. And, even if *Pogge* does teach that thermal stresses are relieved by the void in the particular device disclosed in *Pogge*, it does

not in my opinion teach that the POSITA would have known that all voids decrease thermal stress in all TSVs because, as discussed above, that assumption by Dr. Thompson is not correct.

75. *Edelstein* similarly does not inform the POSITA that a void in a TSV can be used to protect the substrate from thermal stresses. *Edelstein*, rather, discloses that a "through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures." Ex. 1006, ¶ [0047]. *Edelstein's* discussion is entirely centered around removing mechanical stresses, not thermal stresses, and in any event, *Edelstein* also never discloses the reduction of stress (whether mechanical or thermal) in the substrate itself. And, even if *Edelstein* does teach that thermal stresses are relieved by the void in the particular device disclosed in *Edelstein*, it does not in my opinion teach that the POSITA would have known that all voids decrease thermal stress in all TSVs because, as discussed above, that assumption by Dr. Thompson is not correct.

76. Therefore, I completely disagree with Dr. Thompson that the POSITA would have recognized that it was well-known in the art at the time of the invention that the presence of a void in a TSV reduces thermal stress in the surrounding

substrate.

77. Although Dr. Thompson states that he is only relying on *Pogge* and *Edelstein* as evidence of the knowledge of a POSITA, he also opines that the structures of the TSV's in *Edelstein*, *Pogge*, *Cooney*, and the '609 Patent are "very similar." Ex. 1002, ¶¶ 127, 130. Dr. Thompson notes that the stress-relieving characteristics of the various voids disclosed in these references would be "manifested by the void in Cooney's TSV." *Id*. I disagree that the structures of the TSV's in the various references are "very similar," and Dr. Thompson does not explain or analyze why they are similar. In particular, the shape and sizes of the disclosed TSV's and voids are different. As stated above, I also disagree with Dr. Thompson that the TSV's disclosed in *Edelstein* and *Pogge* reduce thermal stress in the substrate materials disclosed in those references at all. And, further, I disagree with Dr. Thompson that, even if the claimed thermal stress relieving characteristics in the substrate were disclosed in *Pogge* or *Edelstein*, they would be "manifested" in the void disclosed in *Cooney*, because Dr. Thompson does not analyze the differences between the TSV and its optional void in *Cooney*, as compared to the TSV's and voids in *Pogge* and *Edelstein*, and does not consider the teachings of *Birner* and *Kinoshita* in his analysis.

B. Grounds 2, 3, and 4 Also Fail

78. Grounds 2, 3, and 4 relate only to dependent Claims 7, 8, 15, and 16. Petitioner and Dr. Thompson rely only on *Cooney* to attempt to invalidate the independent claims. Because, as discussed above, *Cooney* does not anticipate or render obvious the independent claims, the dependent claims also are not rendered obvious by *Cooney* in combination with *Dean*, *Farooq*, or *Chen*.

X. MATERIALS CONSIDERED

79. In providing my technical review, analysis, insights, and opinions, I have considered the ’609 Patent and its prosecution history.

80. I have also considered the Petition filed by the Petitioner in this proceeding and the relevant exhibits relied on by Petitioner, including the expert Declaration submitted by Scott E. Thompson, Ph.D. I have also reviewed the transcript of the deposition of Dr. Thompson, dated June 17, 2025 (Ex. 2007).

81. In addition, I have reviewed the materials cited in this Declaration, as well as the prosecution history of *Cooney*.

82. I have also considered my own experience and knowledge, as discussed above, and as described more fully in my CV, in areas including semiconductor design, manufacturing, and other related technologies.

XI. CONCLUSION

83. I declare under penalty of perjury that the foregoing is true and correct.

Dated: June 26, 2025

John Berg

APPENDIX A

JOHN BERG

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SUMMARY

As the Chief Technologist at American Semiconductor, Mr. Berg developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using 45nm double-gate FET technology. Before joining ASI, Mr. Berg developed automated tools for the nano-imprint industry at Transfer Devices. Prior to Transfer Devices, Mr. Berg was a Managing Director at Cypress Semiconductor, where he managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology.

Mr. Berg has been an expert witness in semiconductor process development, silicon device physics, semiconductor design, CAD tools, lithography, semiconductor bonding including CMP, and business practices. He served as the plaintiff's expert witness in the Palmchip v. Ralink (Mediatek) microprocessor patent infringement. He was an expert witness for the plaintiff in Semi-Materials Co. Ltd. v. MEMC Pasadena Inc, in which he testified at jury trial twice and was deposed twice. In both cases, the plaintiff won, with more than $19M being awarded to Mr. Berg's client. Mr. Berg also has testified in front of the US Patent Office in the re-examinations of three patents, all of which were successfully defended, and has been an expert in numerous IPR cases. He was deposed as a Cypress employee in Cypress Semiconductor v. Altera Corp., where Altera was sued for interference with contract, trade secret misappropriation, and unfair competition involving programmable logic devices. At Standard Microsystems, he did reverse engineering analysis on competitors' products; these analyses led to three successful licensing agreements with other semiconductor companies.

PROFESSIONAL EXPERIENCE

BERG-ATTENBOROUGH, INC. **SEPTEMBER 2010 - PRESENT**

PRINCIPAL (2 EMPLOYEES)

Berg-Attenborough, Inc. is a consulting firm, which does technical consulting for Top 50 semiconductor companies and does expert witness work for patent and business issues.

Key Achievements:

- Developed wafer bonding and CMP for advanced photonics integrated circuit processing.
- Fan-Out Wafer Level Packaging, FO-WLP consulting for Draper Laboratories
    - Successfully developed a 60+ chip multi-chip module including MPU, FPGA, DRAM, and FLASH.
    - Uncovered two temperature cycle reliability problems with the existing FO-WLP technology and instituted corrective actions to the process and design to eliminate these.
        - Modified interlayer dielectric and solder mask to correct die cracking
            - Problem uncovered by SEM and verified via SEM and reliability testing
        - Modified metal bus rules using Ansys and empirical data to ameliorate die cracking

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PROFESSIONAL EXPERIENCE (CONT.)

AMERICAN SEMICONDUCTOR, INCORPORATED **2005-2014**

CHIEF TECHNOLOGIST (22 EMPLOYEES)

American Semiconductor is fabricating radiation-hard CMOS products for military and aerospace customers.

Key Achievements:

- Hands-on in-fab development the front-end & back-end full wafer scale process for an antenna array product, which resulted in a Top Supplier of the Year Award from Boeing. A low temperature substrate-to-substrate bonding technique was developed specifically for this product.
- Hands-on in-fab development of the company's double-gate FET process, and successful transfer of the company's double-gate FET CMOS process from university laboratory into a CMOS production facility. This included CMP, lithography, and etching processes.
- Design of MCU/analog RF/sensor/memory flexible system-on-chip reference products:
  - Products includes hardware and software/firmware for system control and security/encryption
  - Process development included direct low temperature and high temperature direct wafer-to-wafer bonding techniques with and without through silicon vias (TSV's) to reduce system form factor.
  - Flip-chip, ball-bond, and wire-bonding used to assemble product.

TRANSFER DEVICES, SANTA CLARA, CA **2004-2005**

CHIEF OPERATING OFFICER (12 EMPLOYEES)

Transfer Devices is a lithography start-up, which is commercializing technology developed in Professor Fabian Pease's laboratory at Stanford University.

Key Achievements:

- Built a class 10 manufacturing clean room and delivered product to customers.
- Launched the ExaGlide 10r nano-patterning production tool development program
- Improved tool uptime from <10% to 95% and product yields from 50% to 99.9%

NANTERO, WOBURN, MA **2003-2004**

VICE PRESIDENT, NEW PRODUCT DEVELOPMENT (50 EMPLOYEES)

Nantero is developing non-volatile random-access memory using carbon nanotube switches.

Key Achievements:

- Hired and led the design team that taped out a 4Mb non-volatile memory chip, which resulted in a radiation-hardened non-volatile memory technology.

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PROFESSIONAL EXPERIENCE (CONT.)

CYPRESS SEMICONDUCTOR, SAN JOSE, CA **1998-2002**

MANAGING DIRECTOR, PROGRAMMABLE LOGIC (5500 EMPLOYEES)

Cypress Semiconductor, a public company, is a broad line supplier of semiconductor components.

Key Achievements:

- Program manager for Delta39K, 37K product lines, including hardware development, and software/firmware development on systems instantiated by customers.
- First Cypress multi-chip module product, using flip-chip and ball-bonding technologies.
- Hired, trained, and managed the ESD team at Cypress (3 technology and design engineers). Reduced the number of corporate ESD-related design errors from 50% to <5% by standardizing ESD design rules, testing and incorporating secondary breakdown into the ESD design, standardizing ESD design methodology, and instituting formal ESD design reviews into Cypress's design flow. Purchased test systems for in-house ESD testing.
- Integrated NAND FLASH IC and SRAM-based CPLD IC into 1st Cypress multichip module
- Developed and put into production the company's 0.25um BiCMOS and 0.18um SiGe HBT processes used for Datacommunications Products. Substantial materials and CMP work.
    - Provided PDK, CAD, and Device support.
- Increased revenues from $38M to $72M by increasing the number of PLD/FPGA product families to 6, including the Ultra37000, Delta39K, Quantum38K and PSI product families
- Designed CPLD products in TSMC's 0.13um technology which used copper interconnect.

ZILOG CORPORATION NAMPA, ID **1990-1998**

VICE PRESIDENT, TECHNOLOGY DEVELOPMENT (1600 EMPLOYEES)

Zilog was a pre-IPO company that successfully went public in 1991 and was later acquired by IXYS.

Key Achievements:

- Trained and led the Nampa site's 15-person Design Department and 30-person Technology Development Department; delivered memory cells (SRAM, EEPROM, EPROM, NOR Flash), memory block compilers, and I/O cells for the company's design library for its system-on-chip and application-specific standard products.
- Designed, built, and qualified the $175M 200mm fabrication facility: 1st silicon yield.
    - 0.25um CMOS technology, including CMP, tungsten plugs, trench isolation, and low k dielectric. First dry-in/dry-out CMP metals and dielectric tools brought into production.
    - Solved the temperature cycle problem with the 200mm line within 90 days after initial observation. Solution involved modifying design rules for metallization and improved planarization.
- Hired, trained, and led the design team that taped out 6 system-on-chip products per year for 8 years for the $120M Z8 microcontroller business unit.
- Worked with outside laboratories to ensure hardware design compliance to FCC's EMF/EMI requirements.
- Modified design rules and design clocking scheme to improve 1st pass yields.

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PROFESSIONAL EXPERIENCE (CONT.)

STANDARD MICROSYSTEMS CORPORATION, HAUPPAUGE, NY **1980-1990**
ENGINEERING DIRECTOR (500 EMPLOYEES)

Standard Microsystems was a public company in 1980, and later, was acquired by Microchip, Inc.

Key Achievements:

- Began career as a hands-on manufacturing CVD engineer working with Applied Materials deposition tools.
- Solved the company's Highly Accelerated Temperature/Humidity Stress Test (HAST) problem, that had been plaguing the company for five years, using optimizing thin film dopant concentration.
- Instituted DOE and six sigma process development practices in 1986.
- Hired, trained, and managed 26 sustaining and development engineers in the company's 2500 wpm wafer fab. Developed and transferred five 2um/sub-2um CMOS technologies into production.
- Reversed engineered Intel, TI, and National Semiconductor products to provide evidence of infringement against Standard Microsystem's patents. This included working with and coordinating external laboratories to provide deconstruction analysis.

EDUCATION

2002-2003 **STANFORD UNIVERSITY** **PALO ALTO, CA**
M.S. Management, Graduate School of Business. Sloan Fellow.

1998-2002 **STANFORD UNIVERSITY** **PALO ALTO, CA**
16 graduate credits in Electrical Engineering (GPA = 4.1) in circuit design

1975-1980 **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** **CAMBRIDGE, MA**
BS Physics. Four-year National Merit Finalist and Scholar. Intercollegiate crew

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PUBLICATIONS

"MOS Transistor Technology from Planar to Nanowire Transistors," Mantha, B. and Berg, J., Silicon Valley Engineering Council Journal, Volume 1, 2009, Pages 23-32.

"Substrate Bias Effects on Transiently Triggered Latchup in Bulk CMOS," Chang, L. and Berg, J.; IEEE Transactions on Electron Devices, Volume 33, Issue 1, Jan. 1986 Pages 165 - 167

"A Derivative Method to Determine a MOSFET's Effective Channel Length and Width Electrically**,"** Chang, L. and Berg, J.; IEEE Electron Device Letters, Volume 7, Issue 4, Apr 1986 Pages 229 – 231.

"A Simplified Model to Predict the Linear Temperature Coefficient of a CMOS Inverter's Delay Time," Chang, L., Khoa Vo and Berg, J.; IEEE Transactions on Electron Devices, Volume 34, Issue 8, Aug 1987 Pages 1834 – 1837.

CONFERENCE LEADERSHIP AND PRESENTATIONS

Co-Chairman, 2007 IEEE San Francisco Bay Area Nanotechnology Symposium, July 2007.

"Rad-Hard Reconfigurable Bidirectional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet 0.18um SOI CMOS Technology," K. DeGregorio, D. Wilson, S. Parke, J. Berg, M. Goldston, R. Hayhurst, D. Hackler 12th NASA Symposium on VLSI Design

Committee Member, Programmable Logic Sub-Committee, 2003 IEEE Solid State Circuits Conference, San Francisco, CA

"Measuring the Effective Channel Length of the Deep Submicron MOSFET and the Channel Broadening Effect," S.H. Chung, Tim Carns, S.K. Lee, L. DeBruler, and J. Berg, Proceedings of the Thirteenth Biennial University/Government/Industry Symposium, IEEE Press, pp. 176-181, 1998.

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PATENTS

Patent Number	Title
8,913,402	Triple-damascene interposer
7,595,527	Non-volatile electromechanical field effect devices and circuits and methods of forming same
6,476,635	Programmable number of metal lines and effective metal width along critical paths in a programmable logic device
6,436,195	Method of fabricating a MOS device
6,190,973	Method of fabricating a high quality thin oxide
6,165,846	Method of eliminating gate leakage in nitrogen annealed oxides
6,156,653	Method of fabricating a MOS device
5,978,127	Light Phase Grating Device
5,631,180	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,498,896	High threshold metal oxide silicon read-only-memory transistors
5,389,565	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,338,423	Method of eliminating metal voiding in a titanium nitride/aluminum processing
5,317,187	Ti/TiN/Ti contact metallization
5,244,831	Method of doping a polysilicon layer on a semiconductor wafer
5,240,880	Ti/TiN/Ti contact metallization
4,895,520	Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant
4,824,803	Multilayer metallization method for integrated circuits

PROFESSIONAL MEMBERSHIPS

• National Science Foundation, Electronics & Nanotechnology Phase I & II SBIR Reviewer •
• Gerson, Lehrman Group: Leader (Top 5%) Council member •
• Chair Emeritus, and Founding Member, IEEE San Francisco Bay Area Nanotechnology Council •
• IEEE National Chapter of the Year Award, 2013 •
• Executive Committee Member, IEEE Santa Clara Valley Section •
• Member, Silicon Valley Engineering Council Steering Committee •
• Senior Member, IEEE •
• Member, Sigma Xi •
• Member, New York Academy of Science •
• Chair, Vistage International 2010-2015 •
• Security Clearance: Secret •

SEMINARS, TUTORIALS & WORKSHOPS

• ESD Association Tutorial: "Prevention of Electrostatic Discharge to Electronic Devices, Assemblies, and Systems." 1998 •
• Juran Institute, "Juran Management Systems," 1989 •

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SOFTWARE

DESIGN TOOLS:

SYNOPSYS: GALAXY DESIGN PLATFORM: DESIGN COMPILER, CUSTOM DESIGNER SE/DE/SDL, PRIMETIME, IC COMPILER, HSPICE, IC VALIDATOR, POWER COMPILER

CADENCE: AMS DESIGNER, ASSURA, SPECTRE, VIRTUOSO

MENTOR GRAPHICS: CALIBRE

TCAD:

SILVACO: ATHENA, ATLAS**,** VICTORY

OTHER TOOLS: VHDL, PYTHON, JSON, JMP, MATLAB, MICROSOFT OFFICE SUITE