

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

Case IPR2024-01404
Patent No. 9,147,609

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

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I. Introduction

The '609 patent invented nothing new. Prior art already disclosed a through substrate via (TSV) including an intentionally formed void to help reduce the thermal stress on the surrounding substrate. The prior art renders all challenged claims unpatentable.

HID primarily argues that not all voids reduce thermal stress in the substrate surrounding the TSV, and that therefore the prior art's disclosure of a void is insufficient to invalidate the challenged claims. But HID's evidence confirms that voids in TSVs reduce substrate thermal stress.

HID's remaining arguments are based on (1) mischaracterizations of the prior art, (2) mischaracterizations of case law, and (3) distinctions based on unclaimed features. The Board should reject these arguments and cancel all challenged claims.

II. There is No Material Dispute Over Level of Ordinary Skill in the Art.

HID argues that a person of ordinary skill in the art ("POSITA") would hold only a bachelor's degree, rather than the master's degree identified in the Petition. *Compare* Paper 17 (POR), §IV, *with* Paper 1 (Pet.), §IV. But HID's proffered variation is immaterial. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Both parties agree that a POSITA would have at least two years of experience in semiconductor design and fabrication, and HID's POR identifies no

analysis that would turn on whether a POSITA held a bachelor's or master's degree. *See* POR §§IV-VII.

III. HID's Arguments Against TSV Voids Reducing Thermal Stress in the Surrounding Substrate Fail in the Face of the Evidence.

HID cites *Birner* (Ex-1022) and *Kinoshita* (Ex-2008) and argues that “not all voids or all hollow centers in through-silicon vias decrease thermal stress.”

POR, 23; *see also* POR, 9. But neither reference supports this assertion.

A. A POSITA would not have understood *Birner* as disclosing that only some voids reduce thermal stress.

According to HID, a “POSITA would have understood from [*Birner*] that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur.” POR, 11, 24. But *Birner* does not support HID's position, which is premised on taking certain statements in *Birner* out of context.

Birner discloses multiple embodiments. After explaining that “[m]etals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material,” *Birner* discloses that “[i]n various embodiments, [its] invention . . . reduc[es] stress around the through substrate via by filling the through substrate via with an effective material with minimal thermal expansion.” *Birner*, ¶¶23-24. *Birner* continues, explaining that “[i]n various embodiments, the effective material comprises a combination of metal and voids,” which “produces an effective material with a coefficient of

expansion [CTE] comparable to the substrate.” *Birner*, ¶24. A POSITA would have understood the stress in *Birner*’s substrate is reduced because the metal-void combination (regardless of void size or shape) reduces the CTE mismatch between the metal-void combination and the substrate. Thompson-Supp (Ex-1025), ¶¶6-9.

Disregarding these embodiments, HID first cites *Birner*’s disclosure that “the size and shape of the tailored void 90 is adjusted to form a through substrate via with *minimum defectivity* arising from thermal or other stress related defects.” POR, 10. A POSITA would have understood “defectivity” as referring to manufacturing defects. Thompson-Supp, ¶10; *Birner*, ¶¶22, 37-38. Furthermore, “minimum” means “the least quantity assignable, admissible, or possible” (Ex-1026, 3). Thompson-Supp, ¶11. Thus, a POSITA would have understood *Birner*’s disclosure to mean adjusting void shape and size to achieve the lowest number of manufacturing defects in *Birner*’s TSV. *Birner*, however, does not suggest that voids of other shapes and sizes would not reduce the number of manufacturing defects. Thompson-Supp, ¶11.

HID also argues that *Birner* discloses “how to select the size and shape of the fill material in order to create a void that reduces thermal stress.” POR, 10-11, 23-24. HID again disregards the multiple embodiments of *Birner* discussed above. *Birner* only discloses that “[i]n one embodiment, [the] effective material comprises a void tailored to specific dimensions and shape.” *Birner*, ¶24 (emphasis added).

Regarding dimensions, *Birner* defines fill fraction f_{FM} as “a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} ,” which may be determined as α_{Si}/α_{FM} , α_{Si} and α_{FM} being CTEs of silicon and fill material respectively. *Birner*, ¶38. As an example, *Birner* discloses a “partial fill that covers about 15% of the sidewall of the trench *minimizes* the stress from thermal expansion.” *Birner*, ¶38 (emphasis added). But the term “minimize” in this disclosure does not suggest that only voids having sizes based on the ratio α_{Si}/α_{FM} can reduce thermal stress. Thompson-Supp, ¶12.

“Minimize” means to “reduce or keep to a minimum” (Ex-1026, 3), “minimum” means “the least quantity assignable, admissible, or possible” (Ex-1026, 3), and “reduce” means “to diminish in size, amount, extent, or number” (Ex-1026, 4). Thompson-Supp, ¶13. A POSITA would therefore understand from *Birner* that selecting a void size based on the ratio α_{Si}/α_{FM} may diminish the stress in the substrate to a lowest possible value. Thompson-Supp, ¶13. Nothing in *Birner*, however, discloses or suggests that void sizes not based on the ratio α_{Si}/α_{FM} , do not reduce the thermal stress, even though such reduction may not be to the lowest possible value. Thompson-Supp, ¶13. Rather, as discussed, *Birner* discloses that in various embodiments, voids (without specifying any size or shape) form an effective material that reduces stress in the substrate. *Birner*, ¶24;

Thompson-Supp, ¶13. Thus, a POSITA would not have understood *Birner* as disclosing that only some voids reduce thermal stress. Thompson-Supp, ¶14.

B. *Kinoshita* does not disclose that a void can increase the thermal stress in the substrate.

HID cites *Kinoshita* asserting “under operational conditions the presence of a void can increase thermal stresses inside the TSV, which could in turn increase thermal stresses in the silicon substrate.” POR, 11-13, 24-26. This is incorrect.

Initially, Petitioner notes *Kinoshita* published more than two years after the '609 patent, is not prior art, and a POSITA would not have been aware of it before the '609 patent priority date.

Even assuming *Kinoshita* were available to a POSITA before the '609 patent priority date, which it was not, a POSITA would have concluded that *Kinoshita* contradicts HID's position. Thompson-Supp, ¶15. Specifically, *Kinoshita* does not disclose that a TSV void increases the thermal stress on the surrounding substrate as HID suggests. Thompson-Supp, ¶15.

HID cites *Kinoshita*, Fig. 5, asserting: “the ‘with void’ TSV structure in *Kinoshita* exhibits higher stress levels along the edges of the TSV as compared to the non-voided TSV.” POR, 26. Even if true, HID's argument is irrelevant because claim 1 of the '609 patent recites “hollow center to reduce thermal **stress in** said **semiconductor substrate**” (Ex-1001, 6:4-10, emphasis added), not stress in the

TSV. Thus, the TSV stress levels in *Kinoshita* are irrelevant to determining whether the void in *Kinoshita*'s TSV decreases stress in the surrounding substrate. Thompson-Supp, ¶16.

HID claims the TSV's higher stress is "transferred directly to the substrate," but offers no supporting evidence. POR, 26. Additionally, HID neglects evidence from *Kinoshita*, which directly contradicts this assertion. For instance, annotated *Kinoshita*, Fig. 7, excerpted below, demonstrates the stress levels present in the substrate during device operation—conditions identical to those in *Kinoshita*, Fig. 5, which HID referenced. Thompson-Supp, ¶¶17-18.

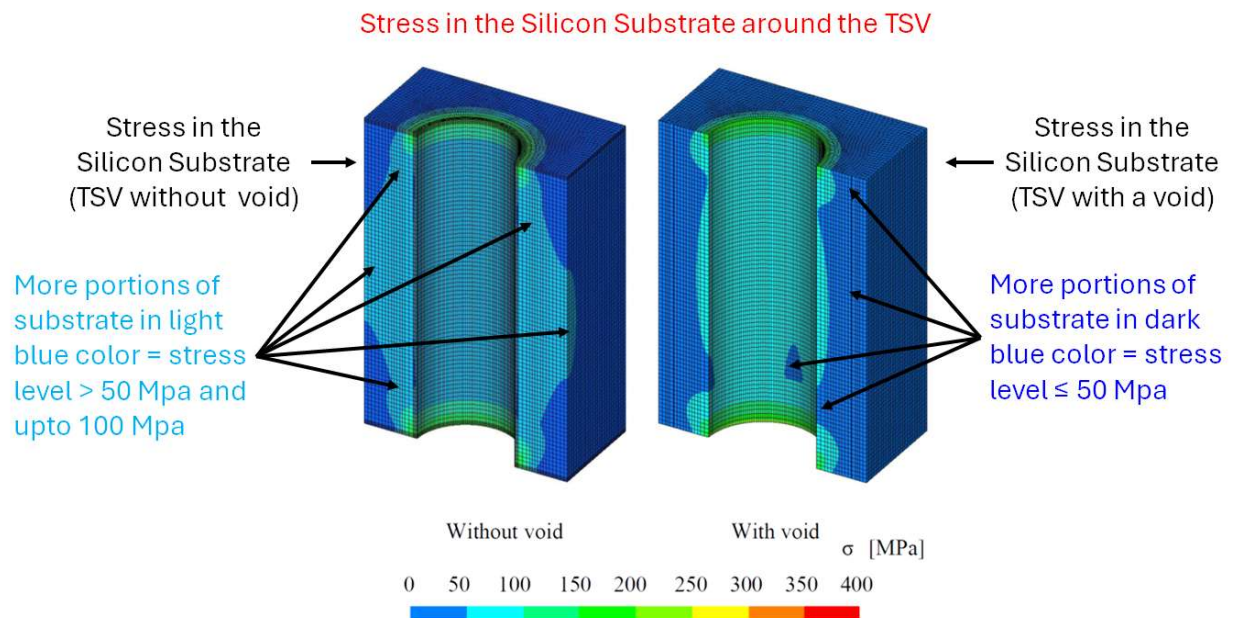


Fig. 7. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of device operation

A POSITA would understand from the above figure that dark blue color represents stress levels below 50 MPa, whereas the light blue color represents

stress levels greater than 50 MPa and up to 100 MPa. Thompson-Supp, ¶19. In the figure on the right (TSV with void), a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa, as compared to the figure on the left (TSV without void). Thompson-Supp, ¶20. Conversely, the figure on the left (without void) depicts a larger portion of the substrate in light blue, representing stress levels up to 100 MPa. Thompson-Supp, ¶20. Thus, *Kinoshita*, Fig. 7 shows that the substrate stress level is lower (more dark blue portions) when the TSV includes a void than when it does not. Thompson-Supp, ¶20.

Rather than examining the full scope of *Kinoshita*, HID cites a single sentence in *Kinoshita* that “[i]n the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa” (*Kinoshita*, 3), and concludes that the a TSV void does not reduce the stress on the substrate. POR, 26. But *Kinoshita* does not indicate where on the inner surface of the substrate the 100 MPa value was determined, nor clarify whether the 100 MPa value represents an average, minimum, or maximum value. Thompson-Supp, ¶21. In contrast, Fig. 7 illustrates that while some portions of the substrate can reach stress levels near 100 MPa, overall stress in the substrate is lower—indicated by more dark blue—when a TSV void is present than when it is absent. Thompson-Supp, ¶21.

As another example, annotated *Kinoshita* Fig. 8, excerpted below, demonstrates the substrate stress levels during a reflow process, at a higher temperature than the device operation conditions of *Kinoshita* Fig. 5.

Thompson-Supp, ¶22.

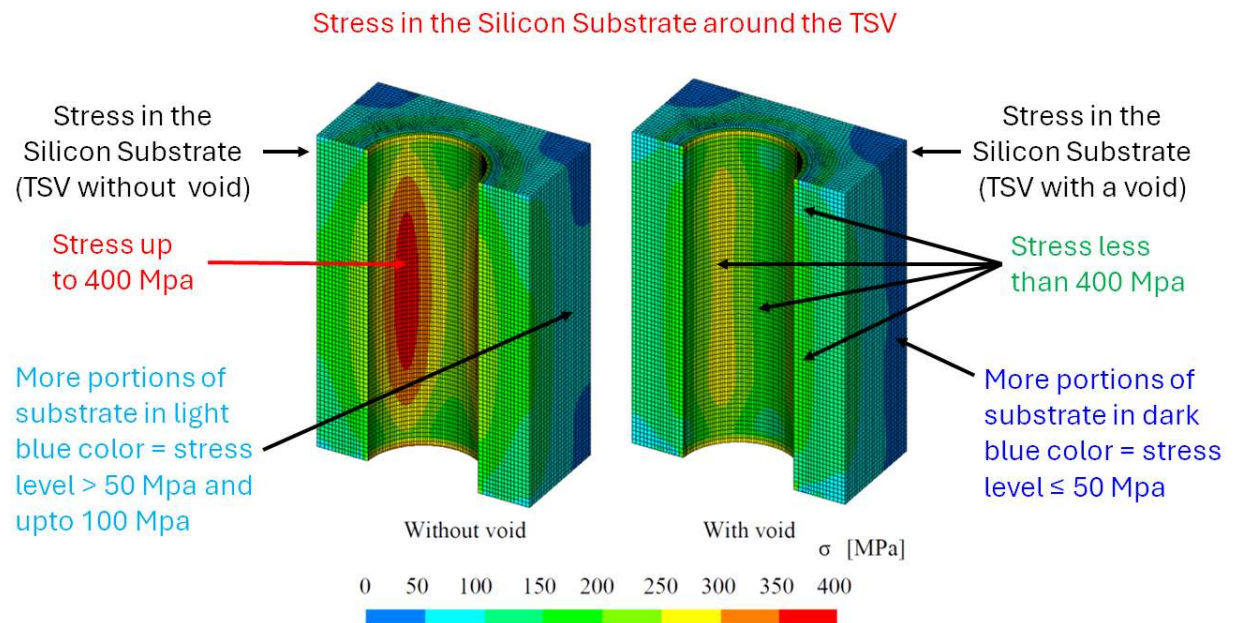


Fig. 8. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of reflow process

As illustrated in the figure on the right above (TSV with void), the stress on the inner surface of the substrate surrounding the void is about 200-250 MPa (significantly lower than 400 MPa), whereas the stress on the same surface in the figure on the left above (TSV without void) is up to 400 MPa. Thompson-Supp, ¶¶23-24. Furthermore, a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa in the figure on the right above (TSV with void), as compared to the figure on the left (TSV without void). Thompson-Supp,

¶24. Thus, *Kinoshita*, Fig. 8 provides additional evidence that the substrate stress level is lower when the TSV includes a void than when it does not.

Thompson-Supp, ¶24.

Kinoshita does not show that a TSV void increases thermal stress in the surrounding substrate. And HID's arguments against TSV voids reducing thermal stress in the surrounding substrate fail in the face of the evidence. Thompson-Supp, ¶25.

IV. HID's Proposed Claim Constructions Do Not Demonstrate That Functional Limitations in the Challenged Claims are entitled to Patentable Weight.

Under the guise of claim construction, HID argues that the functional limitations in the challenged claims are not statements of intended use. POR, 8, 9. The Board should reject HID's arguments for the following reasons.

A. "to reduce thermal stress in said semiconductor substrate"

HID proposes this limitation "should be construed to require the hollow center to cause reduction in thermal stress." POR, 15. HID concedes, however, "[t]he claim language in the '609 Patent is *intended to convey the purpose* of the hollow center: to reduce thermal stress in the substrate." POR, 13. Petitioner agrees. Because this functional limitation recites the intended use or purpose of the hollow center, it should not be entitled to any patentable weight.

Regardless, HID argues that this limitation should be afforded patentable weight because “[n]ot all hollow centers and not all configurations of vias reduce thermal stress in all semiconductor substrates.” POR, 9-13 (citing *Birner* and *Kinoshita*). As explained, however, HID’s evidence does not call into question that all voids reduce thermal stress in the substrate. Section III.

As Dr. Thompson testified, “[a] void that’s buried obviously reduces stress as the tungsten expand[s] and squashes – squashes the void and expands inward into the void.” Ex-2007, 30:25-31:11. Dr. Thompson’s opinion is consistent with *Birner*, *Pogge*, *Edelstein*, and *Kinoshita*, and HID’s admission that the patent’s “hollow center ‘reduces thermal and mechanical stress in substrate 412 by providing space for conductive filler 430 to expand inward rather than outward in high temperature conditions.’” POR, 13-14 (citing ’609 patent, 4:60-67).

Accordingly, the Board should afford no patentable weight to the limitation “to reduce thermal stress in said semiconductor substrate,” because it was well known that TSV voids perform this function and because this limitation merely recites the purpose or intended use of the claimed “hollow center.” Ex-1002, ¶¶48-49, 125-131.

HID advances several case law arguments, none of which are tenable. HID first cites *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1363–64 (Fed. Cir. 1999), asserting that “[f]unctional language generally limits the claim to a structure when

the functional language describes something about the structure of the apparatus rather than merely listing its intended or preferred uses.” POR, 13. But, *K-2 Corp.* does not so hold. In *K-2 Corp.*, Appellant argued the “claim term ‘for substantially preventing movement therebetween at least in a horizontal plane’ dictates the meaning of ‘permanently affixed’ to mean that it prevents movement in a horizontal plane.” *K-2 Corp.*, 191 F.3d at 1363; POR, 13. The court disagreed, stating: “We cannot accept this reading of the claim.” *K-2 Corp.*, 191 F.3d at 1363.

Even assuming HID’s assertion were correct, the limitation “hollow center to reduce thermal stress in said semiconductor substrate” says nothing about the structure of the hollow center. For example, this limitation provides no information regarding the shape, size, or location of the hollow center that would result in reduction of thermal stress. Ex-1002, ¶123. Nor does the ’609 patent. Instead, the limitation simply states the hollow center’s intended use or purpose. Accordingly, this limitation should be afforded no patentable weight because “apparatus claims cover what a device is, not what a device does.” *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, (Fed. Cir. 1990); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

HID next asserts that “[t]he hollow center portion in Claim 1 must therefore be sufficient to reduce thermal stress in the semiconductor substrate, or it will not be the claimed ‘hollow center.’” POR, 14. HID bases this on the holding in

Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc., 381 F.3d 1111, 1117–20 (Fed. Cir. 2004) that the functional relationship “operatively connected” means that the claimed components must be “connected in a way to perform a designated function.” POR, 14. *Innova* is inapposite.

Unlike *Innova*, in claim 1 of the ’609 patent, the phrase “to reduce thermal stress in said semiconductor substrate” does not describe a functional relationship between two or more claimed components. Rather, it describes the intended use of a single component—“the hollow center.” Thus, *Innova* is inapplicable. Even if it were not, *Pogge*, *Edelstein*, *Birner*, and *Kinoshita* all demonstrate the well-known thermal stress relieving behavior of a TSV void. Pet., 21; Section III.B.

HID’s criticism of Petitioner’s case law is also unwarranted. HID asserts that “the court in *Atlas Powder*, 190 F.3d at 1346, did not hold that all air increased sensitivity.” POR, 15, n1. HID therefore concludes that Petitioner’s evidence that voids reduce thermal stress in the substrate is insufficient. POR, 14-15. HID’s distinction is wrong for two reasons. First, contrary to HID’s assertion, in *Atlas Powder*, the court concluded that air from any source did increase sensitivity, noting “the inventor of the patents in suit, testified that air from any source would contribute to the explosion of a heavy ANFO composition and, particularly, air trapped within the pores of porous prilled AN.” *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342, 1348 (Fed. Cir. 1999). Second, like *Atlas Powder*, there is ample

evidence here that TSV voids reduce thermal stress in the surrounding substrate.

See, e.g., Pogge, Edelstein, Birner, Kinoshita. Nothing more is required.

HID attempts to distinguish *In re Sinex*, 309 F.2d 488, 492 (C.C.P.A. 1962), and *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019), arguing that these cases only apply to claim preambles reciting functional language. POR, 15. This is incorrect. For example, the *Arctic Cat* court made clear that functional language is not entitled to patentable weight even when it is present in a claim limitation instead of in the preamble. Specifically, the *Arctic Cat* court relied on “the statutory distinction, in identifying the permissible subject matter of a patent claim, between a physical product (which may be defined in part by its claimed functional capabilities) and activities that constitute a process (which may include a new ‘use’ of a known invention).” *Arctic Cat*, 919 F.3d at 1328. The court noted the “well settled” fundamental principle “that the recitation of a new intended use for an old product does not make a claim to that old product patentable.” *Id.*

Thus, HID’s case law arguments lack merit. The Board should not afford any patentable weight to the limitation “to reduce thermal stress in said semiconductor substrate.”

**B. “to provide space for said conductive filler to expand inward,”
and “to prevent contamination during processing of said
semiconductor substrate”**

HID presents no new arguments regarding these limitations, stating only that “[t]he remaining functional limitations should be given patentable weight for the same reasons.” POR, 16. HID’s references to *Birner* and *Kinoshita* do not show these limitations are more than statements of intended use. For the reasons in Section IV.A, the Board should not give patentable weight to these limitations.

V. HID’s Arguments Against Anticipation by *Cooney* Lack Merit and Should Be Rejected.

HID asserts “it is improper in an anticipation ground to use the knowledge of a person of skill in the art to fit prior art that is missing limitations into the claim language.” POR, 21. Petitioner did not rely on Dr. Thompson’s opinion to provide a missing limitation. Rather, Petitioner cited Dr. Thompson to show what a POSITA would have understood from *Cooney*’s disclosure of a void. *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) (holding that expert opinion “may be used to interpret [an] allegedly anticipating reference and to shed light on what it would have meant to” a POSITA); *see also Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001). Specifically, Petitioner relied on Dr. Thompson’s opinion that “a POSITA would have understood that void 25 in *Cooney*’s TSV would also

reduce thermal stress in Cooney's substrate" just like the voids in *Pogge*, *Edelstein*, and *Birner*. Ex-1002, ¶123.

HID also asserts that "Petitioner and Dr. Thompson rely on a foundational assumption that all voids in all TSVs reduce thermal stress in the substrate, and this assumption is flatly contradicted by extrinsic evidence." POR, 22. But HID's extrinsic evidence (*Birner* and *Kinoshita*) failed to disprove the well-known thermal stress relieving behavior of TSV voids. Section III. Therefore, the Board should find that *Cooney* anticipates claim 1 for two reasons: (1) because *Cooney* discloses the structure recited in claim 1 and the limitation "to reduce thermal stress in said semiconductor substrate" should not be entitled to any patentable weight, and (2) because it was well known in the art that a void as disclosed by *Cooney* would reduce thermal stress in the substrate. Thompson-Supp, ¶¶26-27.

A. The Board should reject HID's purported distinction between a "void" and the "hollow center."

HID does not provide a construction for the claimed "hollow center" but states that "[a] 'void' is different from a hollow center." POR, 22, 31. HID also asserts that *Cooney*'s use of the term "void" implies "a very small imperfection" similar to a pinhole type of defect in a TSV. POR, 27 (citing *Kong* as purportedly showing voids smaller than 4-5 μm). However, the claims of the '609 patent do not limit the size of the hollow center. Moreover, Petitioner's prior art and HID's own

evidence debunk HID's purported distinction by showing that the term void is not limited to dimensions smaller than 4-5 μm and that voids do reduce thermal stress in the substrate. Thompson-Supp, ¶¶28-29.

For example, as Dr. Thompson explains, *Birner* discloses a void diameter of 3.5 μm for a TSV diameter of 5 μm , and a void diameter of 10.5 μm for a TSV diameter of 15 μm . Thompson-Supp, ¶29 (citing *Birner*, ¶¶29, 38 disclosing TSV diameters of 5-15 μm and a fill fraction of 30%). Likewise, *Kinoshita* discloses its void's minor axis (i.e., void diameter) is 12 μm . *Kinoshita*, 2. Thompson-Supp, ¶30. These void diameters are significantly larger than HID's alleged pinholes and no different than the claimed "hollow center." Thompson-Supp, ¶¶29-30. And, as discussed in Section III, the TSV voids in both *Birner* and *Kinoshita* reduce thermal stress in the surrounding substrate. Thompson-Supp, ¶30.

Although not required by the claims, a POSITA would have determined the void size in *Cooney* can be about 14 μm based on the dimensions disclosed in *Cooney*. Thompson-Supp, ¶31 (citing *Cooney*, ¶¶51, 54). Indeed, Dr. Thompson testified that "Cooney's void is a typical void" similar to the voids disclosed by *Birner* and *Kinoshita*. Ex. 2007, 30:8-14. Thus, *Cooney*'s void would also reduce thermal stress in the substrate like the voids of *Birner* and *Kinoshita*. Thompson-Supp, ¶31.

Accordingly, HID cannot distinguish *Cooney*'s void from the claimed "hollow center." Thompson-Supp, ¶32.

B. HID's arguments regarding the shape of *Cooney*'s TSV are irrelevant and should be disregarded.

HID cites Mr. Berg, asserting "the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV." POR, 29. But Mr. Berg provides no analysis or evidence to support this conclusion. Ex-2012, ¶71. The Board should disregard such unsupported expert testimony. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Upjohn Co. v. Mova Pharm. Corp.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000) ("Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity determination.").

Moreover, claim 1 of the '609 patent recites a "hollow center to reduce the thermal stress in the substrate," and does not require a straight TSV. Thus, the question is whether *Cooney*'s torpedo-shaped TSV with the optional void results in lower thermal stress in the substrate, compared to the same torpedo-shaped TSV without the void, not whether *Cooney*'s TSV reduces thermal stress relative to a straight TSV. Thompson-Supp, ¶¶33-34. It does. Ex-1002, ¶¶47-49, 125-131, 141-145 (citing, *Birner, Pogge, Edelstein, Tsui*). The '609 patent itself makes clear that

it is the hollow center 432 that reduces thermal stress “by providing space for conductive filler 430 to expand inward,” not the straight shape of TSV. ’609 patent, 4:62-66. Neither HID nor its expert provide any explanation regarding the relevance of the TSV shape in determining whether *Cooney*’s void decreases the thermal stress in *Cooney*’s substrate. POR, 28-29.

C. HID’s arguments regarding the size and desirability of *Cooney*’s TSV are also irrelevant and should be disregarded.

HID states “Petitioner’s analysis of the Figures in *Cooney* also fails because it interprets dimensionality from an exemplary figure” but contradicts itself stating the “Petition makes no attempt to analyze the size of the optional void in relation to the size or shape of the torpedo shaped via, and therefore an attempt to interpret this size from the Figures is improper.” POR. 30. HID’s contention is irrelevant. Moreover, as explained above and by Dr. Thompson, *Cooney*’s disclosure itself makes clear that voids in *Cooney* may have diameters of 14 μm . Thompson-Supp, ¶31.

Citing its expert, HID further argues “[r]ather than desirable features, voids are typically to be avoided.” POR, 30. But the prior art contradicts this assertion. For example, *Birner* explains that its invention reduces stress around the TSV by filling the TSV with an effective material that “comprises a combination of metal

and voids.” *Birner*, ¶24; Section III.A. Thus, *Birner* discloses purposefully including voids in the TSV. Thompson-Supp, ¶35.

Similarly, *Pogge* discloses that with a via structure, “a conducting path is established between the bottom of the trench and the top surface of the wafer, while a void 25 remains near the bottom of the trench” and that “the void 25 has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature.” *Pogge*, ¶27, claim 3 (“A method according to claim 1, wherein said depositing step further comprises depositing metal so as to form a void in the feature.”). Thompson-Supp, ¶36.

Edelstein likewise discloses “a substrate 224 in which the through-via comprises an annular ring of insulating material 223 within which is disposed a conductive via of metal (e.g., copper) 225 having a void 220 at its core.” *Edelstein*, ¶47. *Edelstein* further explains that “[c]are must be taken at both the top and bottom surfaces to leave metal across the entire via surface in order to preserve the void within.” *Edelstein*, ¶48. Like *Birner*, both *Pogge* and *Edelstein* disclose intentionally forming voids within a TSV. Thus, a POSITA would have understood that instead of avoiding voids, deliberately forming voids in TSVs helps mitigate thermal stress in the substrate. Thompson-Supp, ¶37.

HID further asserts that “[v]oids, as typically understood by the POSITA, are not large enough to have any appreciable impact on the reduction of thermal stress in the semiconductor substrate. POR, 30-31. The ’609 patent and the challenged claims do not specify the hollow center’s size or shape. Prior art also contradicts HID’s position. As noted, *Birner*, *Pogge*, and *Edelstein* all show that voids are intentionally formed to reduce thermal stresses. Even HID’s own reference, *Kinoshita*, discloses that a TSV void lowers thermal stress on the substrate. Section III.B; Thompson-Supp, ¶38.

VI. HID’s Arguments Against Obviousness Over Cooney Lack Merit and Should Be Rejected.

HID incorrectly argues that “[n]either *Pogge* nor *Edelstein* disclose[s] that voids reduce thermal stresses in the semiconductor substrate.” POR, 31.

A. HID’s contention that *Pogge* does not disclose reduction of thermal stress in the substrate is wrong.

According to HID, although *Pogge* discloses that “the void ‘has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE),” *Pogge* “does not mention or state that the stresses would be borne by the semiconductor substrate.” POR, 32. But a POSITA does not rely solely on the text in a single reference to understand its disclosure, but also relies on the POSITA’s knowledge of the state of the art. *Standard Oil Co. v. Am.*

Cyanamid Co., 774 F.2d 448, 454 (Fed. Cir. 1985) (A POSITA “is presumed to be aware of all the pertinent prior art.”)

While Dr. Thompson provided *Pogge* and *Edelstein* as examples (Ex-1002, ¶¶125-131), he also cited *West* and *Birner* (Ex-1002, ¶¶47-49). Dr. Thompson noted *West*’s disclosure that “[c]opper, as well as some other TSV filler materials, have a significantly higher coefficient of thermal expansion (CTE) as compared to conventional IC substrates, such as silicon” and that “[t]his CTE mismatch (Δ CTE) can result in significant thermally induced stress in the silicon including the circuitry (e.g. MOS transistors) in the silicon surrounding the TSVs.” Ex-1002, ¶47 (citing *West*, ¶5). Dr. Thompson also cited *Birner*, which states: “Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material” of the TSV. *Birner*, ¶23, Ex-1002, ¶49. Further, Dr. Thompson noted that by including voids in the TSV, *Birner* discloses reducing the CTE mismatch. Ex-1002, ¶49. Thus, Dr. Thompson presented ample evidence regarding the state of the art indicating that a CTE mismatch causes thermal stress in the substrate and further that reducing the CTE mismatch reduces the thermal stress in the substrate. *See also* Ex-2007, 26:16-18 (“[A] combination of changing temperature and having different CTEs causes stress in the integrated circuits.”).

In view of the knowledge of the state of the art that voids in the TSV reduce the CTE mismatch between the TSV and the surrounding substrate and consequently reduce the stress induced in the substrate, a POSITA would have understood *Pogge*'s disclosure of the stress relieving function of its void as including relieving stresses in the substrate. To suggest otherwise would require a POSITA to ignore their knowledge of the state of the art, which is counter to the very definition of a POSITA. *Standard Oil*, 774 F.2d at 454.

A POSITA reading *Pogge* would have understood that CTE differences would cause different amounts of expansion in *Pogge*'s TSV and the substrate. Thompson-Supp, ¶¶39-41; *Birner*, ¶23. A POSITA would have further understood that such differences in thermal expansion would induce stress in both the TSV and in the substrate around the TSV. Thompson-Supp, ¶41; *Birner*, ¶23; *West*, ¶5. And a POSITA would have understood that by reducing the difference in the CTE, the stresses induced in the substrate would be lower. Thompson-Supp, 41. Thus, a POSITA would have understood *Pogge* as disclosing relieving stress in the semiconductor substrate. Thompson-Supp, 41.

B. HID's contention that *Edelstein* only discloses mechanical stress and not thermal stress is similarly wrong.

HID argues that “*Edelstein*'s discussion is entirely centered around removing mechanical stresses, not thermal stresses.” POR, 32-33. A POSITA

would have understood that thermal stress is mechanical stress caused due to thermal expansion. Thompson-Supp, ¶42 (citing *Timoshenko* (Ex-1027), 18, 40). A POSITA would have also understood that the Poisson's ratio and modulus determine the thermal stress generated as a result of the thermal expansion. Thompson-Supp, ¶42 (citing *Timoshenko*, 66).

Furthermore, *Edelstein* discloses “provid[ing] a through-via structure including conductive material having a coefficient of thermal expansion which closely matches the substrate material, a reduced modulus and a reduced Poisson ratio in order to minimize the negative effects of thermal mismatch.” A POSITA would have understood *Edelstein* as disclosing that reducing the CTE mismatch between the conductive and substrate materials, and reducing the modulus and Poisson's ratio would reduce thermal stresses in the substrate. Thompson-Supp, ¶42 (citing *Timoshenko*, 66).

Even *Kinoshita*, cited by HID, equates thermal stresses with mechanical stresses, stating the effect of TSV voids on “*thermal stresses* in the TSV structure” are analyzed and that “*mechanical stresses in the Cu TSVs and in the Si chips* are obtained from the simulations.” *Kinoshita*, 2 (emphases added). Thus, the Board should reject HID's misplaced attempts to distinguish thermal stress from mechanical stress. Thompson-Supp, ¶44.

Next HID asserts that “*Edelstein* also never discloses the reduction of stress (whether mechanical or thermal) in the substrate itself.” POR, 33. This too is incorrect.

For example, *Edelstein* discloses “most metals which are commonly used for integrated circuit interconnect vias generate unacceptable stress levels *on the carrier layer material (e.g., Si or glass)* due to thermal expansion mismatch.” *Edelstein*, ¶8 (emphasis added). *Edelstein*’s carrier layer is the substrate surrounding *Edelstein*’s TSV. Thompson-Supp, ¶¶45-46. Additionally, *Edelstein* expressly discloses that the presence of a TSV void effectively reduces the CTE mismatch between the TSV and substrate materials, which also reduces the stress on the substrate. Thompson-Supp, ¶47. For example, *Edelstein* discloses providing “a through-via having an effective coefficient of thermal expansion which most closely matches that of the substrate,” thus minimizing the CTE mismatch. *Edelstein*, ¶¶14, 15, 19.

Edelstein also discloses that voids in a TSV “reduce[] the effective modulus and Poisson ratio of the through-via ... exert[ing] *much less stress* and force *on the surrounding structures*” and that the TSV “behaves on a whole as if it had a much smaller thermal expansion mismatch with the substrate.” *Edelstein*, ¶47 (emphasis added). Thus, *Edelstein* discloses that inclusion of a TSV void reduces the thermal

stress in the substrate surrounding the TSV because the TSV behaves as if it had a much smaller CTE mismatch with the substrate. Thompson-Supp, ¶¶47-48.

HID further argues that even if *Pogge* and *Edelstein* teach that thermal stresses are relieved by the voids in their respective devices, these references would not have taught a POSITA that all voids decrease thermal stress in all TSVs. POR, 32, 33. The Board should reject this argument because HID has failed to establish that all voids do not reduce thermal stress in the surrounding substrate. Section III; Thompson-Supp, ¶49.

HID also argues that thermal stress relieving behavior of voids was not well known. POR, 33-34. As discussed above, Petitioner and Dr. Thompson have provided ample evidence (e.g., *Pogge*, *Edelstein*, *Birner*) that establishes the well-known thermal stress relieving behavior of voids. Moreover, even *Kinoshita*, cited by HID, establishes the thermal stress relieving behavior of voids. Section III.B. Thus, a POSITA would have found it obvious to include a void in *Cooney*'s TSV to achieve these stress-relieving benefits. Thompson-Supp, ¶50; Ex-1002, ¶¶125-133. HID has presented no contrary evidence. And obviousness does not require that all voids decrease thermal stress in all TSVs, just that a POSITA would have been motivated to include voids in TSVs to decrease thermal stress with a reasonable expectation of success, which Petitioner has shown.

Accordingly, the Board should cancel claims 1-6, 9-14, 17, and 18 based on Grounds 1A and 1B.

VII. HID's Arguments Against Obviousness Based on Grounds 2-4 Fail.

HID does not contest that *Dean*, *Farooq*, and *Chen* disclose the additional features of claims 7, 8, 15, and 16 as shown in Petitioner's Grounds 2-4. Instead, HID relies on its arguments for *Cooney*. Because its arguments for *Cooney* fail (*see* Sections II-VI), the Board should cancel claims 7, 8, 15, and 16 based on Grounds 2-4.

VIII. Conclusion

For the reasons set forth above, and in the Petition, challenged claims 1-18 of the '609 patent are unpatentable and should be canceled.

Dated: September 19, 2025

By: / Joshua L. Goldberg /
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(c)(1), the undersigned hereby certifies that the foregoing Petitioner's Reply to Patent Owner's Response contains 5,537 words, excluding the parts exempted under 37 C.F.R. § 42.24(c) as measured by the word-processing system used to prepare this paper.

Dated: September 19, 2025

By: / Joshua L. Goldberg /
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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Petitioner's Reply to Patent Owner's Response** was served on September 19, 2025, via email directed to counsel of record for the Patent Owner at the following:

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