

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01404
U.S. Patent No. 9,147,609

**SUPPLEMENTAL DECLARATION OF SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 9,147,609**

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I. Introduction

1. I, Scott E. Thompson, Ph.D., provide the following supplemental declaration in connection with IPR2024-01404 concerning U.S. Patent No. 9,147,609 (“the ’609 patent”) (Ex. 1001).

2. I have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”). Previously, I submitted an opening declaration (Ex. 1003) in support of Samsung’s Petition for *Inter Partes* Review.

3. I submit this supplemental declaration in response to the Patent Owner’s Response (“POR”) (Paper 17) filed by Harbor Island Dynamic, LLC (“Patent Owner” or “HID”). I was asked to address certain arguments raised by HID’s POR, as well as certain testimony provided by HID’s expert, Mr. John Berg, in his declaration (Ex. 2012). My lack of direct response to other points or issues raised in the POR or by Mr. Berg’s declaration should not be construed as agreement or admission. Nothing in the POR or Mr. Berg’s declaration changes the opinions that I expressed in my opening declaration.

II. Materials Considered

4. In forming my opinions in this supplemental declaration, I have reviewed and considered the Board’s Institution Decision (Paper 9), HID’s POR, Mr. Berg’s declaration, and all of the materials cited therein. I have further relied

upon my experience, professional background, and knowledge of the relevant art, as detailed in my opening declaration and curriculum vitae. All of the foregoing are incorporated herein by reference. In addition, I have relied upon the materials considered in my opening declaration (Ex. 1002, §IV), as well as the documents directly cited to in this supplemental declaration.

III. Mr. Berg's Arguments Against TSV Voids Reducing Thermal Stress in the Surrounding Substrate Lack Merit

5. Mr. Berg cites *Birner* (Ex. 1022) and *Kinoshita* (Ex. 2008) and argues that “[a]ll voids do not decrease thermal stress.” Ex. 2012, ¶¶ 47-54, 63-67. I disagree because neither reference supports this assertion.

A. A POSITA would not have understood *Birner* as disclosing that only some voids reduce thermal stress.

6. According to Mr. Berg, a “POSITA would have understood from [*Birner*] that while a void *can* reduce thermal stress, it must be designed in a particular manner in order for that to occur.” Ex. 2012, ¶¶ 49, 63. But *Birner* does not support Mr. Berg’s position, which is premised on taking certain statements in *Birner* out of context.

7. *Birner* discloses multiple embodiments. Particularly, *Birner* discloses: “Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material.” *Birner*, ¶ 23. *Birner* discloses that “[i]n various embodiments, [its] invention . . . reduc[es] stress

around the through substrate via by filling the through substrate via with an effective material with minimal thermal expansion.” *Birner*, ¶ 24. *Birner* goes on to explain that “[i]n various embodiments, the effective material comprises a combination of metal and voids,” which “produces an effective material with a coefficient of expansion comparable to the substrate.” *Birner*, ¶ 24. In my opinion, one skilled in the art would have understood *Birner* as disclosing numerous embodiments in which the coefficient of thermal expansion (CTE) of the effective material, including metal and voids, would have a value lower than the CTE of the metal alone and higher than the CTE of the material in the voids. In my opinion, a skilled artisan would have also understood this would be true regardless of the number or size of the voids in the metal because *Birner* does not disclose or suggest a particular number or size of voids required to achieve this effect.

8. Because *Birner* discloses that the CTE of the silicon surrounding *Birner*’s TSV is smaller than that of the metal filled in the TSV, in my opinion, one skilled in the art would have understood from *Birner*’s disclosure that the difference between the CTE of the metal-void combination and silicon would also be smaller than the difference between the CTE of the metal alone relative to silicon. As a result, one skilled in the art would have understood from *Birner* that the CTE of the metal-void combination would be closer to or similar to the CTE of the silicon substrate material surrounding the metal-void combination.

9. *Birner* discloses that the CTE mismatch between materials induces stress in the silicon substrate. For example, *Birner* discloses: “Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material.” *Birner*, ¶ 23. Therefore, because the mismatch in the CTE between the metal-void combination and the silicon substrate is smaller, in my opinion a skilled artisan would have understood from *Birner*’s disclosure that the stress in *Birner*’s substrate would also be reduced. And because the mismatch in CTE is lowered regardless of the number, size, or shape of voids, a skilled artisan would have understood that the stress in *Birner*’s substrate would be reduced regardless of void number, size, or shape.

10. Disregarding these embodiments, Mr. Berg cites *Birner*’s disclosure that “the size and shape of the tailored void 90 is adjusted to form a through substrate via with *minimum defectivity* arising from thermal or other stress related defects.” Ex. 2012, ¶ 49 (citing *Birner*, ¶ 37). In my opinion, this portion of *Birner* focuses on manufacturing defects arising from thermal or other stresses. In particular, in my opinion, one skilled in the art would have understood the term “defectivity” disclosed in this portion of *Birner* as referring to manufacturing defects. For example, *Birner* discloses that one of the key problems associated with stacking silicon devices “arises from yield loss arising from stress induced failure of the product.” *Birner*, ¶ 22. *Birner* explains that “manufacturability is a key

concern.” *Birner*, ¶ 38. Thus, one skilled in the art would have understood *Birner*’s disclosure of “*minimum defectivity* arising from thermal or other stress related defects” to mean minimizing of manufacturing defects that may be caused due to thermal or other stresses. *Birner*, ¶ 37 (emphasis added).

11. The term “minimum” means “the least quantity assignable, admissible, or possible.” Ex. 1026, 3. In my opinion, therefore, one skilled in the art would have understood the phrase “minimum defectivity” to mean a least or smallest possible number of defects. More particularly, a skilled artisan would have understood *Birner*’s ¶ 37 disclosure to mean adjusting void shape and size to achieve the smallest possible number of manufacturing defects in *Birner*’s through substrate via (TSV). A skilled artisan would have also understood that nothing in *Birner* suggests that voids of other shapes and sizes would not also reduce manufacturing defects. Rather, the skilled artisan would have understood from *Birner* that while voids of other shapes and sizes would have reduced manufacturing defects, the resulting number of manufacturing defects might not be the smallest possible number of manufacturing defects.

12. Mr. Berg also argues that *Birner* discloses “how to select the size and shape of the fill material in order to create a void that reduces thermal stress.” Ex. 2012, ¶¶ 49, 63. In my opinion, Mr. Berg again disregards the multiple embodiments of *Birner* that I discussed above. *Birner* only discloses that “[i]n one

embodiment, [the] effective material comprises a void tailored to specific dimensions and shape.” *Birner*, ¶ 24 (emphasis added). Regarding dimensions, *Birner* defines fill fraction f_{FM} as “a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} .” *Birner*, ¶ 38. *Birner* explains that this fill fraction f_{FM} may be determined as the ratio $\alpha_{Si} / \alpha_{FM}$, where α_{Si} and α_{FM} are the CTEs of silicon and the fill material respectively. *Birner*, ¶ 38. *Birner* provides an example in which the fill material is copper and the fill fraction f_{FM} is about 30%. *Birner*, ¶ 38. *Birner* explains a “partial fill that covers about 15% of the sidewall of the trench *minimizes* the stress from thermal expansion.” *Birner*, ¶ 38 (emphasis added). However, as I explain below, a skilled artisan would not have understood the term “minimizes” in this disclosure as suggesting that only voids having sizes based on the ratio $\alpha_{Si} / \alpha_{FM}$ can reduce thermal stress.

13. The term “minimize” means “to reduce or keep to a minimum.” Ex. 1026, 3. As I explained, the term “minimum” means “the least quantity assignable, admissible, or possible.” Ex. 1026, 3. Further, the term “reduce” means “to diminish in size, amount, extent, or number.” Ex. 1026, 4. Therefore, in my opinion, one skilled in the art would have understood from *Birner* that selecting a void size based on the ratio $\alpha_{Si} / \alpha_{FM}$ may result in diminishing the stress in the substrate to a lowest possible value. A skilled artisan would have understood, however, that nothing in *Birner* discloses or suggests that void sizes not based on

the ratio $\alpha_{Si} / \alpha_{FM}$, do not reduce the thermal stress. Rather, one skilled in the art would have understood that while voids of dimensions different from those based on the ratio $\alpha_{Si} / \alpha_{FM}$ would reduce the thermal stress in the substrate, such thermal stress reduction may not be to the lowest possible value. Indeed, as I discussed above, *Birner* discloses numerous embodiments, in which the presence of voids (without specifying any size or shape) in the metal filled in *Birner*'s TSV, reduces the CTE mismatch between the metal-void combination and the silicon substrate surrounding *Birner*'s TSV, and consequently reduces the stress in the substrate surrounding the TSV. *Birner*, ¶ 24.

14. To summarize, one skilled in the art would have understood *Birner* as disclosing that the metal-void combination (regardless of void size) reduces thermal stress in the substrate, though not necessarily to the lowest possible value. Furthermore, one skilled in the art would have understood from *Birner* that the void size could be selected based on the ratio $\alpha_{Si} / \alpha_{FM}$ to achieve the lowest possible value of stress in the substrate. However, a skilled artisan would not have interpreted *Birner* as disclosing or suggesting that a void must be designed in a particular manner to reduce the thermal stress in the substrate.

B. *Kinoshita* does not disclose that a void can increase the thermal stress in the substrate.

15. Mr. Berg cites *Kinoshita*, asserting “under operational conditions the presence of a void can increase thermal stresses inside the TSV, which could in

turn increase thermal stresses in the silicon substrate.” Ex. 1012, ¶¶ 49, 64. I disagree because *Kinoshita*’s disclosure contradicts Mr. Berg’s position. In particular, as I explain below, *Kinoshita* does not disclose that a void in a TSV increases the thermal stress on the surrounding substrate as Mr. Berg contends.

16. Mr. Berg relies on Figure 5 of *Kinoshita* and asserts that “the ‘with void’ TSV structure in *Kinoshita* exhibits higher stress levels than the non-voided TSV, including on the edge of the TSV.” Ex. 2012, ¶¶ 52, 67. In my opinion, Mr. Berg’s argument regarding the stress level in the TSV is irrelevant. This is because claim 1 of the ’609 patent recites “hollow center to reduce thermal **stress in said semiconductor substrate**” (Ex. 1001, 6:4-10, emphasis added); claim 1 does not recite stress in the TSV. Thus, Mr. Berg’s analysis of the stress levels in the TSV of *Kinoshita* is wholly irrelevant to determining whether the void in *Kinoshita*’s TSV decreases stress in the surrounding substrate.

17. Mr. Berg claims that the TSV’s higher stress is “transferred to the semiconductor substrate.” Ex. 2012, ¶¶ 52, 67. But Mr. Berg offers no evidence to support this conclusory statement. Ex. 2012, ¶¶ 52, 67. In particular, Mr. Berg does not identify anything in *Kinoshita* to suggest that the stress distribution in the TSV is directly attributable to the substrate. Instead, Mr. Berg neglects evidence from *Kinoshita*, which directly contradicts this assertion.

18. For example, below I have provided an annotated version of Figure 7 of *Kinoshita*, showing the stress distribution present in the substrate during device operation. Note that Figure 5 of *Kinoshita*, which Mr. Berg relies on also corresponds to the same conditions, namely device operation. See Ex. 2012, ¶¶ 52, 67.

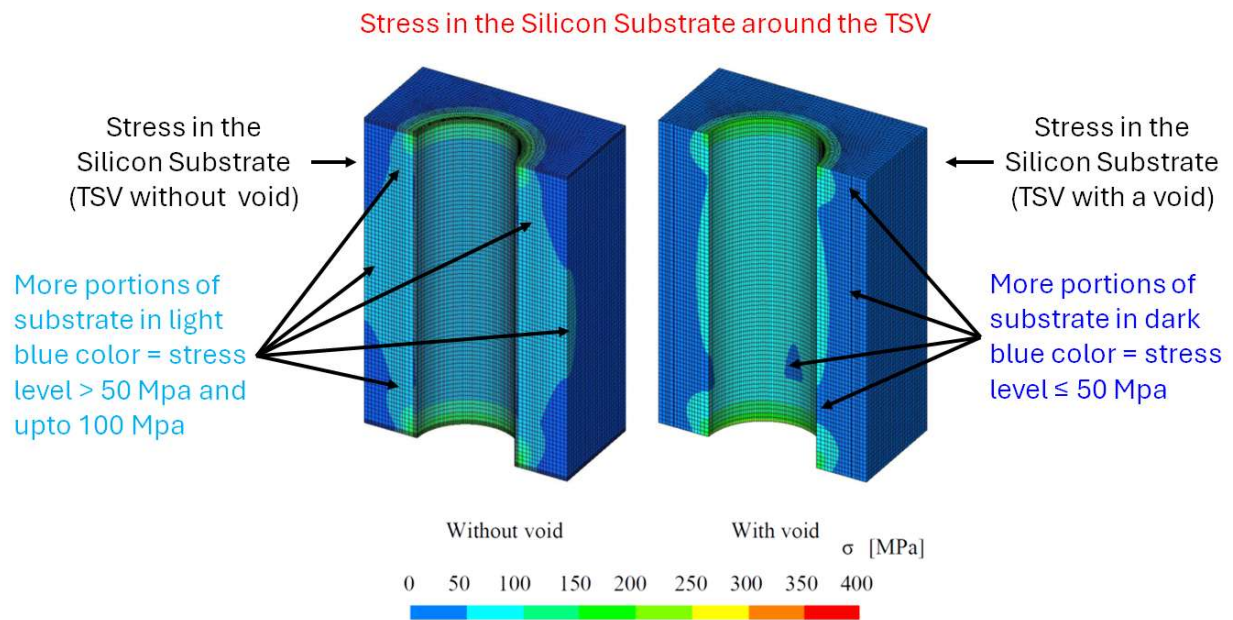


Fig. 7. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of device operation

19. One skilled in the art would understand from the scale and legends shown in Figure 7 of *Kinoshita* that the dark blue color represents stress levels less than 50 MPa. A skilled artisan would also understand that the light blue color shown in the Figure 7 of *Kinoshita* represents stress levels greater than 50 MPa and up to 100 MPa. The figure depicted on the right side of Figure 7, above, represents the stress distribution in the substrate when the TSV includes a void. In contrast,

the figure depicted on the left side of Figure 7, above, represents the stress distribution in the substrate when the TSV does not include a void.

20. As illustrated in Figure 7 of *Kinoshita*, above, in the figure on the right side (TSV with void), a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa. Compare this with the figure on the left (TSV without void) in which a smaller portion of the substrate is covered with dark blue color. Conversely, as illustrated in Figure 7 of *Kinoshita*, in the figure on the left (TSV without void), a larger portion of the substrate is colored light blue, representing stress levels up to 100 MPa as compared to the figure on the right (TSV with void). Thus, a person of ordinary skill in the art would have understood from Figure 7 of *Kinoshita* that the stress level in the substrate is lower (more dark blue portions) when the TSV includes a void than when it does not.

21. Mr. Berg disregarded Figure 7 of *Kinoshita*. Instead, Mr. Berg cited a single sentence in *Kinoshita*: “In the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa.” Ex. 2012, ¶¶ 52, 67 (citing *Kinoshita*, 3). And based on this single sentence, Mr. Berg concluded that the presence of a void does not reduce the stress on the inside of the substrate. Ex. 2012, ¶¶ 52, 67. I note that the sentence of *Kinoshita* cited by Mr. Berg does not specify the location on the inner surface of substrate at which the stress level is 100 MPa. *Kinoshita* also does not indicate whether the stated 100

MPa value represents an average value, minimum value, or maximum value.

However, Figure 7 of *Kinoshita* clearly illustrates that while some portions of the substrate can reach stress levels near 100 MPa, the overall stress in the substrate is lower—indicated by **more dark blue** regions—when a TSV void is present compared to when it is absent.

22. *Kinoshita* provides an additional example of how a TSV void reduces thermal stress in a substrate during a reflow process that may be used during manufacturing of the substrate. For example, annotated Figure 8 of *Kinoshita*, excerpted below, illustrates the stress levels present in the substrate during the reflow process, which occurs at a higher temperature than the device operation conditions of *Kinoshita*'s Figure 7.

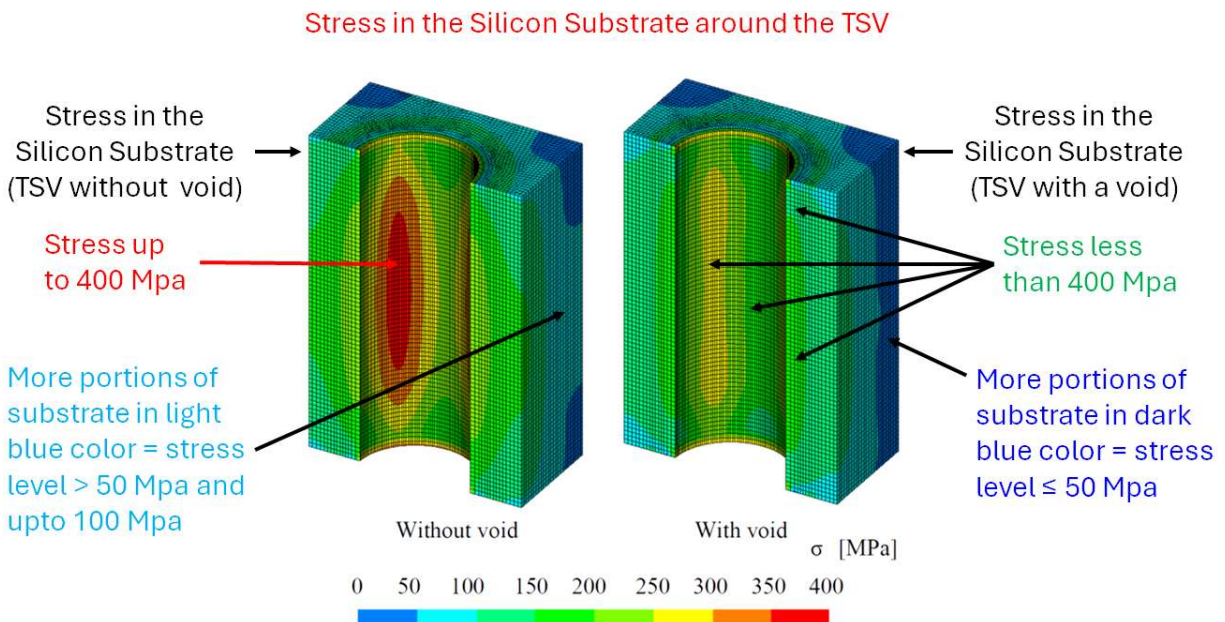


Fig. 8. Maximum principal stress distribution of Si without void (left) and with void (right) at condition of reflow process

23. One skilled in the art would understand from the scale and legends shown in Figure 8 of *Kinoshita* that the dark blue color represents stress levels less than 50 MPa, the yellow color represents stress levels of 250-300 MPa and the green color represents stress levels between 100-250 MPa. Further, a skilled artisan would understand that the red color shown in Figure 8 of *Kinoshita* represents stress levels greater than 350 Mpa and up to 400 MPa.

24. As illustrated in Figure 8 of *Kinoshita*, in the figure on the right side (TSV with void), the inner surface of the substrate surrounding the void has a stress of the order of 200-250 MPa (significantly lower than 400 MPa). Compare this with the figure on the left (TSV without void) in which the same inner surface of the substrate has stress levels between 350-400 MPa. Furthermore, as illustrated in the above figure, in the figure on the right (TSV with void) a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa, as compared to the figure on the left (TSV without void). Thus, a person of ordinary skill in the art would have understood that Figure 8 of *Kinoshita* provides additional evidence that the stress level in the substrate is lower when the TSV includes a void than when it does not.

25. In my opinion, therefore, a skilled artisan would have concluded from *Kinoshita* that the presence of a TSV void reduces the overall stress level on the

substrate. Thus, Mr. Berg's arguments against TSV voids reducing thermal stress in the surrounding substrate are contradicted by the very evidence he relies on.

IV. Mr. Berg's Arguments Against Anticipation by *Cooney* Lack Merit

26. Mr. Berg asserts that "the foundational assumption by Petitioner and Dr. Thompson that all voids and hollow centers in all TSV's reduce thermal stress is incorrect." Ex. 2012, ¶ 63. In support, Mr. Berg cites *Birner* and *Kinoshita*. Ex. 2012, ¶¶ 63-67. But as I explained, *Birner* and *Kinoshita* disclose the opposite. Specifically, neither *Birner* nor *Kinoshita* disproves the well-known thermal stress relieving behavior of TSV voids. Section III.

27. In my opinion, therefore, and as I explained in my opening declaration, *Cooney* anticipates claim 1 for two reasons: (1) because *Cooney* discloses the structure recited in claim 1 and the limitation "to reduce thermal stress in said semiconductor substrate" should not be entitled to any patentable weight, and (2) because it was well known in the art that a void as disclosed by *Cooney* would reduce thermal stress in the substrate. Ex. 1002, ¶¶ 120-123.

A. Mr. Berg's purported distinction between a "void" and the "hollow center" is wrong.

28. Mr. Berg states that "[a] 'void' is different from a hollow center." Ex. 2012, ¶¶ 62, 72. Mr. Berg also asserts that *Cooney*'s use of the term "void" is understood to be a very small pinhole type of defect that occurs when a TSV is incompletely filled. Ex. 2012, ¶ 69. In support, Mr. Berg cites *Kong* as illustrating

voids in TSVs having dimensions smaller than 4-5 μm . Ex. 2012, ¶ 69. Mr. Berg is wrong. The term void is not limited to dimensions smaller than 4-5 μm and as I explained in my opening declaration, like the claimed “hollow center,” voids do reduce thermal stress in the substrate.

29. In fact, the prior art used in the Petition and the extrinsic evidence relied on by Mr. Berg demonstrate the fallacy in Mr. Berg’s purported distinction. For example, *Birner* discloses a “through substrate via 1 formed by filling a through substrate opening 250 with a fill material 50.” *Birner*, ¶ 29. *Birner* explains that “the diameter of the through substrate opening 250 is around 5-15 μm .” *Birner*, ¶ 29. *Birner* also discloses a fill fraction of 30%. *Birner*, ¶ 38. *Birner* explains that the fill fraction is the fraction of the radius of the TSV occupied by the fill material. *Birner*, ¶ 38; Section III.A. Thus, a skilled artisan would have understood that a fill fraction of 30% implies that the fraction of the TSV diameter occupied by the void would be 70%. One of ordinary skill in the art would also understand that when the void diameter is 70% of a TSV diameter of 5 μm , the void diameter would be about 3.5 μm , and when the TSV diameter is 15 μm , the void diameter would be about 10.5 μm . In other words, a skilled artisan would have understood from *Birner*, that the void in *Birner* has a diameter of 3.5 μm for a TSV of diameter 5 μm , and a diameter of 10.5 μm for a TSV diameter of 15 μm . Further, one skilled in the art would have understood that these void

diameters are significantly larger than the smaller than 4-5 μm pinholes that Mr. Berg purportedly equates with the term “void.”

30. Similarly, *Kinoshita*, a reference relied on by Mr. Berg, discloses that the minor axis (i.e., void diameter) of its void is 12 μm . *Kinoshita*, 2. Here again, contrary to Mr. Berg’s assertions, the diameter of the void in *Kinoshita* is significantly larger than the 4-5 μm pinholes that Mr. Berg purportedly equates with the term “void.” In my opinion, therefore, the voids disclosed in the prior art are not pinholes and no different than the claimed “hollow center.” And as I discussed in Sections III.A and III.B, like the claimed “hollow center,” the voids in *Birner* and *Kinoshita* also reduce the thermal stress in the substrate surrounding the TSV. The claims require nothing more.

31. Although not required by the claims, in my opinion *Cooney*’s void size can be about the same as *Birner*’s and *Kinoshita*’s: 14 μm . For example, *Cooney* discloses that its region R1 has a linewidth of 3-50 μm , region R2 has a linewidth of 1-35 μm , and region R3 has a linewidth of 3-50 μm . *Cooney*, ¶ 51. *Cooney* also discloses that the linewidth of region R1 is preferably from 1.3 to 1.5 times that of region R4. *Id.*, ¶ 54. Thus, one skilled in the art would understand that when region R1 has a linewidth of 50 μm , the linewidth of region R4 would be about 35.7 μm ($=50/1.4$). *Cooney* also discloses that the linewidth of region R4 is preferably 0.1 to 2 times a deposition thickness of the conductor layer. *Cooney*,

¶ 54. Thus, one skilled in the art would understand that if the conductor layer is fully filled in region R4, the thickness of the conductor layer on either side of the void (namely the deposition thickness) in region R3 would be $R4/2$ ($= 35.7/2 = 18 \mu\text{m}$). Based on these disclosures, a skilled artisan would have further understood that the void diameter in *Cooney* in a region R3 having linewidth $50 \mu\text{m}$ would be about $14 \mu\text{m}$ ($= 50 - 18 - 18$) because $18 \mu\text{m}$ of thickness on either side of the void would be filled with the conductor layer. Thus, a person of ordinary skill in the art would have understood *Cooney* as disclosing void diameters of the same order of magnitude as disclosed in *Birner* and *Kinoshita*. And as I explained in my opening declaration, *Cooney*'s void would also reduce thermal stress just like the voids in *Birner*, *Pogge*, *Edelstein*, and *Kinoshita*. Ex. 1002, ¶¶47-49, 125-131, 141-145.

32. In my opinion, therefore, Mr. Berg has provided no evidence to distinguish between *Cooney*'s void and the claimed "hollow center." Quite the contrary, *Kong*, *Birner*, and *Kinoshita* demonstrate that voids may have diameters smaller than $4 \mu\text{m}$ and also may have much larger diameters, for example, $12 \mu\text{m}$ or larger. Also, as taught by the prior art, voids reduce thermal stress in the substrate. In my opinion, therefore, Mr. Berg's attempts to distinguish voids from the claimed hollow center should be rejected.

B. Mr. Berg's arguments regarding the shape of *Cooney's* TSV are irrelevant and should be disregarded.

33. Mr. Berg asserts that “the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV.” Ex. 2012, ¶ 71. But Mr. Berg provides no analysis or evidence to support his conclusion. As I explain below, even assuming Mr. Berg's statement were to be true, which it is not, his discussion of the impact of the torpedo shape on the thermal stress is irrelevant to the validity of claim 1 of the '609 patent over *Cooney*.

34. Specifically, claim 1 of the '609 patent recites a “hollow center to reduce the thermal stress in the substrate.” Nothing in claim 1 recites a straight TSV. In fact, claim 1 does not recite anything at all regarding the shape of the TSV. Nor does the '609 patent. Thus, in evaluating the disclosure of *Cooney*, a skilled artisan would have considered whether *Cooney's* torpedo-shaped TSV with the optional void results in lower thermal stress in the substrate, compared to the same torpedo-shaped TSV without the void; not whether *Cooney's* TSV reduces thermal stress relative to a straight TSV.

C. Mr. Berg's arguments regarding undesirability of voids should be disregarded.

35. Mr. Berg argues that “[r]ather than desirable features, voids are typically to be avoided.” Ex. 2012, ¶ 72. As I explained in my opening declaration,

however, the prior art contradicts Mr. Berg's assertion. For example, *Birner* discloses a method comprising "forming an enclosed cavity within the opening" of its TSV. *Birner*, ¶ 7. *Birner* explains that its invention reduces stress around the TSV by filling the TSV with an effective material that "comprises a combination of metal and voids." *Birner*, ¶ 24; Section III.A. In my opinion, one skilled in the art would have understood from these disclosures that that *Birner* advocates purposefully including voids in the TSV for reducing the thermal stress in the surrounding substrate. Section III.A.

36. *Pogge* likewise discloses that with a via structure, "a conducting path is established between the bottom of the trench and the top surface of the wafer, while a void 25 remains near the bottom of the trench" and that "the void 25 has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature." *Pogge*, ¶ 27. Indeed, *Pogge* includes claim 3, which recites: "A method according to claim 1, wherein said depositing step further comprises depositing metal so as to form a void in the feature."). *Pogge*, claim 3. A skilled artisan would have understood from these disclosures that *Pogge* also advocates purposeful formation of voids in a TSV to relieve stresses in the surrounding substrate.

37. Similarly, *Edelstein* discloses "a substrate 224 in which the through-via comprises an annular ring of insulating material 223 within which is

disposed a conductive via of metal (e.g., copper) 225 having a void 220 at its core.” *Edelstein*, ¶ 47. *Edelstein* further explains that “[c]are must be taken at both the top and bottom surfaces to leave metal across the entire via surface in order to preserve the void within.” *Edelstein*, ¶ 48. A person of ordinary skill in the art would have understood this disclosure to mean that *Edelstein* advocates intentionally forming voids within a TSV. Thus, contrary to Mr. Berg’s assertions, in my opinion, a skilled artisan would have understood that instead of avoiding voids, deliberately forming voids in TSVs helps mitigate thermal stress in the substrate surrounding the TSVs.

38. Nevertheless, Mr. Berg asserts that “[v]oids, as typically understood by the POSITA, are not large enough to have any appreciable impact on the reduction of thermal stress in the semiconductor substrate.” Ex. 2012, ¶ 72. First, I note that neither the ’609 patent nor the challenged claims specify the hollow center’s size or shape required to reduce thermal stress in the semiconductor substrate. Second, as I explained, *Birner*, *Pogge*, and *Edelstein* contradict Mr. Berg’s position and expressly disclose that voids are intentionally formed to reduce thermal stresses. Indeed, as I explained, even *Kinoshita*, which Mr. Berg relied on, discloses that a void in its TSV lowers thermal stress on the substrate.

Section III.B.

V. Mr. Berg's Arguments Against Obviousness Over Cooney Lack Merit

A. Mr. Berg's contention that *Pogge* does not disclose reduction of thermal stress in the substrate is wrong.

39. According to Mr. Berg, although *Pogge* discloses that “the void ‘has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE),’ *Pogge* “does not mention or state that the stresses would be borne by the semiconductor substrate.” Ex. 2012, ¶ 74. In my opinion, one skilled in the art would have recognized that the stress relieving behavior of the void described in *Pogge* refers to relieving stresses in the substrate.

40. For example, as I discussed in my opening declaration, *West* discloses that “[c]opper, as well as some other TSV filler materials, have a significantly higher coefficient of thermal expansion (CTE) as compared to conventional IC substrates, such as silicon” and that “[t]his CTE mismatch (Δ CTE) can result in significant thermally induced stress in the silicon including the circuitry (e.g. MOS transistors) in the silicon surrounding the TSVs.” Ex. 1002, ¶ 47 (citing *West*, ¶5). As I also discussed in my opening declaration, *Birner* discloses: “Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material” of the TSV. Ex. 1002, ¶ 59 (citing *Birner*, ¶24). In my opinion, one of ordinary skill in the art would have been aware of this state of the art, indicating that the mismatch in CTE causes thermal stress in the substrate, even in the absence of a similar disclosure in *Pogge*. In my opinion,

therefore, in view of the knowledge of the state of the art, a skilled artisan would have understood *Pogge*'s disclosure of the stress relieving function of its void as including relieving stresses in the substrate.

41. One skilled in the art reading *Pogge* would have understood that differences in CTE would cause different amounts of expansion in *Pogge*'s TSV and the substrate. *See Birner*, ¶ 23. One skilled in the art would have further understood that such differences in thermal expansion would induce stress in the substrate surrounding the TSV. *See Birner*, ¶23; *West*, ¶5. Additionally, one skilled in the art would have understood that reducing the difference in the CTE would result in lower stresses induced in the substrate. Thus, a skilled artisan would have understood *Pogge* as disclosing relieving stress in the semiconductor substrate even in the absence of an explicit writing in *Pogge* confirming this well-known behavior of TSV voids.

B. Mr. Berg's contention that *Edelstein* only discloses mechanical stress and not thermal stress is similarly wrong.

42. Mr. Berg argues that "*Edelstein*'s discussion is entirely centered around removing mechanical stresses, not thermal stresses." Ex. 2012, ¶ 75. I disagree. A person of ordinary skill in the art would have understood that thermal stress is nothing but mechanical stress caused due to thermal expansion. For example, as explained by a well-known and well-regarded text on Strength of Materials, mechanical stress results from displacement or strain induced by

external forces. *Timoshenko* (Exhibit 1027), 18 (*see e.g.*, Eqs. 2-4). *Timoshenko* explains that thermal stress is evaluated using the same expressions that are used to determine mechanical stress, except that the displacement or strain is determined based on the coefficients of thermal expansion and the change in temperature. *Timoshenko*, 40 (*see e.g.*, Eq. 12).

43. *Edelstein* discloses providing “a through-via structure including conductive material having a coefficient of thermal expansion which closely matches the substrate material, a reduced modulus and a reduced Poisson ratio in order to minimize the negative effects of thermal mismatch.” *Edelstein*, ¶ 13. One skilled in the art would have understood that Poisson’s ratio and modulus determine the thermal stress generated as a result of the thermal expansion. *Timoshenko*, 66. In my opinion therefore, one skilled in the art would have understood *Edelstein* as disclosing that reducing the CTE mismatch between the conductive and substrate materials, and reducing the modulus and Poisson’s ratio would reduce thermal stresses in the substrate. In my opinion, therefore, contrary to Mr. Berg’s assertion, a skilled artisan would have understood that thermal stress is nothing but mechanical stress generated due to strain induced by temperature change. Furthermore, in my opinion, one skilled in the art would have understood *Edelstein*’s discussion of matching the CTE of the TSV with voids to the substrate,

and reducing Poisson's ratio and modulus as being directed towards reducing the amount of thermal stress in the substrate surrounding *Edelstein's* TSV.

44. I further note that even *Kinoshita*, which Mr. Berg relied on, equates thermal stresses with mechanical stresses because it uses these terms interchangeably. For example, *Kinoshita* states:

In this study, the effects of the presence of voids inside the TSVs in a 3D SiP structure on the *thermal stresses in the TSV structure* under device operating condition are analyzed using the large scale simulator, ADVENTURECluster [15]. The *mechanical stresses in the Cu TSVs and in the Si chips* are obtained from the simulations."

Kinoshita, 2 (emphases added).

45. Mr. Berg further asserts that "*Edelstein* also never discloses the reduction of stress (whether mechanical or thermal) in the substrate itself." Ex. 2012, ¶ 75. This too is incorrect.

46. *Edelstein* discloses "most metals which are commonly used for integrated circuit interconnect vias generate unacceptable stress levels *on the carrier layer material (e.g., Si or glass)* due to thermal expansion mismatch." *Edelstein*, ¶8 (emphasis added). One skilled in the art would understand that *Edelstein's* carrier layer is the substrate surrounding *Edelstein's* TSV.

47. *Edelstein* also discloses:

Although it does not change the thermal expansion coefficient [of the conductive material or the substrate], the introduction of a void or voids reduces the effective modulus and Poisson ratio of the through-via, resulting in a compliant through-via that exerts *much less stress* and force *on the surrounding structures*. In other words it *behaves on a whole as if it had a much smaller thermal expansion mismatch with the substrate*, thereby reducing piston-like deviations at the top during thermal cycling.

Edelstein, ¶ 47 (emphases added).

48. Thus, contrary to Mr. Berg's assertion, *Edelstein* expressly discloses that the presence of the void in its TSV effectively reduces the CTE mismatch between the conductive and substrate materials, which also exerts less stress on the surrounding structures like the substrate.

49. Mr. Berg further argues that even if *Pogge* and *Edelstein* teach that thermal stresses are relieved by the voids in their respective devices, these references would not have taught a POSITA that all voids decrease thermal stress in all TSVs. Ex. 2012, ¶¶ 74-75. As I explained, however, Mr. Berg failed to demonstrate that all voids do not reduce thermal stress. Section III. Quite the contrary, Mr. Berg's evidence, *Birner* and *Kinoshita*, demonstrates that voids in TSVs reduce thermal stresses in the surrounding substrate.

50. Mr. Berg also argues that thermal stress relieving behavior of voids was not well-known. Ex. 2012, ¶¶ 73-76. As I discussed above and in my opening declaration, the disclosures of *Pogge*, *Edelstein*, *West*, and *Birner* establish the well-known thermal stress relieving behavior of voids. And even *Kinoshita*, relied on by Mr. Berg, establishes the thermal stress relieving behavior of voids. Section III.B. In my opinion, therefore, one skilled in the art would have found it obvious to include a void in *Cooney*'s TSV to achieve these stress relieving benefits.

VI. Conclusion

51. For the reasons set forth here and in my opening declaration, it is my opinion that one skilled in the art would have found claims 1-18 of the '609 patent anticipated by or obvious over the prior art.

52. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

53. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: September 19, 2025

Respectfully submitted,

A handwritten signature in black ink that reads "Scott E. Thompson". The signature is written in a cursive, flowing style. Below the signature is a horizontal line.

Scott E. Thompson, Ph.D.