

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,147,609
Filing Date: March 8, 2012
Issue Date: September 29, 2015

Inventors: Hadi Jebory and David J. Howard
Title: THROUGH SILICON VIA STRUCTURE, METHOD OF
FORMATION, AND INTEGRATION IN SEMICONDUCTOR SUBSTRATE

PATENT OWNER'S SUR-REPLY

Case No. IPR2024-01404

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<i>Yeda Rsch. and Dev. Co., v. Mylan Pharms. Inc.</i> , 906 F.3d 1031 (Fed. Cir. 2018)	5

LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung’s Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants’ Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	Merriam-Webster Dictionary definition for the word “taper.”
2005	Dictionary.com definition for the word “tapered.”
2006	Oxford English Dictionary definition for the word “tapered.”
2007	Transcript of June 17, 2025 Deposition of Dr. Scott E. Thompson
2008	<i>Thermal Stresses around Void in Through Silicon Via in 3D SiP</i> by T. Kinoshita, et al., published in the 2014 International Conference on Electronics Packaging (April 2014)
2009	<i>3D-interconnect: Visualization of Extrusion and Voids Induced in Copper-Filled Through-Silicon Vias (TSVs) at Various Temperatures Using X-Ray Microscopy</i> , by Kong et al., published in <i>Microelectronic Engineering</i> 92 (2012),
2010	<i>TSV Cu Filling Failure Modes and Mechanisms Causing the Failures</i> , by J.W. Choi, et al., published in <i>IEEE Transactions on Components, Packaging, and Manufacturing Technology</i> , Vol. 4, No. 4 (April 2014)

Exhibit No.	Description of Document
2011	<i>Low Stress TSV Arrays for High-Density Interconnection</i> , by Jiao, et al. (2022)
2012	Declaration of Mr. John Berg

I. INTRODUCTION

Petitioner's Reply cannot rebut the understanding of the POSITA that not all voids in TSVs reduce thermal stress in the substrate, which is not a statement of intended use but a requirement of both independent claims in the '609 Patent. Petitioner and its expert continue to rely on the mistaken assumption that because a void exists in a TSV in the prior art, then necessarily thermal stress is reduced. As shown by Patent Owner, this is not accurate. Petitioner takes issue with the disclosures in *Birner* and *Kinoshita*, despite the plain reading of both references being: (1) that voids must be designed to decrease thermal stress (in the case of *Birner*); and (2) that the presence of a void can increase thermal stress in the substrate (in the case of *Kinoshita*). Petitioner's attempt to distinguish both of these references fail.

Petitioner presents no inherency arguments or any arguments that the "optional void" in *Cooney* would be modified by the POSITA to reduce thermal stress. Because *Cooney* does not expressly disclose a void that decreases thermal stress in the substrate, it does not anticipate. And because the knowledge of the POSITA that Petitioner allegedly uses to fill this gap in *Cooney* is wrong, *Cooney* in combination with the knowledge of a POSITA would not render any claim of the

'609 Patent obvious.

II. RESPONSE TO THE KNOWLEDGE AS TO THE POSITA WITH RESPECT TO TSV VOIDS REDUCING THERMAL STRESS

Petitioner began this proceeding with a simple premise that is necessary for its claim construction and invalidity positions to succeed; that all voids in through-silicon vias reduce thermal stress in the substrate. *See* Ex. 1002, ¶ 123 (“Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney*’s void 25 reduces thermal stress in *Cooney*’s substrate.”). This premise is incorrect, as discussed at length in Patent Owner’s Response. In addition to the Declaration of Mr. Berg, Patent Owner also noted that *Birner*, a reference relied upon by Petitioner, and *Kinoshita*, a contemporaneous reference, evidence the knowledge of a POSITA that, while some voids may reduce thermal stress, others may increase thermal stress or have no impact whatsoever. POR, at 22–28.

On Reply, Petitioner takes issue with the citations to *Birner* and *Kinoshita*. But Petitioner misreads and misinterprets the documents, and its submission of a new Declaration of Dr. Thompson is further evidence of its flawed original premise.

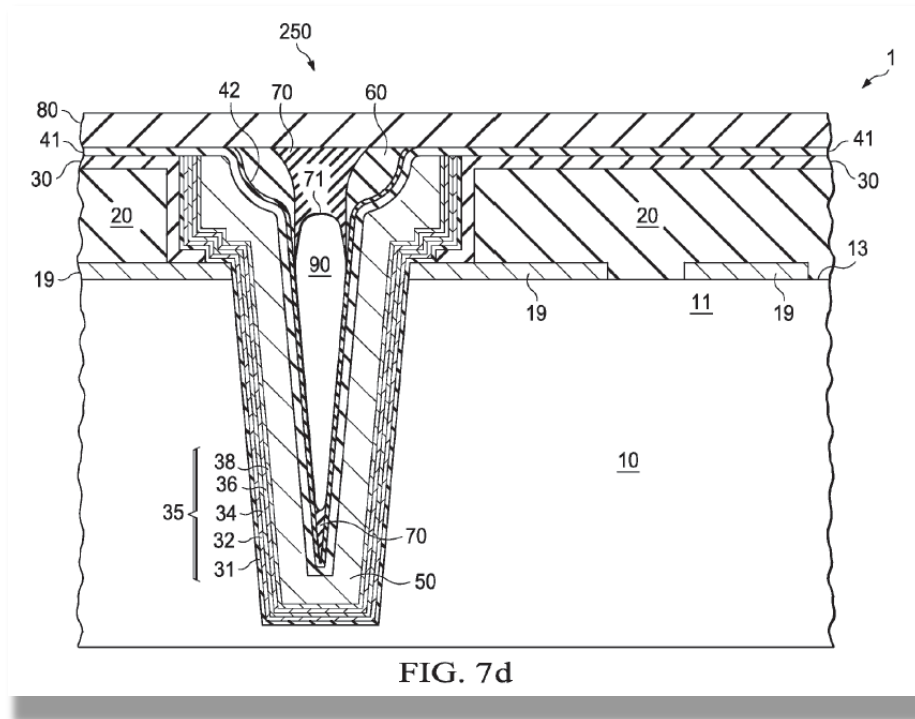
A. *Birner* Evidences the Knowledge of a POSITA that Voids Must Be Specifically Designed to Impact Thermal Stress

Birner discloses, in plain English, that the type, size, and amount of fill

material must be selected to “minimize[] the stress from thermal expansion.” Ex. 1022, ¶ [0038]. The implication here, supported by other evidence available to the POSITA, is that if these conditions are not met, the void will not minimize the stress from thermal expansion. Ex. 2012, ¶ 49. In an effort to deflect this clear flaw in its reasoning, Petitioner claims that Mr. Berg is “ignoring . . . embodiments” of *Birner* and that, in these embodiments, “the presence of voids (without specifying any size or shape) in the metal filled in *Birner*’s TSV, reduces the CTE mismatch . . . and consequently reduces the stress in the substrate surrounding the TSV.” Ex. 1025, ¶¶ 7–14 (citing *Birner* ¶ 24). But *Birner* need not disclose a void that has no impact on thermal stress in *every* embodiment, only one.

Birner discusses using “a numerical simulator” or other simulations to determine “the appropriate shape and structure of the tailored void 90 relative to the fill material 50” and that these calculations “can account for changes in stress in different regions, for example, in the corners.” Ex. 1022, ¶ [0038]. While *Birner* mentions manufacturability, it also notes that the tailored void 90 “comprises dimensions that are tailored to minimize stress concentration during, for example, subsequent thermal cycling.” *Id.* ¶ [0073]. The void, as would be known to the POSITA, must be “tailored” to minimize these stresses. Figure 7(d) of *Birner*

discloses the void that has been tailored as such:



As relied upon by Mr. Berg, *Birner*’s specific discussion of *how* to tailor the void to minimize thermal stress is completely missing from Petitioner’s analysis of the “optional void” in *Cooney*, and is evidence that the POSITA would have known that, while it is possible for voids in TSVs to reduce thermal stress, not all voids do so.

Petitioner also argues that, while *Birner* provides disclosure of how to “minimize” thermal stress, it does not suggest that there could exist voids that have *no* impact on thermal stress. Reply at 4. Herein lies the flaw in Petitioner’s logic. Petitioner continues to assume that *all* voids decrease thermal stress, and that when

Birner uses the term “minimize” that does not disprove Petitioner’s original theory. But, as shown by Mr. Berg in the concept of *Kinoshita*, voids can actually increase thermal stress. Thus, *Birner*’s discussion of the “minimization” of thermal stress can also be understood to mean that a void, if designed outside of the characteristics disclosed in *Birner*, can also have no impact or maximize thermal stress.

B. *Kinoshita* Discloses a Void that Increases Thermal Stress in the Substrate

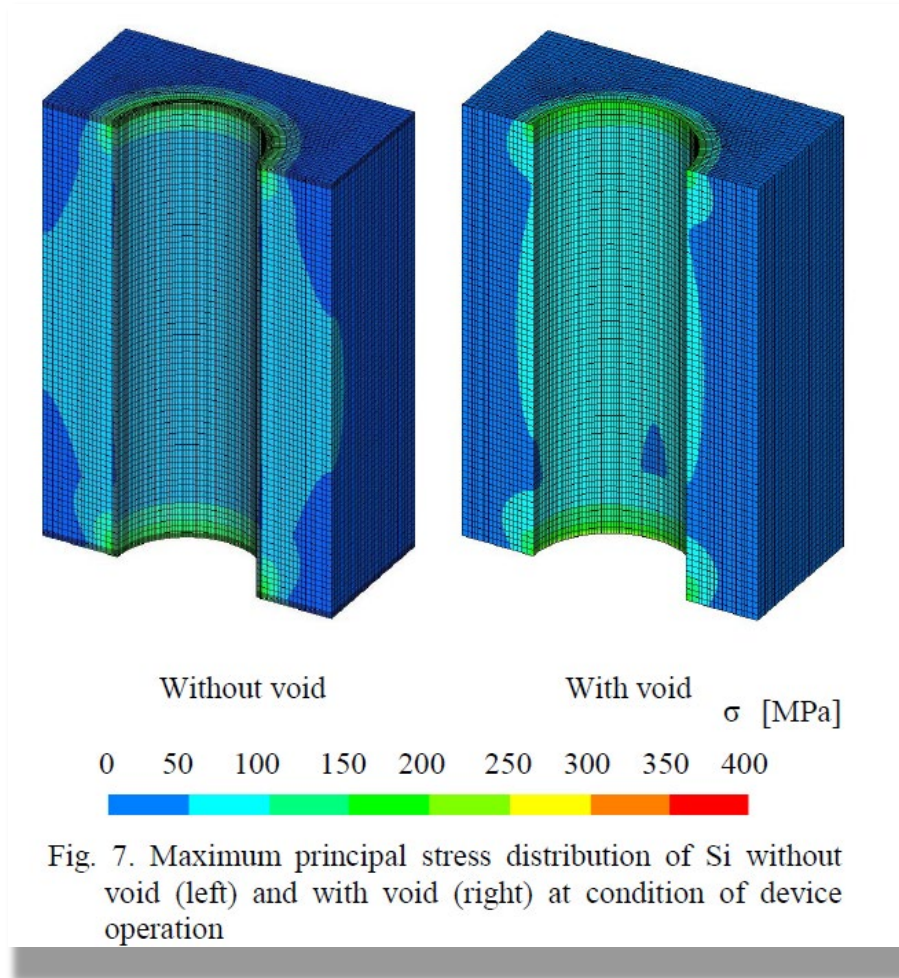
In addition to the clear disclosures of *Birner*, Patent Owner also relies on *Kinoshita* for the proposition that all voids in all TSV’s do not automatically decrease thermal stress.

Petitioner first states that because *Kinoshita* is not prior art, it would have not been available to the POSITA. Reply at 5. But post-priority documents can be used to show the knowledge of the POSITA. *Yeda Rsch. and Dev. Co., v. Mylan Pharms. Inc.*, 906 F.3d 1031, 1041–42 (Fed. Cir. 2018).

Petitioner next argues that *Kinoshita* contradicts Patent Owner’s position. Reply at 5. But *Kinoshita* does nothing of the sort. *Kinoshita* discloses a TSV with a void that has higher thermal stress at equivalent temperatures than a TSV without a void. Ex. 2012, ¶¶ 65–67. This disclosure is, like the above disclosure in *Birner*, independently fatal to Petitioner’s analysis. Petitioner does not dispute or contradict

this disclosure; rather, it argues that Patent Owner provides “no support” for the proposition that the higher stress in the voided TSV in *Kinoshita* is “transferred directly to the substrate.” Reply at 6. Patent Owner did provide support for this proposition, in the form of expert testimony. Ex. 2012, ¶ 67. Petitioner’s additional attempts to burden-shift should be dismissed.

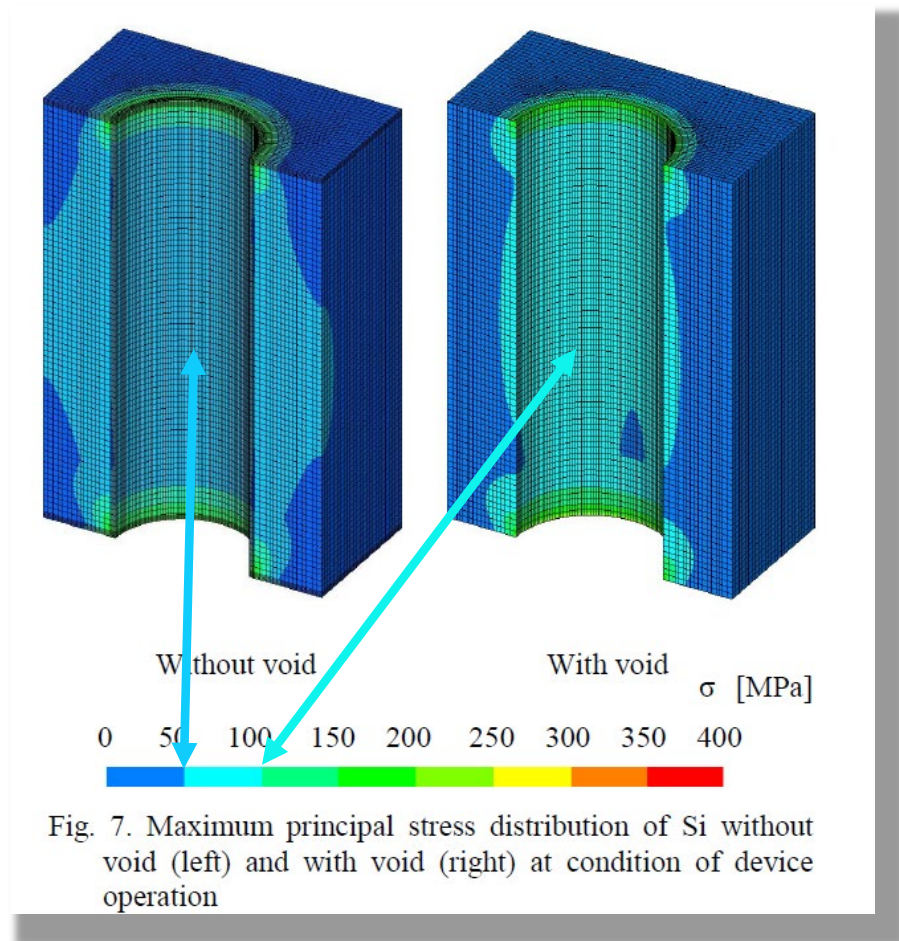
Kinoshita’s Figure 7 also supports Patent Owner’s position. Figure 7 shows the “cylindrical inner surfaces of Si,” with the TSV and the SiO₂ insulator layers removed. Ex. 2008 at 3. As can be seen, the thermal stress on the substrate in the simulation with the void is higher than that of the simulation without the void:



Kinoshita, Fig. 7

The stress in the Si of the voided TSV on the right, above, clearly contains more area of stress between 100 and 150 MPa than the stress on the Si of the non-voided TSV on the left. Petitioner notes that while the stress travels further into the substrate on the left, the distance traveled is irrelevant to the claims or arguments at issue. Dr. Thompson states that a “larger portion of the substrate is shown in dark

blue” on the right side (TSV with void). Ex. 1025, ¶ 20. But even the most cursory review of *Kinoshita* shows that the voided TSV exhibits *more* stress on the inner surface of the Silicon layer. An annotated version of Figure 7 is provided below, with arrows showing the approximate stress levels on the inner surface of the Si substrate:



Kinoshita, Fig. 7 (annotated)

Petitioner's argument that there is no decrease in thermal stress in the void because some minor thermal stress travels slightly further into the substrate does not disprove Patent Owner's interpretation of *Kinoshita* that the presence of a void does not inherently reduce thermal stress in the substrate, as required by the claims.

Petitioner also mentions Figure 8 of *Kinoshita*, which shows the stress distribution at a higher temperature (during reflow). But this Figure is irrelevant; it is not necessary to show that the void increases thermal stress under all conditions in order to discredit Petitioner's fundamental logical assumption that all voids decrease thermal stress.

III. CLAIM CONSTRUCTION

Petitioner continues to advocate for ignoring the claim language in order to advance its untenable positions for anticipation and obviousness. Statements of intended use, in certain situations, can be ignored particularly when they appear in the preamble of a claim. But where the claim language describes something about the structure of the apparatus, that claim language is entitled to patentable weight.

A. “to reduce thermal stress in said semiconductor substrate”

Each Challenged Claim in the '609 Patent requires a plurality of through-silicon vias “having a hollow center to reduce thermal stress in said semiconductor

substrate.” Petitioner’s proposed construction, which is to give no patentable weight to this claim element, would mean that a plurality of through-silicon vias with hollow centers would automatically be within the scope of this claim term, regardless of whether they reduce, increase, or have no impact on the thermal stress in the semiconductor substrate. This absurd result is contrary to established case law.

Petitioner’s flawed case law on intended use is distinguished in Patent Owner’s Response. POR, at 9–16. On Reply, Petitioner attempts to distinguish Patent Owner’s case law. Reply at 10. But Petitioner cannot.

The doctrine that gives no patentable weight to statements of intended use is to prevent claiming new uses for old products. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997) (“It is well settled that the recitation of a new intended use for an old product does not make a claim to that old product patentable.”). But here, the claim language at issue does not recite a new use for the claimed hollow center. Rather, the claimed hollow center must be structured in a way so as “to reduce thermal stress in the semiconductor substrate.” A void does not inherently reduce thermal stress in the semiconductor substrate and, therefore, this claim language should not be ignored.

Petitioner attempts to distinguish *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1363-64 (Fed. Cir. 1999), by stating that “the limitation ‘hollow center to reduce thermal stress in said semiconductor substrate’ says nothing about the structure of the hollow center.” Reply at 11. But this is where Petitioner is incorrect—the structure of the hollow center must be such that it reduces thermal stress in the semiconductor substrate. Ex. 2012 , ¶¶ 47–54.¹

Petitioner next cites to *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469 (Fed. Cir. 1990), again for the well-known proposition that “apparatus claims cover what a device is, not what a device does.” Reply at 11. This misses the mark, as apparatus claims can, of course, include functional limitations that cannot be ignored. *Wright Medical Tech., Inc. v. Osteonics Corp.* 122 F.3d 1440, 1443–44 (Fed. Cir. 1997) (functional language analyzed as claim limitation and

¹ Petitioner also purports to cite the holding of *K-2* as somehow antithetical to Patent Owner’s position. However, the court in that case specifically held that the proposed functional language in the claim was not to be ignored and that “the functional language tells us something about the structural requirements of the attachment between the bootie and the base.” *K-2 Corp.*, 191 F.3d at 1363.

noting that accused product “meets the functional objective of the invention”). Petitioner also attempts to distinguish *Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 381 F.3d 1111, 1117–20 (Fed. Cir. 2004) by arguing that in that case, the term “operatively connected” means that the claimed components must be “connected in a way to perform a designated function.” Reply, at 12. But that is precisely what is required by the claims of the ’609 Patent, which is that the hollow center must perform a designated function, namely, reduction of thermal stress in the substrate.

Because the functional language in the Challenged Claims of the ’609 Patent are not merely statements of intended use, they cannot be eviscerated.

B. “to provide space for said conductive filler to expand inward,” and “to prevent contamination during processing of said semiconductor substrate”

The dispute with respect to these terms is the same as the dispute regarding the first term. These functional limitations, for the same reasons, cannot be eviscerated from the claims.

C. Prosecution History Acquiescence

Petitioner did not respond to Patent Owner’s rebuttal of its argument regarding Prosecution History Acquiescence (POR at 16), and therefore Petitioner appears to

have abandoned this argument.

IV. GROUND 1A: ANTICIPATION BY *COONEY*

Because Petitioner based its argument on the flawed assumption that all voids decrease thermal stress in the substrate, there can be no anticipation by *Cooney*. Neither Petitioner nor its expert performed *any* analysis of the “optional void” in *Cooney* to determine whether any of its characteristics would cause a decrease in thermal stress in the substrate. Patent Owner, in its Response, noted this lack of analysis. POR, at 27-28. On Reply, Petitioner submits a supplemental declaration attempting to backfill its expert declaration with an analysis of the size of *Cooney*’s void. Reply, at 15–16.

Petitioner first presents case law allegedly supporting its position that it is entitled to supply a missing limitation from *Cooney* using expert testimony in an anticipation analysis. *Id.*, at 14. According to Petitioner, it used the expert declaration of Dr. Thompson “to show what a POSITA would have understood from *Cooney*’s disclosure of a void.” *Id.* While it is true that an expert opinion may be used to interpret an allegedly anticipating reference, Dr. Thompson did nothing of the sort. Rather, he merely stated in a single line that because *Cooney* contains a void, that void reduces thermal stress in the substrate. Ex. 1002, ¶ 123. But “a

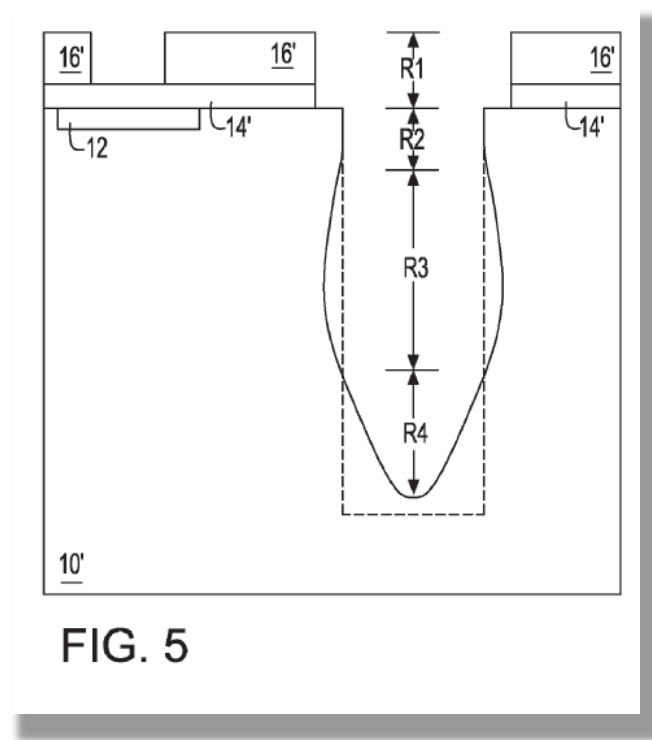
petitioner asserting anticipation cannot rely on its expert to supply disclosure of a claim element that is not expressly or inherently present in the reference.” P.T.A.B. Consolidated Trial Practice Guide, at 36 (Nov. 2019).² Expert testimony cannot be used to take the place of disclosure in an anticipatory reference, which is precisely what occurred here.

Petitioner next backfills its original argument by analyzing the size and shape of the void in *Cooney*, noting that “a POSITA would have determined the void size in *Cooney* can be about 14 μ m based on the dimensions disclosed in *Cooney*.” Reply, at 16.³ Petitioner cites to its supplemental expert declaration and paragraphs 51 and

² Petitioner’s case law is unavailing. Both *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1328 (Fed. Cir. 2001) and *Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co.*, 878 F.3d 1336, 1345 (Fed. Cir. 2018) relate to the use of expert testimony to prove inherency. But Petitioner is not making any inherent anticipation argument here, nor can it.

³ It is also unclear why Petitioner makes reference to the size of the voids in *Birner* and *Kinoshita* (Reply at 16) because, as discussed above, those voids do not decrease thermal stress in the substrate.

54 of *Cooney* to allegedly make this conclusion. Ex. 1025, ¶ 31 (citing *Cooney*, ¶¶ 51, 54). Dr. Thompson relies on the linewidths disclosed in *Cooney* which only relate to the depth of the TSV itself. *Cooney*'s Figure 5 contains several "linewidths" that delineate the TSV into four "regions" R1 through R4:



Dr. Thompson uses these measurements to estimate that “a skilled artisan would have further understood that the void diameter in *Cooney* in a region R3 having linewidth 50 μm would be about 14 μm ($= 50 - 18 - 18$) because 18 μm of thickness on either side of the void would be filled with the conductor layer.” Ex. 1025 ¶ 31. This calculation appears to be based completely on the relative linewidths

in *Cooney*, which represent the vertical depth, not the horizontal width of either the torpedo shape or the void itself. There is simply no disclosure of the size of the “optional void” in *Cooney*, nor is there any disclosure of that void reducing thermal stress in the substrate. Dr. Thompson, aside from improperly calculating the size of the void in *Cooney*, does not analyze any other characteristic of *Cooney*’s void (or the non-standard shape of the TSV itself) to conclude that it reduces thermal stress. *Id.*, ¶¶ 28–34. On this record, Petitioner cannot show that *Cooney*’s void decreases thermal stress in the substrate.

If the “optional void” in *Cooney* were designed to reduce thermal stress in the substrate, it likely would not have been referred to as a “void,” which, according to Mr. Berg and contemporaneous expert testimony, is a term typically used to refer to a pinhole type defect that occurs when a TSV is incompletely filled. Ex. 2012, ¶ 69. Mr. Berg also analyzes the shape of the TSV in *Cooney*, noting that the unconventional torpedo shape increases thermal stress in the substrate. *Id.*, ¶ 71. Petitioner somehow claims that this opinion is “unsupported expert testimony” (Reply at 17), despite Mr. Berg opining that:

[T]he torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical

straight TSV. This is because filling this bulge requires additional metal to fill the TSV. Because there is more metal, it will increase by a greater factor at a given temperature than a straight TSV with less metal. And the torpedo shape itself can increase thermal stresses, by focusing stress on certain portions of the substrate rather than spreading them out along the entire TSV.

Dr. Thompson did not analyze the shape of the void in *Cooney*.

Ex. 2012, ¶ 71. This is significantly more analysis than Dr. Thompson's discredited boilerplate recitation that all voids decrease thermal stress in the substrate. While Claim 1 does not require a TSV or a void therein to be any particular shape, it does require that the void decrease thermal stress in the substrate, a disclosure that is demonstrably missing from *Cooney* and Petitioner's anticipation analysis. Dr. Thompson does not address this argument, merely noting that "the optional void results in lower thermal stress in the substrate, compared to the same torpedo-shaped TSV without the void." Ex. 1025, ¶ 34. The torpedo shape of the TSV in *Cooney*,

in combination with its complete lack of disclosure of reduction of thermal stress in the substrate, means that *Cooney* cannot anticipate any claim.

Petitioner's remaining arguments for anticipation by *Cooney* repeat the discredited assertion that all voids and hollow centers decrease thermal stress in the substrate. Reply, at 18–19. While certain voids and hollow centers certainly *can* decrease thermal stress in the substrate, they must be specifically designed to do so, and there remains no analysis of how *Cooney*'s void so does. The POSITA, aware of the characteristics of voids and hollow centers in TSVs, would have understood that an analysis would need to be conducted regarding the thermal stresses caused by or relieved by each, and this analysis was not performed. Ex. 2012, ¶¶ 63–77.

V. GROUND 1B: OBVIOUSNESS BY *COONEY*

Recognizing the inherent weakness in *Cooney*, Petitioner presents several obviousness arguments involving *Cooney*. But none of these secondary references nor the understanding of a POSITA supply the missing limitation. Petitioner does not argue why or how the “optional void” in *Cooney* would need to be modified in order to reduce thermal stress, and Petitioner's secondary references merely stand for the same propositions as above, which is that while some voids decrease thermal stress in the substrate, others do not.

A. Petitioner Does Not Present any Evidence Regarding Modification of *Cooney's* Void

Critically, the Petition does not suggest that the optional void in *Cooney* could or should be modified to be of a size, shape, or other characteristic that would reduce thermal stress in the substrate. Rather, Petitioner merely argues that “it was well known that the presence of a void in a filled TSV results in a lower amount of thermal stress in the surrounding substrate.” Pet. at 21 (citing Ex. 1002, ¶ 125). This, as discussed above, is incorrect. While a void *can* decrease thermal stress in the substrate, the lack of discussion in the Petition as to *how* the void in *Cooney* decreases thermal stress is fatal to the analysis. Pet., 19–22; 53. And supplying the knowledge of a POSITA, as evidenced by any number of secondary references, does not provide any motivation to modify the “optional void” in *Cooney* to cause such a reduction as required by the claims.

B. *Pogge* and *Edelstein* Do Not Supply the Missing Limitation

Neither *Pogge* nor *Edelstein*, nor any other cited reference, stand for the proposition that the POSITA would have understood that *all* voids and hollow centers reduce thermal stress in the substrate as required by the claims. POR, at 31–33. And, as opined upon by Mr. Berg, there exist voids that increase such thermal stress. Ex. 2012, ¶¶ 74, 75. Even assuming that *Pogge* or *Edelstein*, or any other

secondary reference discloses a particular hollow center that, in that particular configuration, reduces thermal stress in the substrate, that is insufficient to show that a POSITA would have understood either that all voids do so, or that the void in *Cooney* does so, absent any analysis of *Cooney*'s void. Therefore, Petitioner has not met its burden to show that any Challenged Claim is obvious over *Cooney* in view of the knowledge of a POSITA.

VI. REMAINING GROUNDS

The remaining grounds all fail because *Cooney* does not anticipate or render obvious either Claim 1 or Claim 11 due to its failure to disclose the reduction of thermal stress in the substrate.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding no claims unpatentable.

Respectfully submitted,

Dated: October 31, 2025

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S SUR-REPLY specified in 37 C.F.R. § 42.24 has 3,481 words in compliance with the 5,600 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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