

Before The Patent Trial And Appeal Board
Oral Hearing
January 7, 2026

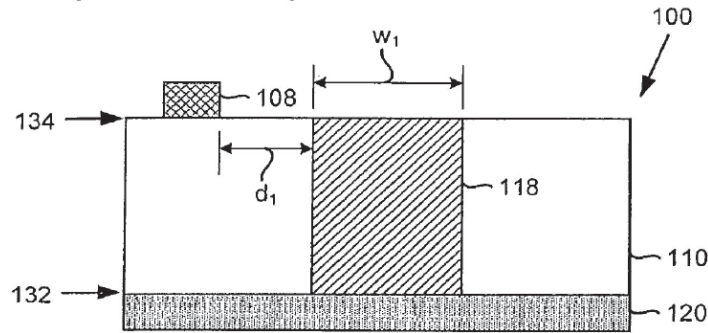
Harbor Island's Presentation

IPR2024-01404: U.S. 9,147,609

Problem to be Solved in the Art

Large Vias Create Multiple Issues

Fig. 1A (Prior Art)



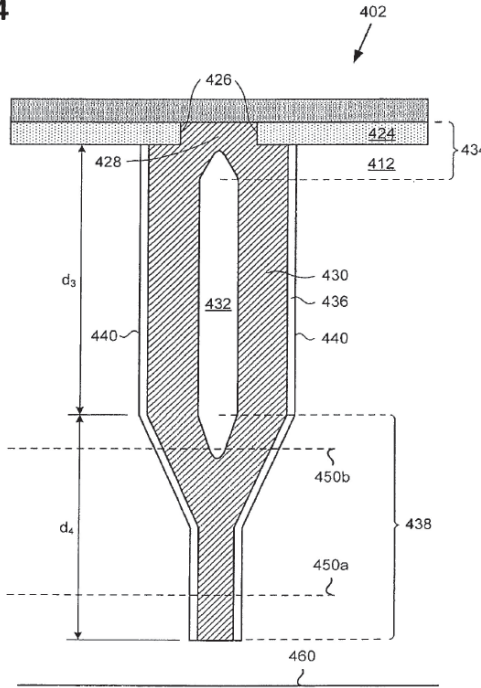
In addition, the very large width of through-wafer via **118** typically limits the number of through-wafer vias that may be formed in a substrate of a particular dimension. For example, in a typical substrate it is common for multiple through-wafer vias to be spaced hundreds of micrometers (μm) apart. Such large spacing between through-wafer vias results in uneven thermal dissipation within the substrate. Differences in the thermal coefficients of substrate **110** and through-wafer via **118** may cause high levels of mechanical stress in substrate **110** when heated, which can lead to cracking of substrate **110**. The very large width of exemplary through wafer via **118** can increase such thermally induced mechanical stress in substrate **110**.

Ex. 1001 ('609 Patent), 2:55-67

Solution to the Problems

Build Many Small Vias With Pinched Off Region

Fig. 4



Use Hollow Center To Decrease Thermal Stress

portion 432 in TSV 402 can be formed using present manufacturing tools and without increasing production costs.

Ex. 1001 ('609 Patent), 4:60-5:2

Challenged Claims

Use Hollow Center To Decrease Thermal Stress

1. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate, said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward;

wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said pinched off region.

11. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:

a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;

a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;

wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.

Petitioner Takes Inconsistent Claim Construction Positions

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy in this forum.¹

Petition at 8.

The phrase “to reduce thermal stress in said semiconductor substrate” states the use of or explanation for the hollow center and should be entitled to no patentable weight over the prior art. *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999) (holding that “a scientific explanation for the prior art’s functioning, does not render the old composition patentably new”);

Petition at 20.

Proper Construction of Functional Limitations

Functional Limitations Cannot Be Ignored

Other than disclosing the presence of a hollow center in the TSV, the '609 patent does not identify any features of the hollow center that contribute to thermal stress reduction in the semiconductor substrate.

Petition at 20.

11. A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:
a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;
a conductive filler disposed within each of said plurality of through silicon vias, each of said plurality of through silicon vias having a hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward for reducing thermal stress in said semiconductor substrate;
wherein each of said plurality of through silicon vias has a pinched off region at a top portion and another pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate, and wherein said hollow center is tapered in said another pinched off region.

Proper Construction of Functional Limitations

Functional Limitations Cannot Be Ignored

K-2's primary argument is that the functional language in the claim following this limitation—“*for substantially preventing movement therebetween at least in a horizontal plane*”—dictates the meaning of “permanently affixed.” That is, K-2 suggests that the inclusion of this functional language converts the meaning of “permanently affixed” to mean “affixed to prevent movement in at least a horizontal plane.” We cannot accept this reading of the claim. ***The functional language is, of course, an additional limitation in the claim.*** See, e.g., *Wright Medical Technology, Inc. v. Osteonics Corp.*, 122 F.3d 1440, 1443–44, 43 USPQ2d 1837, 1840 (Fed.Cir.1997) (functional language analyzed as a claim limitation). This limitation requires that the attachment between the bootie and the base “substantially prevent[]” movement of the bootie (and presumably, the user's foot when inserted in the bootie) in a horizontal plane. In other words, ***the functional language requires that the attachment prevent the bootie from sliding around on top of the base***; it demands a structural rigidity in the horizontal dimension to the connection between the bootie and the base.

K-2 Corp. v. Salomon S.A., 191 F.3d 1356, 1363-64 (Fed. Cir. 1999)

Proper Construction of Functional Limitations

Not All Hollow Centers Reduce Thermal Stress

44. I disagree with Dr. Thompson that no claim terms need express construction to resolve the disputes in this proceeding, because he is apparently interpreting the claims to merely require the existence of the claimed hollow center, not a hollow center that reduces thermal stress.

Berg Decl., ¶ 44.

Proper Construction of Functional Limitations

Hollow Centers Can Increase Thermal Stress

49. Contrary to Dr. Thompson's analysis, in my opinion, the POSITA would have understood that in certain circumstances, the presence of a hollow center or void in a TSV may increase thermal stress in the substrate, rather than reduce it, even when it provides space for the TSV fill material to expand inward.

Berg Decl., ¶ 49.

Proper Construction of Functional Limitations

Birner Shows That Hollow Centers Must Be Specifically Designed to Decrease Thermal Stress

[0037] In various embodiments, the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum defectivity arising from thermal or other stress related defects. Although, only one through substrate via 1 is illustrated, a through substrate via chip may comprise more than one through substrate via 1.

Birner, Ex. 1022, ¶¶ 37

POR at 10-11

Proper Construction of Functional Limitations

Hollow Centers Must Be Designed to Decrease Thermal Stress

[0038] As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material 50 is selected relative to the dimension of the tailored void 90. For example, a fraction of the fill material 50 (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1b, this fraction of the fill material 50 (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} . The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material 50 (α_{FM}) and the tailored void (α_V) as $f_{FM} = (\alpha_{Si} - \alpha_V) / (\alpha_{FM} - \alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM} \approx 0$, the fraction $f_{FM} = \alpha_{Si} / \alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening 250 r_{TSV} . In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion.

Birner, Ex. 1022, ¶ 38
POR at 10-11

Proper Construction of Functional Limitations

***Kinoshita* Shows That Hollow Centers Can Increase Thermal Stress**

50. As another example, as shown in the paper *Thermal Stresses around Void in Through Silicon Via in 3D SiP* by T. Kinoshita, et al., which was published in the 2014 International Conference on Electronics Packaging (April 2014) (Ex. 2008, “Kinoshita”), under operational conditions the presence of a void can actually increase thermal stresses inside the TSV, which would in turn increase thermal stresses in the silicon substrate.

Proper Construction of Functional Limitations

Kinoshita Shows That Hollow Centers Can Increase Thermal Stress

Thermal Stresses around Void in Through Silicon Via in 3D SiP

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C. Thermal stress simulation

In this study, an inelastic thermal stress simulation was carried out to discuss the effect of the presence of void inside the TSVs on the thermal stresses in the Cu TSV and the Si chip under the device operating condition and the reflow process. It was assumed that the temperature of the model was uniformly changed under both conditions. The stress free temperature was assumed to be the room temperature of 25 deg. C., which corresponds to the power OFF state of the devices. In case of device operation, temperature was elevated up to 85 deg. C. In case of reflow process, temperature was elevated up to 260 deg. C. in the simulations.

Kinoshita, Ex. 2008, at 107

Proper Construction of Functional Limitations

III. RESULTS

The results of the inelastic thermal stress simulation, the equivalent stress distributions in the cross-sections of the models without and with a void inside the TSVs were shown in Fig. 5. In the case of the TSV structure without voids the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa. The magnitude of the equivalent stress was lower than the yield stress of bulk copper which is 230 MPa. It was insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation. In case of the TSV structure with a void the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa. It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper. It was also insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation.

Kinoshita, Ex. 2008, at 107

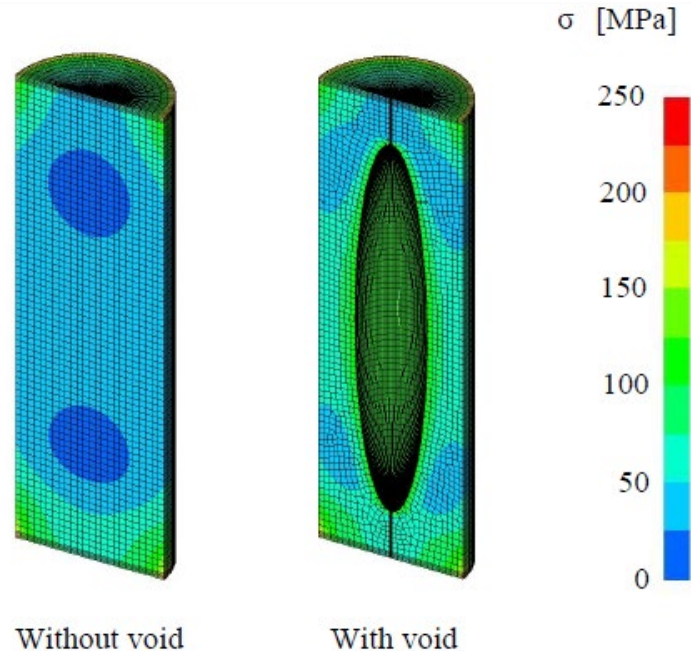
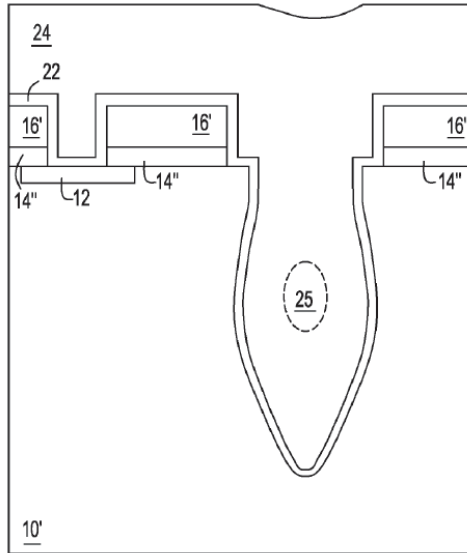


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

The Prior Art: *Cooney*

Dr. Thompson's Analysis of *Cooney's* Void



Ex. 1004, FIG. 6

123. **Ground 1A:** Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney's* void 25 reduces thermal stress in *Cooney's* substrate. The '609 patent does not identify any characteristics or properties of the hollow center that contribute to thermal stress reduction in the semiconductor substrate. Ex. 1001, 4:60-61; *see generally* Ex. 1001.

Ex. 1002 (Thompson Decl.) ¶ 123

The Prior Art: *Cooney*

Dr. Thompson's Analysis of *Cooney*'s Void

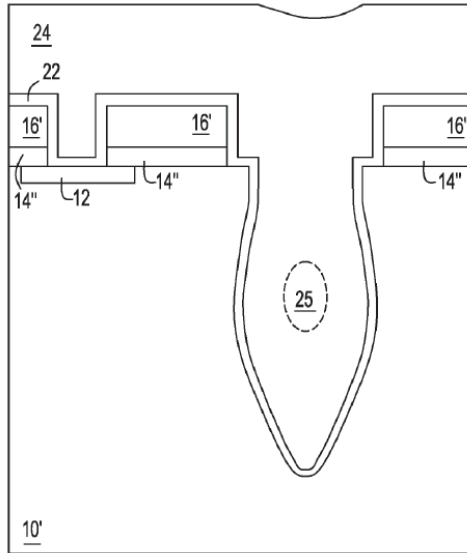


FIG. 6

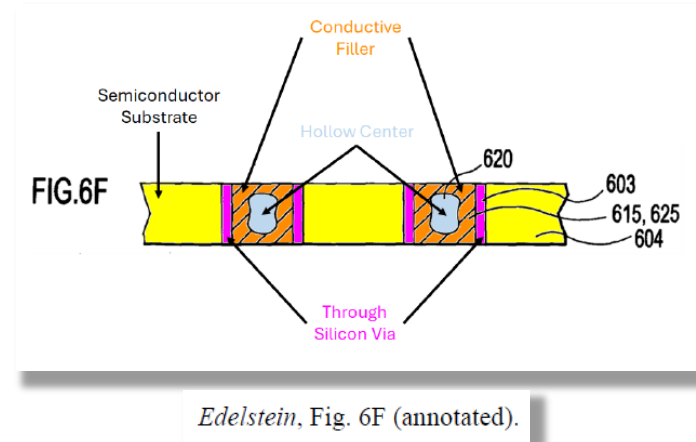
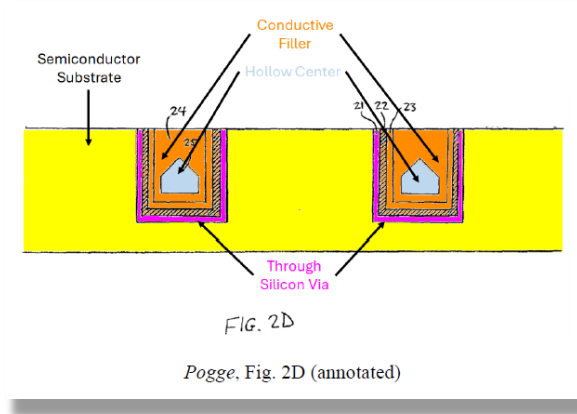
Ex. 1004, FIG. 6

124. **Ground 1B:** To the extent the Patent Owner argues otherwise, a POSITA would have found it obvious to include *Cooney*'s purposeful void 25 to "reduce thermal stress in said semiconductor substrate," in view of the POSITA's knowledge of the state of the art.

Ex. 1002 (Thompson Decl.) ¶ 124

The Knowledge of a POSITA

Pogge and *Edelstein* Disclose Specific Voids That Decrease Thermal Stress



Thompson Decl., ¶¶ 125-131

The Prior Art: Cooney

Pogge and *Edelstein* Disclose Specific Voids That Decrease Thermal Stress

15 Q. Does Cooney state the purpose of the
16 optional void 25 in his apparatus?

17 MR. ZANG: Objection to form.

18 A. By allowing for the optional void,
19 these are well-known -- exceptionally
20 well-known features in the semiconductor
21 processing for tungsten vias. It has different
22 benefits.

23 A POSITA would know that it would
24 reduce stress and other properties, too.

25 Q. But the Cooney reference, Exhibit 4,

2 does not explicitly discuss thermal stress; is
3 that correct?

4 MR. ZANG: Same objection.

5 A. Cooney doesn't use the word
6 "stress," but things that are obvious don't
7 need to be said.

8 A void that's buried obviously
9 reduces stress as the tungsten expand and
10 squashes -- squashes the void and expands
11 inward into the void.

Ex. 2007, Thompson Dep., 30:15-31:11

The Prior Art: Cooney

Cooney Does Not Disclose A Void That Decreases Thermal Stress

The “optional void” in *Cooney* does not anticipate or render obvious any claim for several reasons. First, Petitioner and Dr. Thompson rely on a foundational assumption that all voids in all TSVs reduce thermal stress in the substrate, and this assumption is flatly contradicted by extrinsic evidence. Second, a POSITA would understand that a “void” is different from a hollow center, and is too small to reduce thermal stress. Third, the torpedo shape used to create *Cooney’s* void actually increases thermal stress by requiring additional metal filler and focusing forces on a smaller part of the silicon, as compared to a typical straight TSV.

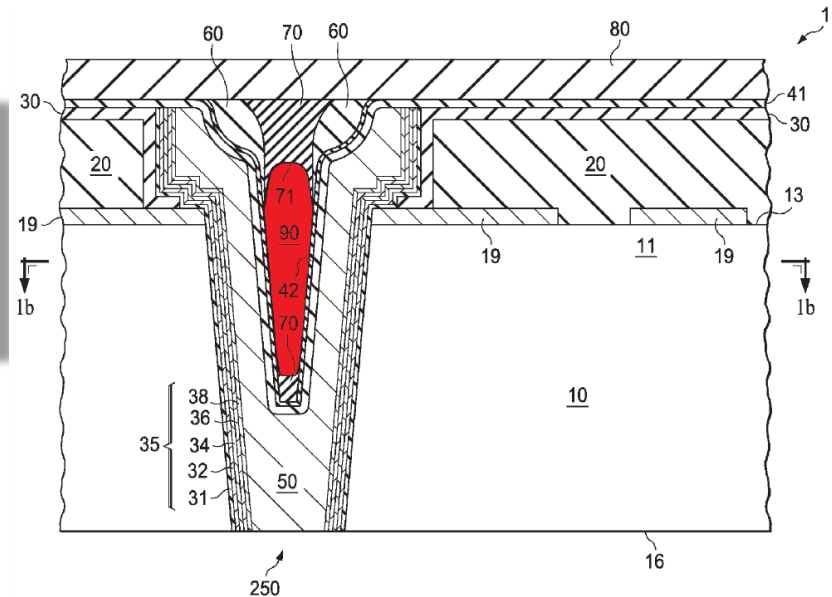
POR at 22.

***Birner* Shows That Hollow Centers Must Be Specifically Designed to Decrease Thermal Stress**

[0037] In various embodiments, the size and shape of the tailored void 90 is adjusted to form a through substrate via with minimum defectivity arising from thermal or other stress related defects. Although, only one through substrate via 1 is illustrated, a through substrate via chip may comprise more than one through substrate via 1.

Birner, Ex. 1022, ¶ 37, Fig. 7d

POR at 23-24.



Hollow Centers Must Be Designed to Decrease Thermal Stress

[0038] As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material 50 is selected relative to the dimension of the tailored void 90. For example, a fraction of the fill material 50 (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1b, this fraction of the fill material 50 (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} . The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material 50 (α_{FM}) and the tailored void (α_V) as $f_{FM} = (\alpha_{Si} - \alpha_V) / (\alpha_{FM} - \alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM} \approx 0$, the fraction $f_{FM} = \alpha_{Si} / \alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening 250 r_{TSV} . In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion.

Birner, Ex. 1022, ¶ 38

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The results of the inelastic thermal stress simulation, the equivalent stress distributions in the cross-sections of the models without and with a void inside the TSVs were shown in Fig. 5. In the case of the TSV structure without voids the stresses in the Cu TSVs were close to the hydrostatic pressure because the equivalent stress has been estimated to be lower than 25 MPa. The magnitude of the equivalent stress was lower than the yield stress of bulk copper which is 230 MPa. It was insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation. In case of the TSV structure with a void the stress-concentration was occurred around the void inside the TSV and the magnitude of the equivalent stress was about 100 MPa. It was larger than the stress obtained for the case of the TSV structure without voids, but it was also lower than the yield stress of the bulk copper. It was also insisted that TSV was not broken by fatigue under thermal cycle condition due to device operation.

Kinoshita, Ex. 2008, at 107
POR at 24-25

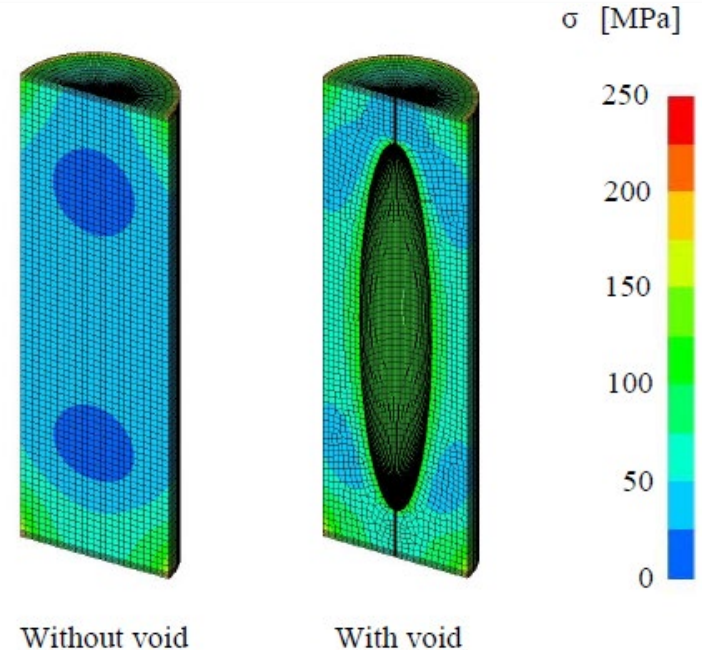


Fig. 5. Equivalent stress distribution of Cu TSV without void (left) and with void (right) at condition of device operation

The Prior Art: Cooney

Cooney's Disclosure is Insufficient

68. In my opinion, Dr. Thompson's analysis of the void in *Cooney* is insufficient. In order to determine whether the optional void in *Cooney* decreases thermal stress in the substrate, Dr. Thompson would have needed to perform *some* analysis of the specific features in *Cooney*, rather than simply relying on the incorrect assumption that all voids decrease thermal stress in the substrate. I do not believe that *Cooney* provides me (or the POSITA) with the information necessary to determine whether the optional void decreases thermal stress, at least because the relative size of the void as compared to the size of the TSV and the size of the liner layer is not given.

The Prior Art: Cooney

Cooney's Void Increases Thermal Stress

71. The optional void in *Cooney* is created by incompletely filling *Cooney's* TSV.³ Ex. 1004, ¶ [0055]. In my opinion, the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV. This is because filling this bulge requires additional metal to fill the TSV. Because there is more metal, it will increase by a greater factor at a given temperature than a straight TSV with less metal. And the torpedo shape itself can increase thermal stresses, by focusing stress on certain portions of the substrate rather than spreading them out along the entire TSV. Dr. Thompson did not analyze the shape of the void in *Cooney*.

Berg Decl., ¶ 71.
POR at 28-29.

The Prior Art: Cooney

The POSITA Would Understand Voids To Be Different From Hollow Centers

The POSITA would have recognized that a “void” in a TSV is typically an artifact of processing caused by incomplete filling of the TSV. Rather than desirable features, voids are typically to be avoided.⁴ Voids, as typically understood by the POSITA, are not large enough to have any appreciable impact on the reduction of thermal stress in the semiconductor substrate. *See Ex. 2011, Low Stress TSV Arrays for High-Density Interconnection*, Jiao et al. at 201-205 (distinguishing a “hollow” TSV from a void). A “void” is different from a hollow center. Aside from the Figure in *Cooney*, *Cooney* does not present any data or information necessary to inform the POSITA as to whether the optional void is large enough to decrease thermal stress in the substrate, and therefore it is my opinion that Dr. Thompson did not have sufficient information on which to base his opinions.

Berg Decl., ¶ 72.
POR at 30-31.

Dr. Thompson's Supplemental Opinion

Attempts To Explain Away *Birner*

Thus, one skilled in the art would have understood *Birner*'s disclosure of “*minimum defectivity* arising from thermal or other stress related *defects*” to mean minimizing of manufacturing defects that may be caused due to thermal or other stresses. *Birner*, ¶ 37 (emphasis added).

Supp. Thompson Decl., ¶ 10.

Dr. Thompson's Supplemental Opinion

Thompson Admits That Void Size Impacts Thermal Stress

13. The term “minimize” means “to reduce or keep to a minimum.”

Ex. 1026, 3. As I explained, the term “minimum” means “the least quantity assignable, admissible, or possible.” Ex. 1026, 3. Further, the term “reduce” means “to diminish in size, amount, extent, or number.” Ex. 1026, 4. Therefore, in my opinion, one skilled in the art would have understood from *Birner* that selecting a void size based on the ratio $\alpha_{SI} / \alpha_{FM}$ may result in diminishing the stress in the substrate to a lowest possible value. A skilled artisan would have understood, however, that nothing in *Birner* discloses or suggests that void sizes not based on

the ratio $\alpha_{SI} / \alpha_{FM}$, do not reduce the thermal stress. Rather, one skilled in the art would have understood that while voids of dimensions different from those based on the ratio $\alpha_{SI} / \alpha_{FM}$ would reduce the thermal stress in the substrate, such thermal stress reduction may not be to the lowest possible value. Indeed, as I discussed above, *Birner* discloses numerous embodiments, in which the presence of voids (without specifying any size or shape) in the metal filled in *Birner*'s TSV, reduces the CTE mismatch between the metal-void combination and the silicon substrate surrounding *Birner*'s TSV, and consequently reduces the stress in the substrate surrounding the TSV. *Birner*, ¶ 24.

Supp. Thompson Decl., ¶ 13.

Dr. Thompson's Supplemental Opinion

Birner Teaches Voids Must Be Designed To Reduce Thermal Stress

In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments, thicker fill material can be used as stress up to a certain critical limit (e.g., critical shear stress) can be safely accommodated. For example, the stress produced during a small increase in temperature may not be significant. Hence, in various embodiments, a numerical simulator is used to design the shape of the voids. In such embodiments, a suitable thickness is calculated numerically to minimize, for example, stress concentrations during subsequent processing. In some embodiments, a more sophisticated analysis utilizing 2D or 3D simulations using finite element simulators determines the appropriate shape and structure of the tailored void 90 relative to the fill material 50. Such numerical calculations can account for changes in stress in different regions, for example, in the corners. Suitable metrics, such as Von Mises criterion, based on the stress tensor may be used to monitor the stress in the structure.

Birner, ¶ 38.

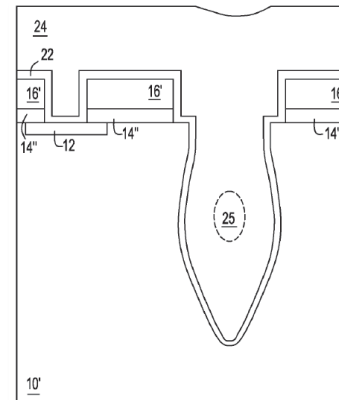
Dr. Thompson's Supplemental Opinion

Kinoshita's Stress is Transferred To The Substrate

16. Mr. Berg relies on Figure 5 of *Kinoshita* and asserts that “the ‘with void’ TSV structure in *Kinoshita* exhibits higher stress levels than the non-voided TSV, including on the edge of the TSV.” Ex. 2012, ¶¶ 52, 67. In my opinion, Mr. Berg’s argument regarding the stress level in the TSV is irrelevant. This is because claim 1 of the ’609 patent recites “hollow center to reduce thermal stress in said semiconductor substrate” (Ex. 1001, 6:4-10, emphasis added); claim 1 does not recite stress in the TSV. Thus, Mr. Berg’s analysis of the stress levels in the TSV of *Kinoshita* is wholly irrelevant to determining whether the void in *Kinoshita*’s TSV decreases stress in the surrounding substrate.

Supp. Thompson Decl., ¶ 16.

Ex. 1002 (Thompson Decl.) ¶ 123
Sur-Reply at 5-6.

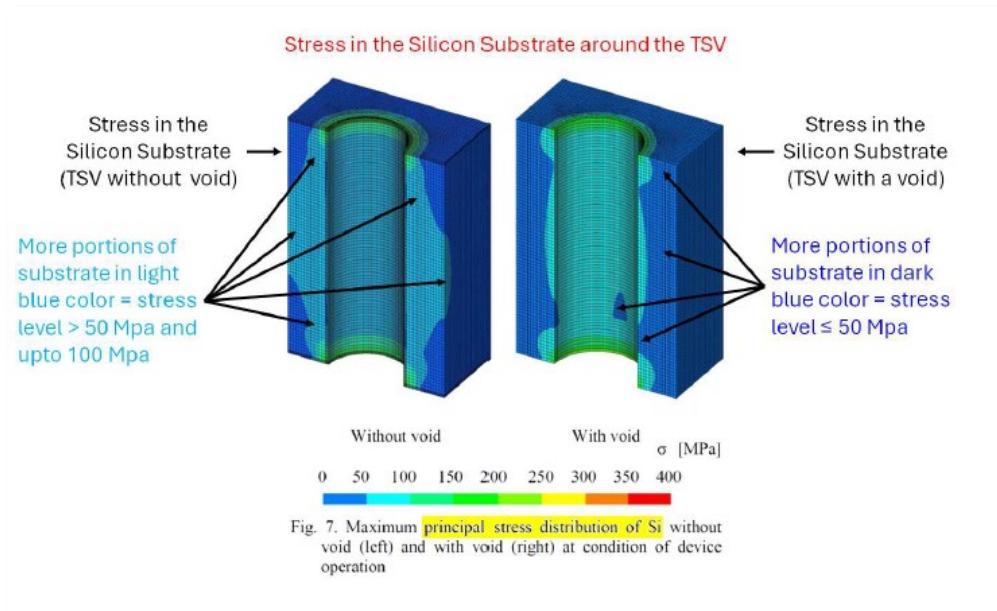


Ex. 1004, FIG. 6 FIG. 6

123. **Ground 1A:** Because *Cooney* discloses the presence of the hollow center or void 25, it is my opinion that *Cooney*’s void 25 reduces thermal stress in *Cooney*’s substrate. The ’609 patent does not identify any characteristics or properties of the hollow center that contribute to thermal stress reduction in the semiconductor substrate. Ex. 1001, 4:60-61; *see generally* Ex. 1001. In my

Dr. Thompson's Supplemental Opinion

Kinoshita Figure 7 Supports Patent Owner's Position

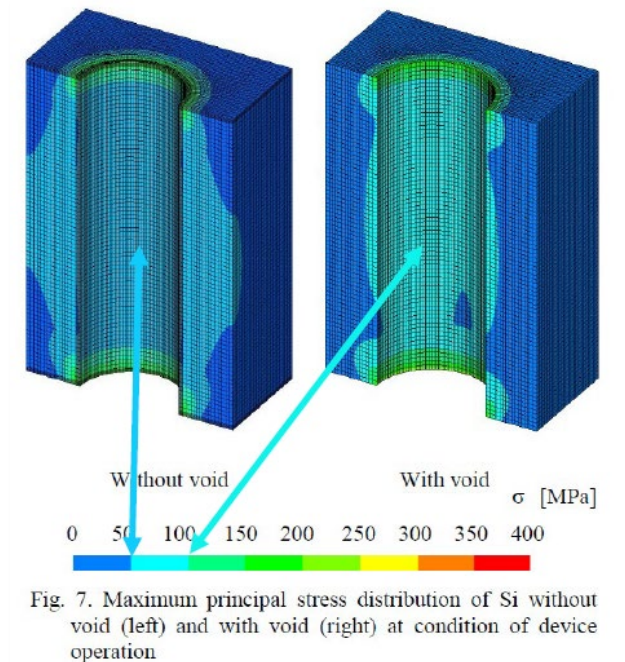


Supp. Thompson Decl., ¶ 18.

Sur-Reply at 6-7.

Dr. Thompson's Supplemental Opinion

Kinoshita Figure 7 Supports Patent Owner's Position



Sur-Reply, Paper 22, at 8

Dr. Thompson's Supplemental Opinion

Untimely Analysis of Cooney Is Wrong and Does Not Account for Torpedo Shape

31. Although not required by the claims, in my opinion *Cooney's* void size can be about the same as *Birner's* and *Kinoshita's*: 14 μm . For example, *Cooney* discloses that its region R1 has a linewidth of 3-50 μm , region R2 has a linewidth of 1-35 μm , and region R3 has a linewidth of 3-50 μm . *Cooney*, ¶ 51. *Cooney* also discloses that the linewidth of region R1 is preferably from 1.3 to 1.5 times that of region R4. *Id.*, ¶ 54. Thus, one skilled in the art would understand that when region R1 has a linewidth of 50 μm , the linewidth of region R4 would be about 35.7 μm ($=50/1.4$). *Cooney* also discloses that the linewidth of region R4 is preferably 0.1 to 2 times a deposition thickness of the conductor layer. *Cooney*,

¶ 54. Thus, one skilled in the art would understand that if the conductor layer is fully filled in region R4, the thickness of the conductor layer on either side of the void (namely the deposition thickness) in region R3 would be $R4/2$ ($= 35.7/2 = 18$ μm). Based on these disclosures, a skilled artisan would have further understood that the void diameter in *Cooney* in a region R3 having linewidth 50 μm would be about 14 μm ($= 50 - 18 - 18$) because 18 μm of thickness on either side of the void would be filled with the conductor layer. Thus, a person of ordinary skill in the art would have understood *Cooney* as disclosing void diameters of the same order of magnitude as disclosed in *Birner* and *Kinoshita*. And as I explained in my opening declaration, *Cooney's* void would also reduce thermal stress just like the voids in *Birner*, *Pogge*, *Edelstein*, and *Kinoshita*. Ex. 1002, ¶¶ 47-49, 125-131, 141-145.

Dr. Thompson's Supplemental Opinion

Use of Relative Linewidths Improper

torpedo shape or the void itself. There is simply no disclosure of the size of the “optional void” in *Cooney*, nor is there any disclosure of that void reducing thermal stress in the substrate. Dr. Thompson, aside from improperly calculating the size of the void in *Cooney*, does not analyze any other characteristic of *Cooney's* void (or the non-standard shape of the TSV itself) to conclude that it reduces thermal stress. *Id.*, ¶¶ 28–34. On this record, Petitioner cannot show that *Cooney's* void decreases thermal stress in the substrate.

Sur-Reply at 16

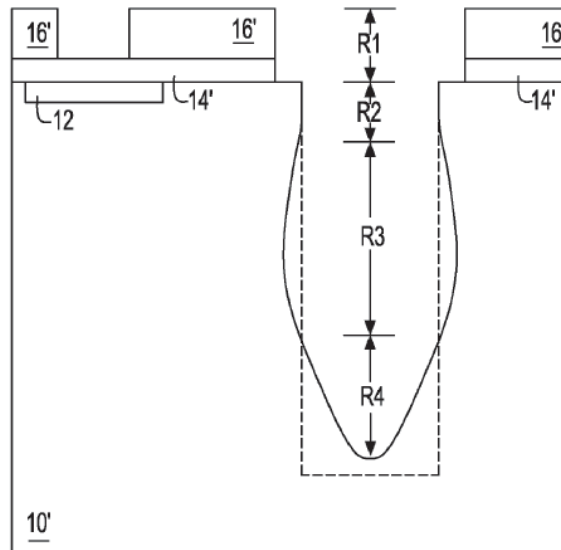


FIG. 5