

Petitioner's Demonstratives

Samsung Electronics Co., Ltd., and Samsung
Electronics America, Inc.

Petitioner

v.

Harbor Island Dynamic, LLC

Patent Owner

IPR2024-01404 - Patent No. 9,147,609

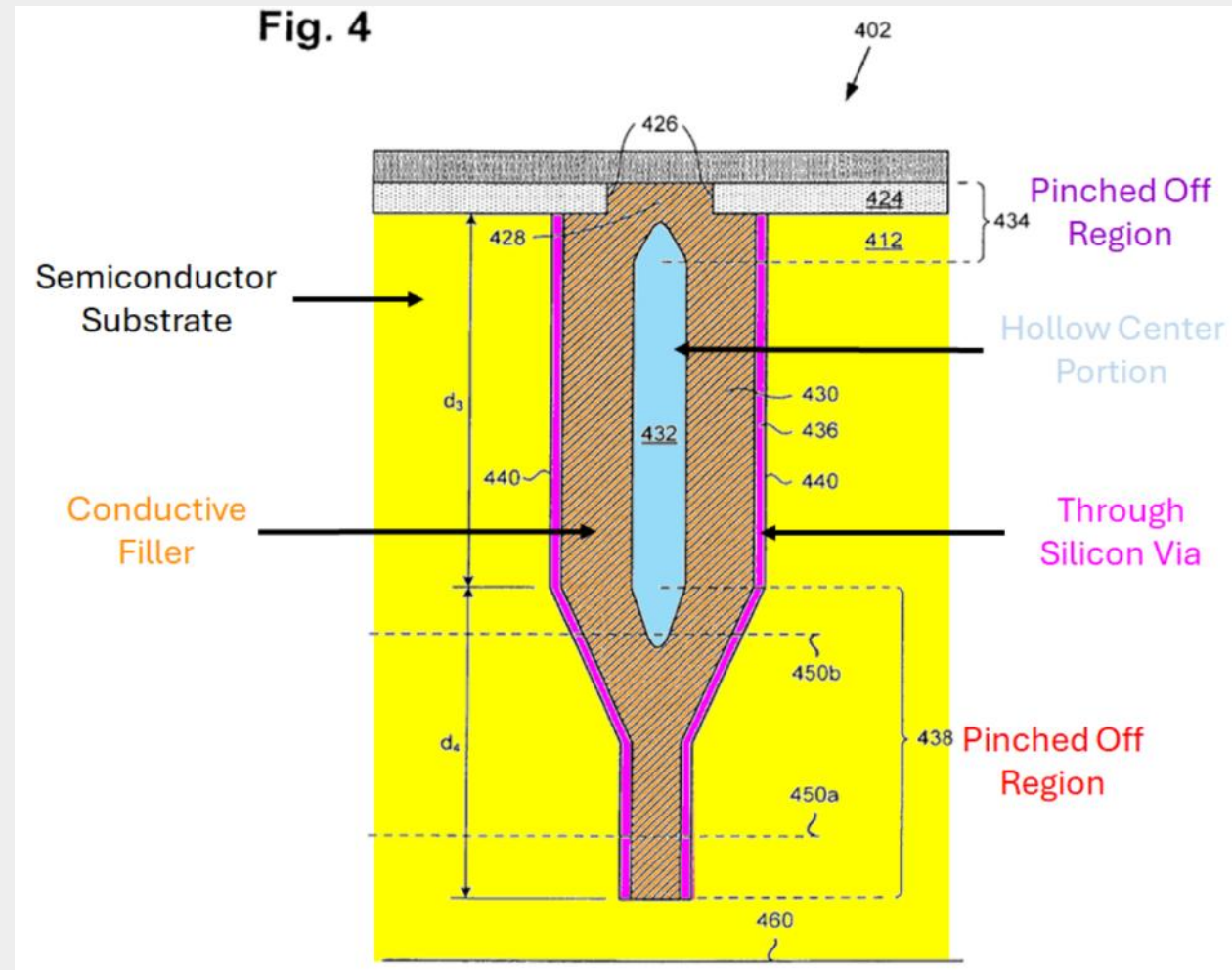
Instituted Grounds

- Claims 1-18 of the '609 patent are challenged:
 - Claims 1-10: A semiconductor substrate . . ., comprising
 - Claims 11-18: A semiconductor substrate . . ., comprising

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 9–14, 17, 18	102	Cooney
1–6, 9–14, 17, 18	103	Cooney
7, 15	103	Cooney, Dean
8, 16	103	Cooney, Farooq
8, 16	103	Che, Cooney

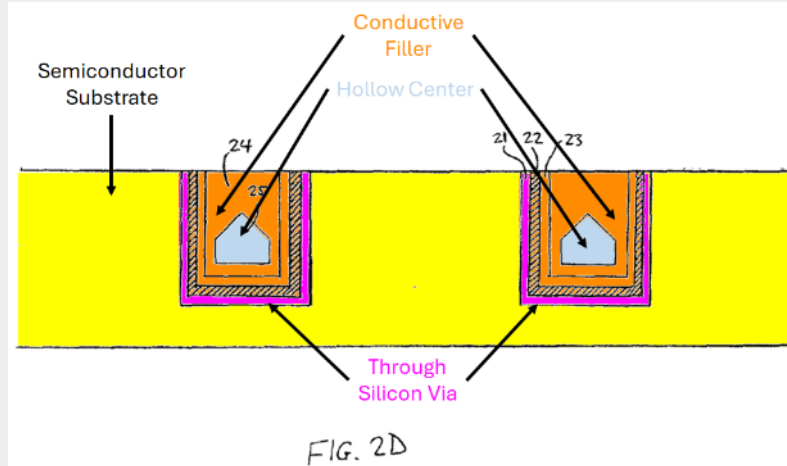
The '609 Patent's Alleged Invention:

Alleged Invention – **Hollow Center** to Reduce Thermal Stress in the Substrate

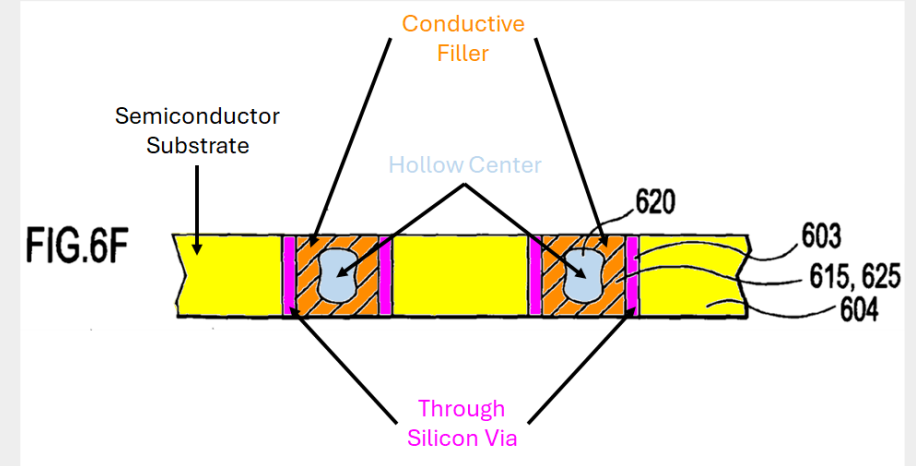


TSV Voids to Reduce Thermal Stress Well-Known in the Art

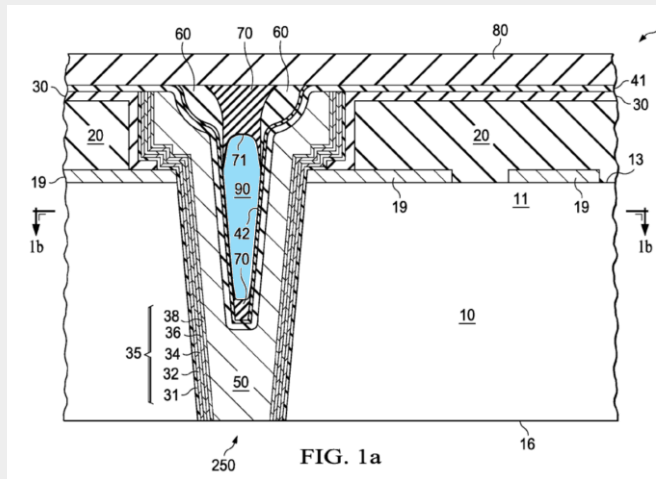
Pogge (2003)



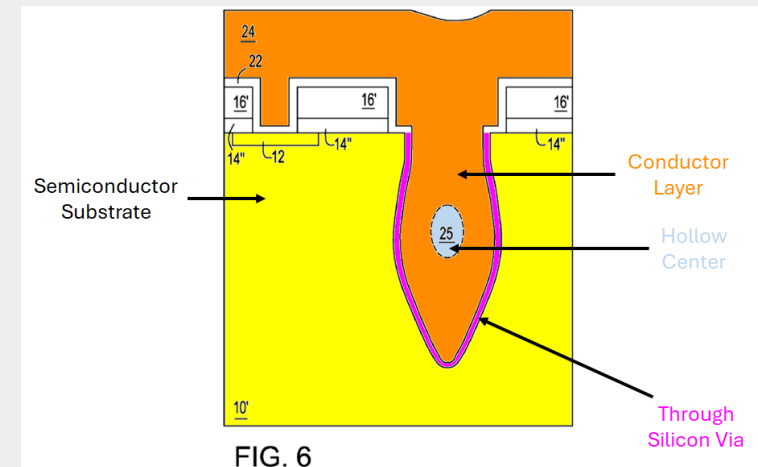
Edelstein (2006)



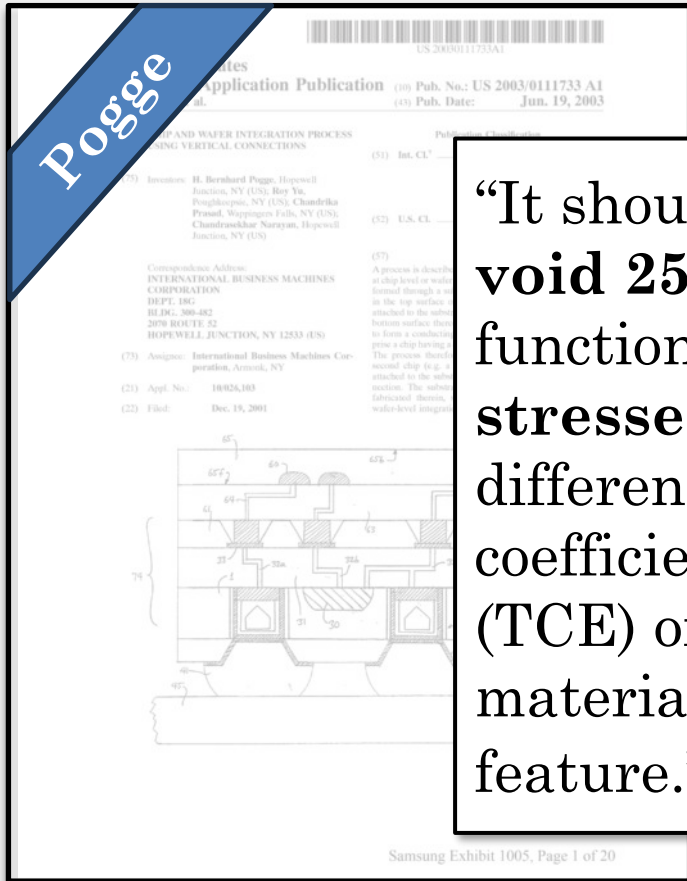
Birner (2009)



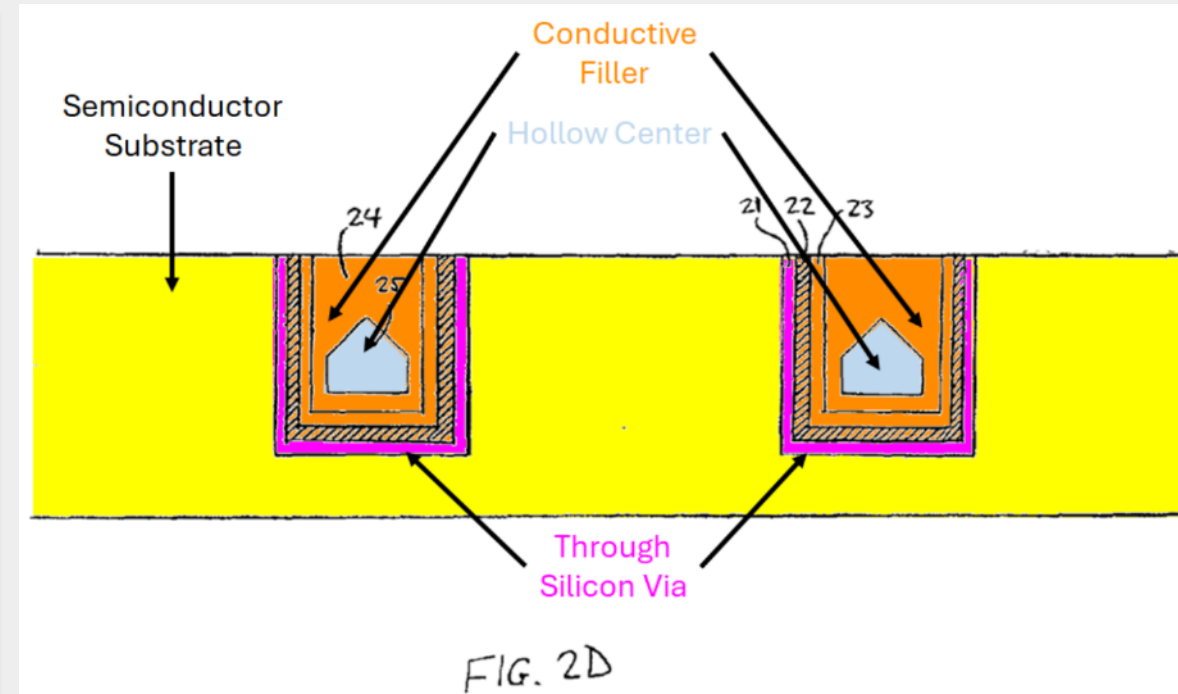
Cooney (2009)



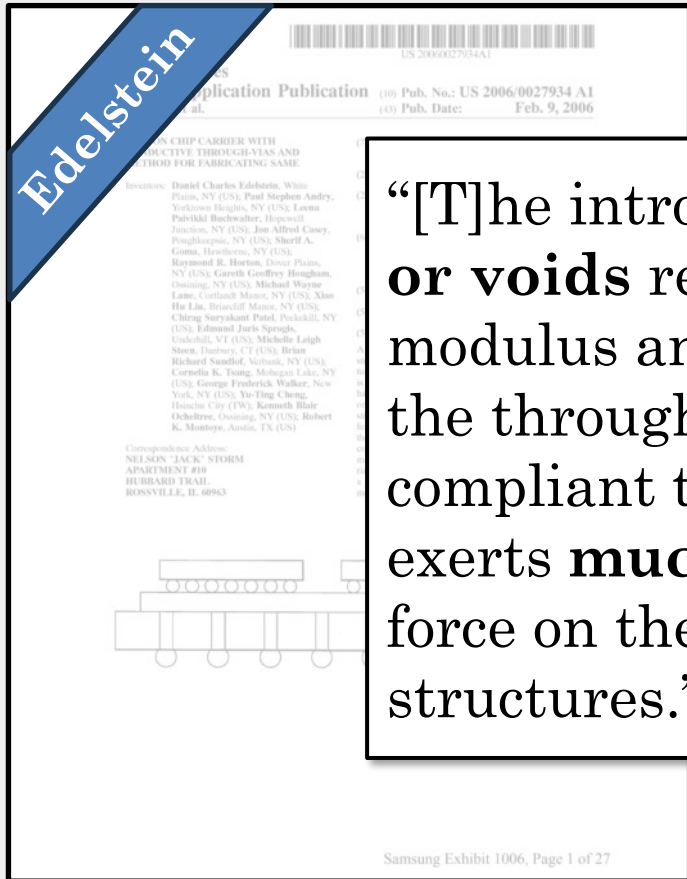
The Problem Faced By the '609 Patent Was Well-Known in the Art



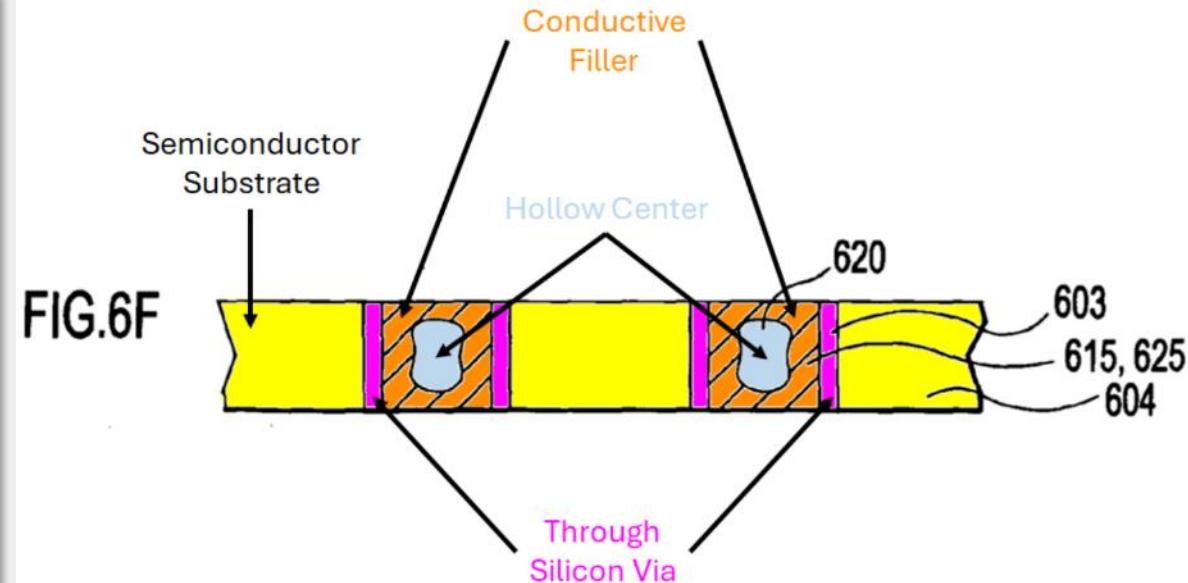
“It should be noted that the **void 25** has an important function in **relieving stresses** caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature.” *Pogge*, ¶ [0027].



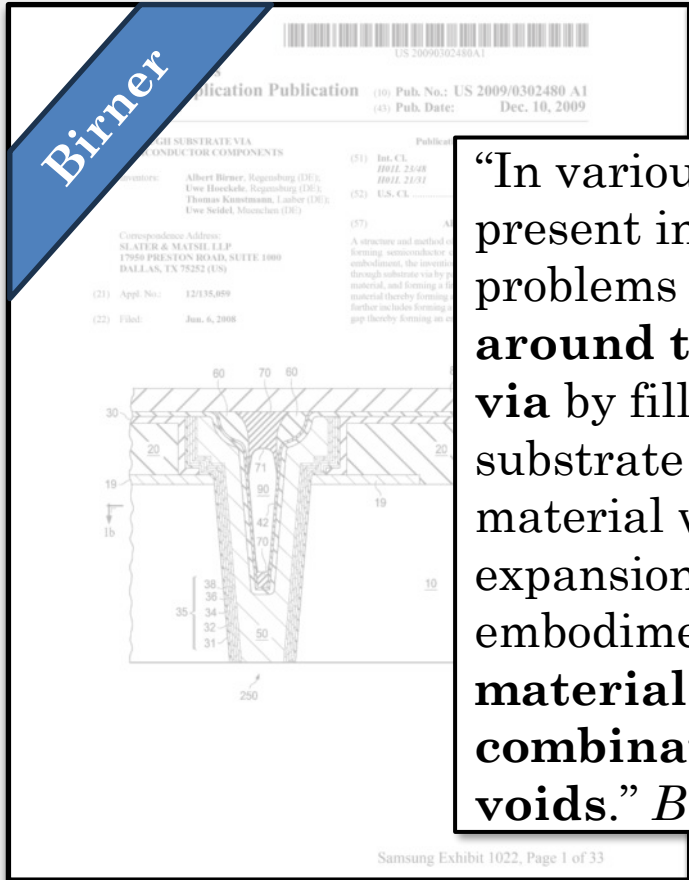
The Problem Faced By the '609 Patent Was Well-Known in the Art



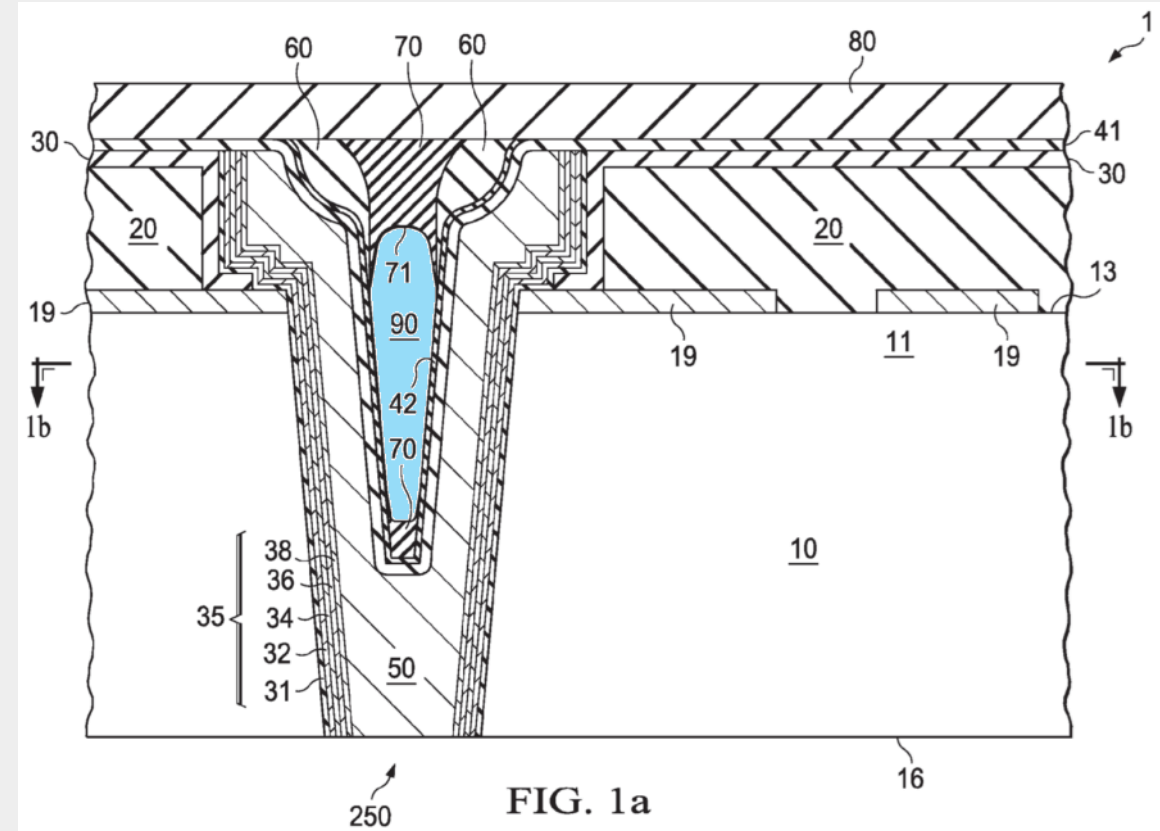
“[T]he introduction of a **void** or **voids** reduces the effective modulus and Poisson ratio of the through-via, resulting in a compliant through-via that exerts **much less stress** and force on the surrounding structures.” *Edelstein*, ¶ [0047].



The Problem Faced By the '609 Patent Was Well-Known in the Art



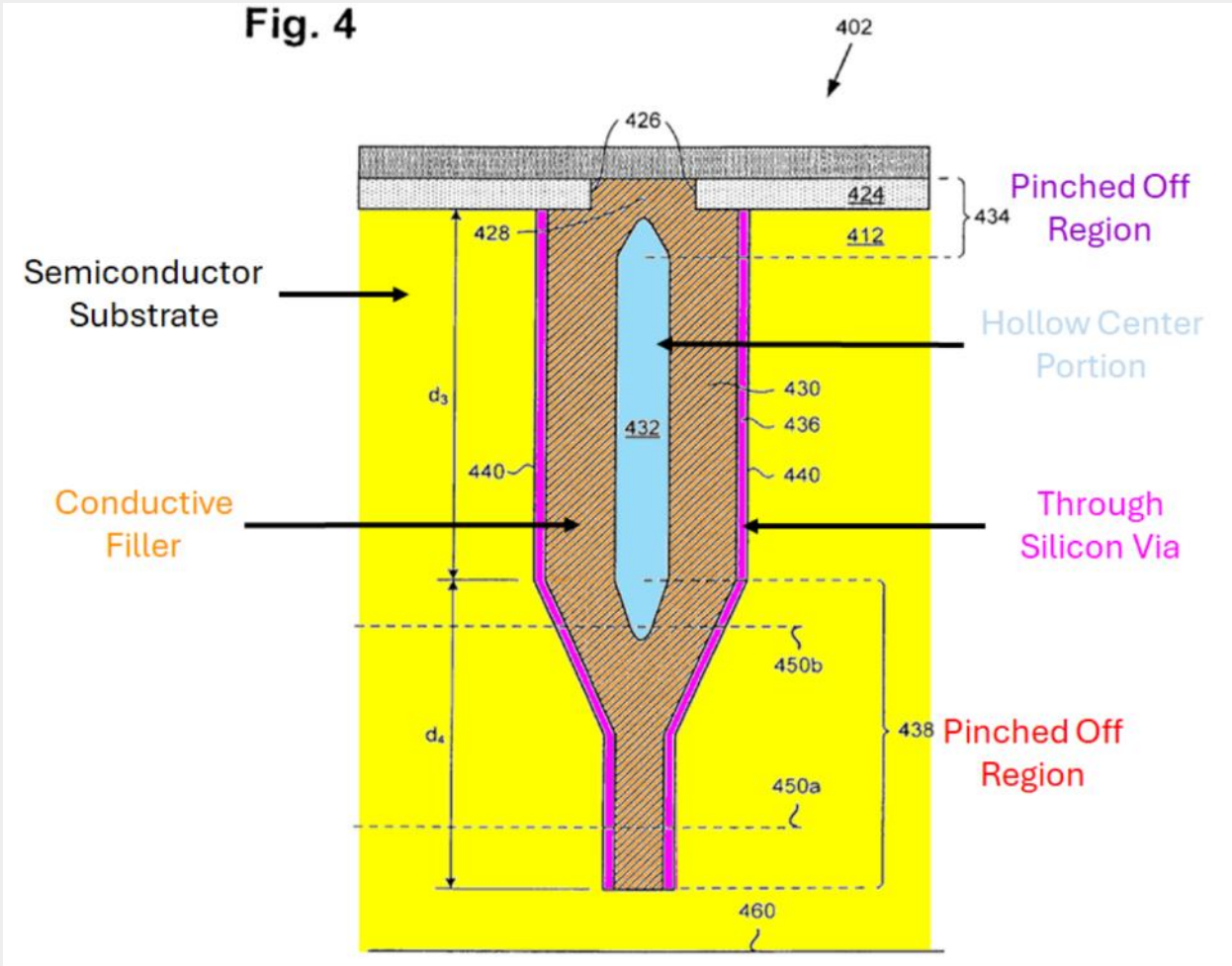
“In various embodiments, the present invention overcomes these problems by **reducing stress around the through substrate via** by filling the through substrate via with an effective material with minimal thermal expansion. In various embodiments, the **effective material comprises a combination of metal and voids.**” *Birner*, ¶ [0024].



Cooney Provides the Same TSV Structure as the '609 Patent

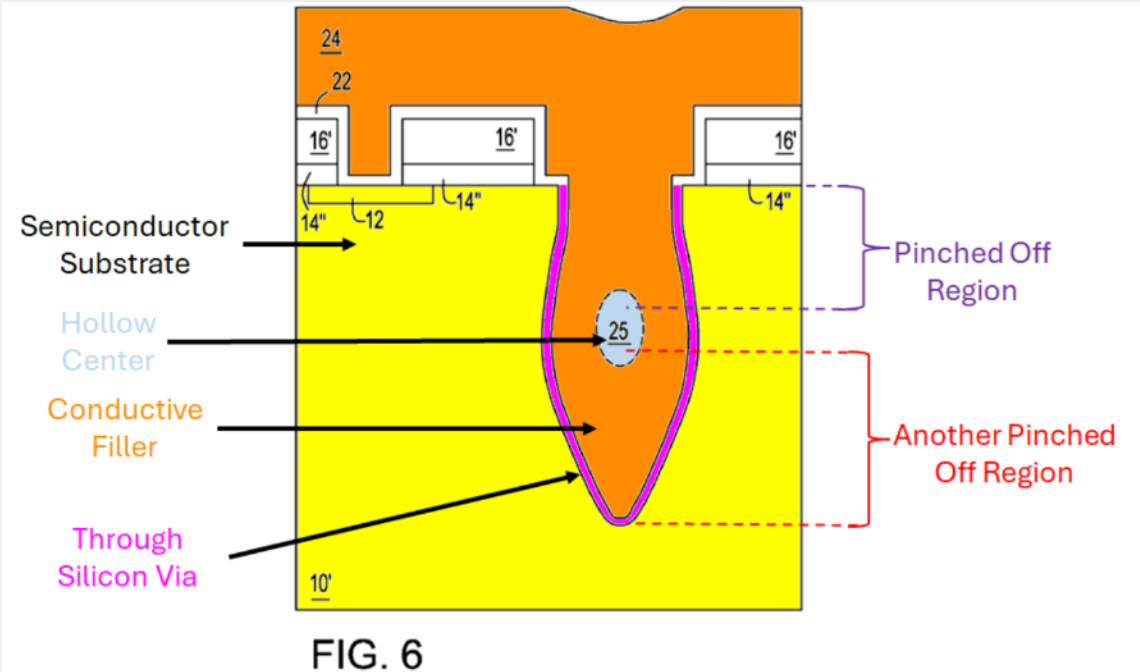
Purported Invention of the '609 Patent

Fig. 4



Pet., 3; '609 Patent, Fig. 4 (annotated)

Cooney (Ex. 1004)



Pet., 54, Cooney, Fig. 6 (annotated)

Cooney Provides the Same TSV Structure as the '609 Patent

Purported Invention of the '609 Patent

The '609 Patent (Ex. 1001) is titled "Through Silicon Via Structure, Method of Formation, and Integration in Semiconductor Substrate" and issued on September 29, 2015. The '609 Patent relates to through silicon vias (TSVs) having pinched off regions. '609 Patent, Abstract, 1:54-59, 4:9-15. In particular, the '609 Patent teaches manufacturing TSVs with hollow centers. *Id.*, 4:47-59. The pinched off regions and hollow centers provide significant advantages, such as reducing the TSV's inductance, and reducing thermal and mechanical stresses. *Id.* 4:60-5:2.

(POPR, 2; POR, 3)

Cooney (Ex. 1004)

[0065] FIG. 10 shows a schematic cross-sectional diagram of a semiconductor structure in accordance with a particular embodiment of the invention that comprises a first and sole preferred embodiment of the invention. The semiconductor structure includes a through substrate via 24" that penetrates from a front side of a semiconductor substrate 10" to a back-side of the semiconductor substrate 10". The through substrate via 24" is located and formed into an aperture within the semiconductor substrate 10" of FIG. 10 that has an irregular sidewall profile. Progressing from the top surface to the bot-

Cooney, [0065] (Pet., 11, 16)

[0055] FIG. 6 shows a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture. FIG. 6 also shows a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.

Cooney, [0055] (Pet., 11, 15, 17, 19, 23, 29, 35)

Overview of Claim 1

- [1pre] A semiconductor substrate having a plurality of devices, said semiconductor substrate comprising:
- [1a] a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate;
 - [1b-1] a conductive filler disposed within each of said plurality of through silicon vias,
 - [1b-2] each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,
 - [1b-3] said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward,
 - [1c-1] wherein each of said plurality of through silicon vias has a pinched off region at a bottom portion to prevent contamination during processing of said semiconductor substrate;
 - [1c-2] wherein said hollow center is tapered in said pinched off region.

Cooney Discloses Claim [1pre] (Undisputed)

“A **semiconductor substrate** having a plurality of **devices**, said semiconductor substrate comprising,”

[0026] FIG. 1 shows a **semiconductor substrate 10** that includes a contact region **12** located within the semiconductor substrate **10**. An etch stop layer **14** is located upon the semi-

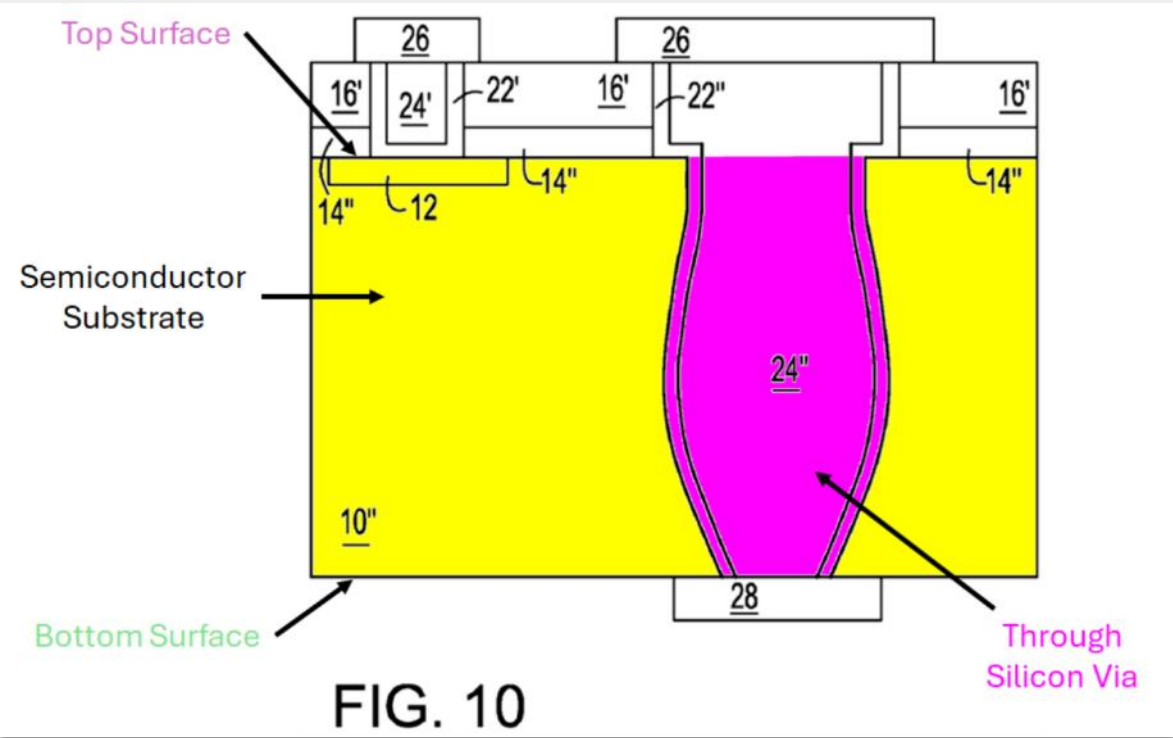
Pet. 15; Cooney, ¶ [0026]; Thompson Decl. ¶ 111

[0032] Although the instant embodiment illustrates the invention within the context of the **semiconductor substrate 10** including the contact region **12**, the embodiment is also not specifically limited to only a contact region within a semiconductor substrate. Rather, the embodiment also contemplates that the **semiconductor substrate 10** will also include located and formed therein semiconductor devices that are appropriate for a semiconductor circuit which is intended to be fabricated within and upon the **semiconductor substrate 10**. Such semiconductor devices may include, but are not necessarily limited to, resistors, transistors, diodes and capacitors.

Pet. 15; Cooney, ¶ [0032]; Thompson Decl. ¶ 111

Cooney Discloses Claim [1a] (Undisputed)

“a plurality of through silicon vias disposed in said substrate extending from a top surface of said substrate to a bottom surface of said substrate,”



Pet. 17, Cooney, Fig. 10

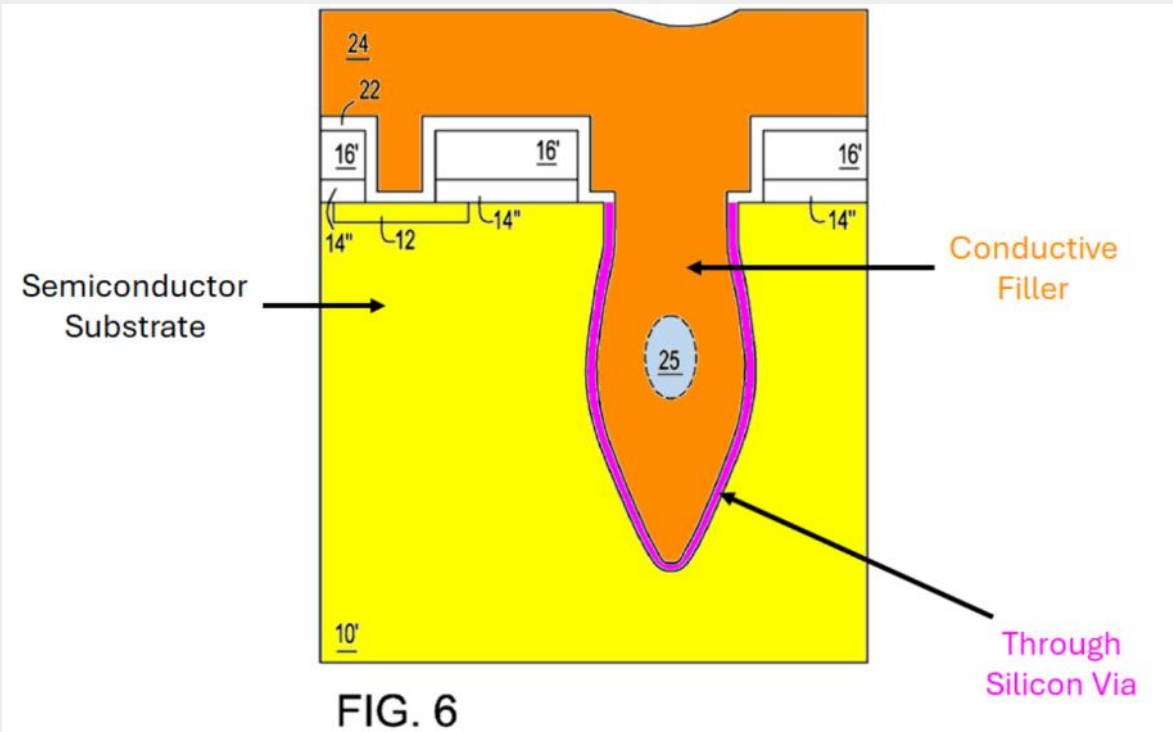
[0065] FIG. 10 shows a schematic cross-sectional diagram of a semiconductor structure in accordance with a particular embodiment of the invention that comprises a first and sole preferred embodiment of the invention. The semiconductor structure includes a through substrate via 24'' that penetrates from a front side of a semiconductor substrate 10'' to a back-side of the semiconductor substrate 10''. The through sub-
Pet. 16; Cooney, ¶ [0065]; Thompson Decl. ¶ 113

[0066] Within this particular sole preferred embodiment, the first comparatively wide region of the aperture aids in efficiently filling the aperture with the through substrate via 24''. The constricted region provides for surface closure of any voids that may form in the second comparatively wide region. The second comparatively wide region, due to the increase in linewidth thereof, provides for ease in filling the aperture. Finally, the inward tapered region allows for ease in filling at least a bottom portion of the aperture absent forming a void within the via that is filled into the aperture. While the instant embodiment illustrates the invention within the context of a single aperture and through substrate via 24'' within a semiconductor substrate, a multiplicity of dimensionally similar or dimensionally identical apertures and corresponding vias may also be used within a single substrate, such as a single semiconductor substrate.

Pet. 16; Cooney, ¶ [0066]; Thompson Decl. ¶ 115

Cooney Discloses Claim [1b-1] (Undisputed)

“a **conductive filler** disposed within each of said plurality of **through silicon vias**,”



Pet. 18; Cooney, Fig. 6

[0055] FIG. 6 shows a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture. FIG. 6 also shows a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.

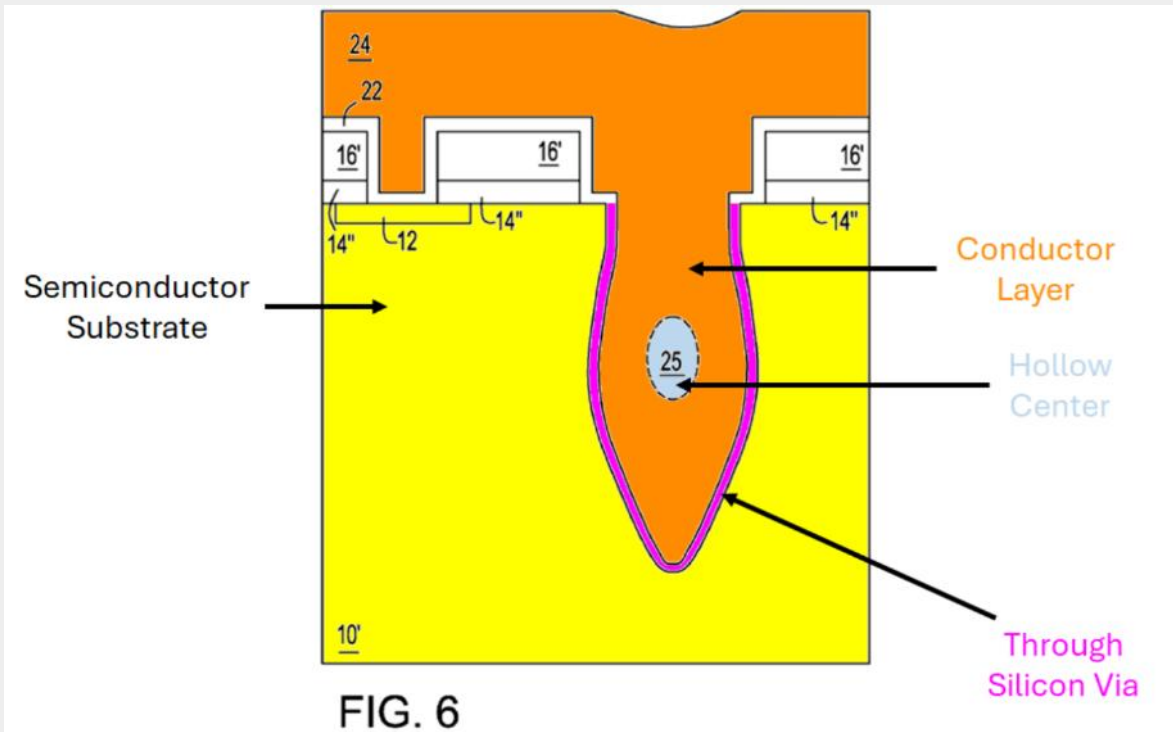
Pet. 17; Cooney, ¶ [0055]; Thompson Decl. ¶ 117

[0059] The conductor layer 24 comprises a conductor material. While in accordance with disclosure above the conductor layer 24 may comprise any of several conductor materials, including but not limited to any of several metals and metal alloys, the conductor layer 24 typically comprises a tungsten material. Such a tungsten material is preferably deposited using a chemical vapor deposition method, although neither the embodiment nor the invention is so limited.

Pet. 18; Cooney, ¶ [0059]; Thompson Decl. ¶ 118

Cooney Discloses Claim [1b-2]

“each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”



Pet. 19; Cooney, Fig. 6

[0055] FIG. 6 shows a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture. FIG. 6 also shows a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.

Pet. 19; Cooney, ¶ [0055]; Thompson Decl. ¶ 121

[0060] As is illustrated by the phantom line enclosure within the schematic diagram of FIG. 6, the conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.

Pet. 19; Cooney, ¶ [0060]; Thompson Decl. ¶ 121

Cooney Discloses Claim [1b-2]

“each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”

The phrase “to reduce thermal stress in said semiconductor substrate” states the use of or explanation for the hollow center and should be entitled to no patentable weight over the prior art. *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999) (holding that “a scientific explanation for the prior art’s functioning, does not render the old composition patentably new”); *In re Sinex*, 309 F.2d 488, 492 (C.C.P.A. 1962) (“The expression ‘for reconcentrating liquid dehydrating agents’ is merely a statement of intended use and does not qualify or distinguish the structural apparatus claimed over the reference.”); *Arctic Cat Inc. v. GEP Power Prods., Inc.*, 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“[T]he recitation of a new intended use for an old product does not make a claim to that old product patentable.”). Other than disclosing the presence of a hollow center in the TSV, the ’609 patent does not identify any features of the hollow center that contribute to thermal stress reduction in the semiconductor substrate. See generally ’609 patent. Thompson, ¶123. This failing further supports the conclusion that this claim language should be entitled to no patentable weight over the prior art.

Pet. 20; Thompson Decl. ¶ 123

Cooney Discloses Claim [1b-2]



Atlas Powder Co. v. Ireco, Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999) (“Artisans of ordinary skill may not recognize the inherent characteristics or functioning of the prior art. []However, the discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discoverer.”)



In re Sinex, 309 F.2d 488, 492 (C.C.P.A. 1962) (“Resolution of these four objections of appellant will determine whether the board was correct in finding appellant’s invention to be obvious over the Harris patent. For the reasons hereinafter stated, we think the board was correct. (a) The expression ‘for reconcentrating liquid dehydrating agents’ is merely a statement of intended use and does not qualify or distinguish the structural apparatus claimed over the reference.”)



Arctic Cat Inc. v. GEP Power Prods., Inc., 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“That rule is grounded in the statutory distinction, in identifying the permissible subject matter of a patent claim, between a physical product (which may be defined in part by its claimed functional capabilities) and activities that constitute a process (which may include a new "use" of a known invention).”)

Cooney Renders Obvious Claim [1b-2]

“each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”

Thompson, ¶123. And at a minimum, a POSITA would have found it obvious to include Cooney’s void 25 to “reduce thermal stress in said semiconductor substrate,” as recited in limitation [1b-2], based on the POSITA’s knowledge of the state of the art. *KSR Int’l. Co. v. Teleflex, Inc.*, 550 U.S. 398, 420-21 (2007) (“A

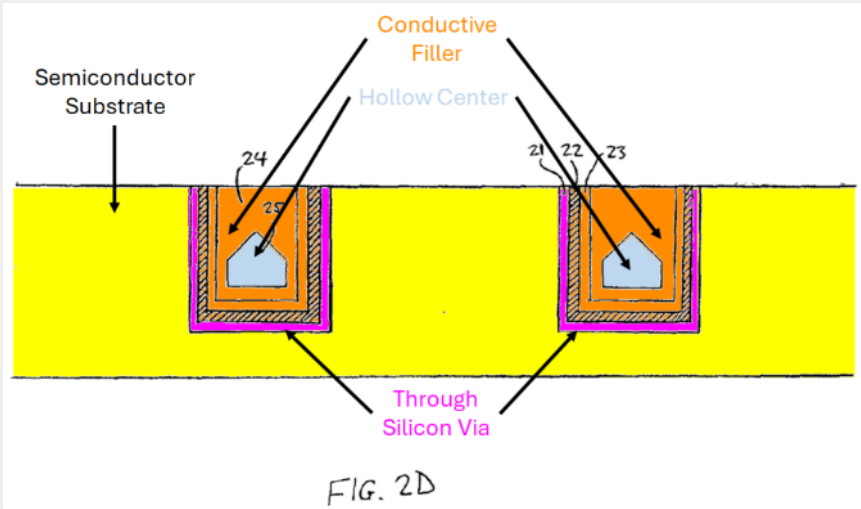
Pet. 21; Thompson Decl. ¶ 124

Thompson, ¶124. As Dr. Thompson explains, it was well known that the presence of a void in a filled TSV results in a lower amount of thermal stress in the surrounding substrate. Thompson , ¶125. For example, Pogge discloses that a void

Pet. 21; Thompson Decl. ¶¶ 125-131

[0027] A layer 24 of copper is formed on layer 23 (e.g. by electroplating) in the trench and on top of the wafer. Layer 24 is built up on the sidewalls of the trench until it reaches a thickness such that the upper part of the trench is closed, as shown in FIG. 2C. With this structure, a conducting path is established between the bottom of the trench and the top surface of the wafer, while a void 25 remains near the bottom of the trench. It should be noted that the void 25 has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature.

Pet. 21; Pogge, ¶ [0027]; Thompson Decl. ¶¶ 126-127

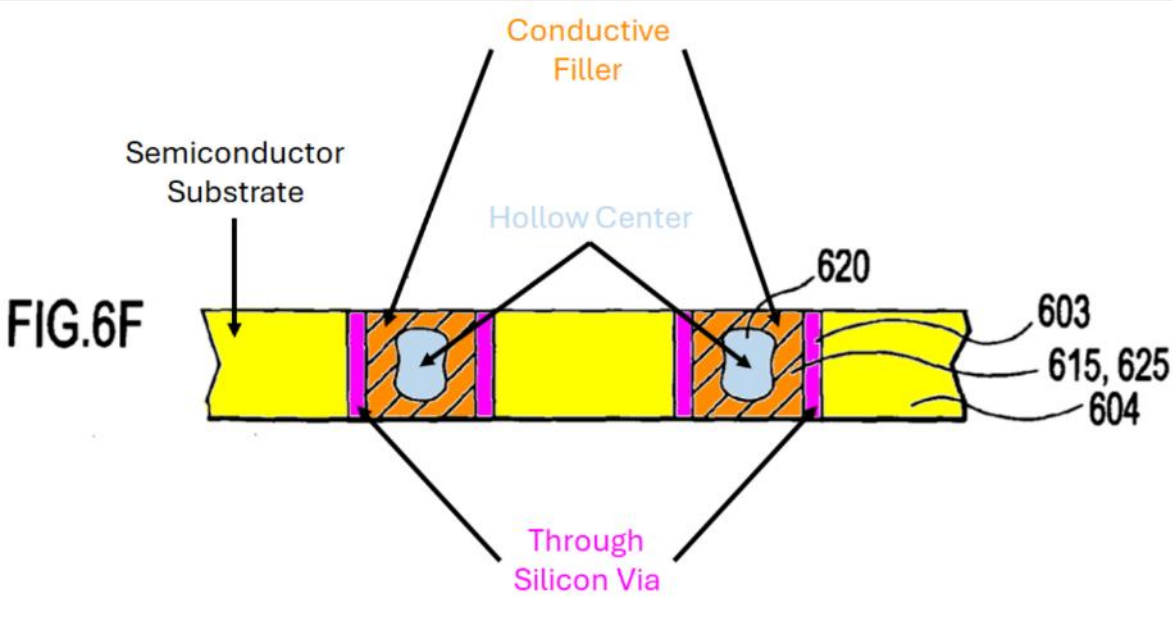


Pogge, Fig. 2D, Thompson Dec. ¶ 126

Cooney Renders Obvious Claim [1b-2]

“each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”

[0047] The structure of FIG. 2B comprises a substrate 224 in which the through-via comprises an annular ring of insulating material 223 within which is disposed a conductive via of metal (e.g., copper) 225 having a void 220 at its core. The top and bottom surfaces of the through-via are copper, and copper covers the insulated sidewalls of the through-via. However, a void filled with a gas such as air, an inert gas, or N₂, or alternatively a vacuum, is disposed at the center of the through-via and provides an effective modulus which is more nearly matched to the substrate 224. The through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures. The effective Poisson ratio here is defined as the ratio of out-of-plane displacement to in-plane displacement due to in-plane stress to reduce mechanical stresses encountered in processing and use. For a through-



Edelstein, Fig. 6F; Thompson Decl. ¶ 128

Pet. 21; Edelstein, ¶ [0047]; Thompson Decl. ¶¶ 128-131

Cooney Renders Obvious Claim [1b-2]

“each of said plurality of through silicon vias having a hollow center to reduce thermal stress in said semiconductor substrate,”

Thompson, ¶123. And at a minimum, a POSITA would have found it obvious to include *Cooney*’s void 25 to “reduce thermal stress in said semiconductor substrate,” as recited in limitation [1b-2], based on the POSITA’s knowledge of the state of the art. *KSR Int’l. Co. v. Teleflex, Inc.*, 550 U.S. 398, 420-21 (2007) (“A

Pet. 21; Thompson Decl. ¶ 124

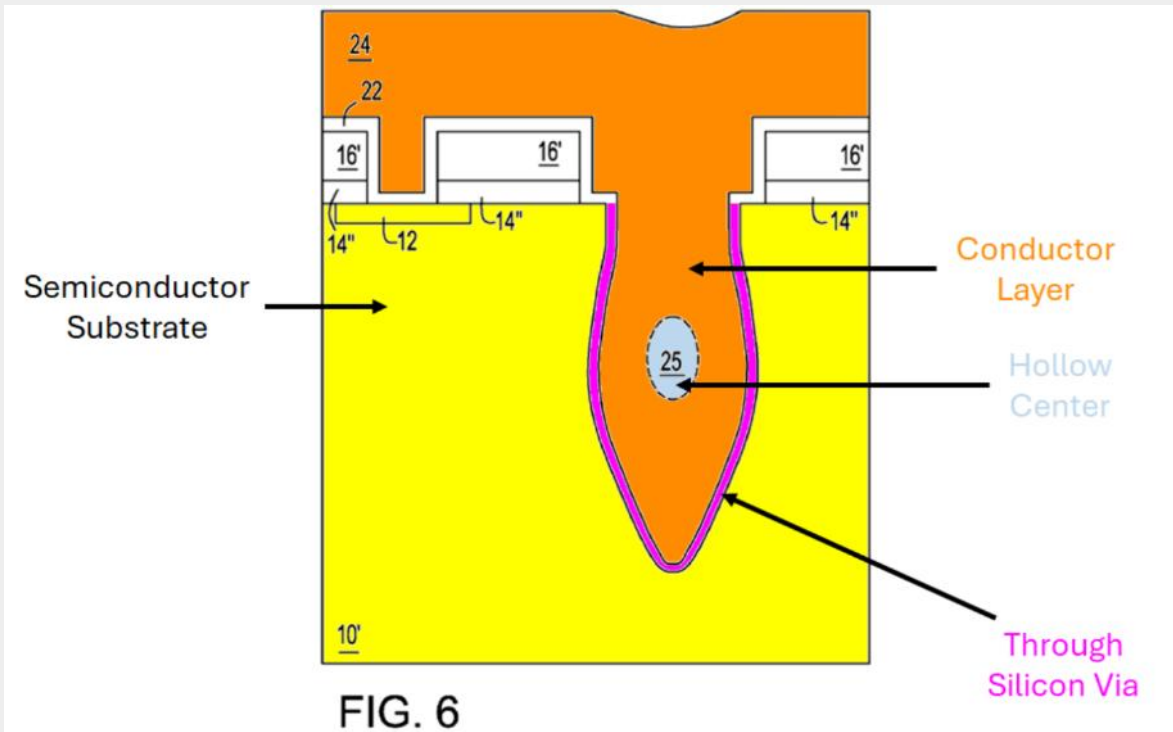
Pet. 21-22; Thompson Decl. ¶¶ 131, 133

131. A POSITA would have been aware of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials before the earliest priority date of the ’609 patent as evidenced by the disclosures of *Pogge* and *Edelstein*. In my opinion, a POSITA would have found it obvious that *Cooney*’s TSV with a void enclosed in the conductor layer would also cause a reduction in the thermal stress in the surrounding substrate consistent with the voids in *Pogge* and *Edelstein*.

133. In view of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*’s TSV to cause a reduction in the thermal stress in the surrounding substrate. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including the void.

Cooney Discloses Claim [1b-3] (Undisputed)

“said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward,”



Pet. 23; Cooney, Fig. 6; Thompson Decl. ¶ 137

[0055] FIG. 6 shows a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture. FIG. 6 also shows a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.

Pet. 23; Cooney, ¶ [0055]; Thompson Decl. ¶ 136

[0051] Within the instant embodiment, the comparatively wide linewidth of the first region R1, the comparatively wide linewidth of the third region R3 and the inward pointed taper of the fourth region R4 in general are intended to provide for ease in filling the extended aperture. In addition, the constriction within the second region R2 is intended to completely seal off any void that may form within the third region R3, and to localize that void to the third region R3.

Pet. 23-24; Cooney, ¶ [0051]; Thompson Decl. ¶ 137

Cooney Discloses Claim [1b-3] (Undisputed)

“said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward,”

The phrase “to provide space for said conductive filler to expand inward” states another use for the functioning of the hollow center and should be entitled to no patentable weight over the prior art. *Atlas Powder*, 190 F.3d at 1347; *Sinex*, 309 F.2d at 492; *Arctic Cat*, 919 F.3d at 1328. Again, other than disclosing the presence of a hollow center in the TSV, the ’609 patent does not identify any features of the hollow center in the TSV that purportedly allows the conductive filler in the TSV to expand inward. *See generally* ’609 patent. Thompson, ¶139. Thus, the patent itself recognizes that this functional language should not be entitled to patentable weight.

Pet. 24-25; Thompson Dec. ¶ 139

Cooney Discloses Claim [1b-3] (Undisputed)



Atlas Powder Co. v. Ireco, Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999) (“Artisans of ordinary skill may not recognize the inherent characteristics or functioning of the prior art. []However, the discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discoverer.”)



In re Sinex, 309 F.2d 488, 492 (C.C.P.A. 1962) (“Resolution of these four objections of appellant will determine whether the board was correct in finding appellant’s invention to be obvious over the Harris patent. For the reasons hereinafter stated, we think the board was correct. (a) The expression ‘for reconcentrating liquid dehydrating agents’ is merely a statement of intended use and does not qualify or distinguish the structural apparatus claimed over the reference.”)



Arctic Cat Inc. v. GEP Power Prods., Inc., 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“That rule is grounded in the statutory distinction, in identifying the permissible subject matter of a patent claim, between a physical product (which may be defined in part by its claimed functional capabilities) and activities that constitute a process (which may include a new "use" of a known invention).”)

Cooney Renders Obvious Claim [1b-3] (Undisputed)

“said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward,”

¶139. And even if HID were to contend otherwise, a POSITA would have found it obvious to include *Cooney*’s void 25 to “provide space for said conductive filler to expand inward,” as recited in limitation [1b-3], based on the POSITA’s knowledge of the state of the art. *KSR*, 550 U.S. at 420-21; Thompson, ¶140. As Dr.

Thompson explains, it was well known that a via surrounded by substrate material expands inward. Thompson, ¶¶141-143. For example, *Tsui* discloses a TSV that is

Pet. 25; Thompson Decl. ¶¶ 140-143

[0036] Preferably the via comprises an electroplated metal layer surrounding a polymer filler. This metal-polymer-metal structure helps to compensate for the different coefficients of thermal expansion of the non-active region 20 of the substrate (usually formed of silicon) and the electroplated metal layer (usually made of copper). Typically the coefficient of thermal expansion of the electroplated metal is much greater than the coefficient of thermal expansion of the non-active region 20. The simple presence of the filler helps to reduce the problems caused by the differences in coefficients of thermal expansion, first by reducing the volume of the electroplated layer and second by having an intermediate co-efficient of thermal expansion itself. Further, the filler layer has a degree of resilience. Therefore, if the electro-plated layer expands, due to a change in temperature, this expansion can be accommodated by a ‘squashing’ of the filler layer. In this way, extra stresses which may lead to cracking or damage to the non-active and active layers of the device can be minimised or avoided.

Pet. 25; *Tsui*, ¶ [0036]; Thompson Decl. ¶¶ 141, 143

Cooney Renders Obvious Claim [1b-3] (Undisputed)

“said hollow center being entirely surrounded by said conductive filler to provide space for said conductive filler to expand inward,”

expansion of the copper into *Tsui*’s polymer filler. Thompson, ¶144. According to Dr. Thompson, it would, therefore, have been obvious to a POSITA to include *Cooney*’s void 25 such that when *Cooney*’s TSV and substrate are subjected to an increase in temperature, the conductive filler in *Cooney* would expand inwardly, squashing the gas-filled void. *Id.*

Pet. 26; Thompson Decl. ¶ 144

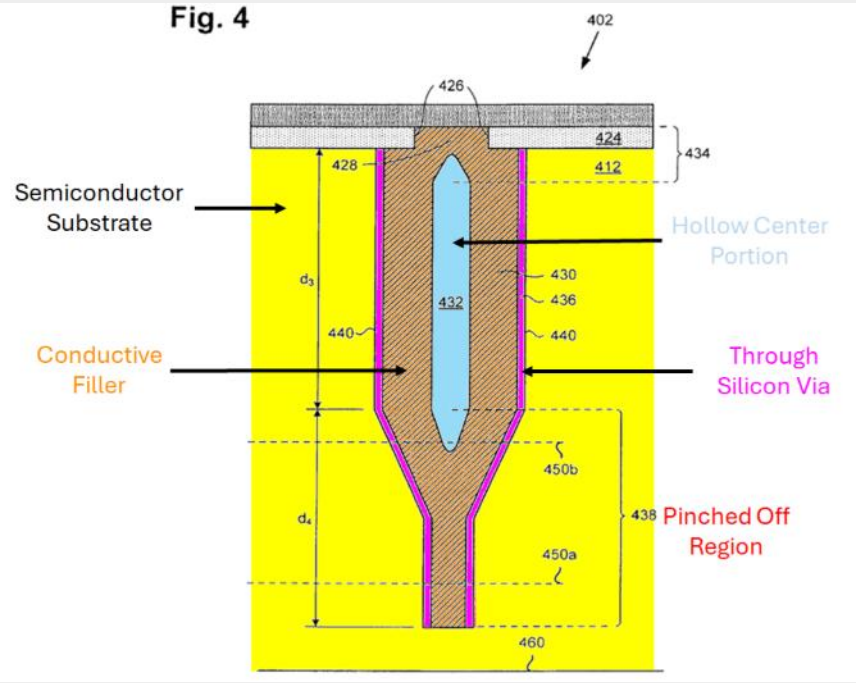
Pet. 26; Thompson Decl. ¶¶ 144-145

144. One skilled in the art would further recognize that a void (e.g., void 25 of *Cooney*) filled with a gas is significantly more resilient (elastic or compressible) than the polymer filler included in the TSV of *Tsui*. Thus, the conductive filler material in *Cooney*’s TSV would more readily expand inward into void 25 as compared to the expansion of *Tsui*’s metal layers into the polymer filler. It would, therefore, have been obvious to a POSITA that when *Cooney*’s TSV and substrate are subjected to an increase in temperature, the conductive filler in *Cooney* would expand inwardly, squashing the gas-filled void.

145. In view of the well-known inward expansion behavior of a conductive filler in a TSV including a void (filled with polymer or gas), a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney*’s TSV to allow *Cooney*’s conductor layer to expand inward into the void. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including a void in its conductor layer.

Cooney Discloses Claim [1c-1] (Undisputed)

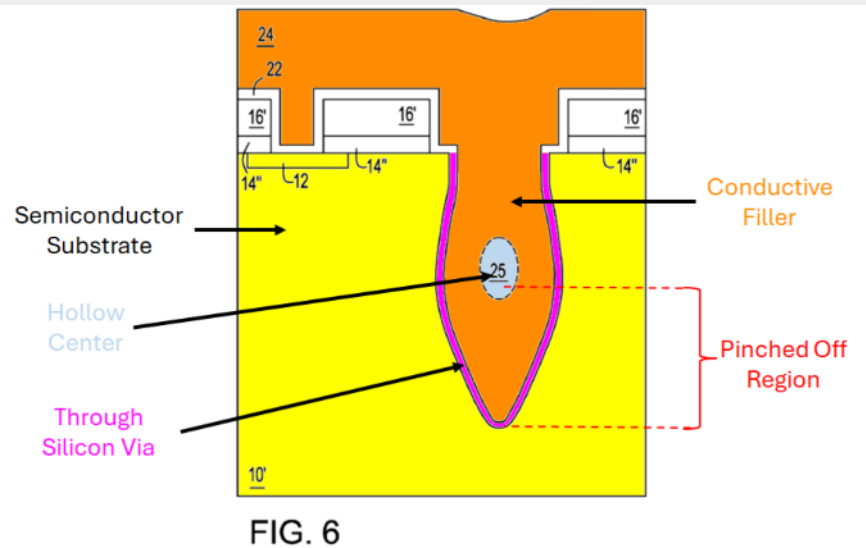
“wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**,”



Pet. 28; '609 patent, Fig. 4; Thompson Decl., ¶ 148

the extended aperture.” *Id.*, ¶[0060]. By localizing void 25, to region R3, *Cooney* discloses a TSV having a pinched off region at a bottom portion of the TSV, as illustrated in Figure 6 below. Thompson, ¶¶149-152.

Pet. 30; Thompson Decl., ¶¶ 149-152



Pet. 30; *Cooney*, Fig. 6; Thompson Decl. ¶ 152

[0060] As is illustrated by the phantom line enclosure within the schematic diagram of FIG. 6, the conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.

Pet. 30; *Cooney*, ¶ [0060]; Thompson Decl., ¶ 152

Cooney Discloses Claim [1c-1] (Undisputed)

“wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**,”

The phrase “to prevent contamination during processing of said semiconductor substrate” states yet another use for the functioning of the pinched off region and should be entitled to no patentable weight over the prior art. *Atlas Powder*, 190 F.3d at 1347; *Sinex*, 309 F.2d at 492; *Arctic Cat*, 919 F.3d at 1328. Other than disclosing the presence of the pinched off region in the TSV, the ’609 patent does not identify any features of the pinched off region that contribute to preventing contamination. See generally ’609 patent. Thompson, ¶154. Thus, this functional language should not be entitled to any patent weight, but even if it were, Cooney’s TSV includes a **pinched off region** similar to that recited in limitation [1c-1], Cooney’s **pinched off region**, like the claimed pinched off region, would prevent contamination during processing of the semiconductor substrate. Thompson, ¶154.

Pet. 31; Thompson Decl. ¶ 154

Cooney Discloses Claim [1c-1] (Undisputed)



Atlas Powder Co. v. Ireco, Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999) (“Artisans of ordinary skill may not recognize the inherent characteristics or functioning of the prior art. []However, the discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discoverer.”)



In re Sinex, 309 F.2d 488, 492 (C.C.P.A. 1962) (“Resolution of these four objections of appellant will determine whether the board was correct in finding appellant’s invention to be obvious over the Harris patent. For the reasons hereinafter stated, we think the board was correct. (a) The expression ‘for reconcentrating liquid dehydrating agents’ is merely a statement of intended use and does not qualify or distinguish the structural apparatus claimed over the reference.”)



Arctic Cat Inc. v. GEP Power Prods., Inc., 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“That rule is grounded in the statutory distinction, in identifying the permissible subject matter of a patent claim, between a physical product (which may be defined in part by its claimed functional capabilities) and activities that constitute a process (which may include a new "use" of a known invention).”)

Cooney Renders Obvious Claim [1c-1] (Undisputed)

“wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**,”

[0012] In the present invention, by the formation of the interlayer insulating film in which the second insulating film, which has an etching selectivity different from those of the first and third insulating films, is inserted between the first and third insulating films, a contact hole is formed to have a sidewall profile in which the second insulating film protrudes farther than the first and third insulating films due to a difference between the films in etch rate during the metal barrier layer pre-cleaning process, so that when the metal barrier layer is subsequently formed, an overhang is formed on the protruding sidewall of the second insulating film in the contact hole; and **when a tungsten film is subsequently deposited for filling the contact hole, a seam in the tungsten film is closed in the vicinity where the overhang occurred, so that the seam is prevented from becoming exposed in the subsequent CMP process and CMP post-cleaning process; thereby, bridging between contact plugs and increased contact plug resistance due to foreign matter becoming caught inside the seam can be inhibited.**

Pet. 32; *Kim*, ¶ [0012]; Thompson Decl. ¶ 159

Pet. 32; Thompson Decl. ¶ 161

¶160. Thus, a POSITA would have found it obvious to include the **pinched off region** in *Cooney*’s TSV to prevent contamination during subsequent processing of *Cooney*’s semiconductor substrate. Thompson, ¶161. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*’s express teaching of including the **pinched off region**. *Id.*

Cooney Renders Obvious Claim [1c-1] (Undisputed)

“wherein each of said plurality of **through silicon vias** has a **pinched off region** at a bottom portion to prevent contamination during processing of said **semiconductor substrate**,”

Thompson, ¶¶162-163. Thus, if not explicitly disclosed, *Cooney* at a minimum have rendered obvious limitation [1c-1] in view of the knowledge of a POSITA. Thompson, ¶164.

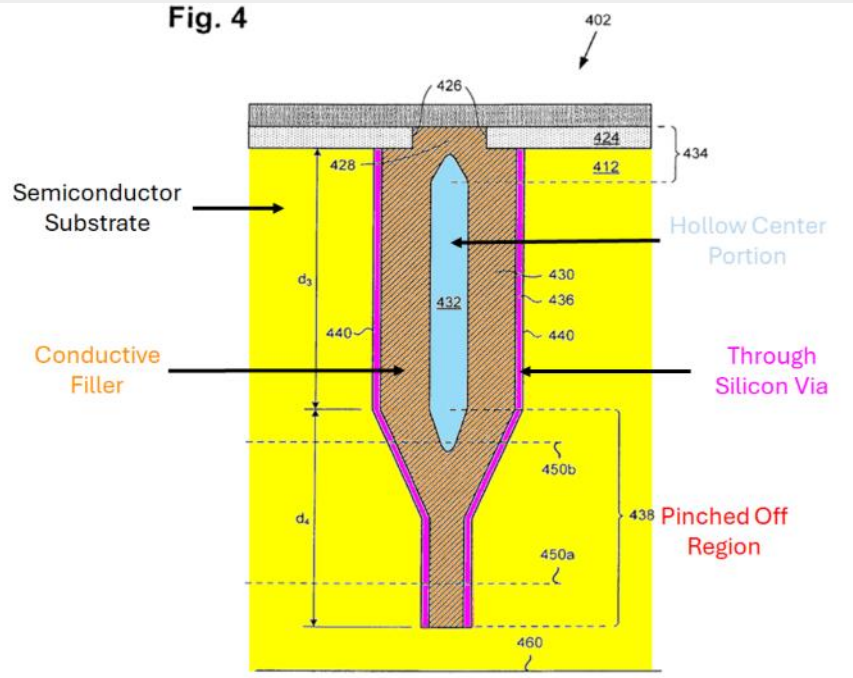
Pet. 34, Thompson Decl. ¶¶ 162-164

161. *Kim* illustrates that it was well known in the art before the earliest priority date of the '609 patent that pinched off regions at the top portion and/or bottom portion of a metal filled via help to prevent contamination of the via during subsequent semiconductor manufacturing processes. In view of this well-known function of pinched portions of a via, in my opinion, a POSITA would have found it obvious to include the pinched off region in *Cooney*'s TSV to prevent contamination during subsequent processing of *Cooney*'s semiconductor substrate. A POSITA would have had a reasonable expectation of success in doing so, given *Cooney*'s express teaching of including the pinched off region.

Pet. 32; Thompson Decl. ¶ 161

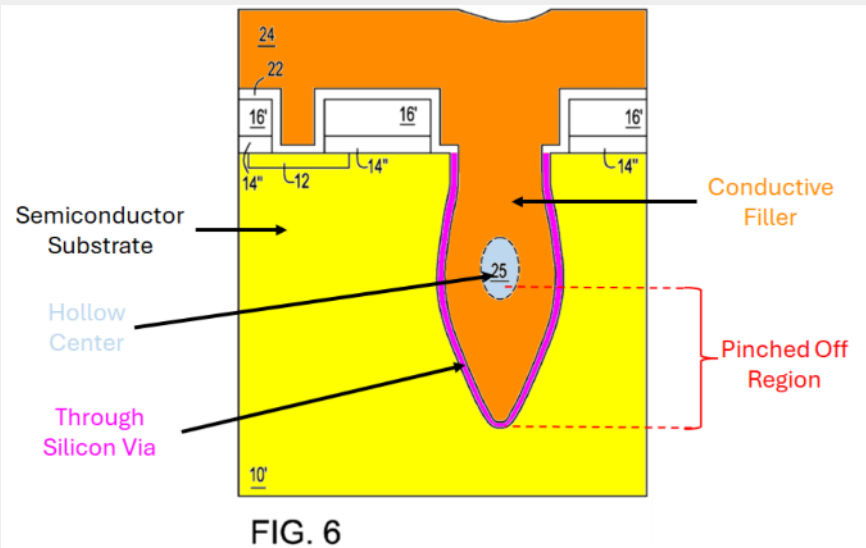
Cooney Discloses Claim [1c-2] (Undisputed)

“wherein said hollow center is tapered in said pinched off region,”



Pet. 28; '609 patent, Fig. 4; Thompson Decl., ¶ 148
the extended aperture.” *Id.*, ¶[0060]. By localizing void 25, to region R3, *Cooney* discloses a TSV having a pinched off region at a bottom portion of the TSV, as illustrated in Figure 6 below. Thompson, ¶¶149-152.

Pet. 30; Thompson, ¶¶ 149-152



Pet. 30, *Cooney*; FIG. 6; Thompson Decl. ¶ 152

[0060] As is illustrated by the phantom line enclosure within the schematic diagram of FIG. 6, the conductor layer 24 may be deposited or formed with a void 25, but due to the irregular sidewall curvature of the extended aperture, the void 25 is localized to the second comparatively wide region R3 of the extended aperture.

Pet. 30; *Cooney*, ¶ [0060]

Cooney Discloses Claim [1c-2] (Undisputed)

“wherein said hollow center is tapered in said pinched off region,”

“With respect to the void in Cooney being in a ‘pinched off region,’ we determine that Petitioner has made a sufficient showing on this preliminary record.” Inst. Dec. 17.

“With respect to the void in Cooney having a taper, we determine that Petitioner has made a sufficient showing on this preliminary record.” Inst. Dec. 18.

What HID Does Not Dispute

- **Ground 1**
 - ✓ *Cooney* discloses structural limitations of claim 1
 - ✓ *Cooney* discloses or renders obvious limitations [1pre], [1a], [1b-1], [1b-3], [1c-1], [1c-2], [11pre], [11a], [11c], and the additional limitations of claims 2-6, 9, 10, 12, 13, 14, 17, and 18
- **Ground 2**
 - ✓ *Cooney* in view of *Dean* renders obvious the additional limitations of dependent claims 7 and 15
- **Ground 3**
 - ✓ *Cooney* in view of *Farooq* renders obvious the additional limitations of dependent claims 8 and 16
- **Ground 4**
 - ✓ *Chen* in view of *Cooney* renders obvious the additional limitations of claims 8 and 16

Disputed Issues

- ☐ Level of Skill in the Art
- ☐ Do All Voids Reduce Thermal Stress?
- ☐ Does Cooney anticipate element [1b-2]?
- ☐ Does Cooney render obvious element [1b-2]?
- ☐ Are functional limitations of claim 1 entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

There Is No Material Dispute Over Level of Ordinary Skill in the Art

Samsung

IV. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (POSITA) at the time of the purported invention of the '609 patent (October 7, 2011) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and *vice versa*. Thompson, ¶¶72-74.

Pet. 9-10; Thompson Decl., ¶¶ 72-74.

HID

IV. LEVEL OF ORDINARY SKILL IN THE ART

As Mr. Berg explains, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. Additional formal education (such as Master of Science degrees) would compensate for less technical experience and vice versa. Ex. 2012 (Berg Declaration), ¶¶ 22-26.

POR. 7; Berg Decl. ¶¶ 22-26.

HID's Proffered Variation Is Immaterial

Compare Paper 17 (POR), §IV, with Paper 1 (Pet.), §IV. But HID's proffered variation is immaterial. See Okajima v. Bourdeau, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Both parties agree that a POSITA would have at least two years of experience in semiconductor design and fabrication, and HID's POR identifies no analysis that would turn on whether a POSITA held a bachelor's or master's degree. See POR §§IV-VII.

Reply, 1-2.

Disputed Issues

- ✓ No Material Dispute Regarding Level of Skill in the Art
- ❑ Do All Voids Reduce Thermal Stress?
- ❑ Does *Cooney* anticipate element [1b-2]?
- ❑ Does *Cooney* render obvious element [1b-2]?
- ❑ Are functional limitations of claim 1 entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

**HID Contends - “All Voids Do Not Reduce Stress”
- WRONG**

Birner Discloses That TSV Voids Reduce Substrate Stress

[0023] A significant difference in coefficient of thermal expansion between the substrate and the fill material in a through substrate via can create large stress concentration around the through substrate via, for example, during subsequent thermal processing. Such increased stress can result in significant yield loss arising from cracks, de-lamination, via collapse, as well as dislocations, stacking faults in the substrate, etc. Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material.

Pet., 2; Reply, 2; *Birner*, ¶ [0023]; Thompson Decl. ¶ 49; Thompson-Supp. Decl. ¶¶ 7, 9

[0024] In various embodiments, the present invention overcomes these problems by reducing stress around the through substrate via by filling the through substrate via with an effective material with minimal thermal expansion. In various embodiments, the effective material comprises a combination of metal and voids. For example, metals typically expand faster than silicon, whereas voids, for example, filled with a gas having negligible expansion relative to the silicon substrate. Hence, a combination of metal with voids produces an effective material with a coefficient of expansion comparable to the substrate. In one embodiment, this effective material comprises a void tailored to specific dimensions and shape, the void forming an inner core region of the through substrate via, while a conductive fill material forms an outer layer of the through substrate via.

Pet., 2; Reply, 2-4; *Birner*, ¶ [0024]; Thompson Decl. ¶ 49; Thompson-Supp. Decl. ¶¶ 7, 12

Birner Discloses That TSV Voids Reduce Substrate Stress

[0038] As manufacturability is a key concern, in various embodiments, after selecting suitable materials, the thickness of the fill material **50** is selected relative to the dimension of the tailored void **90**. For example, a fraction of the fill material **50** (f_{FM}) may be identified based on the materials selected. For example, in FIG. 1*b*, this fraction of the fill material **50** (f_{FM}) is a ratio of thickness of the fill material r_{FM} to the radius of the through substrate opening r_{TSV} . The fraction (f_{FM}) depends on the relative difference between the coefficient of thermal expansions of silicon (α_{Si}), fill material **50** (α_{FM}) and the tailored void (α_V) as $f_{FM} = (\alpha_{Si} - \alpha_V) / (\alpha_{FM} - \alpha_V)$. Assuming negligible expansion of the tailored void or $\alpha_{DM} \approx 0$, the fraction $f_{FM} = \alpha_{Si} / \alpha_{FM}$. Hence, if copper is the fill material, a suitable fraction is about 30% the radius of the through substrate opening **250** r_{TSV} . In other words, a partial fill that covers about 15% of the sidewall of the trench minimizes the stress from thermal expansion. In various embodiments,

Reply, 4; *Birner*, ¶ [0038]; Thompson-Supp. Decl. ¶ 12

Birner Discloses That TSV Voids Reduce Substrate Stress

“reduce thermal stress” – Claim Term

re·duce \ri-'dūs, -'dyūs\ *vb* **re·duced**; **re·duc·ing** [ME, to lead back, fr. L *reducere*, fr. *re-* + *ducere* to lead — more at TOW] *vt* (14c) 1 **a** : to draw together or cause to converge : CONSOLIDATE <~ all the questions to one> **b** (1) : to diminish in size, amount, extent, or number <~ taxes> <~ the likelihood of war> (2) : to decrease the volume and concentrate the flavor of by boiling <add the wine and ~ the sauce for two minutes> **c** : to narrow down : RESTRICT <the Indians were *reduced* to small reservations> **d** : to make shorter : ABRIDGE 2 *archaic*

Reply, 4; Ex. 1026, 4

“minimize thermal stress” – HID’s construction when interpreting *Birner*

min·i·mize \'mi-nə-,mīz\ *vt* **-mized**; **-miz·ing** (1802) 1 : to reduce or keep to a minimum 2 : to underestimate intentionally : PLAY DOWN, SOFT-PEDAL <*minimizing* losses in our own forces while maximizing those of the enemy> — **min·i·mi·za·tion** \,mi-nə-mə-'zā-shən\ *n* — **min·i·miz·er** \'mi-nə-,mī-zər\ *n*
min·i·mum \'mi-nə-məm\ *n, pl* **-i·ma** \-nə-mə\ or **-i·mums** [L, neut. of *minimus* smallest; akin to L *minor* smaller — more at MINOR] (1674) 1 : the least quantity assignable, admissible, or possible 2 : the least of a set of numbers; *specif* : the smallest value assumed by a continuous function defined on a closed interval 3 **a** : the lowest degree or amount of variation (as of temperature) reached or recorded **b** : the lowest speed allowed on a highway — **minimum** *adj*

Reply, 4; Ex. 1026, 3

Birner Discloses That TSV Voids Reduce Substrate Stress

(Ex-1026, 4). Thompson-Supp, ¶13. A POSITA would therefore understand from *Birner* that selecting a void size based on the ratio α_{Si}/α_{FM} may diminish the stress in the substrate to a lowest possible value. Thompson-Supp, ¶13. Nothing in *Birner*, however, discloses or suggests that void sizes not based on the ratio α_{Si}/α_{FM} , do not reduce the thermal stress, even though such reduction may not be to the lowest possible value. Thompson-Supp, ¶13. Rather, as discussed, *Birner* discloses that in various embodiments, voids (without specifying any size or shape) form an effective material that reduces stress in the substrate. *Birner*, ¶24; Thompson-Supp, ¶13. Thus, a POSITA would not have understood *Birner* as disclosing that only some voids reduce thermal stress. Thompson-Supp, ¶14.

Reply, 4-5; Thompson-Supp Decl. ¶¶ 13-14

14. To summarize, one skilled in the art would have understood *Birner* as disclosing that the metal-void combination (regardless of void size) reduces thermal stress in the substrate, though not necessarily to the lowest possible value. Furthermore, one skilled in the art would have understood from *Birner* that the void size could be selected based on the ratio $\alpha_{Si} / \alpha_{FM}$ to achieve the lowest possible value of stress in the substrate. However, a skilled artisan would not have interpreted *Birner* as disclosing or suggesting that a void must be designed in a particular manner to reduce the thermal stress in the substrate.

Reply, 4-5; Thompson-Supp Decl. ¶ 14

Kinoshita Discloses That TSV Voids Reduce Substrate Stress

ICEP 2014

TAP-1

Thermal Stresses around Void in Through Silicon Via in 3D SiP

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Abstract—Thermal stresses around void in Through Silicon Via (TSV) structure in 3D SiP were discussed under conditions of device operation and reflow process using Finite Element Method. In case of the device operation, equivalent stress around void was estimated at around 100 MPa. It showed the low cycle fatigue of Cu TSV under device operation. The stress was lower than yield stress of Si. However, temperature elevation due to reflow process was once or twice during the process. It showed the low possibility for fracture by low cycle fatigue under reflow process. In case without void, maximum principal stress of Si was estimated around 400 MPa. It was almost similar to the bending strength of Si. Stress concentrations were occurred at parts of corner and interface of materials. It has possibility that singular stress field was formed at the parts, and we should discuss fracture induced by singular stress field.

Keywords—Thermal Stresses, Void, TSV/Through Silicon Via, 3D SiP, FEM(Finite Element Method)

1. INTRODUCTION

Recently, the high density 3D packaging technology has been developed to reduce the size and to improve the performance of semiconductor devices [1-8]. Through silicon via (TSV) technique has enabled faster electrical-signal communication between semiconductor chips. The delay time of the signals, which depends on circuit lengths, is become short in 3D packaging structures as compared to the existing 2D packaging structures. Due to above advantages, 3D SiP (Three Dimensional System in Package) with TSV technique has been widely investigated for cooling systems, manufacturing systems and device designs.

The cross-sectional photograph of a 3D stacked structure is shown in Fig. 1. The TSVs are arranged in full area array configuration in this system. The structure was developed by ASET (Association of Super-Advanced Electronics Technology) [9]. In complex device structures which were shown in Fig. 1, the thermal stresses generated in the systems are mainly caused by the mismatch of coefficients of thermal expansion (CTE) and temperature variations of the materials constituting the systems. Several studies on 3D device

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Proceedings

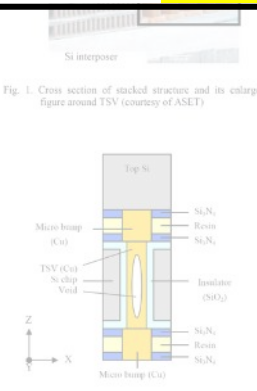


Fig. 1. Cross section of stacked structure and its enlarged figure around TSV (courtesy of ASET)

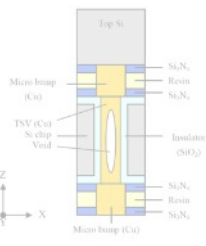
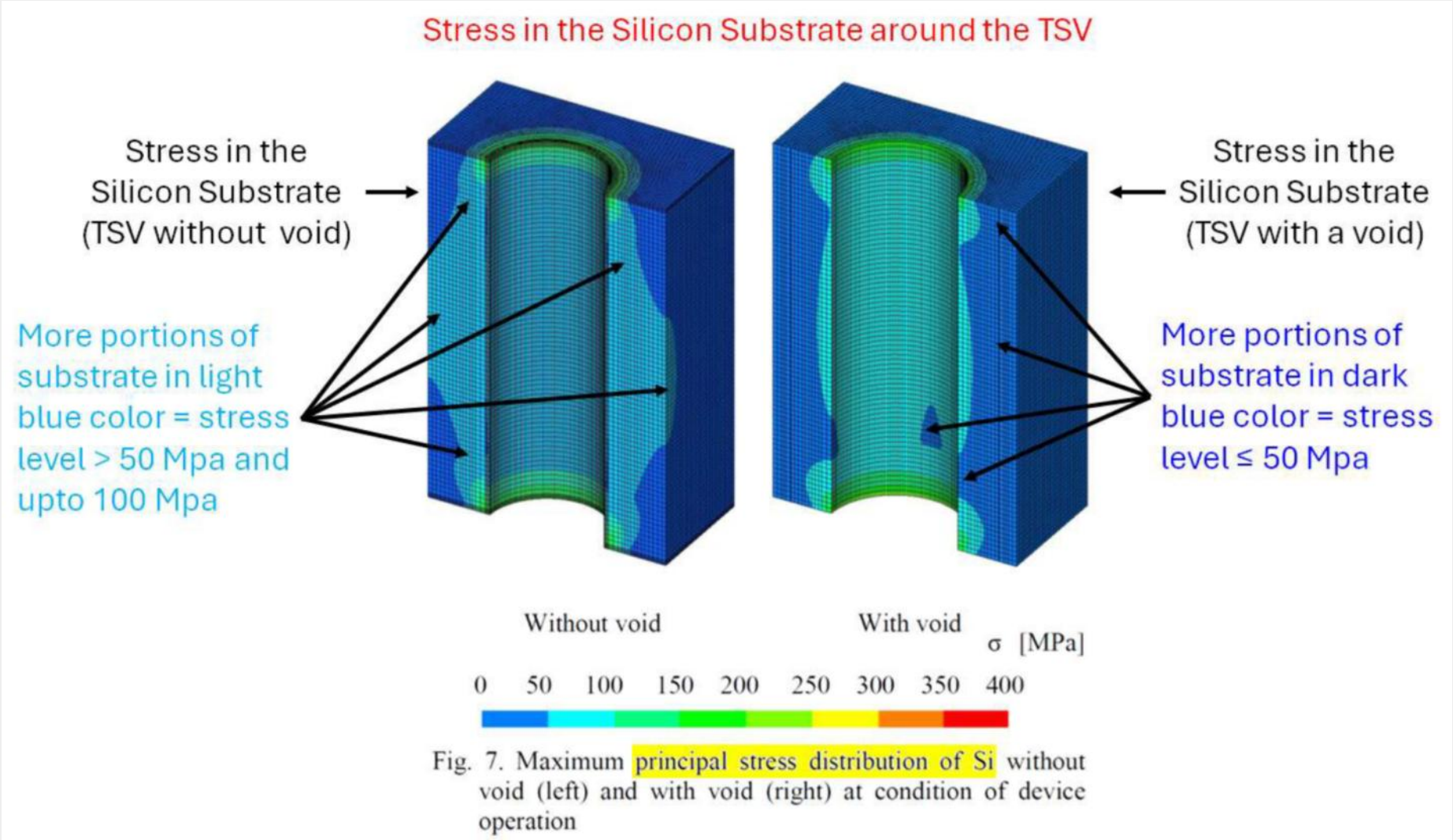


Fig. 2. Schematic image of simulation model of the TSV structure with void in TSV

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Kinoshita Discloses That TSV Voids Reduce Substrate Stress



Reply, 6; Kinoshita, Fig. 7 (annotated)

Kinoshita Discloses That TSV Voids Reduce Substrate Stress

A POSITA would understand from the above figure that dark blue color represents stress levels below 50 MPa, whereas the light blue color represents stress levels greater than 50 MPa and up to 100 MPa. Thompson-Supp, ¶19. In the figure on the right (TSV with void), a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa, as compared to the figure on the left (TSV without void). Thompson-Supp, ¶20. Conversely, the figure on the left (without void) depicts a larger portion of the substrate in light blue, representing stress levels up to 100 MPa. Thompson-Supp, ¶20. Thus, *Kinoshita*, Fig. 7 shows that the substrate stress level is lower (more dark blue portions) when the TSV includes a void than when it does not. Thompson-Supp, ¶20.

Reply, 6-7; Thompson-Supp Decl. ¶¶ 19-20

HID Contradicts Itself

HID – Patent Owner Response

Stress with void is 100 MPa

this stress is transferred directly to the substrate. Ex. 2012, ¶¶ 54, 66. *Kinoshita* also notes that “[i]n the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa,” indicating that the presence of a void does not reduce the stress on the inside of the substrate. Ex. 2008, at 107; Berg Decl., ¶ 67. Due to the POSITA’s knowledge of void characteristics at

POR, 26; Berg Decl. ¶ 67

HID Sur Reply

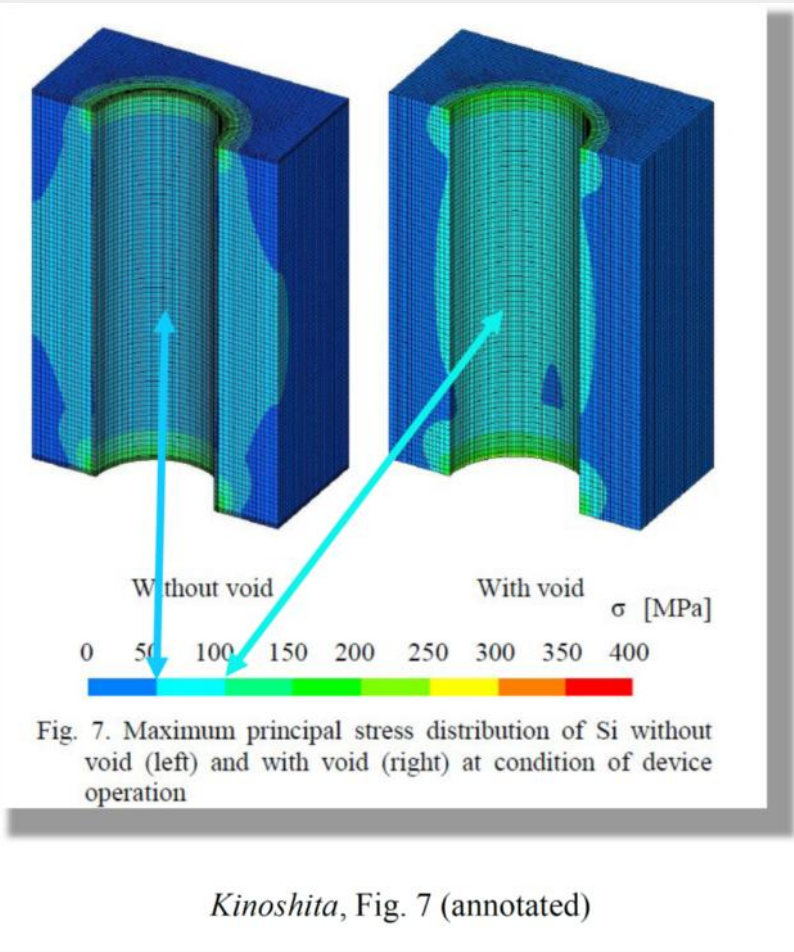
Stress with void is between 100-150 MPa

The stress in the Si of the voided TSV on the right, above, clearly contains more area of stress between 100 and 150 MPa than the stress on the Si of the non-voided TSV on the left. Petitioner notes that while the stress travels further into the

Sur-Reply, 7

HID's Interpretation of *Kinoshita* Fig. 7 is **INCONSISTENT**

HID's **Incorrect** Interpretation



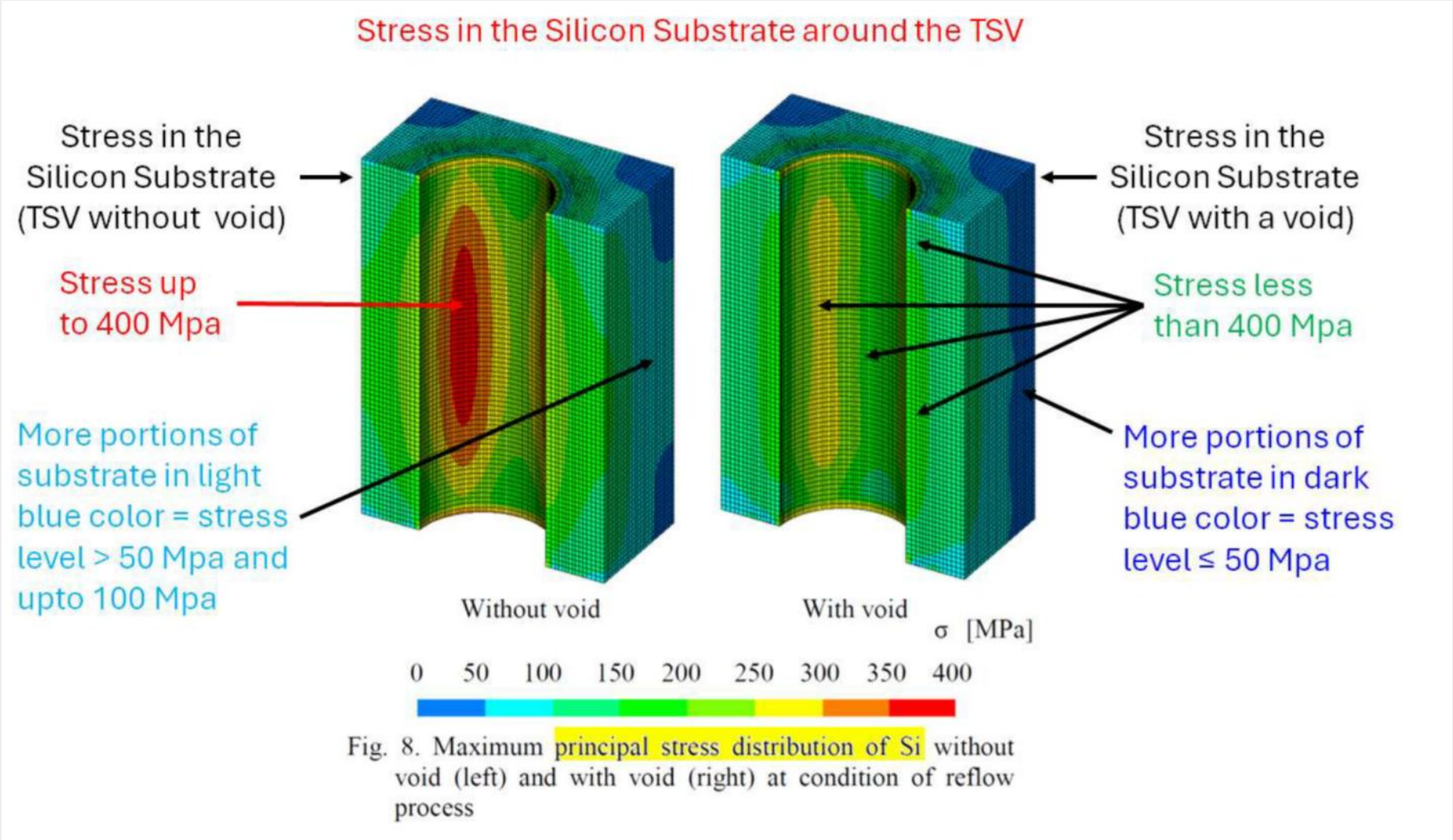
Sur-Reply, 8

Correct Interpretation

Maximum principal stress distributions at device operation in the cross-section of one chip model without voids and with a void were shown in Fig. 7. The TSV and the SiO₂ insulator layers were removed in the figure and only the cylindrical inner surfaces of Si were shown. In the cases the TSV structure without voids and with a void, the stress on inner surface of Si was estimated to be about 100 MPa.

POR, 26; *Kinoshita*, 3

Kinoshita Discloses That TSV Voids Reduce Substrate Stress



Reply, 8; Kinoshita, Fig. 7 (annotated)

Kinoshita Discloses That TSV Voids Reduce Substrate Stress

As illustrated in the figure on the right above (TSV with void), the stress on the inner surface of the substrate surrounding the void is about 200-250 MPa (significantly lower than 400 MPa), whereas the stress on the same surface in the figure on the left above (TSV without void) is up to 400 MPa. Thompson-Supp, ¶¶23-24. Furthermore, a larger portion of the substrate is shown in dark blue, indicating stress levels below 50 MPa in the figure on the right above (TSV with void), as compared to the figure on the left (TSV without void). Thompson-Supp, ¶24. Thus, *Kinoshita*, Fig. 8 provides additional evidence that the substrate stress level is lower when the TSV includes a void than when it does not.

Thompson-Supp, ¶24.

Reply, 8-9; Thompson-Supp Decl. ¶¶ 23-24

Kinoshita Discloses That TSV Voids Reduce Substrate Stress

Kinoshita does not show that a TSV void increases thermal stress in the surrounding substrate. And HID's arguments against TSV voids reducing thermal stress in the surrounding substrate fail in the face of the evidence. Thompson-Supp, ¶25.

Reply, 9; Thompson-Supp Decl. ¶ 25

Disputed Issues

- ✓ No Material Dispute Regarding Level of Skill in the Art
- ✓ HID Fails to Demonstrate That “All Voids Do Not Reduce Thermal Stress”
- ❑ Does *Cooney* anticipate element [1b-2]?
- ❑ Does *Cooney* render obvious element [1b-2]?
- ❑ Are functional limitations of claim 1 entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

Dr. Thompson Did Not Supply a Missing Limitation



Monsanto Tech. LLC v. E.I. DuPont de Nemours & Co., 878 F.3d 1336, 1345 (Fed. Cir. 2018) (holding that expert opinion “may be used to interpret [an] allegedly anticipating reference and to shed light on what it would have meant to” a POSITA)



Telemac Cellular Corp. v. Topp Telecom, Inc., 247 F.3d 1316, 1328 (Fed. Cir. 2001) (“The evidence must make clear that the missing feature is necessarily present, and that it would be so recognized by persons of ordinary skill in the art.”)

Dr. Thompson Did Not Supply a Missing Limitation

semiconductor substrate. Ex. 1001, 4:60-61; *see generally* Ex. 1001. In my opinion, a POSITA would have understood that void 25 in *Cooney's* TSV would also reduce thermal stress in *Cooney's* substrate, *see supra* VI.C.1, consistent with the hollow center of the '609 patent providing stress reduction in the substrate of the '609 patent.

Reply, 15; Thompson Decl. ¶ 123

Dr. Thompson Did Not Supply a Missing Limitation

Thompson Declaration, Section VI.C.1

1. TSV Voids to Reduce Thermally Induced Stress

48. A number of solutions have been proposed to reduce problems caused by CTE mismatches for ICs having copper. As one example, *Pogge* (Ex. 1005) discloses that a void in a copper filled TSV “has an important function in relieving stress caused by differences in thermal coefficient of expansion (TCE) of the various materials in and around the feature.” *Pogge*, ¶[0027]. Similarly, *Edelstein* (Ex. 1006) discloses that a “through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures.” *Edelstein*, ¶[0047]. Moreover, during prosecution of the ’609 patent, the Examiner cited *Edelstein* and *Beyne* for the proposition that a void enclosed in a TSV reduces the amount of thermal stress on the surrounding substrate, and Patent Owner acquiesced to the rejection and did not rebut the Examiner’s statement. Ex. 1003, at 88, 70-77, 67, 65.

49. The mechanism for the voids to reduce the stress was well known.

This is because “metals typically expand faster than silicon, whereas voids, for example, filled with a gas having negligible expansion relative to the silicon substrate.” *Birner* (Ex. 1022), ¶[0024]. “Hence, a combination of metal with voids produces an effective material with a coefficient of expansion comparable to the substrate.” *Id.* For example, Figure 1a of *Birner*, below, shows that a TSV opening 250 includes a void 90 tailored to specific dimensions and shape. *Id.*, ¶[0024], [0032]. The void 90 forms an inner core region of the TSV, while a metal filler material 50 forms an outer layer of the TSV. *Id.* The void 90 provides room for the metal filler material 50 to expand and thus, on average, the void-metal combination has a thermal expansion profile similar to the silicon.

Reply, 14; Thompson Decl. ¶ 49

Reply, 15; Thompson Decl. ¶ 48

Reply, 15; Thompson Decl. ¶¶ 48-49

HID's Distinction Between Size of a Void and the "Hollow Center" Lacks Merit

"[T]he claims of the '609 patent do not limit the size of the hollow center."
Reply, 15; '609 Patent

For example, as Dr. Thompson explains, *Birner* discloses a void diameter of 3.5 μm for a TSV diameter of 5 μm , and a void diameter of 10.5 μm for a TSV diameter of 15 μm . Thompson-Supp, ¶29 (citing *Birner*, ¶¶29, 38 disclosing TSV diameters of 5-15 μm and a fill fraction of 30%). Likewise, *Kinoshita* discloses its void's minor axis (i.e., void diameter) is 12 μm . *Kinoshita*, 2. Thompson-Supp, ¶30. These void diameters are significantly larger than HID's alleged pinholes and no different than the claimed "hollow center." Thompson-Supp, ¶¶29-30. And, as discussed in Section III, the TSV voids in both *Birner* and *Kinoshita* reduce thermal stress in the surrounding substrate. Thompson-Supp, ¶30.

Reply, 16; Thompson-Supp
Decl., ¶¶ 29-30

HID Arguments Regarding The Torpedo Shape of *Cooney's* TSV Are Irrelevant

“[C]laim 1 of the '609 patent recites a ‘hollow center to reduce the thermal stress in the substrate,’ and does not require a straight TSV.” Reply, 17.

“Thus, the question is whether Cooney’s torpedo-shaped TSV with the optional void results in lower thermal stress in the substrate, compared to the same torpedo-shaped TSV without the void, not whether Cooney’s TSV reduces thermal stress relative to a straight TSV.” Reply, 17.

Law Regarding Expert Opinion



Upjohn Co. v. Mova Pharm. Corp., 225 F.3d 1306, 1311 (Fed. Cir. 2000) (“Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity determination.”)

“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” 37 C.F.R. § 42.65(a)

Mr. Berg's Unsupported Testimony Regarding The Torpedo Shape of *Cooney's* TSV Is Entitled to No Weight

2. The Shape of *Cooney's* TSV Increases Thermal Stress

71. The optional void in *Cooney* is created by incompletely filling *Cooney's* TSV.³ Ex. 1004, ¶ [0055]. In my opinion, the torpedo shape itself in *Cooney* increases thermal stress in the substrate as compared to a more typical straight TSV. This is because filling this bulge requires additional metal to fill the TSV. Because there is more metal, it will increase by a greater factor at a given temperature than a straight TSV with less metal. And the torpedo shape itself can increase thermal stresses, by focusing stress on certain portions of the substrate rather than spreading them out along the entire TSV. Dr. Thompson did not analyze the shape of the void in *Cooney*.

Berg Decl. ¶ 71; POR, 28-29

Disputed Issues

- ✓ No Material Dispute Regarding Level of Skill in the Art
- ✓ HID Fails to Demonstrate That “All Voids Do Not Reduce Thermal Stress”
- ✓ *Cooney* discloses element [1b-2] and therefore anticipates this element
- ❑ Does *Cooney* render obvious element [1b-2]?
- ❑ Are functional limitations of claim 1 entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

HID's Theory – *Pogge* Discloses That Voids Relieve Stress But Not That the Stress Is Borne By The Substrate - **WRONG**



Standard Oil Co. v. Am. Cyanamid Co., 774 F.2d 448, 454 (Fed. Cir. 1985) (A POSITA “is presumed to be aware of all the pertinent prior art.”)

Prior Art Discloses That CTE Differences Generate Stress In The Substrate Surrounding The TSV

Pogge

[0027] A layer 24 of copper is formed on layer 23 (e.g. by electroplating) in the trench and on top of the wafer. Layer 24 is built up on the sidewalls of the trench until it reaches a thickness such that the upper part of the trench is closed, as shown in FIG. 2C. With this structure, a conducting path is established between the bottom of the trench and the top surface of the wafer, while a void 25 remains near the bottom of the trench. It should be noted that the void 25 has an important function in relieving stresses caused by differences in the thermal coefficient of expansion (TCE) of the various materials in and around the feature.

Pet., 21; Thompson Decl. ¶¶ 126-127; Pogge, ¶ [0027]

West

[0005] Copper, as well as some other TSV filler materials, have a significantly higher coefficient of thermal expansion (CTE) as compared to conventional IC substrates, such as silicon. For example, copper has a CTE of approximately 17 ppm/° C., whereas silicon has a CTE of approximately 2 to 3 ppm/° C. This CTE mismatch (Δ CTE) can result in significant thermally induced stress in the silicon including the circuitry (e.g. MOS transistors) in the silicon surrounding the TSVs, particularly during certain fab processing subsequent to the fabrication of the TSV (e.g., 360 to 410° C. sinters), during assembly and test/operations as may occur during solder reflow (e.g., up to about 260° C.) or during thermo-compressive bonding (e.g., up to 400° C.), during certain temperature cycle reliability testing (e.g., -55° C. to 125° C.), or even during long-term field operation of the IC.

Pet., 2; Thompson Decl. ¶ 47; Reply, 21; West, ¶ [0005]

Birner

[0023] A significant difference in coefficient of thermal expansion between the substrate and the fill material in a through substrate via can create large stress concentration around the through substrate via, for example, during subsequent thermal processing. Such increased stress can result in significant yield loss arising from cracks, de-lamination, via collapse, as well as dislocations, stacking faults in the substrate, etc. Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material.

Pet., 2; Thompson Decl. ¶¶ 48; Reply, 21; Birner, ¶ [0023]

“It’s a combination of changing temperature and having different CTEs causes stress in the integrated circuits.” Thompson Depo. Tr., 26:16-18

Reply, 21; Thompson Depo. Tr. (Ex. 2007), 26:16-18

HID's Theory – *Edelstein* Only Discloses Mechanical Stress And Not Thermal Stress - **WRONG**

“A POSITA would have understood that thermal stress is mechanical stress caused due to thermal expansion.” Reply, 22-23

$$\sigma = \frac{P}{A}. \quad (2)$$

This force per unit area is called *stress*. In the following, the force will be measured in pounds and the area in square inches so that the stress will be measured in pounds per square inch. The elongation of the bar per unit length is determined by the equation

$$\epsilon = \frac{\delta}{l} \quad (3)$$

and is called the *unit elongation* or the *tensile strain*. Using eqs. (2) and (3), Hooke's law may be represented in the following form:

$$\epsilon = \frac{\sigma}{E}, \quad (4)$$

and the unit elongation is easily calculated provided the stress and the modulus of elasticity of the material are known. The

Reply, 22-23; Thompson-Supp Decl., ¶ 42; *Timoshenko*, 18

from the condition that the length remains unchanged. Let α denote the coefficient of thermal expansion and σ the compressive stress produced by the reactions. Then the equation for determining σ will be

$$\alpha(t - t_0) = \frac{\sigma}{E},$$

from which

$$\sigma = E\alpha(t - t_0). \quad (12)$$

Reply, 22-23; Thompson-Supp Decl., ¶ 42;
Timoshenko, 40

Kinoshita, Cited By HID, Equates Thermal And Mechanical Stress

In this study, the effects of the presence of voids inside the TSVs in a 3D SiP structure on the thermal stresses in the TSV structure under device operating condition are analyzed using the large scale simulator, ADVENTURECluster [15]. The mechanical stresses in the Cu TSVs and in the Si chips are obtained from the simulations.

Reply, 23; *Kinoshita*, 2; Thompson-Supp Decl. ¶ 44

HID's Theory – *Edelstein* Never Discloses Stress Reduction In The Substrate - **WRONG**

[0047] The structure of FIG. 2B comprises a substrate 224 in which the through-via comprises an annular ring of insulating material 223 within which is disposed a conductive via of metal (e.g., copper) 225 having a void 220 at its core. The top and bottom surfaces of the through-via are copper, and copper covers the insulated sidewalls of the through-via. However, a void filled with a gas such as air, an inert gas, or N₂, or alternatively a vacuum, is disposed at the center of the through-via and provides an effective modulus which is more nearly matched to the substrate 224. The through-via becomes compliant when voided, resulting in a lower effective modulus and a lower effective Poisson ratio, and therefore exhibiting lower stresses and forces due to surrounding structures. The effective Poisson ratio here is defined as the ratio of out-of-plane displacement to in-plane displacement due to in-plane stress to reduce mechanical stresses encountered in processing and use. For a through-via material with high Poisson ratio of 0.4, the effective

Poisson ratio can be reduced to about 0.22 with the introduction of a percolated network of through-voids with an effective radius of three quarters of the through-via radius when a through-void of radius of three quarters of the via radius is introduced in the through-via. Although it does not change the thermal expansion coefficient, the introduction of a void or voids reduces the effective modulus and Poisson ratio of the through-via, resulting in a compliant through-via that exerts much less stress and force on the surrounding structures. In other words it behaves on a whole as if it had a much smaller thermal expansion mismatch with the substrate, thereby reducing piston-like deviations at the top during thermal cycling.

Pet, 21, Thompson Decl. ¶ 129; *Edelstein*, ¶ [0047]

Disputed Issues

- ✓ No Material Dispute Regarding Level of Skill in the Art
- ✓ HID Fails to Demonstrate That “All Voids Do Not Reduce Thermal Stress”
- ✓ *Cooney* discloses element [1b-2] and therefore anticipates this element
- ✓ *Cooney* in view of the knowledge of a POSITA renders obvious element [1b-2]
- ❑ Are functional limitations of claim 1 entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

**HID Contends – Functional Limitations in Claim 1
Are Entitled to Patentable Weight - **WRONG****

Statement of Intended Use or Scientific Explanation Not Entitled to Patentable Weight



Atlas Powder Co. v. Ireco, Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999) (“However, the discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art’s functioning, does not render the old composition patentably new to the discoverer.”)

“sufficient aeration ... to enhance sensitivity” determined to be unappreciated property of prior art composition. *Id.* at 1348.

- ❑ Here – All voids reduce thermal stress – *Pogge, Edelstein, Birner, Kinoshita*
- ❑ HID failed to show: “All voids do not reduce thermal stress”

HID Concedes That “to reduce thermal stress in the substrate” is the Purpose or Intended Use of the Hollow Center

The claim language in the '609 Patent is intended to convey the purpose of the hollow center: to reduce thermal stress in the substrate.

POR, 13

K-2 Corp. Does Not Help HID

HID's Position

“Functional language generally limits the claim to a structure when the functional language describes something about the structure of the apparatus rather than merely listing its intended or preferred uses.” (citing *K-2 Corp.* as holding that claim term ‘for substantially preventing movement therebetween at least in a horizontal plane’ dictates the meaning of ‘permanently affixed’ to mean that it prevents movement in a horizontal plane.)” POR, 13



K-2 Corp. v. Salomon S.A., 191 F.3d 1356, 1363–64 (Fed. Cir. 1999) (“K-2’s primary argument is that the functional language in the claim following this limitation-‘for substantially preventing movement therebetween at least in a horizontal plane’-dictates the meaning of ‘permanently affixed.’ That is, K-2 suggests that the inclusion of this functional language converts the meaning of ‘permanently affixed’ to mean ‘affixed to prevent movement in at least a horizontal plane.’ We cannot accept this reading of the claim.”

“[T]he limitation ‘hollow center to reduce thermal stress in said semiconductor substrate’ says nothing about the structure of the hollow center ... no information regarding the shape, size, or location of the hollow center that would result in reduction of thermal stress.”

Reply, 11

Innova/Pure Water Does Not Help HID

HID's Position

“The hollow center portion in Claim 1 must therefore be sufficient to reduce thermal stress in the semiconductor substrate, or it will not be the claimed ‘hollow center.’” POR, 14.



Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc., 381 F.3d 1111, 1117–20 (Fed. Cir. 2004) (holding that the functional relationship “operatively connected” means that “the claimed components must be connected in a way to perform a designated function.”)

“[T]he phrase ‘to reduce thermal stress in said semiconductor substrate’ does not describe a functional relationship between two or more claimed components. Rather, it describes the intended use of a single component—“the hollow center.”

Reply, 12

Sinex And Arctic Cat Not Just Limited to Preambles

HID's Position

In re Sinex and Arctic Cat “merely hold[] that a preamble is not limiting because it is merely a statement of intended use.” POR, 15.



Arctic Cat Inc. v. GEP Power Prods., Inc., 919 F.3d 1320, 1328 (Fed. Cir. 2019) (“That rule is grounded in the statutory distinction, in identifying the **permissible subject matter of a patent claim**, between a physical product (which may be defined in part by its claimed functional capabilities) and activities that constitute a process (which may include a new "use" of a known invention).”)

Disputed Issues

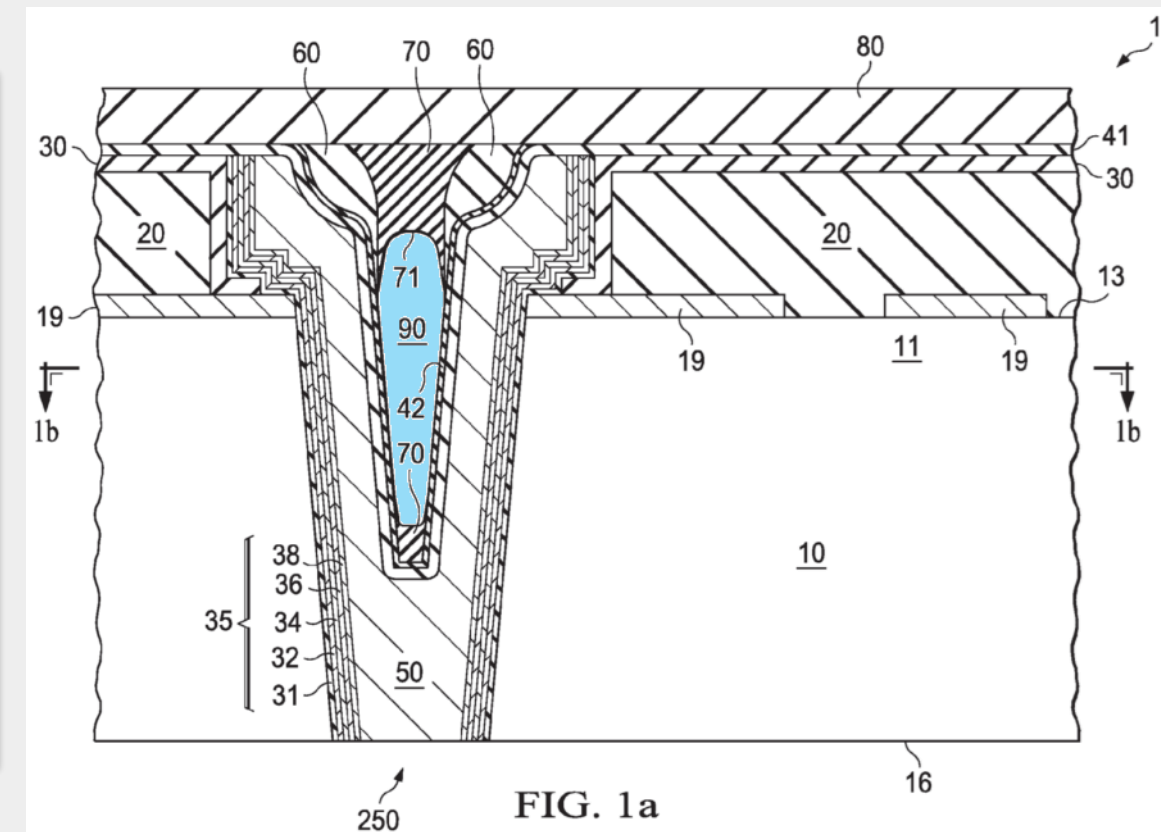
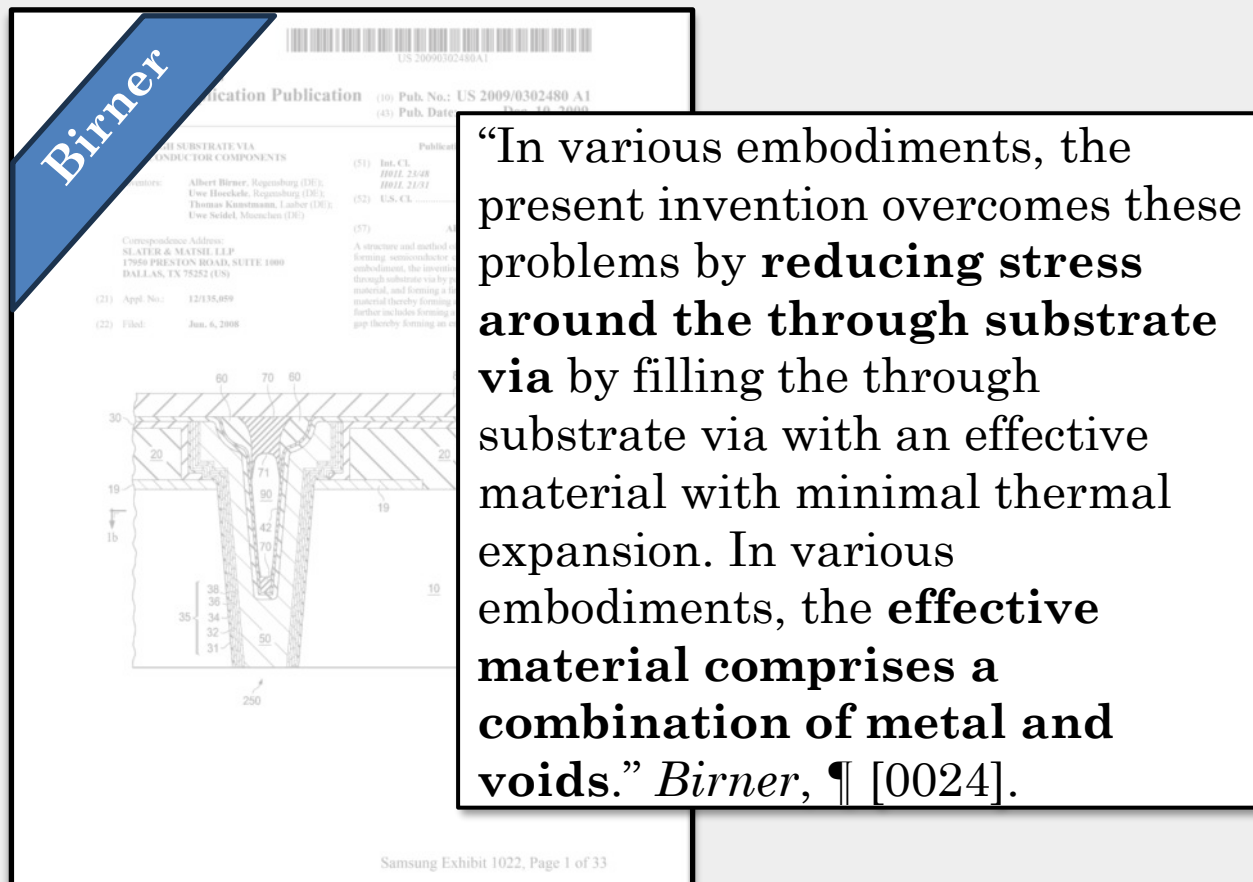
- ✓ No Material Dispute Regarding Level of Skill in the Art
- ✓ HID Fails to Demonstrate That “All Voids Do Not Reduce Thermal Stress”
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- ✓ *Cooney* in view of the knowledge of a POSITA renders obvious element [1b-2]
- ✓ Functional limitations of claim 1 not entitled to patentable weight?
 - “to reduce thermal stress in said semiconductor substrate”
 - “to provide space for said conductive filler to expand inward”
 - “to prevent contamination during processing of said semiconductor substrate”

Additional Slides

Birner Does Not Disclose That Some Voids Increase Stress

HID's Position

“Thus, Birner’s discussion of the ‘minimization’ of thermal stress can also be understood to mean that a void, if designed outside of the characteristics disclosed in Birner, can also have no impact or maximize thermal stress.” Sur-Reply, 5



Birner Discloses That TSV Voids Reduce Substrate Stress

[0023] A significant difference in coefficient of thermal expansion between the substrate and the fill material in a through substrate via can create large stress concentration around the through substrate via, for example, during subsequent thermal processing. Such increased stress can result in significant yield loss arising from cracks, de-lamination, via collapse, as well as dislocations, stacking faults in the substrate, etc. Metals typically expand faster than silicon thus creating regions of high compressive stress in the substrate as well as inside the fill material.

Pet., 2; Reply, 2; *Birner*, ¶ [0023]; Thompson Decl. ¶ 49; Thompson-Supp. Decl. ¶¶ 7, 9

[0024] In various embodiments, the present invention overcomes these problems by reducing stress around the through substrate via by filling the through substrate via with an effective material with minimal thermal expansion. In various embodiments, the effective material comprises a combination of metal and voids. For example, metals typically expand faster than silicon, whereas voids, for example, filled with a gas having negligible expansion relative to the silicon substrate. Hence, a combination of metal with voids produces an effective material with a coefficient of expansion comparable to the substrate. In one embodiment, this effective material comprises a void tailored to specific dimensions and shape, the void forming an inner core region of the through substrate via, while a conductive fill material forms an outer layer of the through substrate via.

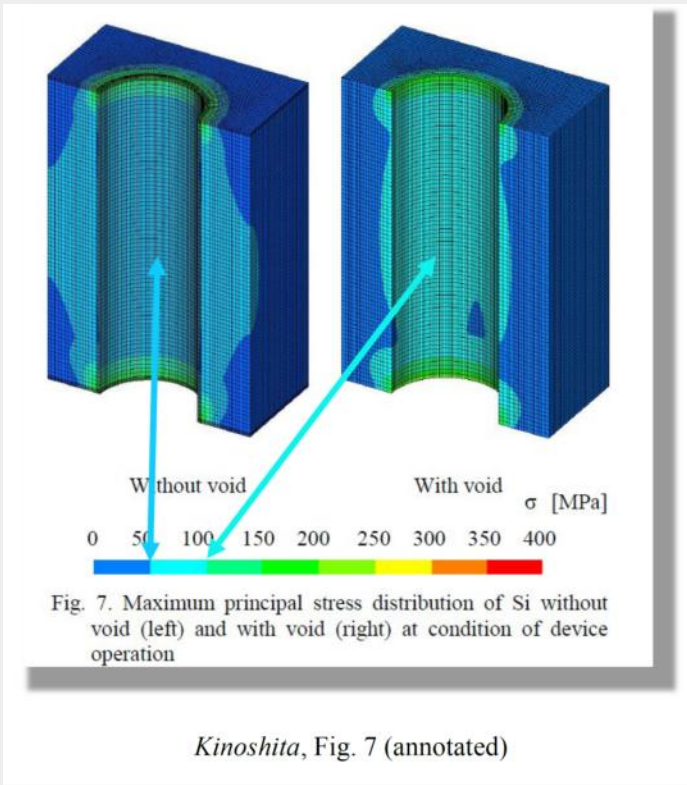
Pet., 2; Reply, 2-4; *Birner*, ¶ [0024]; Thompson Decl. ¶ 49; Thompson-Supp. Decl. ¶¶ 7, 12

Kinoshita Does Not Disclose That Some Voids Increase Stress

HID's Position

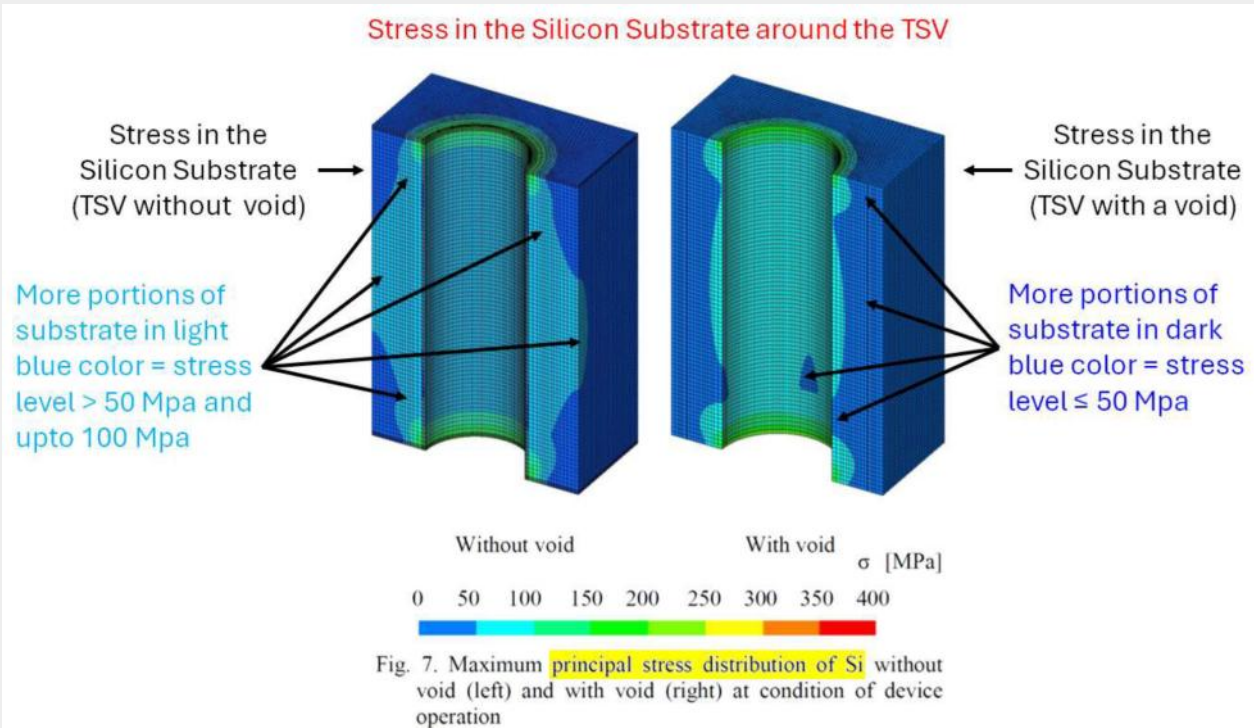
“Kinoshita discloses a TSV with a void that has higher thermal stress at equivalent temperatures than a TSV without a void.” Sur-Reply, 5

HID's Incorrect Interpretation



Sur-Reply, 8

Correct Interpretation



Reply, 6; Kinoshita, Fig. 7 (annotated)

HID Introduces New Arguments Not Included In The Patent Owner's Response

HID's NEW Position

“Critically, the Petition does not suggest that the optional void in Cooney could or should be modified to be of a size, shape, or other characteristic that would reduce thermal stress in the substrate.”

Sur-Reply, 19

[0055] FIG. 6 shows a liner layer 22 located and formed conformally upon the semiconductor structure of FIG. 5 and incompletely filling the extended aperture. FIG. 6 also shows a conductor layer 24 with an optional void 25 located therein, located and formed upon the liner layer 22 and completely filling the extended aperture.

Pet. 19; *Cooney*, ¶ [0055]; Thompson Decl. ¶ 121

In view of the well-known thermal stress relieving behavior of voids in TSVs filled with conductive materials, if not explicitly disclosed, a POSITA would have found it obvious to include a void enclosed in the conductor layer in *Cooney's* TSV to cause a reduction in the thermal stress in the surrounding substrate. Thompson, ¶133. A POSITA would have had a reasonable expectation

Pet. 22; Thompson Decl. ¶ 133