

PATENT APPLICATION COVER SHEET

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 COMMISSIONER FOR PATENTS
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Transmitted herewith is the patent application of:

ASSIGNEE: NEWPORT FAB, LLC DBA JAZZ SEMICONDUCTOR

Inventor(s): Hadi Jebory, David J. Howard, Scott B. Stetson

For: "Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate"

This application is a ☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____.

Enclosed are:

- ☒ Five (5) Sheets of drawings
- ☐ Request for Non-Publication (Form PTO/SB/35 (11-00))
- ☐ Separate Payment Form PTO-2038 for \$40.00 is Attached for Assignment of the invention to: _____
- ☐ The enclosed payment includes \$_____ for the recording of the assignment
- ☐ Information Disclosure Statement
- ☒ Application Data Sheet PTO/AIA/14
- ☒ Three (3) Declarations
- ☒ The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)
FOR:	No. Filled	No. Extra
BASIC FEE		
SEARCH FEE		
EXAMINATION FEE		
APPLICATION SIZE FEE (Total Number of Sheets)	(28 -100)/50 =	0
TOTAL CLAIMS	20 -20 =	0
INDEPENDENT CLAIMS	2 -3 =	0
MULTIPLE DEPENDENT CLAIMS PRESENTED		

If the difference in Col. 1 is less than zero,
 enter "0" in Col. 2

SMALL ENTITY

RATE	FEE
	\$140.00
	\$300.00
	\$360.00
x \$200.00 =	\$
x \$40.00 =	\$
x \$210.00 =	\$
+ \$390.00 =	\$
TOTAL	\$

**OTHER THAN A
SMALL ENTITY**

RATE	FEE
	\$280.00
	\$600.00
	\$720.00
x \$400.00 =	\$
x \$80.00 =	\$
x \$420.00 =	\$
+ \$780.00 =	\$
TOTAL	\$1,600.00

- ☒ Enclosed is a payment in the amount of \$1,600.00 by credit card.
- ☐ Please charge Deposit Account No. 50-0731 in the amount of \$ _____.
- ☒ The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Date:

1/27/2014



MICHAEL FARJAMI, ESQ.

Reg. No.: 38,135

Customer No.: 25700

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, CA 92691
(949) 282-1000

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being submitted electronically to the United States Patent and Trademark Office through the EFS Filing System, on 1/27/14.

EVAN C. GUNDERMAN
Name

Evan C. Gund
Signature

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0150176
		Application Number	
Title of Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Hadi		Jebory		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Irvine	State/Province	CA	Country of Residence	US
Mailing Address of Inventor:					
Address 1	36 Valente				
Address 2					
City	Irvine	State/Province	CA		
Postal Code	92602	Country	US		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	David	J.	Howard		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Irvine	State/Province	CA	Country of Residence	US
Mailing Address of Inventor:					
Address 1	19 Springwater				
Address 2					
City	Irvine	State/Province	CA		
Postal Code	92604	Country	US		
Inventor 3					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Scott	B.	Stetson		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0150176		
		Application Number			
Title of Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate				
City	Huntington Beach	State/Province	CA	Country of Residence	US
Mailing Address of Inventor:					
Address 1	9911 Big Sur Drive				
Address 2					
City	Huntington Beach	State/Province	CA		
Postal Code	92646	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	25700
Email Address	Add Email Remove Email

Application Information:

Title of the Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		
Attorney Docket Number	0150176	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

EES Web 2.2.0

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		Application Number	
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Customer Number	25700		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Claims benefit of provisional	61776063	2013-03-11

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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		Application Number	
Title of Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.		
Applicant 1		
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear		
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor:		
If the Applicant is an Organization check here. ☒		
Organization Name	Newport Fab, LLC dba Jazz Semiconductor	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0150176
		Application Number	
Title of Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		

Mailing Address Information For Applicant:			
Address 1		4321 Jamboree Road	
Address 2			
City	Newport Beach	State/Province	CA
Country	US	Postal Code	92660
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

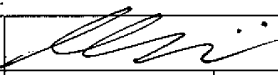
Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0150176
		Application Number	
Title of Invention	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature				Date (YYYY-MM-DD)	2014-01-27
First Name	Michael	Last Name	Farjami	Registration Number	38135
Additional Signature may be generated within this form by selecting the Add button.					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of
Invention**

**ANCHOR VIAS FOR IMPROVED BACKSIDE METAL ADHESION TO
SEMICONDUCTOR SUBSTRATE**

As the below named inventor, I declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT International application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Hadi Jebory

Date: Jan, 20th, 2014

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.
Use an addition PTO/AIA/01 form for each additional inventor

37 C.F.R. Section 1.56 - Duty to disclose information material to patentability.

A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

Prior art cited in search reports of a foreign patent office in a counterpart application, and

The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

It refutes, or is inconsistent with, a position the applicant takes in:

Opposing an argument of unpatentability relied on by the Office, or

Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

Each inventor named in the application;

Each attorney or agent who prepares or prosecutes the application; and

Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	ANCHOR VIAS FOR IMPROVED BACKSIDE METAL ADHESION TO SEMICONDUCTOR SUBSTRATE
-------------------------------	--

As the below named inventor, I declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT International application number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I acknowledge the duty to disclose information, which is material to patentability of this application as defined in Section 1.56 of Title 37, Code of Federal Regulations (see the last page attached hereto).

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

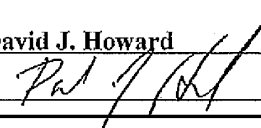
WARNING:

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LEGAL NAME OF INVENTOR

Inventor: David J. Howard

Date: 2014.01.20TH

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an addition PTO/AIA/01 form for each additional inventor

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Each inventor named in the application;

Each attorney or agent who prepares or prosecutes the application; and

Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

DJH
2014/1/20

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
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Title of
Invention

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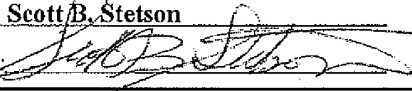
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LEGAL NAME OF INVENTOR

Inventor: Scott B. Stetson

Date: 1-20-2014

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.
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Prior art cited in search reports of a foreign patent office in a counterpart application, and

The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

It refutes, or is inconsistent with, a position the applicant takes in:

Opposing an argument of unpatentability relied on by the Office, or

Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

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Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

**UNITED STATES PATENT APPLICATION
FOR**

**ANCHOR VIAS FOR IMPROVED
BACKSIDE METAL ADHESION TO
SEMICONDUCTOR SUBSTRATE**

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12JAZ0008

BACKGROUND

The present application claims the benefit of and priority to a provisional patent application entitled "Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate", Serial Number 61/776,063, filed on March 11, 2013. The disclosure in this provisional application is hereby incorporated fully by reference into the present application.

Semiconductor substrate density has continuously increased, and continues to increase. Further miniaturization and increased density in semiconductor substrates has typically relied on a backside metal layer attached to the substrate to provide a common ground for the increasing number of active components on the semiconductor substrate. However, to ensure high fabrication yields the backside metal layer must remain securely attached to the substrate throughout the entire fabrication process and then for years during operation.

One conventional method of adhering a backside metal layer to a substrate relies on forming a backside metal stack having several layers, the first of which must form an adhesive bond with the substrate. For example, an interface layer may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer. However, fabrication procedures such as semiconductor die singulation and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die. Because adhesion of the backside metal stack to the substrate is almost entirely dependent on the adhesive qualities between the substrate and the interface layer, unacceptably low yields are often

achieved during fabrication due to the backside metal layer peeling from the semiconductor substrate.

SUMMARY

The present disclosure is directed to anchor vias for improved backside metal adhesion to a semiconductor substrate, substantially as shown in and/or described in connection with at least one of the figures, and as set forth more completely in the claims.

5

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A presents an exemplary diagram disclosing a cross-section of a semiconductor structure having anchor vias for improved backside metal adhesion, in accordance with an implementation of the present application.

5 Figure 1B presents an exemplary diagram disclosing a magnified cross-section of a portion of an anchor via for improved backside metal adhesion, in accordance with an implementation of the present application.

Figure 2A presents an exemplary diagram disclosing a backside view of a semiconductor structure having anchor vias for improved backside metal adhesion, in
10 accordance with an implementation of the present application.

Figure 2B presents an exemplary diagram disclosing a magnified view of through silicon vias (TSVs).

Figure 2C presents an exemplary diagram disclosing a magnified view of anchor vias disposed in a straight-line configuration for improved backside metal adhesion, in
15 accordance with an implementation of the present application.

Figure 2D presents an exemplary diagram disclosing a magnified view of anchor vias disposed in a staggered configuration for improved backside metal adhesion, in accordance with an implementation of the present application.

Figure 3A presents an exemplary diagram disclosing a backside view of a
20 semiconductor structure having clusters of anchor vias for improved backside metal adhesion, in accordance with another implementation of the present application.

Figure 3B presents an exemplary diagram disclosing a magnified view of a cluster of anchor vias for improved backside metal adhesion, in accordance with an implementation of the present application.

Figure 3C presents an exemplary diagram disclosing a magnified top side view of a semiconductor structure having anchor vias straddling a seal ring for improved backside metal adhesion, in accordance with an implementation of the present application.

Figure 3D presents an exemplary diagram disclosing a magnified top side view of a semiconductor structure having anchor vias adjacent to a seal ring for improved backside metal adhesion, in accordance with another implementation of the present application.

Figure 3E presents an exemplary diagram disclosing a magnified top side view of a semiconductor structure having anchor vias adjacent to a seal ring for improved backside metal adhesion, in accordance with another implementation of the present application.

15

DETAILED DESCRIPTION

The following description contains specific information pertaining to implementations in the present disclosure. One skilled in the art will recognize that the present disclosure may be implemented in a manner different from that specifically
5 discussed herein. The drawings in the present application and their accompanying detailed description are directed to merely exemplary implementations. Unless noted otherwise, like or corresponding elements among the figures may be indicated by like or corresponding reference numerals. Moreover, the drawings and illustrations in the present application are generally not to scale, and are not intended to correspond to actual
10 relative dimensions.

The present inventive concepts utilize one or more anchor vias fabricated along the periphery of a semiconductor substrate and bonded to the backside metal layer to improve backside metal adhesion to the semiconductor substrate. Advantages of the present inventive concepts include a substantial reduction in peeling backside metal
15 layers, increased RF performance, increased fabrication yields, and more robust semiconductor substrates and devices, as will be explained in more detail below.

Figure 1A presents an exemplary diagram disclosing a cross-section of a semiconductor structure having anchor vias for improved backside metal adhesion, in accordance with an implementation of the present application. Figure 1A discloses
20 semiconductor structure 100, including semiconductor substrate 110 having top surface 111, or front side, and bottom surface 112, or backside, after a backside grind or polish and deposition of a backside metal stack 150. As is customary in semiconductor

fabrication, front side processes may be performed on semiconductor substrate 110 before backside processes. However, for the purpose of illustration, any material layers formed during a front side process are not shown in Figure 1A. Figure 1A shows group 120 of through silicon vias (TSVs) as well as anchor via 132 and anchor via 133. Each
5 may be formed in semiconductor substrate 110 and may be filled with a metal filler, such as tungsten or titanium for example. As shown in Figure 1A, group 120 of TSVs is formed in a core region of semiconductor substrate 110, while each of anchor vias 132 and 133 are formed in a peripheral region of semiconductor substrate 110. Metal filler within group 120 of TSVs provide low resistance, low inductance ground connections to
10 one or more active devices fabricated in and/or on semiconductor substrate 110 and may be electrically connected to an overlying metal layer, such as a metal 1 layer for example, for grounding active devices such as the emitters of bipolar transistors.

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices and instead provides physical anchor points between
15 semiconductor substrate 110 and the underlying backside metal stack 150, which may be formed on bottom side 112 of semiconductor substrate 110 as shown in more detail in Figure 1B. Each of anchor vias 132 and 133 may be formed to a depth d_0 of 100 μ m into semiconductor substrate 110. However, anchor vias 132 and 133 are not so limited and d_0 may be greater or less than this value, according to the particular application. In
20 addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the metal filler within

anchor vias 132 and 133 essentially has a floating voltage potential during operation.

Where the metal filler within anchor vias is connected to an overlying metal layer, the anchor vias may provide increased holding strength due to the additional physical connection to the overlying metal layer.

5 Figure 1B presents an exemplary diagram disclosing a magnified cross-section of a portion of an anchor via for improved backside metal adhesion, in accordance with an implementation of the present application. For example, Figure 1B shows magnified view 130 including anchor via 132 and backside metal stack 150 formed on bottom side 112 of semiconductor substrate 110. Insulating layer 135 may optionally be formed
10 within anchor via 132 before metal filler 134 is deposited in applications where substantial isolation between semiconductor substrate 110 and metal filler 134 is desired. Insulating layer 135 may be a dielectric layer such as silicon dioxide, for example. As shown in Figure 1B, metal filler 134 may protrude from bottom side 112 to form protruding portion 136 such that when interface layer 152 is deposited on bottom side
15 112 of semiconductor substrate 110 the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond. Metal filler 134 may be tungsten, titanium, or any other suitable metal filler. Interface layer 152 may be formed from metals such as titanium or chrome-vanadium. Conduction layer 154 may then be formed on interface layer 152 using metals such as nickel or copper. Packaging
20 layer 156 may then be formed on conduction layer 154 using metals such as gold or silver to provide a very low resistance contact surface. Packaging layer 156 may subsequently be connected to one or more contacts, such as contact 158 for example, which may be a

solder bump on a semiconductor package or on a printed circuit board (PCB), or a metal epoxy or a solid metal contact. Though the thickness of each of interface layer 152, conduction layer 154, and packaging layer 156 may vary, backside metal stack 150 may have a total thickness d_1 of between $0.5\mu\text{m}$ and $3.0\mu\text{m}$. However, backside metal stack 5 150 is not so limited and may have a thickness outside this range, according to the requirements of a particular application. Moreover, the present application contemplates implementations including one or more of interface layer 152, conductive layer 154, and/or packaging layer 156. Thus, any of these layers in isolation or in combination may be interchangeable with the term backside metal stack or backside metal layer.

10 Moreover, the metals disclosed above for each of interface layer 152, conductive layer 154, and packaging layer 156 are exemplary only and may include any appropriate metals according to the particular application.

Figure 2A presents an exemplary diagram disclosing a backside view of a semiconductor structure having anchor vias for improved backside metal adhesion, in accordance with an implementation of the present application. For example, view 200 15 may correspond to a view of the structure shown in Figure 1A taken at plane 2A-2A' and in the direction of the arrows. Likewise, Figure 1A may correspond to a view of the structure shown in Figure 2A taken at plane 1A-1A' and in the direction of the arrows. For simplicity of illustration, Figure 2A provides a backside view of semiconductor 20 substrate 210 after a backside grind or polish and before application of a backside metal stack. Semiconductor substrate 210 may include group 220 of TSVs and several anchor vias, such as anchor via 232a, anchor via 232b, and anchor via 232c. Although several

anchor vias are shown along the edges and in the corners of semiconductor substrate 220, the present inventive concepts may include at least one anchor via placed in at least one corner of the semiconductor substrate. In the alternative, two, four or any other suitable number of anchor vias may be formed in straight or staggered lines, or in specially oriented clusters at each corner and/or along the periphery of semiconductor substrate 210. Figure 2A further shows dicing street 242, dicing street 244, dicing street 246 and dicing street 248, which delineate portions of the semiconductor substrate which are removed in order to singulate semiconductor substrate 210 into a semiconductor die. As stated above, singulation of semiconductor substrate 210 without the use of anchor vias may result in a backside metal stack peeling from the edges and/or corners of the substrate.

Figure 2B presents an exemplary diagram disclosing a magnified view of group 220 of TSVs as shown in Figure 2A. Although the specific pattern of TSVs shown in Figure 2A includes a group of 9 TSVs, for simplicity of illustration, only the central three darker shaded TSVs shown in Figure 2A are shown in Figure 2B. For example, group 220 of TSVs may include TSV 222a, TSV 222b and TSV 222c. Each of TSVs 222a through 222c may have a length d_2 of approximately $8\mu\text{m}$ and a width d_4 of approximately $3\mu\text{m}$. However, TSVs 222a through 222c are not so limited and may have larger or smaller dimensions according to a specific application. As shown, TSVs 222a through 222c may have alternating orientations such that each TSV has a perpendicular orientation with respect to an adjacent TSV. In addition, each of TSVs 222a through 222c may be separated from one another by a distance d_3 of approximately $6\mu\text{m}$.

Because forming each via requires the removal of the semiconductor material at that location, forming too many vias too close together may result in an undesirable perforating effect within the semiconductor substrate, thus forming a cleavage plane. Accordingly, to avoid forming such a cleavage plane, a linear density of metal filler

5 within each anchor via with respect to the substrate, measured across the top surface or bottom surface of semiconductor substrate 210, should desirably be less than 10% of the total linear distance of a straight or staggered line along the periphery of the semiconductor substrate that includes the anchor vias, and most preferably less than 2% of such a total linear distance. In addition, the area of the anchor vias should account for

10 less than approximately 0.5% of the total semiconductor substrate area to avoid adversely affecting subsequent front side processes. However, with respect to group 220 of TSVs, having the dimensions $d_2=8\mu\text{m}$, $d_3=6\mu\text{m}$, and $d_4=3\mu\text{m}$, the total linear density is:

$$(8\mu\text{m}+3\mu\text{m})/(8\mu\text{m}+6\mu\text{m}+3\mu\text{m}+6\mu\text{m}) = 11\mu\text{m}/23\mu\text{m} = \sim 48\%$$

With a linear density of 48% group 220 of TSVs may introduce one or more

15 cleavage planes into semiconductor substrate 210 making the substrate susceptible to breakage.

Figure 2C presents an exemplary diagram disclosing a magnified view of anchor vias disposed in a straight-line configuration for improved backside metal adhesion, in accordance with an implementation of the present application. For example, view 230a

20 may correspond to 230 of Figure 2A. Figure 2C shows anchor via 232a, anchor via 232b and anchor via 232c formed in the periphery of semiconductor substrate 210 along a straight line delineated by plane 235. Each of anchor vias 232a through 232c may have a

length d_5 of $8\mu\text{m}$ and a width d_7 of $3\mu\text{m}$. However, anchor vias 232a through 232c are not so limited and may have lengths and widths different from those discussed above and/or different from one anchor via to the next. In order to reduce the linear density of the anchor vias, each anchor-via may be spaced from an adjacent anchor via by a large distance relative to its length. For example, Figure 2C shows each of anchor vias 232a through 232c separated from adjacent anchor vias by a distance d_6 of approximately $100\mu\text{m}$. However, this distance d_6 may be greater or less than $100\mu\text{m}$ depending on the specific application. Thus, by separating each anchor via sufficiently, a linear density of less than 10% may be achieved, avoiding formation of undesirable cleavage planes in semiconductor substrate 210, while still preventing peeling of the backside metal stack. For example, with the above dimensions $d_5=8\mu\text{m}$ and $d_6=100\mu\text{m}$, the total linear density of anchor vias 232a through 232c is:

$$(8\mu\text{m})/(8\mu\text{m}+100\mu\text{m}) = 8\mu\text{m}/108\mu\text{m} = \sim 7\%$$

In the alternative, to further reduce the incidence of cleavage planes in the semiconductor substrate, anchor vias may be staggered from one another with respect to their perpendicular distance to the proximate edges of the semiconductor substrate. For example, Figure 2D presents an exemplary diagram disclosing a magnified view of anchor vias disposed in a staggered configuration for improved backside metal adhesion, in accordance with an implementation of the present application. For example, view 230b may also correspond to 230 of Figure 2A. The anchor vias of Figure 2D may correspond, respectively, to each of the anchor vias of Figure 2C in all respects with the exception that anchor vias 232a through 232c are alternately formed in a staggered

configuration along plane 235 and plane 236, which may be offset from plane 235 by a predetermined distance d_8 measured perpendicular to the proximate edge of semiconductor substrate 210. The precise value of d_8 may vary depending on the specific application. Thus, the orientation shown in Figure 2D may prevent backside metal stack peeling while further resisting the formation of cleavage planes within the semiconductor substrate by staggering the placement of the anchor vias with respect to the proximate edge of the semiconductor substrate in addition to ensuring a linear density of less than approximately 10%.

In addition to causing cleavage planes near the dicing streets, having too many anchor vias around the periphery of the semiconductor substrate may adversely affect RF performance. Specifically, forming too many anchor vias around the periphery of the semiconductor substrate may effectively form a faraday cage around the substrate, cancelling the electric field within the cage. Thus, the least number of anchor vias should be fabricated that will satisfactorily prevent peeling of the backside metal stack during fabrication and subsequent operation. Accordingly, forming just one anchor via, or a small cluster of anchor vias near the corners of the semiconductor substrate may be desirable.

Figure 3A presents an exemplary diagram disclosing a backside view of a semiconductor structure having clusters of anchor vias for improved backside metal adhesion, in accordance with another implementation of the present application. For simplicity of illustration, Figure 3A provides a backside view 300 of semiconductor substrate 310 after a backside grind or polish and before application of a backside metal

stack. Figure 3A shows semiconductor substrate 310 having group 220 of TSVs and several clusters of anchor vias, such as cluster 330 of anchor vias. Figure 3A further shows dicing street 342, dicing street 344, dicing street 346 and dicing street 348, which delineate portions of semiconductor substrate 310 which are removed for singulation. As stated above, singulation of semiconductor substrate 310 without the use of anchor vias may result in a backside metal stack peeling from the edges and/or corners of the die. Thus, cluster 330 of anchor vias may be fabricated proximate to a corner of semiconductor substrate 310 in order to prevent the backside metal stack from peeling at the corners of the die.

Figure 3B presents an exemplary diagram disclosing a magnified view of a cluster of anchor vias for improved backside metal adhesion, in accordance with an implementation of the present application. For example, within Figure 3B cluster 330 of anchor vias may correspond to cluster 330 of anchor vias shown in Figure 3A. Cluster 330 of anchor vias may include anchor via 332a, anchor via 332b, anchor via 332c, and anchor via 332d. Each of anchor vias 332a through 332d may have a width d_7 of approximately $3\mu\text{m}$, a length d_5 of approximately $8\mu\text{m}$, and may be spaced from adjacent anchor vias by a predetermined distance d_9 . Though distance d_9 may vary according to the specific application, values of less than $10\mu\text{m}$ may be preferred in order to consolidate the peel-resistance in the corners of the semiconductor substrate. In addition, each of anchor vias 332a through 332d may be oriented in a perpendicular direction to each adjacent anchor via, thus further reducing the probability of forming a cleavage plane. The use of a cluster of anchor vias allows for the use of fewer total anchor vias,

while concentrating the “holding power” at the corners, where the stresses prompting backside metal peeling are greatest.

In another implementation, where seal rings are utilized on a front side of the semiconductor substrate to prevent cracks from spreading into the substrate during singulation, such anchor vias or clusters of anchor vias may be formed adjacent to or straddling the seal ring, as shown in Figures 3C through 3E.

Figure 3C presents an exemplary diagram disclosing a magnified top side view of a semiconductor structure having anchor vias straddling a seal ring for improved backside metal adhesion, in accordance with an implementation of the present application. For example, magnified view 360a may show seal ring 370 fabricated in a front side process for preventing cracks from spreading into semiconductor substrate 310 during singulation. Clusters 330a, 330b and 330c of anchor vias may be formed adjacent to a proximate edge of semiconductor substrate 310 and straddling seal ring 370. Each of clusters 330a through 330c of anchor vias may correspond to cluster 330 of anchor vias shown in Figure 3A. Cluster 330a of anchor vias may be formed a predetermined distance d_{10} from the corner of semiconductor substrate 310m which may vary depending on the particular application. Moreover, each of clusters 330a through 330c of anchor vias may be separated from an adjacent cluster by a distance d_{11} , which may be approximately $100\mu\text{m}$. However, distance d_{11} is not so limited and may have a value greater or less than this value depending on the particular application. However, care must be taken to ensure a linear density of substantially less than 10% and preferably less

than 2%, while limiting the total surface area of all clusters of anchor vias to less than approximately 0.5% of the total die area, as described above.

Figure 3D presents an exemplary diagram disclosing a magnified top side view of a semiconductor structure having anchor vias adjacent to a seal ring for improved
5 backside metal adhesion, in accordance with another implementation of the present application. All elements of Figure 3D may be identical to those as described in Figure 3C, with the exception that each of clusters 330a, 330b and 330c of anchor vias may be disposed adjacent to and along an inner perimeter of seal ring 370.

Figure 3E presents an exemplary diagram disclosing a magnified top side view of
10 a semiconductor structure having anchor vias adjacent to a seal ring for improved backside metal adhesion, in accordance with another implementation of the present application. All elements of Figure 3E may be identical to those as described in Figure 3C, with the exception that each of clusters 330a, 330b and 330c of anchor vias may be disposed adjacent to and along an outer perimeter of seal ring 370.

15 Thus, the present inventive concepts utilize one or more anchor vias or clusters of anchor vias disposed along a perimeter and/or at the corners of a semiconductor substrate to prevent undesired peeling of a backside metal stack from the die. Application of such anchor vias for preventing backside metal stack peeling may be extremely beneficial for technologies in which an unpatterned backside metal layer is utilized, such as in the
20 power amplifier and wireless communications markets. Advantages of the present inventive concepts may include substantially reduced incidence of peeling backside metal

layers, increased RF performance, increased fabrication yields, and more robust semiconductor substrates and devices.

From the above description it is manifest that various techniques can be used for implementing the concepts described in the present application without departing from the scope of those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

CLAIMS

1. A structure comprising:
at least one anchor via disposed in at least one corner of a semiconductor
substrate;
5 a metal filler within said at least one anchor via, said metal filler having a
protruding portion extending from a backside of said semiconductor substrate;
a backside metal layer on a bottom surface of said semiconductor substrate, said
backside metal layer being bonded to said protruding portion of said metal filler of said at
least one anchor via.
10
2. The structure of claim 1, wherein said at least one anchor via comprises a
cluster of anchor vias.
3. The structure of claim 2, wherein each anchor via within said cluster of anchor
15 vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.
4. The structure of claim 1, wherein said at least one anchor via comprises a
plurality of anchor vias disposed in a straight line along a periphery of said
semiconductor substrate.

20

5. The structure of claim 4, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

5 6. The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

7. The structure of claim 1, wherein a total area of said at least one anchor via is
10 less than approximately 0.5% of a total area of said semiconductor substrate.

8. The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

15 9. The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

10 10. The structure of claim 1, further comprising an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via.

11. A method comprising:

forming at least one anchor via in at least one corner of a semiconductor substrate;

depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal

5 filler of said at least one anchor via.

12. The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.

10 13. The method of claim 12, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

14. The method of claim 11, wherein said forming said at least one anchor via
15 comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate.

15. The method of claim 14, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along
20 said periphery of said semiconductor substrate.

16. The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

5 17. The method of claim 11, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

18. The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of:

10 forming an interface layer;
 forming a conduction layer;
 forming a packaging layer.

19. The method of claim 11, further comprising bonding said metal filler within
15 said at least one anchor via to a metal layer overlying said semiconductor substrate.

20. The method of claim 11, further comprising forming an insulating layer between said semiconductor substrate and said metal filler in said at least one anchor via.

ABSTRACT

Disclosed is a structure having anchor vias for improved backside metal adhesion and an associated method for the structure's fabrication. The structure includes at least one anchor via disposed in at least one corner of a semiconductor substrate. A metal
5 filler may be formed within the at least one anchor via, the metal filler having a protruding portion extending from a backside of the semiconductor substrate. The structure may further include a backside metal layer on a bottom surface of the semiconductor substrate, the backside metal layer being bonded to the protruding portion of the metal filler in the at least one anchor via. The at least one anchor via may include
10 a cluster of anchor vias, a plurality of anchor vias disposed in a straight line and/or in a staggered configuration along a periphery of the semiconductor substrate.

Fig. 2A

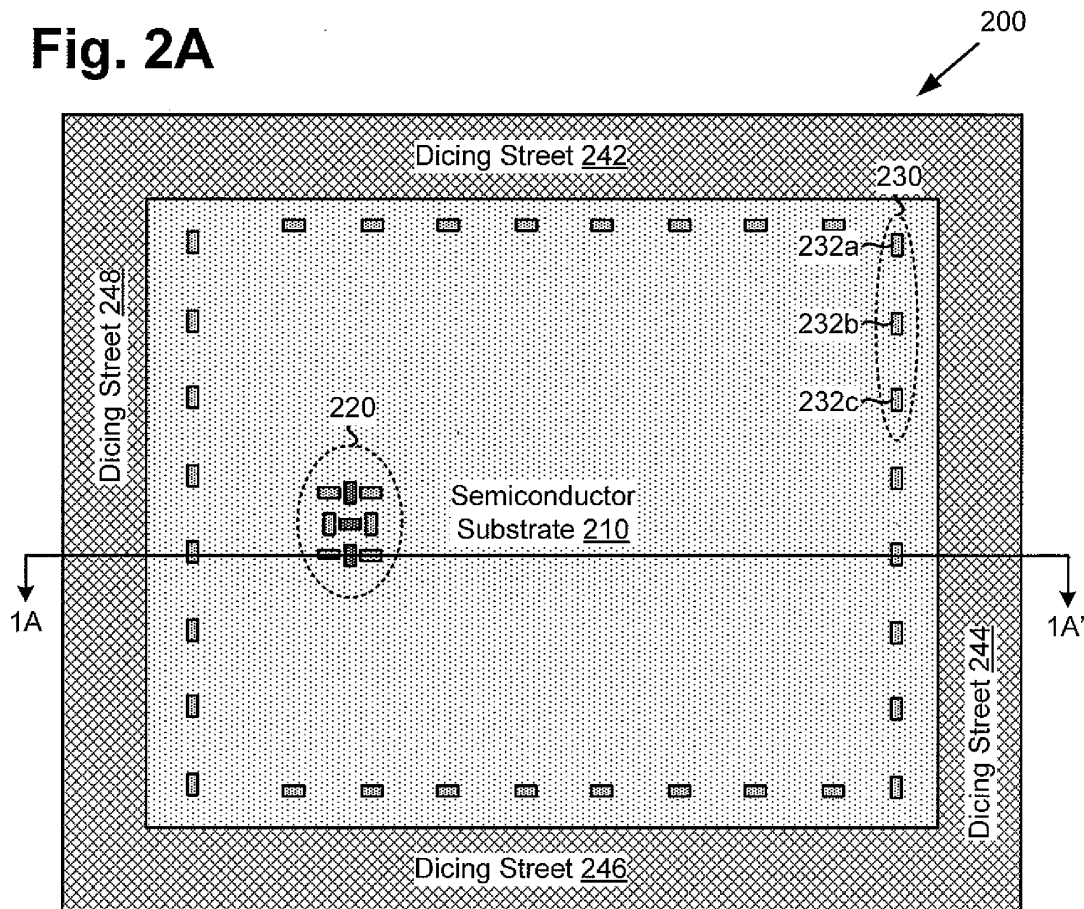


Fig. 2B

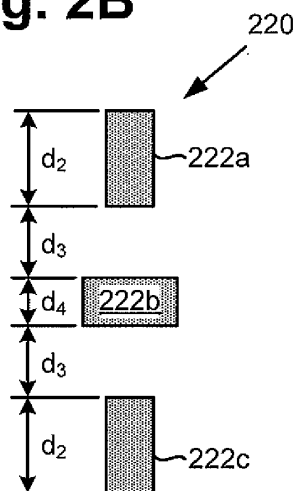


Fig. 2C

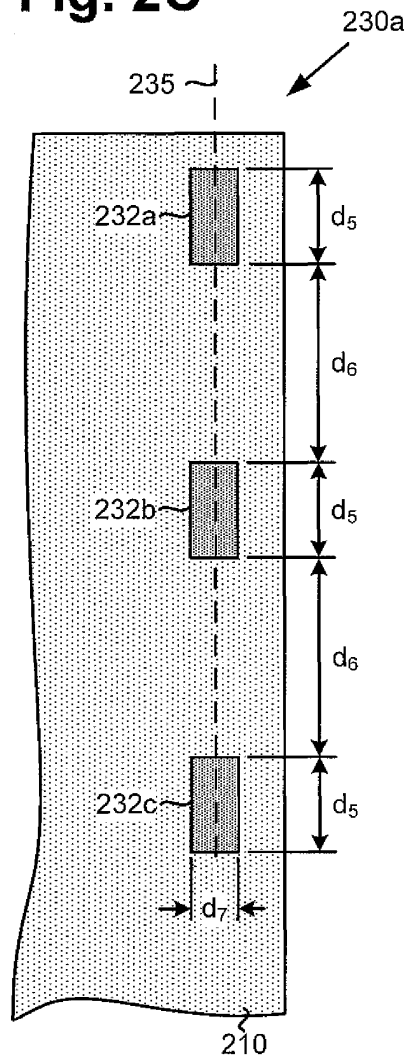


Fig. 2D

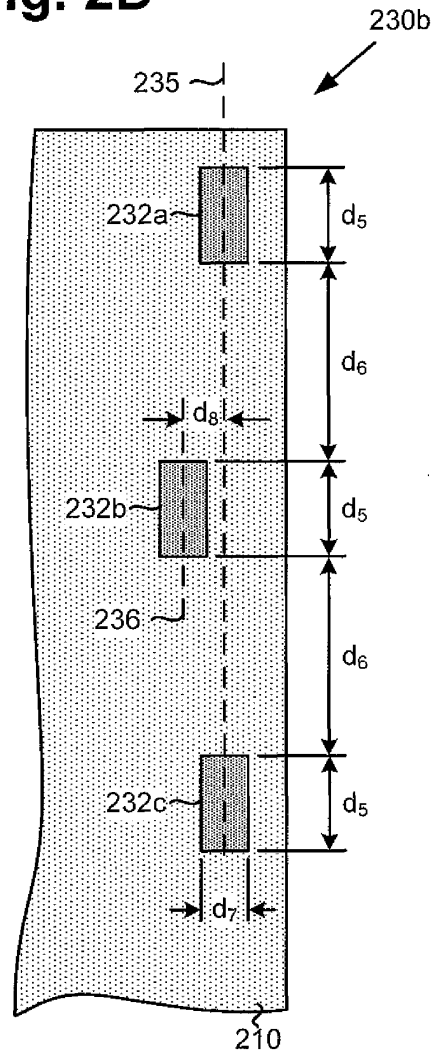


Fig. 3A

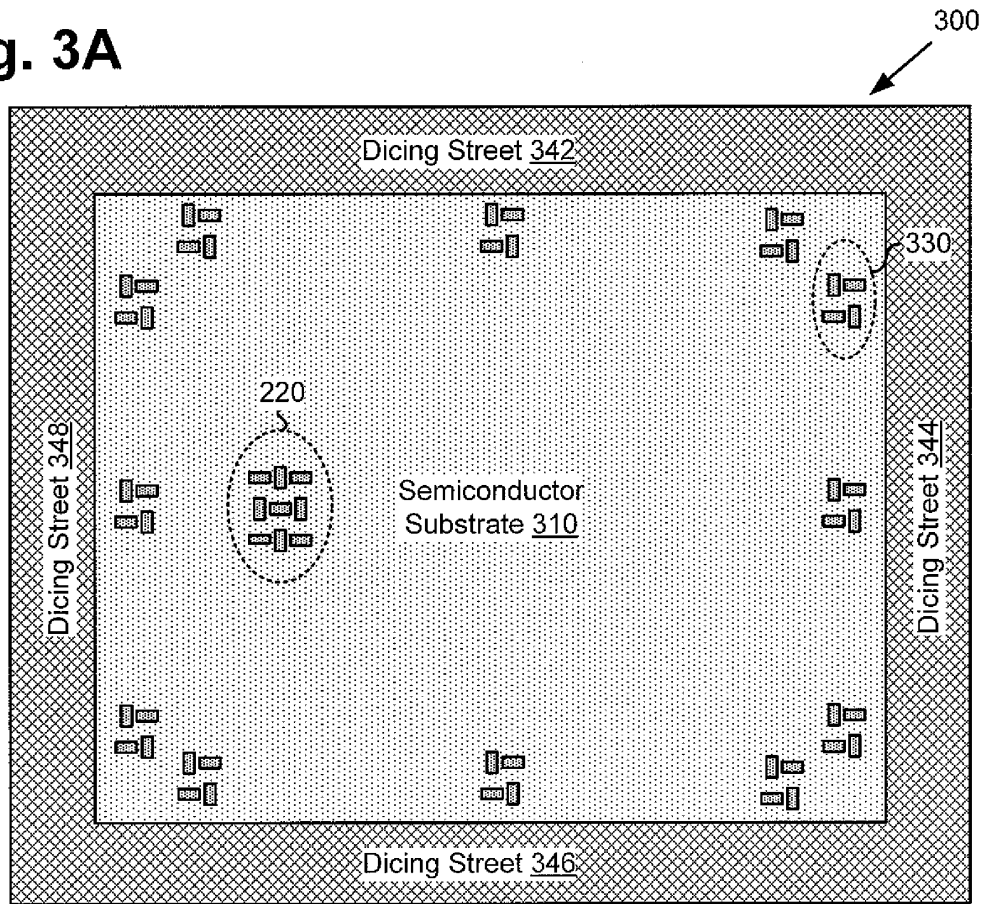


Fig. 3B

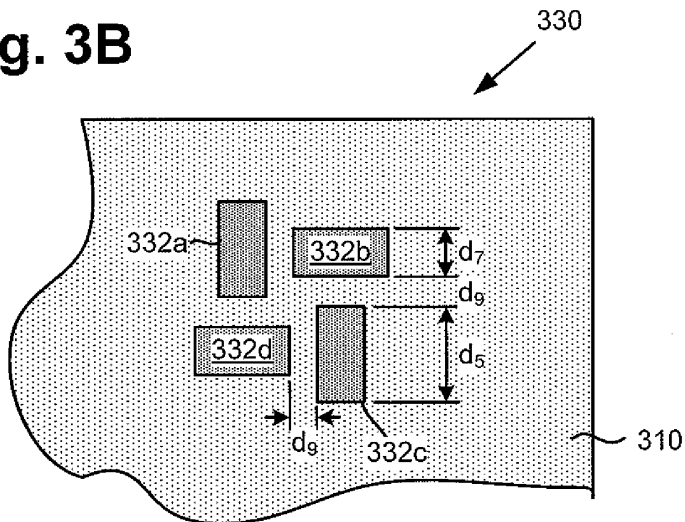


Fig. 3C

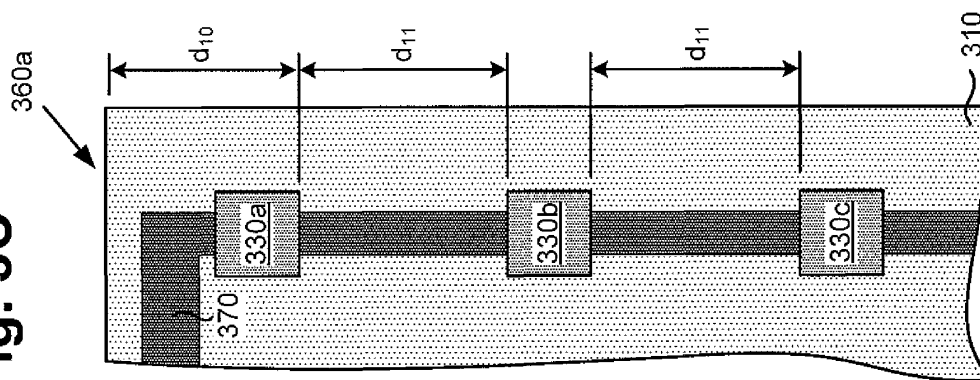


Fig. 3D

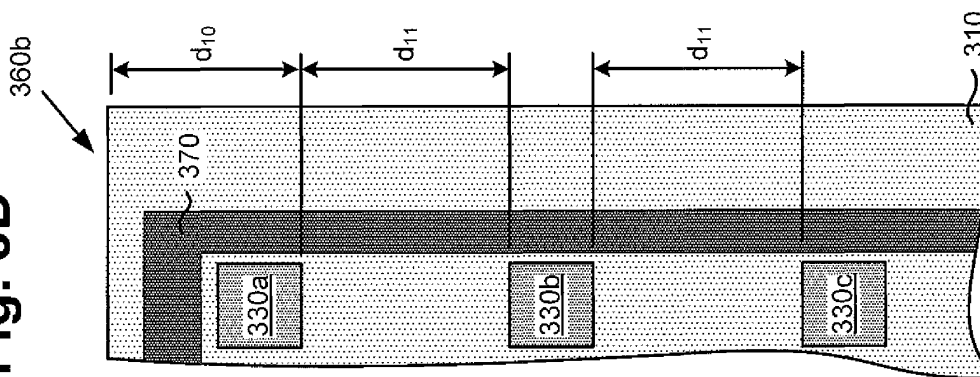
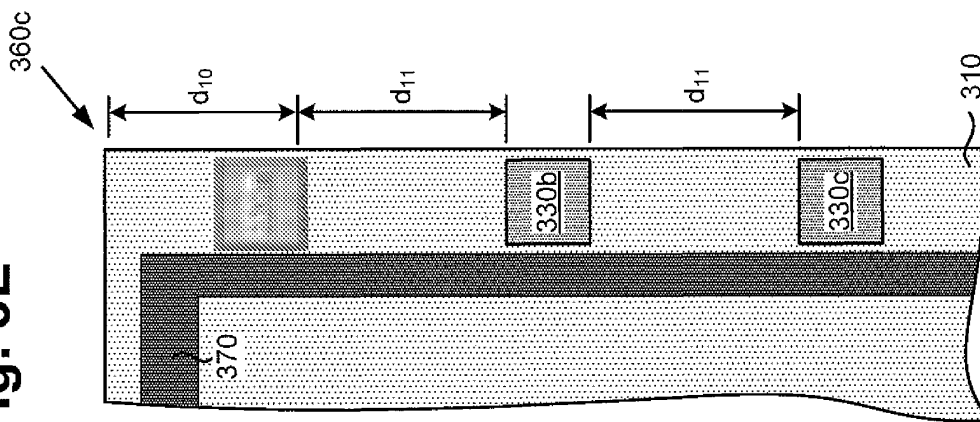


Fig. 3E



Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate		
First Named Inventor/Applicant Name:		Hadi Jebory		
Filer:		Michael Farjami/Evan Gunderman		
Attorney Docket Number:		0150176		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

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International Application Number:	
Confirmation Number:	4221
Title of Invention:	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate
First Named Inventor/Applicant Name:	Hadi Jebory
Customer Number:	25700
Filer:	Michael Farjami/Evan Gunderman
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Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	6797
Deposit Account	500731
Authorized User	FARJAMI, MICHAEL
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0150176_Patent_Application_As_Filed_Jan_27_14_EFS_MF.pdf	943911	yes	42
			9165af84c8e2c6eedb22a1e4263ca2225df5b17c		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal of New Application		1	2	
	Application Data Sheet		3	8	
	Oath or Declaration filed		9	14	
	Specification		15	32	
	Claims		33	36	
	Abstract		37	37	
	Drawings-only black and white line drawings		38	42	
	Warnings:				
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32786	no	2
			0aca49fe3dc87b7a03845fc217b8c945e0493b4		
Warnings:					
Information:					
Total Files Size (in bytes):			976697		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 14165377

Document Date: 01/27/2014

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (<http://Score.uspto.gov/ScoreAccessWeb/>).
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Form Revision Date: September 30, 2013

JAN 31 2014

PTO/AIA/80 (07-12)

Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒

Practitioners associated with Customer Number:

25700

OR

☐

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒

The address associated with Customer Number:

25700

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address: Newport Fab, LLC dba Jazz Semiconductor
4321 Jamboree Road
Newport Beach, CA 92660

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	<i>Allen R. Grogan</i>	Date	November 14, 2012
Name	Allen Grogan	Telephone	949-435-8000
Title	General Counsel of Newport Fab, LLC dba Jazz Semiconductor		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

JAN 31 2014

PTO/AIA/96 (08-12)

Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Attorney Docket No.: 0150176
Client Docket No.: 12JAZ0008

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Hadi Jebory, David J. Howard, Scott B. StetsonApplication No./Patent No.: 14/165,377 Filed/Issue Date: January 27, 2014Titled: Anchor Vias for Improved Backside Metal Adhesion to Semiconductor SubstrateNewport Fab, LLC dba Jazz Semiconductor, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3, or 4 below):

1. ☒ The assignee of the entire right, title, and interest
2. ☐ An assignee of less than the entire right, title and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:
- [Redacted Box]
- Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.
3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:
- [Redacted Box]
- Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.
4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified documents(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 032055, Frame 0839, or for which a copy thereof is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PAGE 3/4 * RCVD AT 1/31/2014 8:17:13 PM [Eastern Standard Time] * SVR:W-PTOFAX-001/11 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):01-11

PTO/AIA/96 (08-12)

Approved for use through 01/31/2013. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
4. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
5. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.
6. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.


Signature

Michael Farjami, Esq.
Printed or Typed Name

1/31/2014
Date

38,135
Title or Registration Number

[Page 2 of 2]

This collection of information is required by 37 CFR 3.73(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PAGE 4/4 * RCVD AT 1/31/2014 8:17:13 PM [Eastern Standard Time] * SVR:WPTOFAX-001/11 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm:ss):01:11

001/004
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JAN 31 2014



FARJAMI & FARJAMI LLP
AN INTELLECTUAL PROPERTY LAW FIRM

www.farjami.com

26522 La Alameda Avenue, Suite 360
Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: January 31, 2014

To: United States Patent and Trademark Office
Examiner: Unknown; Art Unit: Unknown

Fax: (571) 273-8300

Re: **Application Serial No.: 14/165,377**
Filing Date: 01/27/2014; First-Named Inventor: Jebory
Attorney Docket No.: 0150176

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 4

Message:

Enclosed please find:

- (1) Power of Attorney (Form PTO/AIA/80);
- (2) Statement Under 37 CFR 3.73(c) (Form PTO/AIA/96).

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/165,377	01/27/2014	Hadi Jebory	0150176

CONFIRMATION NO. 4221

POA ACCEPTANCE LETTER

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691



Date Mailed: 02/13/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/31/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/nguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/165,377	01/27/2014	2812	1600	0150176	20	2

CONFIRMATION NO. 4221

25700

FARJAMI & FARJAMI LLP

26522 LA ALAMEDA AVENUE, SUITE 360

MISSION VIEJO, CA 92691

FILING RECEIPT



OC000000066580919

Date Mailed: 02/13/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;
Scott B. Stetson, Huntington Beach, CA;

Applicant(s)

Newport Fab, LLC dba Jazz Semiconductor, Newport Beach, CA

Assignment For Published Patent Application

Newport Fab, LLC dba Jazz Semiconductor, Newport Beach, CA

Power of Attorney: The patent practitioners associated with Customer Number 25700

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/776,063 03/11/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 02/11/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/165,377**

Projected Publication Date: 09/11/2014

Non-Publication Request: No

Early Publication Request: No
Title

Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/165,377			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *			OR	x 80 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
			TOTAL			TOTAL	1600		
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
			TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))					OR			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR			
			TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/165,377	01/27/2014	Hadi Jebory	0150176

CONFIRMATION NO. 4221

PUBLICATION NOTICE

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691



OC00000070688742

Title:Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate

Publication No.US-2014-0252651-A1

Publication Date:09/11/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/165,377	01/27/2014	Hadi Jebory	0150176	4221
25700 7590 02/26/2015 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER CLARK, JASMINE JHIHAN B	
			ART UNIT 2816	PAPER NUMBER
			NOTIFICATION DATE 02/26/2015	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@farjami.com
farjamidocketing@yahoo.com
ffarjami@farjami.com

Office Action Summary	Application No. 14/165,377	Applicant(s) JEBORY ET AL.	
	Examiner JASMINE CLARK	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1,4,6,8-11,14,16 and 18-20 is/are rejected.
- 8) ☒ Claim(s) 2,3,5,7,12,13,15, and 17 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

1. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

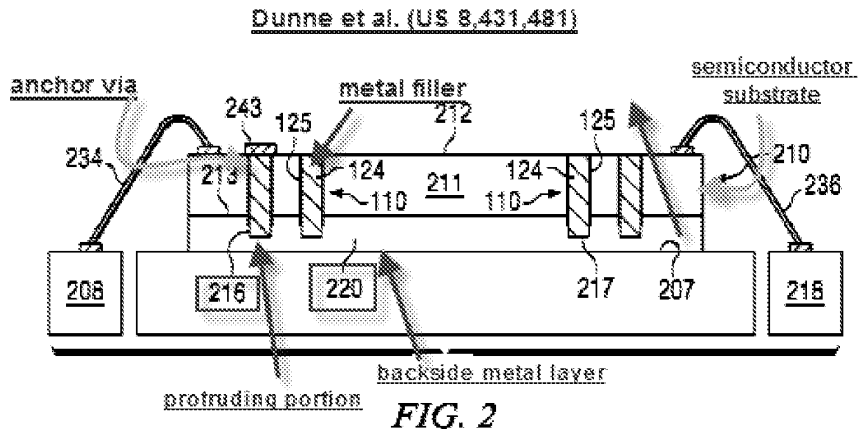
This application currently names joint inventors. In considering patentability of the claims under pre-AIA 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of pre-AIA 35 U.S.C. 103(c) and potential pre-AIA 35 U.S.C. 102(e), (f) or (g) prior art under pre-AIA 35 U.S.C. 103(a).

Claims 1, 4, 6, 8-11, 14, 16, and 18-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Dunne et al. (US 8,431,481) in view of Bai et al. (US 8,710,629).

At column 7, line 45 to column 8, line 15, i.e., **Dunne '481** teaches a structure comprising:

at least one anchor via disposed in a semiconductor substrate (210);

a metal filler (124) within said at least one anchor via, said metal filler having a



protruding portion (216, i.e.,) extending from a backside of said semiconductor substrate;

a backside metal layer (220) on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via. (Please see **Dunne's** Fig. 2 with interpretation labels shown above).

However, **Dunne '481** does not specifically teach disposing the at least one anchor via in at least one corner of the semiconductor substrate. **Bai '629** teaches comprising a through silicon vias (TSV) at corners of a semiconductor die to reduce warpage of the semiconductor die (see Fig. 5 of **Bai '629**).

It would have been obvious for **Dunne '481** to practice using the teaching of **Bai '629** by having the anchor vias in at least one corner of the semiconductor substrate for the same reason as taught by **Bai' 629**.

Re claim 4, the limitation therein “wherein said at least one anchor via comprises a plurality of anchor vias” is met by Fig. 2 of **Dunne ‘481** shown above. However, **Dunne ‘481** does not specifically show that the anchor vias are being disposed in a straight line along a periphery of said semiconductor substrate. It would have been obvious to rearrange the plurality of anchor vias in a straight line along a periphery of said semiconductor substrate, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Re claim 6, with regards to “wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate”, please see In re Japikse in the rejection of claim 4 above.

Re claim 8, the limitation therein “wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer” is met by Fig. 2 shown above which show the backside metal layer (220) which also serves as an interface layer.

Re claim 9, the limitation therein “wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate” is met by **Dunne’s** Fig. 2.

Re claim 10, the limitation therein “The structure of claim t, further comprising an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via” is met by Fig. 2 and column 4, lines 30-34, which shows a liner (125) which is a dielectric layer between the semiconductor substrate and the metal filler (124).

Re claim 11, the limitations therein “A method comprising:
forming at least one anchor via in a semiconductor substrate;
depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via” are met by, i.e., column 7, line 45 to column 8, line 15, and Fig. 2 of **Dunne ‘481**. Regarding “at least one anchor via is formed in at least one comer of a semiconductor substrate”, please see the discussion in the rejection of claim 1 above.

Re claims 14 and 16, with regards to “wherein said forming said at least one anchor via comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate” and “wherein said forming said at least one anchor via comprises forming a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate”, please see In re Japikse in the rejection of claim 4 above.

Re claim 18, the limitation therein “wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of forming an interface layer; forming a conduction layer; forming a packaging layer” is met as advanced above in the rejection of claim 8.

Re claim 19, the limitation therein “The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate” is met by **Dunne's** Fig. 2 shown above.

Re claim 20, the limitation therein “The method of claim t 1, further comprising forming an insulating layer between said semiconductor substrate and said metal filler in said at least one anchor via” is met as advanced above in the rejection of claim 10.

Allowable Subject Matter

2. Claims 2, 3, 5, 7, 12, 13, 15, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art(s) fail to further teach and/or suggest:

(i) wherein said at least one anchor via comprises a cluster of anchor vias as set forth in claims 2 and 12;

(ii) wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate as set forth in claims 5 and 15; and

(iii) wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate as set forth in claims 7 and 17.

Telephone Inquiry Contacts

Art Unit: 2816

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASMINE CLARK whose telephone number is (571)272-1726. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JASMINE CLARK/
Primary Examiner, Art Unit 2816

JC/02/22/2015

Notice of References Cited	Application/Control No. 14/165,377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.	
	Examiner JASMINE CLARK	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,431,481	04-2013	Dunne et al.	438/629
*	B	US-8,710,629	04-2014	Bai et al.	257/618
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2262	@py<="2013" and 257/e21.597.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 22:51
L3	115	@py<="2013" and 257/774.ccls. and ((through adj hole) or (via adj hole)) and backside and ((three adj dimensional) or 3D)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 23:30
L4	58	@py<="2013" and 438/629,630,637-640,668,672,675)/.ccls. and ((through adj hole) or (via adj hole)) and backside and ((three adj dimensional) or 3D)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 23:33
L5	126	@py<="2013" and 438/629,630,637-640,668,672,675)/.ccls. and ((through adj hole) or (via adj hole)) and backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 23:56
L6	9151	@py<="2013" and h01I21/76898.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/15 00:34
L7	3690	h01I21/76898.CPC. and (TSV or (via with hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/15 00:35
L8	1820	h01I21/76898.CPC. and (semiconductor adj substrate) and (TSV or (via with hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/15 00:36
L9	170	h01I21/76898.CPC. and ((semiconductor adj substrate) with backside) and (TSV or (via with hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/15 00:44
S1	752	@py<="2013" and 257/621.ccls. and ((TSV) or (through with via))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 01:45
S2	1498	@py<="2013" and 257/621.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 01:57

EAST Search History

S3	1	"7491582" and "72" and "buffer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 02:41
S4	1	"7491582" and "72" and "stress"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 02:43
S5	6	"7291899"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/14 20:23

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BIB DATA SHEET

CONFIRMATION NO. 4221

SERIAL NUMBER 14/165,377	FILING or 371(c) DATE 01/27/2014 RULE	CLASS 257	GROUP ART UNIT 2816	ATTORNEY DOCKET NO. 0150176		
APPLICANTS Newport Fab, LLC dba Jazz Semiconductor, Newport Beach, CA, Assignee (with 37 CFR 1.172 Interest); INVENTORS Hadi Jebory, Irvine, CA; David J. Howard, Irvine, CA; Scott B. Stetson, Huntington Beach, CA; ** CONTINUING DATA ***** This appln claims benefit of 61/776,063 03/11/2013 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/11/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JASMINE CLARK/</u> Examiner's Signature		☐ Met after Allowance JC Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691 UNITED STATES						
TITLE Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.
	Examiner JASMINE CLARK	Art Unit 2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	02/22/2015								
	1	✓								
	2	O								
	3	O								
	4	✓								
	5	O								
	6	✓								
	7	O								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	O								
	13	O								
	14	✓								
	15	✓								
	16	✓								
	17	O								
	18	✓								
	19	✓								
	20	✓								

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7	("7291899" "8710629").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 12:52
L2	1830	257/621.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 13:03
L3	326	257/774.ccls. and ((through adj silicon adj via) or TSV) and (back same metal\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 14:33
L4	4	"20120013022" and "13"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 15:48
L5	95	257/e21.597.ccls. and ((through adj silicon adj via) or TSV) and (back same metal\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 16:00
L6	137	438/629,630,637- 640,668,672,675)/.ccls. and ((through adj silicon adj via) or TSV) and (back same metal\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/02/22 16:03

2/ 22/ 2015 4:52:41 PM**C:\Users\jclark1\Documents\EAST\Workspaces\ ~ AutoSave.05-02-2014.wsp**

JUN 26 2015

Attorney Docket No.: 0150176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Jebory et al.**

Serial No.: 14/165,377

Filing Date: 01/27/2014

For: **Anchor Vias for Improved Backside
Metal Adhesion to Semiconductor
Substrate**

Art Unit: 2816

Examiner: Clark, Jasmine Jhihan B.

AMENDMENT AND RESPONSE TO *NON-FINAL* OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Non-Final* Office Action dated February 26, 2015 in the above-referenced patent application. Please enter and consider the following amendments and remarks.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

06/29/2015 APEREZAH 00000000 14165377

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Page 1

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Attorney Docket No.: 0150176

In the Claims:**Claim 1 (currently amended):** A structure comprising:

at least one anchor via disposed in at least one corner of a semiconductor substrate;

a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.**Claim 2 (original):** The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.**Claim 3 (original):** The structure of claim 2, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

Attorney Docket No.: 0150176

Claim 4 (original): The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a straight line along a periphery of said semiconductor substrate.

Claim 5 (original): The structure of claim 4, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

Claim 6 (original): The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

Claim 7 (original): The structure of claim 1, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

Claim 8 (original): The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

Claim 9 (original): The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

Attorney Docket No.: 0150176

Claim 10 (original): The structure of claim 1, further comprising an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via.

Claim 11 (currently amended): A method comprising:
forming at least one anchor via in at least one corner of a semiconductor substrate;
depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;
wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

Claim 12 (original): The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.

Claim 13 (original): The method of claim 12, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

Attorney Docket No.: 0150176

Claim 14 (original): The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate.

Claim 15 (original): The method of claim 14, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

Claim 16 (original): The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

Claim 17 (original): The method of claim 11, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

Claim 18 (original): The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of:

- forming an interface layer;
- forming a conduction layer;

Attorney Docket No.: 0150176

forming a packaging layer.

Claim 19 (original): The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate.

Claim 20 (original): The method of claim 11, further comprising forming an insulating layer between said semiconductor substrate and said metal filler in said at least one anchor via.

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JUN 26 2015

Attorney Docket No.: 0150176

REMARKS

Prior to the present amendment and response, claims 1-20 were pending in the present application. Claims 2, 3, 5, 7, 12, 13, 15 and 17 are allowable if rewritten in independent form including all of the limitations of its base claim and any intervening claims. By the present amendment and response, Applicants have amended claims 1 and 11. Thus, after the present amendment and response, claims 1-20 remain pending in the present application. Applicants respectfully request reconsideration and allowance of claims 1, 4, 6, 8-11, 14, 16 and 18-20 in view of the above amendments and the following remarks.

A. Rejection of Claims 1, 4, 6, 8-11, 14, 16 and 18-20 under pre-AIA 35

U.S.C. § 103(a)

In the *Non-Final* Office Action, dated February 26, 2015 (hereinafter "Office Action"), the Examiner rejects claims 1, 4, 6, 8-11, 14, 16 and 18-20 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable for purported obviousness over U.S. Patent Number 8,431,481 to Dunne et al. (hereinafter "Dunne") in view of U.S. Patent Number 8,710,629 to Bai et al. (hereinafter "Bai"). See page 2 of the Office Action. For the reasons discussed below, Applicants respectfully submit that amended independent claims 1 and 11 are patentably distinguishable over Dunne and Bai, either singly or in combination.

The present application is directed, in part, to “anchor vias for improved backside metal adhesion to a semiconductor substrate.” *See*, e.g., page 4, lines 2-3 of the present application. For example, in one implementation, as shown in described in Figure 1A of the present application, exemplary semiconductor structure 100 includes group 120 of through silicon vias (TSVs) as well as anchor via 132 and anchor via 133 formed in semiconductor substrate 110 and filled with a metal filler, for example. *See*, e.g., *id.* at page 7, line 19 through page 8 line 6 with Figure 1A.

As illustrated in Figure 1A, “group 120 of TSVs is formed in a core region of semiconductor substrate 110, while each of anchor vias 132 and 133 are formed in a peripheral region of semiconductor substrate 110.” *Id.*, e.g., at lines 6-8 with Figure 1A. For example, “[m]etal filler within group 120 of TSVs provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110 and may be electrically connected to an overlying metal layer [...] for grounding active devices.” *Id.*, e.g., at lines 8-12.

As further disclosed in the present application,

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices and instead provides physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150, which may be formed on bottom side 112 of semiconductor substrate 110 as shown in more detail in Figure 1B. Each of anchor vias 132 and 133 may be formed to a depth d_0 of 100 μ m into semiconductor substrate 110. However, anchor vias 132 and 133 are not so limited and d_0 may be greater or less than this value, according to the particular application. In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or if contacting a front side metal layer such as metal 1 layer, the

Attorney Docket No.: 0150176

contacted portion of metal 1 layer may be patterned such that the metal filler within anchor vias 132 and 133 essentially has a floating voltage potential during operation. Where the metal filler within anchor vias is connected to an overlying metal layer, the anchor vias may provide increased holding strength due to the additional physical connection to the overlying metal layer. *See, e.g., id.* at page 8, line 13 through page 9, line 4 (emphases added by Applicants).

By the present amendment and response, Applicants have amended independent claim 1 to recite, in part, “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.” *See* claim 1 above. Support for amended independent claim 1 can be found at least in page 8, line 13 through page 9, line 4 and Figure 1A of the present application. Applicants have also amended independent claim 11 to include features similar to those in amended independent claim 1. *See* claim 11 above.

In the Office Action, the Examiner asserts that Dunne discloses various features of independent claim 1 of the present application. *See* pages 2-3 of the Office Action.

Specifically, the Examiner asserts:

At column 7, line 45 to column 8, line 15, i.e., Dunne ‘481 teaches a structure comprising:

at least one anchor via disposed in at least one corner of a semiconductor substrate (210);

a metal filler (124) within said at least one anchor via, said metal filler having a protruding portion (216, i.e.,) extending from a backside of said semiconductor substrate;

a backside metal layer (220) on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to

said protruding portion of said metal filler of said at least one anchor via. (Please see Dunne's Fig. 2 [...]). *Id.*

Turning to Dunne, Dunne describes a specific integrated circuit (IC) die having TSVs for providing low resistance ground connection paths to a package substrate. *See* column 2, lines 12-16 of Dunne. With reference to Figure 2, Dunne provides:

Referring now to FIG. 2, a cross sectional depiction of semiconductor device 200 comprising first IC die 210 comprising of substrate (e.g., wafer or die) 211 including active top semiconductor surface 212 and a bottom surface 213, according to an embodiment of the invention, is shown. Device 200 comprises a package substrate with leadframe 205 comprising a die paddle 206, wherein the die paddle 206 has a top metal comprising surface 207. Packaging material, such as plastic encapsulant, is not shown. Bond wires 234 and 236 are shown providing a connection between an I/O or power supply node for integrated circuitry formed on active semiconductor surface 212 to lead fingers 208 and 218. First IC die 210 is shown mounted face up on the top metal comprising surface 207. A plurality of TSVs 110 comprising a first electrically conductive filler material 124 extends from the top semiconductor comprising surface 212 to protruding integral tips 216 and 217 that extend beyond the bottom surface 213 and provide an electrical contact between die paddle 206 and a ground pad (i.e. connected to ground pins of the IC 210) 243 on the top semiconductor surface 212. Although not shown, TSVs 110 generally include a barrier layer and seed layer in the case of conventional Cu TSVs. *See id.* at column 7, lines 46-67 with Figure 2 (emphasis added by Applicants).

As cited above, Dunne describes IC die 210 having TSVs 110 and metal layer 220, where TSV 110 provides a low resistance ground connection path to a package substrate. Specifically, TSVs 110 provide electrical contact between die paddle 206 and ground pad 243, which is connected to ground pins of IC 210 on top semiconductor surface 212. Thus, Applicants respectfully assert that Dunne does not disclose or suggest, for example,

Attorney Docket No.: 0150176

“wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate,” as recited by amended independent claim 1 of the present application.

In the Office Action, the Examiner concedes that “Dunne ‘481 does not specifically teach disposing the at least one anchor via in at least one corner of the semiconductor substrate.” *See* page 3 of the Office Action. In an attempt to cure the acknowledged deficiency of Dunne, the Examiner suggests combining Dunne with Bai. *Id.* Specifically, the Examiner asserts “Bai ‘629 teaches comprising a through silicon vias (TSV) at corners of a semiconductor die to reduce warpage of the semiconductor die (see Fig. 5 of Bai ‘629).” *Id.* However, even assuming, *ad arguendo*, that the Examiner’s assertions above are proper, Applicants respectfully assert that Bai also fails to disclose or suggest, for example, the above-cited features of amended independent claim 1 of the present application.

For all of the reasons set forth above, Applicants respectfully submit that amended independent claims 1 and 11 are neither anticipated by, nor are obvious in light of, the disclosures provided by Dunne and Bai, either singly or in combination. Consequently, Applicants respectfully submit that independent claims 1 and 11 are patentably distinguishable over Dunne and Bai. As such, claims 4, 6 and 8-10 depending from and further limiting patentable independent claim 1, and claims 14, 16 and 18-20 depending from and further limiting patentable independent claim 11 are, *a fortiori*, also patentably

Attorney Docket No.: 0150176

distinguishable over Dunne and Bai, for at least the reasons discussed above, and also for the additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that independent claims 1 and 11, and claims depending therefrom, are patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all of the reasons presented above, Applicants respectfully request reconsideration and allowance of claims 1, 4, 6, 8-11, 14, 16 and 18-20, and an early Notice of Allowance directed to all claims 1-20 pending in the present application.

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The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 6/26/2015

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Michael Farjami, Esq.
Reg. No. 38,135

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number 571-273-8300 on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

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FACSIMILE TRANSMISSION COVER SHEET

Date: June 26, 2015
To: United States Patent and Trademark Office
Examiner: Clark, Jasmine Jhihan B.; Art Unit: 2816
Fax: (571) 273-8300
Re: Application Serial No.: 14/165,377
Filing Date: 01/27/2014; First-Named Inventor: Jebory
Attorney Docket No.: 0150176
From: Farjami & Farjami LLP

Number of pages including the cover sheet: 15

Message:

Enclosed, please find the Amendment and Response to Non-Final Office Action dated February 26, 2015.

Payment for First Month Extension in the Amount of **\$200.00** is hereby enclosed on Form PTO-2038.

Further authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 14/165,377		Filing Date 01/27/2014		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))		N/A		N/A		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	06/26/2015		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))		* 20	Minus	** 20	= 0	x \$80 =		0
	Independent (37 CFR 1.16(h))		* 2	Minus	***3	= 0	x \$420 =		0
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))		*	Minus	**	=	X \$ =		
	Independent (37 CFR 1.16(h))		*	Minus	***	=	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

25700 7590 09/14/2015
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER

CLARK, JASMINE JHIHAN B

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 09/14/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/165,377	01/27/2014	Hadi Jebory	0150176	4221

TITLE OF INVENTION: Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/14/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 09/14/2015
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/165,377	01/27/2014	Hadi Jebory	0150176	4221

TITLE OF INVENTION: Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/14/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLARK, JASMINE JHIHAN B	2816	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/165,377	01/27/2014	Hadi Jebory	0150176	4221
25700 7590 09/14/2015 FARJAMI & FARJAMI LLP 26522 LA ALAMEDA AVENUE, SUITE 360 MISSION VIEJO, CA 92691			EXAMINER CLARK, JASMINE JHIHAN B	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 09/14/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/165,377	Applicant(s) JEBORY ET AL.	
	Examiner JASMINE CLARK	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed 06/26/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other ____
--	---

/JASMINE CLARK/ Primary Examiner, Art Unit 2816	
--	--

EAST Search History

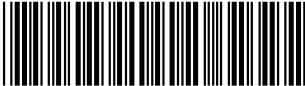
EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"20140252651"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 22:28
L2	97	h01l23/5226;h01l23/3178;h01l23/5286;h01l23/481;h01l23/562.cpc. and ((via with corner) same (semiconductor adj (substrate or device)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:11
L3	17315	h01l23/5226;h01l23/3178;h01l23/5286;h01l23/481;h01l23/562.cpc. and (semiconductor adj (chip or die or device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:18
L4	151	h01l23/5226;h01l23/3178;h01l23/5286;h01l23/481;h01l23/562.cpc. and ((semiconductor adj (chip or die or device)) with via with (back adj side))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:20
L5	0	h01l23/5226;h01l23/3178;h01l23/5286;h01l23/481;h01l23/562.cpc. and ((semiconductor adj (die or chip or device)) with via with coner)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:28
L6	0	257/774,621,e21.597;438/629,630,637-640,668,675)/.ccls. and ((semiconductor adj (die or chip or device)) with via with coner)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:31
L7	54	257/774,621,e21.597;438/629,630,637-640,668,675)/.ccls. and ((semiconductor adj (die or chip or device)) with via with corner)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:31
L8	8	257/774,621,e21.597;438/629,630,637-640,668,675)/.ccls. and ((through adj via) with corner)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2015/09/07 23:33

EAST Search History

			IBM_TDB			
L9	14	257/774,621,e21.597;438/629,630,637-640,668,675)/.ocls. and ((through adj via) with (top adj view))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2015/09/07 23:34

9/8/2015 12:00:07 AM**C:\Users\jclark1\Documents\EAST\Workspaces\ ~ AutoSave.05-02-2014.wsp**

Search Notes 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.
	Examiner JASMINE CLARK	Art Unit 2816

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner
h01l21/76898.cpc.;	02/15/2015	JC
h01l23/5226.cpc.; h01l23/3178.cpc.; h01l23/5286.cpc.; h01l23/481.cpc.; h01l23/562.cpc.	09/08/2015	JC

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	774, 621, e21.597	02/15/2015	JC
438	629, 630, 637-640, 668, 672, 675	02/15/2015	JC
257	621, 774, e21.597	09/08/2015	JC
438	629, 630, 637-640, 668, 672, 675	09/08/2015	JC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPI; DERWENT; IBM-TDB)	02/15/2015	JC
See Attached	09/08/2015	JC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
Above	To Date	09/08/2015	JC

	/JASMINE CLARK/ Primary Examiner.Art Unit 2816
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<i>Index of Claims</i> 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.
	Examiner JASMINE CLARK	Art Unit 2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE													
Final	Original	02/22/2015	09/07/2015												
	1	✓	=												
	2	O	=												
	3	O	=												
	4	✓	=												
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	6	✓	=												
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	11	✓	=												
	12	O	=												
	13	O	=												
	14	✓	=												
	15	✓	=												
	16	✓	=												
	17	O	=												
	18	✓	=												
	19	✓	=												
	20	✓	=												

Issue Classification 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.	
	Examiner JASMINE CLARK	Art Unit 2816	

CPC					
Symbol				Type	Version
H01L	23	/	481	F	2013-01-01
H01L	2924	/	0002	A	2013-01-01
H01L	23	/	562	A	2013-01-01

CPC Combination Sets								
Symbol				Type	Set	Ranking	Version	
H01L		2924		0002	A	1	1	2013-01-01
H01L		2924		00	A	1	2	2013-01-01

NONE		Total Claims Allowed:	
		20	
(Assistant Examiner)	(Date)		
/JASMINE CLARK/ Primary Examiner. Art Unit 2816	09/08/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.
	Examiner JASMINE CLARK	Art Unit 2816

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED									
257		774				H	O	1	L	23 / 48 (2006.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			
257	E21.597																			
438	629	668																		

NONE		Total Claims Allowed:	
		20	
(Assistant Examiner) /JASMINE CLARK/ Primary Examiner. Art Unit 2816	(Date) 09/08/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 14165377	Applicant(s)/Patent Under Reexamination JEBORY ET AL.
	Examiner JASMINE CLARK	Art Unit 2816

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
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	7														
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	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE		Total Claims Allowed:	
		20	
(Assistant Examiner) /JASMINE CLARK/ Primary Examiner. Art Unit 2816	(Date) 09/08/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

25700 7590 09/14/2015
 FARJAMI & FARJAMI LLP
 26522 LA ALAMEDA AVENUE, SUITE 360
 MISSION VIEJO, CA 92691



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
 I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Kate Paulson (Depositor's name)
Kate Paulson (Signature)
 12/11/15 (Date)

12/14/2015 CCHAU2 00000019 14165377

01 FC:1501

968.00 OP

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14165.377	01/27/2014	Hadi Jebray	0150176	4221

TITLE OF INVENTION: Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEES DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/14/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
CLARK, JASMINE JIHAN B	2816	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47, Rev. 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

FARJAMI & FARJAMI LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE (CITY AND STATE OR COUNTRY)

Newport Fab, LLC dba Jazz Semiconductor

Newport Beach, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 80-0731 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.29
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature

Michael Farjami

Date

December 11, 2015

Typed or printed name

Registration No.

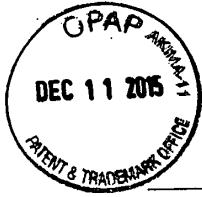
38135

Page 2 of 3

PTOL-85 Part B (10-13) Approved for use through 10/31/2013.

OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



Attorney Docket No.: 0150176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Jebory et al.**

Application Serial No.: **14/165,377**

Filed: **1/27/2014**

Title: **Anchor Vias for Improved Backside
Metal Adhesion to Semiconductor
Substrate**

Group Art Unit: 2816

Examiner: Clark, Jasmine Jhihan B.

Notice of Allowance: September 14, 2015

ISSUE FEE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Enclosed, please find the completed "Issue Fee Transmittal" form and a "Payment by Credit Card" form (PTO-2038) in the amount of \$960.00 to cover the issue fee. The drawings filed in the present application have been accepted as formal drawings by the Examiner.

Attorney Docket No.: 0150176

COMMENTS ON STATEMENTS OF REASONS FOR ALLOWANCE

The Applicant recognizes that in accordance with M.P.E.P. § 1302.14, the reasons for allowance provided by the Examiner do not necessarily include all of the reasons why the claims are allowed. The Applicant does not concede that the stated reasons for allowance are the only grounds for patentability of the allowed claims or that any element excluded from the Examiner's Reasons for Allowance is taught or suggested by the art of record.

Further, the Applicant does not concede that all of the elements identified by the Examiner are required to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the Examiner does not assert, and the Applicant would not agree, that the stated reasons for allowance have any bearing on the patentability of claims in any other applications.

Each dependent claim stands on its own and is allowable based on its own elements or in combination with one or more elements recited in its base claim(s). The combination of elements need not include all of the elements identified in the stated reasons for allowance.

The Commissioner is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0731.

Attorney Docket No.: 0150176

An early issuance of the present application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: Dec. 11, 2015

By: 
Michael Farjami
Reg. No. 38,135
Attorneys for Applicants

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Tel: (949) 282-1000
Fax: (949) 282-1002

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Mail Stop Issue Fee, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, or being facsimile transmitted to the USPTO at (571) 273-2885, on the date indicated below.

Date: 12/11/15

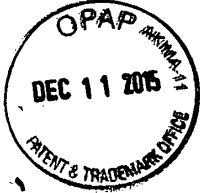
Kate Mulson
Name of Person Mailing or Transmitting Paper and/or Fee


Signature



FARJAMI & FARJAMI LLP
AN INTELLECTUAL PROPERTY LAW FIRM

www.farjami.com



26522 La Alameda Avenue, Suite 360
Mission Viejo, California 92691
tel: (949) 282-1000
fax: (949) 282-1002

FACSIMILE TRANSMISSION COVER SHEET

Date: December /1 , 2015

To: United States Patent and Trademark Office
Examiner: Clark, Jasmine Jhian B.; Art Unit: 2816

Fax: (571) 273-2885

Re: **Application Serial No.: 14/165,377**
Filing Date: 1/27/2014 ; First-Named Inventor: Jebory
Attorney Docket No.: 0150176

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 6

Message:

Enclosed please find the Issue Fee.

Payment in the Amount of \$960.00 is hereby enclosed on Form PTO-2038.

Authorization is hereby given to the Commissioner to charge any fees associated with this communication or credit any overpayment to Deposit Account No. **50-0731**.

Thank you.

The documents accompanying this facsimile contain PRIVILEGED AND CONFIDENTIAL information intended only for use of the individual or entity named above. If you are not the intended recipient, disclosure, copying, distribution or use of the contents of this facsimile information is prohibited. If you have received this facsimile in error, please immediately notify us by telephone and return the original facsimile to us at the above address via U.S. Postal Service. We will reimburse you for all expenses incurred.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P. O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/165,377	01/26/2016	9245826	0150176	4221

25700 7590 01/06/2016
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Newport Fab, LLC dba Jazz Semiconductor, Newport Beach, CA;
Hadi Jebory, Irvine, CA;
David J. Howard, Irvine, CA;
Scott B. Stetson, Huntington Beach, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: 22888

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
9,245,826	14/165,377

Completed by (check one):

☐ Applicant/Inventor	/E. Eric Hoffman/ _____ Signature
☒ Attorney or Agent of record <u>38,186</u> (Reg. No.)	E. Eric Hoffman _____ Typed or printed name
☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)	(925) 895-3545 _____ Requester's telephone number
☐ Assignee recorded at Reel _____ Frame _____	October 19, 2016 _____ Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below".

☒ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. **SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA,
Document Description: Power of Attorney

PTO/AIA/828 (07-13)
Approved for use through 11/28/2014, CSED 0051-0001
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

22698

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Newport Fab, LLC dba Jazz Semiconductor

☐ Inventor or Joint Inventor (file not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (file not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Ronit Vardi

Title

Chief Financial Officer

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of ONE forms are submitted.

This collection of information is required by 37 CFR 1.331, 1.32, and 1.47. The information is required to obtain or retain a benefit by the public which is to be used by the USPTO to process an application. Confidentiality is guaranteed by 35 U.S.C. 182 and 37 CFR 1.47 and 1.54. This collection is a statement to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEEB OR COMPLETION FORMS TO THIS ADDRESS. SEND TO: Correspondence for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing this form, call 1-800-PTO-8199 and select option 2.

CHANGE OF CORRESPONDENCE ADDRESS <i>Patent</i> Address to: Mail Stop Post Issue Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Patent Number	9,245,826
	Issue Date	01/26/2016
	Application Number	14/165,377
	Filing Date	01/27/2014
	First Named Inventor	Hadi Jebory
	Attorney Docket Number	TSJ-0150176

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: 22888

OR

☐ Firm or Individual Name

Address

City	State	ZIP
Country		
Telephone	Email	

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 38,186.

Signature /E. Eric Hoffman/

Typed or Printed Name E. Eric Hoffman

Date October 19, 2016

Telephone (925) 895-3545

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Post Issue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	27265873
Application Number:	14165377
International Application Number:	
Confirmation Number:	4221
Title of Invention:	Anchor Vias for Improved Backside Metal Adhesion to Semiconductor Substrate
First Named Inventor/Applicant Name:	Hadi Jebory
Customer Number:	25700
Filer:	Patrick T. Bever/Carrie Reddick
Filer Authorized By:	Patrick T. Bever
Attorney Docket Number:	0150176
Receipt Date:	19-OCT-2016
Filing Date:	27-JAN-2014
Time Stamp:	17:47:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TSJ-0150176-PTO-CHG-Adrs- POA-MF-CHG-Adrs-FILED.pdf	633805 e3231ca01f719f91ac98483a957cd96933950938	yes	3

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Maintenance Fee Address Change		1	1
Power of Attorney		2	2
Change of Address		3	3

Warnings:

Information:

Total Files Size (in bytes):	633805
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/165,377	01/27/2014	Hadi Jebory	

22888
BEVER HOFFMAN & HARMS, LLP
39500 Stevenson Place
Suite 209
Fremont, CA 94539

CONFIRMATION NO. 4221
POA ACCEPTANCE LETTER



Date Mailed: 10/26/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/19/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/165,377	01/27/2014	Hadi Jebory	

25700
FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

CONFIRMATION NO. 4221
POWER OF ATTORNEY NOTICE



Date Mailed: 10/26/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/19/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/rmtturner myles/

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas, Marshall Division on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:24-cv-00140	DATE FILED 2/28/2024	U.S. DISTRICT COURT for the Eastern District of Texas, Marshall Division
PLAINTIFF Harbor Island Dynamic, LLC		DEFENDANT Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,245,826	1/26/2016	Harbor Island Dynamic, LLC
2 7,772,673	8/10/2010	Harbor Island Dynamic, LLC
3 9,147,609	9/29/2015	Harbor Island Dynamic, LLC
4 7,745,886	6/29/2010	Harbor Island Dynamic, LLC
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy