US 20110248404A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2011/0248404 A1

(43) Pub. Date: Oct. 13, 2011

Chiu et al.

(54) **DUMMY PATTERN IN WAFER BACKSIDE ROUTING**

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(21) Appl. No.: **12/756,727**

(22) Filed: **Apr. 8, 2010**

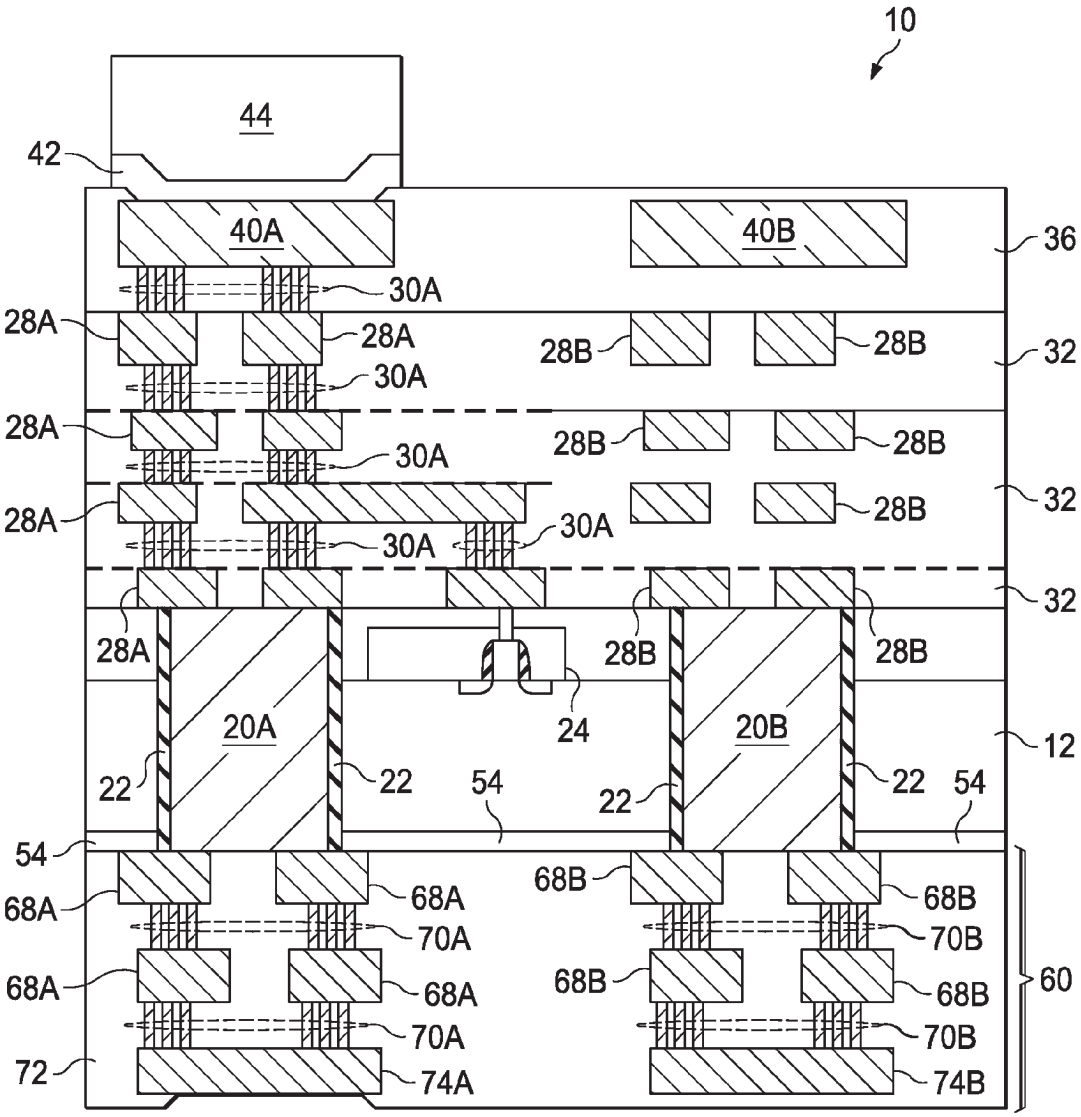
Publication Classification

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.** **257/773**; 257/E23.011

(57) **ABSTRACT**

A device includes a semiconductor substrate including a front side and a backside. A through-substrate via (TSV) penetrates the semiconductor substrate. A dummy metal line is formed on the backside of the semiconductor substrate, and may be connected to the dummy TSV.



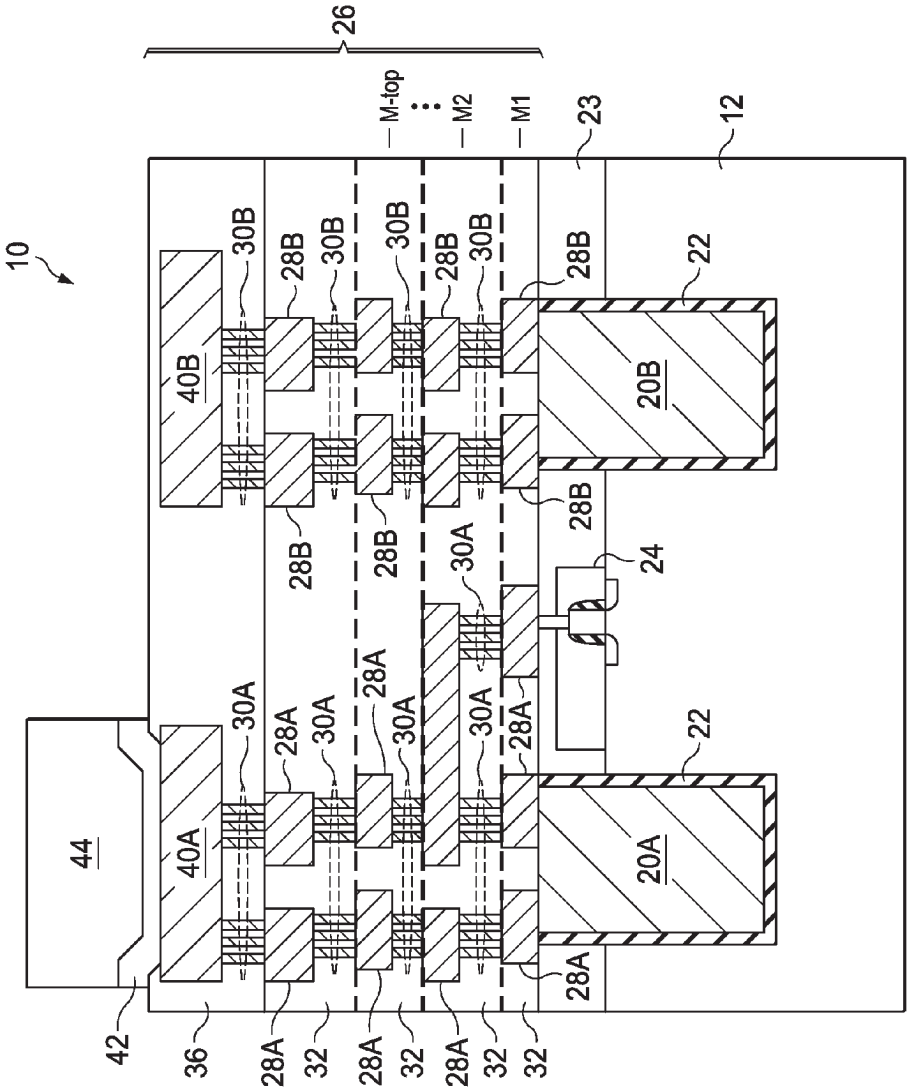

26
M-top
M2
M1
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FIG. 1

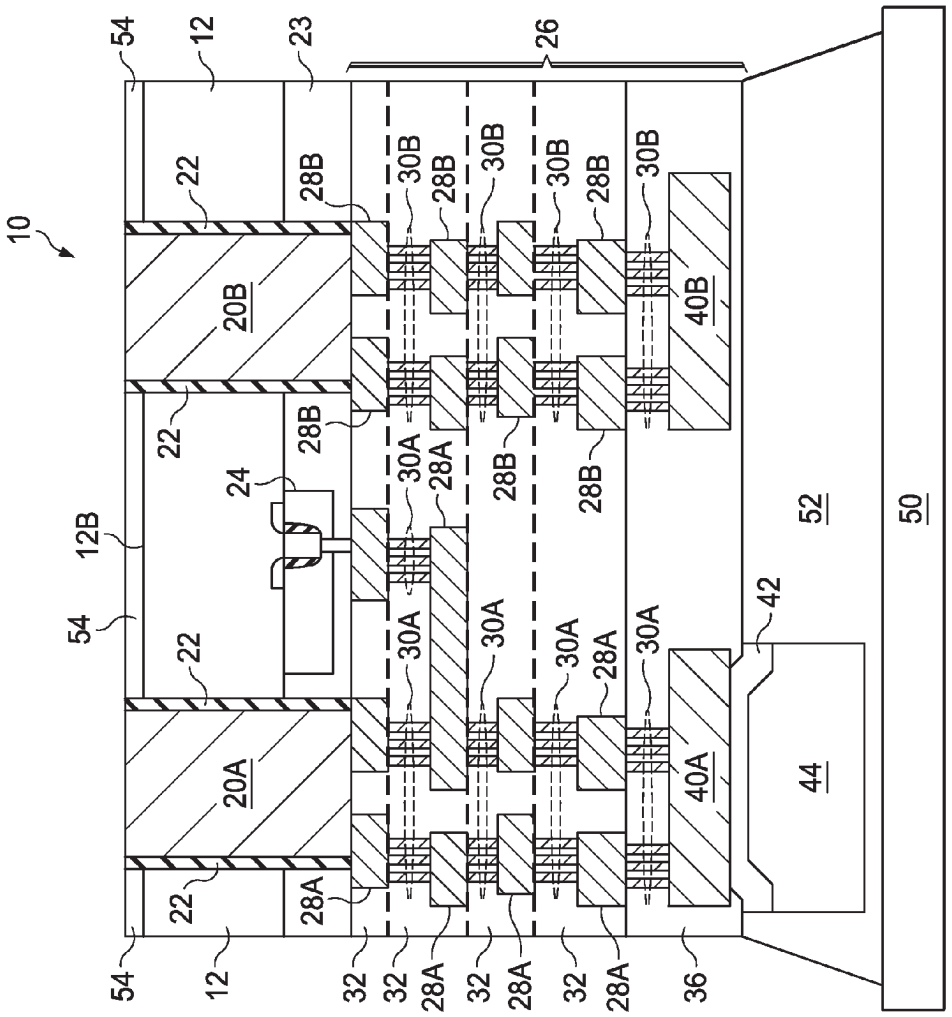

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FIG. 2

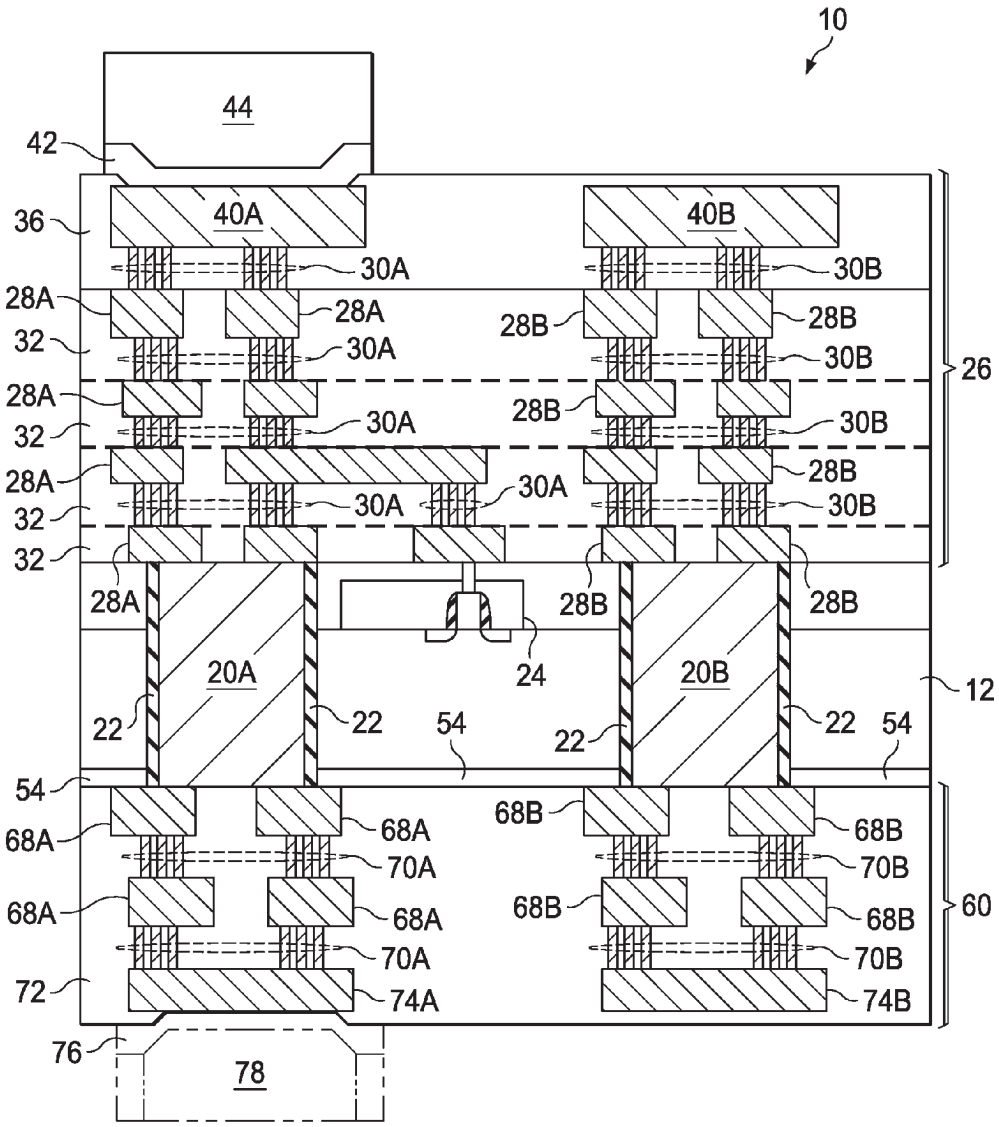

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FIG. 3

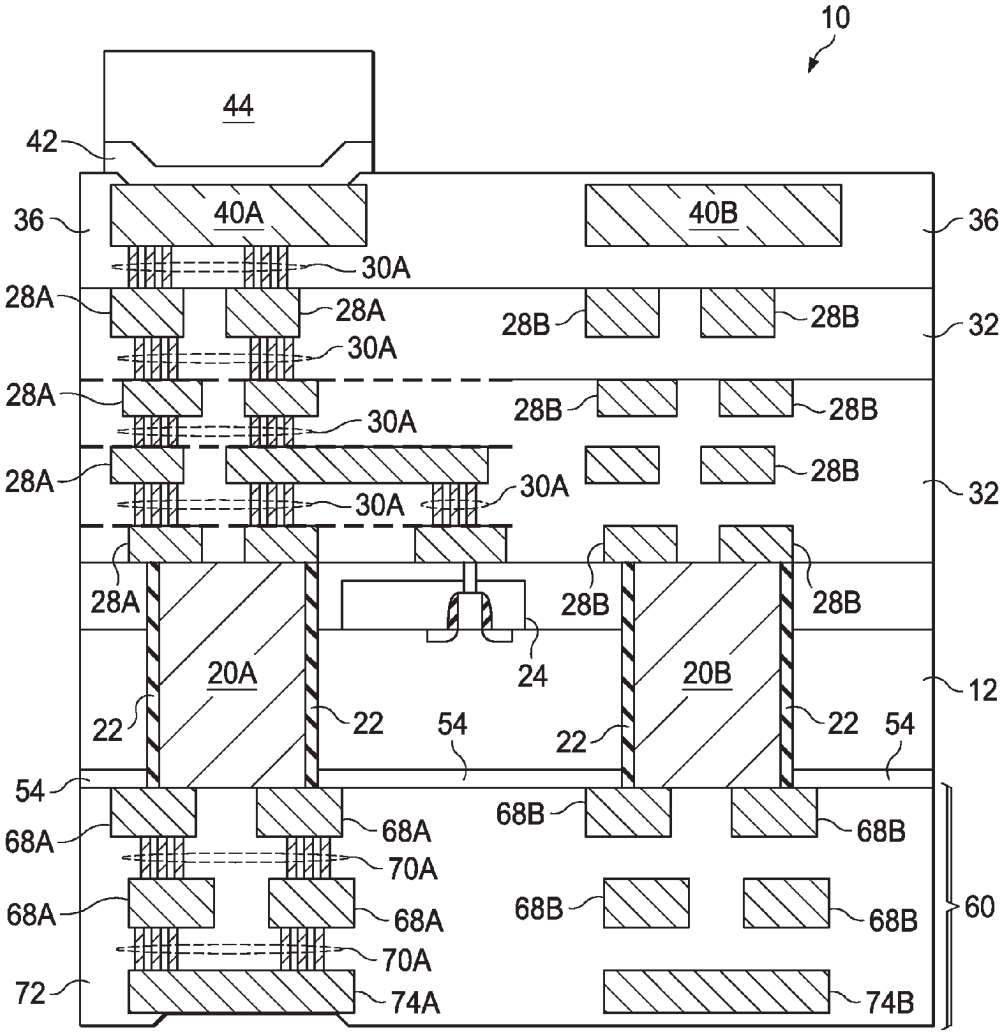

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FIG. 4

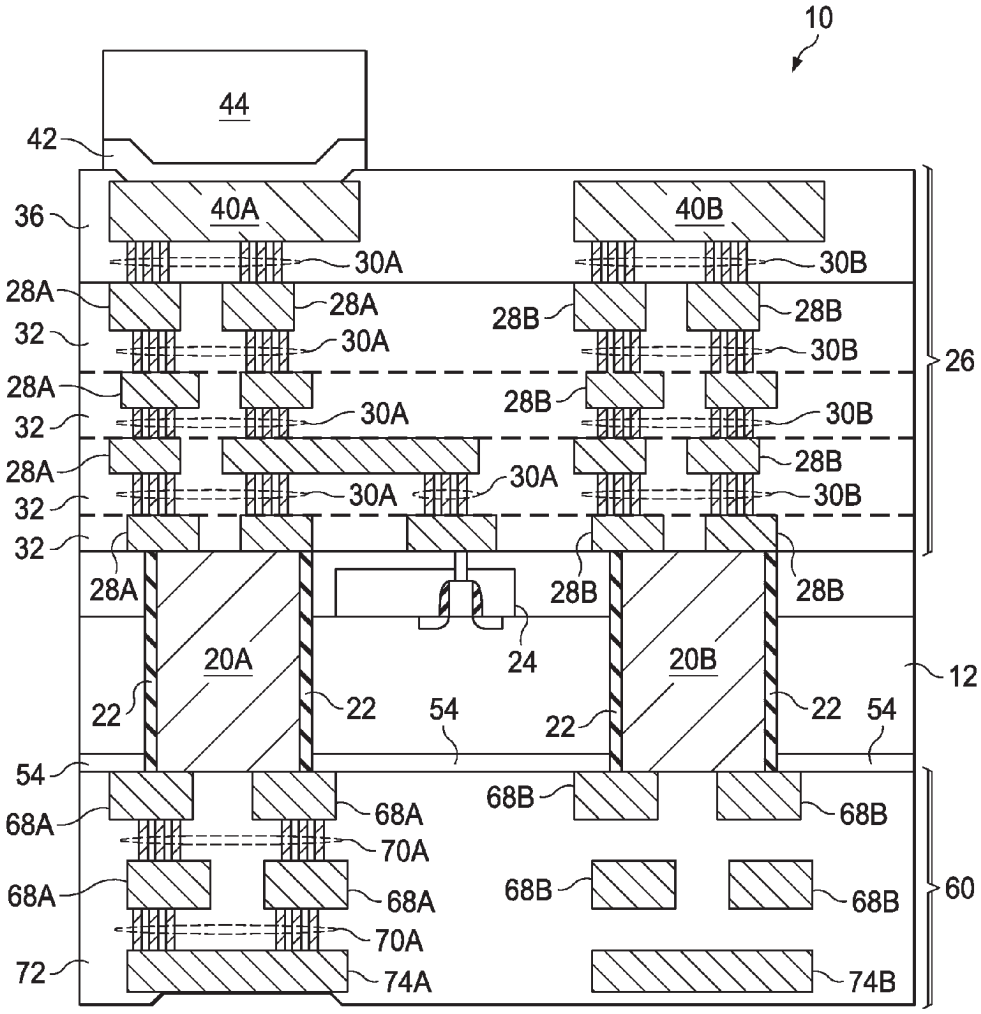

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FIG. 5

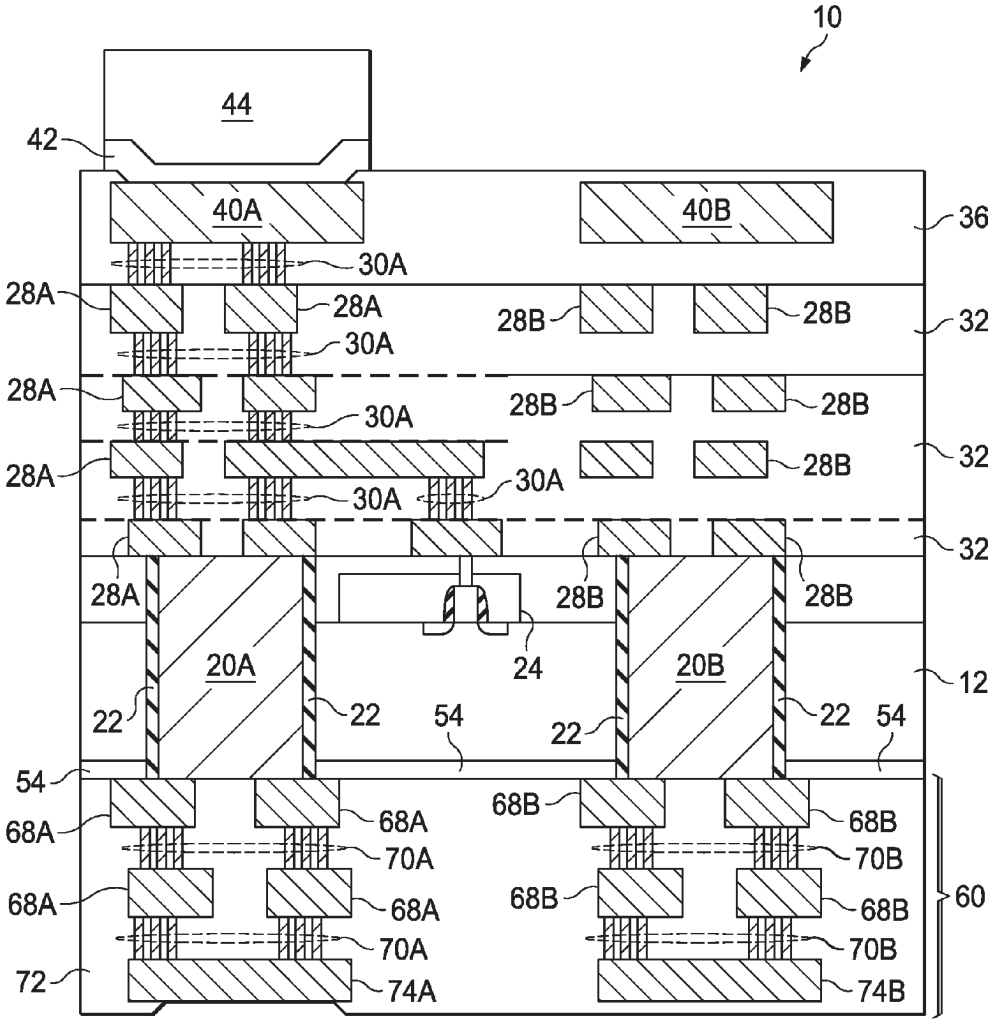

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FIG. 6

DUMMY PATTERN IN WAFER BACKSIDE ROUTING

TECHNICAL FIELD

[0001] This disclosure relates generally to semiconductor devices, and more particularly to three-dimensional integrated circuits (3DICs), and even more particularly to dummy patterns formed on the backside of wafers.

BACKGROUND

[0002] The semiconductor industry has experienced continuous rapid growth due to constant improvements in the integration density of various electronic components (i.e., transistors, diodes, resistors, capacitors, etc.). For the most part, these improvements in integration density have come from repeated reductions in minimum feature size, allowing more components to be integrated into a given chip area.

[0003] These integration improvements are essentially two-dimensional (2D) in nature, in that the volume occupied by the integrated components is essentially on the surface of the semiconductor wafer. Although dramatic improvements in lithography have resulted in considerable improvements in 2D integrated circuit formations, there are physical limitations to the density that can be achieved in two dimensions. One of these limitations is the minimum size needed to make these components. Also, when more devices are put into one chip, more complex designs are required.

[0004] An additional limitation comes from the significant increase in the number and lengths of interconnections between devices as the number of devices increases. When the number and the lengths of interconnections increase, both circuit RC delay and power consumption increase.

[0005] Among the efforts for resolving the above-discussed limitations, three-dimensional integrated circuits (3DICs) and stacked dies are commonly used. Through-silicon vias (TSVs) are thus used in 3DICs and stacked dies. In this case, TSVs are often used to connect the integrated circuits on a die to the backside of the die. In addition, TSVs are also used to provide short grounding paths for grounding the integrated circuits through the backside of the die, which may be covered by a grounded metallic film.

SUMMARY

[0006] In accordance with one aspect, a device includes a semiconductor substrate including a front side and a backside. A through-substrate via (TSV) penetrates the semiconductor substrate. A dummy metal line is formed on the backside of the semiconductor substrate, and may be connected to the TSV.

[0007] Other embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] FIGS. **1** through **3** are, in accordance with various embodiments, cross-sectional views of intermediate stages in the manufacturing of a wafer comprising dummy through-substrate vias (TSVs) and dummy metal features on a backside of the wafer; and

[0010] FIGS. **4** through **6** are cross-sectional views of wafers in accordance with alternative embodiments, wherein the wafers comprise dummy TSVs and dummy metal features in backside interconnect structures.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0011] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.

[0012] A novel integrated circuit device comprising through-substrate vias (TSVs) and the method of forming the same are provided in accordance with an embodiment. The variations of the embodiment are then discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0013] FIGS. **1** through **3** illustrate cross-sectional views of intermediate stages in the manufacturing of a wafer comprising dummy metal features on a backside of the wafer and dummy TSVs in the wafer. FIG. **1** illustrates a portion of semiconductor chip **10**, which may also be a portion of an un-sawed wafer (also referred to as wafer **10**). Wafer **10** includes substrate **12**, on which active circuits **24** are formed. Substrate **12** may be a semiconductor substrate formed of commonly used semiconductor materials, such as silicon, silicon germanium, silicon carbide, gallium arsenide, or the like. Active circuits **24** may include complementary metal-oxide-semiconductor (CMOS) transistors, diodes, resistors, capacitors (not shown), and/or the like. Interconnect structure **26** is formed over active circuits **24**. Interconnect structure **26** includes a plurality of metallization layers comprising metal lines **28** (including active metal lines **28**A and dummy metal lines **28**B) and vias **30** (including active vias **30**A and dummy vias **30**B) in a plurality of dielectric layers **32**, which include commonly known inter-metal dielectrics (IMDs). Metal lines **28** are also commonly known as trench interconnects. Dielectric layers **32** in interconnect structure **26** may include low-k dielectric layers, which may have k values lower than about 3.0, or even lower than about 2.5.

[0014] Dummy metal lines **28**B and dummy vias **30**B may be formed in the metallization layers including the bottom metallization layer (commonly known as M1), the top metallization layer (commonly known as M-top), and all metallization layers therebetween. Dummy metal lines **28**B and dummy vias **30**B in different metallization layers may vertically overlap each other, and connect with each other to form a tower, or may be isolated from each other. Metal lines **28** and vias **30** may be formed using damascene processes. Alternatively, they may be formed by depositing blanket metal layers, and then etching the blanket metal layers to form desirable patterns. Active metal lines **28**A and active vias **30**A have electrical functions for electrically coupling integrated circuit devices. For example, active metal lines **28**A and active vias **30**A may interconnect different devices in active circuits **24**, and may connect active circuits **24** to overlying metal pads and solder bumps.

[0015] Metal pads **40** (including active metal pad **40**A and dummy metal pad **40**B) are formed over interconnect structure **26**, and may be formed in passivation layer(s) **36**, which may be formed of silicon oxide, silicon nitride, un-doped silicate glass (USG), polyimide, or the like. Metal pads **40** may comprise aluminum, and hence are also referred to as aluminum pads **40** throughout the description, although they may also be formed of, or include, other metallic materials, such as copper, silver, gold, nickel, tungsten, alloys thereof, and/or multi-layers thereof. Active metal pad **40**A may be electrically coupled to active circuits **24** through active metal

lines **28**A and active vias **30**A in interconnect structure **26**. In an embodiment, metal pads **40** are formed of aluminum copper (AlCu). Over metal pads **40**, under-bump-metallurgies (UBMs) **42** and metal bump **44** may be formed. In an embodiment, metal bump **44** is a solder bump. In alternative embodiments, metal bump **44** is a copper bump, and may be coated with nickel, gold, or other metals or metal alloys.

[0016] Dummy metal pad **40**B may be formed at a same level, and formed simultaneously with, active metal pad **40**A. Dummy metal pad **40**B, dummy metal lines **28**B, and dummy vias **30**B may not have any electrical function. In other words, they may be electrically decoupled from all active circuits in wafer **10**, and may be electrically decoupled from metal bumps/metal pads on the surface of wafer **10**. In an embodiment, dummy metal pad **40**B, dummy metal lines **28**B, and dummy vias **30**B are electrically floating. With the formation of dummy metal pad **40**B, dummy metal lines **28**B, and dummy vias **30**B, the pattern densities in wafer **10** become more uniform, and hence the pattern-loading effect in the formation of metal lines **28**, vias **30**, and metal pads **40** is reduced.

[0017] Through-substrate vias (TSVs) **20** (including active TSV **20**A and dummy TSV **20**B) are formed in wafer **10** and extend into substrate **12**. In a first embodiment, as shown in FIG. **1**, TSVs **20** are formed using a via-first approach, and is formed before the formation of a bottom metallization layer (commonly known as M1). Accordingly, TSVs **20** only extend into inter-layer dielectric (ILD) **23** that is used to cover the active devices, but not into the IMD layers in interconnect structure **26**. In alternative embodiments, TSVs **20** are formed using a via-last approach, and are formed after the formation of interconnect structure **26**. Accordingly, TSVs **20** penetrate through both substrate **12** and interconnect structure **26**, and extend into substrate **12**. Isolation layers **22** are formed on the sidewalls of TSVs **20** and electrically insulate TSVs **20** from substrate **12**. Isolation layers **22** may be formed of commonly used dielectric materials, such as silicon nitride, silicon oxide (for example, tetra-ethyl-ortho-silicate (TEOS) oxide), or the like.

[0018] Active TSV **20**A may be electrically coupled to active circuits **24**, active metal lines **28**A and active vias **28**B. Dummy TSV **20**B may be electrically coupled to, or may be decoupled from, dummy metal lines **28**B and dummy vias **28**B. Further, dummy TSV **20**B may physically contact the dummy features in interconnect structure **26** to form an integrated metal structure. Similarly, with the formation of dummy TSV **20**B, the pattern density of TSV openings (filled with TSVs **20**) may be more uniform than if no dummy TSV **20**B is formed, and the pattern-loading effect, for example, in the etching of substrate **12** for the formation of TSVs **20**, is reduced.

[0019] Referring to FIG. **2**, carrier **50** is bonded to the front side of wafer **10** through adhesive **52**. A backside grinding is performed to remove excess portions of substrate **12** so that TSVs **20** are exposed. Backside isolation layer **54** is formed to cover back surface **12**B of substrate **12**. In an exemplary embodiment, the formation of backside isolation layer **54** includes slightly etching back surface **12**B of substrate **12**, blanket forming backside isolation layer **54**, and performing a light chemical mechanical polish (CMP) to remove the portion of backside isolation layer **54** directly over TSVs **20**. Accordingly, TSVs **20** are exposed through backside isolation layer **54**.

[0020] Next, as shown in FIG. **3**, backside interconnect structure **60** is formed on the backside of wafer **10**, and then carrier **50** is de-bonded. Backside interconnect structure **60** may also include a plurality of metal lines **68** (including active metal lines **68**A and dummy metal lines **68**B) and vias **70** (including active vias **70**A and dummy vias **70**B) in a plurality of dielectric layers **72**. Dielectric layer **72** may be formed of dielectric materials, such as silicon oxide, silicon nitride, polyimide, and/or the like, and may be formed using CVD, spin-on, or other commonly used methods. Again, active metal lines **68**A and active vias **70**A have electrical functions for interconnecting integrated circuit devices, and may be electrically coupled to active TSV **20**A, active circuits **24**, active metal lines **28**A, and/or active vias **30**A. Dummy metal lines **68**B and dummy vias **70**B may not have electrical functions, and may be electrically floating. However, dummy metal lines **68**B and dummy vias **70**B may be electrically coupled to dummy TSV **20**A, dummy metal lines **28**A, and/or dummy vias **30**A, although all of them may be electrically floating. Throughout the description, when a first dummy feature is referred to as being "electrically coupled" to a second dummy feature, it indicates that a conductive path may be found between the first and the second dummy features, although both of them may be floating. Again, metal lines **68** and vias **70** may be formed either using damascene processes, or formed by depositing and etching blanket metal layers. In an embodiment, the backside interconnect structure includes active metal pad (or bond pad) **74**A and dummy metal pad **74**B, wherein active metal pad **74**A is used for bonding the respective chip to another device, such as a die or a package substrate. Dummy metal pad **74**B, on the other hand, is not used for bonding, and may be electrically floating. In alternative embodiments, UBM **76** and metal bump **78** may be formed on active metal pad **74**A.

[0021] In subsequent steps, wafer **10** is sawed into dies, during the use of the dies, electrical signals may be connected to active circuits **24**, active metal lines **28**A/**68**A, and active vias **30**A/**70**A. However, no electrical signal or voltage may be connected to dummy metal lines **28**A/**68**A and dummy vias **30**A/**70**A.

[0022] FIGS. **4** through **6** illustrate variations of the embodiments. Like reference notations in these embodiments represent like elements as in the previously discussed embodiments, unless specified otherwise. The embodiment shown in FIG. **4** is similar to the embodiment shown in FIG. **3**, except no dummy vias are formed in any of front-side interconnect structure **26** and backside interconnect structure **60**. However, dummy metal lines **28**B and **68**B are still formed. In FIG. **5**, dummy vias **30**B are formed in front-side interconnect structure **26**, while no dummy vias are formed in backside interconnect structure **60**. Accordingly, dummy metal lines **68**B are formed as discrete features electrically insulated from each other. FIG. **6** illustrates the embodiments with no dummy vias formed in front-side interconnect structure **26**, while dummy vias **70**B are formed in backside interconnect structure **60**. In addition, in each of the embodiments shown in FIGS. **3** through **6**, dummy TSV **20**B may, or may not, be formed, while active TSV **20**A is still formed.

[0023] With the formation of dummy metal lines and dummy vias on the backside of wafer **10**, the formation of backside interconnect structure **60** suffers less from pattern-loading effects. Further, the dummy metal lines and dummy vias on the backside of wafer **10** may be connected to the dummy metal lines and dummy vias on the front side of wafer **10** to form an integrated metal feature. As a result, the likelihood of dielectric peeling between dielectric layers **32** and **72** is reduced, and hence the strength of wafer **10** may be improved.

[0024] Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A device comprising:
- a semiconductor substrate comprising a front side and a backside;
- a through-substrate via (TSV) penetrating the semiconductor substrate; and
- a first dummy metal line on the backside of the semiconductor substrate.

2. The device of claim **1**, wherein the first dummy metal line is electrically floating.

3. The device of claim **1** further comprising a dummy TSV penetrating the semiconductor substrate.

4. The device of claim **3**, wherein the first dummy metal line is electrically coupled to the dummy TSV.

5. The device of claim **4** further comprising a second dummy metal line on the front side of the semiconductor substrate, wherein the second dummy metal line is electrically coupled to the dummy TSV and the first dummy metal line.

6. The device of claim **4** further comprising:
- a plurality of dielectric layers on the backside of the semiconductor substrate;
- a plurality of dummy metal lines, with one of the plurality of dummy metal lines in each of the plurality of dielectric layers; and
- a plurality of dummy vias electrically coupled to the plurality of dummy metal lines, with the plurality of dummy metal lines, the plurality of dummy vias, and the dummy TSV forming an integrated metal structure.

7. The device of claim **1** further comprising a bond pad on the backside of the semiconductor substrate, wherein the first dummy metal line is at a same level as the bond pad.

8. The device of claim **1** further comprising a dummy via on the backside of the semiconductor substrate and connected to the first dummy metal line.

9. A device comprising:
- a semiconductor substrate comprising a front side and a backside;
- an active circuit on the front side of the semiconductor substrate;
- a through-substrate via (TSV) penetrating the semiconductor substrate;
- a dummy TSV penetrating the semiconductor substrate; and
- a first dummy metal line on the backside of the semiconductor substrate and electrically coupled to the dummy TSV, wherein the first dummy metal line and the dummy TSV are electrically floating.

10. The device of claim **9**, wherein the first dummy metal line physically contacts the dummy TSV.

11. The device of claim **9**, wherein the semiconductor substrate is a portion of a chip, and wherein the device further comprises:
- a bond pad at a back surface of the chip; and
- a dummy metal feature at a same level as the bond pad.

12. The device of claim **9** further comprising:
- a plurality of dielectric layers on the backside of the semiconductor substrate; and
- a plurality of dummy metal features, with each of the plurality of dielectric layers comprising one of the plurality of dummy metal features therein, and wherein the plurality of dummy metal features and the dummy TSV form an integrated metal structure.

13. The device of claim **12** further comprising a plurality of dummy vias, each in one of the plurality of dielectric layers and contacting a respective one of the plurality of dummy metal features.

14. The device of claim **9** further comprising a second dummy metal line on the front side of the semiconductor substrate.

15. The device of claim **14**, wherein the second dummy metal line is electrically coupled to the dummy TSV and the first dummy metal line.

16. The device of claim **14** further comprising:
- a plurality of dielectric layers on the front side of the semiconductor substrate; and
- a plurality of dummy metal features, with each of the plurality of dielectric layers comprising one of the plurality of dummy metal features therein, wherein the plurality of dummy metal features is electrically coupled to the dummy TSV.

17. A device comprising:
- a semiconductor substrate comprising a front side and a backside;
- an active circuit on the front side of the semiconductor substrate;
- a through-substrate via (TSV) penetrating the semiconductor substrate;
- a dummy TSV penetrating the semiconductor substrate;
- a first plurality of dielectric layers on the backside of the semiconductor substrate;
- a first plurality of dummy metal features, with each of the first plurality of dielectric layers comprising one of the first plurality of dummy metal features therein;
- a second plurality of dielectric layers on the front side of the semiconductor substrate; and
- a second plurality of dummy metal features, with each of the second plurality of dielectric layers comprising one of the second plurality of dummy metal features therein, and wherein the first and the second plurality of dummy metal features and the dummy TSV form an integrated metal structure, and are electrically floating.

18. The device of claim **17** further comprising a bond pad on the backside of the semiconductor substrate, wherein one of the first plurality of dummy metal features is at a same level as the bond pad.

19. The device of claim **17**, wherein one of the first plurality of dummy metal features is a dummy via.

* * * * *