

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

Case IPR2024-01405
Patent No. 9,245,826

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,245,826 to Jebory et al. (“’826 patent”)
Ex. 1002	Prosecution History of the ’826 patent (downloaded from Patent Center)
Ex. 1003	Declaration of Scott Thompson, Ph.D. (“Thompson”)
Ex. 1004	U.S. Patent Application Publication No. 2009/0079056 to Conn, filed December 7, 2007, and published March 26, 2009 (“ <i>Conn</i> ”)
Ex. 1005	U.S. Patent Application Publication No. 2014/0138844 to Gambino et al., filed November 21, 2012, and published May 22, 2014 (“ <i>Gambino</i> ”)
Ex. 1006	U.S. Patent Application Publication No. 2011/0057319 to Dean et al., filed September 9, 2009, and published March 10, 2011 (“ <i>Dean</i> ”)
Ex. 1007	U.S. Patent Publication No. 2009/0140395 to Davis et al., filed December 4, 2007, and published June 4, 2009 (“ <i>Davis</i> ”)
Ex. 1008	U.S. Patent Application Publication No. 2012/0104546 to Ding et al., filed November 1, 2010, and published May 3, 2012 (“ <i>Ding</i> ”)
Ex. 1009	U.S. Patent Application Publication No. 2013/0082382 to Torii, filed September 28, 2012, and published April 4, 2013 (“ <i>Torii</i> ”)
Ex. 1010	U.S. Patent Application Publication No. 2012/0256310 to Ide, filed April 5, 2012, and published October 11, 2012 (“ <i>Ide</i> ”)
Ex. 1011	U.S. Patent Application Publication No. 2013/0154108 to Lin et al., filed December 14, 2011, and published June 20, 2013 (“ <i>Lin</i> ”)
Ex. 1012	U.S. Patent No. 8,338,961 to Su et al., filed April 26, 2012, and issued December 25, 2012 (“ <i>Su</i> ”)
Ex. 1013	U.S. Patent Application Publication No. 2011/0089572 to Tezcan et al., filed September 17, 2010, and published April 21, 2011 (“ <i>Tezcan</i> ”)
Ex. 1014	U.S. Patent No. 6,140,703 to Cronin et al., filed December 26, 1996, and issued October 31, 2000 (“ <i>Cronin</i> ”)
Ex. 1015	U.S. Patent Application Publication No. 2009/0026619 to Zeng et al., filed July 24, 2007, and published January 29, 2009 (“ <i>Zeng</i> ”)
Ex. 1016	U.S. Patent Application Publication No. 2011/0018109 to Blaschke et al., filed May 20, 2010, and published January 27, 2011 (“ <i>Blaschke</i> ”)
Ex. 1017	U.S. Patent Application Publication No. 2010/0252934 to Law et al., filed January 6, 2010, and published October 7, 2010 (“ <i>Law</i> ”)
Ex. 1018	U.S. Patent Application Publication No. 2013/0334699 to Kuo et al., filed June 19, 2012, and published December 19, 2013 (“ <i>Kuo</i> ”)

Exhibit	Description
Ex. 1019	U.S. Patent No. 8,183,580 to Wang, filed March 2, 2010, and issued May 22, 2012 (“ <i>Wang</i> ”)
Ex. 1020	U.S. Patent Application Publication No. 2011/0248404 to Chiu et al., filed April 8, 2010, and published October 13, 2011 (“ <i>Chiu</i> ”)
Ex. 1021	U.S. Patent No. 4,946,376 to Sharma et al., filed April 6, 1989, and issued August 7, 1990 (“ <i>Sharma</i> ”)
Ex. 1022	U.S. Patent No. 8,912,091 to Burnham et al., filed January 10, 2013, and issued December 16, 2014 (“ <i>Burnham</i> ”)
Ex. 1023	U.S. Patent No. 8,431,481 to Dunne et al., filed April 11, 2012, and issued April 30, 2013 (“ <i>Dunne</i> ”)
Ex. 1024	U.S. Patent Application Publication No. 2010/0171226 to West et al., filed December 29, 2009, and published July 8, 2010 (“ <i>West</i> ”)
Ex. 1025	Excerpt of <i>Merriam-Webster’s</i> Collegiate Dictionary (11th ed. 2011)
Ex. 1026	U.S. Patent Application Publication No. 2010/0090318 to Hsu et al., filed December 11, 2008, and published April 15, 2010 (“ <i>Hsu</i> ”)
Ex. 1027	U.S. Patent No. 8,455,983 to Wood et al., filed November 22, 2011, and issued June 4, 2013 (“ <i>Wood</i> ”)
Ex. 1028	U.S. Patent Application Publication No. US2010/0225005 to Nishio et al., filed May 18, 2010, and published September 9, 2010 (“ <i>Nishio</i> ”)
Ex. 1029	U.S. Patent No. 7,939,369 to Farooq et al., filed May 14, 2009, and issued May 10, 2011 (“ <i>Farooq</i> ”)
Ex. 1030	U.S. Patent Application Publication No. US2011/0095435 to Volant et al., filed October 28, 2009, and published April 28, 2011 (“ <i>Volant</i> ”)
Ex. 1031	Reserved
Ex. 1032	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Plaintiff’s Infringement Contentions Cover Pleading (July 18, 2024)
Ex. 1033	<i>Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al</i> , Case No. 2:24-cv-00140, Dkt. No. 38, Docket Control Order (E.D. Tex. August 2, 2024)

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc., requests IPR of U.S. Patent No. 9,245,826 (Ex. 1001), assigned to Patent Owner Harbor Island Dynamic, LLC (“HID”), and cancellation of claims 1-20.

The ’826 patent “is directed to anchor vias for improved backside metal adhesion to a semiconductor substrate.” ’826 patent, 1:42-46. For example, claim 1 recites:

[1pre] “A structure comprising:”

[1a] “at least one **anchor via** disposed in at least one **corner** of a semiconductor substrate;”

[1b] “a **metal filler** within said at least one **anchor via**, said **metal filler** having a **protruding portion** extending from a backside of said semiconductor substrate;”

[1c] “a **backside metal layer** on a bottom surface of said semiconductor substrate, **said backside metal layer being bonded to said protruding portion** of said **metal filler** of said at least one **anchor via**,”

[1d] “wherein said **metal filler** within said at least one **anchor via** **does not provide ground connection to one or more active devices** in said semiconductor substrate.”

Id., 7:58-8:3.¹

Dependent claims 2-10 recite various other structural features of the anchor via and metal layer. And claims 11-20 recite corresponding methods for manufacturing the structures in claims 1-10, respectively.

The claims recite nothing more than well-known prior-art features. Indeed, all the features of claim 1 were already present in a single reference, i.e., each of *Conn* (Ex. 1004), *Torii* (Ex. 1009), and *Ide* (Ex. 1010). *Conn*'s disclosure even uses the term “anchor via.” *Conn*, *Torii*, and *Ide* each also anticipate many other challenged claims. And the remaining claimed features would have been obvious over these references and others, none of which were considered by the Examiner. The Board should institute review and cancel all challenged claims.

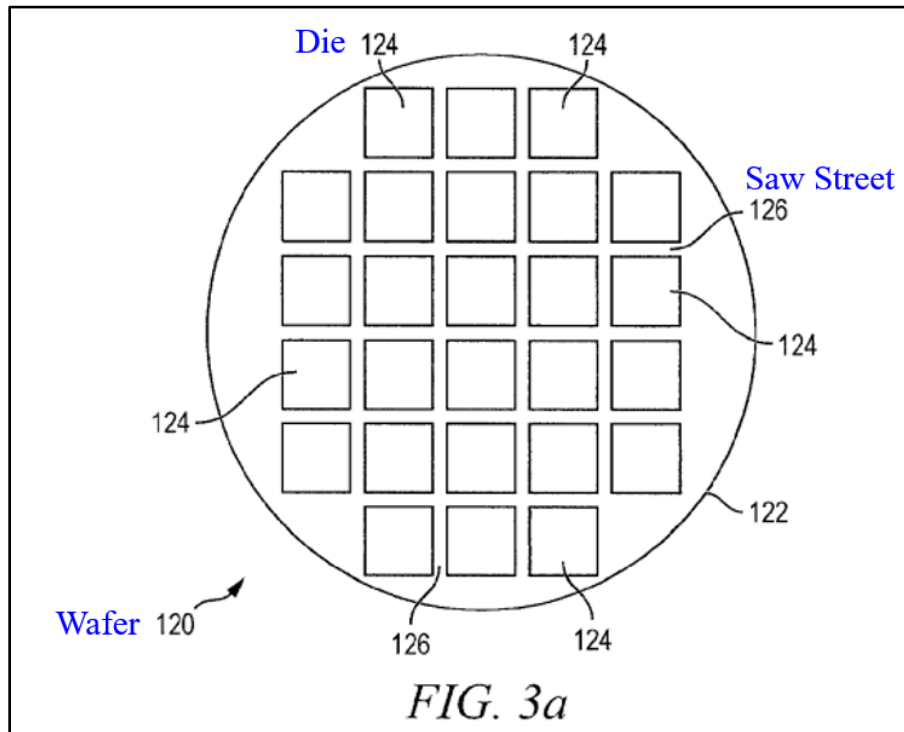
II. State of the Art

A. Semiconductor Device Manufacturing

Like houses are built on foundations, semiconductor devices are fabricated on substrates. Thompson, ¶39. As shown below, “a semiconductor wafer 120 with a base substrate material 122,” e.g., silicon, serves as the “structural support” for semiconductor devices. *Lin* (Ex. 1011), [0042]. Wafer 120 is divided into an array of dies 124 by a grid of saw streets 126. *Id.* Cutting tools, e.g., laser or saw blade,

¹ Bold and italics in the quotes are added, unless indicated as original.

can be used to singulate (i.e., cut) the wafer into individual dies along the saw streets. *Id.*, [0032], [0042]. Each die can be packaged to form a chip. Thompson, ¶39.



Lin, Fig. 3a.²

“Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits.”³ *Id.*, [0023].

² All figures in this Petition containing color are annotated relative to the original figures in the patent or prior art, and all text in color is added.

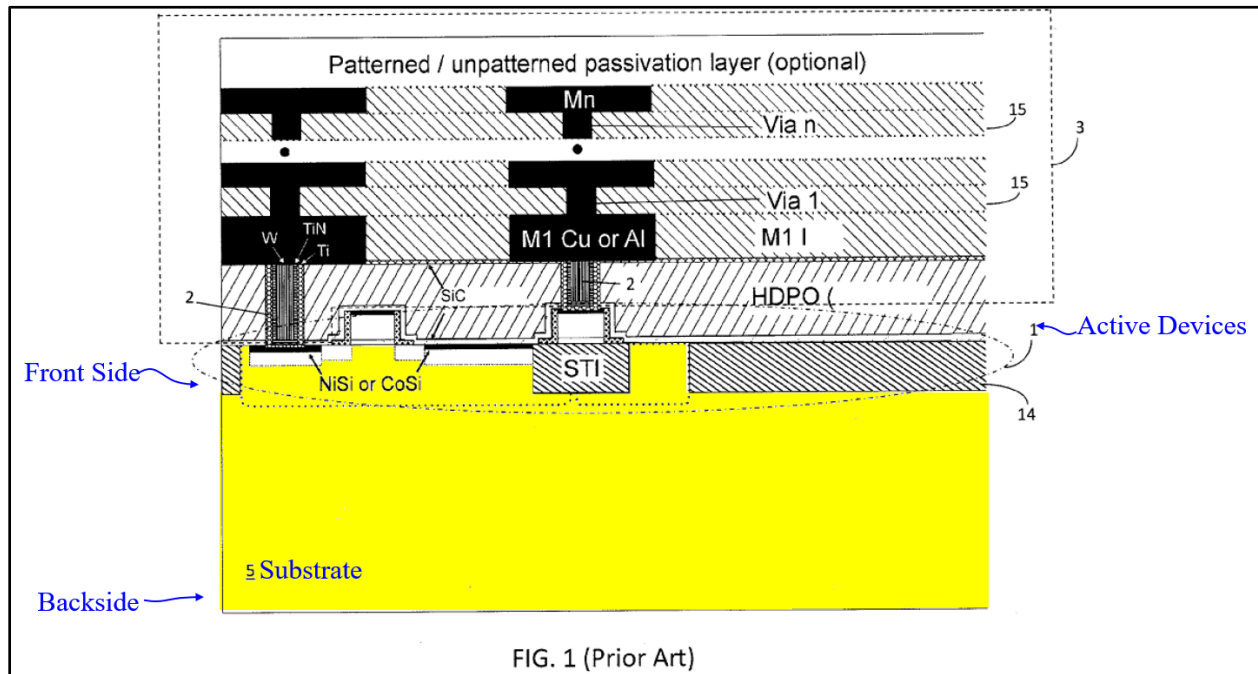
³ The active and passive electrical components are also referred to as “active devices” and “passive devices” throughout this Petition.

“Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current” and are used for converting and supplying electrical power for a circuit. *Id.*; *Lin*, [0005]; Thompson, ¶40. “Passive electrical components, such as capacitors, inductors, resistors, and transformers, create a relationship between voltage and current necessary to perform electrical circuit functions,” (*Lin*, [0023]), and consume the electrical power in the circuit (rather than supplying the power to the circuit). *Lin*, [0005]; Thompson, ¶40.

B. Front Side and Backside of Semiconductor Substrate

In the semiconductor industry, “front side” and “backside” are usually used to refer to the two opposite sides of a semiconductor substrate, respectively. *Lin*, [0008] (“both a front side and a backside of a semiconductor die”). But the specific definitions of “front side” and “backside” depend on the context. *Su* (Ex. 1012), 6:30-31 (“The terms ‘front’ and ‘back’ are somewhat arbitrary.”); Thompson, ¶¶41-42. In one example, if active devices are formed on the substrate, “[t]he front-side of a substrate ... is the side where the active devices of a chip ... are located,” and the backside “is the side opposite to the side where the active devices are located.” *Tezcan* (Ex. 1013), [0059]; *Tezcan*, [0030]; Thompson, ¶42. The following figure shows “a CMOS device with a substrate 5, comprising a front-end-of-line 1 comprising active devices, for example[,] transistors.” *Tezcan*, [0006]. In this example, the side of the substrate 5 with the active devices (i.e., the

top side in the figure) is the front side, and the opposite side (i.e., the bottom side in the figure) is the backside. Thompson, ¶42.



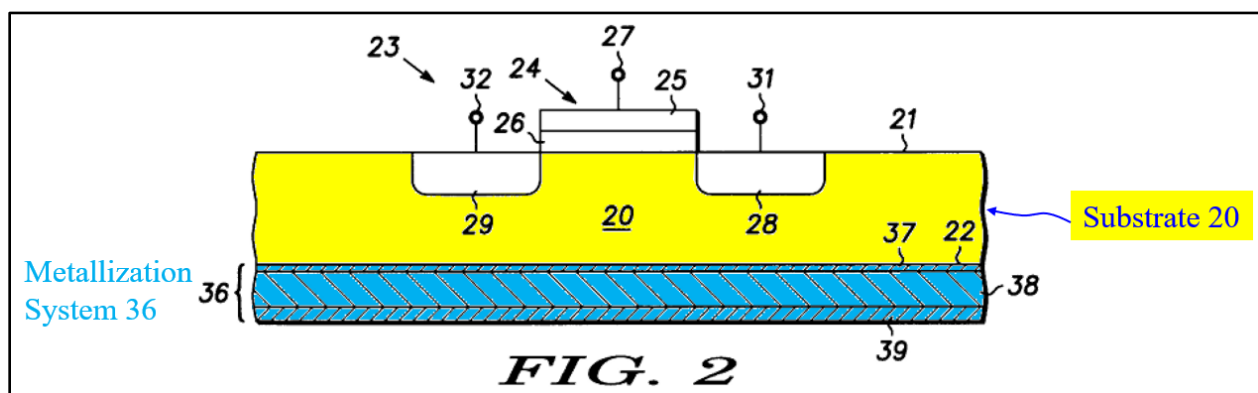
Tezcan, Fig. 1.

A semiconductor substrate's front side and backside generally have no relation to its orientation. Thompson, ¶43. For example, during fabrication, the backside may face up to facilitate backside processing. *Torii*, [0099] (wafer is held “upside down” to grind the backside surface); *Ide*, [0150] (“wafers are upside down ... to process the rear surface”). Moreover, in final products, the backside may face up in a “flip chip” configuration to facilitate packaging. *Ide*, [0163];

Gambino (Ex. 1005), [0002]; *West* (Ex. 1024), [0026] (“die (or wafer) can be assembled ... bottom side up (i.e. face down)”).

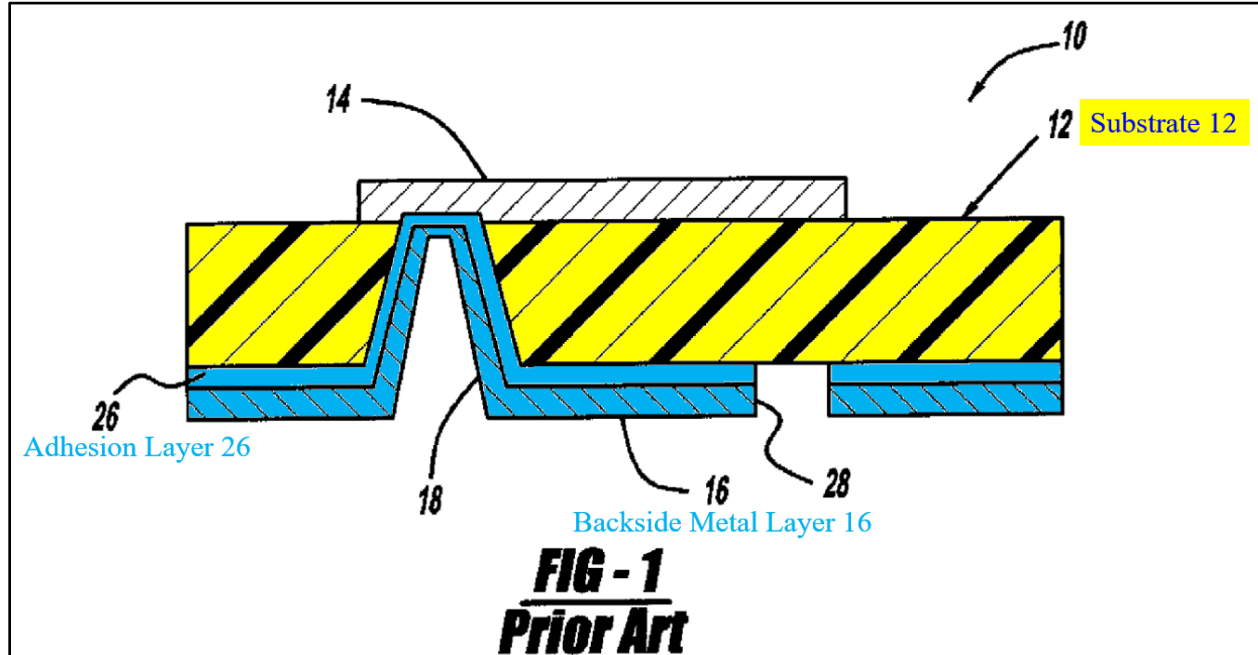
C. Backside Metal Layer

Metal layer(s) can be formed at the backside of the semiconductor substrate. Thompson, ¶44. The backside metal layer can serve various purposes. For example, “[a]n important use of” the backside metal layer is “to promote bonding of the semiconductor die to a ceramic or a metal structure such as a leadframe.” *Cronin* (Ex. 1014), 1:12-15, 1:25-26. As shown below, “a semiconductor substrate 20 ha[s] a top surface 21 and a bottom surface 22.” *Id.*, 1:64-66. A “semiconductor device 23” is “formed on top surface 21,” (*id.*, 2:3-6), and “a metallization system 36 [is] disposed” on bottom surface 22. *Id.*, 2:22-24. Metallization system 36 is a three-layer stack including “adhesion layer 37,” “barrier layer 38,” and “protective layer 39,” each of which is formed using sputter deposition techniques. *Id.*, 2:24-29, 2:42-43, 2:63-64.



Cronin, Fig. 2.

As another example, the backside metal layer(s) can serve electrical functions, such as providing “RF, DC[,] and/or ground signals.” *Zeng* (Ex. 1015), Abstract; *id.*, [0007]-[0008], [0015]. The following figure “is cross-sectional view of a circuit package 10 including a semiconductor substrate 12 on which is fabricated an integrated circuit 14[.]” *Id.*, [0005]. “A backside metal layer 16 is deposited on a backside of the semiconductor substrate 12” and “electrically coupled to the integrated circuit 14 by a metallized via 18 extending through the substrate 12.” *Id.* Moreover, “an adhesion layer 26” made of metal is also disposed on the backside “to reduce backside metal layer peeling.” *Id.*, [0006]; Thompson, ¶45.



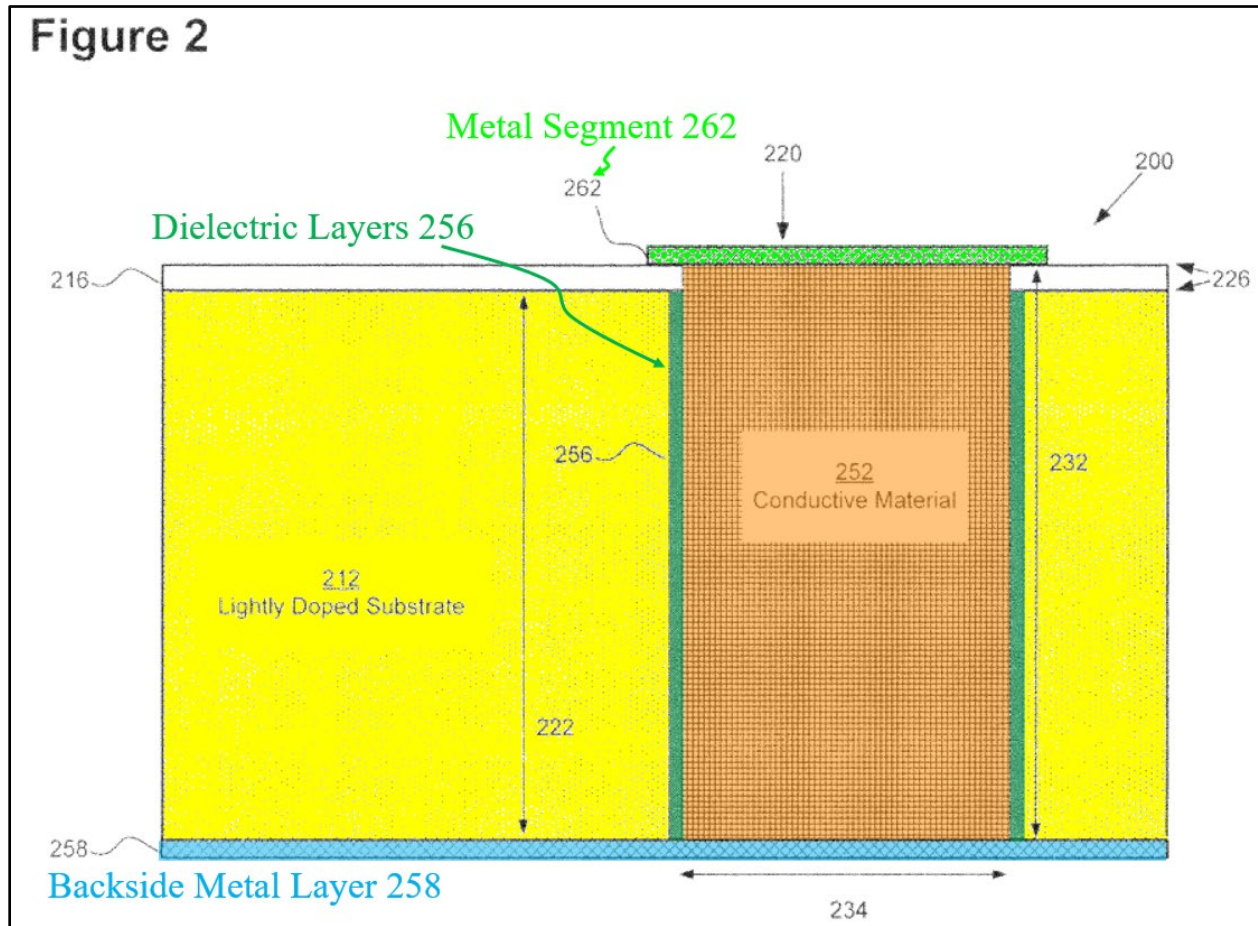
Zeng, Fig. 1.

D. Via Structures

In the above figure, a via structure 18 is used to electrically connect front-side integrated circuit 14 and backside metal layer 16. *Id.*, [0005]. But via structures had also been widely used in the art to provide nonelectrical functions. Thompson, ¶¶46-52.

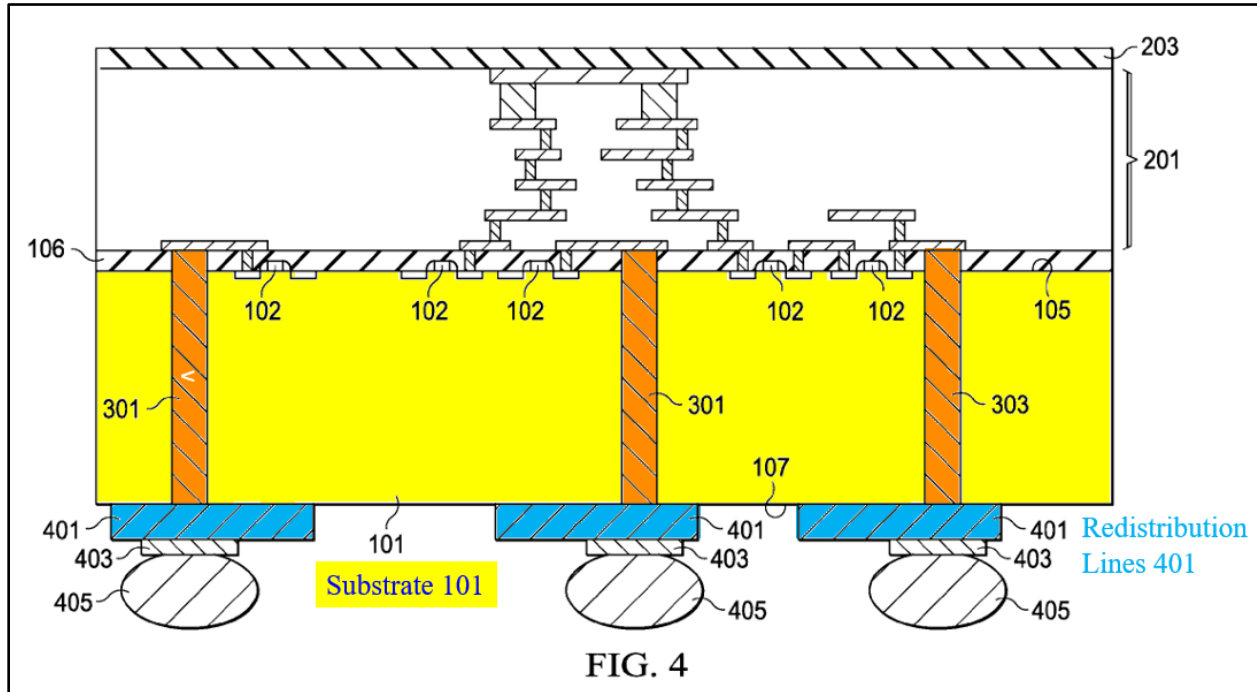
1. Electrical Functions

As to the electrical functions, through silicon vias (TSVs), also called through wafer vias (TWVs), had been used to provide electrical connections along a vertical direction, e.g., connecting devices on the front side of the substrate to the backside metal layer. For example, the following figure shows a TWV 220 is surrounded by a substrate 212 and used for connecting a “backside metal layer 258” to a “metal segment 262 situated over TWV 220.” *Blaschke* (Ex. 1016), [0022]. Metal segment 262 is in turn connected to an active device (not shown) such that “TWV 220 creates a low resistance ground path” between backside metal layer 258 and the active device. *Id.*, [0022]-[0023]; Thompson, ¶47. “TWV 220 includes sidewall dielectric layers 256 surrounding conductive plug 252, which can be made of a highly conductive material such as copper or gold.” *Blaschke*, [0022].



Blaschke, Fig. 2.

As another example, the following figure shows a semiconductor die in which signal vias 301 and power/ground (P/G) vias 303 are formed through a substrate 101 and connected to redistribution lines 401 on the backside of the substrate 101. *Law* (Ex. 1017), [0018]-[0019], [0031]-[0032]. “[R]edistribution lines 401 comprise at least one conductive layer formed of a metal ...,” and therefore constitute backside metal layers. *Id.*, [0032]-[0033]; Thompson, ¶48.



Law, Fig. 4.

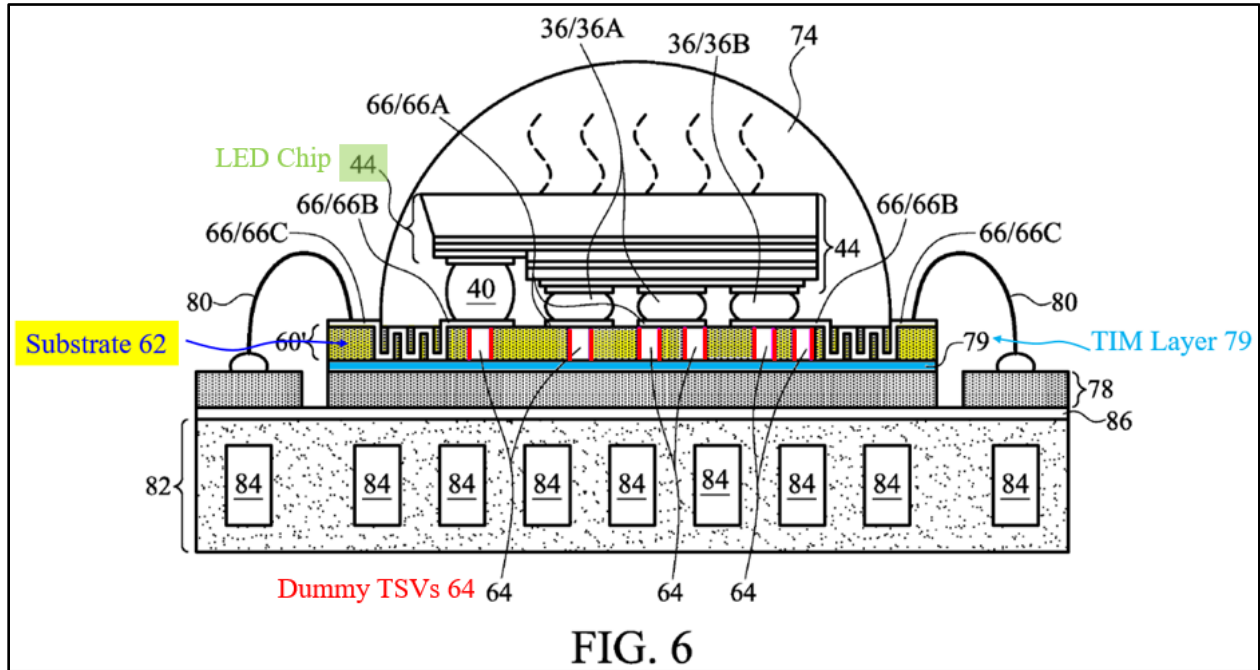
2. Nonelectrical Functions

Regarding the nonelectrical functions, via structures had been used to improve the structural integrity of the wafer or die. Thompson, ¶¶50-52. For example, as shown in the following cross-sectional view (Figure 2) and backside plan view (Figure 3), a semiconductor chip 15 (i.e., a die) includes traditional TSVs (represented by 100a, 100b, 100c, 100d, 100e) located in a central region of the chip, and peripheral TSVs (represented by 100f, 100g, 100h, 100i) in a peripheral region. *Su*, 6:1-14. The traditional TSVs provide electrical connections, whereas the peripheral TSVs serve nonelectrical functions such as to “stiffen the semiconductor chip 15 and resist bending due to” thermal cycling, or to play “a crack stop role in that the TSVs provide interspersed barriers to crack propagation

7:33-37.



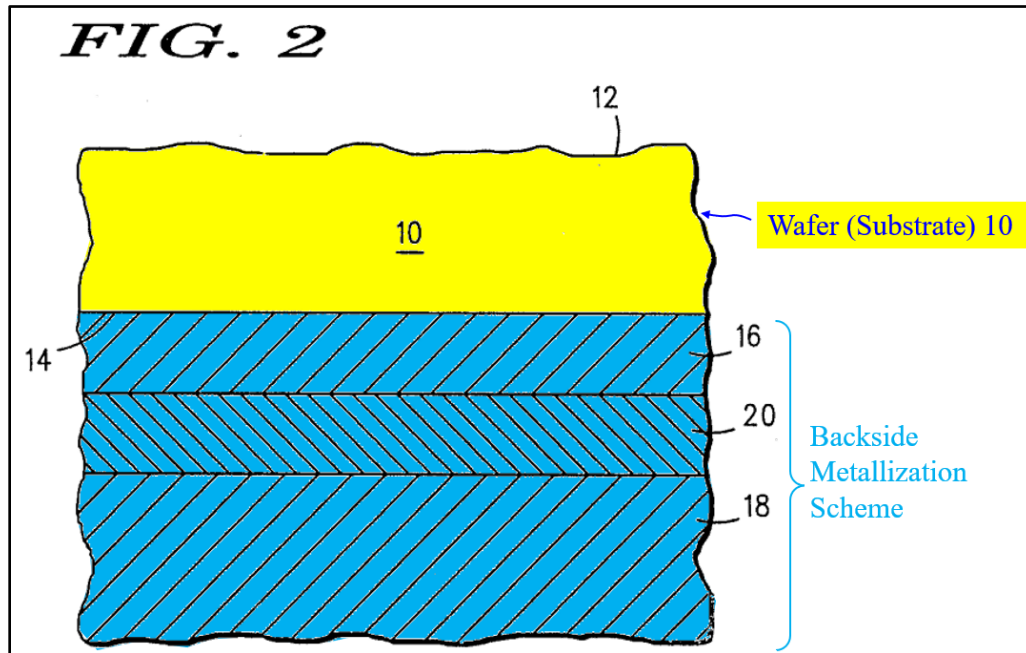
Via structures had also been used to dissipate heat generated by semiconductor devices. For example, the following figure illustrates a “carrier chip 60’ being bonded to at least one LED chip 44.” *Wang* (Ex. 1019), 3:64-67. Carrier chip 60’ includes a substrate 62 with multiple dummy TSVs 64 formed therein. *Id.*, 3:14-19. “TSVs 64 are dummy TSVs since they are not used to conduct [electrical] currents,” but rather are used for “dissipating heat.” *Id.*, 3:23-27. Dummy “TSVs 64 may be formed of copper or other metals....” *Id.*, 3:19-20. Carrier chip 60’ is adhered to a lead frame 78 “through thermal interface material (TIM) layer 79,” which may be made of “pure alloy or metal.” *Id.*, 4:12-21; Thompson, ¶52. Here, the bottom side of carrier chip 60’ is opposite to the side where LED chip 44 (i.e., the active device) is located, thereby constituting the backside of substrate 62. *Supra*, §II.B. Hence, TIM layer 79 constitutes a backside metal layer. Thompson, ¶52.



Wang, Fig. 6.

E. Via Structures to Improve Backside Metal Layer Adhesion

It is desirable to improve backside metal layer adhesion. *Cronin*, 4:4-6; *Zeng*, Abstract. The quest for improved adhesion dates back to at least the 1980s, and early efforts focused on modifying the sub-layer structure and/or material composition of the backside layer. *See, e.g., Sharma* (Ex. 1021); *Thompson*, ¶53.



Sharma, Fig. 1.

Those skilled in the art also used via structures, including the TSVs or TWVs, to improve adhesion. For example, the following “FIG. 3 shows a packaged module with a backside metal ground plane [16] attached to a substrate [10][.]” *Burnham* (Ex. 1022), 5:14-16. Substrate 10 includes a TSV 12 forming “electrical communication with” a device 100 fabricated in the substrate. *Id.*, 5:16-21. The details of the connection portion between TSV 12 and backside metal 16 are illustrated in Figure 2c. *Id.*, 2:15-17, 5:1-3. It shows an oxide layer 14 is disposed between substrate 10 and backside metal 16 to “provide[] improved metal adhesion[.]” *Id.*, 4:48-52. Additionally, TSV 12 forms a protruding portion that extends from the backside of substrate 10 and penetrates into backside metal 16, thereby further improving the backside metal adhesion. *Id.*, Fig. 2c; Thompson,

with the backside metal 16.” *Burnham*, 5:24-26.



Burnham, Figs. 2c, 3.

F. Summary

In summary, it was well-known that:

- (i) improving backside metal layer adhesion to the semiconductor substrate is important and desirable (§II.C);
- (ii) via structures can serve nonelectrical functions (e.g., *Wang's* dummy vias not providing ground connection to active devices) and may be disposed at the peripheral regions of the semiconductor substrate (e.g., *Su's* peripheral TSVs) (§II.D.2); and

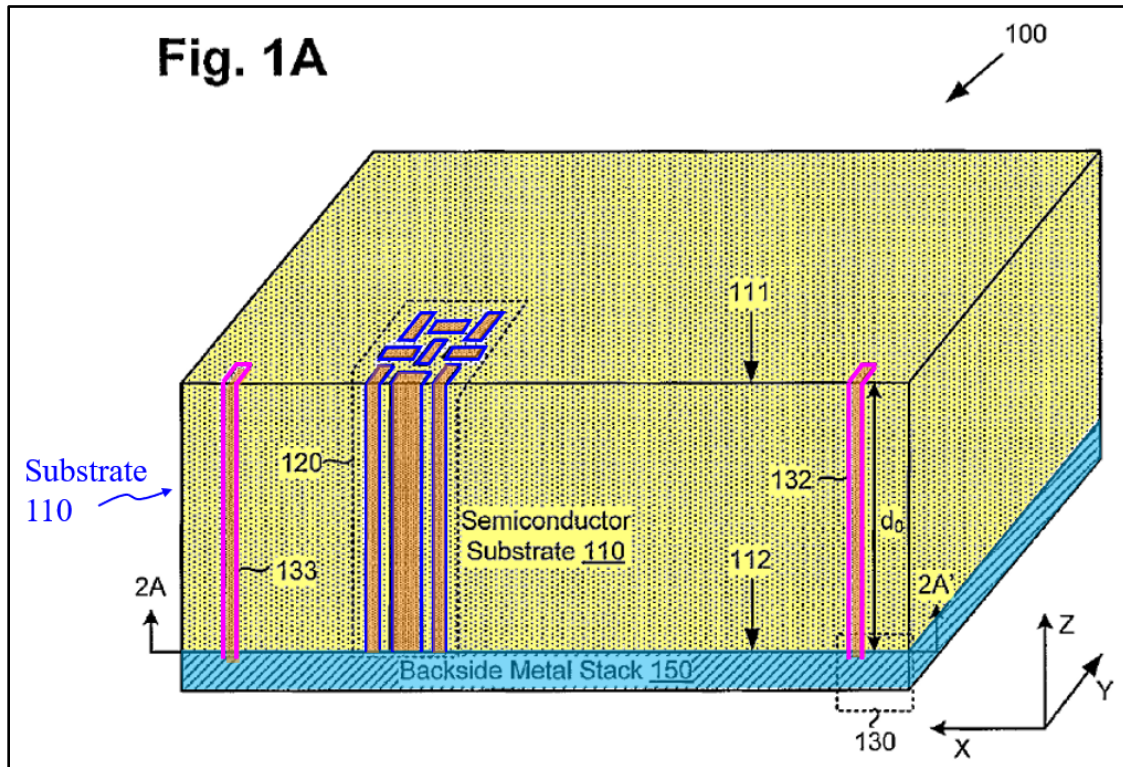
- (iii) the via structures can be used to improve backside metal adhesion by forming a protruding portion to be bonded with the backside metal (§II.E). Thompson, ¶55.

Accordingly, before the time of the '826 patent, the art already possessed all the claimed elements for making “anchor vias for improved backside metal adhesion to semiconductor substrate.” '826 patent, Title; Thompson, ¶56.

III. The '826 Patent

A. Alleged Invention

The '826 patent's Figure 1A shows a semiconductor device 100 including a semiconductor substrate 110 that has a front side surface 111 and a backside surface 112. '826 patent, 2:56-60. Two types of vias are formed in semiconductor substrate 110: (1) a [group 120 through silicon vias \(TSVs\)](#) used for providing electrical ground connection to active devices and formed in the substrate's core region, and (2) [anchor vias 132, 133](#) used for improving [backside metal](#) adhesion and formed in the substrate's peripheral region. *Id.*, 2:53-3:11.



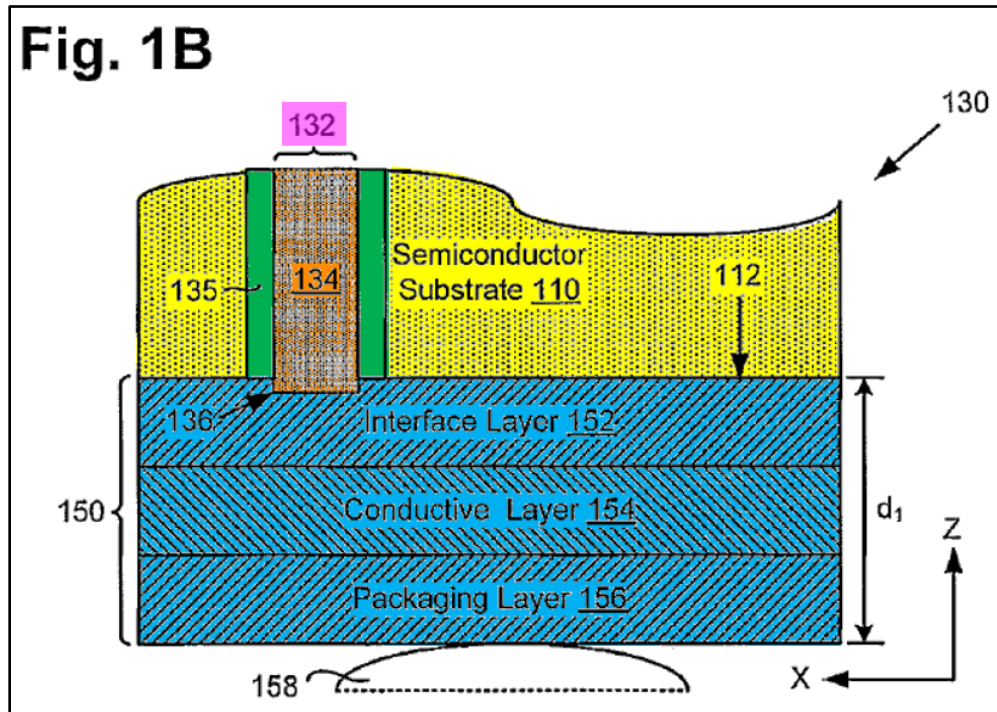
'826 patent, Fig. 1A.

TSV group 120 and anchor vias 132, 133 all have metal fillers, but they serve different purposes. *Id.*, 3:5-17. Specifically, the “[m]etal filler within group 120 of TSVs provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110....” *Id.*, 3:5-11. “By contrast, [the] metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices and instead provides physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150....” *Id.*, 3:12-17. Moreover, even if the metal

filler within anchor vias 132, 133 contacts a front side metal layer,⁴ the metal layer is patterned such that the metal filler only has a floating voltage potential during operation. *Id.*, 3:21-27. Also, unlike TSV group 120, anchor vias 132, 133 do not need to be through the entire substrate, but rather may be formed to a certain depth into the substrate. *Id.*, 3:17-21.

Figure 1B, below, provides a magnified cross-sectional view of anchor point 130 of anchor via 132. *Id.*, 3:32-38. As shown, “metal filler 134 may protrude from bottom side 112 to form protruding portion 136” that metallicity bonds with backside metal stack 150. *Id.*, 3:43-48. Anchor via 132 may have an insulating layer 135 formed on its sidewall and backside metal stack 150 may include one or more sub-layers. *Id.*, 3:38-43, 3:65-67.

⁴ An example of such metal layer (not illustrated in the '826 patent) is the overlying metal segment 262 in Figure 2 of *Blaschke. Supra*, §II.D.1; Thompson, n.5.



'826 patent, Fig. 1B.

The '826 specification also describes some other claimed features. *Id.*, Figs. 2A, 2C, 2D, 3A; Thompson, ¶¶60-63.

B. Prosecution History

During prosecution, in response to the Examiner's rejection based in part on U.S. Patent No. 8,431,481 (*Dunne*, Ex. 1023), the applicant amended both independent claims 1 and 11 to add the limitation "wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate," and argued that *Dunne*'s TSV is used for providing a ground connection and hence does not disclose the amended

claims. Ex. 1002, 59-66, 73-85. The Examiner subsequently allowed the application. *Id.*, 88-92.

C. Claim Construction

Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). To the extent it is needed to resolve any dispute in this proceeding, Petitioner submits the following proposed construction. Petitioner believes no other terms need construction.⁵

1. Independent method claim 11 does not require the steps therein to be performed in their recited order

Claim 11 recites the following steps:

- [11a] “forming at least one anchor via in at least one corner of a semiconductor substrate;”
- [11b] “depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;” and
- [11c] “forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to

⁵ Petitioner reserves the right to argue in an appropriate forum that certain limitations in the challenged claims are indefinite.

said protruding portion of said metal filler of said at least one anchor via.”

’826 patent, 8:35-43.

Claim 11 does not require steps [11b] and [11c] to be performed in their recited order. Generally, a method claim is not limited to the recited order. *Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001). The Federal Circuit has adopted a two-part test to determine whether a claim should be limited to a specific sequence: “[f]irst, we look to the claim language to determine if, as a matter of logic or grammar, [the steps] must be performed in the order written,” and, “[i]f not, we next look to the rest of the specification to determine whether it ‘directly or implicitly requires such a narrow construction.’” *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369–70 (Fed. Cir. 2003).

Here, as to part one of the test, the grammar does not suggest an order because the claimed “forming a backside metal layer on a bottom surface of said semiconductor substrate” does not mention anything about the “metal filler.” Logic also does not suggest an order because the backside metal layer is formed “on a bottom surface of said semiconductor substrate,” not the “metal filler,” and claim 11 does not recite that the bonding is an affirmative step that happens at any particular time or depends on the order of [11b] and [11c]. ’826 patent, 8:34-46.

As to part two, the figures in the '826 patent all depict final structures that do not depend on any particular order of fabrication steps. *Id.*, 1:50-2:28; Thompson, ¶70. And the rest of the specification does not describe any specific method for making the structures. Thus, the specification cannot limit the steps in claim 11 to a particular order.

IV. Statement of Precise Relief Requested

A. Prior Art

- Ex. 1004, US2009/0079056 (“*Conn*”), published March 26, 2009, is prior art under §§102(a), (b), and (e).
- Ex. 1005, US2014/0138844 (“*Gambino*”), filed November 21, 2012, published May 22, 2014, is prior art under §102(e).
- Ex. 1008, US2012/0104546 (“*Ding*”), published May 3, 2012, is prior art under §§102(a) and (e).
- Ex. 1009, US2013/0082382 (“*Torii*”), filed September 28, 2012, and published April 4, 2013, is prior art under §102(e).
- Ex. 1010, US2012/0256310 (“*Ide*”), published October 11, 2012, is prior art under §§102(a) and (e).

B. Challenges

Ground		Challenged Claims	Basis	Prior Art
1		1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	§102	<i>Conn</i>
2	2A	1, 2, 4-7, 9, 11, 12, 14-17, 19	§103	<i>Conn</i> in view of knowledge of a person of ordinary skill in the art (POSA)
	2B	8, 18	§103	<i>Conn</i> in view of knowledge of POSA and Applicant Admitted Prior Art (AAPA)
3	3A	1, 2, 4-7, 11, 12, 14-17	§103	<i>Gambino</i> in view of <i>Conn</i>
	3B	10, 20	§103	<i>Gambino</i> in view of <i>Conn</i> and <i>Ding</i>
4		1, 8-11, 18-20	§102	<i>Torii</i>
5		1-3, 9, 11-13, 19	§102	<i>Ide</i>

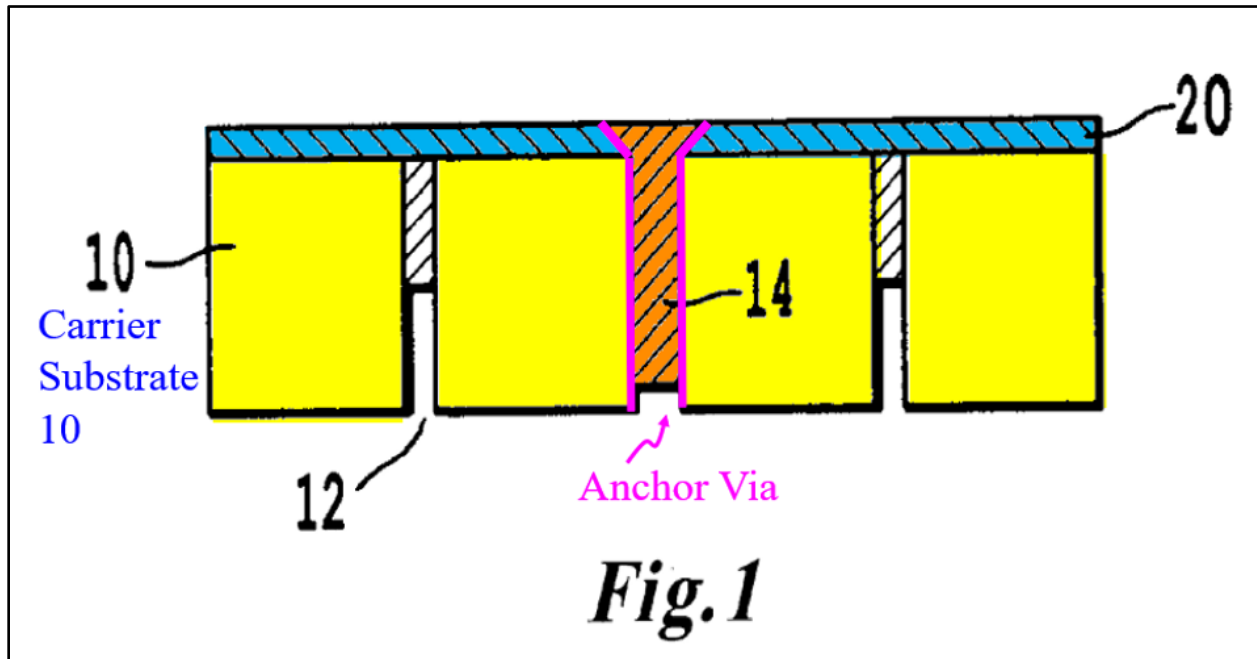
V. Level of Ordinary Skill in the Art

A POSA at the time of the purported invention of the '826 patent (March 11, 2013) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Thompson, ¶¶73-74. Additional relevant work experience can compensate for less education, and *vice versa*. *Id.*

VI. Ground 1: *Conn* Anticipates Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19

A. Overview of *Conn*

Like the '826 patent, *Conn* discloses using “anchor vias” to “secure” a “conducting layer,” e.g., backside metal layer, to a “carrier substrate.” *Conn*, Abstract, [0011]. Specifically, Figure 1 shows a side view of an electronic package structure, which “includes a carrier substrate 10 having first and second surfaces (e.g., the top and bottom surfaces of the carrier substrate)[.]” *Id.*, [0029]. “[C]arrier substrate 10 ha[s] at least a **conducting layer 20** formed on a first main surface of the carrier substrate 10.” *Id.*, [0026]. “[C]arrier substrate 10 ... has one or plural vias 12,” which “can be through-vias or can be vias that extend from the first main surface but do not reach the opposing second main surface of the carrier substrate 10.” *Id.*, [0028]. At least one of vias 12 is filled with “a **via conductor 14**” that connects to **conducting layer 20**, thereby forming “an **anchor via**.” *Id.*; Thompson, ¶¶78-79. **Via conductor 14** in the **anchor via** forms “a rivet [] in the carrier substrate and in contact with the **conducting layer 20** by which the **conducting layer 20** maintains its structure under thermal stress.” *Conn*, [0028]. In the **anchor via** shown in Figure 1, “**via conductor 14** is formed to enter at least partially in the via 12 but the **via conductor 14** does not necessarily have to go all the way through the via 12.” *Id.*; *Conn*, [0032].

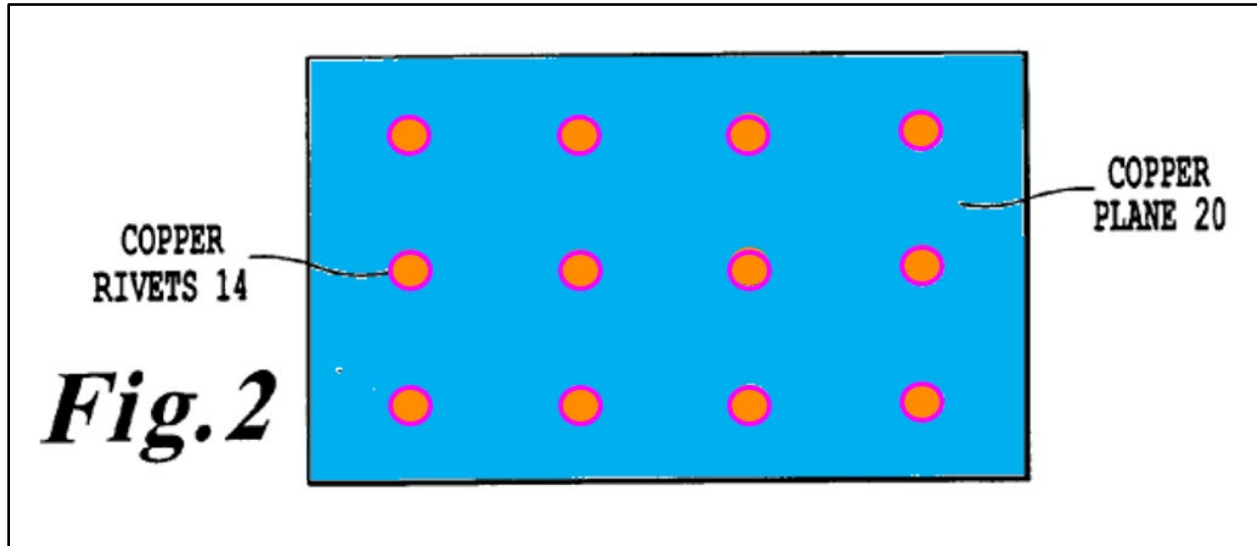


Conn, Fig. 1.

Conn explains that the above structure can be used for packaging electronic devices (e.g., computing devices) that, during usage, will produce a large amount of heat and undergo repeated thermal cycles. *Id.*, [0005]-[0008]. In this environment, **conducting layer 20** tends to crack or delaminate from the carrier substrate, because they are made of materials (e.g., copper and silicon, respectively) that have drastically different thermal conductivities and coefficients of thermal expansion, which induces significant thermal stresses under heat. *Id.*, [0005], [0008], [0027], [0030]. The **anchor via**'s rivet structure solves this problem by "secur[ing] the **conducting layer 20** to the carrier substrate 10" and preventing "delamination." *Id.*, [0029]-[0030].

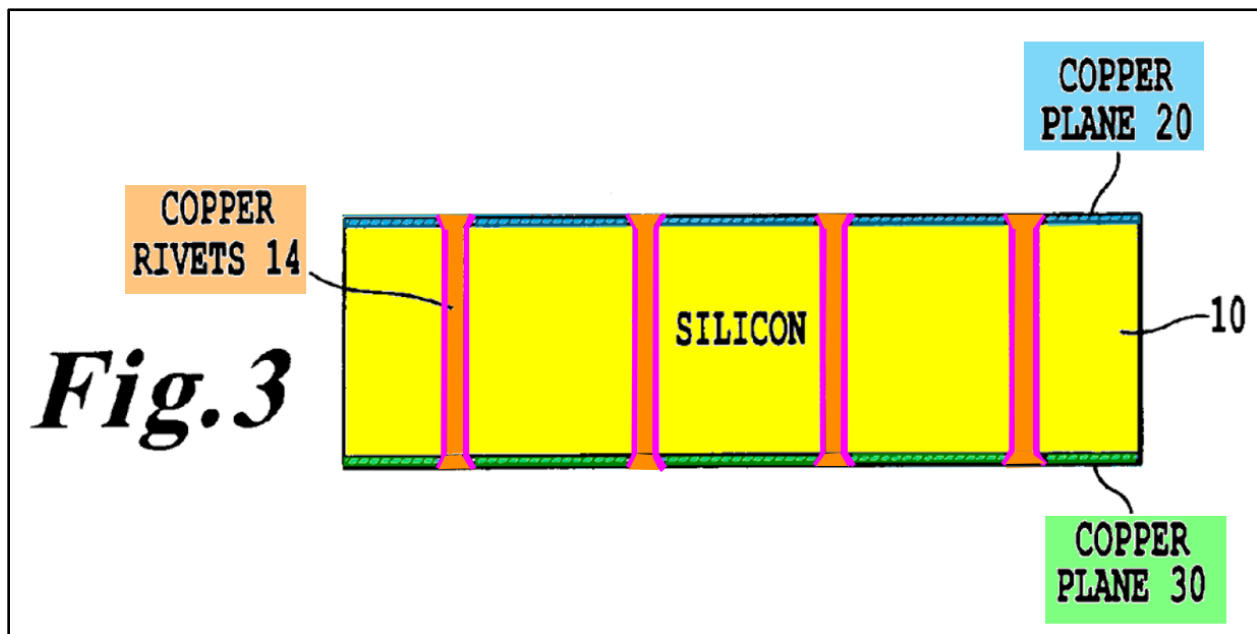
The electronic package can include multiple **anchor vias**. *Id.*, [0029]. Figure 2 shows a plan view in which multiple “**copper rivets 14**,” i.e., **via conductors 14** in multiple **anchor vias**, are “distributed relative to the **conducting layer 20** in a pattern.” *Id.*, [0018], [0035], Fig. 2; Thompson, ¶80. “[C]onducting layer 20 has a length and a width extending laterally in two dimensions across a major part of the first surface of the carrier substrate 10,” and may “cover[] at least 90% of an entirety of the surface area of the carrier substrate.”⁶ *Conn*, [0029], [0031]. “The **anchor vias** form plural **attachments (i.e., rivets)** along the length and the width of the **conducting layer 20** to secure the **conducting layer 20** to the carrier substrate 10.” *Id.*

⁶ Figure 2 (plan view) does not show carrier substrate 10, which is underneath and slightly larger than **conducting layer 20**. Thompson, n.6.



Conn, Fig. 2.

Conn discloses that the **anchor vias** can be used to secure conducting layers formed on either or both of the two main surfaces (i.e., top and bottom surfaces as shown in Figure 3) of carrier substrate 10. *Id.*, [0037]-[0041]; Thompson, ¶81.

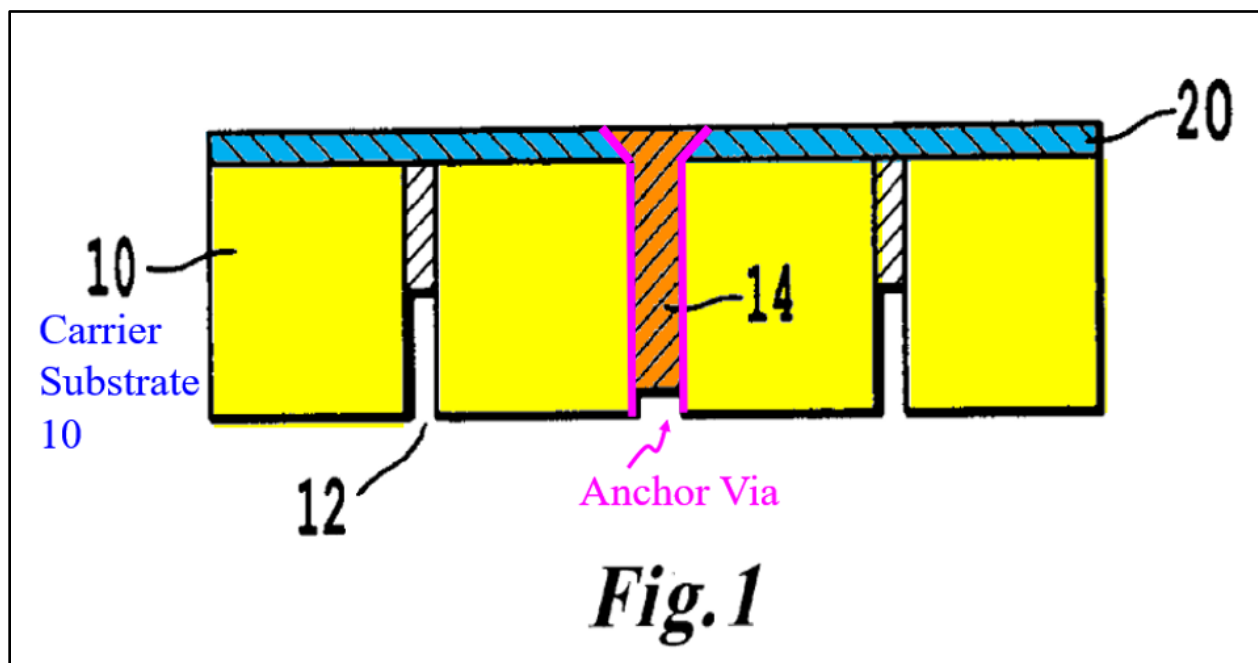


Conn, Fig. 3.

B. Independent Claim 1

1. [1pre] A structure comprising:

Conn discloses the preamble by disclosing an electronic package structure as illustrated in its Figure 1. *Conn*, [0017], [0029]; Thompson, ¶82. The electronic package includes “a carrier substrate 10 having at least a **conducting layer 20** formed on a first main surface of the carrier substrate 10.” *Conn*, [0026].

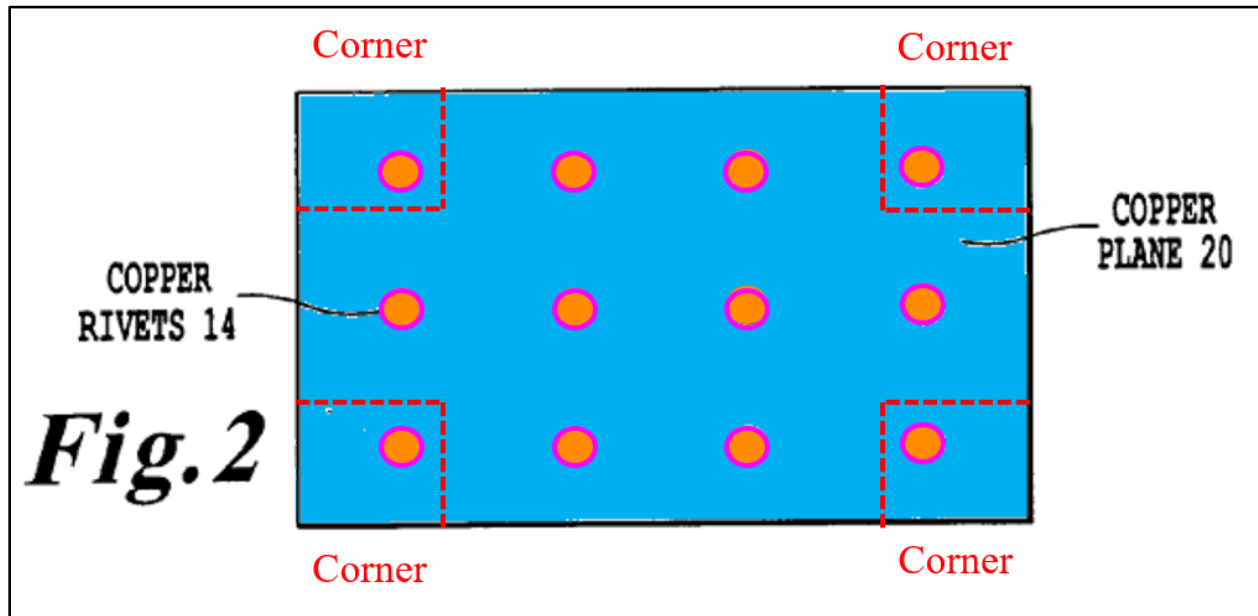


Conn, Fig. 1.

2. [1a] at least one **anchor via disposed in at least one **corner** of a semiconductor substrate;**

Conn discloses [1a] by disclosing carrier substrate 10 in Figure 1 includes “a plurality of **anchor vias** (e.g., **via conductor 14**)[.]” *Id.*, [0029]. Moreover, the plan view in Figure 2 shows the plurality of **anchor vias** (see **copper rivets 14** in Figure 2) are “distributed relative to the **conducting layer 20** in a pattern[.]” *Id.*, [0035].

Figure 2 shows the **anchor via** pattern covers the entire surface of **conducting layer 20**, such that some **anchor vias** are disposed at the **corners** of **conducting layer 20**.⁷ *Id.*; Thompson, ¶83.



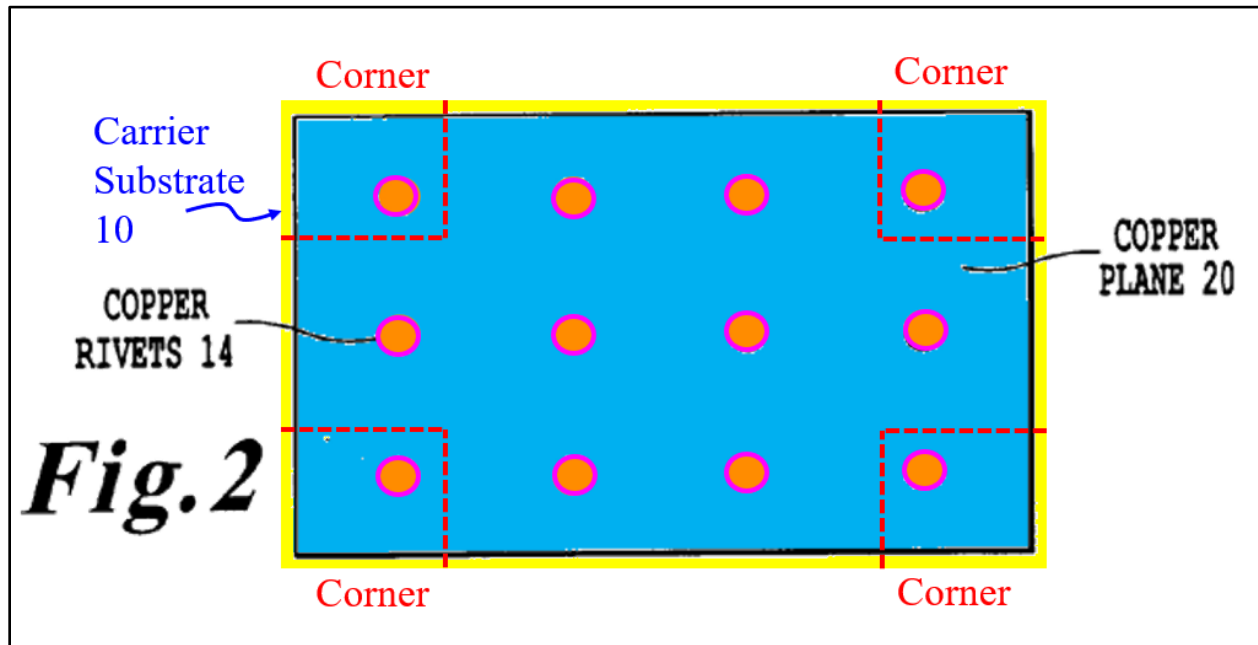
Conn, Fig. 2.

Figure 2 does not show carrier substrate 10, but *Conn* discloses that **conducting layer 20** can cover more than “90% of an entirety of the surface area of the carrier substrate,” even approaching “100%.” *Id.*, [0031]; Thompson, ¶84.

Under this configuration, **conducting layer 20** covers almost the entirety of the surface area of carrier substrate 10, as shown in the following modified Figure 2.

⁷ Features clearly shown in prior art drawings can be relied for anticipation. *In re Mraz*, 455 F.2d 1069, 1072 (C.C.P.A. 1972); *Ex parte Jurek*, Appeal 2018-006215, p. 6 (P.T.A.B. Apr. 17, 2019).

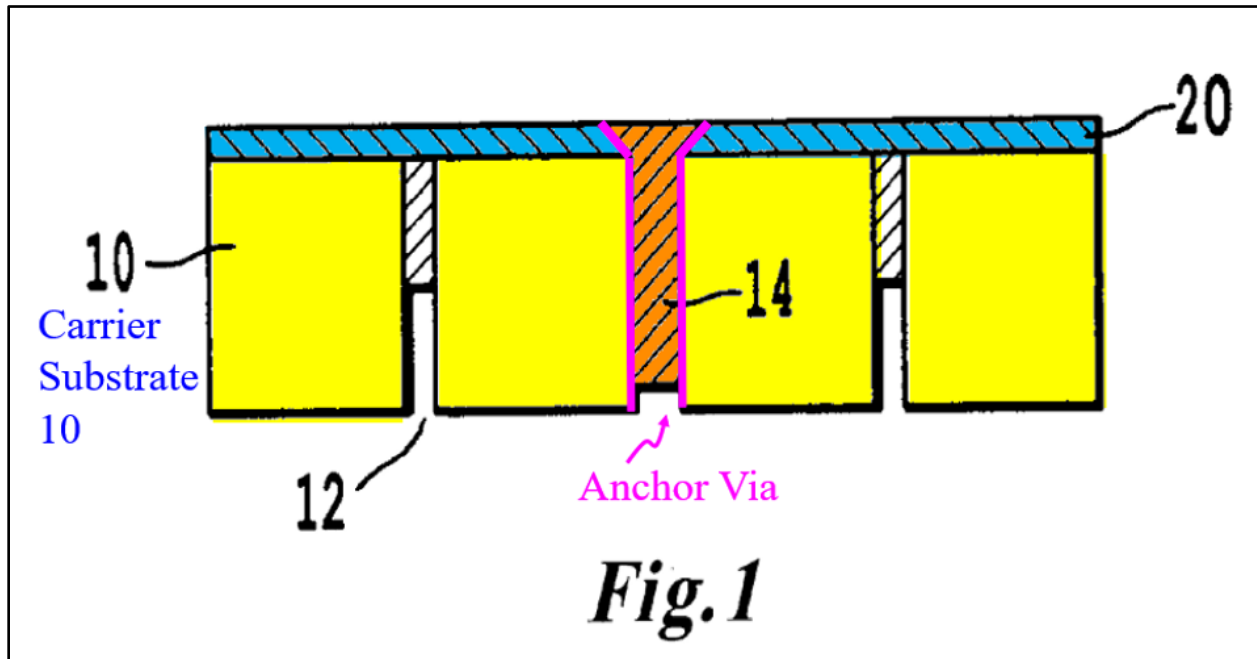
Thompson, ¶84. Namely, the **corners** of **conducting layer 20** are also the **corners** of carrier substrate 10. *Id.* It follows that the **anchor vias** located at the **corners** of **conducting layer 20** are also located at the **corners** of carrier substrate 10. *Id.*



Conn, Fig. 2 (modified).

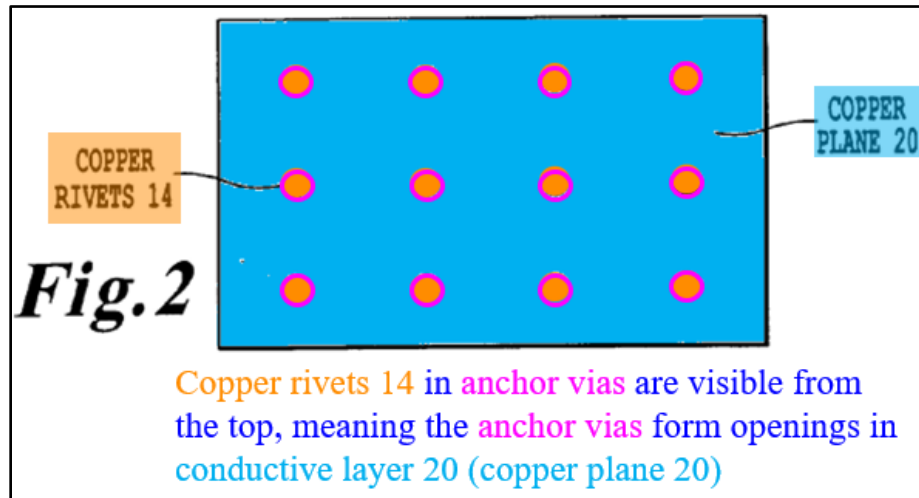
3. [1b] a **metal filler** within said at least one **anchor via**, said **metal filler** having a **protruding portion** extending from a backside of said semiconductor substrate;

Conn discloses [1b] by disclosing the **via conductors** in the **anchor vias** form rivet structures (i.e., “**copper rivets 14**” in Figure 2) that **protrude** from a side of the substrate surface. Thompson, ¶¶85-90. First, as shown in Figure 1, *Conn* discloses the claimed “**metal filler**” by disclosing each **anchor via** is formed by filling “a **via conductor 14** [] in a via 12.” *Conn*, [0028]; *id.*, [0029]. “[V]ia conductor 14 may be formed of copper, aluminum, gold, silver or other conductors.” *Id.*, [0033].



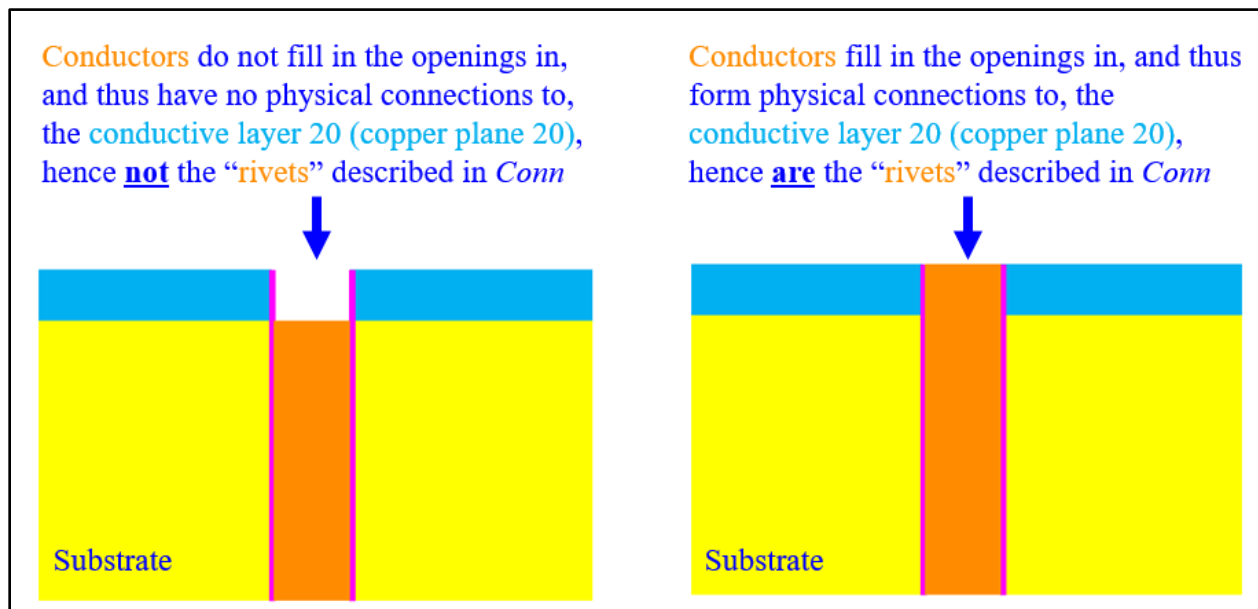
Conn, Fig. 1.

Second, *Conn* discloses the claimed “protruding portion” by disclosing via conductors 14 in the anchor vias form “rivets” (i.e., “attachments”) that are mechanically “connected to” and “in contact with” conducting layer 20. *Id.*, [0028]-[0029]; *Conn*, [0030], [0038], [0040], [0055], Figs. 1-3. Figure 2, below, shows that “copper rivets 14” (i.e., via conductors 14 in the anchor vias) are visible. *Id.*, Fig. 2. This means the anchor vias form openings in conducting layer 20. Thompson, ¶86.



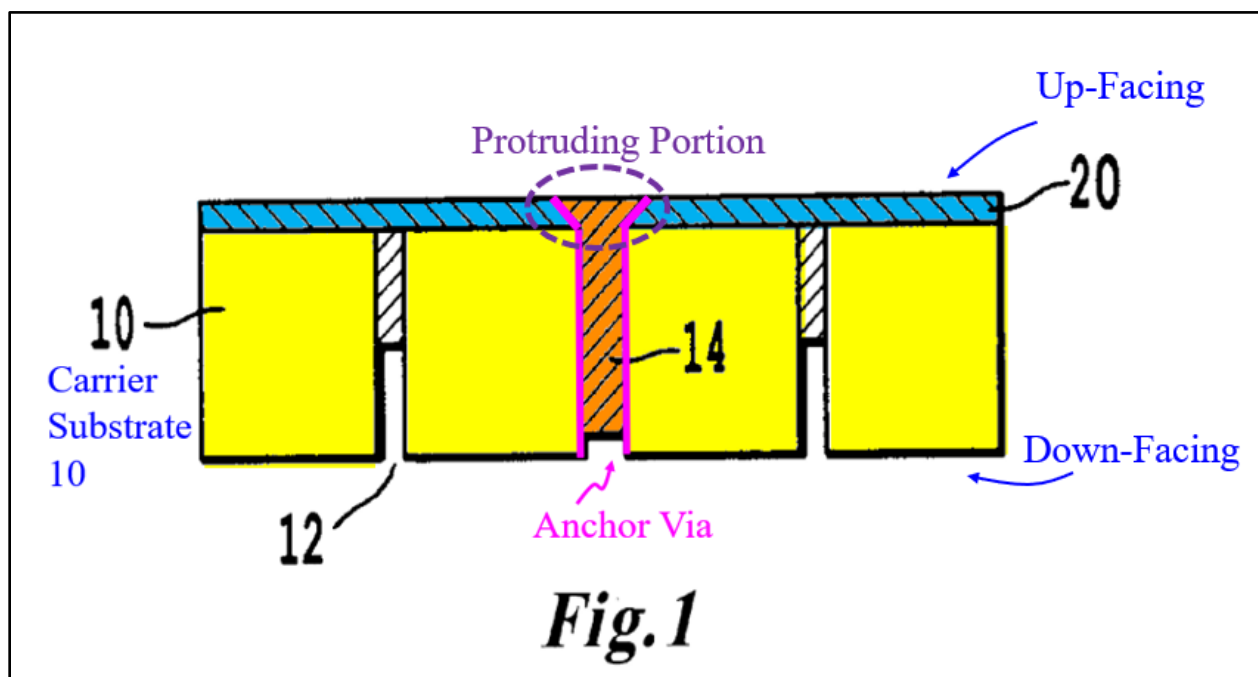
Conn, Fig. 1.

Moreover, as shown in the following schematic illustration, a POSA would understand that the anchor vias' copper rivets 14 (i.e., conductors) must enter the openings in conducting layer 20, to achieve Conn's described physical connection between conducting layer 20 and copper rivets 14. Thompson, ¶¶87-88.



Thompson, ¶88.

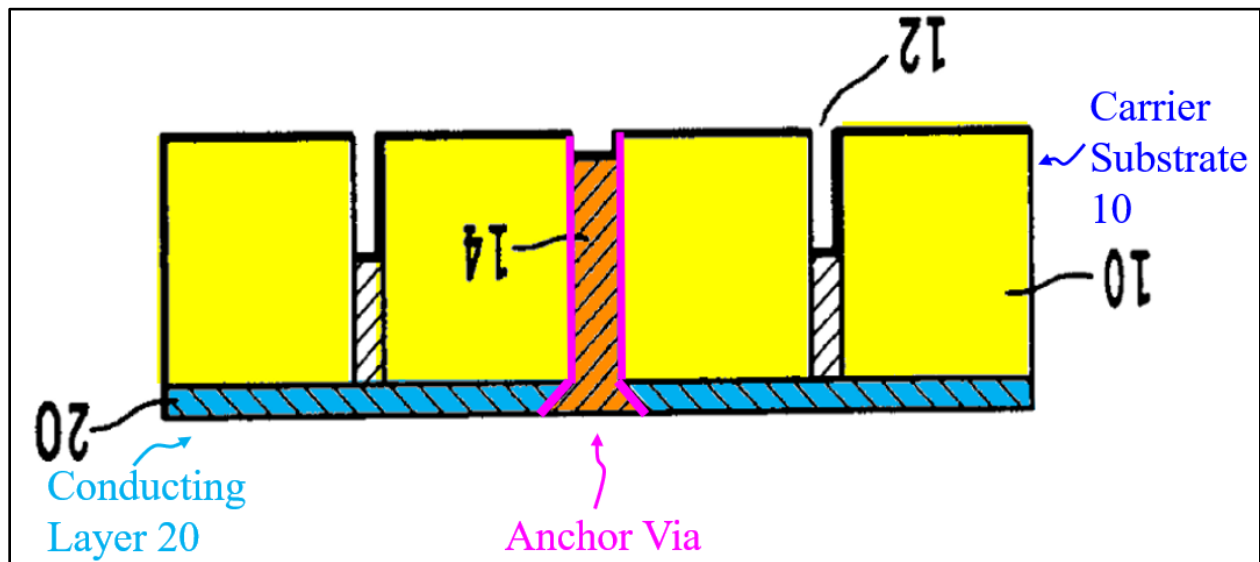
Therefore, as shown below, a POSA would understand that *Conn*'s anchor via rivet is a conductor that has an end entering conducting layer 20 and forming "a protruding portion extending from ... said semiconductor substrate," as claimed. Thompson, ¶89. This understanding is also consistent with the dictionary definition of "rivet," which is described as a metal structure "for uniting two or more pieces by passing the shank through a hole in each piece...." Ex. 1025, 3; Thompson, ¶89. Like the shank, *Conn*'s anchor via rivet has a protruding portion passing through the conducting layer. Thompson, ¶89.



Conn, Fig. 1.

Third, *Conn*'s conducting layer 20 is on a side of the substrate corresponding to the claimed "backside." Thompson, ¶90. A POSA would understand the backside can face either up or down, *supra*, §II.B, so the up-facing side shown in

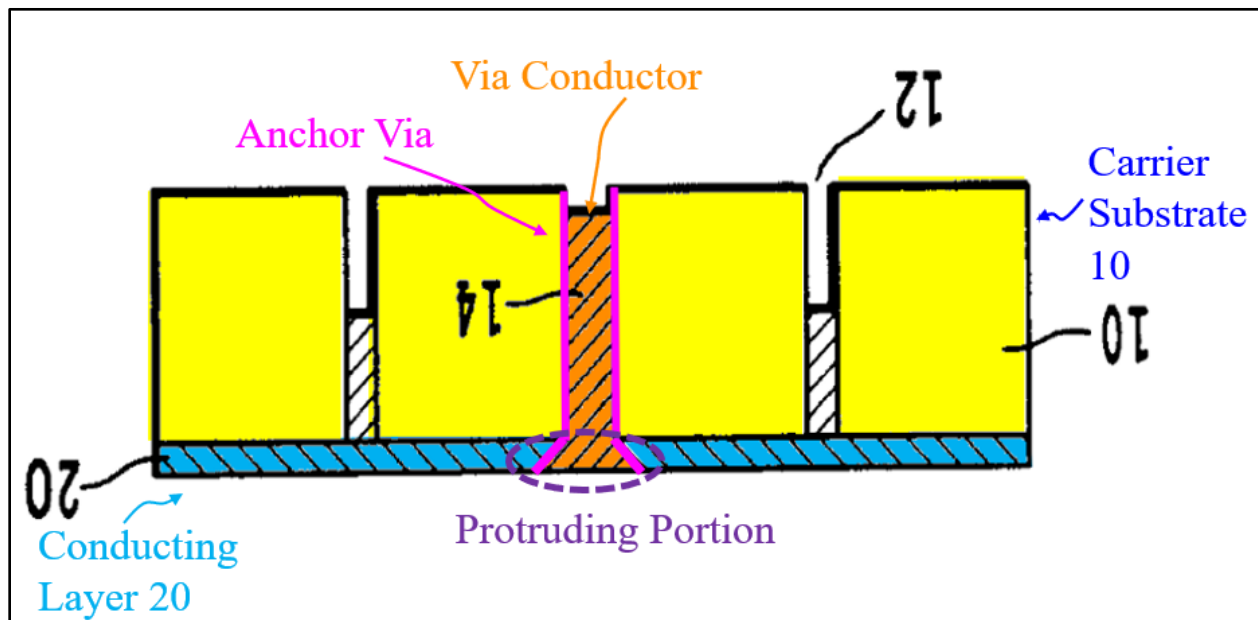
Conn's Figure 1, above, meets the claimed "backside." *Id.* Moreover, as illustrated below, a POSA would understand **conducting layer 20** in Figure 1 can also face down because *Conn*'s text generally describes **it** as being formed on "a first main surface" of carrier substrate 10, without limiting the first main surface to be up-facing or down-facing. *Conn*, [0026]. Additionally, *Conn* discloses the **anchor vias** can act as rivets to secure conducting layers on opposite sides of carrier substrate 10, confirming **conducting layer 20** is not limited to any particular side. *Id.*, [0037]-[0038], [0040], Fig. 3; Thompson, ¶90. Accordingly, *Conn* discloses that **conducting layer 20** and the **rivet protruding portion** formed therein are on the "backside," as claimed. Thompson, ¶90.



Conn, Fig. 1 (rotated by 180°).

4. [1c] a **backside metal layer** on a bottom surface of said semiconductor substrate, said **backside metal layer** being bonded to said **protruding portion** of said **metal filler** of said at least one **anchor via**;

Conn discloses [1c] by disclosing **conducting layer 20** in Figure 1 is disposed on one of the main surfaces of the carrier substrate and is connected to the **protruding portion** of the **anchor via conductor**. Thompson, ¶¶91-92. First, the '826 patent equates “bottom surface” to “backside.” '826 patent, 2:56-60 (“semiconductor substrate 110 having ... bottom surface 112, or backside”). As discussed in §VI.B.3, *Conn*’s **conducting layer 20** is on the backside, so it constitutes the claimed “**backside metal layer**” and the substrate surface on which **conducting layer 20** is disposed constitutes the claimed “bottom surface.” Thompson, ¶91.



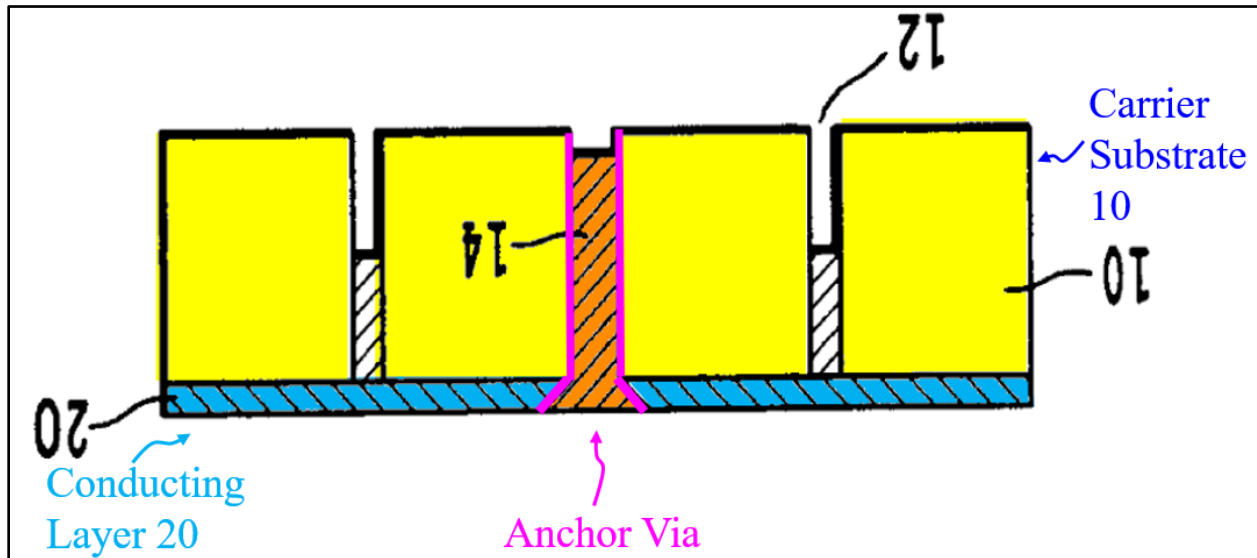
Conn, Fig. 1 (rotated by 180°).

Second, as discussed in §VI.B.3, *Conn* discloses the **via conductors** in the **anchor vias** form **protruding portions** that are mechanically “connected to” and “in contact with” **conducting layer 20**. *Id.*, [0028]-[0029]; *Conn*, [0030], [0038], [0040], [0055], Figs. 1-3. To manufacture such connections, *Conn* discloses that **via conductors 14** and **conducting layer 20** are “formed to be a unitary, single, monolithic structure” or “formed in separate process steps out of a single material” (e.g., copper or tungsten). *Id.*, [0033]-[0034]; *Conn*, [0037], [0041]. A POSA would understand that both methods will cause **via conductors 14** to form a metallic bond with **conducting layer 20**. Thompson, ¶92. Namely, the first method means these two conductors are necessarily fused and bonded to each other. *Id.* Moreover, as commonly done in the integrated-circuit industry, both methods are performed under vacuum at elevated temperature. *Id.* In this condition, metals coming in contact with each other would form a metal-on-metal bond just like that described in the ’826 patent, thereby meeting the “bonded to” limitation. ’826 patent, 3:43-48 (“protruding portion ... form[s] a very strong physical, metal-on-metal bond”); Thompson, ¶92.

5. [1d] wherein said **metal filler** within said at least one **anchor via** does not provide ground connection to one or more active devices in said semiconductor substrate.

Conn discloses [1d] by *not* disclosing that any **anchor vias** provide any ground connection but instead disclosing the **anchor vias** or the **via conductors**

therein do not need to reach the opposite side of the carrier substrate, thus recognizing the purpose of the **anchor vias** is *not* to provide any ground connection. *Conn*, Fig. 1; Thompson, ¶93. Specifically, *Conn* discloses that the **anchor vias** “do not [need to] reach the opposing second main surface of the carrier substrate 10.” *Conn*, [0028]. Separately, *Conn* discloses “**via conductor[s] 14** do[] not necessarily have to go all the way through” the **anchor vias**. *Id.* This means the **anchor vias** and **via conductors 14** are *not* designed for providing electrical connection (including ground connection) to any active device on that side. Thompson, ¶93. Moreover, **via conductors 14** do not provide ground connection to any active devices in the carrier substrate because it may only have “[p]assive components,” not active devices. *Conn*, [0026]; Thompson, ¶93. Finally, vias are not designed for providing electrical connection between devices on the same side of the substrate, so a POSA would understand that **via conductors 14** would not provide ground connection to any active devices on the same side as **conducting layer 20**. Thompson, ¶93.

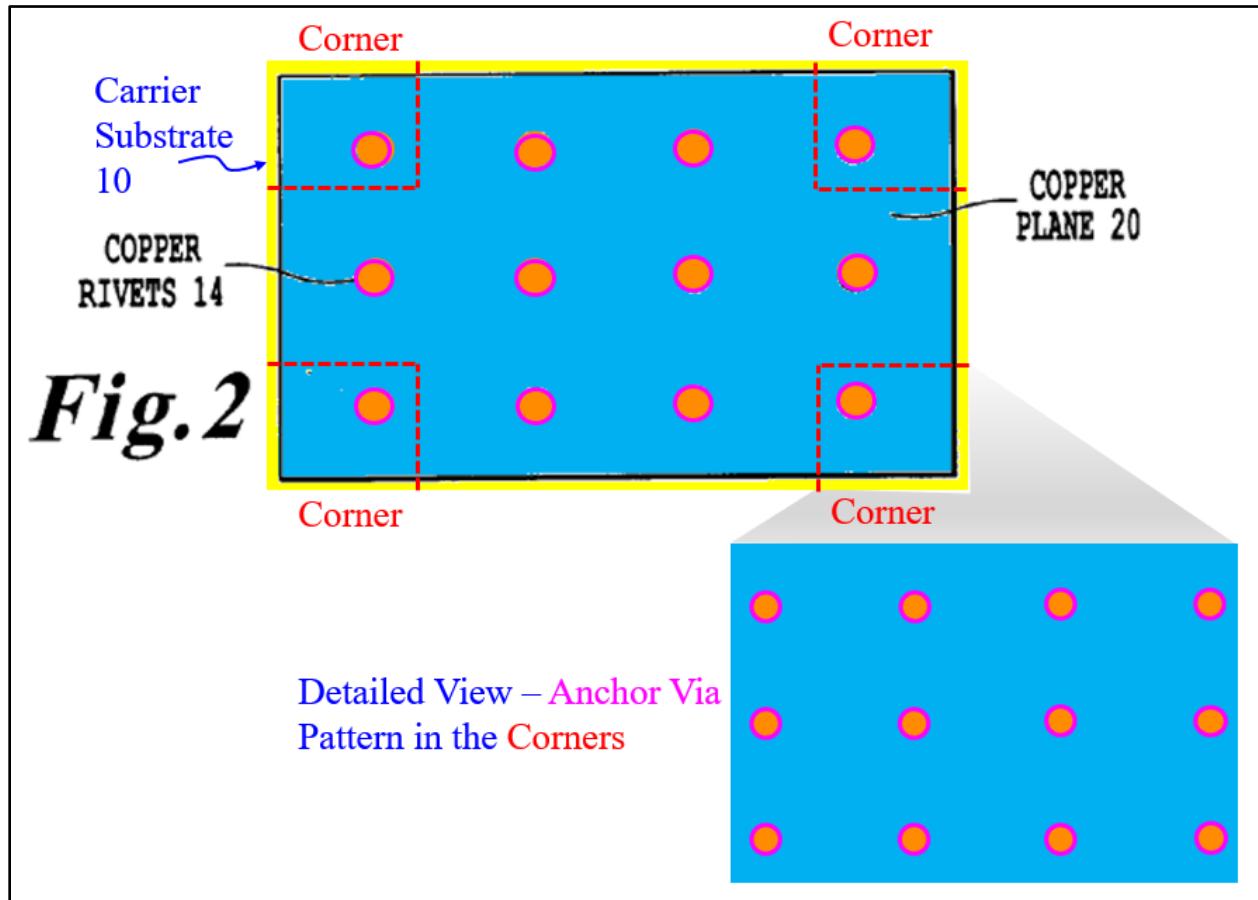


Conn, Fig. 1 (rotated by 180°).

C. Claim 2

The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.

As discussed in §VI.B.2, *Conn* discloses at least one anchor via disposed in a corner of a semiconductor substrate by disclosing a pattern of anchor vias that spreads across the substrate and extends to its corners. *Conn*, [0031], [0035], Fig. 2. This means the anchor vias are repeated in the substrate, including the corners, according to the pattern, and having certain densities as disclosed in *Conn*, e.g., 400 vias per mm². *Id.*, [0035]-[0036]; Thompson, ¶94. Thus, as illustrated below, a POSA would understand that each corner has a pattern of repeating anchor vias, i.e., “a cluster of anchor vias.” Thompson, ¶94.



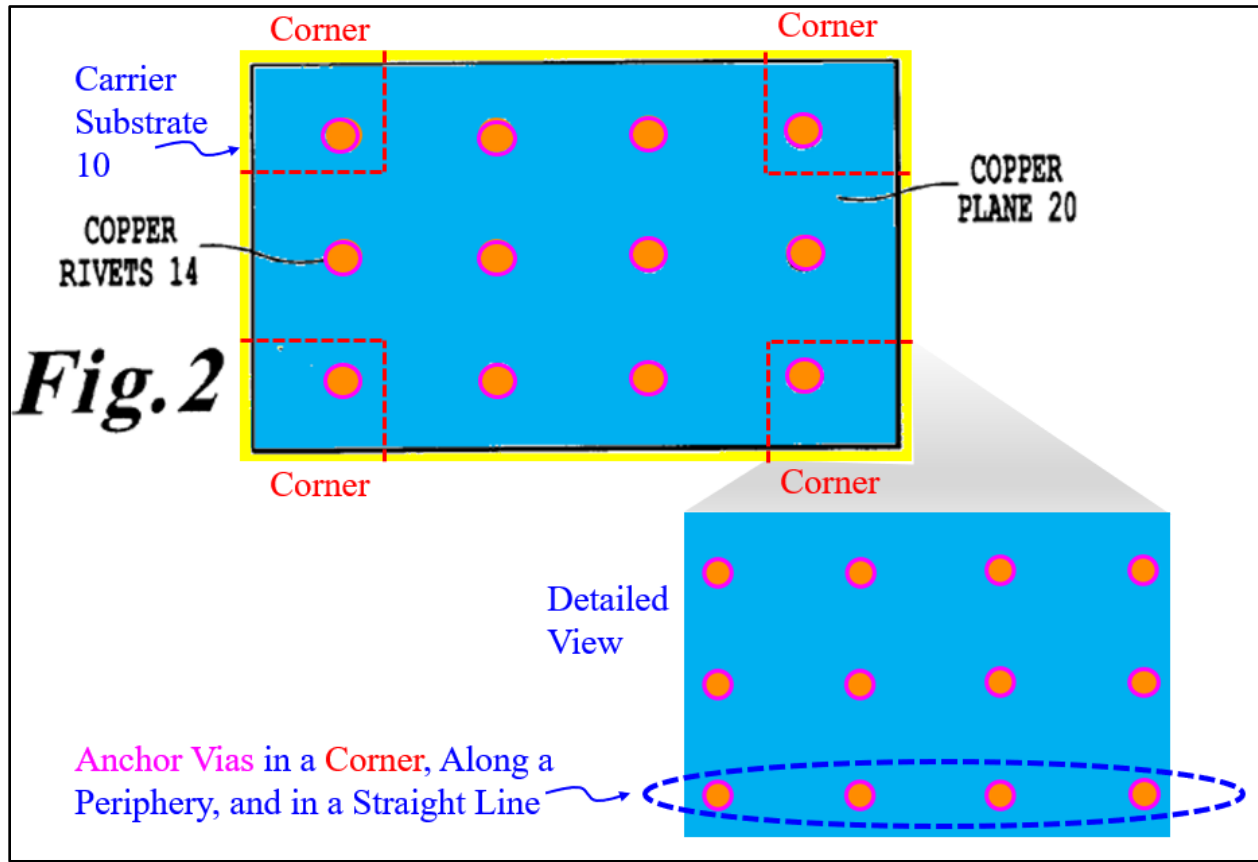
Conn, Fig. 2 (modified).

D. Claim 4

The structure of claim 1, wherein said at least one **anchor via** comprises a plurality of **anchor vias** disposed in a straight line along a periphery of said semiconductor substrate.

Conn discloses claim 4 for the same reasons discussed regarding claim 2.

Supra, §VI.C; Thompson, ¶95. As illustrated below, *Conn* discloses each **corner** of the carrier substrate has the **anchor vias** repeating according to the pattern depicted in Figure 2, within which multiple **anchor vias** are disposed in a straight line and along a periphery. *Conn*, [0031], [0035]-[0036], Fig. 2; Thompson, ¶95.



Conn, Fig. 2 (modified).

E. Claim 5

The structure of claim 4, wherein a linear density of said plurality of **anchor vias** is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

Conn discloses claim 5 by disclosing the **anchor vias** in the pattern depicted in Figure 2 can have a minimum diameter of “30” μm , and a repeating pitch as large as “1000 μm .” *Id.*, [0035]. This means the linear density of the anchor vias

can be as small as $(30/1000) \times 100\% = 3\%$, i.e., “less than approximately 10%,” as claimed.⁸ Thompson, ¶96.

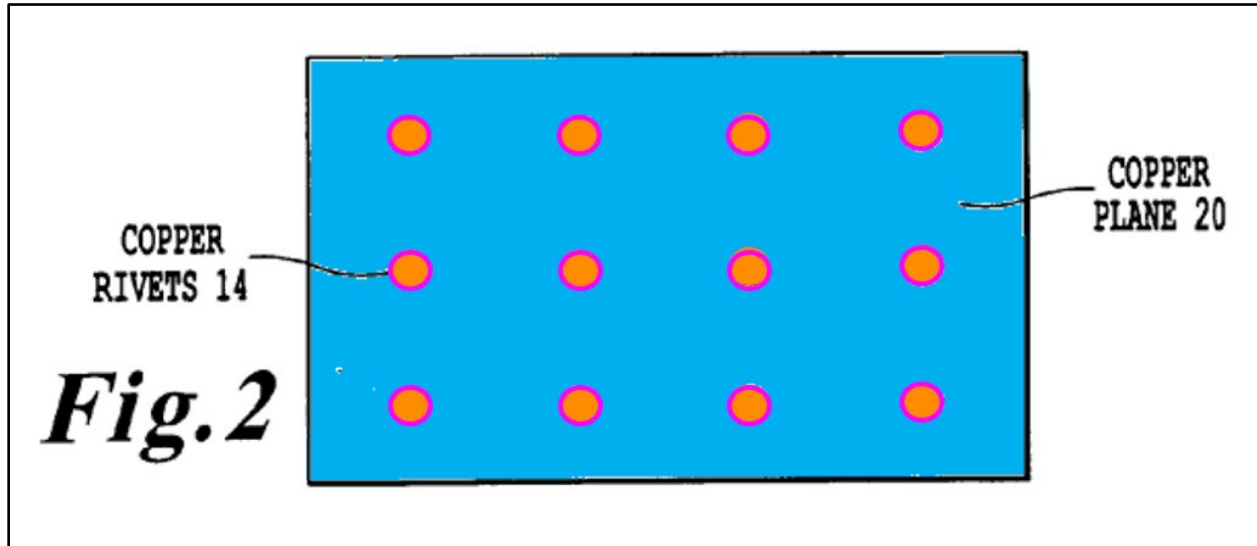
F. Claim 7

The structure of claim 1, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

Conn discloses two use cases that meet claim 7. Thompson, ¶¶97-99.

Specifically, *Conn* discloses that the anchor vias “can have a diameter between 30 and 150 μm .” *Conn*, [0035]. Namely, the smallest possible area occupied by a single anchor via is $\pi \times (0.03/2)^2 \text{ mm}^2$. Thompson, ¶97. In a first case, *Conn* discloses that “[a] density of the via conductors in the [anchor via] pattern is between 0.01 and 400 via conductors per unit square millimeter.” *Conn*, [0035]. Here, the percentage of the total area of the conducting layer occupied by the anchor vias can be as small as $\pi \times (0.03/2)^2 \times 0.01 \times 100\% = 0.0007\%$. Thompson, ¶97.

⁸ *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015) (a claimed range can be anticipated by a prior art reference’s disclosure of a point within the range) (citation omitted).



Conn, Fig. 2.

In a second case, *Conn* discloses “a **conducting layer** having approximate sizes of 140 mm by 80 mm” can have “a minimum of 5000” of **anchor vias**.

Id., [0036]. This means that the percentage of the total area of the **conducting layer** occupied by the **anchor vias** can be as small as

$\pi \times (0.03/2)^2 \times 5000 \times 100\% / (140 \times 80) = 0.03\%$. Thompson, ¶98.

In the above discussion, the “total area” refers to the **conducting layer**, not the carrier substrate. But, as discussed in §VI.B.2, the **conducting layer** covers 90%–100% of the surface area of the carrier substrate. *Conn*, [0031]. Thus, the carrier substrate has a total area no less than that of the **conducting layer**.

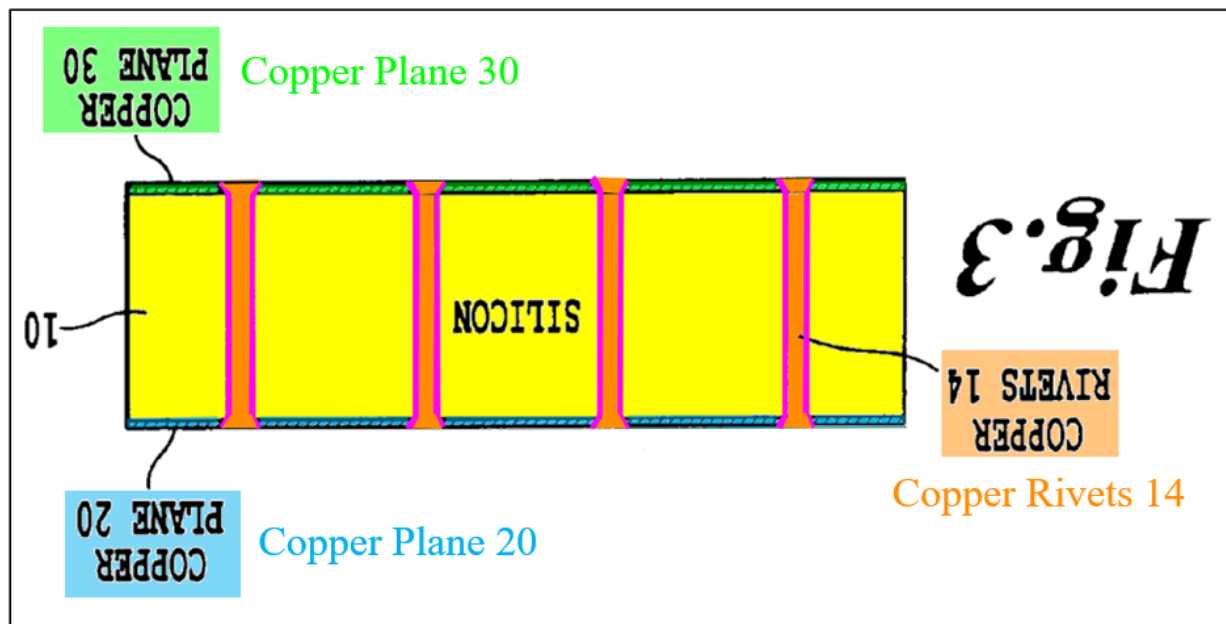
Thompson, ¶99. It follows that the percentage of the total area of the carrier

substrate occupied by the **anchor vias** can be as small as 0.0007% (first case) or 0.03% (second case), both meeting claim 7.⁹ Thompson, ¶99.

G. Claim 9

The structure of claim 1, wherein said **metal filler within said at least one **anchor via** is bonded to a **metal layer** overlying said semiconductor substrate.**

Conn discloses “another **conducting layer 30** is formed on the second main surface of the carrier substrate 10, as shown in FIG. 3.” *Conn*, [0037]. Like **conducting layer 20**, **conducting layer 30** is similarly bonded to the **anchor vias**. *Conn*, [0038], [0040]-[0041]. Thus, **conducting layer 30** constitutes the claimed overlying “**metal layer**.” Thompson, ¶100.



Conn, Fig. 3 (rotated by 180°).

⁹ *Supra*, n.8.

H. Independent Claim 11

Independent claim 11 is substantially similar to claim 1, except it recites a method for making the structure in claim 1. Specifically, claim 11 recites the same structural features of the anchor vias as those in claim 1. The only substantive difference is that claim 11 also recites the method steps of: [11a] “forming” at least one **anchor via**, [11b] “depositing” a **metal filler** within said at least one anchor via, and [11c] “forming” a **backside metal layer**. Thompson, ¶101. *Conn* discloses these steps. *Id.*, ¶¶101-103.

1. “Forming,” depositing,” and “forming” steps

Figure 7 of *Conn* discloses a method for manufacturing the electronic package structure in Figure 1. *Conn*, [0023], [0055]; Thompson, ¶102. This method includes, in part, the following steps: “a step 700 of forming in the carrier substrate a plurality of **vias** extending from the first surface, a step 710 of forming a **first conducting layer** on the first surface of the carrier substrate, [and] a step 720 of depositing a pattern of **via conductors** disposed in a predetermined number of the vias[.]” *Conn*, [0055], Fig. 7. Steps 700, 720, and 710 respectively disclose the claimed [11a] “forming,” [11b] “depositing,” and [11c] “forming” steps.

’826 patent, 8:35-43; Thompson, ¶102. As discussed in §III.C.1, claim 11 does not require the [11b] “depositing” and [11c] “forming” steps to be performed in their recited order. Thus, *Conn*’s disclosure satisfies the claimed steps.

2. Remaining limitations of claim 11

The remaining features of claim 11 are similar to those in claim 1 and disclosed by *Conn* for the same reasons in §§VI.B.2–VI.B.5. Thompson, ¶104.

I. Claims 12, 14, 15, 17, 19

Claims 12, 14, 15, 17, and 19 are anticipated by *Conn* for the reasons discussed for claims 11, 2, 4, 5, 7, and 9. Thompson, ¶¶105-109.

VII. Ground Set 2: *Conn*-Based Obviousness

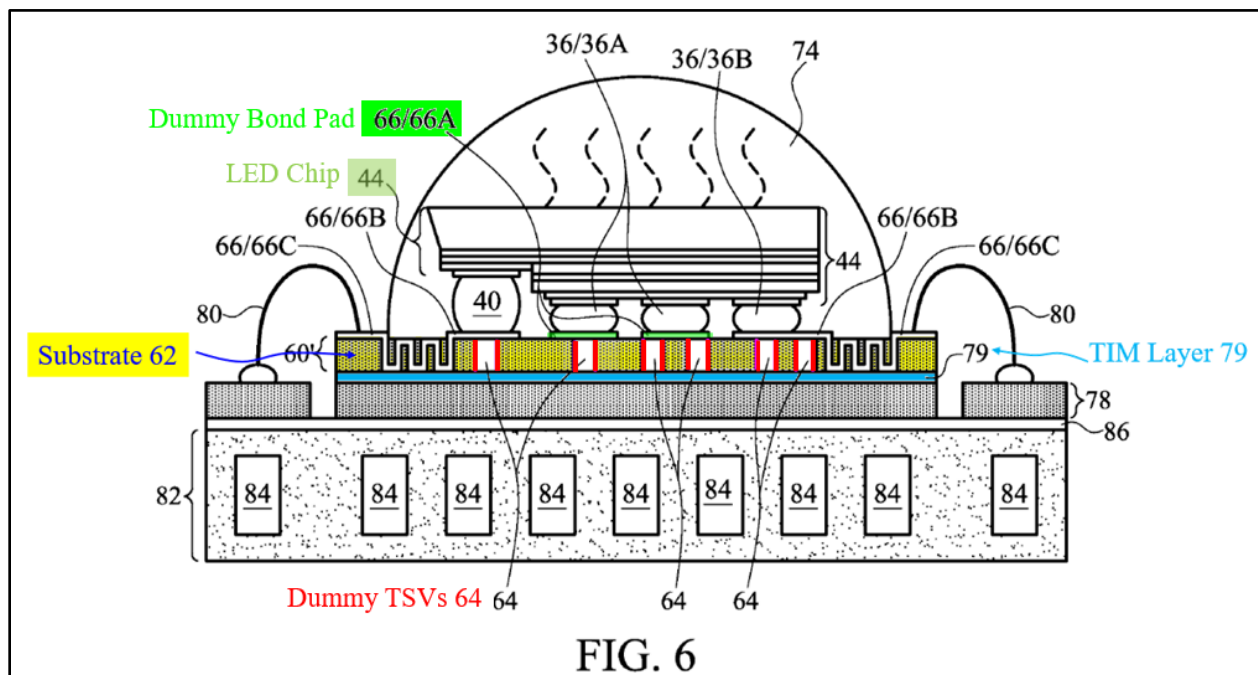
A. Ground 2A: *Conn* in View of Knowledge of POSA Renders Obvious Claims 1, 2, 4-7, 9, 11, 12, 14-17, 19

1. Claims 1, 11: “backside metal layer” and “does not provide ground connection”

As discussed in §§VI.B.4 and VI.B.5, *Conn* anticipates “a backside metal layer” and “said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.” Nevertheless, to the extent that HID may (erroneously) argue that *Conn* does not expressly disclose “backside” or “active devices,” they would have been obvious based on *Conn* and a POSA’s knowledge. Thompson, ¶110.

Specifically, *Conn* discloses that its carrier substrate is used “for mounting of semiconductor chip devices and components.” *Conn*, [0003]; *id.*, [0030], [0035]. *Conn* does not show how the chips are mounted, but a POSA would have known this. Thompson, ¶111. For example, *Wang* (*supra*, §II.D.2) provides a use case for

Conn's carrier substrate. As discussed in §II.D.2, *Wang* discloses a carrier chip 60' for mounting an LED chip 44. *Wang*, 3:64-67. Carrier chip 60' includes a substrate 62 adhered to lead frame 78 by metal TIM layer 79. *Id.*, 4:18-19. Substrate 62 includes multiple heat-dissipating dummy TSVs 64. Both *Conn* and *Wang* are analogous to the '826 patent because they are in the same field of endeavor as the '826 patent—semiconductor devices having via structures and methods of manufacturing them. Thompson, ¶112; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

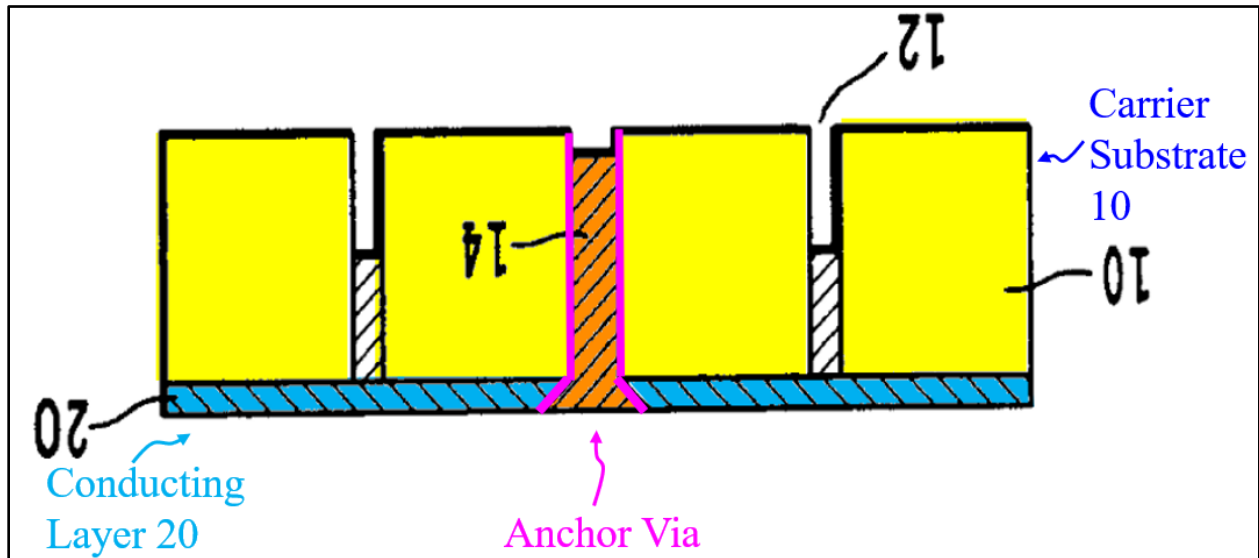


Wang, Fig. 6.

As shown below, the pair of carrier substrate 10 and conducting layer 20 in *Conn*'s Figure 1 shares the same relative positional relationship as *Wang*'s carrier substrate 60 and TIM layer 79. Compare *Conn*, Fig. 1, with *Wang*, Fig. 6.

Moreover, both *Conn* and *Wang* concern heat dissipation in electronic packages.

Conn, [0030] (using the **conducting layer** for “dissipating heat from mounted IC chips”); *Wang*, 4:36-38 (“The package component is thus suitable for being used for high-power LED devices where heat dissipation is important to optimal device operation.”). Further, both *Conn*’s **conducting layer** and *Wang*’s **TIM layer** are intended to be capable of covering the entire surface of the carrier substrate and bonding the carrier substrate to a lead frame. *Conn*, [0030]-[0031] (the **conducting layer** can cover more than 90% of the substrate surface and is not for use as signal lines); *Wang*, 4:12-15 (carrier chip 60’ is adhered to a lead frame 78 through **TIM layer 79**); *supra*, §II.C (backside metal layer was a well-known way of bonding semiconductor die to a lead frame). Additionally, *Conn* allows **metal layers** overlying the substrate. Compare *Conn*, Fig. 3 (“**conducting layer 30**”), [0037], with *Wang*, Fig. 6 (“**dummy bond pads 66A**”), 3:21-22, 3:27-33. Therefore, a POSA would have appreciated that *Conn*’s electronic package structure is suitable for use in *Wang* to mount **LED chip 44**. Thompson, ¶113. Namely, *Conn*’s carrier substrate 10 and **conducting layer 20** can serve as *Wang*’s carrier substrate 62 and **TIM layer 79**, respectively. *Id.* *Conn*’s **anchor vias** can substitute *Wang*’s **dummy TSVs 64** to achieve the dual purpose of improving *Wang*’s heat dissipation and metal layer adhesion. *Id.*



Conn, Fig. 1 (rotated by 180°).

In the *Conn-Wang* use case, *Conn*’s **conducting layer** is disposed on a side of the carrier substrate opposite to the **LED chip—active device**, thereby constituting a **backside metal layer**. *Supra*, §II.B; Thompson, ¶114. And, the **via conductors** in *Conn*’s **anchor vias** do not provide ground connection to the **LED chip**, because they are dummy vias designed for dissipating heat and securing backside metal, but *not* for providing electrical connection. *Conn*, [0011]; *Wang*, 3:23-27; *supra*, §VI.B.5; Thompson, ¶114.

Accordingly, considering the actual use cases of *Conn*’s electronic package, *Conn* renders obvious the “backside metal layer” and “not provide ground connection” limitations. Thompson, ¶115. A POSA would have had a reasonable expectation of success in implementing *Conn* with these limitations because doing

so would have simply required using *Conn* as it was intended, that is, “for mounting of semiconductor chip devices and components,” in a known way. *Id.*

2. Claim 11: recited order of the steps

As discussed in §§III.C.1 and VI.H.1, the ’826 patent does not require the steps in claim 11 to be performed in their recited order, and *Conn* anticipates each and every one of these steps. Nevertheless, to the extent that HID may (erroneously) argue that the order is required, it would have been obvious to modify the method in *Conn*’s Figure 7, to perform step 720 (i.e., claim [11b] “depositing” via metal filler) before step 710 (i.e., claim [11c] “forming” backside metal layer). Thompson, ¶116.

Specifically, *Conn* discloses that conductive layer 20 and via conductors 14 can be made “during a same step,” *Conn*, [0041], or “in separate process steps.” *Id.*, [0033]. In both options, it would have been obvious to deposit the via metal filler before forming backside metal layer. Thompson, ¶117.

First, when *Conn*’s steps 710 and 720 are combined into the same step, the order of depositing via metal filler and forming the backside metal layer is simply a design choice, and may merely depend on how the metal sputtering machine or MOCVD is programmed. *Conn*, [0055]; Thompson, ¶118. Moreover, choosing which order is a matter of convenience and does not meaningfully affect the structure of the end product. Thompson, ¶118. As illustrated by Dr. Thompson,

both orders can result in the rivet structure taught by *Conn*, so a POSA would have a reasonable expectation of success to deposit the via metal filler before forming backside metal layer. *Id.*

Second, when *Conn*'s steps 710 and 720 are performed as separate process steps, a POSA would have found it obvious to perform step 720 before step 710. Thompson, ¶119. A POSA would have been motivated to do so because depositing the via metal filler immediately after forming the vias, without being interrupted by the step of forming the backside metal layer, offers some advantages to the fabrication process. *Id.* For instance, this can minimize the time during which the via sidewall is exposed to the ambient air, thus avoiding contaminants from being introduced into the vias. *Id.* As another example, before the metal is filled into the anchor vias, intermediate layers such as an insulating liner or diffusion barrier layer may need to be formed on the via sidewall first. *Id.* In this case, it is desirable to deposit the via metal filler immediately after the intermediate layers are formed, to maximize adhesion between the metal filler and the intermediate layers. *Id.* Moreover, a POSA would have had a reasonable expectation of success in changing the sequence of steps 710 and 720. *Id.* Particularly, the modified sequence of processes is predictable because it had been used in the art before the time of the '826 patent. *Id.* For example, in the same field of endeavor as the '826 patent, *Hsu* (Ex. 1026) illustrates a process in which TSV metal filler is deposited

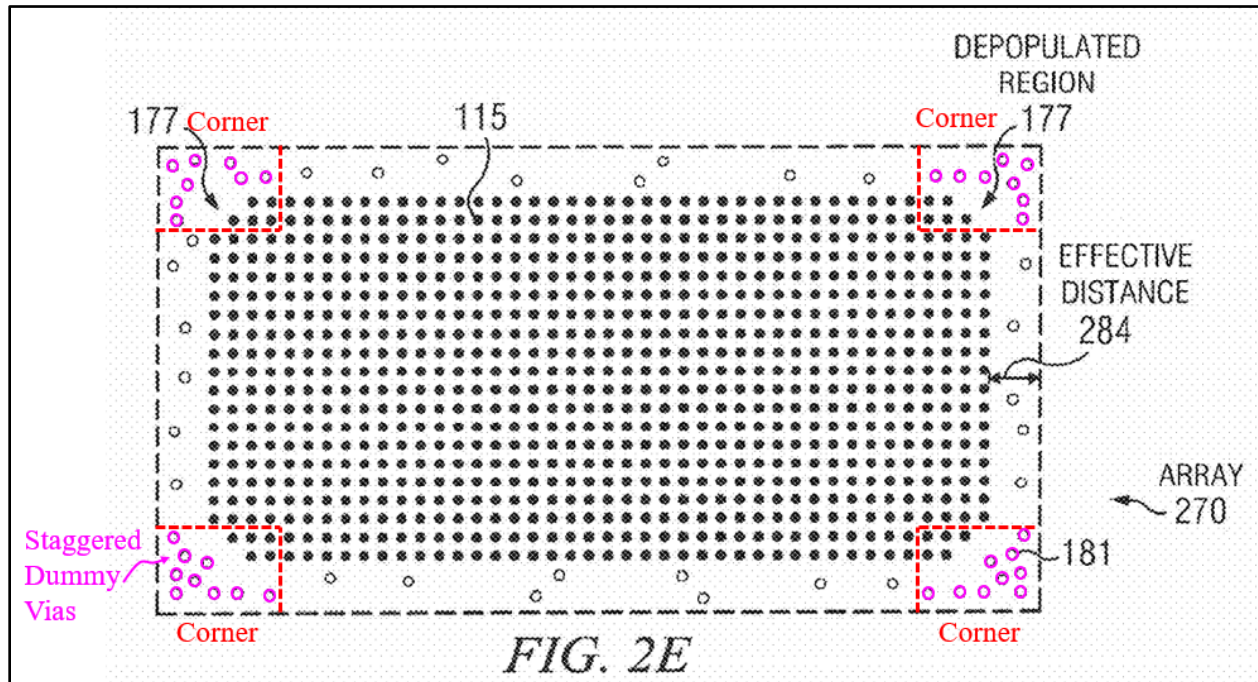
first to form a protrusion on a surface of a substrate, and then an under-bump metallurgy (UBM) layer—backside metal—is deposited on the TSV protrusion. *Hsu*, [0019], Figs. 2-3; Thompson, ¶119. Also, the modification would yield a predictable result because, as illustrated by Dr. Thompson, it would still result in the rivet structure taught by *Conn*. Thompson, ¶¶118-119.

3. Remaining limitations of claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19

Conn discloses the remaining limitations of these claims for the reasons discussed in Ground 1. *Supra*, §§VI.B–VI.I; Thompson, ¶120.

4. Claims 6, 16: “a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate”

Conn in view of a POSA’s knowledge renders obvious claims 6 and 16. Thompson, ¶¶121-125. Figure 2 of *Conn* shows that the anchor via array has a regular matrix-like pattern. *Conn*, [0035], Fig. 2. But *Conn* also discloses that “[o]ther distribution patterns and irregular distribution patterns are also permissible and may be needed to accommodate chip attachment.” *Id.* A POSA would have understood that the “irregular distribution patterns” can be a staggered distribution along a periphery of a semiconductor substrate. Thompson, ¶121. For example, *West* shows “randomly (i.e. aperiodically) positioned dummy TSVs 181” that have a staggered distribution. *West*, [0031].



West, Fig. 2E.

A POSA should have understood that such staggered pattern can be used to accommodate chip attachment. Thompson, ¶122. For example, *West* discloses the **staggered dummy vias** are used to reduce structural stresses and can “act as sacrificial stress absorbers” for electrical TSVs during assembling of TSV dies *West*, [0026]-[0027]. As another example, *Dean* (Ex. 1006) discloses that “reduc[ing] a number of the linearly aligned TSVs” can “result[] in less wafer breakage.” *Dean*, Abstract. *West* and *Dean* both pertain to semiconductor devices having via structures and methods of manufacturing them. They are thus analogous to the ’826 patent. Thompson, ¶122. Therefore, a POSA would have been motivated to arrive at the staggered pattern to prevent wafer breakage during chip attachment. *Id.*

Moreover, a POSA would have understood that the staggered pattern is structurally more stable than a linear pattern. Thompson, ¶123. By adopting a staggered pattern, the same level of securing the conducting layer to the carrier substrate can be achieved by using less anchor vias. *Id.* A POSA would have understood that using less vias is beneficial because it can reduce the stress induced by the vias. *Supra* (discussion of *West*). Therefore, a POSA would have been motivated to adopt the staggered pattern. Thompson, ¶123.

Additionally, there would have been a reasonable expectation of success for applying the staggered pattern to *Conn* because it expressly discloses that an irregular pattern, of which a POSA would understand a staggered pattern is an example, is “permissible.” *Conn*, [0035]; Thompson, ¶124.

Accordingly, *Conn* in view of a POSA’s knowledge renders obvious claim 6. Claim 16 differs from claim 6 only by reciting a step for “forming” such staggered anchor vias, and thus is obvious for the same reasons discussed for claims 11 and 6. Thompson, ¶125.

B. Ground 2B: *Conn* in View of Knowledge of POSA and AAPA Renders Obvious Claims 8, 18

1. Claim 8

The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

AAPA discloses the three-layer backside metal stack in claim 8 had been used as a conventional method of adhering a backside metal layer to a substrate. '826 patent, 1:24-30. A POSA would have appreciated *Conn*'s anchor vias and AAPA's three-layer stack are complimentary solutions, and thus been motivated to harvest their respective benefits for improving the backside metal adhesion. *See supra*, §II.E (*Burnham* combines TSVs and an intermediate oxide layer to improve backside metal adhesion); Thompson, ¶¶126-127.

Particularly, *Conn* addresses the metal adhesion problem during usage of a packaged chip. *Conn*, [0005]. A POSA would have understood that using a large number or density of *Conn*'s anchor vias in the substrate may have certain drawbacks. *Supra*, §VII.A.4 (discussing teachings of *West* and *Dean*); Thompson, ¶127. A POSA thus would have appreciated the need to balance the anchor vias' benefit in securing conductive layers to the substrate against their potential adverse effect to the chip packaging reliability. Thompson, ¶127. To that end, a POSA would have been motivated to "increase the anchor vias' "spacing ... [to] reduce[] stress," (*West*, [0006]), while using AAPA's three-layer backside metal stack to

supplement the adhesion. Thompson, ¶127. Although AAPA discloses that the three-layer stack is not capable of completely preventing the backside metal layer peeling from the semiconductor substrate during fabrication of the chip, (’826 patent, 1:30-38), this problem can be cured by placing *Conn*’s anchor vias only at certain strategic locations, such as “near the edges and/or corners of the die” where the backside metal is easy to peel off. ’826 patent, 1:30-33; Thompson, ¶127. As such, combining *Conn* and AAPA would yield a solution that ensures backside metal adhesion at both the fabrication and usage stages of the chip, while free of the respective potential drawbacks of the anchor vias and three-layer backside metal stack. Thompson, ¶127.

The above-proposed combination is predictable because it only requires combining the known elements from the prior art—*Conn*’s anchor vias and AAPA’s three-layer stack of backside metal—without modification to each element’s structure or manufacturing process. Thompson, ¶128. As discussed in §§II.C (*Cronin*) and II.E (*Sharma*), the multi-layer backside metal stack was a mature technique dating back to the 1980s. A POSA would have thus had a reasonable expectation of success in adding AAPA’s three-layer stack to *Conn*, which would result in the claimed combination. Thompson, ¶128.

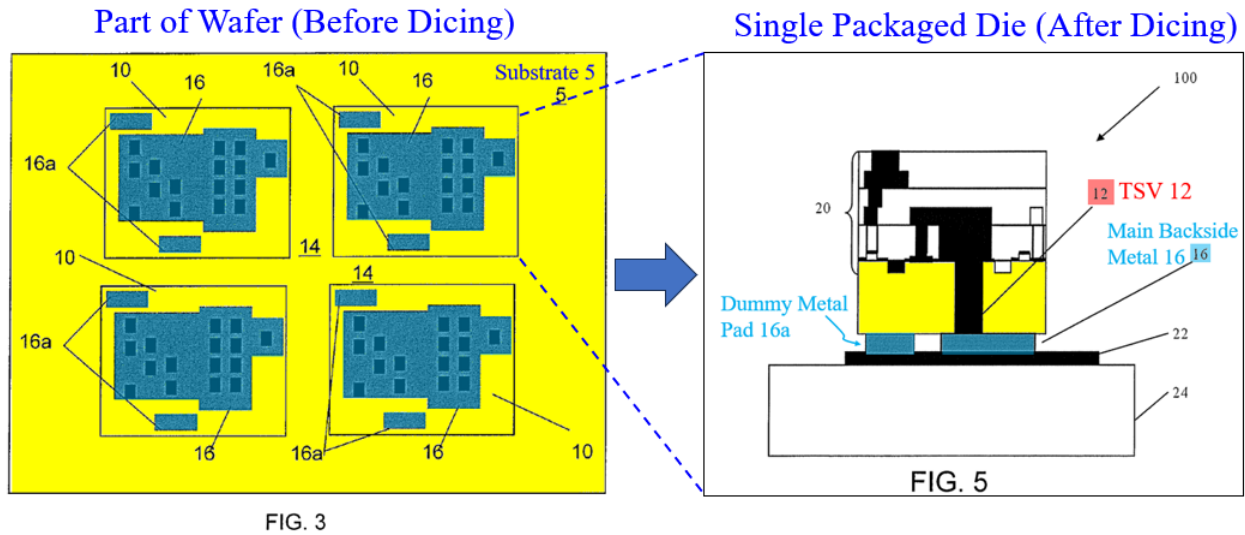
2. Claim 18

Claim 18 differs from claim 8 only by reciting steps for “forming” the three-layer backside metal stack, and thus would have been obvious for the same reasons discussed for claims 11 and 8. Thompson, ¶129.

VIII. Ground Set 3: *Gambino*-Based Obviousness

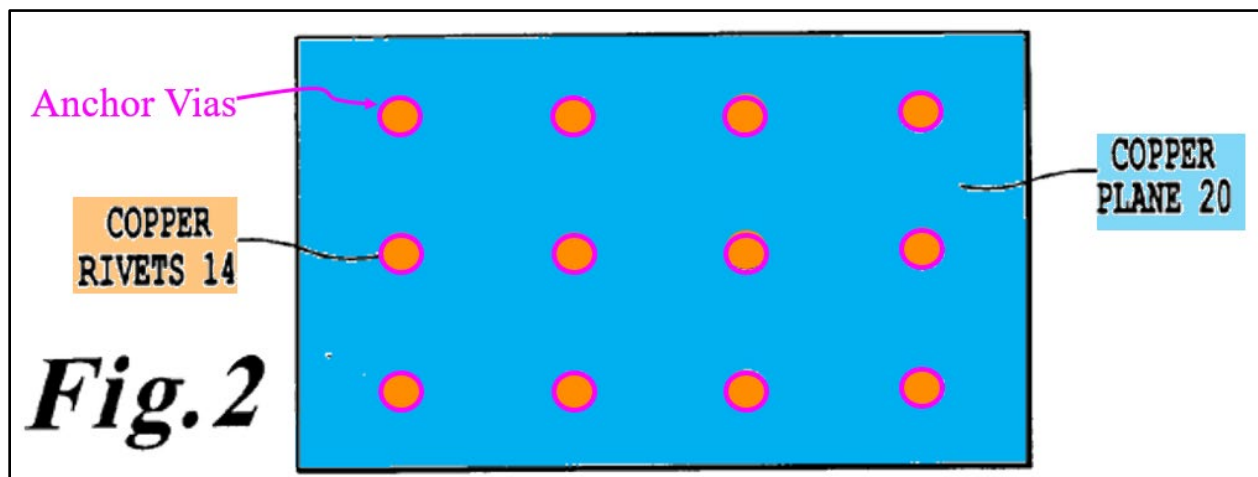
A. Overview of the *Gambino* Combinations

Gambino discloses that a backside metal layer can be formed on a wafer to provide ground connections to TSVs, but it is prone to peeling from the semiconductor substrate during the dicing process when the wafer is cut into individual dies. *Gambino*, [0016]. As shown below, to address this problem, *Gambino* proposes patterning the backside metal layer to avoid the dicing channels 14 and cover only selected locations in each die 10. *Id.*, [0015], [0017], [0023]-[0027]. Consequently, the resulting die (Figure 5, after dicing) includes a main backside metal 16 covering an area having TSVs 12, and dummy metal pads 16a “at strategic locations on the dies 10 to provide mechanical support,” “such that the die 10 will sit flatly on the package substrate, during packaging.” *Id.*, [0027]-[0028].



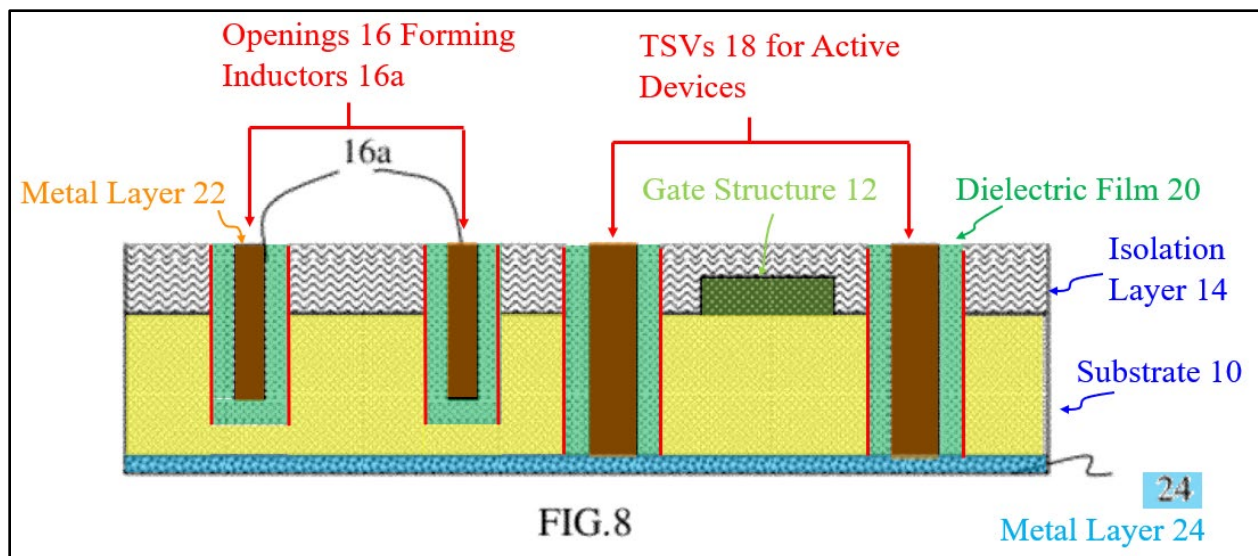
Gambino, Figs. 3 and 5.

Conn, as discussed in §VI.A, discloses using **anchor vias** to secure a **metal layer** to a semiconductor substrate surface. *Conn*, Abstract, [0028], [0035].



Conn, Fig. 2.

Ding proposes utilizing TSV processing to manufacture high-Q value inductors to reduce cost.¹⁰ *Ding*, [0003], [0015]. Figure 8 shows that openings 16 and traditional TSVs 18 are created using the same TSV processing technique. *Id.*, [0016], [0018]-[0019], [0021]-[0025]. TSVs 18 are used for connecting active devices like gate structure 12, while openings 16 are used to make inductors, a type of passive device. *Id.*, [0002], [0015], [0024].



Ding, Fig. 8.

Gambino, *Conn*, and *Ding* are all analogous to the '826 patent because they are in the same field of endeavor as the '826 patent—semiconductor devices having via structures and methods of manufacturing them. Thompson, ¶¶130-133.

¹⁰ “High-Q” standards for high quality, meaning the inductor has low power loss and is suitable for high-frequency applications. *Ding*, [0003]; Thompson, n.7.

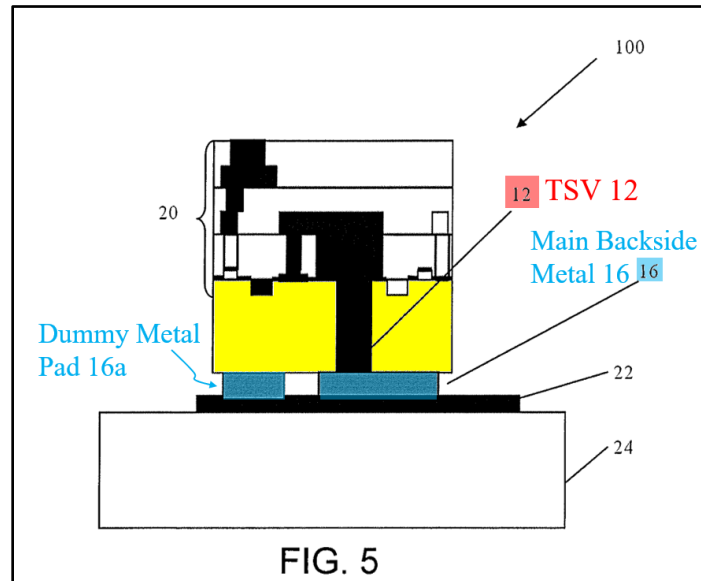
B. Ground 3A: *Gambino* in View of *Conn* Renders Obvious Claims 1, 2, 4-7, 11, 12, 14-17

1. Rationale for combining *Gambino* with *Conn*

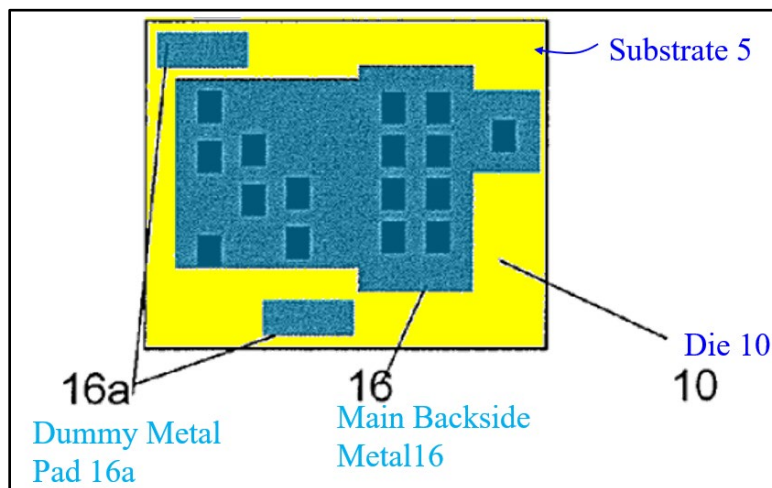
a. Proposed combination

Figure 5 of *Gambino* “shows a packaged module with a backside metal ground plane attached to a substrate[.]” *Gambino*, [0013], [0030]. The packaged module is based on a die generated after dicing a wafer. *Id.*, [0005], [0017]; Thompson, ¶134. The package module includes TSVs 12 “in electrical communication with” wiring layers 20, which include “active or passive devices.”¹¹ *Gambino*, [0030]. Figure 3 (excerpted) shows the module’s backside metal ground plane includes a main backside metal 16 covering the electrical TSVs, and one or more dummy metal pads 16a located at the corners and peripheries of the substrate “to provide mechanical support” to the module. *Id.*, [0027]-[0028].

¹¹ TSVs 12 in *Gambino* will be referred to as electrical TSVs hereafter.

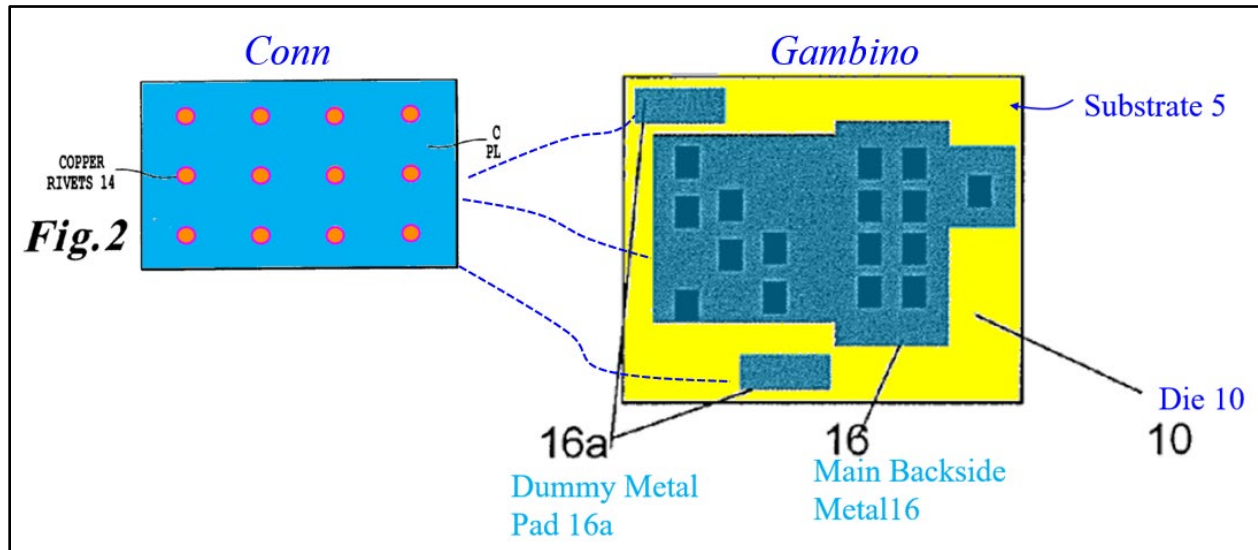


Gambino, Fig. 5.



Gambino, Fig. 3 (excerpted).

As shown below, a POSA would have found it obvious to apply *Conn*'s teachings to create **anchor vias** in *Gambino*'s **dummy metal pads 16a** and/or **main backside metal 16**, to secure **them** to the substrate and prevent delamination during singulation. Thompson, ¶135.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

b. A POSA would have been motivated to combine *Gambino* and *Conn*

A POSA would have been motivated to combine the teachings of *Gambino* and *Conn* at least because both references are directed to improving structural integrity of packaged devices. *Gambino*, [0001] (“improved metal adhesion”), [0017] (“reducing the overall cost of the packaged module”); *Conn*, [0011] (“an electronic package includes a carrier substrate” and “to secure the [] conducting layer to the carrier substrate”); Thompson, ¶136. Since *Gambino* and *Conn* address the same problem (metal adhesion to substrate) in semiconductor packaging, a POSA would have considered them to be closely related and would have consulted both references’ teachings. Thompson, ¶136.

Moreover, a POSA would have found it desirable to combine the advantages proffered by *Gambino* and *Conn*. Thompson, ¶137. These two references tackle

metal adhesion problems occurring at different stages. *Id.* *Gambino* concerns the backside metal peeling problem during dicing (i.e., at the manufacturing stage), while *Conn* addresses the metal delamination issue due to thermal fatigue during the usage of the package device. *Gambino*, [0016]; *Conn*, [0005]. It is thus attractive to combine *Gambino* and *Conn* to offer a metal adhesion solution covering the entire life cycle of a semiconductor device, from its manufacturing to usage. Thompson, ¶137. Particularly, in view of *Conn*'s teachings, a POSA would understand that the dummy metal pads 16a and main backside metal 16 in *Gambino*'s packaged module have a high chance to delaminate from the substrate when the module is used in a computing device. *Conn*, [0005]-[0008]. Therefore, there would have been a desire to improve *Gambino* by adding *Conn*'s anchor vias at dummy metal pads 16a and main backside metal 16, to ensure they remain secured to the substrate during the module's useful life. Thompson, ¶137.

Additionally, despite *Gambino*'s solution being able to “solve[] the metal peeling problem” during dicing, (*Gambino*, [0017]), a POSA would have understood that *Gambino*'s dummy metal pads 16a located at the corners and peripheries of the die are the most vulnerable during the dicing process.

Thompson, ¶138. Yet, dummy metal pads 16a are “at strategic locations on the dies” and indispensable to the module's structural “stability.” *Gambino*, [0028].

Therefore, a POSA would have wanted to use *Conn*'s anchor vias at dummy metal

pads 16a to reinforce their adhesion, to provide a fail-safe or error-proof measure.

Thompson, ¶138. This is important to ensuring the “die yield and reliability.”

Gambino, [0016]; Thompson, ¶138.

Moreover, *Gambino* is ready for improvement because it already uses electrical TSVs and employs a TSV manufacturing process. *Gambino*, [0020];

Thompson, ¶139. The anchor vias could be made using the same process.

Thompson, ¶139.

Further, *Gambino* and *Conn* attack the backside metal adhesion problem from two different angles. Thompson, ¶140. *Gambino* patterns the backside metal, while *Conn* uses anchor vias. *Gambino*, [0015] (“patterned backside metal ground planes for improved metal adhesion”); *Conn*, [0030] (“the anchor via maintain the utility of the carrier substrate laminate to continue to dissipate heat and be a viable support”). A POSA would have been interested in combining these two techniques to maximize the backside metal adhesion. Thompson, ¶140.

c. The combination of *Gambino* and *Conn* would have yielded a predictable result

First, the structure of the resulting combination is predictable because it merely requires a simple incorporation of *Conn*’s anchor vias to *Gambino*’s substrate, and does not require any modification to *Gambino*’s overall die structure. Thompson, ¶141. Particularly, since the anchor vias are only formed at the backside of the substrate, they do not require redistribution of the active

devices and wiring layers on the front side of the substrate. *Id.* Moreover, *Gambino*'s **dummy metal pads 16a** are located at the corners and peripheries of the substrate, which are less crowded areas that are not usually for planting active/passive devices, so adding the **anchor vias** here would not affect other elements in the devices. *Id.*

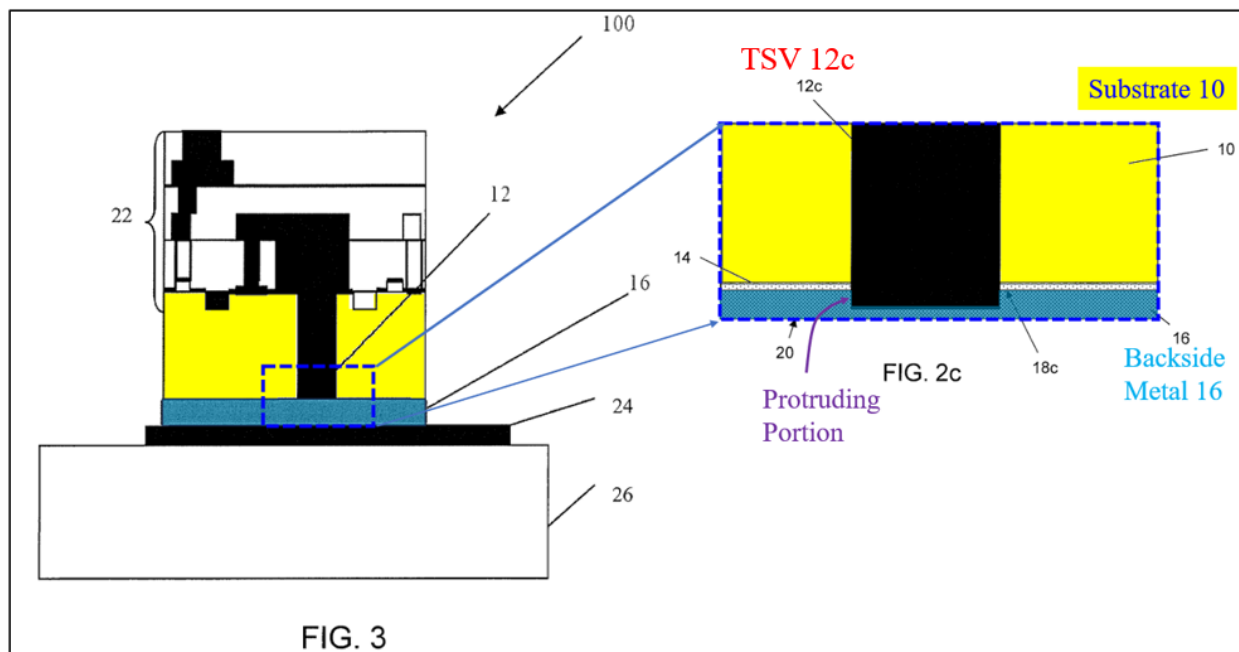
Second, the process of making the proposed combination is predictable because the same process used for manufacturing *Gambino*'s **electrical TSVs** can be used to manufacture the **anchor vias**. Thompson, ¶142. As illustrated by Dr. Thompson, *Gambino*'s method can yield the same rivet-like **anchor via** structure contemplated by *Conn*—the resulting **via conductors** will form **protruding portions** bonded to the **backside metal**. *Id.* Thus, the proposed combination does not require modification to *Gambino*'s existing manufacturing method. *Id.*

Third, the function of the resulting combination is predictable because the introduction of *Conn*'s **anchor vias** to *Gambino* will not affect the packaged module's electrical functions. Thompson, ¶143. The **anchor vias** themselves do not need to be connected to active or passive devices. *Supra*, §VI.B.5. *Gambino*'s **dummy metal pads 16a** also do not serve electrical functions. Thus, the **anchor vias**' presence will not change these devices' functioning. Thompson, ¶143.

Fourth, there would have been a reasonable expectation of success for the resulting combination because *Conn* discloses the **anchor vias** can secure

conducting layers with sizes ranging from 10% to 100% of the substrate's total surface area. *Conn*, [0030]-[0031]. *Gambino*'s patterned dummy metal pads 16a and main backside metal 16 have sizes in this range, and thus can be securely held by the anchor vias. Thompson, ¶144.

Fifth, the proposed combination was well-known. Thompson, ¶145. For example, *Burnham* had already used via structures with protrusion portions to improve backside layer adhesion. *Supra*, §II.E. A POSA would have appreciated that the proposed combination is simply replicating prior art and would have succeeded. Thompson, ¶145.

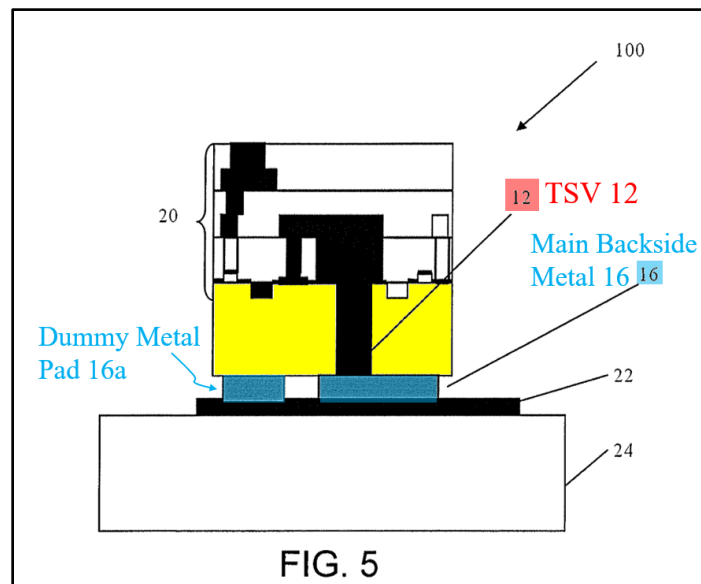


Burnham, Figs. 2c and 3.

2. Independent Claim 1

a. [1pre]

Gambino/Conn discloses a structure by disclosing a packaged semiconductor device module as shown in *Gambino*'s Figure 5. *Gambino*, [0030]; Thompson, ¶146.

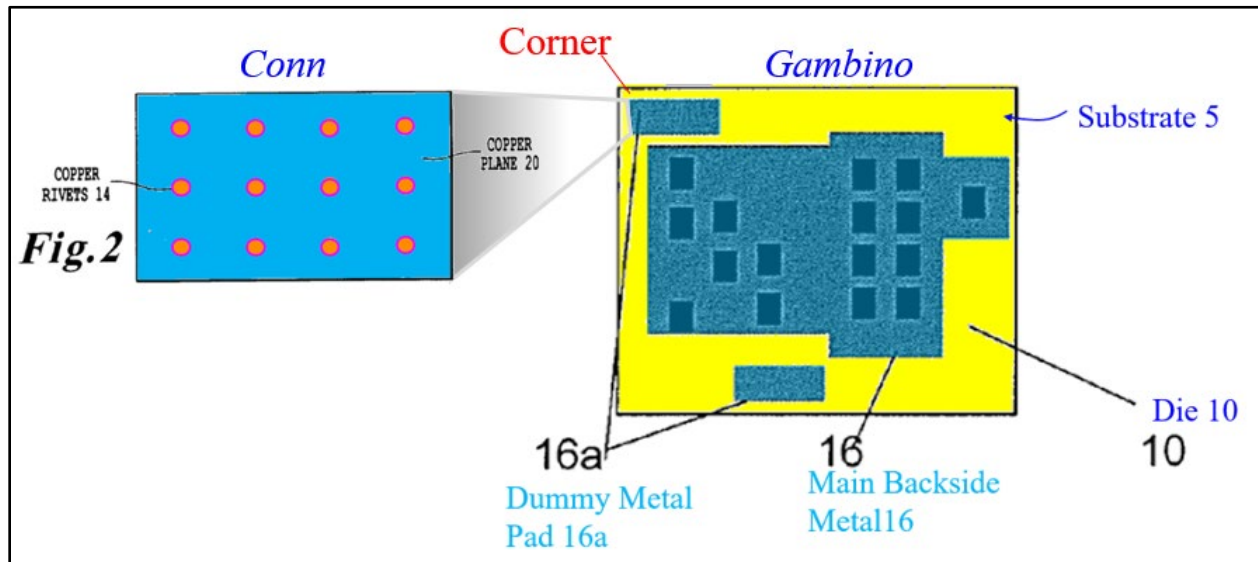


Gambino, Fig. 5.

b. [1a]

Gambino/Conn satisfies [1a] by disclosing dummy metal pad 16a is located in at least one corner of the substrate “to provide mechanical support.” *Gambino*, [0028]; *Gambino*, [0019], [0027], [0030]; Thompson, ¶147. *Gambino* discloses dummy metal pads 16a are placed “at strategic locations” to provide “stability on the backside of the die 10,” “such that the die 10 will sit flatly on the package substrate[.]” *Gambino*, [0028]. The corner is one of these strategic locations.

Thompson, ¶147. Therefore, *Gambino/Conn*'s anchor vias at the corner-located dummy metal pad(s) 16a meet claim [1a]. *Id.*

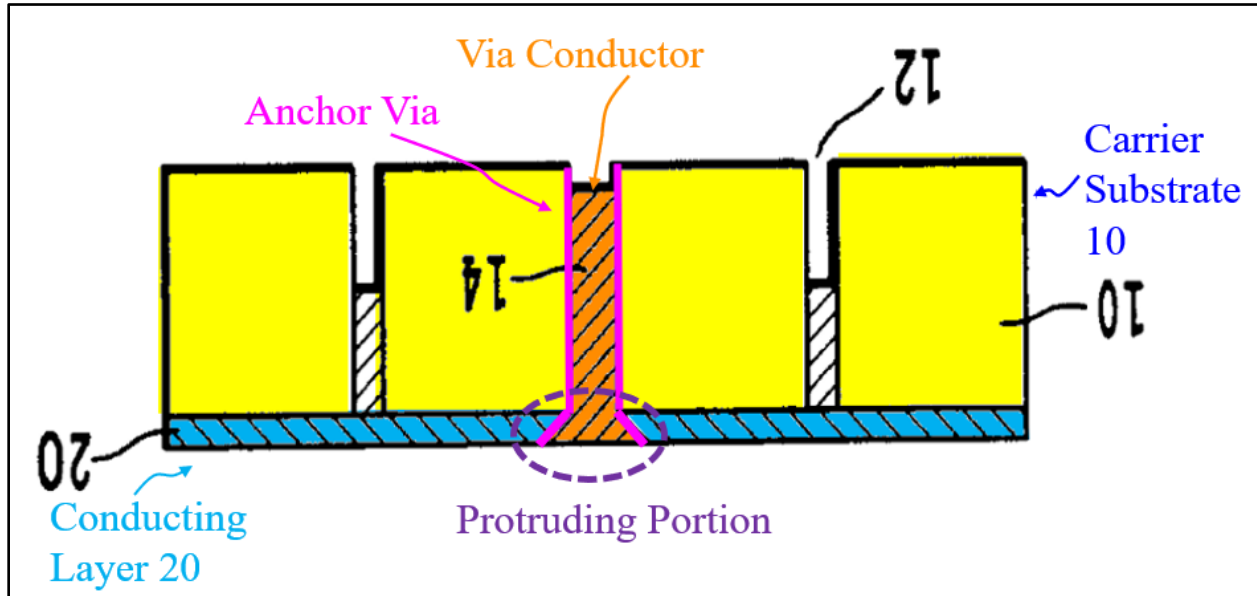


Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

c. [1b]

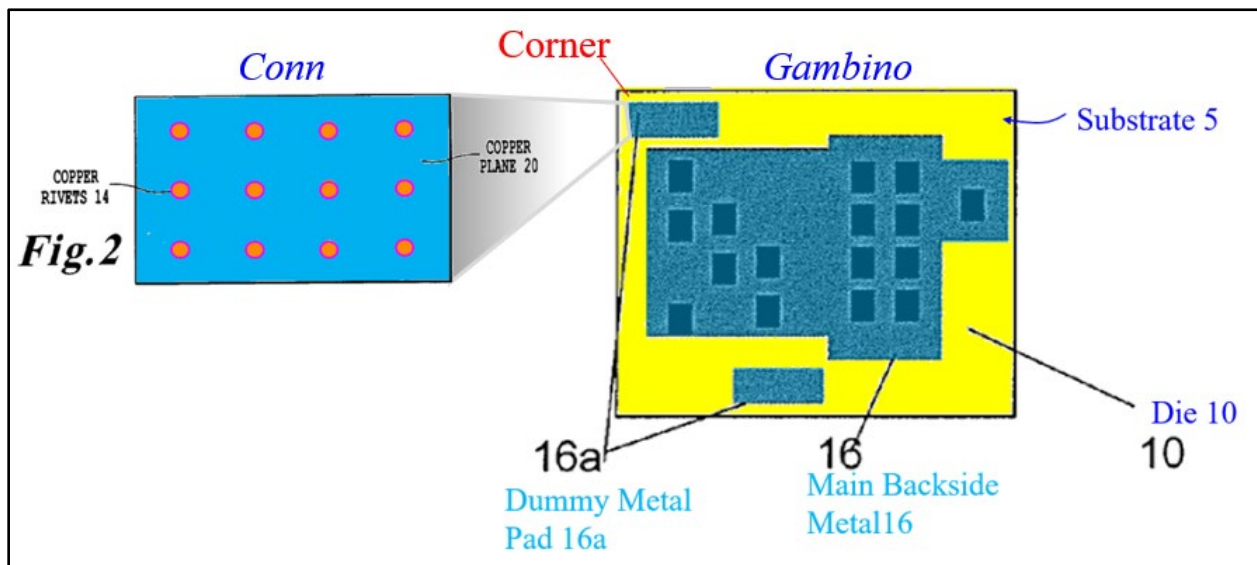
Gambino/Conn satisfies [1b] because *Conn* discloses the via conductors in the anchor vias form protruding portions that are connected to a conducting layer.

Supra, §VI.B.3; Thompson, ¶148.



Conn, Fig. 1 (rotated by 180°).

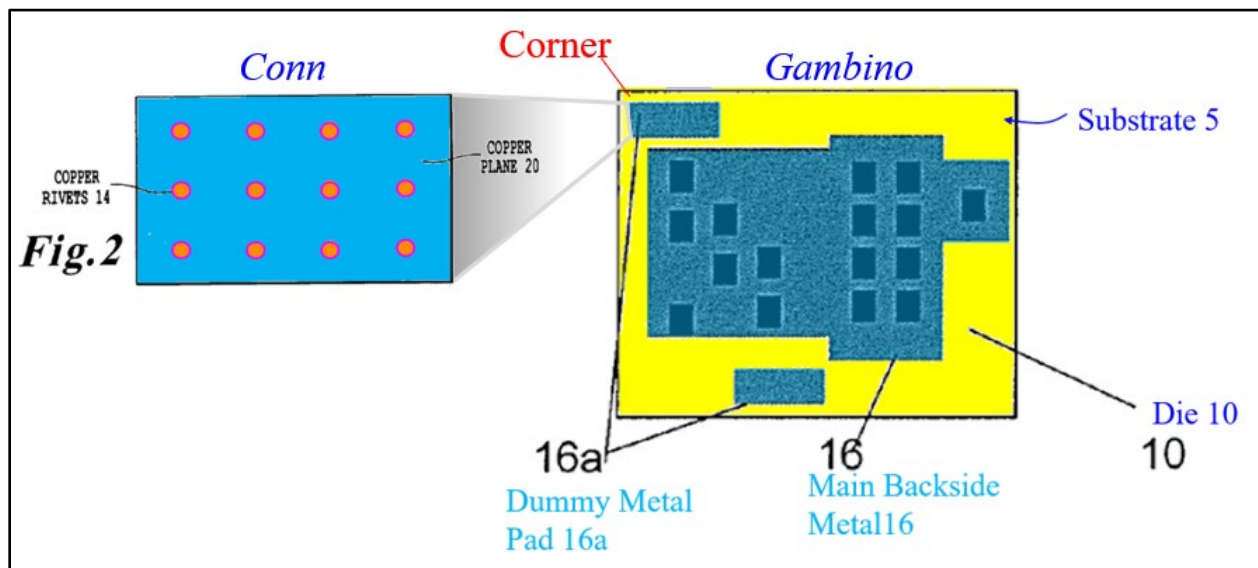
Applying *Conn*'s teachings to *Gambino*, a POSA would understand that the anchor vias in *Gambino/Conn* have via conductors forming protruding portions connected to corner-located dummy metal pad(s) 16a. Thompson, ¶149.



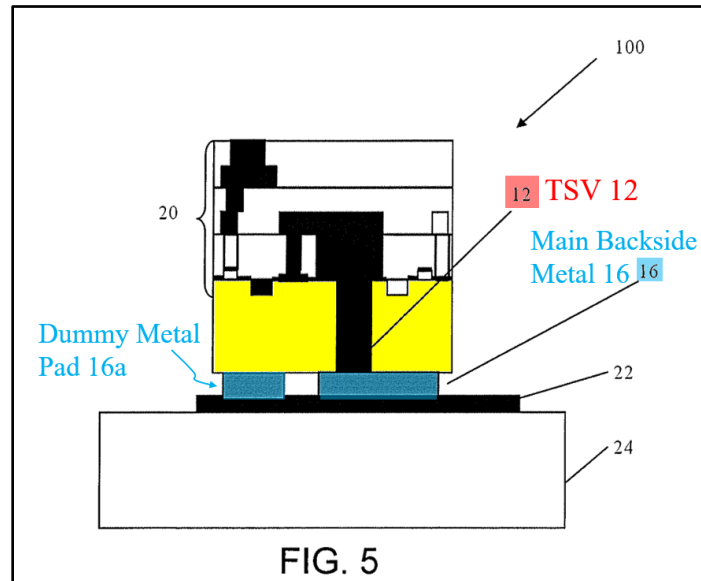
Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

d. [1c]

Gambino/Conn satisfies [1c] because corner-located dummy metal pad(s) 16a is the claimed “backside metal layer.” Thompson, ¶150. Moreover, applying *Conn*’s teachings regarding the anchor vias, a POSA would understand the protruding portions are “bonded to” corner-located dummy metal pad(s) 16a. *Supra*, §VI.B.4; Thompson, ¶150.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Gambino, Fig. 5.

e. [1d]

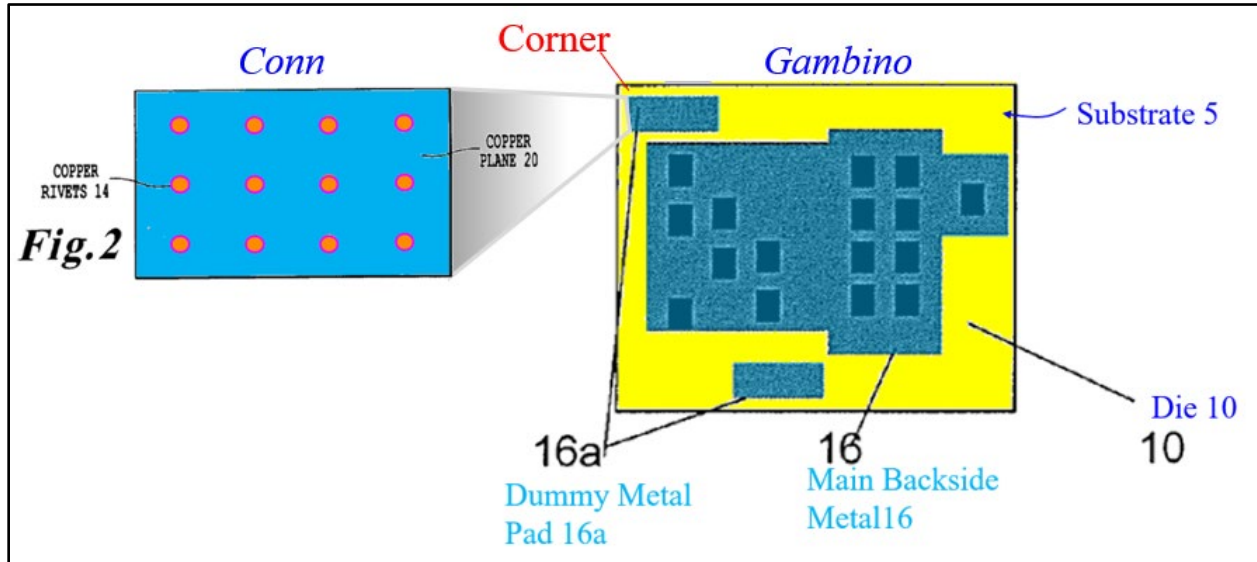
Gambino/Conn satisfies [1d] because corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection, which means the anchor vias therein do not provide ground connection to active devices.

Gambino, [0028], [0030]; Thompson, ¶151.

3. Claims 2, 4-7

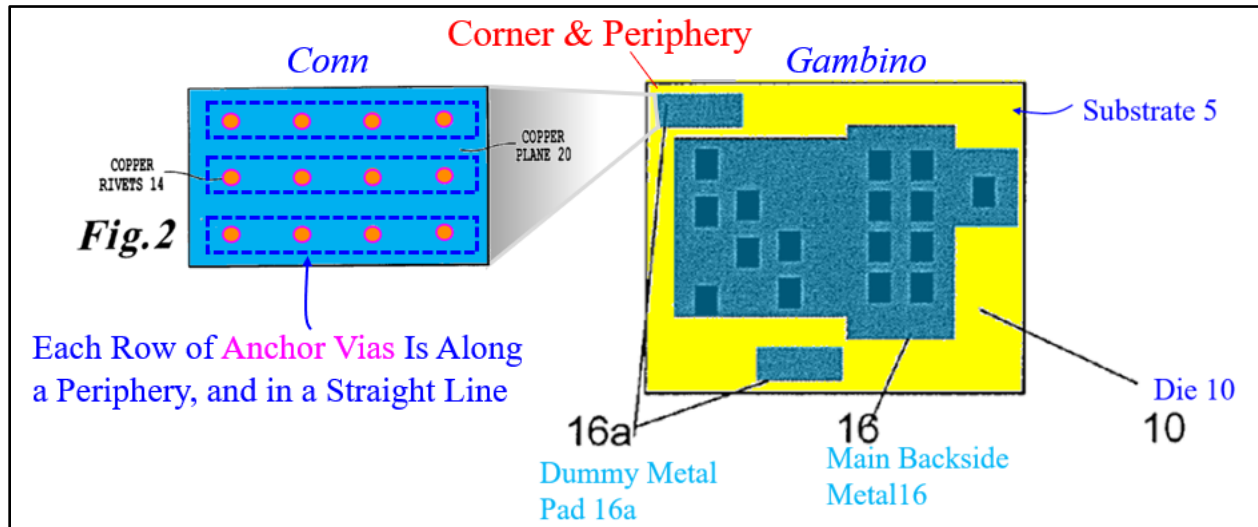
a. *Gambino/Conn*’s teachings

Claim 2 recites the at least one corner anchor via “comprises a cluster of anchor vias.” ’826 patent, 8:4-5. *Gambino/Conn* meets it because *Conn* discloses a pattern of anchor vias (i.e., “a cluster of anchor vias”) is formed at corner-located dummy metal pad(s) 16a. *Conn*, [0035]-[0036]; *supra*, §VI.C; Thompson, ¶152.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

Claim 4 recites a plurality of **corner anchor vias** “disposed in a straight line along a **periphery** of said semiconductor substrate.” ’826 patent, 8:10-12. As illustrated below, *Gambino/Conn* meets it because *Gambino*’s **corner**-located **dummy metal pad(s) 16a** is located at a **periphery** of the substrate and *Conn* discloses the **anchor vias** therein can have a regular pattern (*Conn*, Fig. 2), in which each row of the **anchor vias** is disposed in a straight line along a periphery. *Conn*, [0035]-[0036], Fig. 2; *see supra*, §VI.D; Thompson, ¶153.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

Claim 5 recites the peripheral **anchor vias** in claim 4 have a linear density “less than approximately 10%.” ’826 patent, 8:13-16. *Gambino/Conn* meets it because *Conn* discloses the **anchor via** pattern at the periphery **corner**-located **dummy metal pad(s) 16a** has a linear density meeting this requirement. *Supra*, §VI.E; Thompson, ¶154.

Claim 6 recites a plurality of **corner anchor vias** are “disposed in a staggered configuration along a **periphery** of said semiconductor substrate.” ’826 patent, 8:17-20. *Gambino/Conn* meets it because *Gambino*’s **corner**-located **dummy metal pad(s) 16a** is located at a **periphery** of the substrate and *Conn* renders obvious the **anchor vias** therein being staggered. *Conn*, [0035]; *supra*, §VII.A.4; Thompson, ¶155.

Claim 7 recites the **corner anchor vias** have a total area “less than approximately 0.5% of a total area of said semiconductor substrate.” ’826 patent, 8:21-23. *Gambino/Conn* meets it because *Conn* discloses the **anchor via** pattern at the **corner**-located **dummy metal pad(s) 16a** has a total area meeting this requirement. *Supra*, §VI.F; Thompson, ¶156.

b. Rationale for obviousness

In addition to the reasons provided in §VIII.B.1, a POSA would have been motivated to apply *Conn*’s teachings regarding the patterns, linear densities, and total areas of the **anchor vias** because they are suitable for achieving *Conn*’s stated purpose of securing backside metal and preventing delamination. *Conn*, Abstract, [0011], [0030], [0035]-[0036]; Thompson, ¶157.

A POSA would also have a reasonable expectation of doing so. First, since *Gambino*’s **corner**-located **dummy metal pad(s) 16a** does not provide electrical connection, applying *Conn*’s teachings would have no effect on the electrical functions of the chip. Thompson, ¶158. Second, both *Gambino* and *Conn* teach using Bosch deep reactive ion etching (DRIE) to form the vias. *Gambino*, [0020]; *Conn*, [0049], [0055]. Thus, a POSA would have reasonably expected that the same process used for creating *Gambino*’s TSVs can also be used to create the **anchor vias**, with the patterns, linear densities, and total areas specified by *Conn*. Thompson, ¶158. Third, *Conn*’s **anchor vias** and *Gambino*’s TSVs share similar

parameters. *Gambino*, [0020] (“TSVs with almost any diameter, from the submicrometer level to hundreds of micrometers”); *Conn*, [0035] (“The vias 12 can have a diameter between 30 and 150 μm .”). Thus, the sizes of *Conn*’s anchor vias fit for *Gambino*’s packaged module. Thompson, ¶158.

4. Independent Claim 11

a. “Forming,” “depositing,” and “forming” steps

Gambino/Conn discloses the claimed method because *Gambino* discloses the claimed [11a] “forming at least one anchor via,” [11b] “depositing a metal filler,” and [11c] “forming a backside metal layer,” by disclosing:

- “a via can be formed in a front side of the die 10 using conventional lithography and etching processes” (*Gambino*, [0020]);
- “[a]fter formation of the via, metal can be deposited therein using conventional deposition processes such as, for example, electroplating or chemical vapor deposition techniques” (*id.*); and
- “a backside metal 16 is formed on the backside of the die 10, in contact with the TSVs 12” (*id.*, [0021]).

Thompson, ¶159.

Although *Gambino* describes the above method as being used to make the electrical TSVs, a POSA would have been motivated to use it to also manufacture the anchor vias. Thompson, ¶160. Doing so would form the electrical TSVs and

anchor vias using the same process, thereby simplifying the manufacturing and minimizing the cost, and a POSA would have thus had a reasonable expectation of success in doing so. *Id.* Moreover, as discussed in §VIII.B.1.c, *Gambino*'s method would yield the same **anchor via** structure contemplated by *Conn*. Thompson, ¶160.

b. Remaining limitations of claim 11

The remaining features of claim 11 are similar to those in claim 1 and taught by *Gambino* and *Conn* for the same reasons in §§VIII.B.2.b–VIII.B.2.e. Thompson, ¶161.

5. Claims 12, 14-17

Claims 12 and 14-17 are taught by *Gambino* and *Conn* for the reasons discussed for claims 11, 2, and 4-7. Thompson, ¶¶162-166.

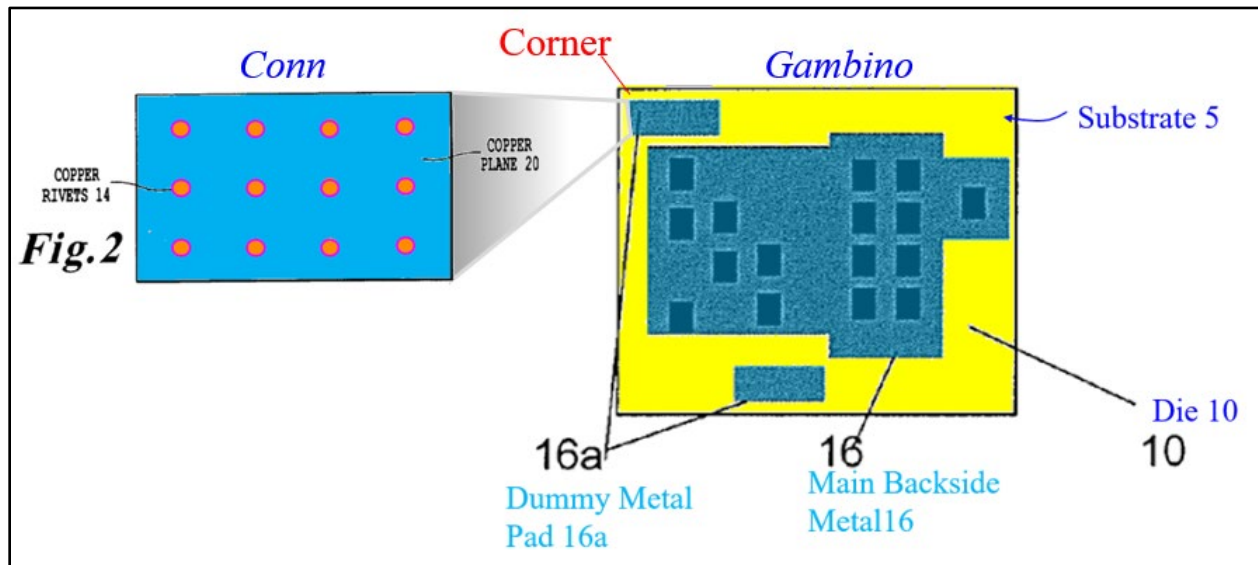
C. Ground 3B: *Gambino* in View of *Conn* and *Ding* Renders Obvious Claims 10, 20

1. Rationale for combining *Gambino/Conn* with *Ding*

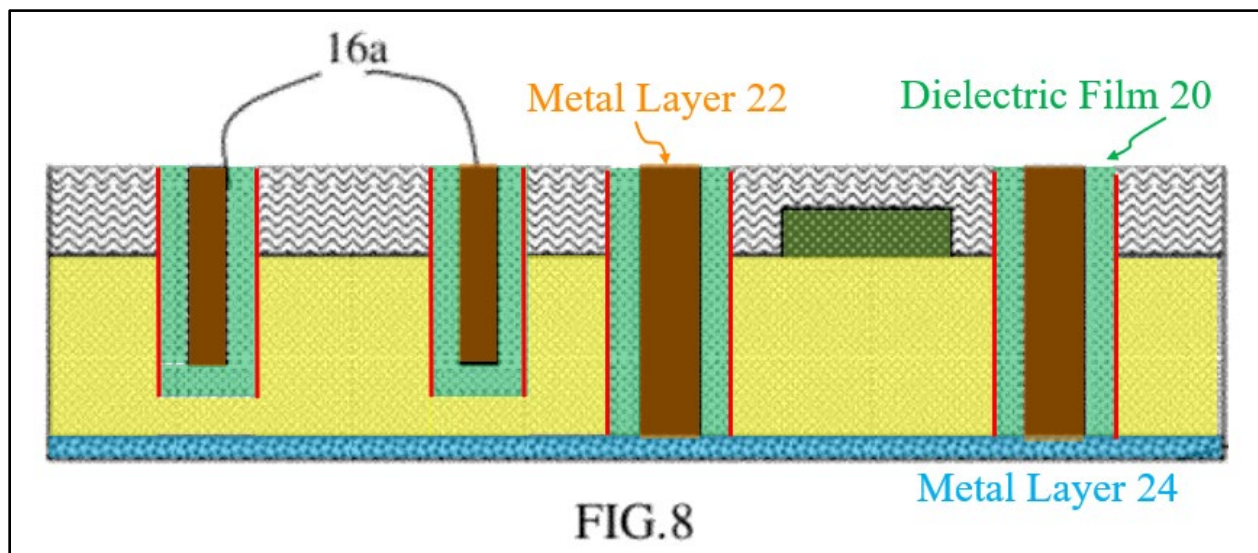
a. Proposed combination

Gambino/Conn discloses its packaged module can be used as “RF analog chips,” and contains “a host of different active or passive devices.” *Gambino*, [0002], [0030]. Inductors are typical passive devices used in RF analog chips. *Ding*, [0015]; Thompson, ¶167. *Ding* proposes using TSV-forming process to make inductors in RF chips. *Ding*, [0015]. A POSA would have been prompted by

Ding's teachings to modify *Gambino/Conn*'s method of forming electrical TSVs and anchor vias, to add a step of forming a dielectric film on the TSVs/anchor-vias, such that the modified method can be used to simultaneously make *Ding*'s high-quality inductor. Thompson, ¶167.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Ding, Fig. 8.

**b. A POSA would have been motivated to combine
Gambino/Conn with *Ding***

Using the same process to manufacture all the above components in an RF chip simplifies fabrication and reduces cost. Thompson, ¶168. Particularly, both *Gambino* and *Ding* aim to improve RF chip function/manufacturing in an inexpensive way. *Gambino*, [0016] (“the peeled metal ... can cause problems with die yield and reliability”), [0017] (“a less expensive dicing process can be used, thereby reducing the overall cost of the packaged module”); *Ding*, [0003] (“there remains a need for high quality factor inductor formation with an inexpensive method”), [0015] (“[t]his significantly reduces the costs”). A POSA would have been motivated to combine their teachings to maximize the benefits. Thompson, ¶168.

Moreover, *Gambino/Conn* would have led a POSA to combine it with *Ding*. Thompson, ¶169. *Gambino* discloses its packaged module includes “passive devices,” and can be “RF analog chips” that use passive devices like inductors. *Gambino*, [0002], [0030]. And *Conn* discloses its carrier substrate may be formed with “[p]assive components (as capacitors, resistors, and inductors),” suggesting its electronic package is suitable for RF applications. *Conn*, [0026]. Thus, *Gambino/Conn* would have prompted a POSA to adopt *Ding*’s teaching about making high-quality inductors. Thompson, ¶169.

Further, *Gambino/Conn* already includes **electrical TSVs** and **anchor vias**, so a POSA would have been attracted by *Ding*'s proposal of using the **TSV/anchor-via** processing to manufacture the high-quality inductors. *Ding*, [0015]; Thompson, ¶170. This means that the manufacturing process can be greatly simplified for RF chips. Thompson, ¶170. Additionally, a POSA would have appreciated that using *Ding*'s **dielectric film** would reduce signal interference between the **electrical TSVs** (providing power and input/output for active devices) and the inductors (passive devices), so making the combination would result in better RF chips. *Id.*

c. The combination of *Gambino/Conn* with *Ding* would have yielded a predictable result

Gambino/Conn's and *Ding*'s via-forming methods use the same steps: forming vias at the front side; depositing metal filler in the vias; and forming backside metal. *Compare Gambino*, [0020]-[0021], with *Ding*, [0019]-[0025], Figs. 3-8; Thompson, ¶171. Thus, the proposed combination does not require any change to *Gambino/Conn*'s existing way of forming the **TSVs/anchor-vias** and **backside metal**. Rather, it only requires adding an additional step of depositing the **dielectric film**, before the metal filler is deposited into the vias. This is a simple modification, and a POSA would have had a reasonable expectation of success in it. Thompson, ¶171.

The modification to *Gambino/Conn*'s via-forming method would yield a predictable result—a **dielectric film** would be formed on the sidewall of the

electrical TSVs and anchor vias. Thompson, ¶172. As discussed in §VIII.C.1.b, such dielectric film would reduce signal interference and yield better-functioning RF chips. Thompson, ¶172.

2. Claims 10, 20: “an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via”

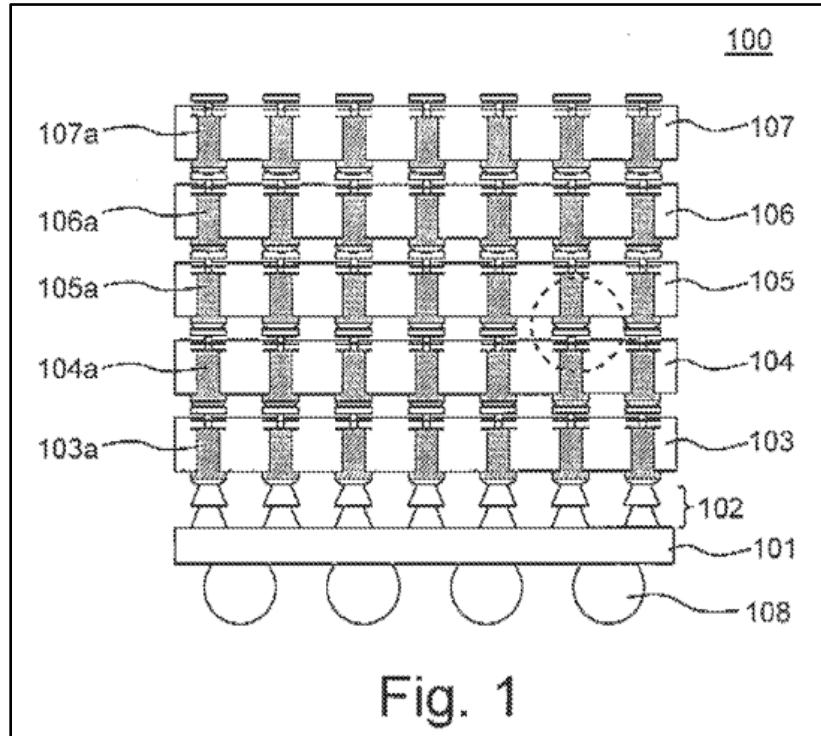
The *Gambino/Conn/Ding* combination discloses this limitation because *Gambino/Conn*’s via-forming method, as modified by *Ding*, would result in a dielectric film formed in the electrical TSVs and anchor vias. *Supra*, §VIII.C.1.a; *Ding*, [0021]-[0023], Fig. 4 and 8; Thompson, ¶173.

IX. Ground 4: *Torii* Anticipates Claims 1, 8-11, 18-20

A. Independent Claim 1

1. [1pre]

Torii discloses [1pre] by disclosing a semiconductor chip. *Torii*, [0002], [0031], [0045], [0040], Figs. 3, 46; Thompson, ¶¶174-176. Multiple of such semiconductor chips, e.g., 103–107 in Figure 1, can be stacked along a vertical direction to form a semiconductor device 100 (e.g., a memory). *Torii*, Abstract, [0004], [0006]-[0008], Fig. 1.

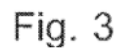


Torii, Fig. 1.

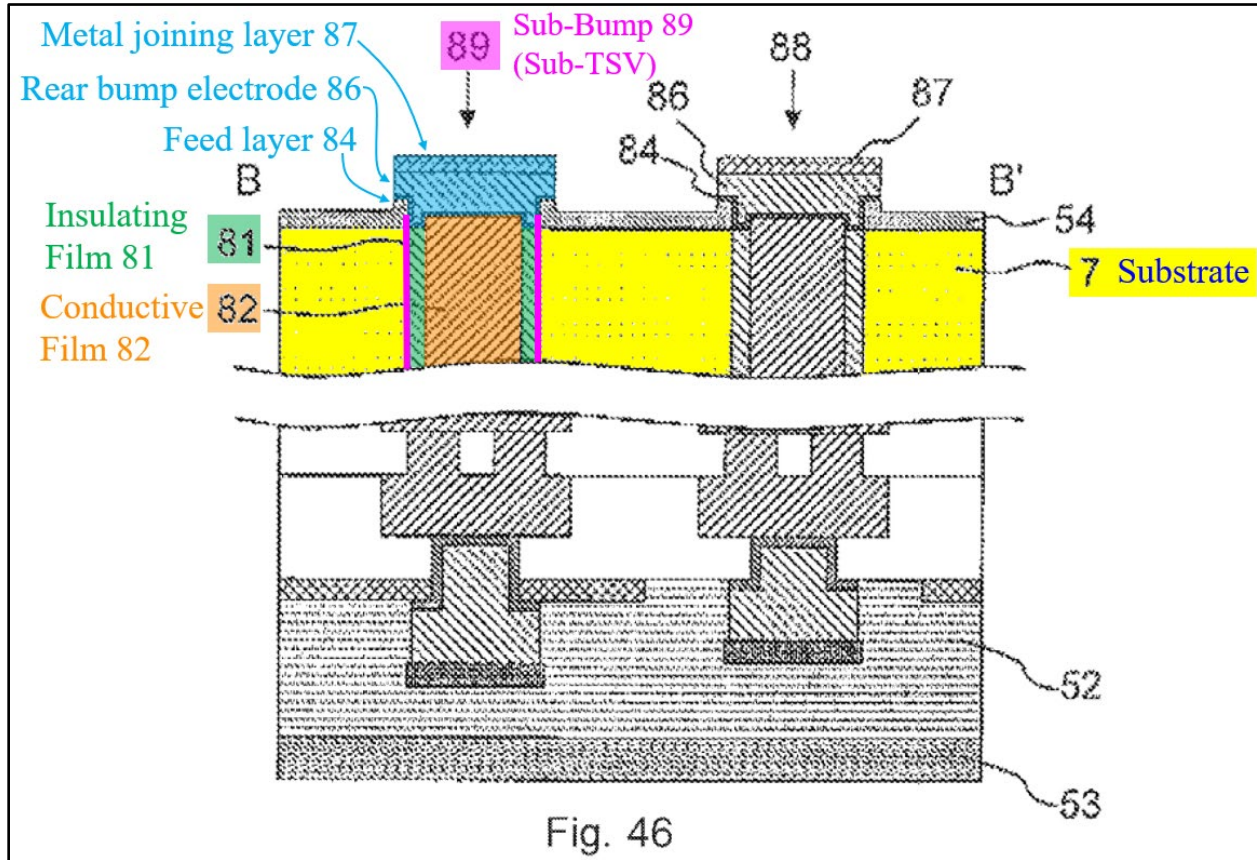
2. [1a]

Figure 3 of *Torii* provides a plan view of the semiconductor chip, showing that “[s]ub-bumps 6 are [] arranged in the outer circumference of semiconductor chip 1,” including corners of the chip. *Torii*, [0045]. *Torii* discloses “a sub-bump is formed as part of a sub-TSV” and uses these two terms interchangeably, so sub-bumps 6’ positions in Figure 3 represent the sub-TSVs’ positions. *Id.*, [0090]; *Torii*, [0048] (“a TSV provided with sub-bumps is referred to as a sub-TSV”); Thompson, ¶177. *Torii* discloses the sub-TSVs are used for joining adjacent semiconductor chips, so they serve as anchor points. *Torii*, [0083], [0090]; Thompson, ¶177. *Torii* further discloses that elements of the chip are formed on a

[0094], [0100]-[0101]. Therefore, *Torii* satisfies claim [1a]. Thompson, ¶177.



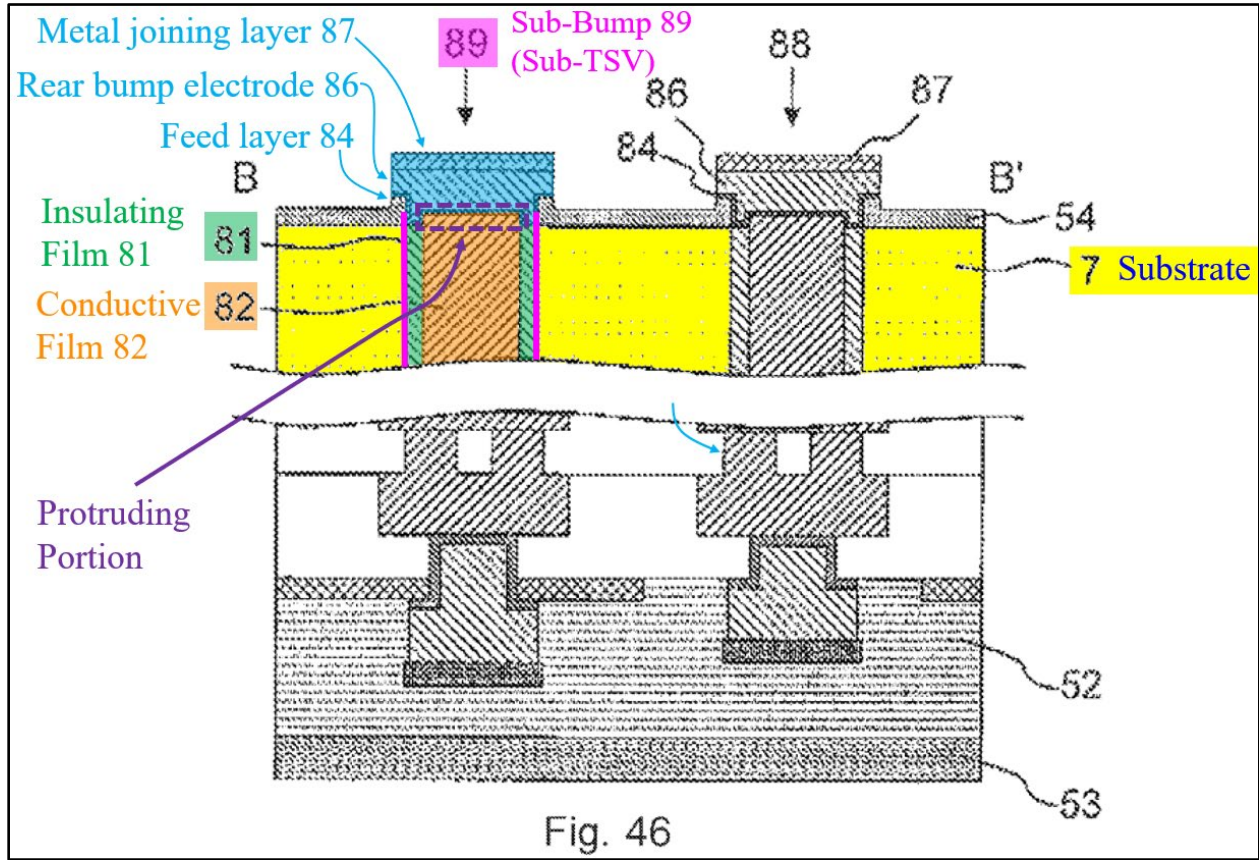
Torii, Fig. 3.



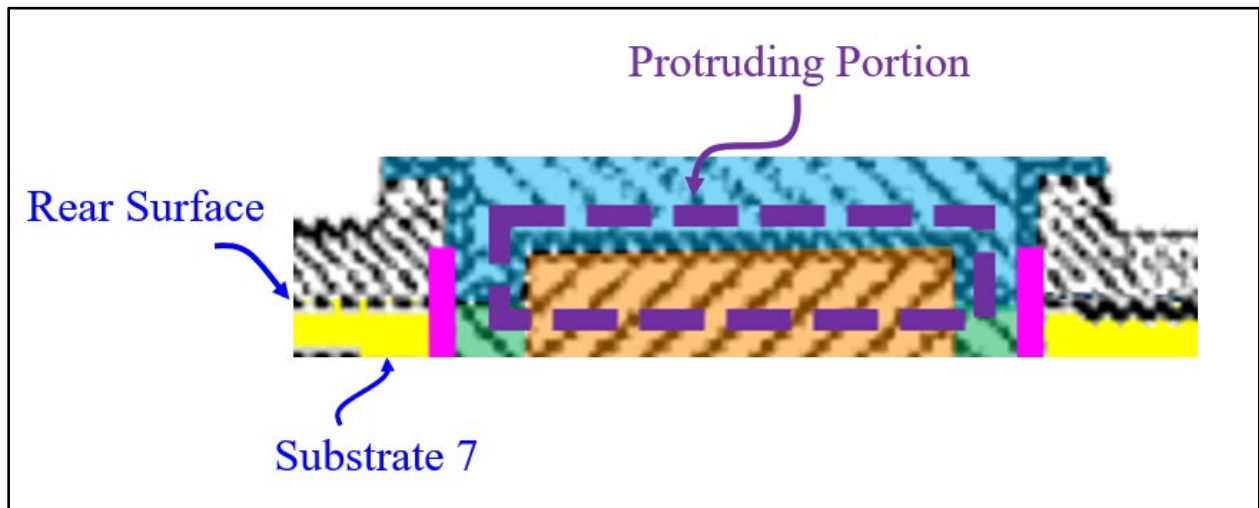
Torii, Fig. 46.

3. [1b]

Torii's Figure 46 shows a **conductive film 82**, e.g., **copper**, is within **sub-bump 89 (sub-TSV)**. *Id.*, [0096]-[0097], [0099]-[0100]. *Torii* discloses "the bottom of **conductive film 82** slightly **protrudes** from the rear surface of the substrate." *Id.*, [0099], Figs. 39, 46. *Torii* therefore satisfies claim [1b]. Thompson, ¶178.



Torii, Fig. 46.



Torii, Fig. 46 (excerpted, zoomed).

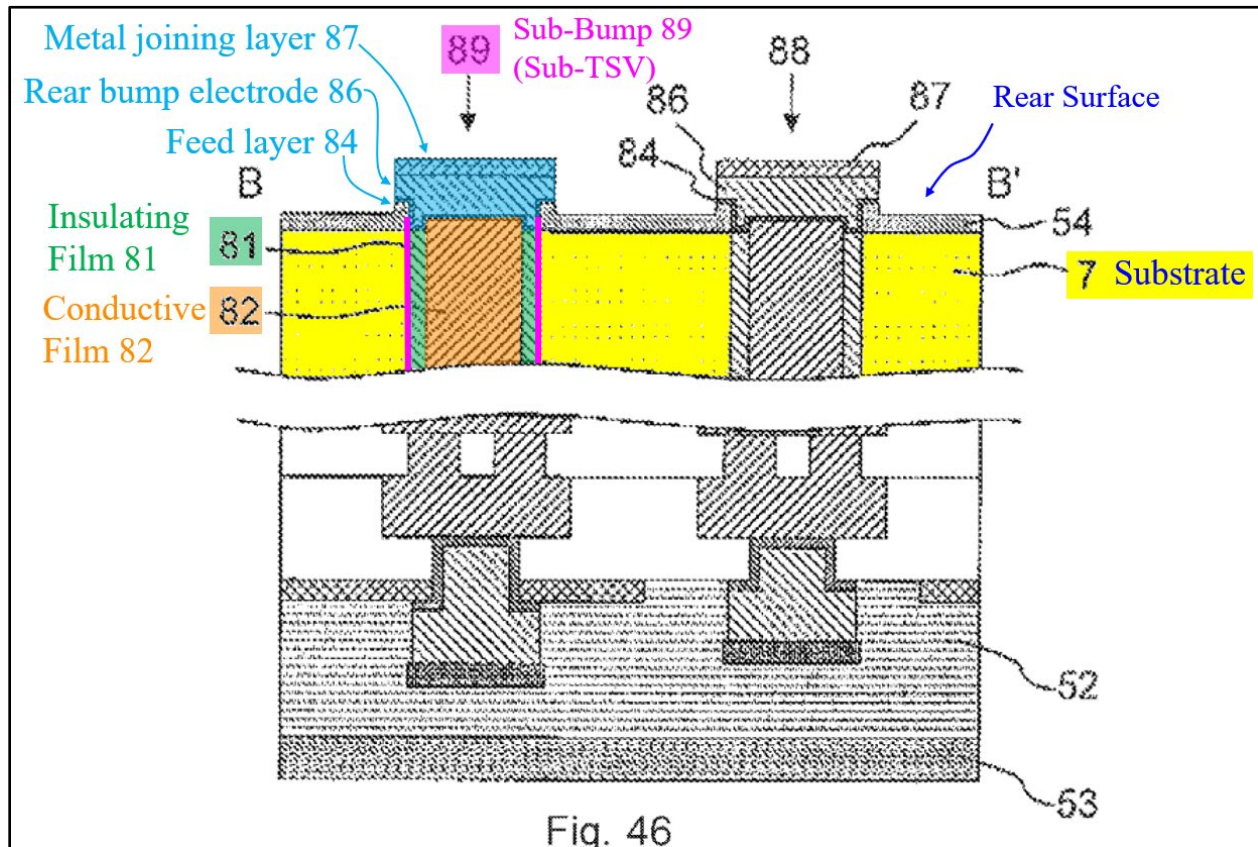
4. [1c]

Torii's Figure 46 discloses a “[s]econd feed layer 84 is formed on the rear surface” of the substrate and the protruding position of conductive film 82. *Id.*, [0100], Figs. 40-46. Notably, Figure 46 shows feed layer 84 forms a shoulder region on the substrate surface.¹² *Id.* This is a result of the fabrication process described in Figures 40-46. Thompson, ¶179. Moreover, the rear surface in Figure 46 is facing up to facilitate a “backside-grinding” process. *Id.*, [0040], [0099]; Thompson, ¶180. Thus, *Torii*'s “rear surface,” i.e., backside, discloses the claimed “bottom surface.” Thompson, ¶180. Moreover, *Torii* discloses second feed layer 84 is made of metal, e.g., copper and/or titanium, and is disposed on the protruding position by a sputtering or electrolytic plating method, resulting in a metallic bonding between second feed layer 84 and conductive film 82. *Id.*, [0067], [0081]; Thompson, ¶180. Also, “rear bump electrode 86 and second metal joining layer 87 are formed by electrolytic plating” and are disposed on second feed layer 84. *Torii*, [0100], Figs. 45-46. Here, second feed layer 84 alone, or together with rear bump

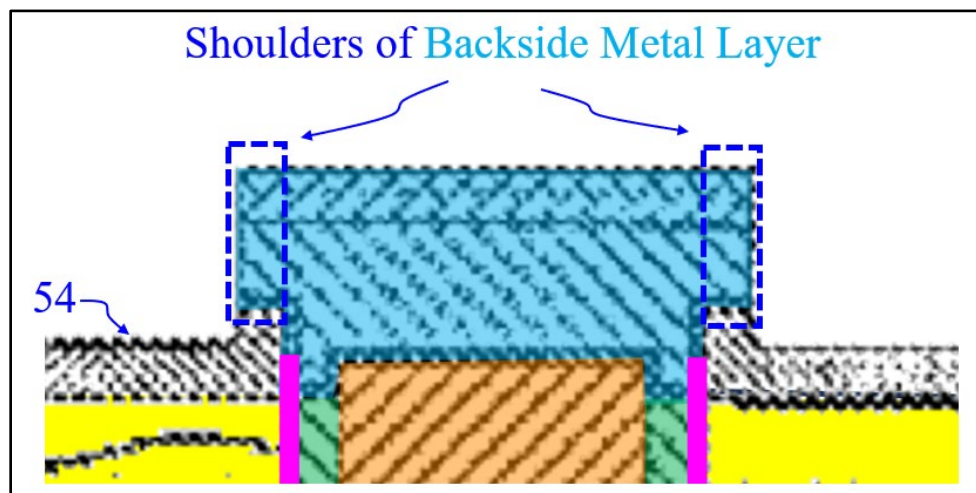
¹² Rear-surface protective film 54 is between the shoulder region and the substrate surface. *Torii*, [0100]. But, the plain and ordinary meaning of “on” does not require direct contact, so the shoulder region is “on” the substrate surface, as claimed.

AFG Indus., Inc. v. Cardinal IG Co., 239 F.3d 1239, 1251 (Fed. Cir. 2001).

electrode 86 and second metal joining layer 87, constitutes the claimed “backside metal layer.” Thompson, ¶180.



Torii, Fig. 46.



Torii, Fig. 46 (excerpted, zoomed).

5. [1d]

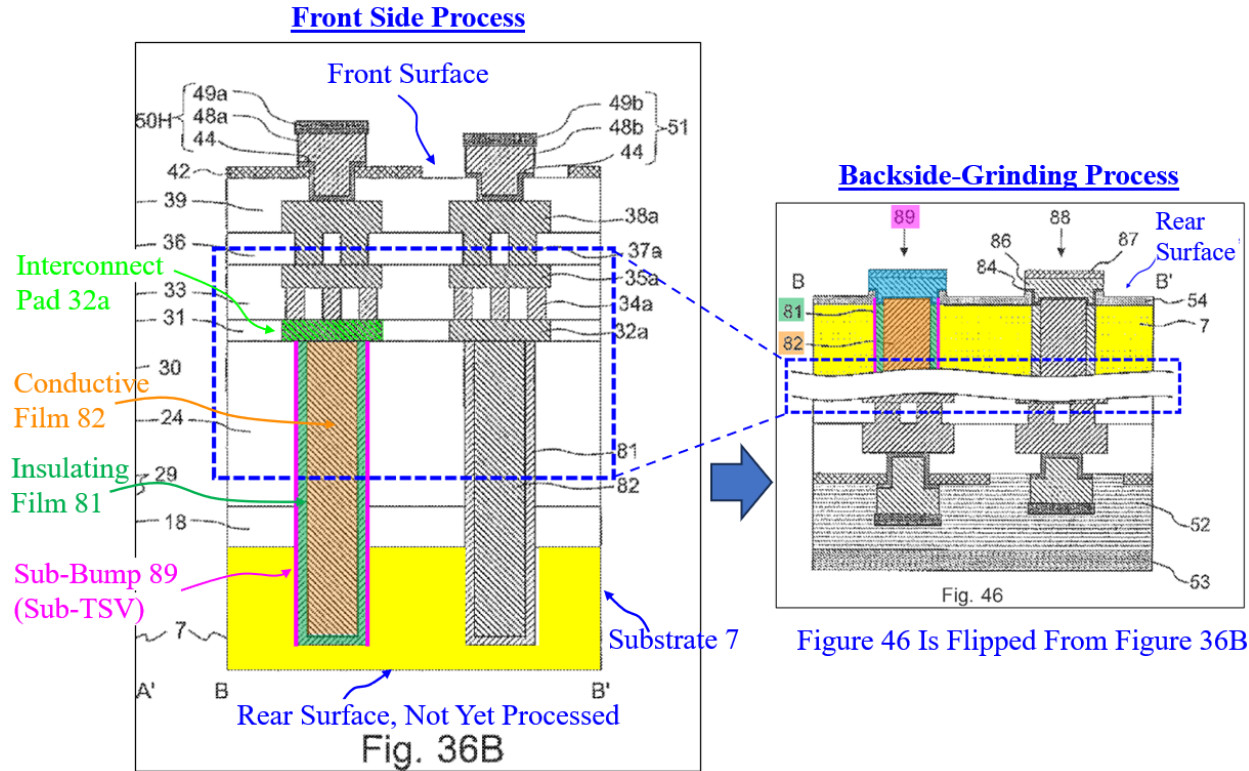
Torii meets it because “[t]he sub-TSV is a dummy ... normally not used as a current pathway.” *Id.*, [0048]; Thompson, ¶181.

B. Claim 8

Torii’s second feed layer 84, rear bump electrode 86, and second metal joining layer 87 respectively correspond to the claimed “interface layer,” “conduction layer,” and “packaging layer.” *Supra*, §IX.A.4; Thompson, ¶182.

C. Claim 9

As discussed in §IX.A.4, the semiconductor device in Figure 46 is placed upside down to show a backside-grinding process. Correspondingly, the semiconductor device in Figure 36B is flipped from Figure 46 and shows a front side process to create the TSVs. *Torii*, [0093], [0098]. Thus, in Figure 36B, the semiconductor device is in its normal orientation with the front surface facing up. Thompson, ¶183. Figure 36B shows conductive film 82 in sub-bump 89 (sub-TSV) is bonded to a third interconnect pad 32a overlying the semiconductor substrate. *Torii*, [0054]. Third interconnect pad 32a is “composed of a conductive material such as metal.” *Id.*, [0055]. Therefore, *Torii* meets claim 9. Thompson, ¶183.

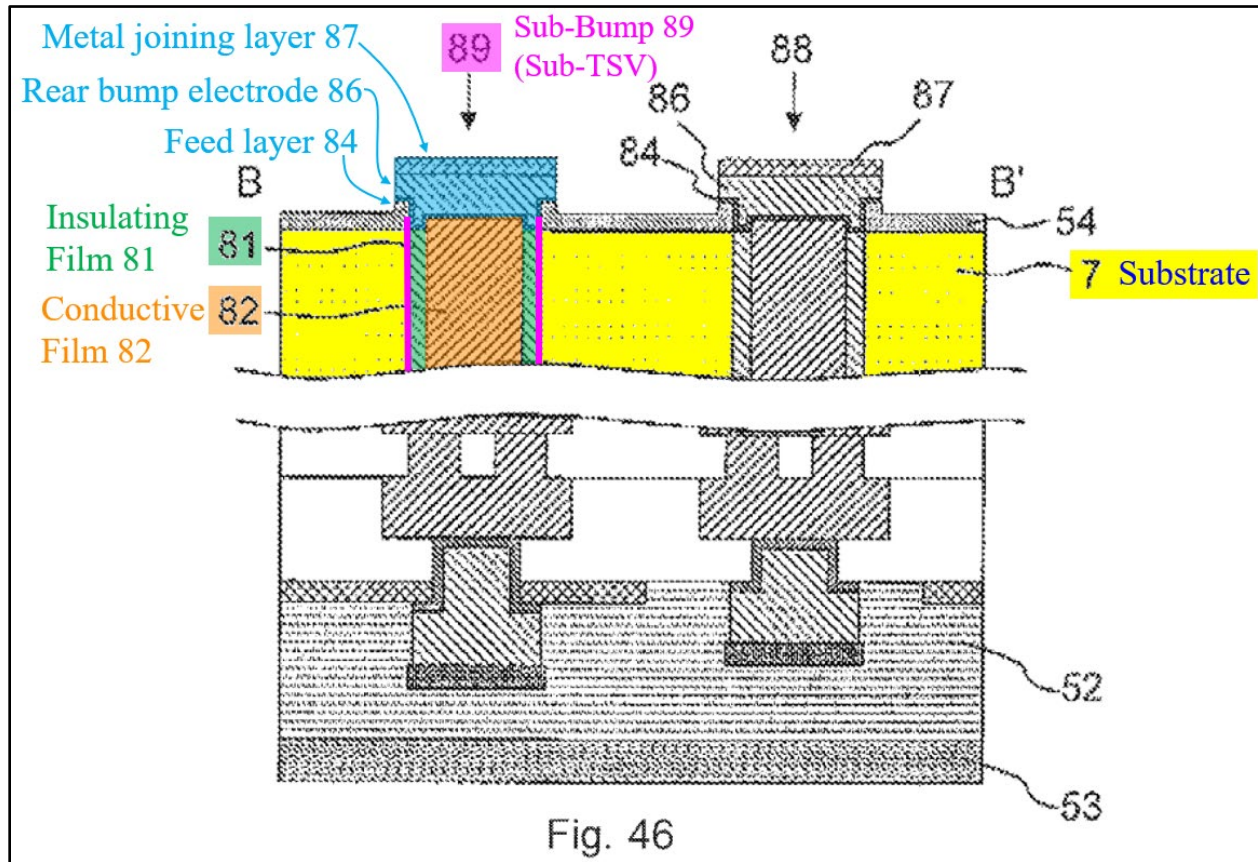


Torii, Figs. 36B, 46.¹³

D. Claim 10

Torii's Figure 46 discloses claim 10 by disclosing an **insulating film 81** is formed on the sidewall of **sub-bump 89 (sub-TSV)**, and between **conductive film 82** and the substrate. *Id.*, [0095], [0097], [0099]-[0100]; Thompson, ¶184.

¹³ The front side process (Figure 36B) occurs before the backside-grinding process (Figure 46), so the rear surface in Figure 36B is not yet processed. Thompson, n.10.



Torii, Fig. 46.

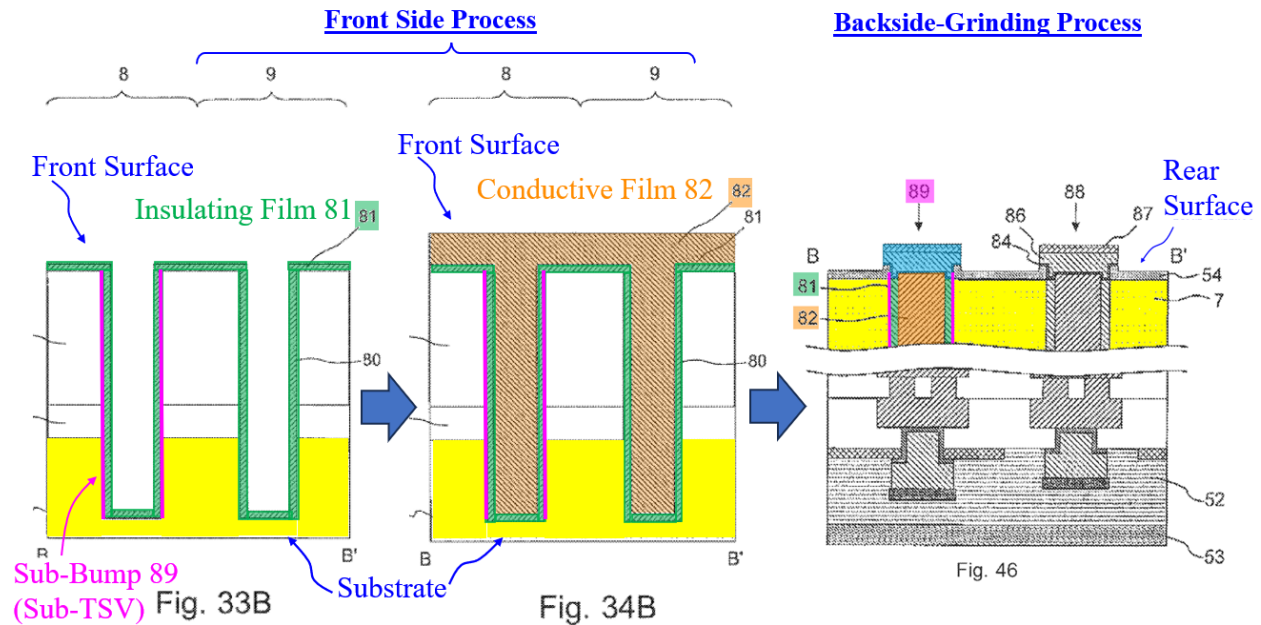
E. Independent Claim 11

1. “Forming,” “depositing,” and “forming” steps

Torii discloses a method for making the semiconductor device in Figures 3 and 46. *E.g.*, *Torii*, [0093]-[0101], Figs. 32A-36B (front side process), Figs. 37-46 (backgrinding process); Thompson, ¶185. As shown below, *Torii* discloses each of the claimed [11a] “forming at least one **anchor via**,” [11b] “depositing a **metal filler**,” and [11c] “forming a **backside metal layer**.” *Torii*, [0093], [0095]-[0096], [0100]; Thompson, ¶185. Figures 33B and 34B show a front side process to form **sub-bump 89 (sub-TSV)** and deposit **conductive film 82** in **sub-bump 89**

(sub-TSV). Thompson, ¶185. Figure 46 shows a backside-grounding process in which the stack of second feed layer 84, rear bump electrode 86, and second metal joining layer 87 is formed on and bonded to the rear surface of conductive film 82.

Id.



Torii, Figs. 33B, 34B, 46.

2. Remaining limitations of claim 11

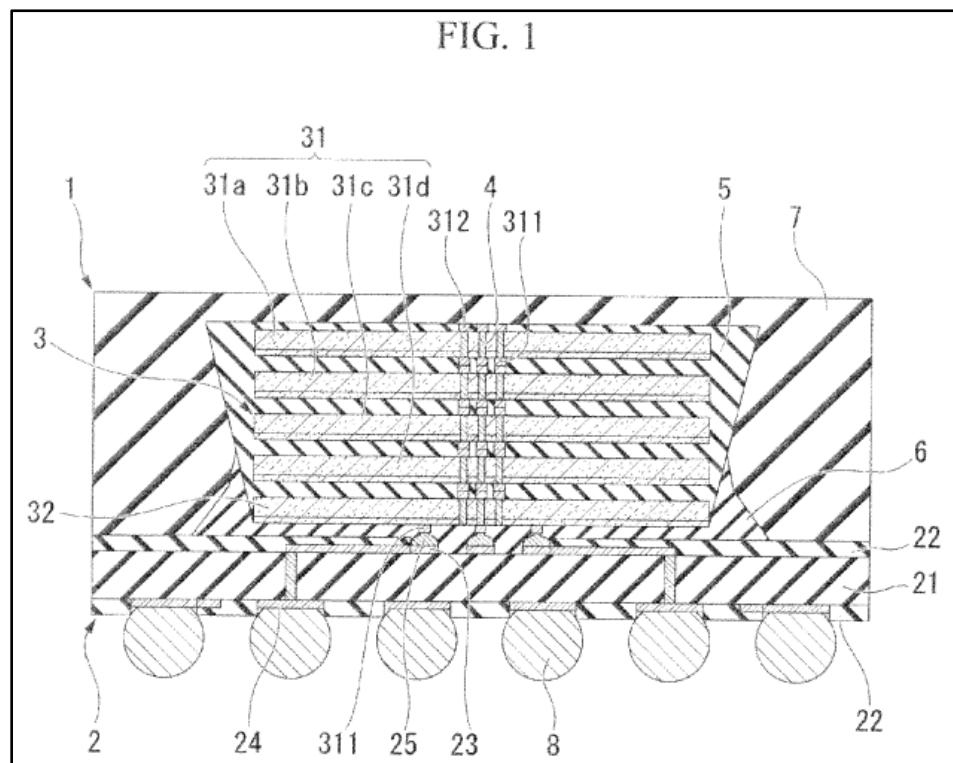
The remaining features of claim 11 are similar to those in claim 1 and disclosed by *Torii* for the same reasons in §§IX.A.2–IX.A.5. Thompson, ¶186.

F. Claims 18-20

Claims 18-20 are anticipated by *Torii* for the reasons discussed for claims 11 and 8-10. Thompson, ¶¶187-189.

X. Ground 5: *Ide* Anticipates Claims 1, 2, 3, 9, 11, 12, 13, 19**A. Independent Claim 1****1. [1pre]**

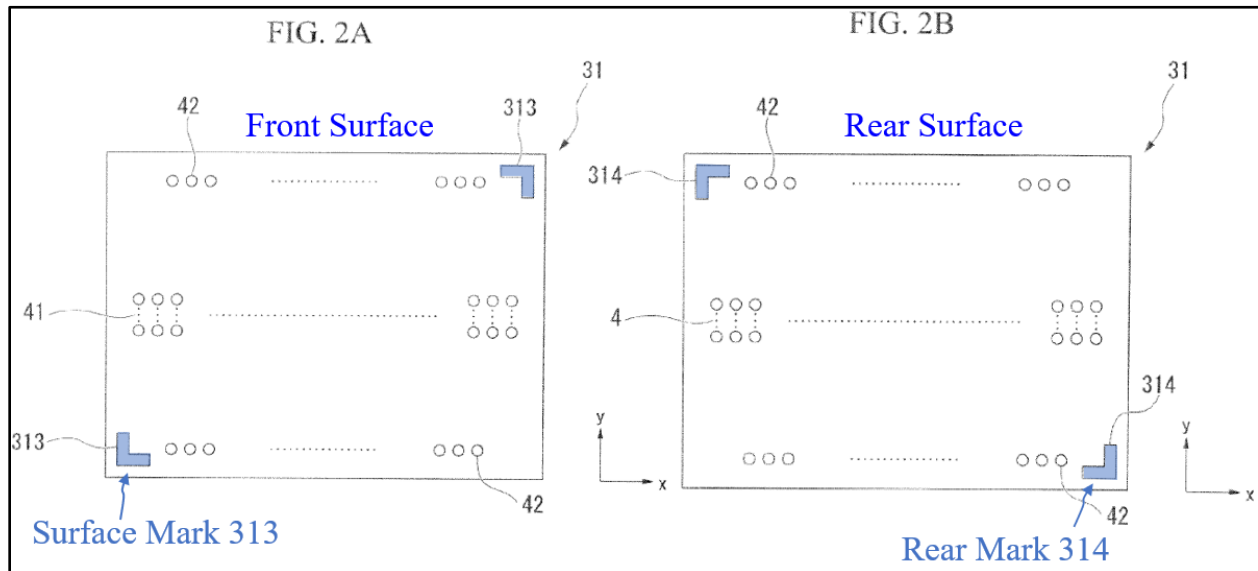
Ide discloses [1pre] by disclosing a semiconductor chip. *Ide*, [0033]-[0036], [0112]-[0127], Figs. 2A-2B, 3A-3B; Thompson, ¶¶190-193. Multiple of such chips (e.g., 31a, 31b, 31c, and 31d in Figure 1) can be vertically stacked to form a memory device. *Ide*, [0005]-[0006], [0010].



Ide, Fig. 1.

To facilitate inter-chip alignment, each chip has [surface marks 313](#) arranged in a pair of corners of its front surface (Figure 2A below) and [rear marks 314](#) arranged

in corresponding corners of its rear surface (Figure 2B below). *Id.*, [0033]-[0034], [0112]-[0114].



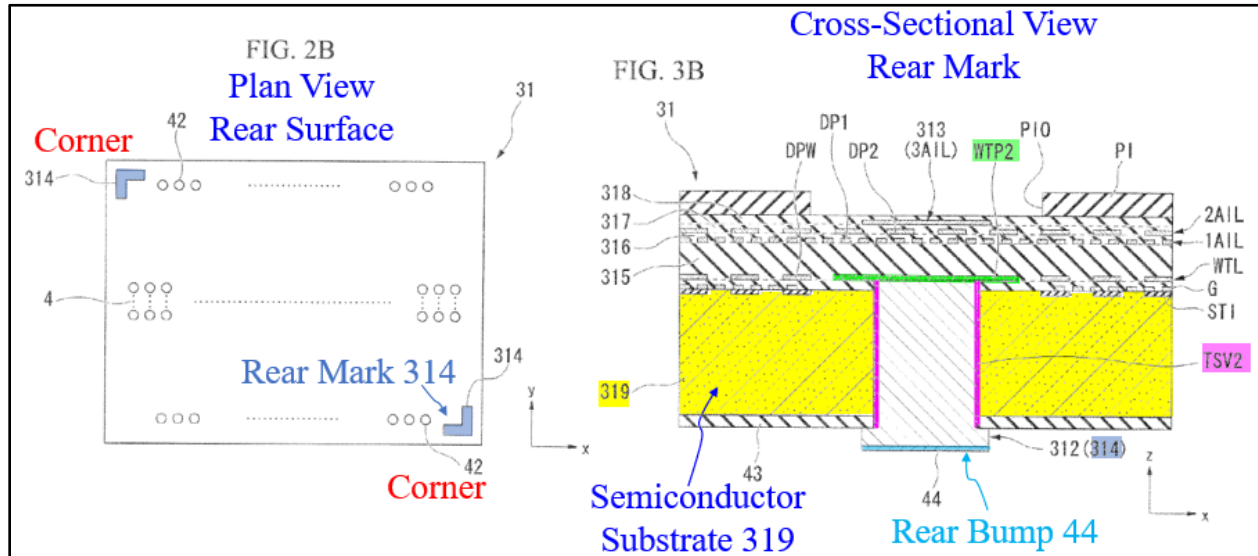
Id., Figs. 2A-2B.

2. [1a]

Figure 2B of *Ide* provides a plan view showing “rear marks 314 are arranged in a pair of corners which are located diagonally to each other[.]” *Ide*, [0114]. And Figure 3B provides a corresponding cross-sectional view showing each rear mark 314 is formed below a through electrode TSV2, so the TSV2s are also located at the corners of the chip in plan view. *Id.*, [0125]; Thompson, ¶194. Figure 3B also shows “[t]he through electrode TSV2 for a mark penetrates the semiconductor substrate 319.” *Ide*, [0130]. The TSV2 connects to a rear bump 44 and a wiring tungsten pad WTP2 on the two opposite sides of the substrate, thereby providing an anchor point for affixing and aligning rear bump 44 and wiring

tungsten pad WTP2. *Id.*, [0125]. Therefore, *Ide*'s TSV2 constitutes the claimed

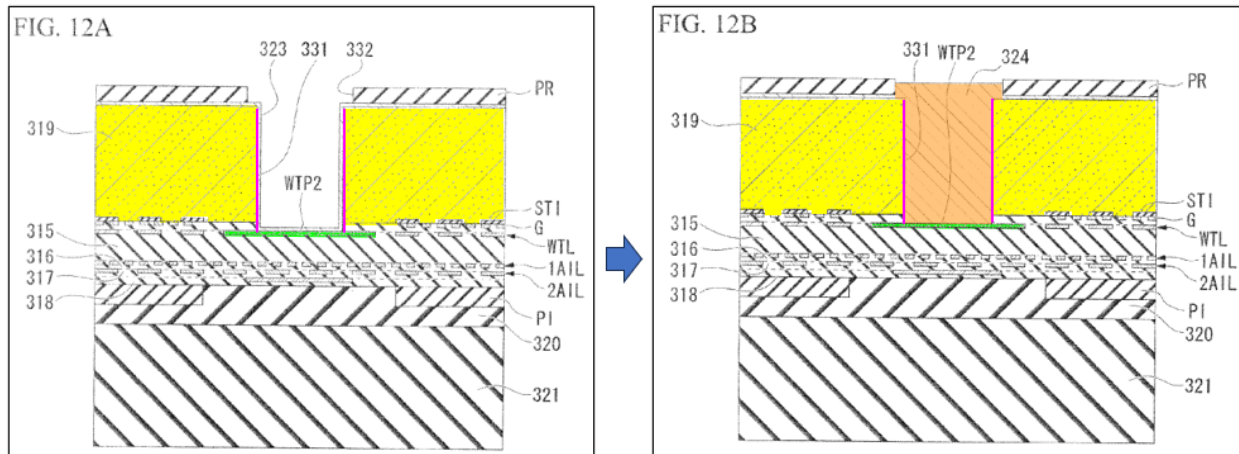
“anchor via.” Thompson, ¶194.



Ide, Figs. 2B, 3B.

3. [1b]

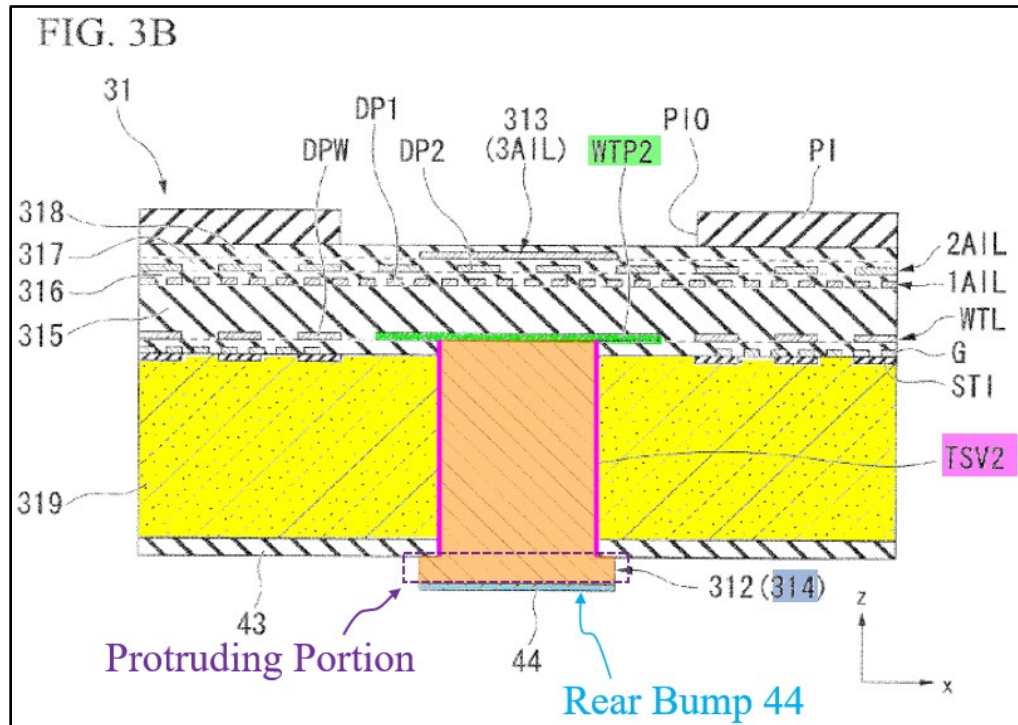
As shown in Figures 12A and 12B, during fabrication, “a Cu plating 324 is grown using a seed layer 323 as an electrode to fill a via of the through electrode TSV2....” *Id.*, [0156]; Thompson, ¶195.



Ide, Figs. 12A-12B.¹⁴

And, as shown in Figure 3B, in the finished device, **Cu plating 324** forms a rear bump electrode 312 (i.e., the claimed “**protruding portion**”) extending from the rear surface (i.e., backside) of semiconductor substrate 319. *Id.*, [0130], [0155]-[0157]; Thompson, ¶196.

¹⁴ The device in Figures 12A and 12B is displayed as having been inversed from the finished product in Figure 3B, to facilitate the backside processing. *Supra*, §II.B; Thompson, n.11.



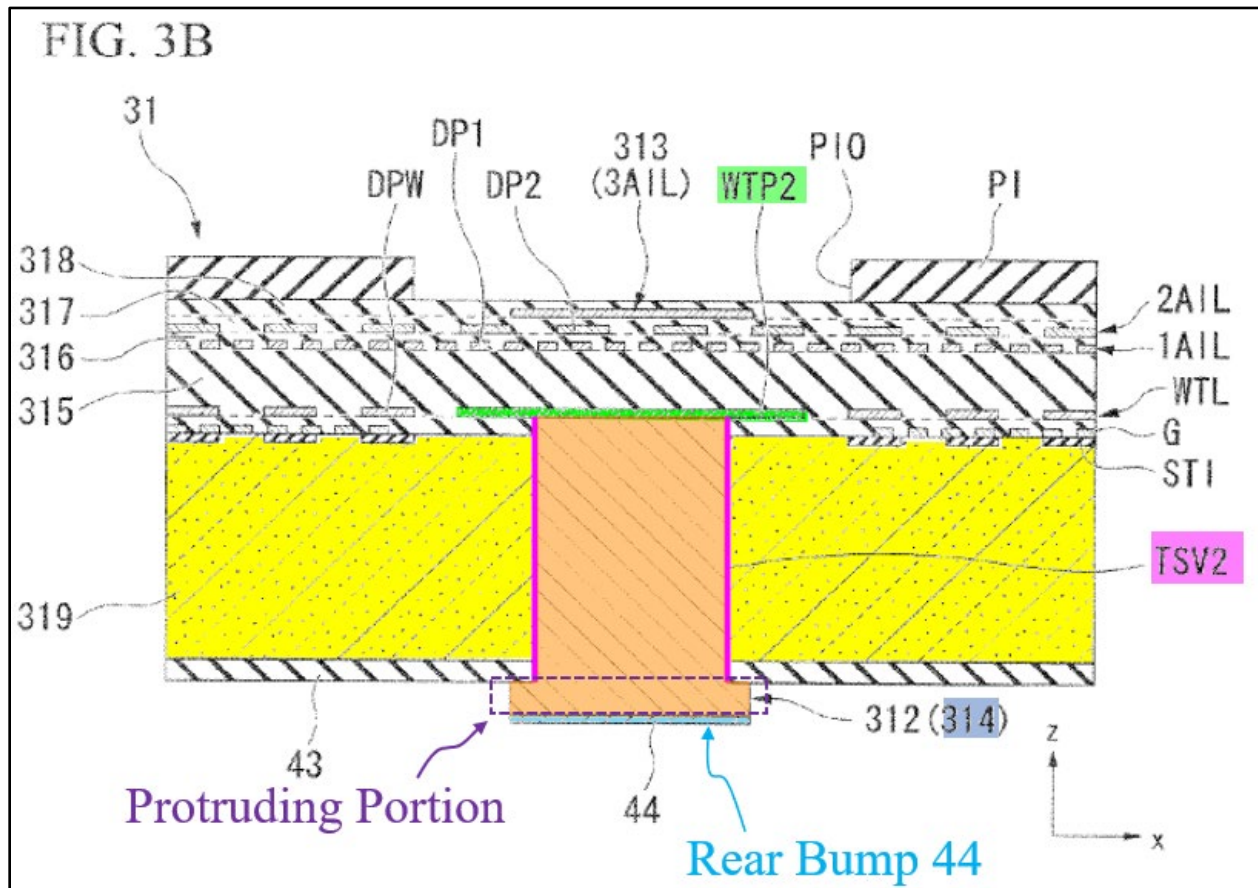
Ide, Fig. 3B.

4. [1c]

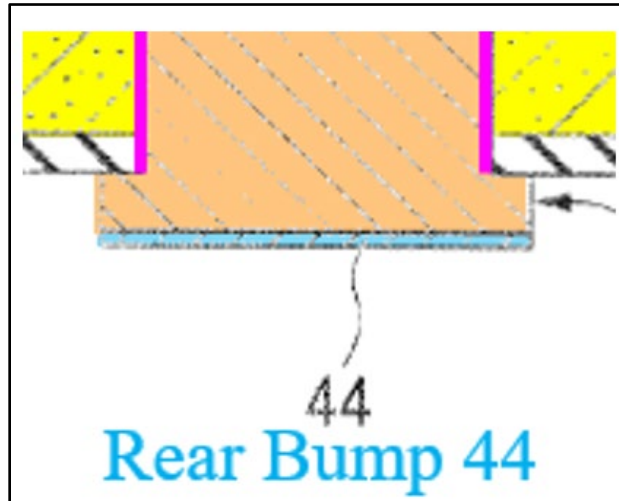
As shown in Figure 3B, *Ide* discloses rear bump 44 is “formed in a surface (a rear surface) of the semiconductor substrate” and “below the through electrode TSV2.” *Id.*, [0120], [0125], Figs. 3B, 13A. Notably, Figure 3B shows that at least part of rear bump 44 is on the rear surface.¹⁵ Thompson, ¶197; *see also Ide*, Fig. 4C. Rear bump 44 is made of “SnAg” (tin-silver alloy), i.e., a metal, and formed on

¹⁵ Despite the intervening rear insulating layer 43 and rear bump electrode 312, (*Ide*, [0120], [0156]-[0157], Fig. 3B), rear bump 44 is “on” and the substrate rear surface, as claimed. *Supra*, n.12.

Cu plating 324 “by plating.” *Id.*, [0157], Fig. 13A; Thompson, ¶198. A POSA would understand that plating the tin-silver alloy on copper will cause them to form a metallic bond. Thompson, ¶198. Thus, rear bump 44 is bonded to the protruding portion of Cu plating 324 in the TSV2. *Id.*



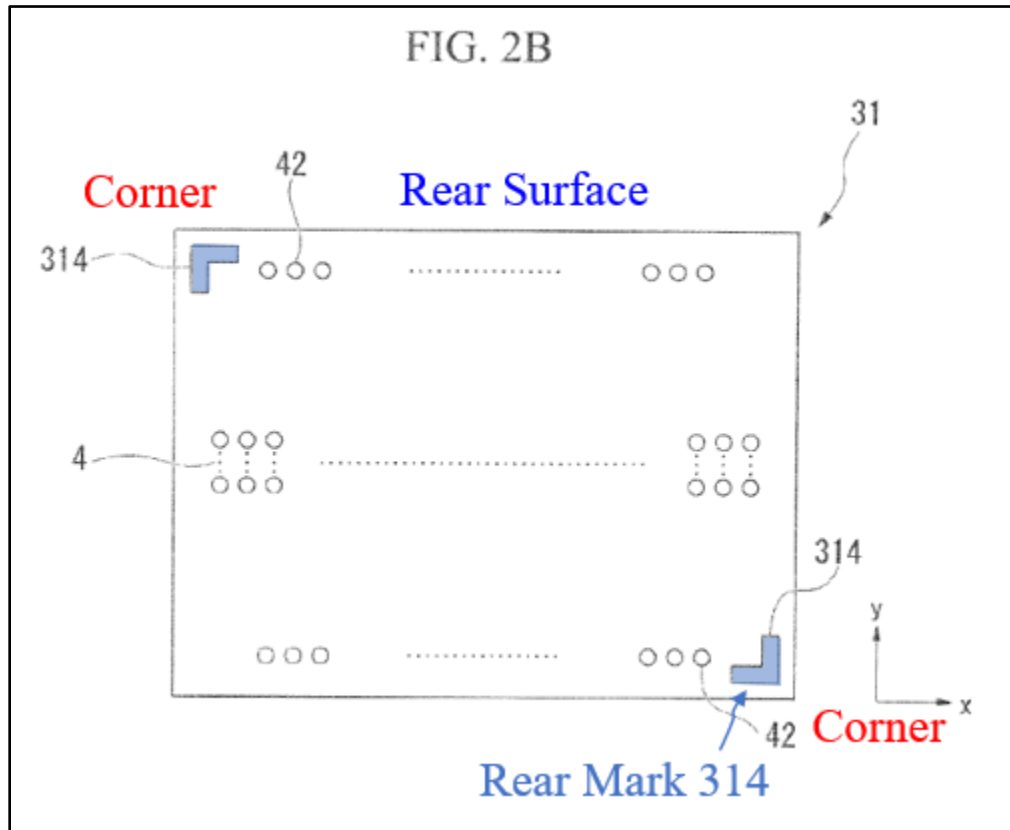
Id., Fig. 3B.



Ide, Fig. 3B (excerpted, zoomed).

5. [1d]

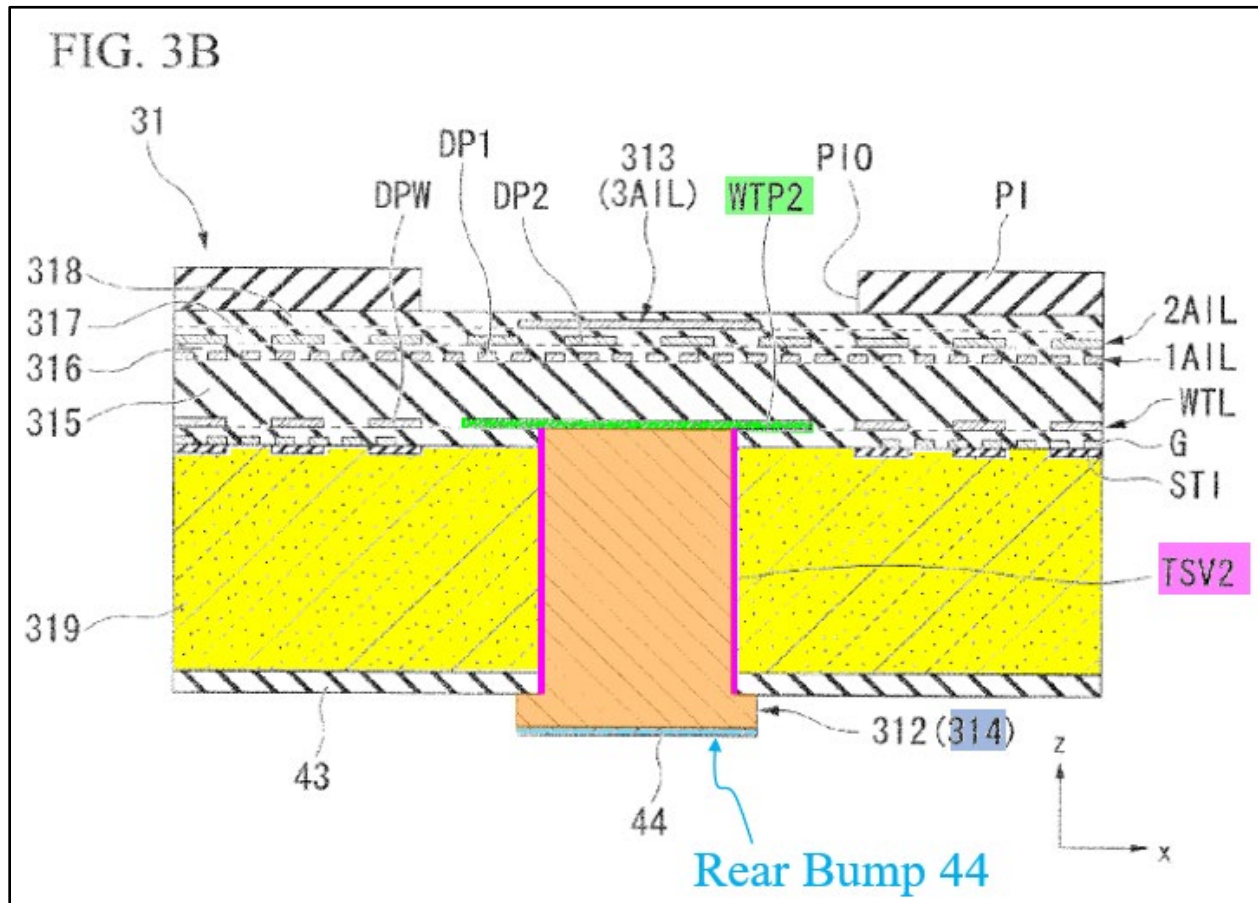
As shown in Figure 3B, *Ide* meets [1d] by disclosing “rear marks 314 are arranged within an area in which the plurality of dummy bump through electrodes 42 are arranged[.]” *Id.*, [0115]; Thompson, ¶199. Thus, rear marks 314, and associated TSV2s, are located in a dummy region of the chip and not intended for electrical connections. Thompson, ¶199.



Ide, Fig. 2B.

Also, *Ide* discloses **Cu plating 324** in the **TSV2** is connected to **wiring tungsten pad WTP2** on the front side of the substrate. *Id.*, [0125]. Figure 3B shows **wiring tungsten pad WTP2** is below “a lower dummy pattern” (first aluminum wiring layer 1AIL) and “an upper dummy pattern” (second aluminum wiring layer 2AIL), both of which are not for electrical connections. *Id.*, [0126]; Thompson, ¶200. *Ide* further discloses that “**the functional wirings are not** arranged in the first and second aluminum wiring layers 1AIL and 2AIL of an area on **wiring tungsten pad WTP2**.” *Ide*, [0127]. This means **wiring tungsten pad**

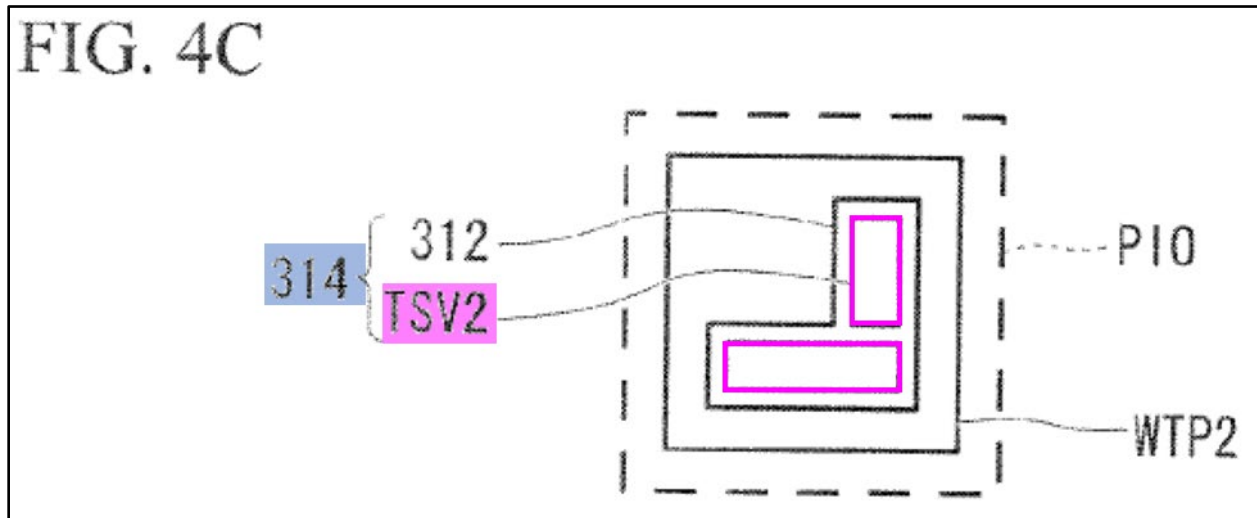
WTP2 cannot function as a path to electrically connect Cu plating 324 in TSV2 to any active devices. Thompson, ¶200.



Ide, Fig. 3B.

B. Claim 2

Ide meets it because Figure 4C (plan view of rear surface) shows that each “rear mark 314 ha[s] an L shape” including a cluster of two perpendicularly arranged TSV2s. *Id.*, [0039], [0129]-[0130]; *Ide*, [0059]-[0060], [0152]-[0153], Figs. 11A-11B; Thompson, ¶201.



Ide, Fig. 4C.

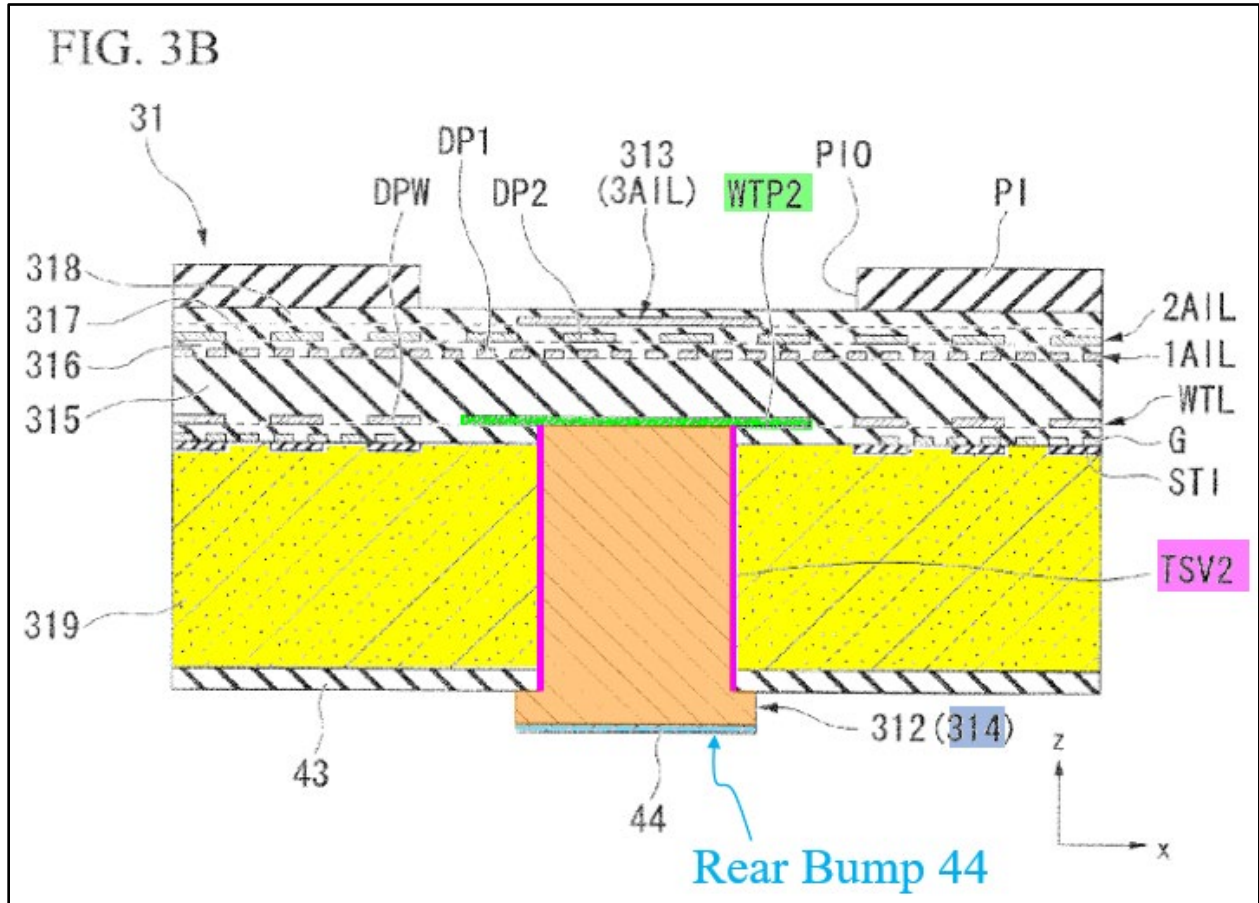
C. Claim 3

The structure of claim 2, wherein each **anchor via** within said cluster of **anchor vias** is oriented perpendicular to an adjacent **anchor via** within said cluster of **anchor vias**.

Ide meets it for the reasons discussed for claim 2. *Supra*, §X.B; Thompson, ¶202.

D. Claim 9

Ide meets it by disclosing **wiring tungsten pad WTP2** overlying semiconductor substrate 319 and bonded to **Cu plating 324** in the **TSV2**. *Ide*, [0125], [0130], [0154]-[0156], Figs. 3B, 12B; Thompson, ¶203.



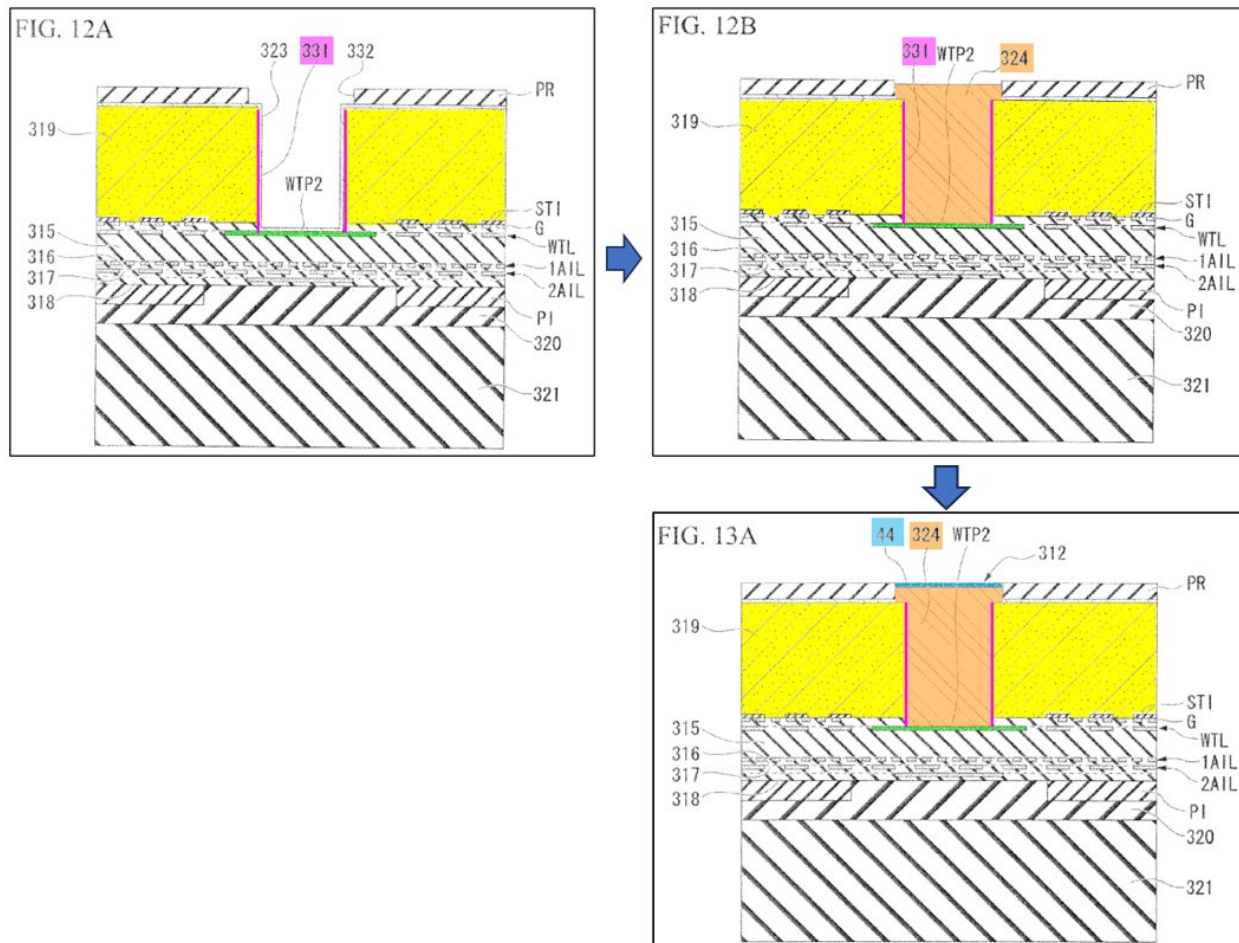
Ide, Fig. 3B.

E. Independent Claim 11

1. “Forming,” “depositing,” and “forming” steps

Ide discloses a method for making a semiconductor device. *Ide*, [0137], Figs. 6A-14; Thompson, ¶204. As shown below, *Ide* discloses each of the claimed [11a] “forming at least one anchor via,” [11b] “depositing a metal filler,” and [11c] “forming a backside metal layer.” *Ide*, [0152]-[0159], Figs. 11A-13C; Thompson, ¶204. Namely, *Ide* discloses “a dry etching process is performed using the photoresist PR as a mask to form an opening 331 of the through electrode TSV2”

(Figure 12A), “a Cu plating 324 is grown using a seed layer 323 as an electrode to fill a via of the through electrode TSV2” (Figure 12B), and “SnAg is formed as rear bump electrode 312 including rear bump 44 by plating” (Figure 13A). *Ide*, [0152], [0156]-[0157]; Thompson, ¶204.



Ide, Figs. 12A-12B, 13A.

2. Remaining limitations of claim 11

The remaining features of claim 11 are similar to those in claim 1 and disclosed by *Ide* for the same reasons in §§X.A.2 through X.A.5. Thompson, ¶205.

F. Claims 12, 13, 19

Claims 12, 13, and 19 are anticipated by *Ide* for the reasons discussed for claims 11, 2, 3, and 9. Thompson, ¶¶206-208.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

A. Denial of Institution Is Not Warranted Under *Fintiv*

Fintiv and the Office’s interim guidelines dated June 21, 2022 (“Interim Procedures”) require institution. Factor 6 requires institution because Petitioner presents a compelling unpatentability challenge; Factors 3 and 4 favor institution; and Factors 1, 2, and 5 are, at worst, neutral.

Factor 3 favors institution because Petitioner acted diligently and almost no parallel investment has occurred. Patent Owner served infringement contentions only on July 18, 2024. Ex. 1032. Fact discovery opened only last month, and will not close until August 18, 2025, with expert discovery closing September 22, 2025. Ex. 1033, 3. The parties will not begin claim construction until March 4, 2025, and the hearing will not take place until July 8, 2025. *Id.*, 3-4.

Factor 4 favors institution because this Petition additionally challenges claims 3, 5-8, 10, 13, 15-18, and 20, which are not involved in the litigation. Moreover, Petitioner has not served invalidity contentions, so no overlap currently exists. Petitioner reserves the right to submit a stipulation after serving invalidity contentions.

Regarding Factors 1, 2, and 5, no stay has been requested, and trial is currently scheduled for January 5, 2026, (*id.*, 1), two months before the anticipated FWD in March, 2026. In these circumstances, Factors 1, 2, and 5 are at worst neutral. *Protect Animals with Satellites v. OnPoint Sys.*, IPR2021-01483, Paper 11 at 12-13, 17 (Mar. 4, 2022). Indeed, the Board has instituted with far more time between trial and FWD. *See NetNut v. Bright Data*, IPR2021-01492, Paper 12 at 9-16 (Mar. 21, 2022) (instituting IPR without stipulation and patent owner arguing trial date six months before FWD); *Protect Animals*, IPR2021-01483, Paper 11 at 18-19 (same with patent owner arguing trial date two months before FWD); Interim Procedures, 8.

Denial of institution is not warranted under *Fintiv*.

B. Denial of Institution Is Not Warranted Under 35 U.S.C. §325(d)

No other proceedings involving the '826 patent are currently pending or have been brought before the Patent Office. Additionally, none of the asserted prior art references were before the Examiner during prosecution. Thus, the same or substantially the same prior art or arguments have not been previously presented to the Patent Office and denial of institution is not warranted under §325(d).

XII. MANDATORY NOTICES

A. Real Party-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.

B. Related Matters

HID asserted the '826 patent in *Harbor Island Dynamic, LLC v. Samsung Electronics Co. Ltd. et al*, Case No. 2-24-cv-00140 (E.D. Tex).

The '826 patent is not related to any known pending applications.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

XIII. GROUNDS FOR STANDING

Petitioner certifies that the '826 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

XIV. CONCLUSION

Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Dated: September 20, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CLAIMS APPENDIX

1. **[1pre]** A structure comprising:
 - [1a]** at least one anchor via disposed in at least one corner of a semiconductor substrate;
 - [1b]** a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
 - [1c]** a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;
 - [1d]** wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.
2. **[2a]** The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.
3. **[3a]** The structure of claim 2, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

4. **[4a]** The structure of claim 1, wherein
said at least one anchor via comprises a plurality of anchor vias disposed in a
straight line along a periphery of said semiconductor substrate.
5. **[5a]** The structure of claim 4, wherein
a linear density of said plurality of anchor vias is less than approximately
10% of a total linear distance of said straight line along said periphery
of said semiconductor substrate.
6. **[6a]** The structure of claim 1, wherein
said at least one anchor via comprises a plurality of anchor vias disposed in a
staggered configuration along a periphery of said semiconductor
substrate.
7. **[7a]** The structure of claim 1, wherein
a total area of said at least one anchor via is less than approximately 0.5% of
a total area of said semiconductor substrate.
8. **[8a]** The structure of claim 1, wherein

said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

9. **[9a]** The structure of claim 1, wherein
said metal filler within said at least one anchor via is bonded to a metal layer
overlying said semiconductor substrate.
10. **[10a]** The structure of claim 1, further comprising
an insulating layer disposed between said semiconductor substrate and said
metal filler in said at least one anchor via.
11. **[11pre]** A method comprising:
[11a] forming at least one anchor via in at least one corner of a
semiconductor substrate;
[11b] depositing a metal filler within said at least one anchor via, said metal
filler having a protruding portion extending from a backside of said
semiconductor substrate;
[11c] forming a backside metal layer on a bottom surface of said
semiconductor substrate, said backside metal layer being bonded to

said protruding portion of said metal filler of said at least one anchor via;

[11d] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

12. **[12a]** The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.

13. **[13a]** The method of claim 12, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

14. **[14a]** The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate.

15. **[15a]** The method of claim 14, wherein

a linear density of said plurality of anchor vias is less than approximately

10% of a total linear distance of said straight line along said periphery
of said semiconductor substrate.

16. **[16a]** The method of claim 11, wherein said forming said at least one anchor via comprises

forming a plurality of anchor vias disposed in a staggered configuration

along a periphery of said semiconductor substrate.
17. **[17a]** The method of claim 11, wherein

a total area of said at least one anchor via is less than approximately 0.5% of

a total area of said semiconductor substrate.
18. **[18a]** The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of:

forming an interface layer; forming a conduction layer; forming a packaging layer.
19. **[19a]** The method of claim 11, further comprising

bonding said metal filler within said at least one anchor via to a metal layer
overlying said semiconductor substrate.

20. **[20a]** The method of claim 11, further comprising
forming an insulating layer between said semiconductor substrate and said
metal filler in said at least one anchor via.

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,893.

Dated: September 20, 2024

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on September 20, 2024, a copy of the foregoing Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1030 and 1032-1033 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 9,245,826:

Bever Hoffman & Harms, LLP
c/o Carrie Reddick, Office Manager
18486 Spring Valley Drive
Grass Valley, CA 95945

Date: September 20, 2024

By: /William Esper/
William Esper
Legal Assistant and PTAB Coordinator
FINNEGAN, HENDERSON, FARABOW,
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