

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01405
U.S. Patent No. 9,245,826

**DECLARATION OF DR. SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 9,245,826**

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4.	[1c] a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;	161
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I. INTRODUCTION

1. I, Scott E. Thompson, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”) in connection with an *inter partes* review (IPR) of U.S. Patent No. 9,245,826 (“the ’826 patent”) (Ex. 1001). I have prepared this declaration in connection with Samsung’s Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1-20 of the ’826 patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’826 patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-20 of the ’826 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of March 11, 2013), it is my opinion that claims 1-20 of the ’826 patent would have been anticipated and/or obvious based on the asserted grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '826 patent and the related prior art.

8. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of semiconductor devices.

9. I received my Bachelor of Electrical Engineering with Highest Honors from the University of Florida in 1987. I also received my Master of Science of Electrical Engineering in 1988 and my Ph.D. in Electrical Engineering in 1992, both from the University of Florida. My Ph.D. was funded by the Semiconductor Research Corporation. My Ph.D. dissertation studied CMOS integrated circuits, and I did extensive measurements and fabrication of CMOS test structures. My

Ph.D. dissertation earned a best paper award from the Semiconductor Research Corporation and a Best Ph.D. award from the University of Florida.

10. In 1992, after receiving my Ph.D., I joined Intel working on research and development of CMOS integrated circuits. From 1992 to 2004, I worked in Integrated Circuit development and semiconductor manufacturing. During this time, I managed the development of several integrated circuit manufacturing technologies for Intel including a 90 nanometer¹ and 130 nanometer² technologies.

11. These semiconductor manufacturing technologies used CMOS transistors, Copper interconnects and ball/pad connections. I won several Intel Achievement Awards for this work (Intel's highest award).

12. In 2000, I was promoted to Director of Semiconductor Technology Development in the Technology and Manufacturing Group at Intel. In that role, I was responsible for current and next-generation technology for integrated circuits.

¹ See S. Thompson et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1T1C SRAM cell," Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 61-64, doi: 10.1109/IEDM.2002.1175779.

² See S. Thompson et al., "130nm Logic Technology Featuring 60nm Transistors, Low-K Dielectrics and Cu Interconnects" (<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=0691ee478ab78508ef236ccb63fc3a04660f2850>).

In that role I managed different areas including transistor technology, interconnects, integrated circuit package integration, integrated circuit yield, in-line defect metrology, and strategic long ranges plans for semiconductor technology. The Intel Technology and Manufacturing Group manufactured billions of dollars of CMOS integrated circuits each year. In 2002, I was appointed to the position of Intel Fellow, which is the highest technical position at Intel, and awarded for outstanding technical achievement both within Intel and industry. In that Intel role, I managed the development and manufacturing of the most advanced CMOS integrated circuits in the semiconductor industry—from 2000 to 2004, Intel surpassed IBM in integrated circuit development and became the industry leader. My team and I presented this work at many international conferences and invited talks and short courses.

13. Since 2004, I have been a professor of electrical and computer engineering at the University of Florida. I was granted tenure and promoted to full professor in 2006. During my teaching career, I developed graduate level courses on advanced semiconductor chip design, semiconductor manufacturing, and packaging technology (e.g., chip stacking). I also teach a graduate level course on the chip technology used for CPU, DRAM, GPU, image sensors, and 2D and 3D image sensor processing. My current research areas include modeling and reliability integrated circuits. I currently have a Research Contract with Texas

Instruments on how package balls and pads introduce mechanical stress and shift the electrical characteristics of integrated circuits. My research in advanced chip technology at the University of Florida has been funded by contracts worth \$4M. I have supervised approximately 20 Ph.D. candidates on topics related to CMOS integrated circuits and have won several University of Florida teaching awards.

14. In 2009, I founded SuVolta, a company that developed ultra-low power chip technology for image sensors, system-on-chip microchips, radio frequency integrated circuits, memory, CPUs, image sensors processors, and other chips. The technology developed by SuVolta was sold to Fujitsu in 2015 and was used in the commercial production of Milbeaut image sensor processors. The technology allowed Fujitsu to lower the power consumption of the image sensor processor by 50%. Working with Fujitsu, we also developed CMOS chips that operated at ultra-low power and operate at less than 0.5V power supply. SuVolta received several awards and honors: (1) 2011 EuroAsia IC Industry Award for start-ups; (2) 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology; and (3) 2014 TiE 50 Top Startup. SuVolta was granted about 80 patents directed to low power transistor structures and integrated circuits on which I am a named inventor.

15. In 2006, I was elected as an IEEE Fellow for Advancing Fabrication of nanoscale MOSFET. In 2008, I received the Semi Award North America for Development of Strained Silicon Transistors.

16. Since 2005, I have worked as a consultant for leading companies in the semiconductor and computer chip industry, including Applied Materials, Cypress Semiconductor, Qualcomm, SanDisk, and Taiwan Semiconductor. I am the author of over 60 papers and one book related to semiconductors and am a named inventor on over 100 granted patents directed to integrated circuits and transistor structures.

17. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

18. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,245,826 to Jebory et al. (“’826 patent”)
Ex. 1002	Prosecution History of the ’826 patent (downloaded from Patent Center)
Ex. 1004	U.S. Patent Publication No. 2009/0079056 to Conn, filed December 7, 2007, and published March 26, 2009 (“ <i>Conn</i> ”)
Ex. 1005	U.S. Patent Publication No. 2014/0138844 to Gambino et al., filed November 21, 2012, and published May 22, 2014 (“ <i>Gambino</i> ”)

Exhibit	Description
Ex. 1006	U.S. Patent Publication No. 2011/0057319 to Dean et al., filed September 9, 2009, and published March 10, 2011 (“ <i>Dean</i> ”)
Ex. 1007	U.S. Patent Publication No. 2009/0140395 to Davis et al., filed December 4, 2007, and published June 4, 2009 (“ <i>Davis</i> ”)
Ex. 1008	U.S. Patent Publication No. 2012/0104546 to Ding et al., filed November 1, 2010, and published May 3, 2012 (“ <i>Ding</i> ”)
Ex. 1009	U.S. Patent Publication No. 2013/0082382 to Torii, filed September 28, 2012, and published April 4, 2013 (“ <i>Torii</i> ”)
Ex. 1010	U.S. Patent Publication No. 2012/0256310 to Ide, filed April 5, 2012, and published October 11, 2012 (“ <i>Ide</i> ”)
Ex. 1011	U.S. Patent Publication No. 2013/0154108 to Lin et al., filed December 14, 2011, and published June 20, 2013 (“ <i>Lin</i> ”)
Ex. 1012	U.S. Patent No. 8,338,961 to Su et al., filed April 26, 2012, and issued December 25, 2012 (“ <i>Su</i> ”)
Ex. 1013	U.S. Patent Publication No. 2011/0089572 to Tezcan et al., filed September 17, 2010, and published April 21, 2011 (“ <i>Tezcan</i> ”)
Ex. 1014	U.S. Patent No. 6,140,703 to Cronin et al., filed December 26, 1996, and issued October 31, 2000 (“ <i>Cronin</i> ”)
Ex. 1015	U.S. Patent Publication No. 2009/0026619 to Zeng et al., filed July 24, 2007, and published January 29, 2009 (“ <i>Zeng</i> ”)
Ex. 1016	U.S. Patent Publication No. 2011/0018109 to Blaschke et al., filed May 20, 2010, and published January 27, 2011 (“ <i>Blaschke</i> ”)
Ex. 1017	U.S. Patent Publication No. 2010/0252934 to Law et al., filed January 6, 2010, and published October 7, 2010 (“ <i>Law</i> ”)
Ex. 1018	U.S. Patent Publication No. 2013/0334699 to Kuo et al., filed June 19, 2012, and published December 19, 2013 (“ <i>Kuo</i> ”)

Exhibit	Description
Ex. 1019	U.S. Patent No. 8,183,580 to Wang, filed March 2, 2010, and issued May 22, 2012 (“ <i>Wang</i> ”)
Ex. 1020	U.S. Patent Publication No. 2011/0248404 to Chiu et al., filed April 8, 2010, and published October 13, 2011 (“ <i>Chiu</i> ”)
Ex. 1021	U.S. Patent No. 4,946,376 to Sharma et al., filed April 6, 1989, and issued August 7, 1990 (“ <i>Sharma</i> ”)
Ex. 1022	U.S. Patent No. 8,912,091 to Burnham et al., filed January 10, 2013, and issued December 16, 2014 (“ <i>Burnham</i> ”)
Ex. 1023	U.S. Patent No. 8,431,481 to Dunne et al., filed April 11, 2012, and issued April 30, 2013 (“ <i>Dunne</i> ”)
Ex. 1024	U.S. Patent Publication No. 2010/0171226 to West et al., filed December 29, 2009, and published July 8, 2010 (“ <i>West</i> ”)
Ex. 1025	Excerpt of Merriam-Webster's Collegiate Dictionary (11th edition), 2011
Ex. 1026	U.S. Patent Publication No. 2010/0090318 to Hsu et al., filed December 11, 2008, and published April 15, 2010 (“ <i>Hsu</i> ”)
Ex. 1027	U.S. Patent No. 8,455,983 to Wood et al., filed November 22, 2011, and issued June 4, 2013 (“ <i>Wood</i> ”)
Ex. 1028	U.S. Patent Publication No. US2010/0225005 to Nishio et al., filed May 18, 2010, and published September 9, 2010 (“ <i>Nishio</i> ”)
Ex. 1029	U.S. Patent No. 7,939,369 to Farooq et al., filed May 14, 2009, and issued May 10, 2011 (“ <i>Farooq</i> ”)
Ex. 1030	U.S. Patent Application Publication No. US2011/0095435 to Volant et al., filed October 28, 2009, and published April 28, 2011 (“ <i>Volant</i> ”)

V. LEGAL STANDARDS

19. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

20. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

21. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

22. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-20 of the '826 patent from the perspective of a person of ordinary skill in the art at the '826 patent's earliest claimed priority date (March 11, 2013), as described in more detail below.

23. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

24. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

25. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

26. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

27. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications

that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

28. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

29. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter

pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

30. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '826 patent.

31. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is March 11, 2013. My opinions would not change if I assumed a later date of invention.

32. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have

also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

33. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

34. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

35. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the

same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

36. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

37. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

38. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

A. Semiconductor Device Manufacturing

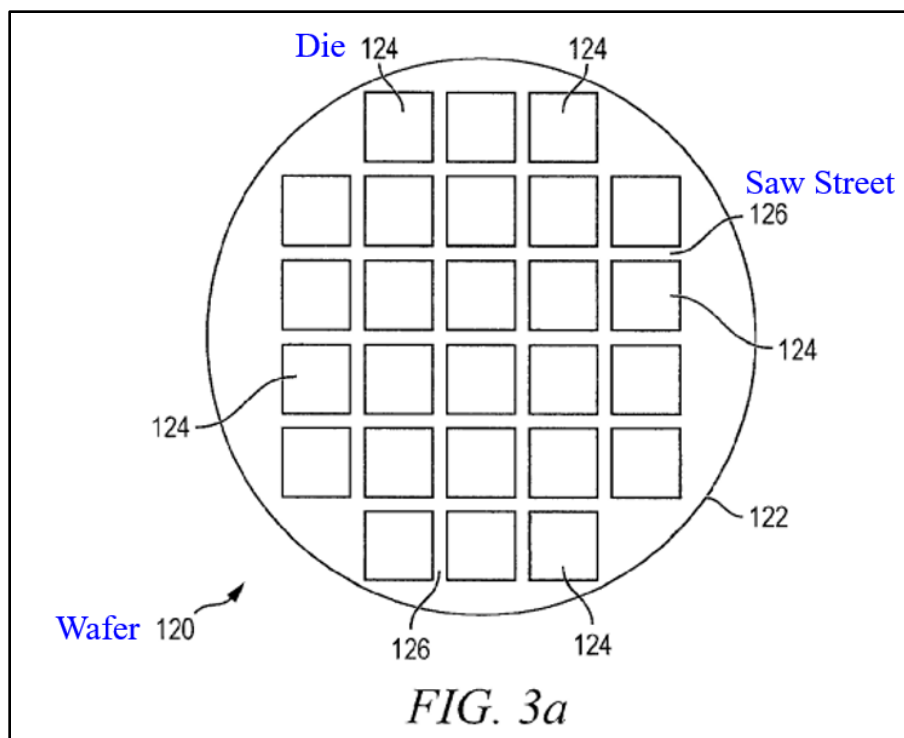
39. Just like houses are built on foundations, semiconductor devices are fabricated on substrates. A semiconductor substrate can be made of single-element semiconductor material such as silicon, or compound semiconductor material such

as gallium arsenide, silicon carbide, etc. *Lin* (Ex. 1011), [0042]. For example, as shown below, “a semiconductor wafer 120 with a base substrate material 122,” such as silicon, serves as the “structural support” for semiconductor devices. *Lin*, [0042]. The wafer 120 is divided into an array of dies 124 by a grid of saw streets 126. *Lin*, [0042]. Cutting tools, e.g., laser or saw blade, can be used to singulate (i.e., cut) the wafer 120 into individual dies 124 along the saw streets 126. *Lin*, [0032], [0042]. Each die can be packaged to form a chip, and is also called a “chip” or “integrated circuit.” The above process is nicely summarized in the literature:

Conventional semiconductor chips are routinely fabricated en masse in large groups as part of a single semiconductor wafer. At the conclusion of the processing steps to form the individual dice, a so-called dicing or sawing operation is performed on the wafer to cut out the individual dice. Thereafter, the dice may be packaged or directly mounted to a printed circuit board of one form or another.

Conventional semiconductor dice are routinely cut out from the wafer as rectangular shapes. By definition, a conventional semiconductor die has four sides and four corners. The dicing operation is a mechanical cutting operation performed with a type of circular saw.

Su (Ex. 1012), 1:47-58.



Lin, Fig. 3a.³

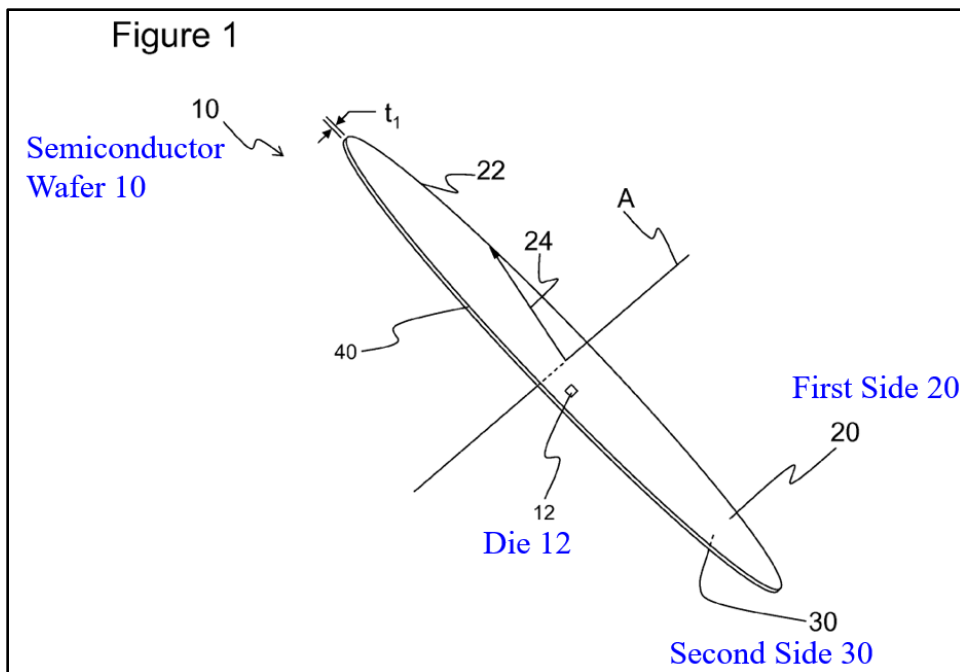
40. Still referring to the above figure, “[e]ach die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits.” *Lin*, [0023]. “Active electrical components,” also called “active devices,” were commonly used in the art to refer to devices that “have the ability to control the flow of electrical current” and are used for converting and supplying electrical power for a circuit. *Lin*, [0023]; *see also Lin*, [0005]. Typical active devices are transistors and diodes. *Lin*, [0023]. And,

³ All figures in this declaration containing color are annotated relative to the original figures in the patent or prior art, and all text in color is added.

“passive electrical components,” also called “passive devices,” are devices that “create a relationship between voltage and current necessary to perform electrical circuit functions,” *Lin*, [0023], and consume the electrical power in the circuit (rather than supplying the power to the circuit). *Lin*, [0005]. Typical passive devices include capacitors, inductors, resistors, and transformers. *Lin*, [0023].

B. Front Side and Backside of Semiconductor Substrate

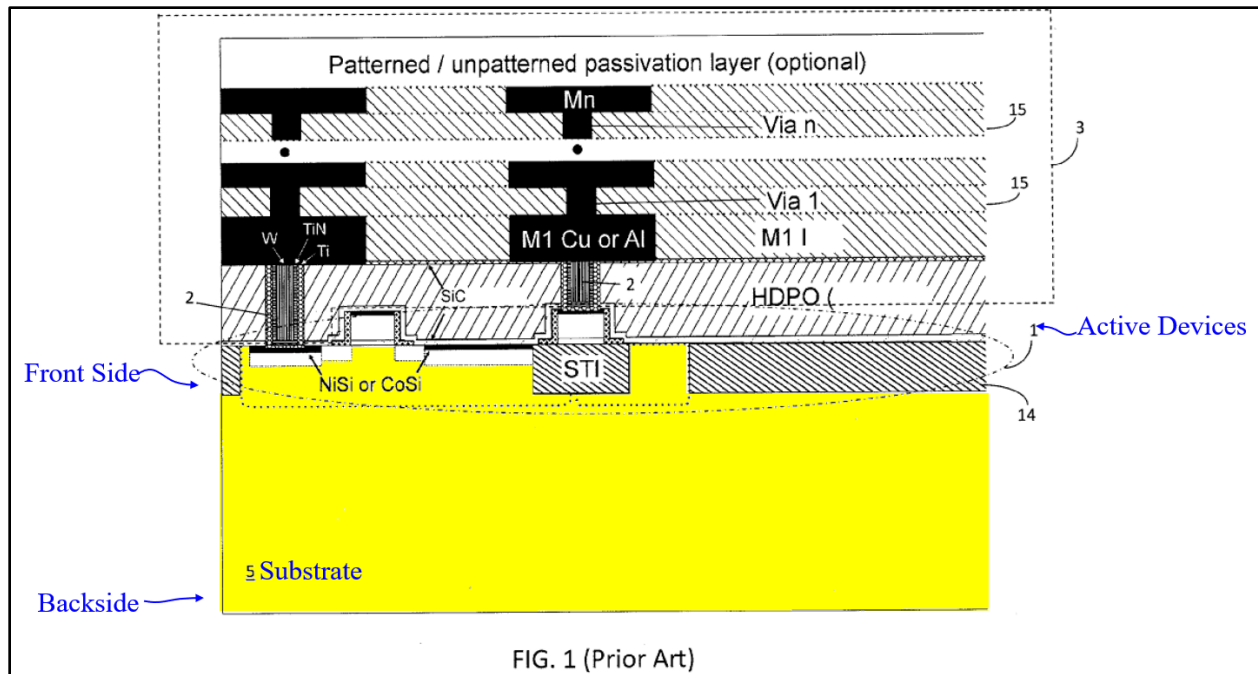
41. As shown below, wafers have a disk-like shape and dies are small pieces cut from the wafers. The wafers/dies are thin plates that have “a first side” and “a second side.” *Wood* (Ex. 1027), 3:22-29 (“The wafer 10 is typically a single crystalline silicon structure but it can be made from any suitable wafer material. The wafer 10 can include a first side 20, a second side 30 spaced from the first side 20 by a first thickness t_1 along an axis A...”). The first and second sides are opposite to each other.



Wood, Fig. 1

42. In the semiconductor industry, “front side” and “backside” are usually used to refer to the two opposite sides of a semiconductor substrate, respectively. *See, e.g., Lin*, [0008] (“both a front side and a backside of a semiconductor die”). But it was understood in the art that “front” and “back,” like “top” and “bottom,” are relative terms and their meanings depend on the context. For example, one reference states that “[t]he terms ‘front’ and ‘back’ are somewhat arbitrary.” *Su*, 6:30-31. I agree with this statement. Indeed, exactly which side of the substrate is referred to by the “front side” and which side of the substrate is referred to by “backside” depend on the specific structures, manufacturing processes, and/or functions of the semiconductor devices at issue. For example, if active devices are formed on the substrate, “[t]he front-side of a substrate [] is the side where the

active devices of a chip [] are located,” and the backside “is the side opposite to the side where the active devices are located.” *Tezcan* (Ex. 1013), [0059]; *see also* *Tezcan*, [0030]. The following figure “shows a prior art example of a CMOS device with a substrate 5, comprising a front-end-of-line 1 comprising active devices, for example transistors.” *Tezcan*, [0006]. In this example, the side of the substrate 5 with the active devices (i.e., the top side of the substrate 5 in the figure) is the front side, and the opposite side (i.e., the bottom side of the substrate 5 in the figure) is the backside. As such, to summarize, when active devices (e.g., transistors, diodes, etc.) are formed on a substrate, the “front side” and “backside” may have specific positional relationships to the active devices. In this example, the process used to fabricate the front side of the substrate is called “front side process,” and the process used to fabricate the backside of the substrate is called “backside process.” The front side process may include steps used for forming the connection wiring for the active devices, whereas the backside process may include steps used for thinning and polishing the substrate backside surface.

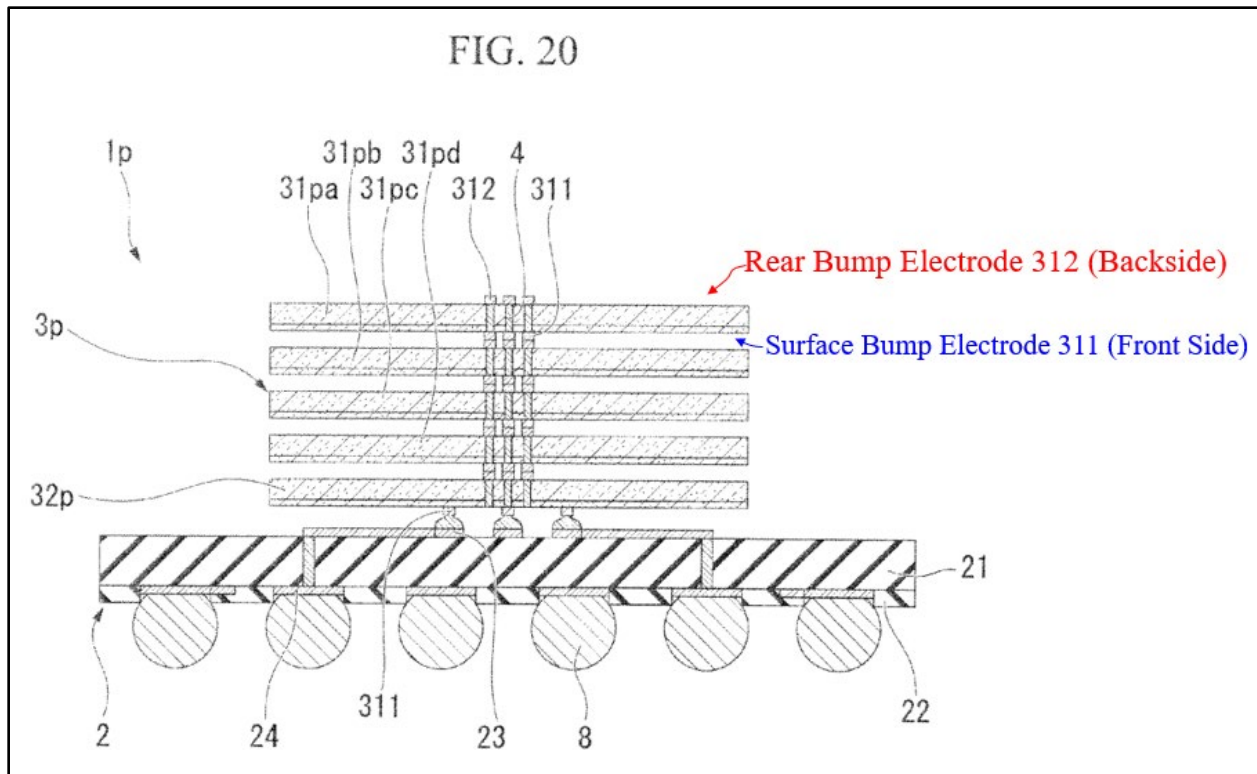


Tezcan, Fig. 1.

43. A semiconductor substrate's front side and backside generally have no relation to the orientation of the substrate. In other words, the front side and backside do not necessarily face up and down, respectively. Rather, sometimes the front side can face down and the backside can face up. For example, during fabrication, the backside may face up to facilitate backside processing. *Torii* (Ex. 1009), [0099] (wafer is held "upside down" to grind the backside surface); *Ide* (Ex. 1010), [0150] ("wafers are upside down ... to process the rear surface"). One such fabrication process is illustrated in *Chiu* (Ex. 1020), which describes that a backside is first facing up to facilitate a "backside grinding" process (Figure 2) and then facing down to facilitate chip packaging (Figure 3). *Chiu*, [0019]-[0021], Figs. 2-3.



Moreover, in final products, the backside may also face up in a “flip chip” configuration to facilitate packaging. *Ide*, [0163]; *Gambino* (Ex. 1005), [0002]; *West* (Ex. 1024), [0026] (“die (or wafer) can be assembled ... bottom side up (i.e. face down)”). One such flip-chip configuration is illustrated in *Ide*’s Figure 20, below, which shows a packaged memory device 1p including a stack of memory chips 31pa, 31pb, 31pc, and 31pd. *Ide*, [0005]-[0006], [0078]. Each of the memory chips has its backside (as indicated by rear bump electrode 312) face up.

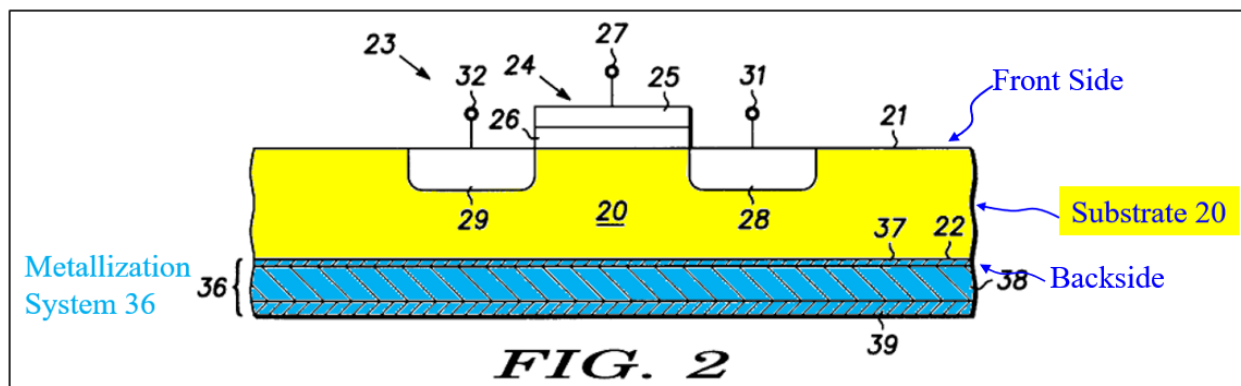


Ide, Fig. 20

C. Backside Metal Layer

44. Metal layer(s) can be formed at the backside of the semiconductor substrate at wafer level (before die singulation) or at die level (after die singulation, e.g., during the packaging process). *Davis* (Ex. 1007), [0005] (“Reliable electrical contact structures often require multiple layers of metal to be formed at the wafer level.”); *Wang* (Ex. 1019), 4:12-21 (“The adhesion of carrier chip 60’ to lead frame 78 may be achieved through thermal interface material (TIM) layer 79, ... In an embodiment, TIM 79 is formed of an organic paste or pure alloy or metal, which can be dispensed onto lead frame 78, and thermal reflowed or cured after carrier chip 60’ is mounted onto lead frame 78.”). The

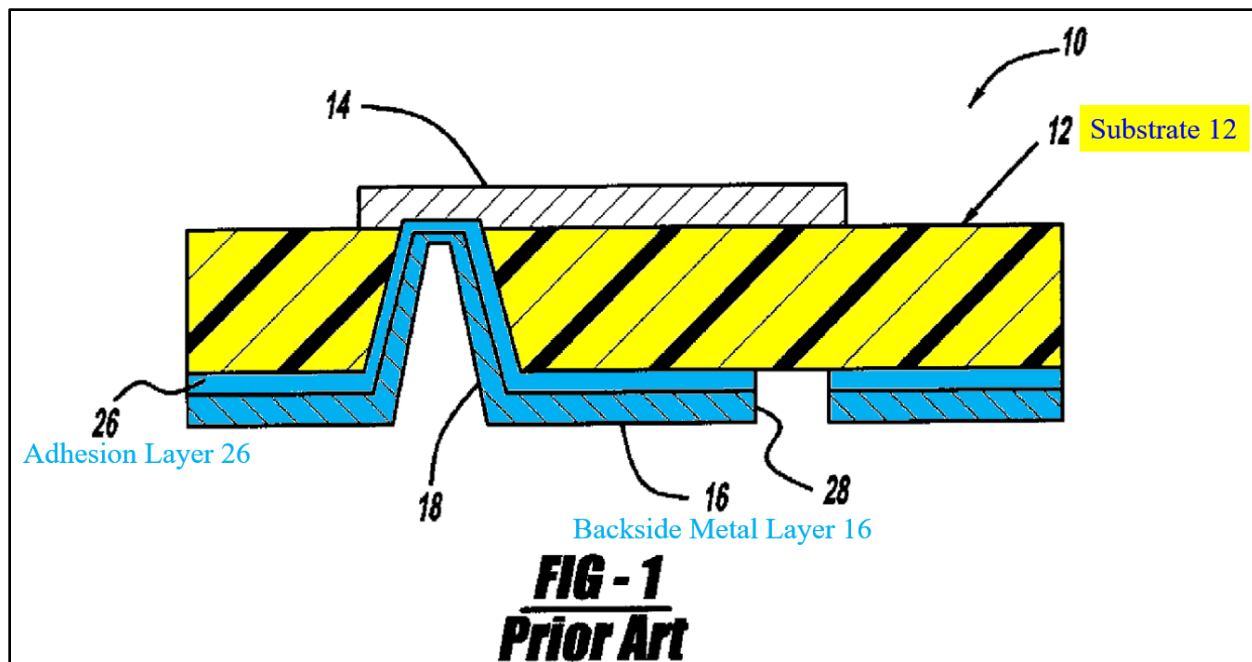
backside metal layer can serve various purposes. For example, “[a]n important use of” the backside metal layer is “to promote bonding of the semiconductor die to a ceramic or a metal structure such as a leadframe.” *Cronin* (Ex. 1014), 1:12-15, 1:25-26. As shown below, “a semiconductor substrate 20 ha[s] a top surface 21 and a bottom surface 22.” *Cronin*, 1:64-66, A “semiconductor device 23,” which may be “a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) having a gate structure 24,” is “formed on top surface 21.” *Cronin*, 2:3-6, And “a metallization system 36 [is] disposed” on bottom surface 22. *Cronin*, 2:22-24, The “metallization system 36 is a three-layer metallization system, wherein each layer is formed using sputter deposition techniques.” *Cronin*, 2:24-27. The three metal layers include “adhesion layer 37,” “barrier layer 38,” and “protective layer 39.” *Cronin*, 2:27-29, 2:42-43, 2:63-64.



Cronin, Fig. 1.

45. As another example, the backside metal layer(s) can serve electrical functions, such as providing “RF, DC and/or ground signals.”⁴ *Zeng*, Abstract; *see also Zeng* (Ex. 1015), [0007]-[0008], [0015]. The following figure “is cross-sectional view of a circuit package 10 including a semiconductor substrate 12 on which is fabricated an integrated circuit 14.” *Zeng*, [0005]. “A backside metal layer 16 is deposited on a backside of the semiconductor substrate 12.” *Zeng*, [0005]. “The backside metal layer 16 is electrically coupled to the integrated circuit 14 by a metallized via 18 extending through the substrate 12.” *Zeng*, [0005]. Moreover, an adhesion layer 26 is also disposed on the backside “to reduce backside metal layer peeling.” *Zeng*, [0006]. The adhesion layer 26 is made of metal material such as “titanium (Ti), titanium/platinum (Ti/Pt), chromium and nickel valadium,” so it is also a backside metal layer. *Zeng*, [0006].

⁴ “RF” was commonly used in the art to stand for “radio frequency,” and “DC” was commonly used in the art to stand for “direct current.”



Zeng, Fig. 1.

D. Via Structures

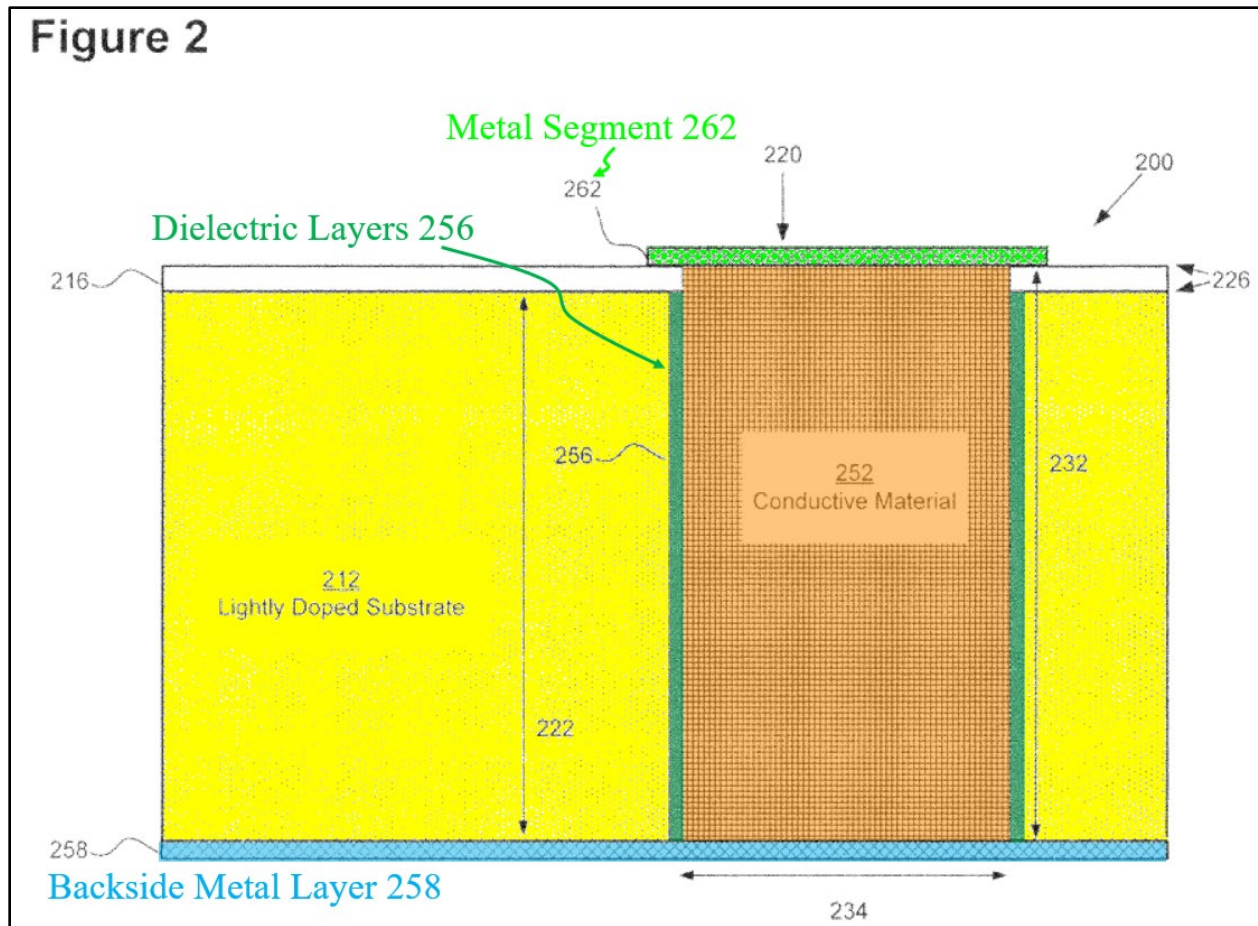
46. As shown in the above figure, a via structure 18 is used to allow electrical connection between the front-side integrated circuit 14 and backside metal layer 16. Zeng, [0005]. In fact, it was well known that via structures had been widely used in the art to provide electrical and non-electrical functions.

1. Electrical Functions

47. As to the electrical functions, through silicon vias (TSVs), also called through wafer vias (TWVs) in the art, had been used to provide electrical connections along the vertical direction, e.g., connecting devices on the front side of the substrate to the backside metal layer. For example, the following figure “shows conventional through-wafer via (TWV) 220 in exemplary semiconductor

die 200.” *Blaschke* (Ex. 1016), [0022]. The TWV 220 is surrounded by a substrate 212 and used for connecting a “backside metal layer 258” to a “metal segment 262 situated over TWV 220.” *Blaschke*, [0022]. A “dielectric layer 216” is disposed on the front side of the substrate 212. *Blaschke*, [0022]. An active device (not shown), e.g., a bipolar junction transistor (BJT), is connected to the TWV 220 via the overlaying metal segment 262. *Blaschke*, [0022].

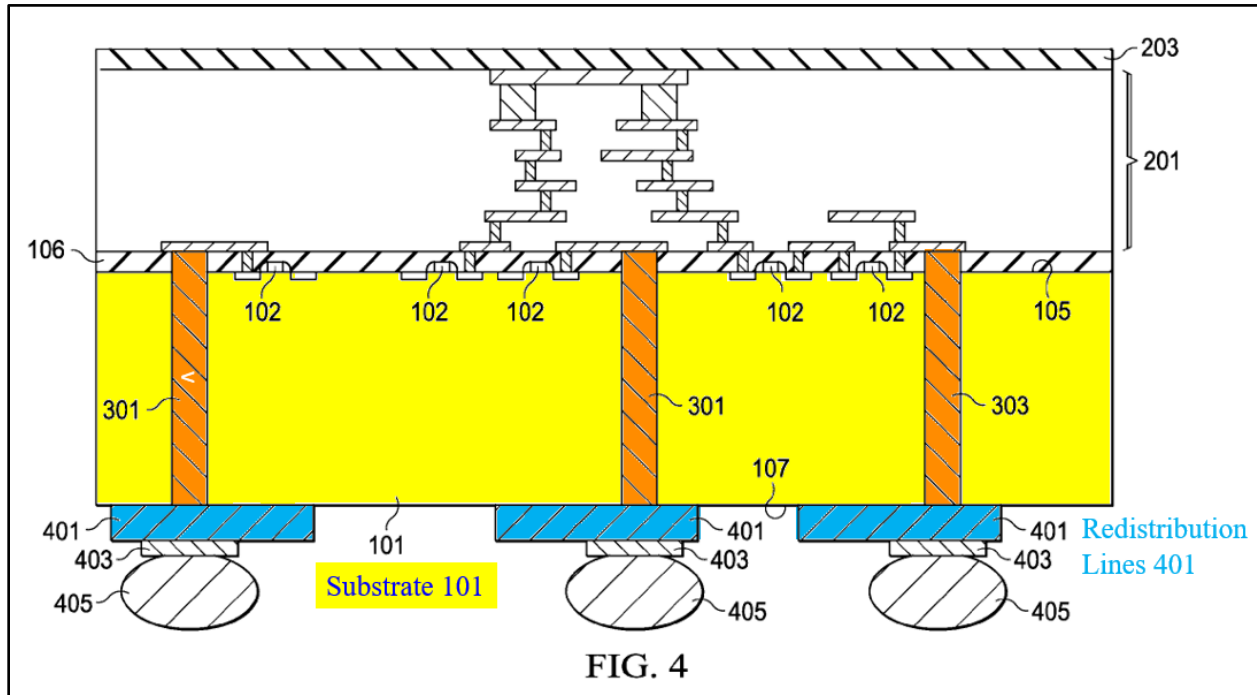
“TWV 220 includes sidewall dielectric layers 256 surrounding conductive plug 252, which can be made of a highly conductive material such as copper or gold.” *Blaschke*, [0022]. “TWV 220 creates a low resistance ground path” between the active device (not shown) and the backside metal layer 258. *Blaschke*, [0023].



Blaschke, Fig. 2.

48. As another example, the following figure shows “a semiconductor die with I/O connections routed to the back side of the semiconductor die in a system-on-chip configuration.” *Law* (Ex. 1017), [0018]. Specifically, signal vias 301 and power/ground (P/G) vias 303 are formed through a substrate 101 and connected to redistribution lines 401 on the backside of the substrate 101. *Law*, [0019], [0031]-[0032]. “The redistribution lines 401 comprise at least one conductive layer formed of a metal such as aluminum, copper, tungsten, titanium, and combinations

thereof,” and therefore constitute backside metal layers. *Law*, [0032]; *see also Law*, [0033].

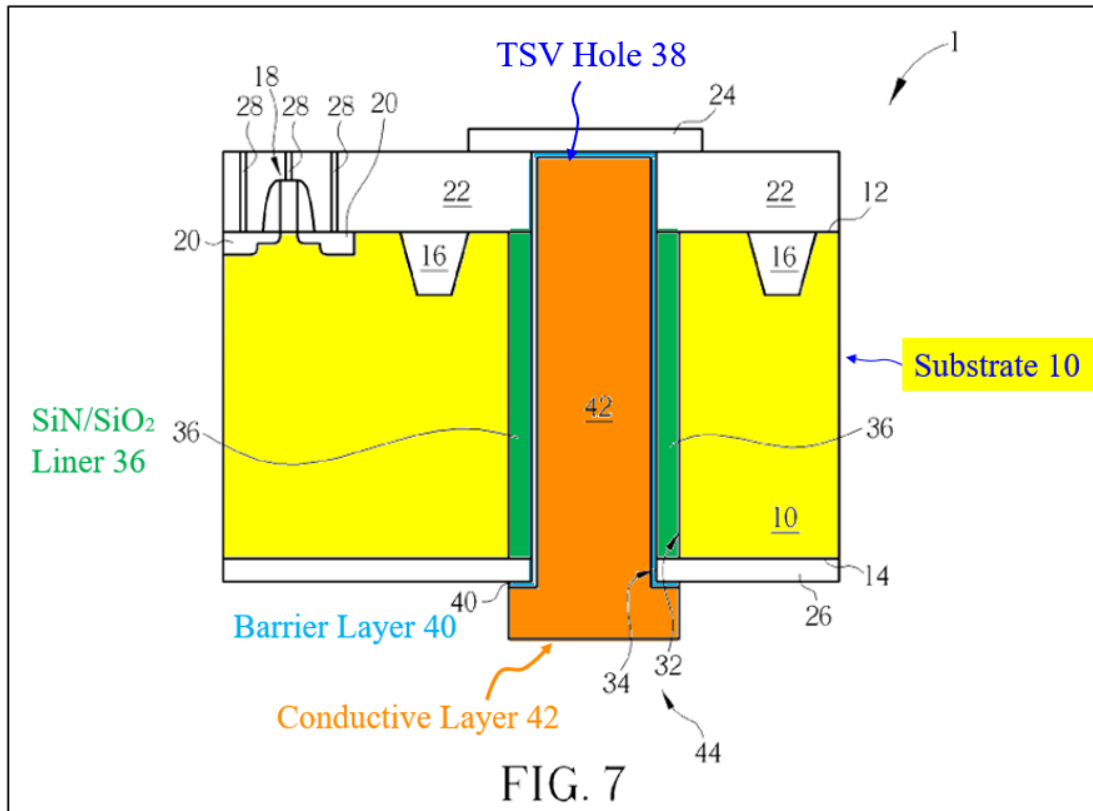


Law, Fig. 4.

49. As yet another example, the following figure shows a TSV hole 38 in a substrate 10. *Kuo* (Ex. 1018), [0022]. “[A] liner 36 [is] disposed on the substrate sidewall 32” of the TSV hole 38, and made of insulating material “such as SiN or SiO₂.” *Kuo*, [0021]-[0022]. “[A] barrier layer 40 is selectively formed in the TSV hole 38” and extends to the backside of the substrate 10. *Kuo*, [0022]. “[T]he barrier layer 40 includes Ti, TiN, Ta or TaN,” and thus the portion of the barrier layer 40 extending on the backside constitutes a backside metal. *Kuo*, [0022]. “[A] conductive layer 42 is [] formed in the TSV hole 38 and on the back surface 14,” such that the conductive layer 42 forms a protruding portion extending from the

back surface 14 and contacting the barrier layer 40 (i.e., the backside metal layer).

Kuo, [0022].

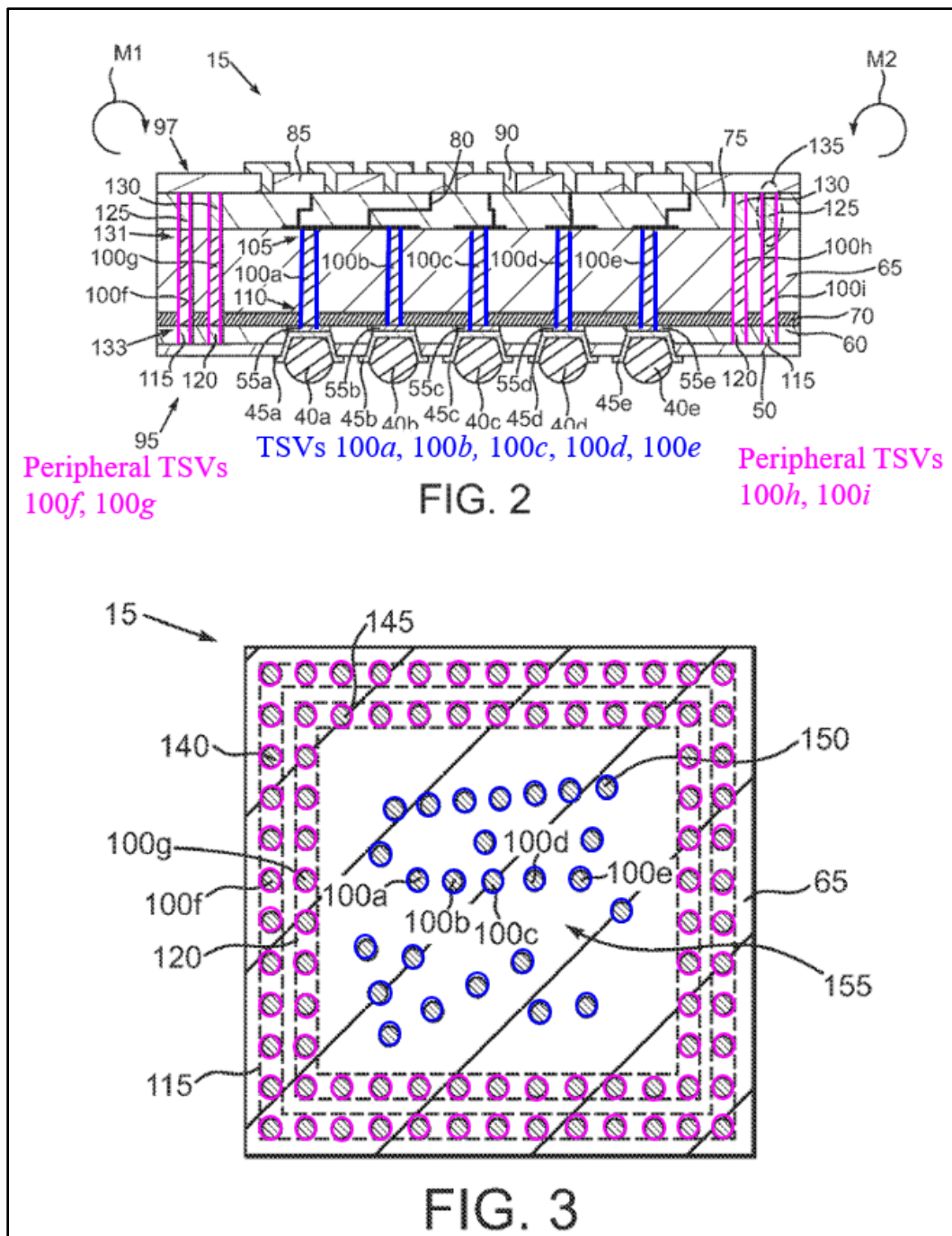


Kuo, Fig. 7.

2. Non-Electrical Functions

50. Regarding the non-electrical functions, via structures had been used to improve the structural integrity of the wafer or die. For example, as shown in the following cross-sectional view (Figure 2) and backside plan view (Figure 3), a semiconductor chip 15 (i.e., a die) includes traditional TSVs (represented by 100a, 110b, 100c, 100d, 100e) located in a central region of the chip, and peripheral TSVs (represented by 100f, 110g, 100h, 100i) in a peripheral region. *Su*, 6:1-14.

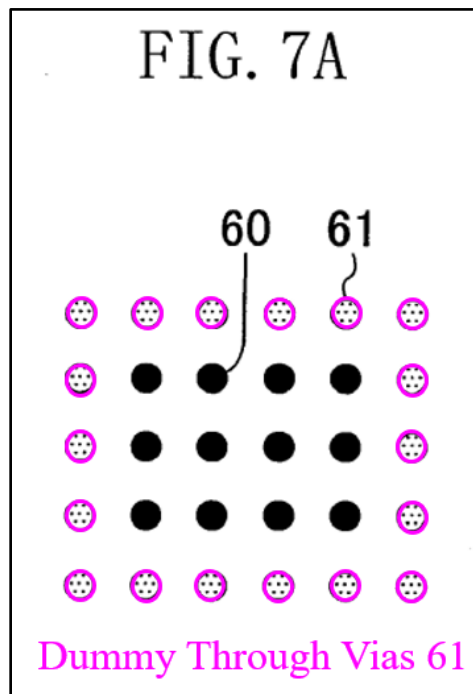
The traditional TSVs serve the traditional functions for providing electrical connections, whereas the peripheral TSVs perform non-electrical functions such as to “stiffen the semiconductor chip 15 and resist bending due to” thermal cycling, or to serve “a crack stop role in that the TSVs provide interspersed barriers to crack propagation towards an interior portion 155 of the semiconductor chip 15.” *Su*, 6:1-8, 6:60-64, 7:33-37.



Su, Figs. 2-3.

51. As another example, in the following illustrated plan view of a semiconductor device, a via group is formed, in which “a plurality of through vias (true through vias) 60 used for electrical connections are disposed at the center

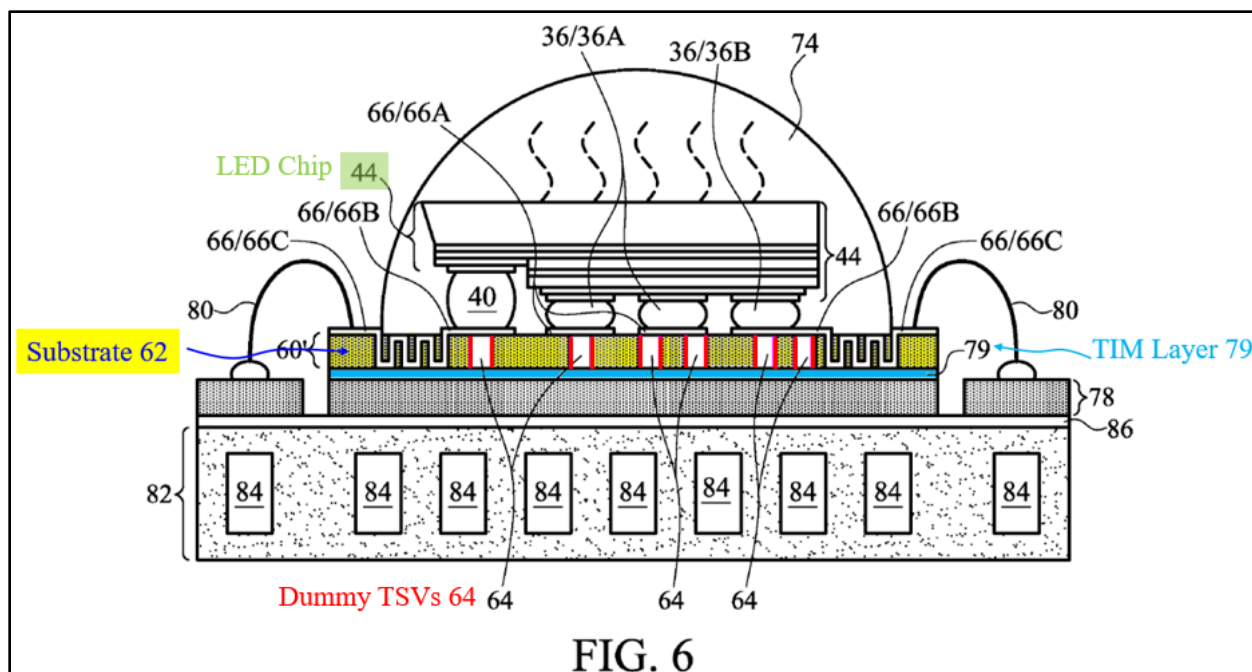
portion of the via group, while dummy through vias 61 not electrically connected to the wires in the semiconductor device are disposed at a peripheral portion of the via group.” *Nishio* (Ex. 1028), [0096]. “[I]n the case of causing a shape failure resulting from a process at the peripheral portion of the via group through the adjustment of process conditions, the occurrence of a problem such as a shape failure in the true through via can be prevented by disposing the dummy through via at the peripheral portion, i.e., by not disposing the true through via at the peripheral portion.” *Nishio*, [0027]. This way, “it is possible to improve the reliability of the true through via.” *Nishio*, [0027].



Nishio, Fig. 7A.

52. Via structures had also been used to dissipate heat generated by semiconductor devices. For example, the following figure illustrates a “carrier

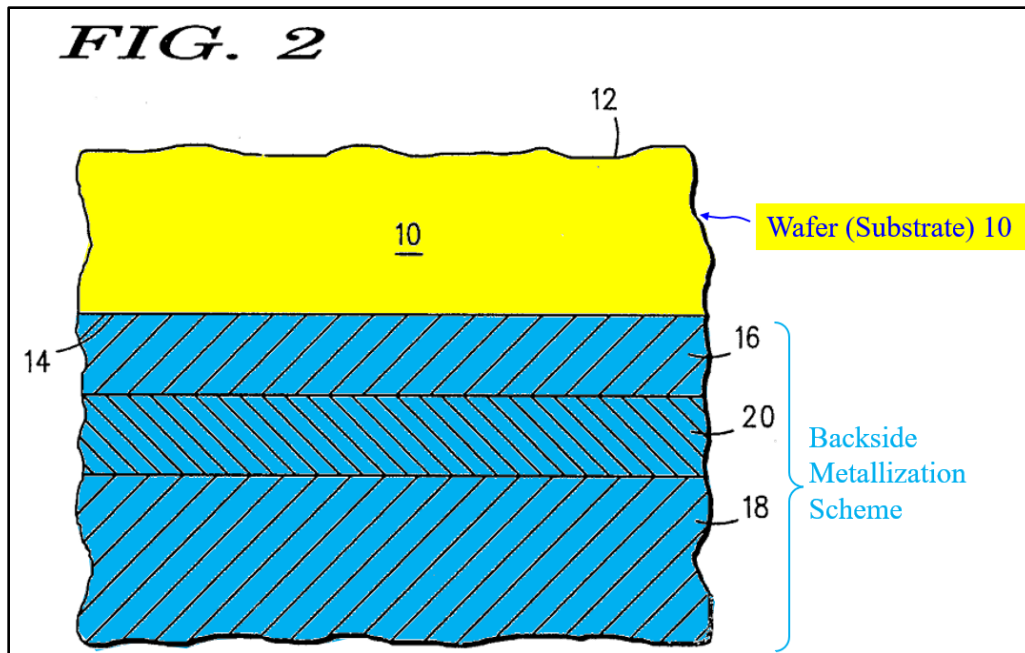
chip 60' being bonded to at least one LED chip 44.” *Wang*, 3:64-67. The carrier chip 60' includes a substrate 62 with multiple dummy TSVs 64 formed therein. *Wang*, 3:14-19. “TSVs 64 are dummy TSVs since they are not used to conduct [electrical] currents, although voltages may be applied thereon.” *Wang*, 3:23-24. Rather, “dummy TSVs 64 ... have the function of dissipating heat.” *Wang*, 3:25-27. Dummy “TSVs 64 may be formed of copper or other metals, such as tungsten, or alloys thereof.” *Wang*, 3:19-20. The carrier chip 60' is adhered to a lead frame 78 “through thermal interface material (TIM) layer 79.” *Wang*, 4:12-15. The TIM layer 79 may be made of “pure alloy or metal, which can be dispensed onto lead frame 78, and thermal reflowed or cured after carrier chip 60' is mounted onto lead frame 78.” *Wang*, 4:17-21. The TIM layer thereby serves as a layer to adhere the bottom side of the carrier chip 60'to the lead frame. Here, the bottom side of carrier chip 60' is opposite to the side where the LED chip 44 (i.e., the active device) is located, thereby constituting the backside of the substrate 62. *Supra*, §VI.B. Hence, the TIM layer 79 constitutes a backside metal layer.



Wang, Fig. 6.

E. Via Structures to Improve Backside Metal Layer Adhesion

53. It is desirable to ensure the backside metal layer firmly adheres to the substrate. *Cronin*, 4:4-6 (“the [backside] metallization system provides good adhesion to the substrate”); *Zeng*, Abstract (“the metal layer is firmly secured to the substrate, and resists peeling”). The quest for good adhesion dated back to at least 1980s, and the early effort focused on modifying the sub-layer structure and/or material composition of the backside layer. *See, e.g., Sharma* (Ex. 1021), Abstract (adding “a vanadium layer” and/or “[a]n optional intermediate layer” into a backside metal layer to improve adhesion).



Sharma, Fig. 1.

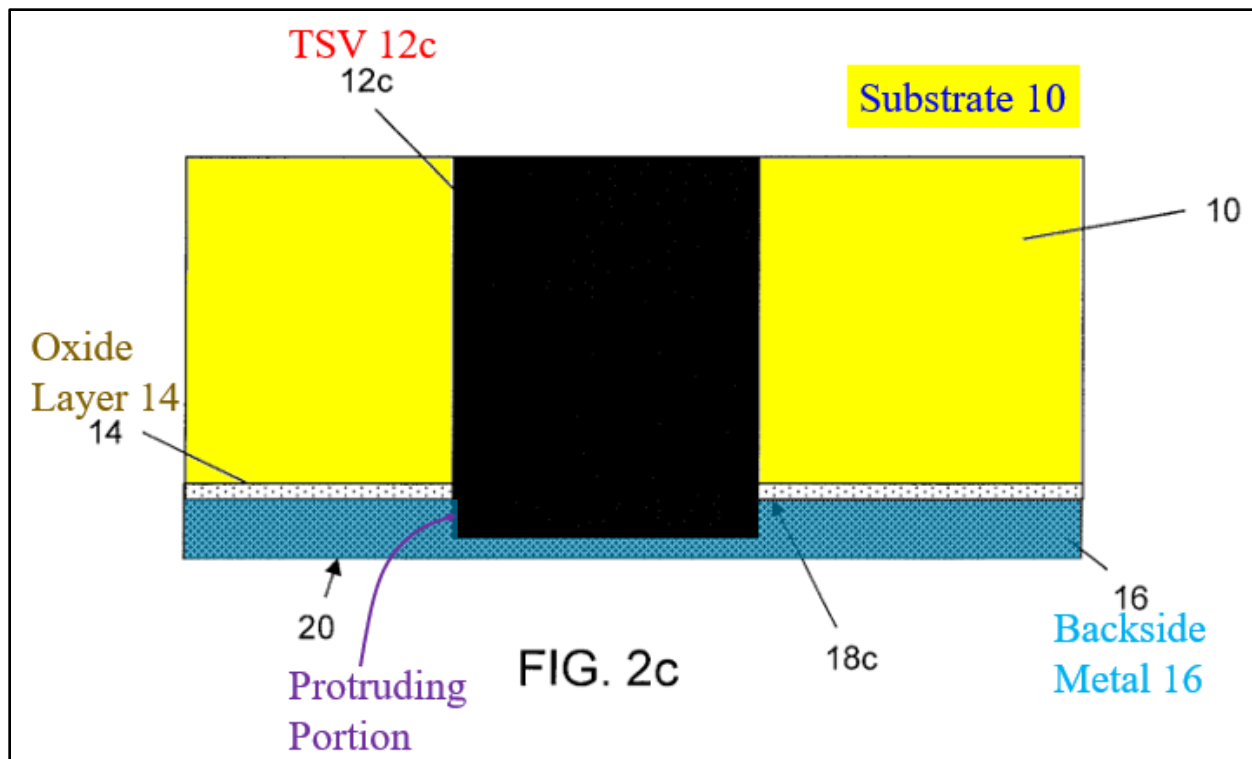
54. With the wide usage of via structures, including the TSVs or TWVs, those skilled in the art had also used them to improve adhesion. For example, the following “FIG. 3 shows a packaged module with a backside metal ground plane [16] attached to a substrate [10].” *Burnham* (Ex. 1022), 5:14-16. The substrate 10 includes a TSV 12 forming “electrical communication with” a device 100 fabricated in the substrate. *Burnham*, 5:19-21. The details of the connection portion between the TSV 12 and backside metal 16 are illustrated in Figure 2c. *Burnham*, 2:15-17. It shows that an oxide layer 14 is disposed between the substrate 10 and the backside metal 16 to “provide improved metal adhesion of the backside metal 16 ... compared to conventional devices in which the backside metal 16 is formed directly on the backside of the Si wafer...” *Burnham*, 5:8-13; *see also*

Burnham, Fig. 2c. This way, “[t]he TSV 12 is ... in [both] mechanical and electrical communication with the backside metal 16.” *Burnham*, 5:24-26.



Burnham, Figs. 2c and 3.

Notably, the structure in Figure 2c uses both the oxide layer (as an intermediate adhesion layer) and the TSV to improve the adhesion of the backside metal adhesion to the substrate, indicating that those skilled in the art had been combining different methods to solve the backside metal adhesion problem.



Burnham, Figs. 2c.

F. Summary

55. In summary, before the time of the '826 patent, it was well-known that:

- (i) improving backside metal layer adhesion to the semiconductor substrate is important and desirable (§VI.C);
- (ii) via structures can serve non-electrical functions (e.g., *Wang's* dummy vias not providing ground connection to active devices) and may be disposed at the peripheral regions of the semiconductor substrate (e.g., *Su's* peripheral TSVs) (§VI.D.2); and

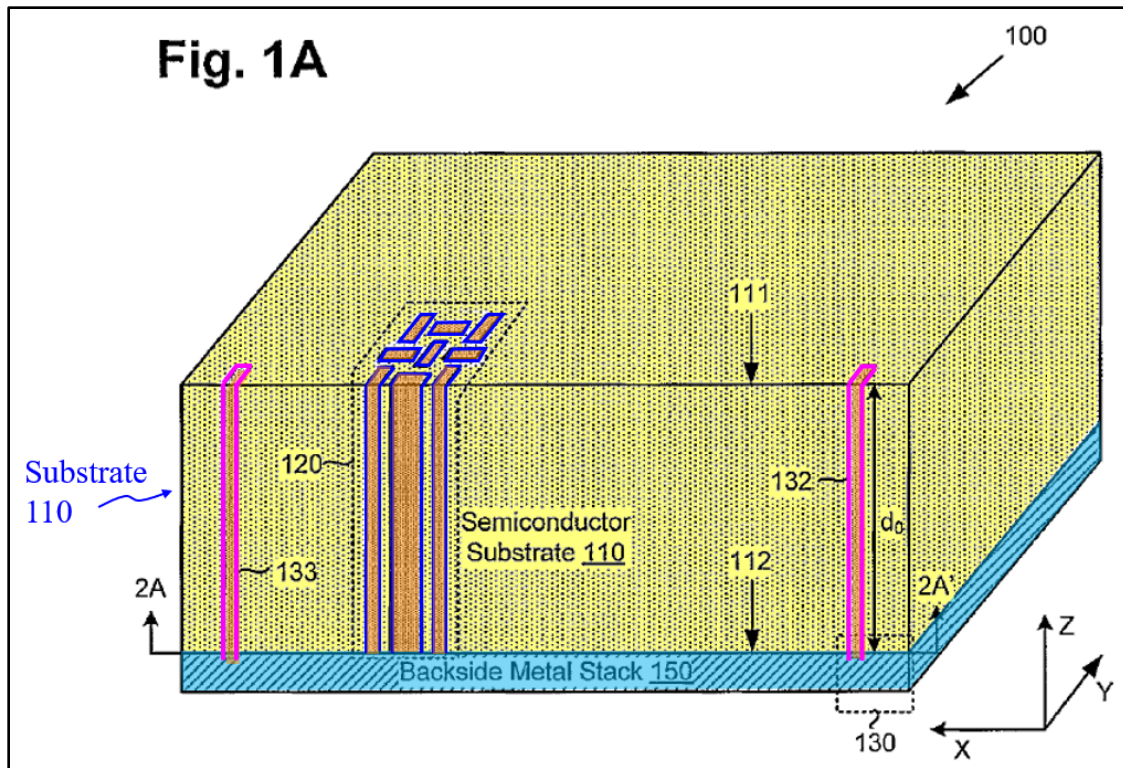
- (iii) the via structures can be used to improve backside metal adhesion by forming a protruding portion to be bonded with the backside metal (§VI.E).

56. Accordingly, in my opinion, before the time of the '826 patent, the art already possessed all the elements that were needed to make the claimed “anchor vias for improved backside metal adhesion to semiconductor substrate.” '826 patent, title.

VII. THE '826 PATENT

A. Alleged Invention of the '826 Patent

57. The '826 patent “is directed to anchor vias for improved backside metal adhesion to a semiconductor substrate.” '826 patent, 1:42-46. Figure 1A shows a semiconductor device 100 including a semiconductor substrate 110 that has a front side surface 111, and a backside surface 112. '826 patent, 2:56-60. There are two types of vias formed in semiconductor substrate 110 — (1) a [group 120 through silicon vias \(TSVs\)](#) used for providing electrical ground connection to active devices and formed in a core region of semiconductor substrate 110, and (2) [anchor vias 132, 133](#) used for improving [backside metal](#) adhesion and formed in a peripheral region of semiconductor substrate 110. '826 patent, 2:53-56, 2:65-66, 3:2-11.



'826 patent, Fig. 1A.

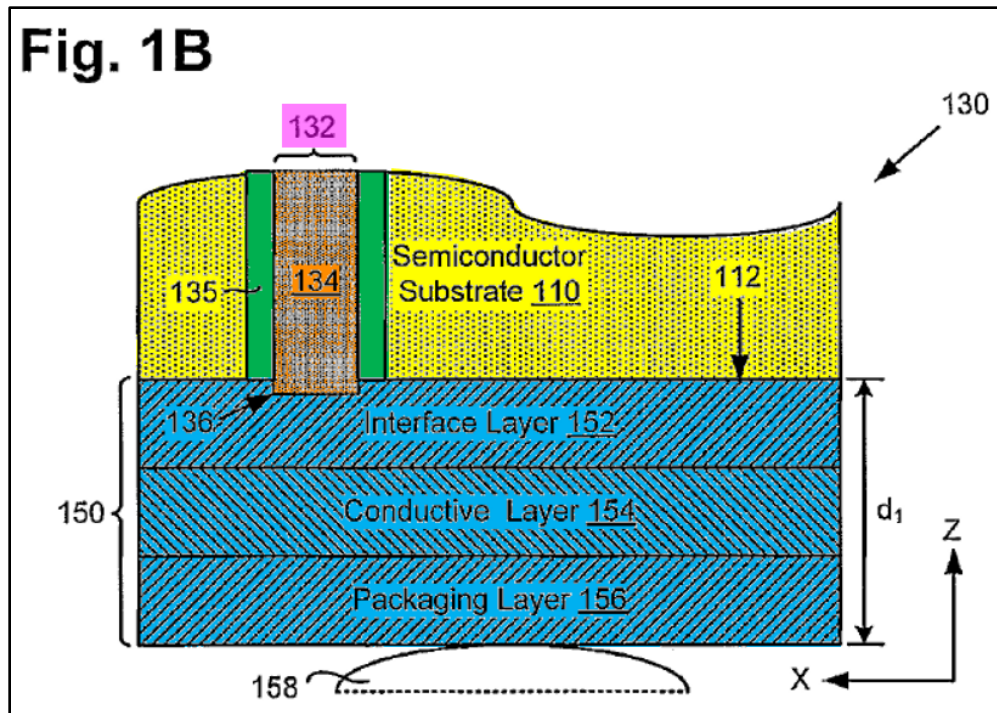
58. The TSV group 120 and anchor vias 132, 133 all have metal fillers, but they serve different purposes. '826 patent, 3:5-17. Specifically, the “[m]etal filler within group 120 of TSVs provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110 and may be electrically connected to an overlying metal layer ... for grounding active devices.”⁵ '826 patent, 3:5-11. “By contrast, [the] metal filler within anchor vias 132 and 133 does not provide ground connection to any active

⁵ An example of the overlying metal layer (not illustrated in the '826 patent) is the overlying metal segment 262 in Figure 2 of *Blaschke. Supra*, §VI.D.1.

devices and instead provides physical anchor points between semiconductor substrate 110 and the underlying [backside metal stack 150](#).” ’826 patent, 3:12-17.

“In addition, the [metal filler](#) within [anchor vias 132 and 133](#) may either not contact a front side metal layer, or if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the [metal filler](#) within [anchor vias 132 and 133](#) essentially has a floating voltage potential during operation.” ’826 patent, 3:21-27. Also, unlike the [TSV group 120](#), [anchor vias 132, 133](#) do not need to be through the entire substrate, but rather may be formed to a certain depth into the substrate. ’826 patent, 3:17-21.

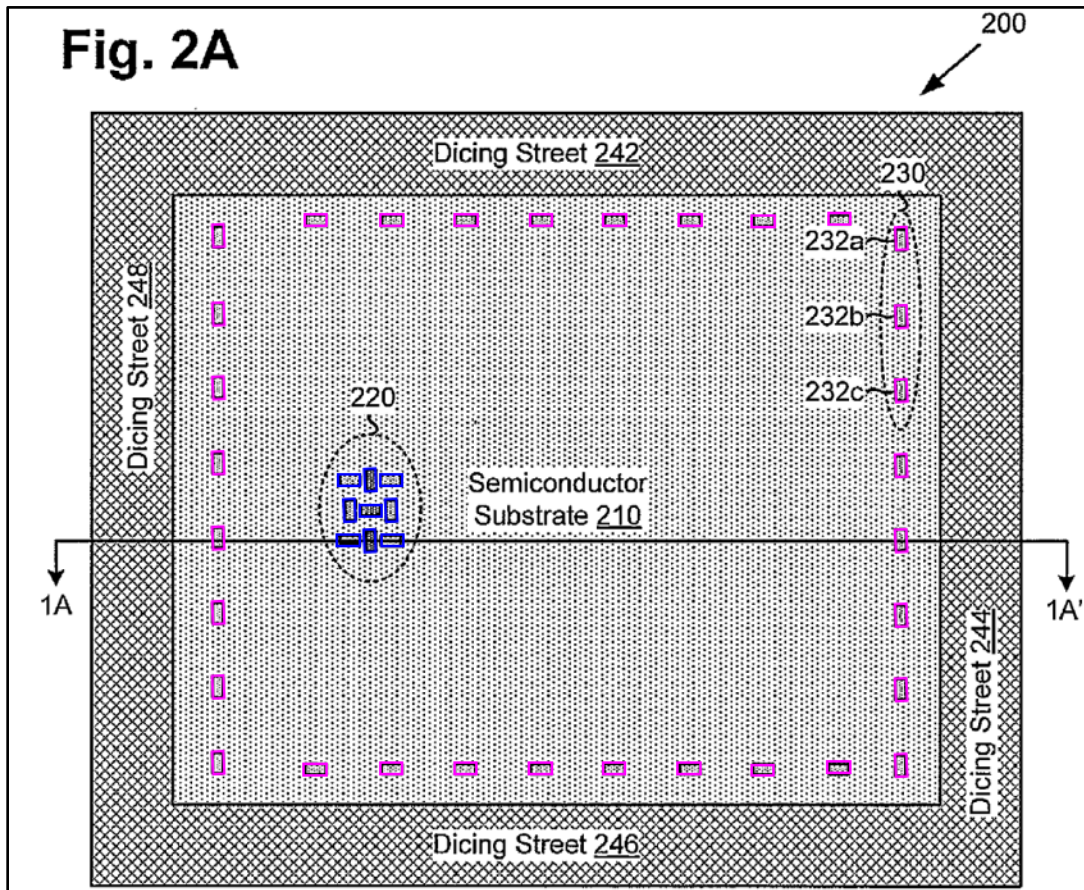
59. Figure 1B, below, provides a magnified cross-sectional view of the anchor points 130 of [anchor via 132](#). ’826 patent, 3:32-38. As shown, “[metal filler 134](#) may protrude from bottom side 112 to form protruding portion 136” to “form a very strong physical, metal-on-metal bond” with the [backside metal stack 150](#). ’826 patent, 3:43-48. “[Insulating layer 135](#) may optionally be formed within [anchor via 132](#)” and “may be a dielectric layer such as silicon dioxide, for example.” ’826 patent, 3:38-43. The [backside metal stack 150](#) “includ[es] one or more of [interface layer 152](#), [conductive layer 154](#), and/or [packaging layer 156](#).” ’826 patent, 3:65-67.



'826 patent, Fig. 1B.

60. Figure 2A, below, provides a backside plan view of a semiconductor device. '826 patent, 4:7-10. In this embodiment, a TSV group 220 (similar to the ground-connecting TSV group 120 in Figure 1A) is formed in an interior region of a semiconductor substrate 210, whereas multiple anchor vias 232 are formed “along the edges and in the corners of [the] semiconductor substrate.” '826 patent, 4:19-25. Fig. 2A. Figure 2A also shows dicing streets 242, 244, 246, and 248, “which delineate portions of the semiconductor substrate ... to singulate semiconductor substrate 210 into a semiconductor die.” '826 patent, 4:29-33. The use of the anchor vias can prevent the “backside metal stack [from]

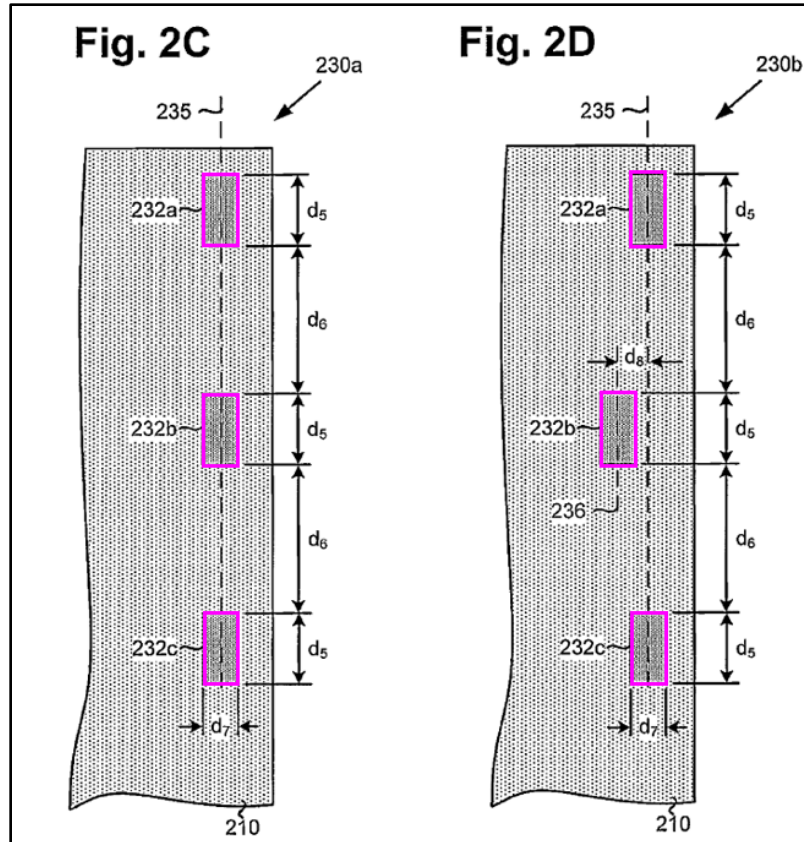
peeling from the edges and/or corners of the substrate” during the singulation. ’826 patent, 4:33-36.



’826 patent, Fig. 2A.

61. The ’826 patent states that “[b]ecause forming each via requires the removal of the semiconductor material at that location, forming too many vias too close together may result in an undesirable perforating effect within the semiconductor substrate, thus forming a cleavage plane.” ’826 patent, 4:53-57. To solve this problem, the anchor vias can be arranged in certain ways and in certain densities. ’826 patent, 4:57-67. Figures 2C shows an embodiment in which the

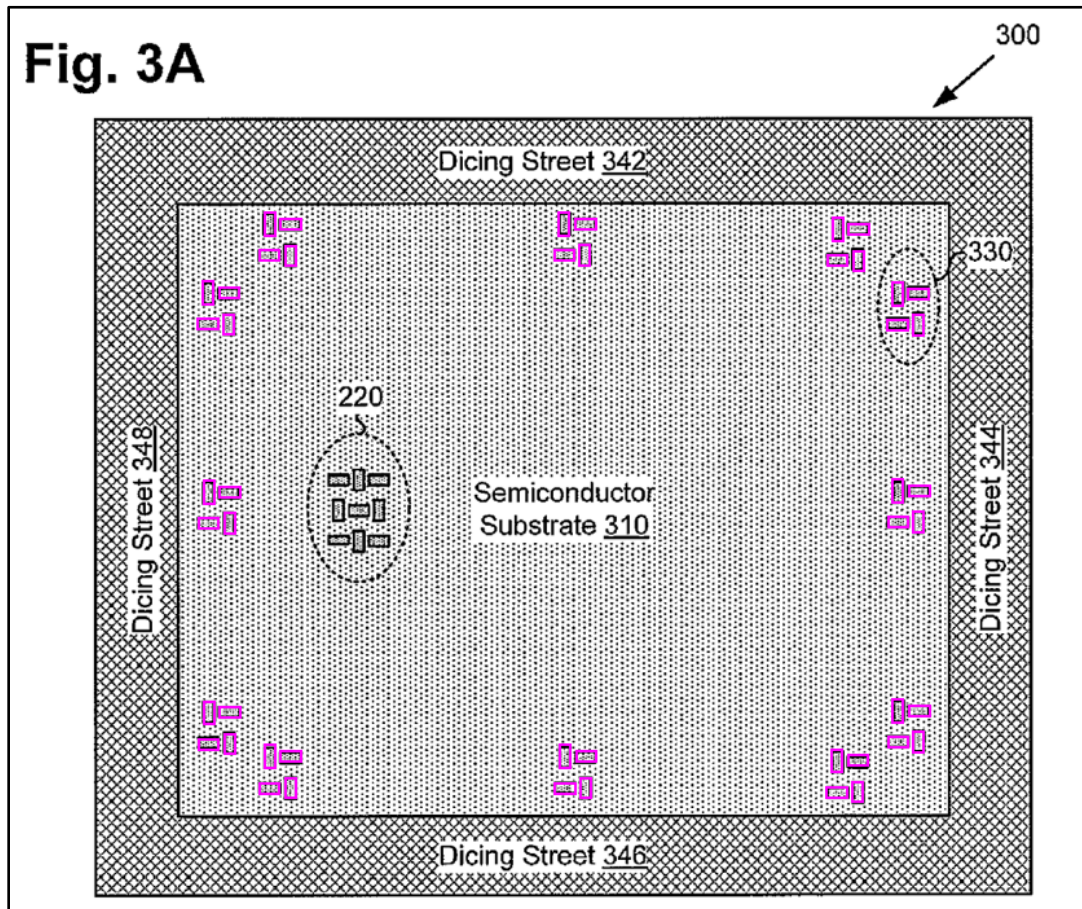
anchor vias 232 are “formed in the periphery of semiconductor substrate 210 along a straight line.” ’826 patent, 5:14-17. “[A] linear density of less than 10% may be” used for these anchor vias 232, to achieve a balance of “avoiding formation of undesirable cleavage planes in semiconductor substrate 210, while still preventing peeling of the backside metal stack.” ’826 patent, 5:29-33. Figures 2D shows an alternative embodiment in which the anchor vias 232 are “disposed in a staggered configuration” to further prevent cleavage. ’826 patent, 5:38-42.



’826 patent, Figs. 2C and 2D.

62. Moreover, the ’826 patent states that spreading too many anchor vias around the periphery of the chip “may adversely affect RF performance.” ’826

patent, 5:62-65. To alleviate this problem, as shown in the backside plan view in Figure 3A, the **anchor vias** can be grouped in clusters and only disposed at selected locations on the substrate. '826 patent, 6:7-25.



'826 patent, Fig. 3A.

63. All of the features regarding the anchor vias described in the '826 patent were already well-known in the art (*supra*, §VI.F) and, as explained below, had already been disclosed or rendered obvious by *Conn*, *Gambino*, *Torii*, *Ide*, and/or the other cited references.

B. Challenged Claims

64. I understand that claims 1-20 of the '826 patent are being challenged in this proceeding. Among them, claims 1-10 recite a semiconductor device structure, and claims 11-20 recite a method for manufacturing the semiconductor device structure.

65. In my opinion, claims 11-20 are substantially similar to claims 1-20, respectively. The following table demonstrates the similarity between claims 1-10 and claims 11-20, with identical language italicized.

Claim 1	Claim 11
[1pre] <i>A structure comprising:</i>	[11pre] <i>A method comprising:</i>
[1a] <i>at least one anchor via disposed in at least one corner of a semiconductor substrate;</i>	[11a] <i>forming at least one anchor via in at least one corner of a semiconductor substrate;</i>
[1b] <i>a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;</i>	[11b] <i>depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;</i>
[1c] <i>a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;</i>	[11c] <i>forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;</i>
[1d] <i>wherein said metal filler within said at least one anchor via does not provide ground connection to one or</i>	[11d] <i>wherein said metal filler within said at least one anchor via does not provide ground connection to one or</i>

Claim 1	Claim 11
<i>more active devices in said semiconductor substrate.</i>	<i>more active devices in said semiconductor substrate.</i>

Claim 2	Claim 12
<i>[2a] The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.</i>	<i>[12a] The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.</i>

Claim 3	Claim 13
<i>[3a] The structure of claim 2, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.</i>	<i>[13a] The method of claim 12, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.</i>

Claim 4	Claim 14
<i>[4a] The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a straight line along a periphery of said semiconductor substrate.</i>	<i>[14a] The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate.</i>

Claim 5	Claim 15
<i>[5a] The structure of claim 4, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said</i>	<i>[15a] The method of claim 14, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said</i>

Claim 5	Claim 15
<i>straight line along said periphery of said semiconductor substrate.</i>	<i>straight line along said periphery of said semiconductor substrate.</i>

Claim 6	Claim 16
<i>[6a] The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.</i>	<i>[16a] The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.</i>

Claim 7	Claim 17
<i>[7a] The structure of claim 1, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.</i>	<i>[17a] The method of claim 11, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.</i>

Claim 8	Claim 18
<i>[8a] The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.</i>	<i>[18a] The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of: forming an interface layer; forming a conduction layer; forming a packaging layer.</i>

Claim 9	Claim 19
[9a] <i>The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.</i>	[19a] <i>The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate.</i>

Claim 10	Claim 20
[10a] <i>The structure of claim 1, further comprising an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via.</i>	[20a] <i>The method of claim 11, further comprising forming an insulating layer between said semiconductor substrate and said metal filler in said at least one anchor via.</i>

C. Prosecution History

66. I have reviewed the prosecution history of the '826 patent. I understand that the '826 patent was filed January 27, 2014, as U.S. Patent Application No. 14/165,377 and claims priority to U.S. provisional application no. 61/776,063, filed March 11, 2013. '826 patent, p. 1. During prosecution, the examiner issued only one Office Action, rejecting the independent claims and some of the dependent claims as obvious based in part on U.S. Patent No. 8,431,481 (*Dunne*, Ex. 1023). Ex. 1003, 59-66. The examiner found the other dependent claims allowable. Ex. 1003, 65. In response, the applicant did not rewrite the Examiner's acknowledged subject matter into independent form, but rather amended both independent claims 1 and 11 to add the limitation "wherein

said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.” Ex. 1003, 73-85. The applicant conceded that *Dunne* discloses a TSV forming a protruding portion to bond with a backside metal layer, but argued that *Dunne*’s TSV is used for providing a low resistance ground connection and hence does not disclose the amended claims. Ex. 1003, 82-83.

67. The examiner then allowed the application, without giving a statement for Reasons for Allowability. Ex. 1003, 88-92.

D. Claim Construction

68. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1003). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope

may be provided in the patent's written description, the patent's prosecution history, or both.

69. I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art (POSA) in the relevant time period.

70. I have been asked to consider whether independent method claim 11 requires steps [11b] and [11c] therein to be performed in their recited order. Specifically, claim 11 recites, in part:

- [11a] "forming at least one anchor via in at least one corner of a semiconductor substrate;"
- [11b] "depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;" and
- [11c] "forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via."

'826 patent, 8:35-43. I have reviewed the '826 patent (Ex. 1001) and its prosecution history (Ex. 1003), and I did not find anything that limits claim 11 to the recited order of steps [11b] and [11c]. In particular, the figures in the '826 patent all depict final structures. '826 patent, 1:50-2:28, Figs. 1A-1B, 2A-2D, 3A-3E. And the rest of the specification does not describe any specific method for making the structures. As well-known in the art, the same final structure can be made by different methods. Without any explicit statement in the '826 patent that limits the order of the manufacturing steps, a POSA would understand the steps in claim 11 are not limited to their recited order. In fact, as I illustrate below, changing the order of steps [11b] and [11c] would arrive at the same end structure (end product). *See, infra*, §XII.A.2 (the same rivet-like anchor via structure can be achieved by a process performing the metal filler deposition first or a process performing the backside metal layer formation first).

71. I was not asked to expressly construe any other terms at this time but was asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '826 patent. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '826 patent as it would have been understood by a

person of ordinary skill in the art at the earliest claimed priority date of the '826 patent (March 11, 2013).

VIII. LEVEL OF ORDINARY SKILL IN THE ART

72. In rendering the opinions set forth in this declaration, I have been asked to consider the '826 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as "one skilled in the art," "skilled artisan," "POSA," or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

73. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '826 patent (Mar. 11, 2013) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and *vice versa*.

74. I was at least a person of ordinary skill in the art as of March 11, 2013.

IX. THE PRIOR ART

75. In forming my opinions, I found the following prior art relevant when considering whether the claims of the '826 patent are anticipated or would have been obvious.

Ex. 1004	U.S. Patent Publication No. 2009/0079056 to Conn, filed December 7, 2007, and published March 26, 2009 (" <i>Conn</i> ")
Ex. 1005	U.S. Patent Publication No. 2014/0138844 to Gambino et al., filed November 21, 2012, and published May 22, 2014 (" <i>Gambino</i> ")
Ex. 1008	U.S. Patent Publication No. 2012/0104546 to Ding et al., filed November 1, 2010, and published May 3, 2012 (" <i>Ding</i> ")
Ex. 1009	U.S. Patent Publication No. 2013/0082382 to Torii, filed September 28, 2012, and published April 4, 2013 (" <i>Torii</i> ")
Ex. 1010	U.S. Patent Publication No. 2012/0256310 to Ide, filed April 5, 2012, and published October 11, 2012 (" <i>Ide</i> ")

X. GROUNDS OF UNPATENTABILITY

76. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my

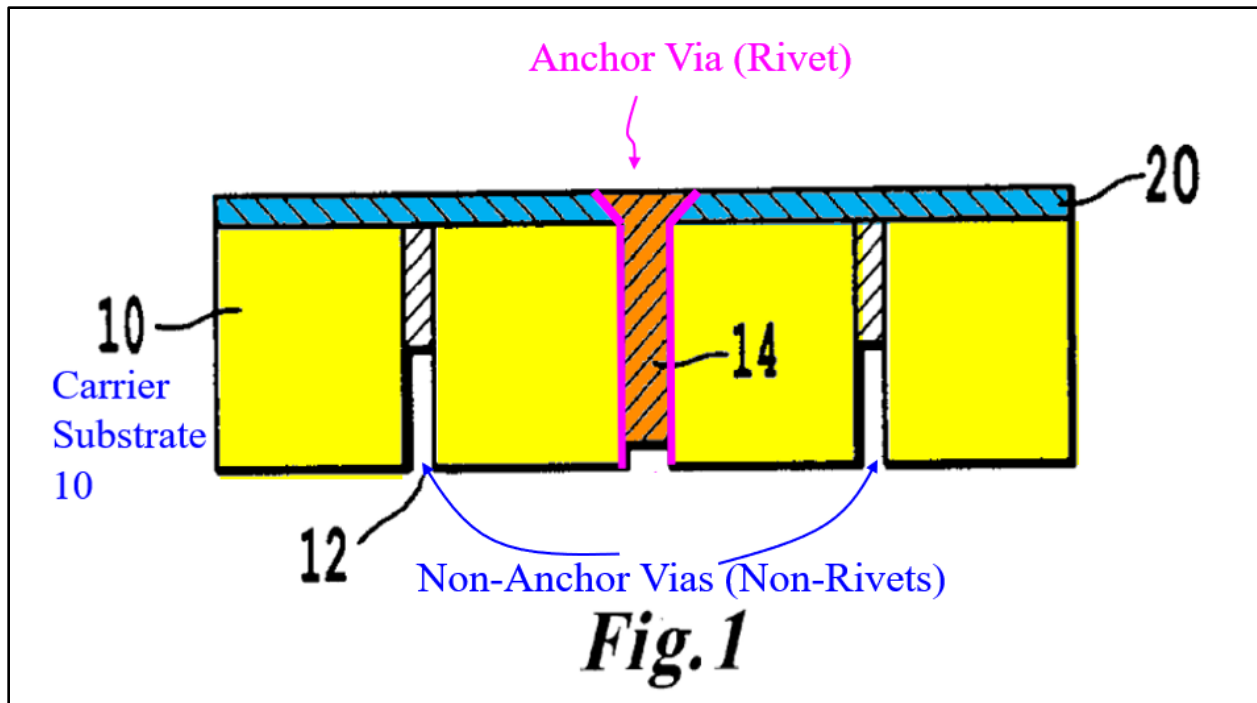
opinion that claims 1-20 of the '826 patent are anticipated by the prior art and would have been obvious to one of ordinary skill in the art.

77. In particular, it is my opinion that claims 1-20 of the '826 patent are unpatentable based on the following grounds:

Ground		Challenged Claims	Basis	Prior Art
1		1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	§102	<i>Conn</i>
2	2A	1, 2, 4-7, 9, 11, 12, 14-17, 19	§103	<i>Conn</i> in view of knowledge of a person of ordinary skill in the art (POSA)
	2B	8, 18	§103	<i>Conn</i> in view of knowledge of POSA and Applicant Admitted Prior Art (AAPA)
3	3A	1, 2, 4-7, 11, 12, 14-17	§103	<i>Gambino</i> in view of <i>Conn</i>
	3B	10, 20	§103	<i>Gambino</i> in view of <i>Conn</i> and <i>Ding</i>
4		1, 8-11, 18-20	§102	<i>Torii</i>
5		1-3, 9, 11-13, 19	§102	<i>Ide</i>

XI. GROUND 1: *Conn* ANTICIPATES CLAIMS 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, AND 19**A. Overview of *Conn***

78. Same as the '826 patent, *Conn* discloses using “anchor vias” to “secure” a “conducting layer,” e.g., backside metal layer, to a “carrier substrate.” *Conn*, Abstract, [0011]. Specifically, Figure 1 shows a side view of an electronic package structure which “includes a carrier substrate 10 having first and second surfaces (e.g., the top and bottom surfaces of the carrier substrate).” *Conn*, [0029]. The “carrier substrate 10 ha[s] at least a **conducting layer 20** formed on a first main surface of the carrier substrate 10.” *Conn*, [0026]. “The carrier substrate 10 ... has one or plural vias 12,” which “can be through-vias or can be vias that extend from the first main surface but do not reach the opposing second main surface of the carrier substrate 10.” *Conn*, [0028]. At least one of the vias 12 is filled with “a **via conductor 14**” that connects to the **conducting layer 20**, thereby forming “an **anchor via**.” *Conn*, [0028]. The **via conductor 14** in the **anchor via** forms “a rivet [] in the carrier substrate and in contact with the **conducting layer 20** by which the **conducting layer 20** maintains its structure under thermal stress.” *Conn*, [0028]. In the **anchor via** shown in Figure 1, “the **via conductor 14** is formed to enter at least partially in the via 12 but the **via conductor 14** does not necessarily have to go all the way through the via 12.” *Conn*, [0028]; *see also Conn*, [0032].



Conn, Fig. 1.

79. *Conn* explains that the above structure can be used for packaging electronic devices (e.g., computing devices) that, during usage, will produce a large amount of heat and undergo repeated thermal cycles. *Conn*, [0005]-[0008]. In this environment, the **conducting layer 20** tends to crack or delaminate from the carrier substrate, because the carrier substrate 10 and **conducting layer 20** are made of materials (e.g., silicon and copper, respectively) that have drastically different thermal conductivities and coefficients of thermal expansion, which induces significant thermal stresses under heat. *Conn*, [0005], [0008], [0027], [0030]. The **anchor via**'s rivet structure solves this problem by "secur[ing] the **conducting**

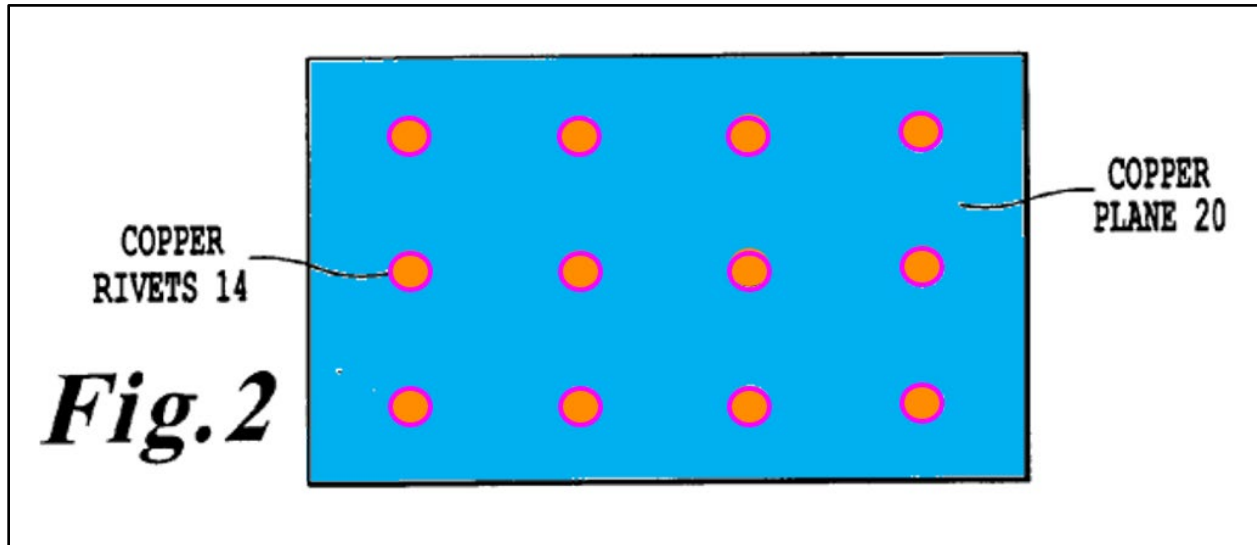
layer 20 to the carrier substrate 10” and preventing “delamination.” *Conn*, [0029]-[0030].

80. An electronic package can include a plurality of anchor vias with via conductor 14. *Conn*, [0029]. Figure 2 of *Conn* shows a top view of the electronic package structure, in which multiple “copper rivets 14,” i.e., via conductors 14 in multiple anchor vias, are “distributed relative to the conducting layer 20 in a pattern.” *Conn*, [0018], [0035]. In the example shown in Figure 2, the pattern is a matrix with defined pitches in the length and width directions of the carrier substrate. Of course, I understand that *Conn* does not limit the pattern to any particular arrangement because it says “[o]ther distribution patterns and irregular distribution patterns are also permissible and may be needed to accommodate chip attachment.” *Conn*, [0035]. “The conducting layer 20 has a length and a width extending laterally in two dimensions across a major part of the first surface of the carrier substrate 10,” and may “cover[] at least 90% of an entirety of the surface area of the carrier substrate.”⁶ *Conn*, [0029], [0031]. “The anchor vias form plural attachments (i.e., rivets) along the length and the width of the

⁶ Figure 2 (top view) does not show the carrier substrate 10, which is under the conducting layer 20 and slightly larger than the conducting layer 20.

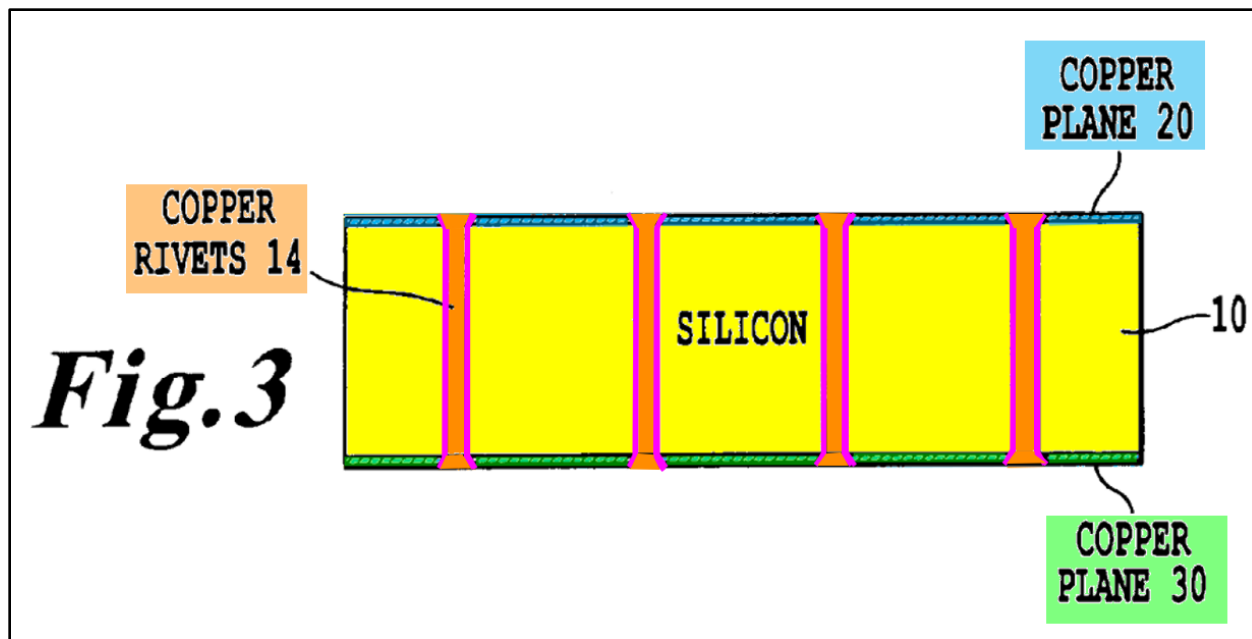
conducting layer 20 to secure the conducting layer 20 to the carrier substrate 10.”

Conn, [0029], [0031].



Conn, Fig. 2.

81. *Conn* discloses that the anchor vias can be used to secure conducting layers formed on either or both of the two main surfaces (i.e., top and bottom surfaces) of the carrier substrate 10. *Conn*, [0037]-[0041]. Figure 3 shows that “another conducting layer 30 is formed on the second main surface of the carrier substrate 10.” *Conn*, [0037]. “The conducting layer 30 can have the same or different area coverage as described above with regard to conductive layer 20.” *Conn*, [0037]. As shown in Figure 3, anchor vias with “copper rivets 14” can “hold the conducting layers 20 and 30 mechanically connected to the substrate.” *Conn*, [0038].

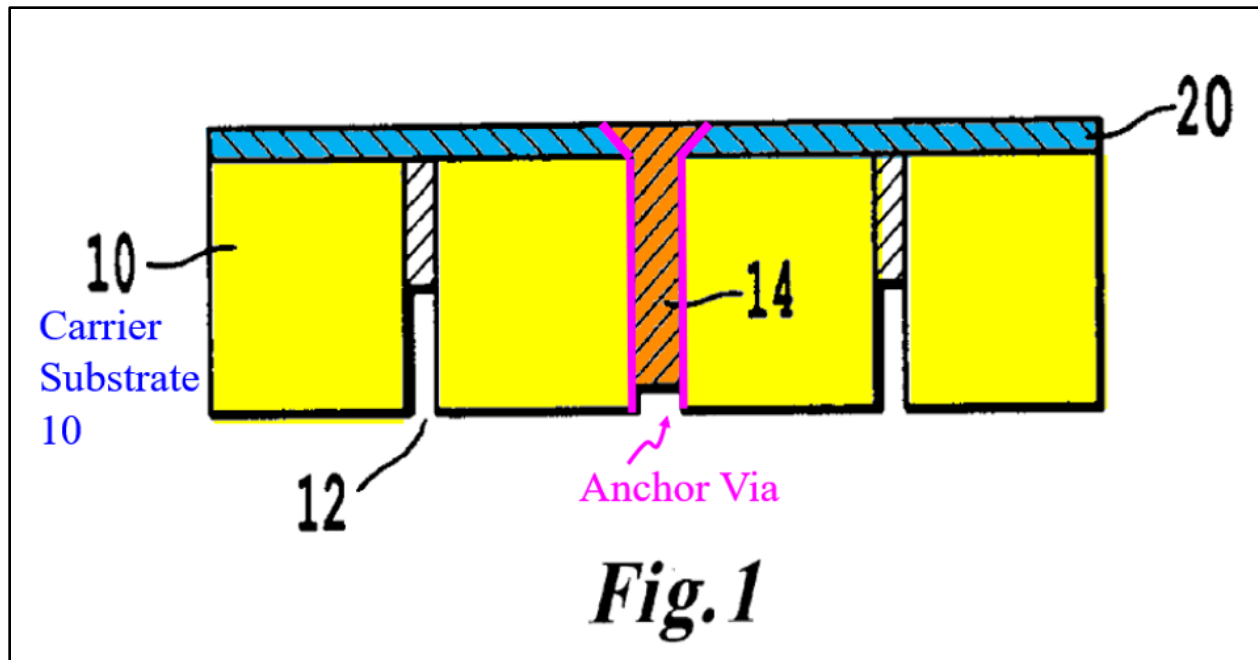


Conn, Fig. 3.

B. Independent Claim 1

1. [1pre] A structure comprising:

82. I was informed by counsel that the preamble of a claim is not necessarily limiting. Nonetheless, to the extent the preamble is limiting, in my opinion *Conn* discloses it. Specifically, *Conn* discloses the preamble [1pre] by disclosing an electronic package structure as illustrated in its Figure 1. *Conn*, [0017], [0029]. The electronic package depicted therein includes “a carrier substrate 10 having at least a **conducting layer 20** formed on a first main surface of the carrier substrate 10.” *Conn*, [0026].

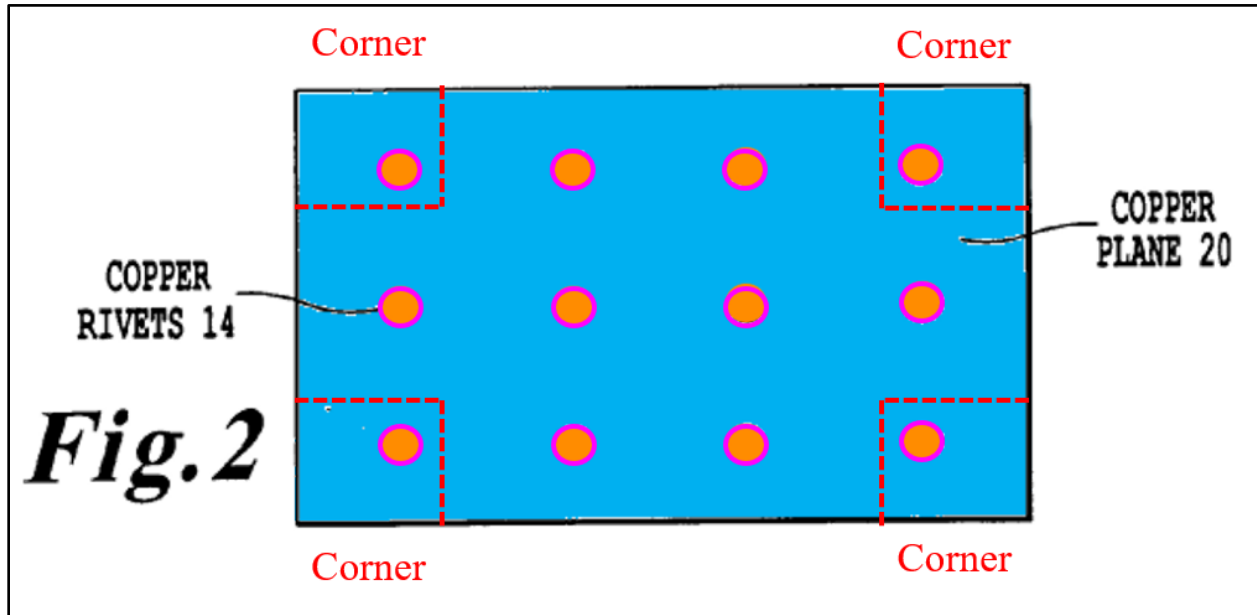


Conn, Fig. 1.

2. [1a] at least one **anchor via** disposed in at least one **corner** of a semiconductor substrate;

83. In my opinion, *Conn* discloses this limitation because it discloses that the carrier substrate 10 in Figure 1 includes “a plurality of **anchor vias** (e.g., **via conductor 14**).” *Conn*, [0029]. Moreover, Figure 2 provides a plan view of the electronic package showing that the plurality of **anchor vias** (see the **copper rivets 14** in Figure 2) are “distributed relative to the **conducting layer 20** in a pattern.” *Conn*, [0035]. Figure 2 shows that the **anchor via** pattern covers the entire surface of the **conducting layer 20**, such that some **anchor vias** are disposed at the **corners** of the **conducting layer 20**. *Conn*, [0035]. In my opinion, those skilled in the art seeing Figure 2 would understand that the depicted **anchor via** pattern is intended to repeat across the length and width directions of the **conducting layer 20**. This

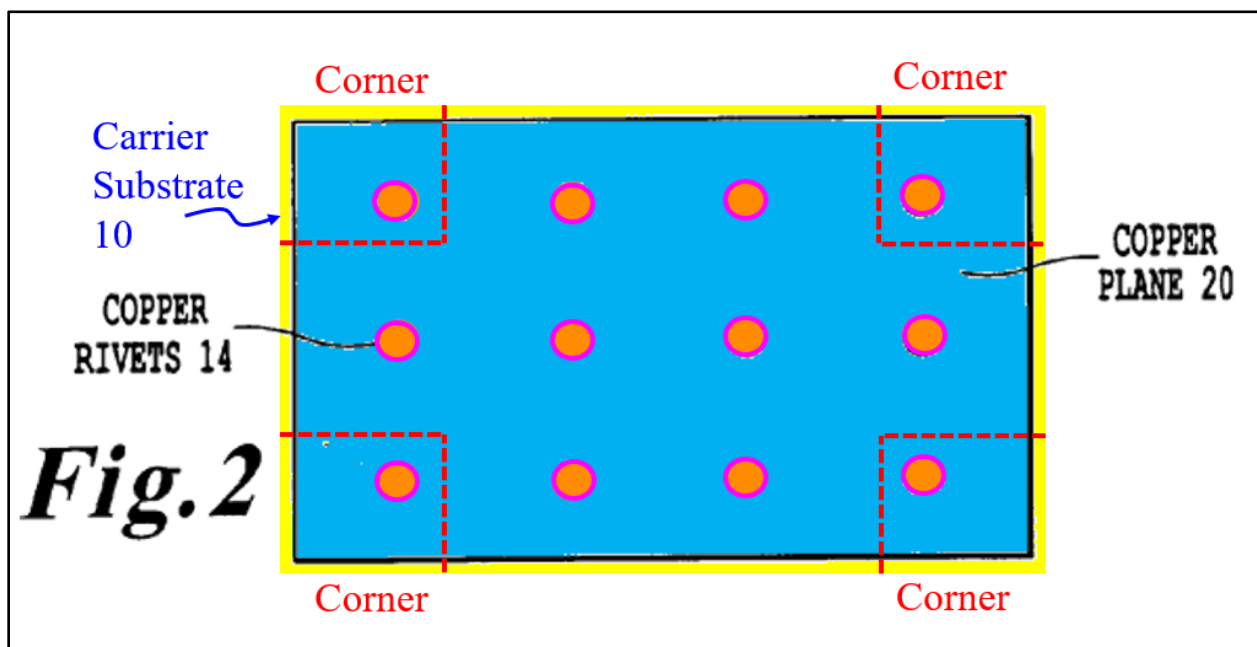
way, the **anchor vias** are distributed on the entire surface of the **conducting layer 20**, including the **corners** of the **conducting layer 20**.



Conn, Fig. 2.

84. Figure 2 does not show the carrier substrate 10, but *Conn* discloses that the **conducting layer 20** can cover more than “90% of an entirety of the surface area of the carrier substrate,” even approaching “100%.” *Conn*, [0031]. In the following modified Figure 2, I use yellow color to show the carrier substrate 10. Since Figure 2 is a top view, the part of the carrier substrate 10 overlapping with the **conducting layer 20** is blocked by the **conducting layer 20** and thus is not visible. The modified Figure 2 shows that when the **conducting layer 20** covers 90%–100% of the surface of the carrier substrate 10, the **conducting layer 20** covers almost the entirety of the surface area of the carrier substrate 10, and only the edges of the carrier substrate 10 are not covered by the **conducting**

layer 20 and thus can be seen in the modified Figure 2. Consequently, the corners of the conducting layer 20 are also the corners of the carrier substrate 10. This would be the case even if conducting layer 20 was not centered relative to carrier substrate 10 when the coverage approaches 100%. It follows that the anchor vias located at the corners of the conducting layer 20 are also located at the corners of the carrier substrate 10.

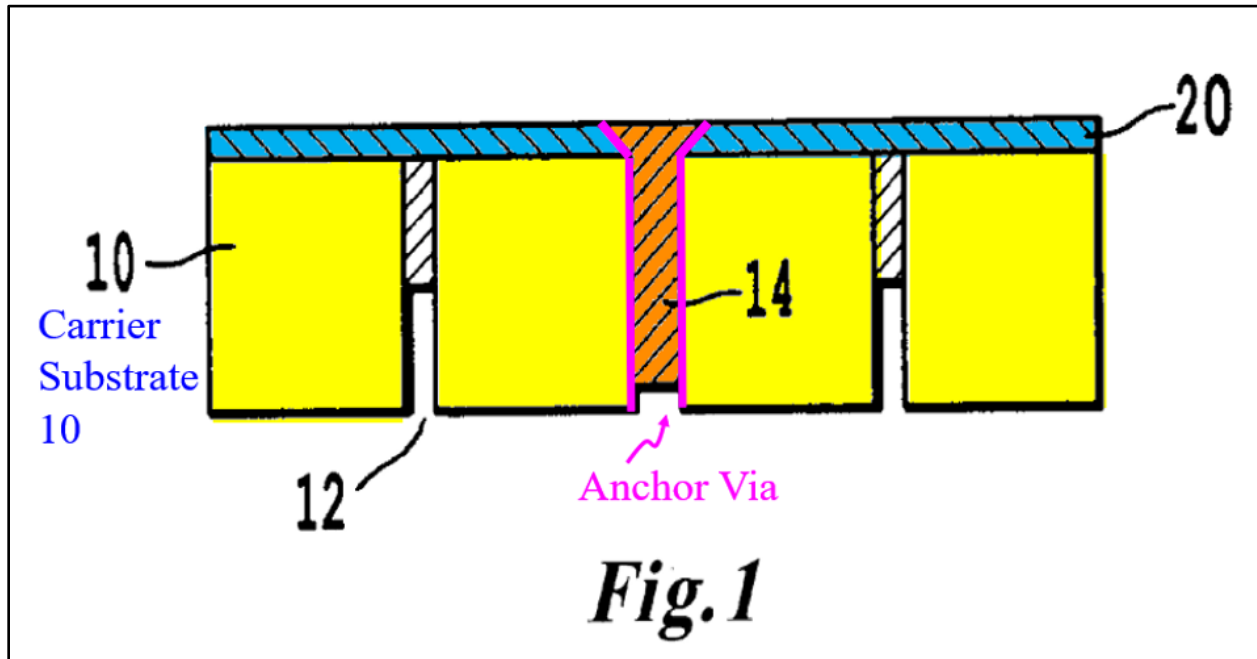


Conn, Fig. 2 (modified),

3. [1b] a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

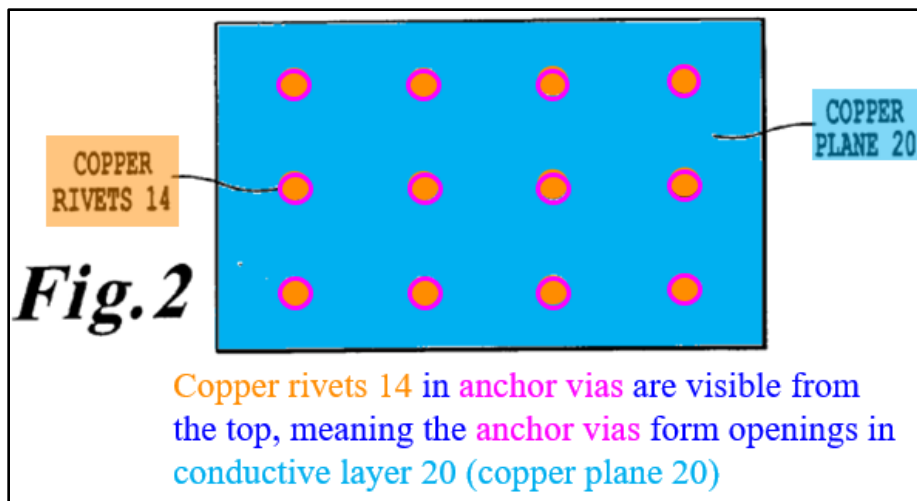
85. In my opinion, Conn discloses this limitation by disclosing the via conductors in the anchor vias form rivet structures (i.e., “copper rivets 14” in Figure 2) that protrude from a side of the substrate surface. First, as shown in

Figure 1, *Conn* discloses the claimed “metal filler” by disclosing that each anchor via is formed by filling “a via conductor 14 [] in a via 12.” *Conn*, [0028]; *see also Conn*, [0029]. “The via conductor 14 may be formed of copper, aluminum, gold, silver or other conductors.” *Conn*, [0033].



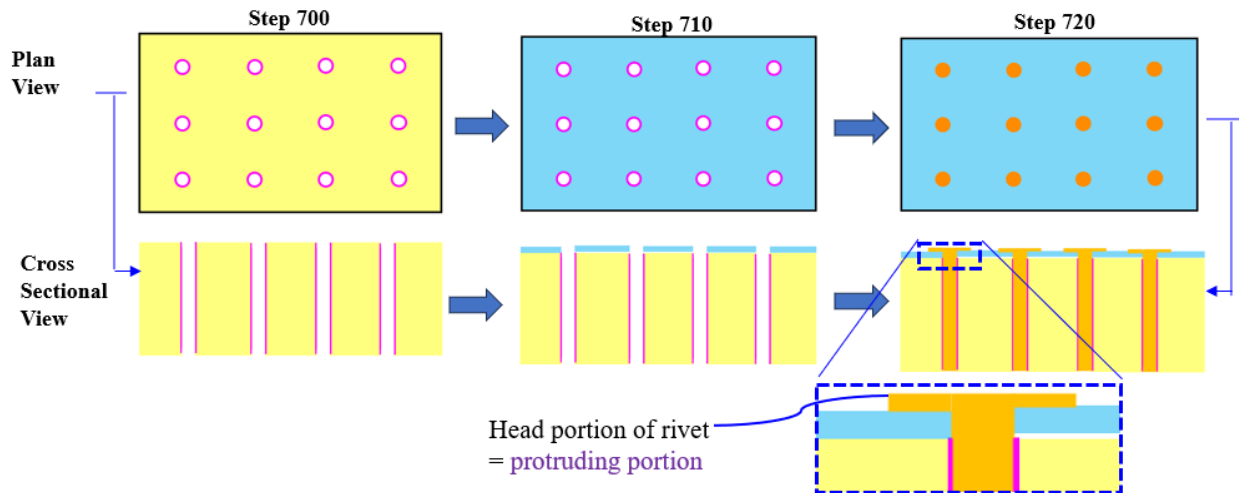
Conn, Fig. 1.

86. Second, *Conn* discloses the claimed “protruding portion” by disclosing the via conductors 14 in the anchor vias form “rivets” (i.e., “attachments”) that are mechanically “connected to” and “in contact with” the conducting layer 20. *Conn*, [0028]-[0029]; *see also Conn*, [0030], [0038], [0040], [0055], Figs. 1-3. As illustrated below, Figure 2 shows that the “copper rivets 14” (i.e., the via conductors 14 in the anchor vias) are visible. *Conn*, Fig. 2. This means that the anchor vias form openings in the conducting layer 20.

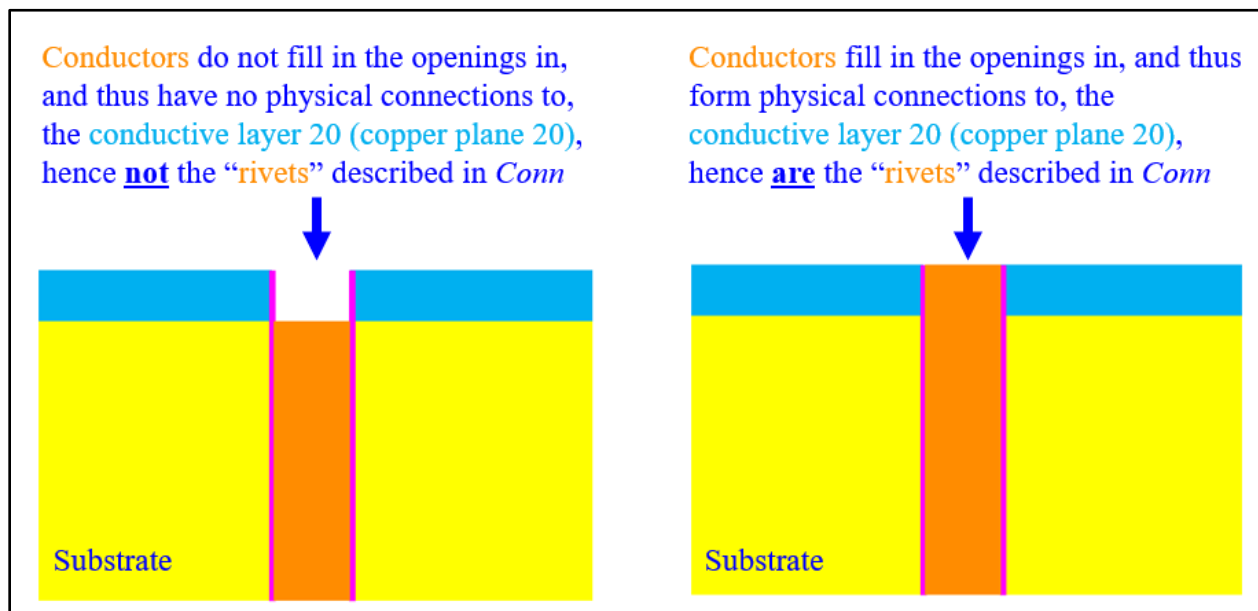


Conn, Fig. 2.

87. *Conn*'s process for making the anchor vias also discloses the claimed "protruding portion." Specifically, *Conn* discloses that the electronic package structure in Figure 1 can be manufactured using a process including "a step 700 of forming in the carrier substrate a plurality of vias extending from the first surface, a step 710 of forming a first conducting layer on the first surface of the carrier substrate, a step 720 of depositing a pattern of via conductors disposed in a predetermined number of the vias and collectively connected to the first conducting layer...." *Conn*, [0055]. As illustrated below, this process would result in a rivet-like structure in which the head portions of the via conductors form protruding portions extending from a backside of the carrier substrate.

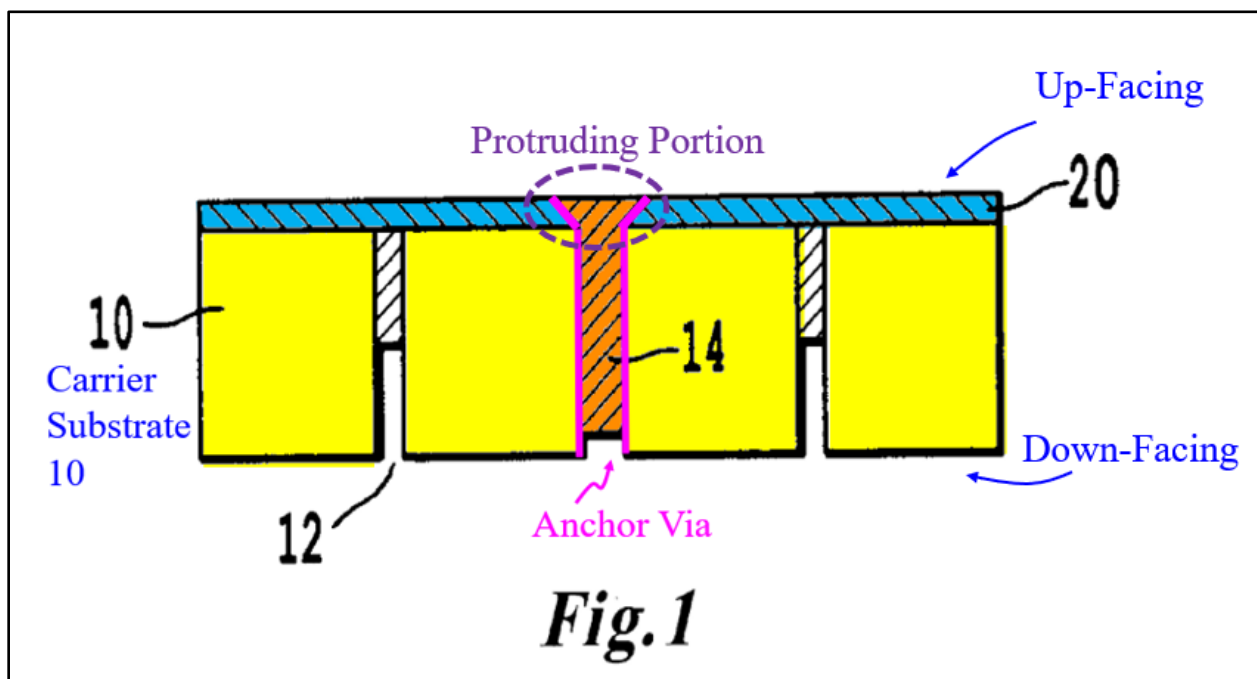


88. Moreover, as shown in the following schematic illustration, a POSA would understand the anchor vias' copper rivets 14 (i.e., conductors) must enter the openings in the conducting layer 20, in order to make Conn's described physical connection between the conducting layer 20 and the copper rivets 14.



89. Therefore, as shown below, in my opinion, a POSA would understand that Conn's anchor via rivet is a conductor that has an end entering the conducting

layer 20 and forming “a protruding portion extending from ... said semiconductor substrate,” as claimed. I notice that this understanding is also consistent with the dictionary definition of “rivet,” which is described as a metal structure “for uniting two or more pieces by passing the shank through a hole in each piece....” Ex. 1025, 3 (emphasis added). Like the shank, *Conn*’s anchor via rivet has a protruding portion passing through the conducting layer.

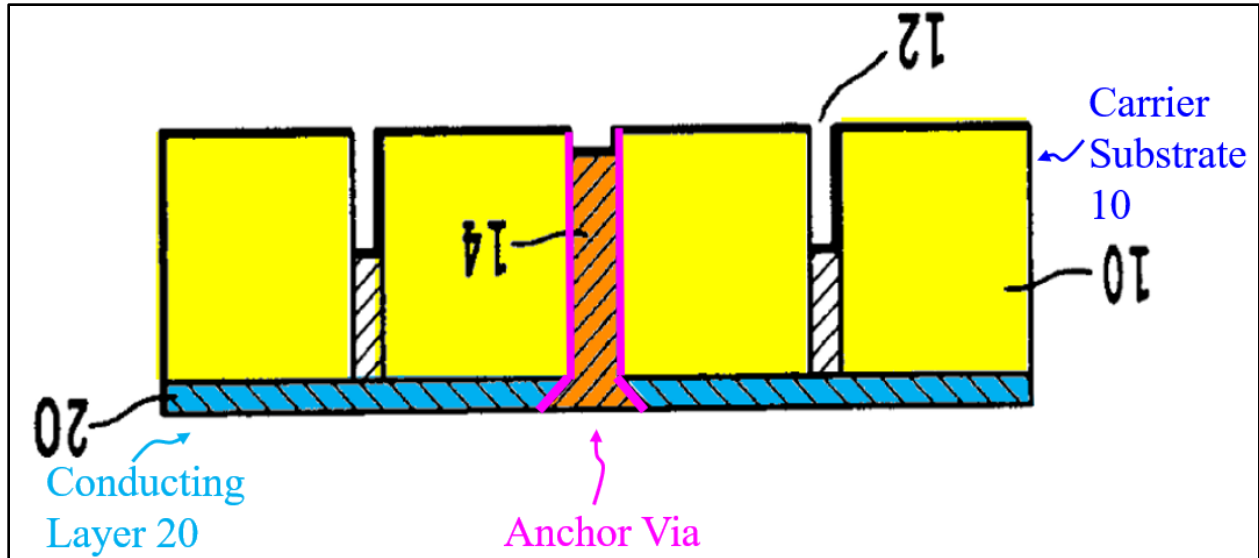


Conn, Fig. 1.

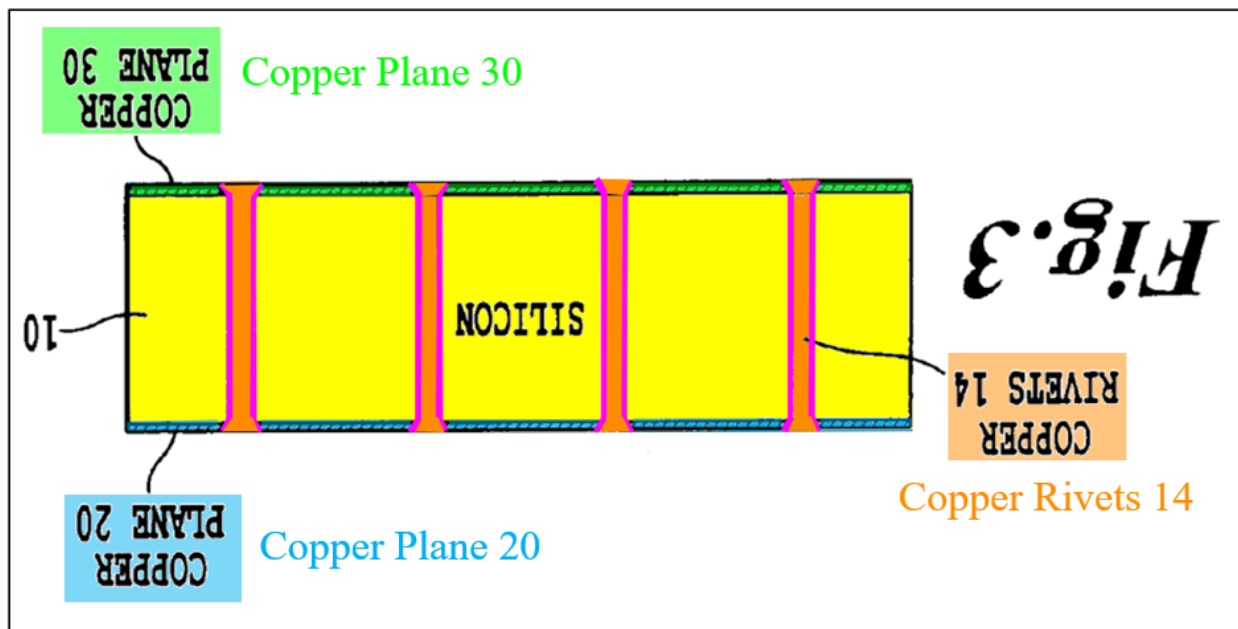
90. Third, *Conn*’s conducting layer 20 is on a side of the substrate corresponding to the claimed “backside.” As discussed in *supra*, §VI.B, a POSA would understand the backside can face either up or down, so the up-facing side shown in *Conn*’s Figure 1 (above) meets the claimed “backside.” Moreover, as illustrated below by rotating Figure 1 by 180°, a POSA would understand

conducting layer 20 in Figure 1 can also face down because *Conn*'s text generally describes it as being formed on "a first main surface" of carrier substrate 10, without limiting the first main surface to be up-facing or down-facing. *Conn*, [0026]; *see also Conn*, [0029] (*Conn* mentions "a carrier substrate 10 having first and second surfaces (e.g., the top and bottom surfaces of the carrier substrate)" but does not specify the first main surface must be the top or bottom surface).

Additionally, as shown in Figure 3, *Conn* discloses that the anchor vias can act as rivets to secure conducting layers (conducting layer 20 and conducting layer 30) located on opposite sides of the carrier substrate 10. *Conn*, [0037]-[0038], [0040], Fig. 3. This means the anchor vias are not limited to connecting conductive layers on any particular side or surface of the carrier substrate, thereby confirming the conducting layer 20 is not limited to any particular side. Accordingly, in my opinion, *Conn* discloses that the conducting layer 20, as well as the rivet protruding portion formed therein, can be on either the up-facing or down-facing side illustrated in Figure 1, which in turn discloses the claimed "backside."



Conn, Fig. 1 (rotated by 180°).

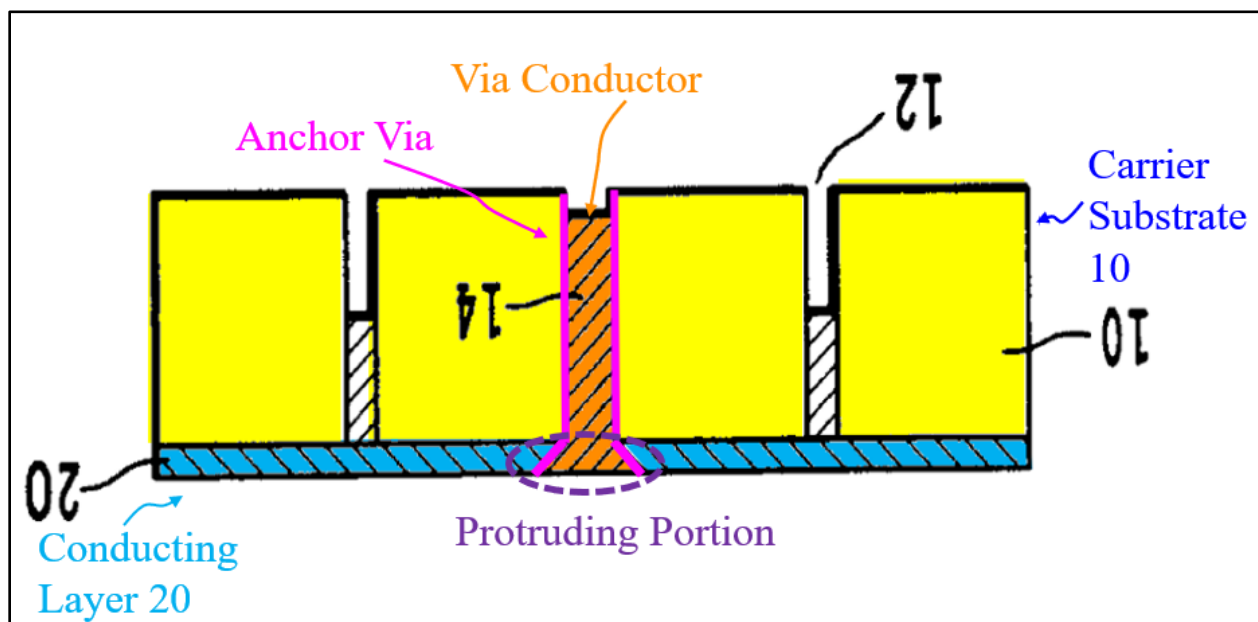


Conn, Fig. 3 (rotated by 180°).

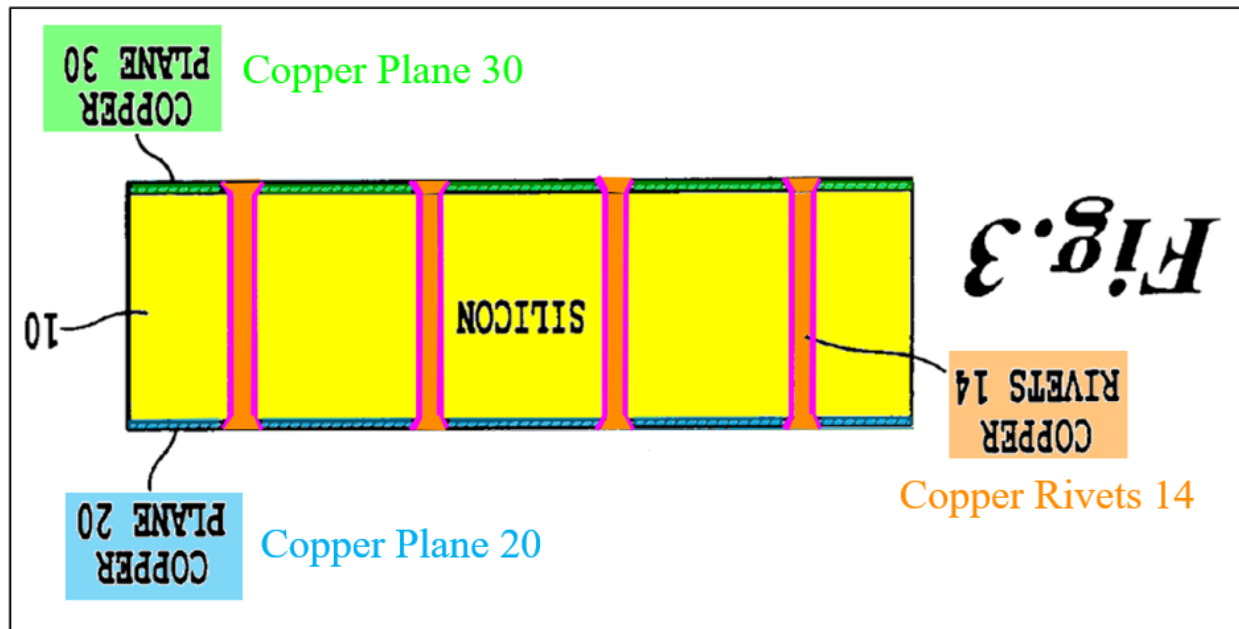
4. [1c] a **backside metal layer** on a bottom surface of said semiconductor substrate, said **backside metal layer** being bonded to said **protruding portion** of said **metal filler** of said at least one **anchor via**;

91. *Conn* discloses this limitation by disclosing the **conducting layer 20** in Figure 1 is disposed on one of the main surfaces of the carrier substrate and is connected to the **protruding portion** of the **anchor via conductor**. First, the '826 patent equates "bottom surface" to "backside." '826 patent, 2:56-60 ("semiconductor substrate 110 having ... bottom surface 112, or backside"). As discussed in §XI.B.3, *Conn*'s **conducting layer 20** is on the backside, so it constitutes the claimed "**backside metal layer**" and the substrate surface on which **conducting layer 20** is disposed constitutes the claimed "bottom surface." Again, as discussed in §VI.B, a semiconductor substrate's backside and bottom surface have no relation to the substrate's orientation. It is understood in the art that the backside and bottom surface can either face up or face down. *Supra*, §VI.B. Thus, *Conn*'s disclosure of **conducting layer 20** and first main surface discloses the claimed "**backside metal layer**" and "bottom surface." Moreover, to the extent that HID may (erroneously) argue that the claimed "backside" and "bottom surface" must face down, *Conn* also discloses it. As discussed in §XI.B.3, *Conn*'s description of **conducting layer 20** and first main surface in Figure 1 does not limit their orientation. *Conn*, [0026], [0029]. For the convenience of discussion, below I rotate Figure 1 by 180° to show the **conducting layer 20** and first main surface can

face down. Additionally, *Conn* discloses the **anchor vias** can act as rivets to connect the **conducting layer 20** and **conducting layer 30** located on opposite sides of the carrier substrate 10. *Conn*, [0038], [0040]. This means the **anchor vias** are not limited to connecting conductive layers on any particular side or surface of the carrier substrate, thereby confirming the **conducting layer 20** and first main surface can face down.



Conn, Fig. 1 (rotated by 180°).



Conn, Fig. 3 (rotated by 180°).

92. Second, as discussed in §XI.B.3, *Conn* discloses the **via conductors** in the **anchor vias** form **protruding portions** that are mechanically “connected to” and “in contact with” the **conducting layer 20**. *Conn*, [0028]-[0029]; *see also Conn*, [0030], [0038], [0040], [0055], Figs. 1-3. To manufacture such connections, *Conn* discloses that the **via conductors 14** and **conducting layer 20** are “formed to be a unitary, single, monolithic structure” or “formed in separate process steps out of a single material” (e.g., copper or tungsten). *Conn*, [0033]-[0034]; *see also Conn*, [0037], [0041]. In my opinion, a POSA would understand that both methods will cause **via conductors 14** to form a metallic bond with **conducting layer 20**. Namely, the first method means these two conductors are necessarily fused and bonded to each other. Moreover, a POSA would understand that in both methods the **via**

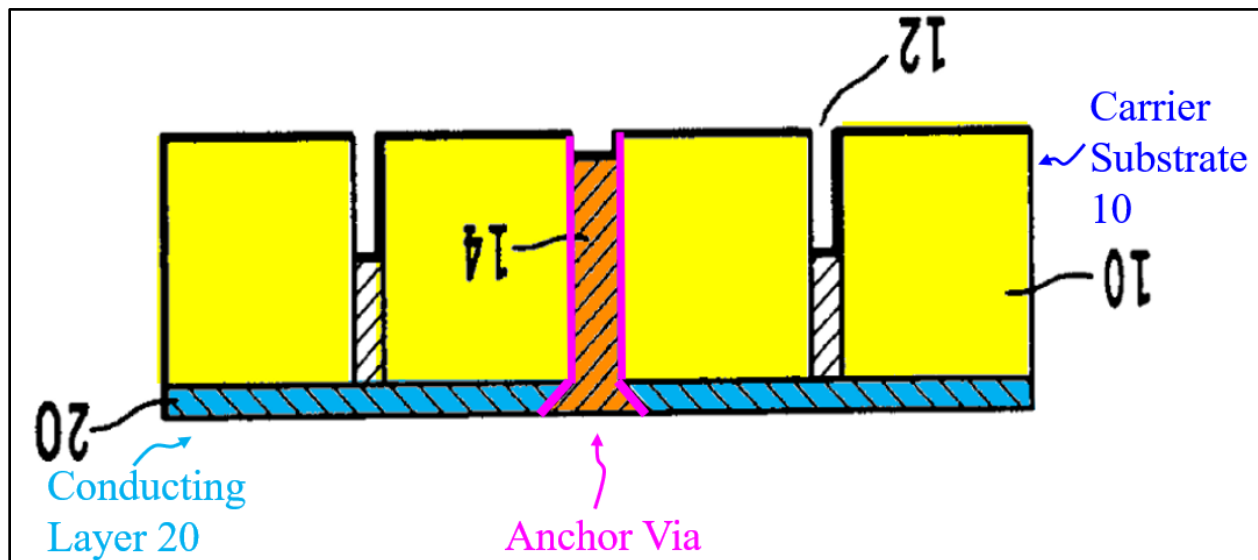
conductors 14 and conducting layer 20 are deposited under vacuum at elevated temperature, which is the typical condition used in the integrated-circuit industry to form metallic bonds. *E.g.*, *Farooq* (Ex. 1029), 5:5-25 (“Referring now to FIG. 3, the first and second semiconductor structures 10, 20 are aligned, contacted and then bonded. In one preferred embodiment, the bonding is made by a solid state bonding process to form a metal to metal bond. The solid state bonding process in general may be accomplished by the following steps. First, the surface of the metallic layers is cleaned or treated so that a pristine surface is presented for joining. ... Lastly, the metallic layers 18, 28 are contacted and pressure of 30 to 50 Kilo Newtons is applied for 30-60 minutes while at a temperature of about 300-400° C. in a suitable ambient such as forming gas, nitrogen or a partial vacuum to complete the solid state bonding process.”). In this condition, when two metals with clean surfaces coming in contact with each other, they form a metal-on-metal bond just like that described in the ’826 patent, thereby meeting the “bonded to” limitation. ’826 patent, 3:43-48 (“protruding portion ... form[s] a very strong physical, metal-on-metal bond”).

5. [1d] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

93. Conn discloses this limitation by *not* disclosing that any anchor vias provide any ground connection but instead disclosing either the anchor vias or the

via conductors therein do not need to reach the opposite side of the carrier substrate, thus recognizing the purpose of the anchor vias is *not* to provide any ground connection. *Conn*, Fig. 1. Specifically, *Conn* discloses that the anchor vias “do not [need to] reach the opposing second main surface of the carrier substrate 10.” *Conn*, [0028]. This is the same as the ’826 patent’s description that anchor vias 132, 133 do not need to be through the entire substrate, but rather may be formed to a certain depth into the substrate. ’826 patent, 3:17-27 (“Each of anchor vias 132 and 133 may be formed to a depth d_0 of 100 μm into semiconductor substrate 110. However, anchor vias 132 and 133 are not so limited and d_0 may be greater or less than this value, according to the particular application. In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer....”). Separately, *Conn* discloses “the via conductor[s] 14 do[] not necessarily have to go all the way through” the anchor vias. *Conn*, [0028]. In both configurations, the via conductors 14 do not reach the side of the carrier substrate opposite to the conducting layer 20, so their purpose is *not* to provide any electrical connection (including ground connection) to any active device on that side. Moreover, the via conductors 14 do not provide ground connection to any active devices in the carrier substrate because it may only have “[p]assive components,” not active devices. *Conn*, [0026]; *supra*, §VI.A. Finally, via structures are designed to connect (electrically or mechanically) components in

different layers, rather than providing connection to components in the same layer or on the same side of the substrate. *See, e.g., Chiu, [0005]* (“Through-silicon vias (TSVs) are thus used in 3DICs and stacked dies. In this case, TSVs are often used to connect the integrated circuits on a die to the backside of the die.”), [0023] (“dummy vias on the backside of wafer 10 may be connected to the dummy metal lines and dummy vias on the front side of wafer 10 to form an integrated metal feature”). Thus, a POSA would understand that *Conn*’s **via conductors 14** would not provide ground connection to any active devices on the same side as **conducting layer 20**.

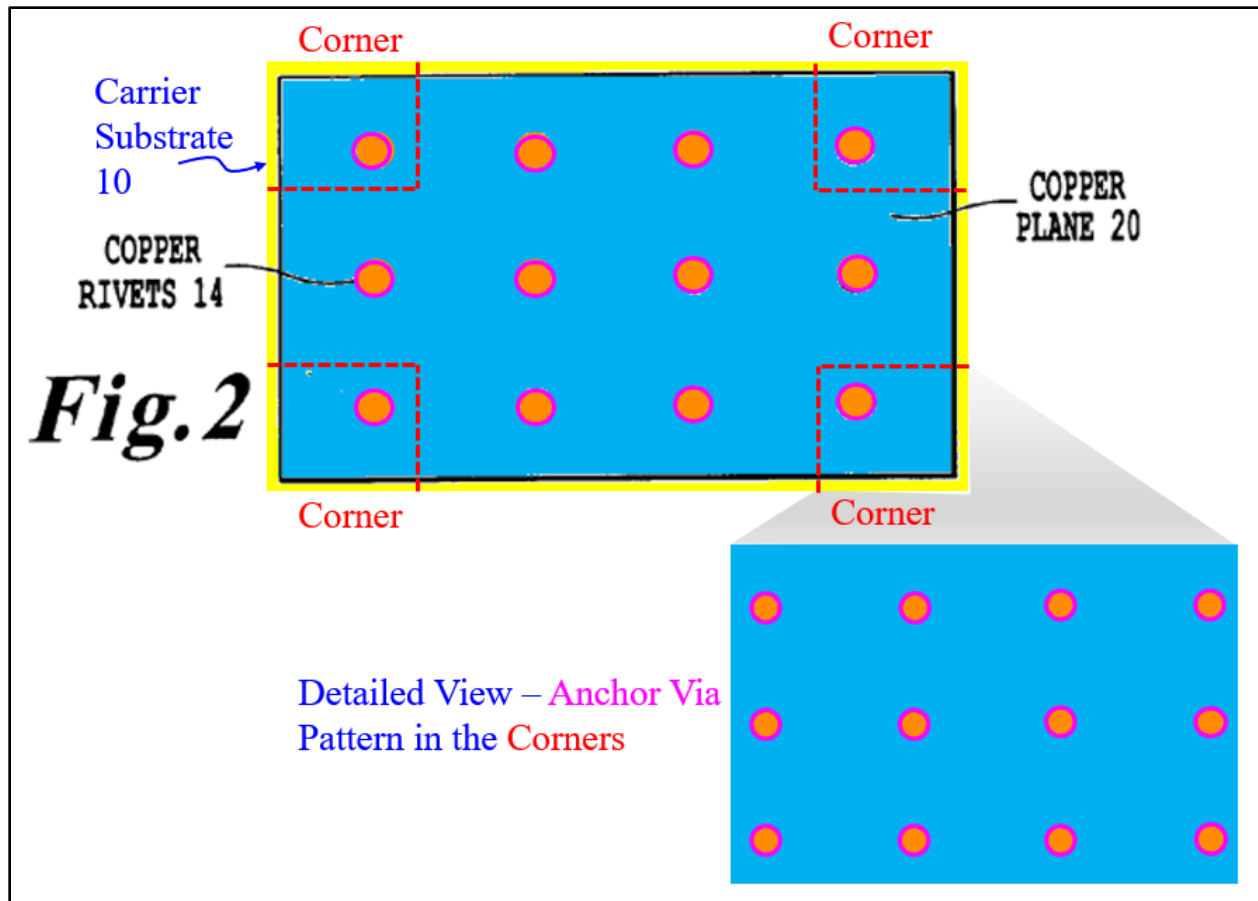


Conn, Fig. 1 (rotated by 180°).

C. Claim 2

The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.

94. As discussed in §XI.B.2, *Conn* discloses at least one anchor via disposed in a corner of a semiconductor substrate by disclosing a pattern of anchor vias that spreads across the substrate and extends to its corners. *Conn*, [0031], [0035], Fig. 2. This means the anchor vias are repeated in the substrate, including the corners, according to the pattern, and having certain densities as disclosed in *Conn*, e.g., 400 vias per mm². *Conn*, [0035]-[0036]. Thus, as illustrated below, a POSA would understand that each corner has a pattern of repeating anchor vias, i.e., “a cluster of anchor vias.” For example, semiconductor dies (i.e., chips) commonly have a size of 1 mm² or more, such as 10 mm² or 100 mm². For a substrate with a total area of 1 mm², if each corner occupies 1% of the total area and the anchor via pattern has a density of 400 vias per mm², then each corner has a cluster of $1 \text{ mm}^2 \times 1\% \times 400 \text{ vias/mm}^2 = 4$ anchor vias. Similarly, for a substrate with a total area of 10 mm², each corner has a cluster of $10 \text{ mm}^2 \times 1\% \times 400 \text{ vias/mm}^2 = 40$ anchor vias; and for a substrate with a total area of 100 mm², each corner has a cluster of $100 \text{ mm}^2 \times 1\% \times 400 \text{ vias/mm}^2 = 400$ anchor vias. Moreover, nothing in the '826 patent prevents a corner from occupying more than 1% of the total area, in which case the numbers of vias I calculate here would be even higher.



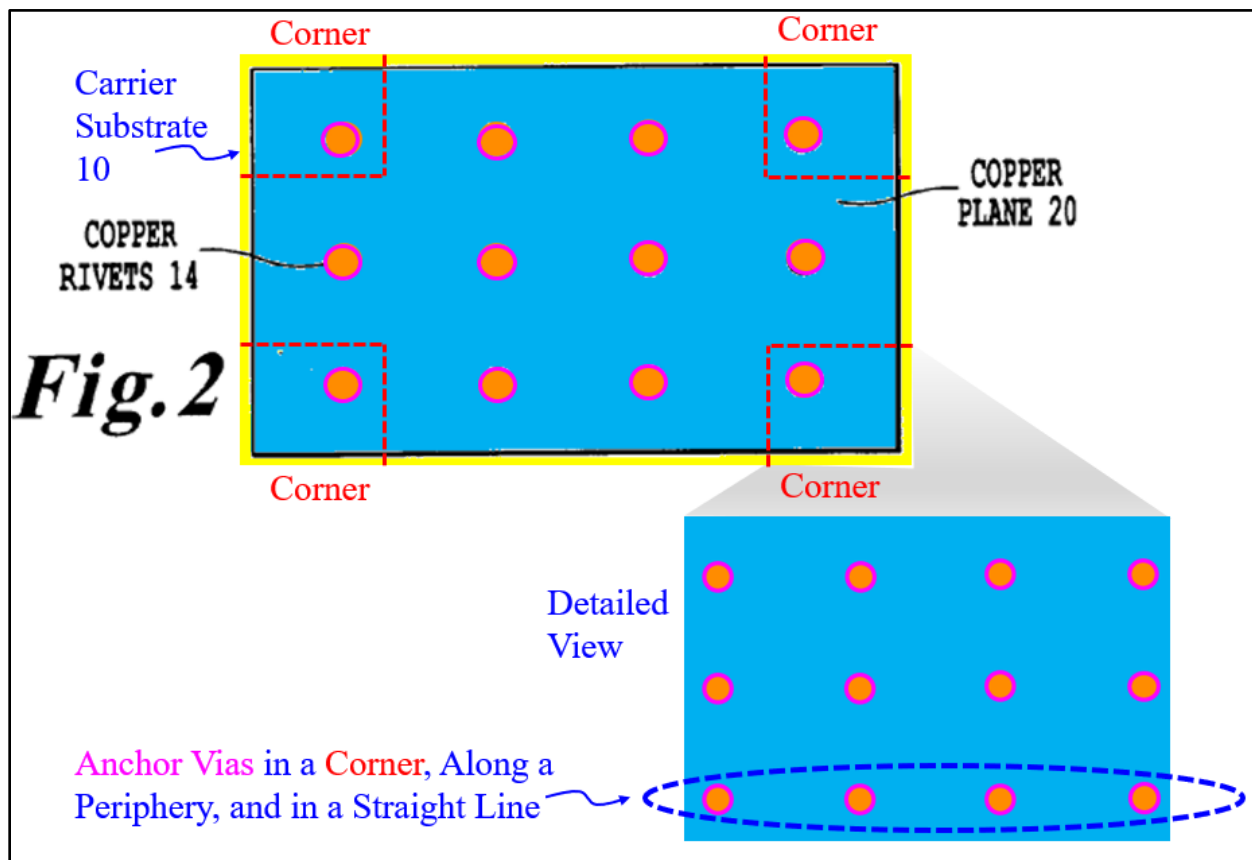
Conn, Fig. 2 (modified).

D. Claim 4

The structure of claim 1, wherein said at least one **anchor via** comprises a plurality of **anchor vias** disposed in a straight line along a periphery of said semiconductor substrate.

95. *Conn* discloses claim 4 for the same reasons discussed regarding claim 2. *Infra*, §XI.C. As illustrated below, *Conn* discloses that each **corner** of the carrier substrate has multiple **anchor vias** repeating according to the pattern depicted in Figure 2, within which multiple **anchor vias** are “disposed in a straight

line along a periphery of said semiconductor substrate,” as claimed. *Conn*, [0031], [0035]-[0036], Fig. 2.



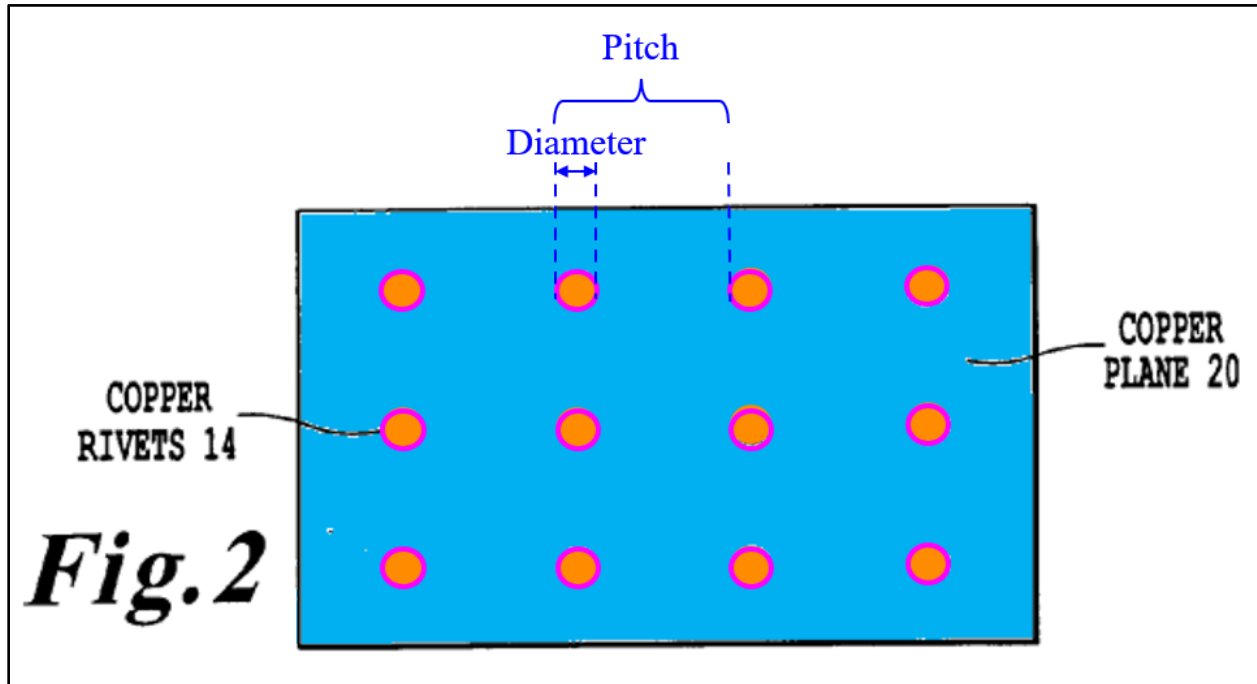
Conn, Fig. 2 (modified).

E. Claim 5

The structure of claim 4, wherein a linear density of said plurality of **anchor vias** is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

96. *Conn* discloses claim 5 by disclosing that the **anchor vias** in the pattern depicted in Figure 2 can have a minimum diameter of “30” μm , and a repeating pitch as large as “1000 μm .” *Conn*, [0035]. This means the linear density

of the anchor vias can be as small as $(30/1000) \times 100\% = 3\%$, i.e., “less than approximately 10%,” as claimed.



Conn, Fig. 2.

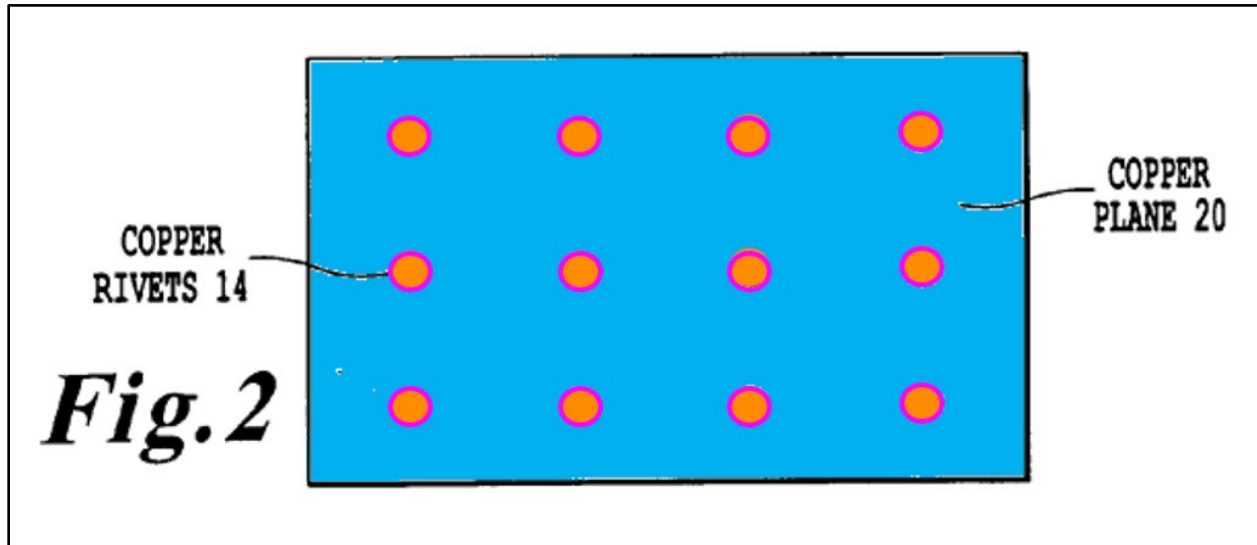
F. Claim 7

The structure of claim 1, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

97. *Conn* discloses two use cases that meet claim 7. Specifically, *Conn* discloses that the **anchor vias** “can have a diameter between 30 and 150 μm .” *Conn*, [0035]. Namely, the smallest possible area occupied by a single anchor via is $\pi \times (0.03/2)^2 \text{ mm}^2$. In a first case, *Conn* discloses that “[a] density of the **via conductors** in the [**anchor via**] pattern is between 0.01 and 400 **via conductors** per unit square millimeter.” *Conn*, [0035]. Here, the percentage of the total area of the

conducting layer occupied by the anchor vias can be as small as

$$\pi \times (0.03/2)^2 \times 0.01 \times 100\% = 0.0007\%.$$



Conn, Fig. 2.

98. In a second case, *Conn* discloses “a conducting layer having approximate sizes of 140 mm by 80 mm” can have “a minimum of 5000” of anchor vias. *Conn*, [0036]. This means that the percentage of the total area of the conducting layer occupied by the anchor vias can be as small as

$$\pi \times (0.03/2)^2 \times 5000 \times 100\% / (140 \times 80) = 0.03\%.$$

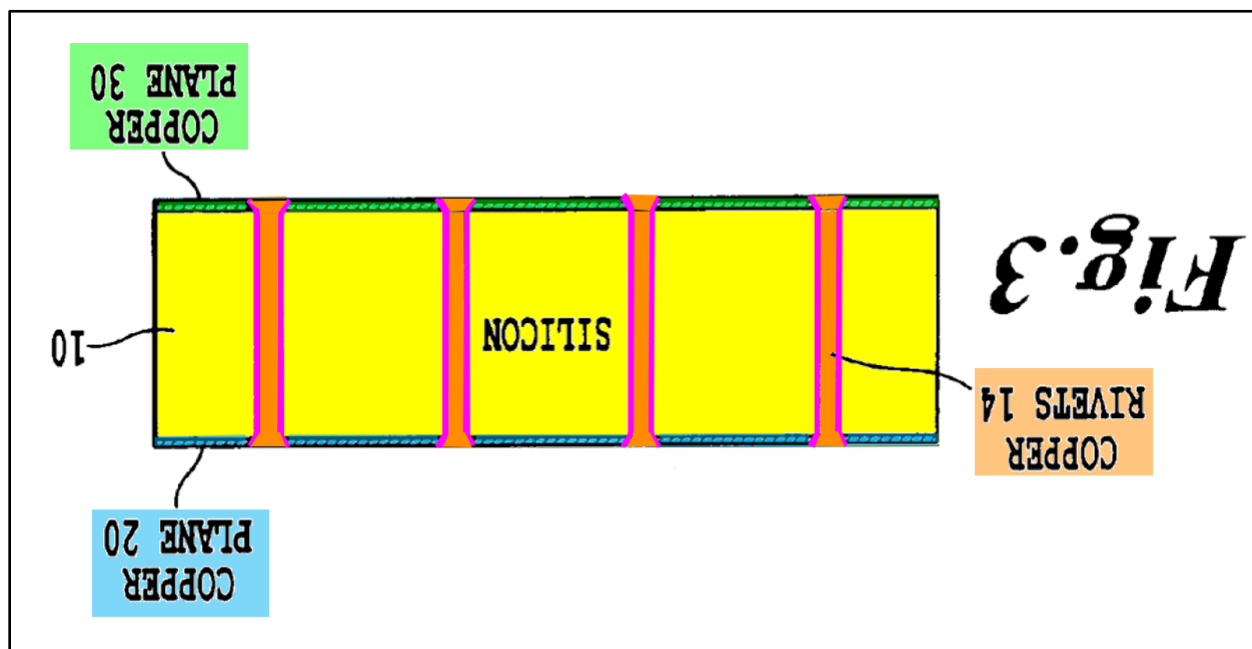
99. In the above discussion, the “total area” refers to the conducting layer, not the carrier substrate. But, as discussed in §XI.B.2, the conducting layer covers 90%–100% of the surface area of the carrier substrate. *Conn*, [0031]. Thus, the carrier substrate has a total area no less than that of the conducting layer. It follows that the percentage of the total area of the carrier substrate occupied by the anchor

vias can be as small as 0.0007% (first case) or 0.03% (second case), both being “less than approximately 0.5%,” as claimed.

G. Claim 9

The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

100. *Conn* discloses claim 9 by disclosing the electronic package structure in Figure 1 can include “another **conducting layer 30** [] formed on the second main surface of the carrier substrate 10, as shown in FIG. 3.” *Conn*, [0037]. Like **conducting layer 20**, **conducting layer 30** is similarly connected to (thus “bonded to”) the **anchor vias**. *Conn*, [0038], [0040]-[0041]. Thus, **conducting layer 30** constitutes an overlying **metal layer** bonded to the **anchor vias**.



Conn, Fig. 3 (rotated by 180°).

H. Independent Claim 11

101. Independent claim 11 is substantially similar to claim 1, except it recites a method for making the structure in claim 1. Specifically, claim 11 recites the same structural features of the anchor vias as those in claim 1. The only substantive difference is that claim 11 also recites the method steps of: [11a] “forming” at least one **anchor via**, [11b] “depositing” a **metal filler** within said at least one anchor via, and [11c] “forming” a **backside metal layer**. *Supra*, §VII.B. In my opinion, *Conn* discloses these steps, as discussed below.

1. “Forming,” “depositing,” and “forming” steps

102. Figure 7 of *Conn* discloses a method for manufacturing the electronic package structure in Figure 1. *Conn*, [0023], [0055]. This method includes, in part, the following steps: “a step 700 of forming in the carrier substrate a plurality of **vias** extending from the first surface, a step 710 of forming a **first conducting layer** on the first surface of the carrier substrate, [and] a step 720 of depositing a pattern of **via conductors** disposed in a predetermined number of the vias.” *Conn*, [0055], Fig. 7. Steps 700, 720, and 710 respectively disclose the claimed steps of:

- [11a] “forming at least one **anchor via** in at least one corner of a semiconductor substrate;”

- [11b] “depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;” and
- [11c] “forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via.”

'826 patent, 8:35-43. Thus, *Conn* discloses each and every claimed step.

103. As discussed in §VII.D, in this proceeding, claim 11 does not require the [11b] “depositing” and [11c] “forming” steps to be performed in their recited order. Thus, in my opinion, *Conn*’s disclosure of each and every step in claim 11 anticipates the claim.

2. Remaining limitations of claim 11

104. The remaining limitations of claims 11 are substantially similar to those structural features recited in claim 1. *Supra*, §VII.B. Thus, given the similarity between claims 1 and 11, the remaining limitations of claim 11 are respectively disclosed by *Conn* for the same reasons discussed above for the corresponding features of claim 1 in §§XI.B.2 through XI.B.5.

I. Claim 12

The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.

105. Aside from depending on claim 11, claim 12 is substantially similar to claim 2. *Supra*, §VII.B. Thus, claim 12 is anticipated by *Conn* for the reasons discussed for claims 11 and 2. *Supra*, §§XI.H and XI.C.

J. Claim 14

The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias in a straight line along a periphery of said semiconductor substrate.

106. Aside from depending on claim 11, claim 14 is substantially similar to claim 4. *Supra*, §VII.B. Thus, claim 14 is anticipated by *Conn* for the reasons discussed for claims 11 and 4. *Supra*, §§XI.H and XI.D.

K. Claim 15

The method of claim 14, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

107. Aside from depending on claim 11, claim 15 is substantially similar to claim 5. *Supra*, §VII.B. Thus, claim 15 is anticipated by *Conn* for the reasons discussed for claims 11 and 5. *Supra*, §§XI.H and XI.E.

L. Claim 17

The method of claim 11, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

108. Aside from depending on claim 11, claim 17 is substantially similar to claim 7. *Supra*, §VII.B. Thus, claim 17 is anticipated by *Conn* for the reasons discussed for claims 11 and 7. *Supra*, §§XI.H and XI.F.

M. Claim 19

The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate.

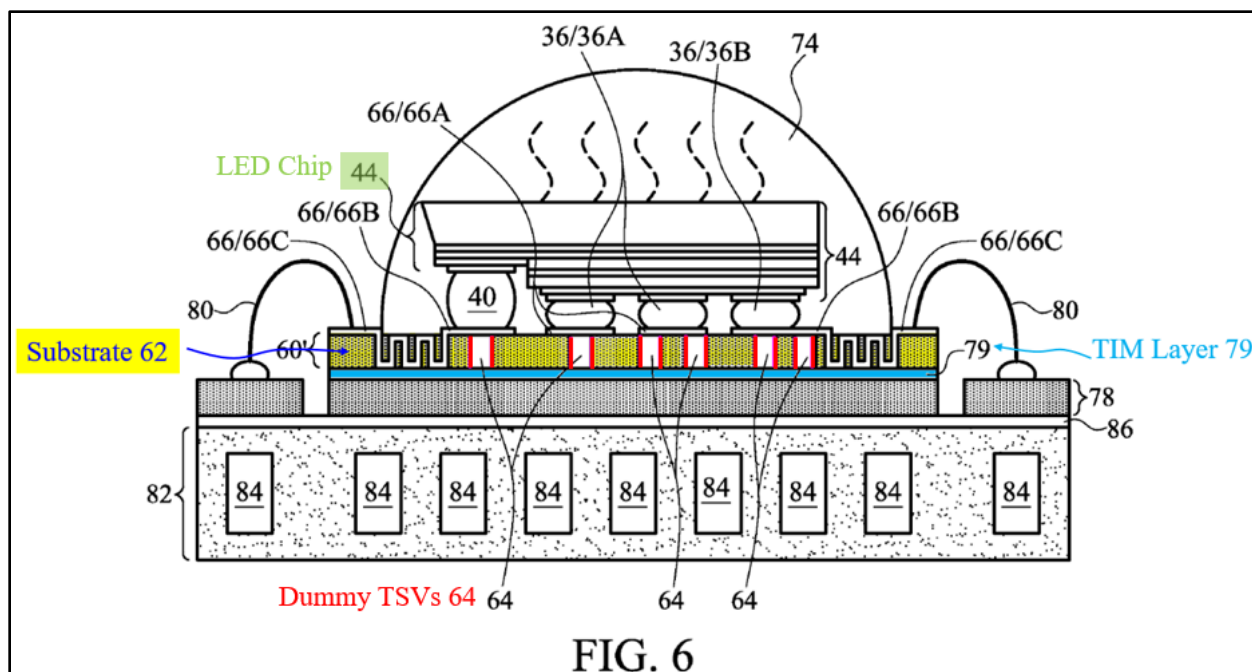
109. Aside from depending on claim 11, claim 19 is substantially similar to claim 9. *Supra*, §VII.B. Thus, claim 19 is anticipated by *Conn* for the reasons discussed for claims 11 and 9. *Supra*, §§XI.H and XI.G.

XII. GROUND SET 2: CONN-BASED OBVIOUSNESS**A. Ground 2A: Conn in View of Knowledge of POSA Renders Claims 1, 2, 4-7, 9, 11, 12, 14-17, and 19****1. Claims 1 and 11: “backside metal layer” and “does not provide ground connection”**

110. As discussed in §§XI.B.4 and XI.B.5, *Conn* anticipates “a backside metal layer” and “said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.” Nevertheless, to the extent that HID may (erroneously) argue that *Conn* does not expressly disclose

“backside” or “active devices,” it is my opinion that these limitations would have been obvious based on *Conn* and a POSA’s knowledge.

111. Specifically, *Conn* discloses that its carrier substrate is used “for mounting of semiconductor chip devices and components.” *Conn*, [0003]; *see also Conn*, [0030], [0035]. *Conn* does not show how the chips are mounted, but a POSA would have known it. For example, *Wang* (*supra*, §VI.D.2) provides a use case for *Conn*’s carrier substrate. *Wang* discloses a carrier chip 60’ for mounting an LED chip 44. *Wang*, 3:64-67. As discussed in §VI.D.2, carrier chip 60’ includes a substrate 62, which is adhered to a lead frame 78 by a metal TIM layer 79. *Wang*, 4:18-19. The substrate 62 includes multiple dummy TSVs 64 for dissipating heat. The dummy TSVs 64 are connected to dummy bond pads 66A (on the top side of substrate 62) and TIM layer 79 (on the bottom of substrate 62). *Wang*, 3:21-22, 3:27-33, Fig. 6.



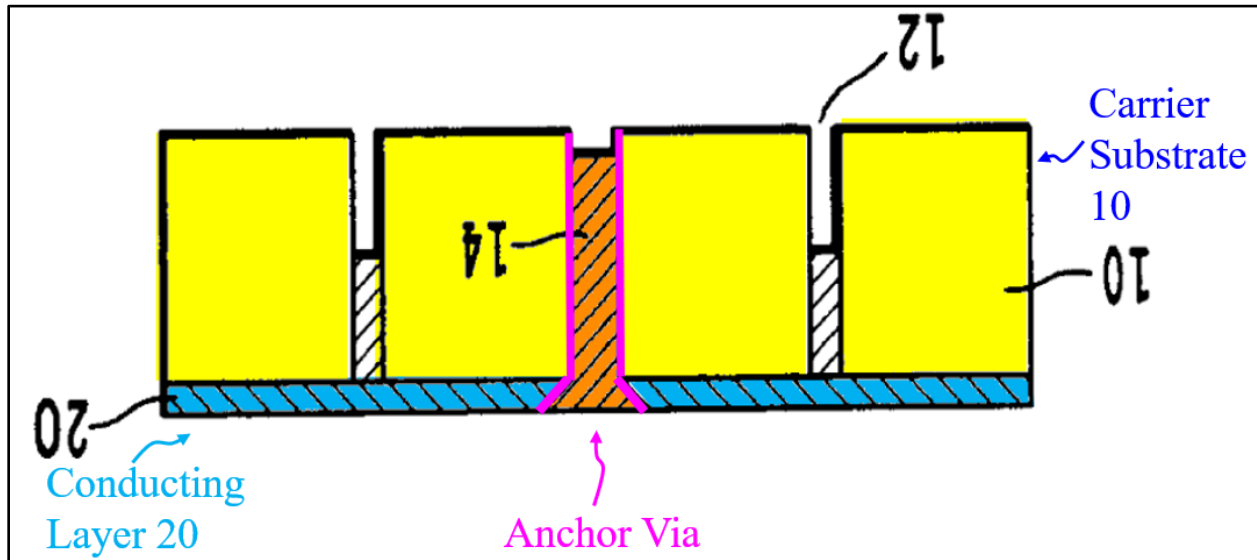
Wang, Fig. 6.

112. Both *Conn* and *Wang* are in the same field of endeavor as the '826 patent—semiconductor devices having via structures and methods of manufacturing them. *Conn* discloses using anchor vias in semiconductor device packages to secure conductive layer to carrier substrate. *Conn*, Abstract. And *Wang* discloses using dummy TSVs to dissipate heat in a packaged LED chip. *Wang*, 3:25-27. These are all in the same field of endeavor as the '826 patent, which describes a semiconductor device using anchor vias (e.g., [anchor vias 132](#), [133](#)) to improve backside metal adhesion to the substrate. *Supra*, §VII.A.

113. In my opinion, a POSA would have been motivated to use *Conn*'s electronic package structure for packing *Wang*'s LED chip. As shown below, the pair of carrier substrate 10 and **conducting layer 20** in *Conn*'s Figure 1 shares the

same relative positional relationship as *Wang*'s carrier substrate 60 and TIM layer 79. Compare *Wang*, Fig. 6, with *Conn*, Fig. 1. Moreover, both *Conn* and *Wang* concern heat dissipation in electronic package. *Conn*, [0030] (using the conducting layer for "dissipating heat from mounted IC chips"); *Wang*, 4:36-38 ("The package component is thus suitable for being used for high-power LED devices where heat dissipation is important to optimal device operation."). Further, both *Conn*'s conducting layer and *Wang*'s TIM layer are intended to be capable of covering the entire surface of the carrier substrate and bonding the carrier substrate to a lead frame. *Conn*, [0030]-[0031] (the conducting layer can cover more than 90% of the substrate surface and is not for use as signal lines); *Wang*, 4:12-15 (carrier chip 60' is adhered to a lead frame 78 through TIM layer 79); *supra*, §VI.C (backside metal layer like *Conn*'s conducting layer was a well-known way of bonding semiconductor die to a lead frame). Additionally, *Conn* allows metal layers overlying the substrate. Compare *Conn*, Fig. 3 ("conducting layer 30"), [0037] ("The conducting layer 30 can have the same or different area coverage as ... conductive layer 20."), with *Wang*, Fig. 6 ("dummy bond pads 66A"), 3:21-22, 3:27-33 (disclosing dummy bond pads 66A are connected to dummy TSVs 64). Therefore, a POSA would have appreciated that *Conn*'s electronic package structure is suitable for use in *Wang* to mount the LED chip 44. Namely, *Conn*'s carrier substrate 10 and conducting layer 20 can serve as *Wang*'s carrier substrate

62 and TIM layer 79, respectively. And Conn's anchor vias substitute Wang's dummy TSVs 64 to achieve the dual purpose of improving Wang's heat dissipation and metal layer adhesion (i.e., securing one or both of TIM layer 79 and dummy bond pads 66A).



Conn, Fig. 1 (rotated by 180°).

114. In the Conn-Wang use case, Conn's conducting layer is disposed on a side of the carrier substrate opposite to the LED chip—active device, thereby constituting a backside metal layer. *Supra*, §VI.B. And, the via conductors in Conn's anchor vias do not provide ground connection to the LED chip, because they are dummy vias designed for dissipating heat and securing backside metal, but *not* for providing electrical connection. *Conn*, [0011]; *Wang*, 3:23-27; *supra*, §XI.B.5.

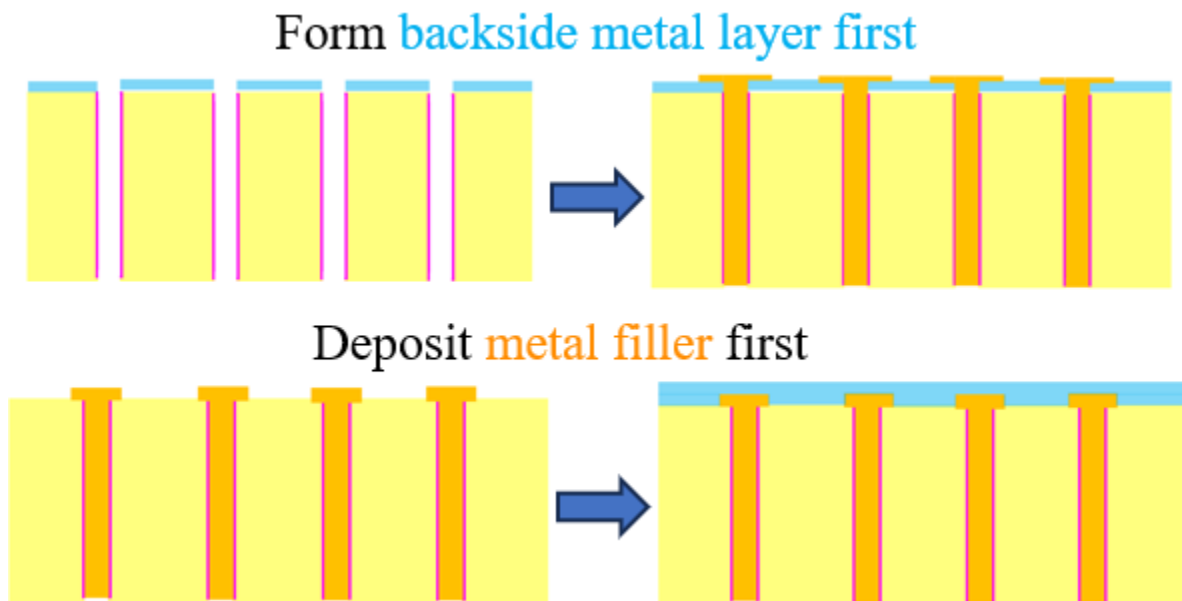
115. Accordingly, considering the actual use cases of *Conn*'s electronic page, it is my opinion that *Conn* renders obvious the "backside metal layer" and "not provide ground connection" limitations. A POSA would have had a reasonable expectation of success in implementing *Conn* with these limitations because doing so would have simply required using *Conn* as it was intended, that is, "for mounting of semiconductor chip devices and components," in a known way.

2. Claim 11: recited order of the steps

116. As discussed in §XI.H.1, the '826 patent does not require the steps in claim 11 to be performed in their recited order or sequence, and *Conn* anticipates each and every one of these steps. Nevertheless, to the extent that HID may (erroneously) argue that the sequence is required, a POSA would have found it obvious to modify the method in *Conn*'s Figure 7, to perform step 720 (i.e., claim [11b] "depositing" via metal filler) before step 710 (i.e., claim [11c] "forming" backside metal layer).

117. Specifically, *Conn* discloses that the conductive layer 20 and via conductors 14 can be made "during a same step," *Conn*, [0041], or "in separate process steps." *Conn*, [0033]. In both options, it would have been obvious to deposit the via metal filler before forming backside metal layer.

118. First, when *Conn*'s steps 710 and 720 are combined into the same step, the order of depositing via metal filler and forming the backside metal layer is simply a design choice, and may merely depend on how the metal sputtering machine or MOCVD is programed. *Conn*, [0055]. Moreover, choosing which order is a matter of convenience, and does not meaningfully affect the structure of the end product. As illustrated below, both orders can result in the rivet structure taught by *Conn*, so a POSA would have a reasonable expectation of success to deposit the via metal filler before forming backside metal layer.

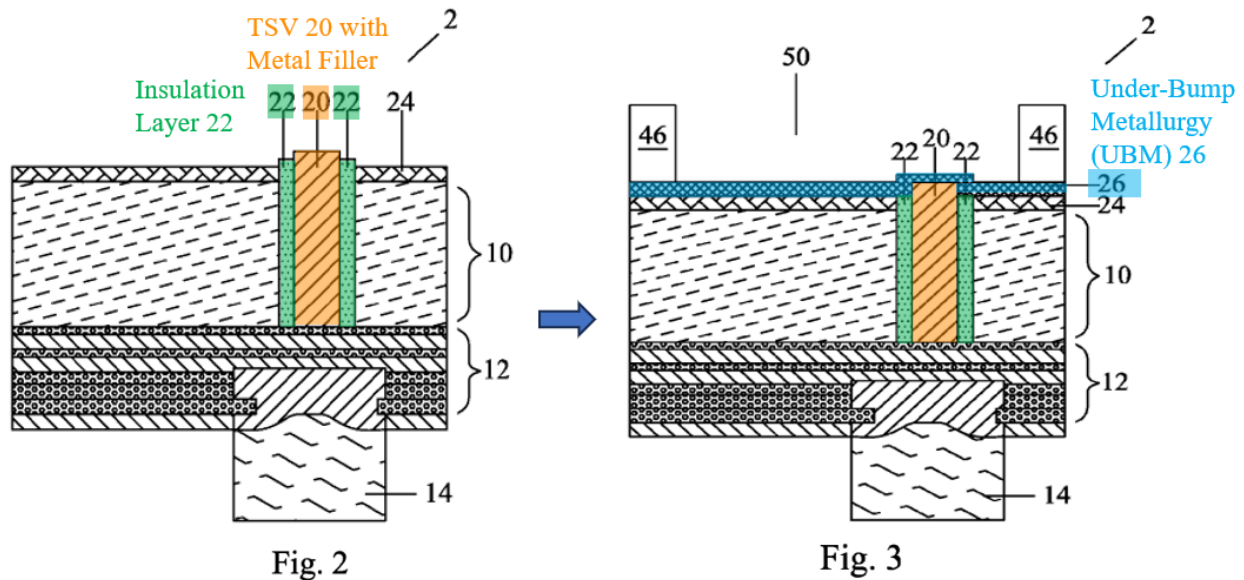


119. Second, when *Conn*'s steps 710 and 720 are performed as separate process steps, a POSA would have found it obvious to perform step 720 before step 710. A POSA would have been motivated to do so because depositing the via metal filler immediately after forming the vias, without being interrupted by the step of forming the backside metal layer, offers some advantages to the fabrication

process. For instance, this can minimize the time during which the via sidewall is exposed to the ambient air, thus avoiding contaminants from being introduced into the vias. As another example, before the metal is filled into the anchor vias, intermediate layers such as an insulating liner or diffusion barrier layer may need to be formed on the via sidewall first. In this case, it is desirable to deposit the via metal filler immediately after the intermediate layers are formed, to maximize adhesion between the metal filler and the intermediate layers. Moreover, a POSA would have had a reasonable expectation of success in changing the sequence of steps 710 and 720. Particularly, the modified sequence of processes is predictable because it had been used in the art before the time of the '826 patent. For example, in the same field of endeavor as the '826 patent (i.e., semiconductor devices having via structures and methods of manufacturing them), *Hsu* (Ex. 1026) illustrates a process in which TSV metal filler is deposited first to form a protrusion on a surface of a substrate, and then an under-bump metallurgy (UBM) layer—backside metal—is deposited on the TSV protrusion. *Hsu*, [0016] (“Semiconductor devices, such as transistors (not shown), may be formed at the front surface (the surface facing down in FIG. 2) of substrate 10.”), [0017] (“TSV 20 is formed in substrate 10, and extends from the back surface (the surface facing up in FIG. 2) to the front surface (the surface with active circuits formed thereon).”), [0018]

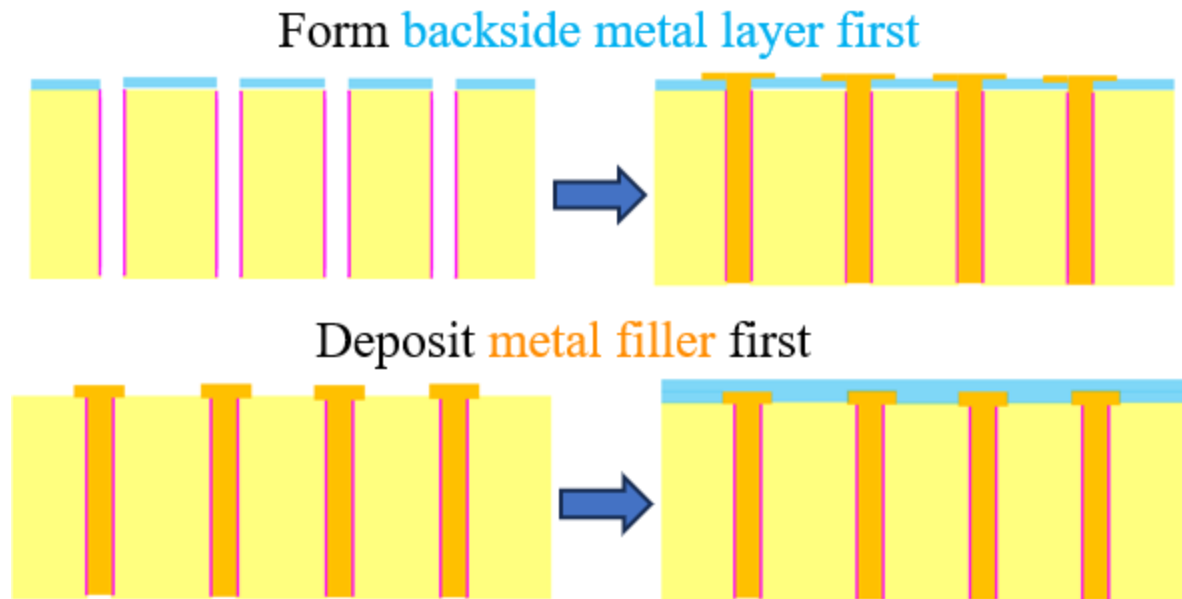
(“TSV 20 is exposed through the back surface of substrate 10.”), [0019]

(discussing forming the **UBM layer**), Figs. 2-3.



Hsu, Figs. 2-3.

Also, the modification would yield a predictable result because, as discussed above, depositing the **metal filler** before forming the **backside metal layer** would still result in the rivet structure taught by *Conn*.



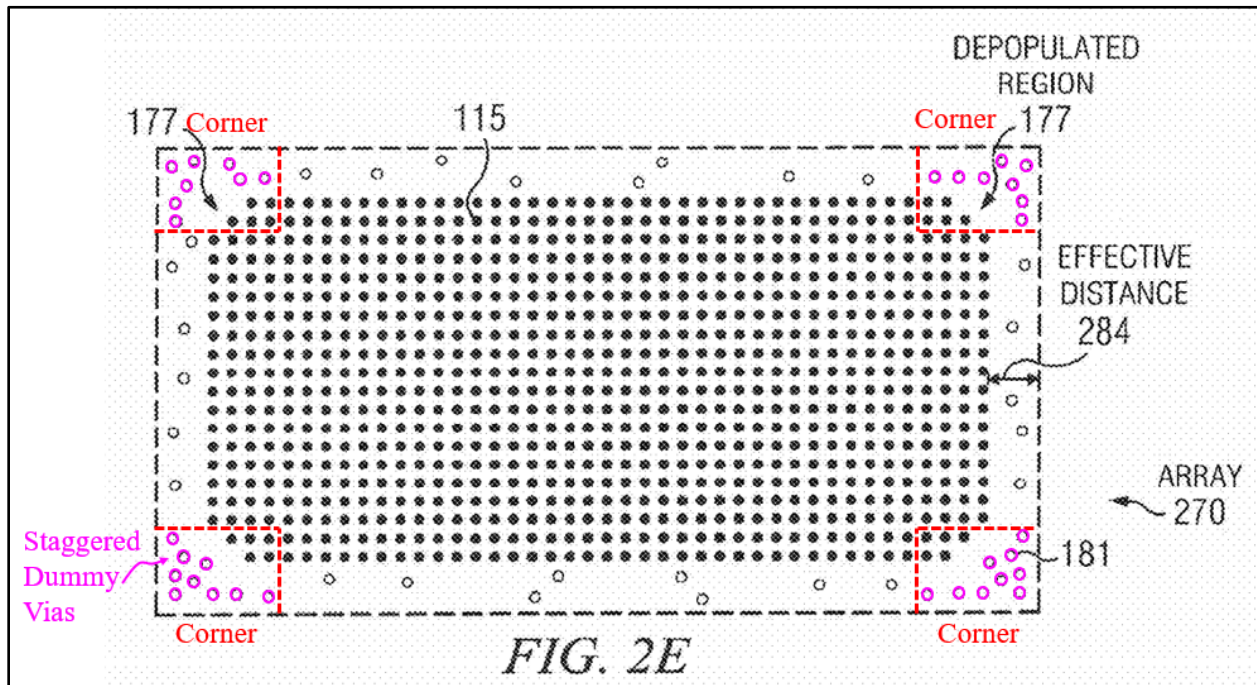
3. Remaining limitations of claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19

120. *Conn* discloses the remaining limitations of claims 1, 2, 4, 5, 7, 11, 12, 14, 15, and 17 for the reasons discussed in Ground 1. *Supra*, §§XI.B through XI.M.

4. Claims 6 and 16: “a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate”

121. *Conn* in view of a POSA’s knowledge renders obvious claims 6 and 16. Figure 2 of *Conn* shows that the anchor via array has a regular matrix-like pattern, in which the anchor vias repeat in the length direction and the width direction of the conducting layer according to a defined pitch. *Conn*, [0035], Fig. 2. But *Conn* also discloses that “[o]ther distribution patterns and irregular distribution patterns are also permissible and may be needed to accommodate chip attachment.” *Conn*, [0035]. In my opinion, a POSA would have understood that the

“irregular distribution patterns” can be a staggered distribution along a periphery of a semiconductor substrate. For example, *West* shows “randomly (i.e. aperiodically) positioned **dummy TSVs 181**” that have a staggered distribution. *West*, [0031].



West, Fig. 2E.

122. A POSA should have understood that such staggered pattern can be used to accommodate chip attachment. For example, *West* discloses the **staggered dummy vias** are used to reduce structural stresses and “can act as sacrificial stress absorbers” in “3D-IC” when, e.g., “the TSV die (or wafer) is assembled face down, such as being bonded to pads of a package (e.g. organic) substrate.” *West*, [0026]-[0027]. As another example, *Dean* (Ex. 1006) discloses that “reduc[ing] a number of the linearly aligned TSVs” can “result[] in less wafer breakage.” *Dean*, Abstract. *West* and *Dean* both pertain to semiconductor devices having via structures and

methods of manufacturing them. They are thus analogous to the '826 patent, which describes a semiconductor device with both electric TSVs (e.g., electrical [TSV group 120](#)) and anchor vias (e.g., [anchor vias 132, 133](#)). *Supra*, §VII.A. As such, a POSA would have been motivated to arrive at the claimed staggered pattern to prevent wafer breakage during chip attachment.

123. Moreover, a POSA would have understood that the staggered pattern is structurally more stable than a linear pattern. By adopting a staggered pattern, the same level of securing the conducting layer to the carrier substrate can be achieved by using less anchor vias. A POSA would have understood that using less vias is beneficial because it can reduce the stress induced by the vias. *Supra* (discussion of *West*). Therefore, a POSA would have been motivated to adopt the staggered pattern.

124. Additionally, there would have been a reasonable expectation of success for applying the staggered pattern to *Conn* because it expressly discloses that an irregular pattern, of which a POSA would understand a staggered pattern is an example, is “permissible.” *Conn*, [0035].

125. Accordingly, in my opinion, *Conn* in view of a POSA’s knowledge renders obvious the anchor vias with “staggered configuration,” as recited in claim 6. Claim 16 differs from claim 6 only by reciting a step for “forming” such anchor

vias, *supra*, §VII.B, and thus is obvious for the same reasons discussed for claim 11 and 6.

B. Ground 2B: *Conn* in View of Knowledge of POSA and AAPA Renders Obvious Claims 8 and 18

1. Claim 8

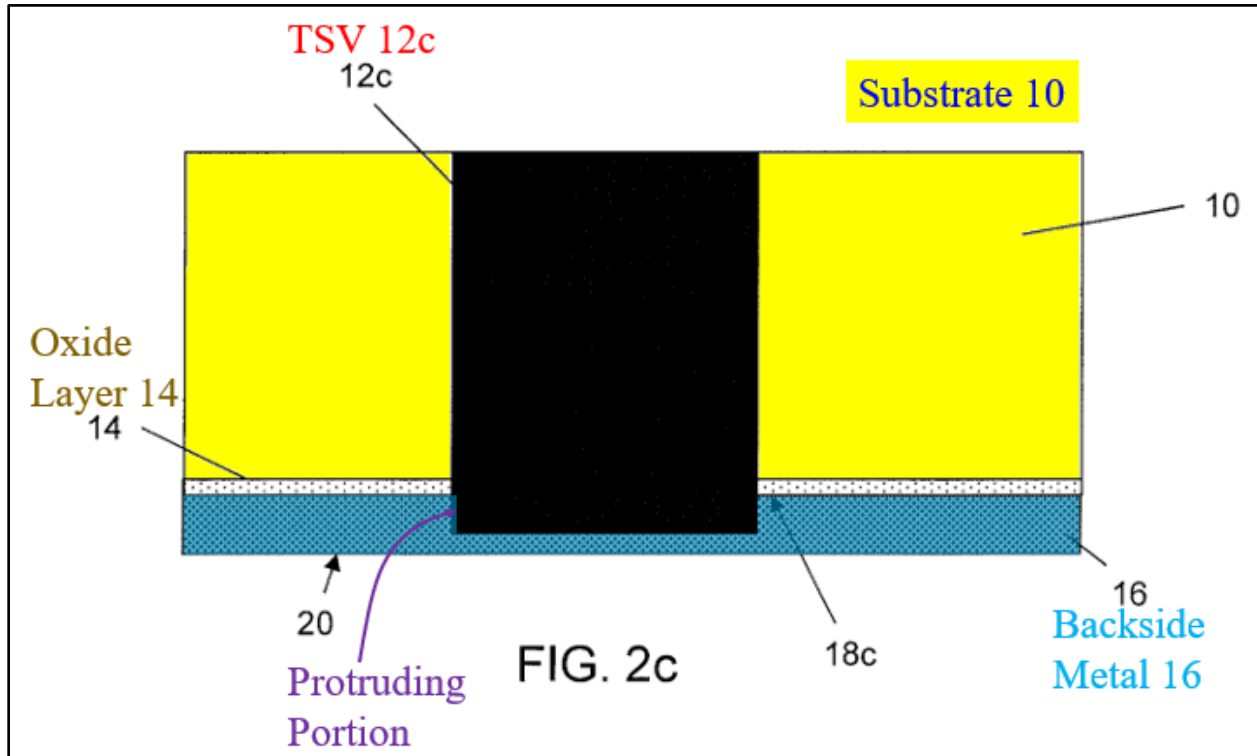
The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

126. AAPA discloses the three-layer backside metal stack in claim 8 had been used as a conventional method of adhering a backside metal layer to a substrate.

One conventional method of adhering a backside metal layer to a substrate relies on forming a backside metal stack having several layers, the first of which must form an adhesive bond with the substrate. For example, an interface layer may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer.

'826 patent, 1:24-30. In my opinion, *Conn* in view of a POSA's knowledge and AAPA renders obvious claim 8. As discussed in §VI.E, the idea of using both TSV and intermediate adhesion layer to improve backside metal adhesion was not new. For example, *Burnham* combines both TSVs and an oxide layer (as an intermediate adhesion layer) in a solution to improve the adhesion. *Burnham*, 5:8-13, 5:24-26. A

POSA would have been motivated to combine *Conn*'s anchor vias with other backside-metal-adhesion methods.



Burnham, Fig. 2c.

127. Moreover, as discussed below, a POSA would have appreciated that *Conn*'s anchor vias and AAPA's three-layer stack are complimentary solutions, and thus been motivated to harvest their respective benefits for improving the backside metal adhesion. Particularly, *Conn* addresses the metal adhesion problem during usage of a packaged chip. *Conn*, [0005]. A POSA would have understood that using a large number or density of *Conn*'s anchor vias in the substrate may have certain drawbacks. For example, using a large number of vias may induce excessive stress to the substrate or make the substrate prone to break. *Supra*,

§XII.A.4 (discussing teachings of *West* and *Dean*). For example, *West* discloses that the via filler material (e.g., copper in *Conn*) has “a significantly higher coefficient of thermal expansion (CTE) as compared to conventional IC substrates, such as silicon.” *West*, [0005]. “This CTE mismatch (Δ CTE) can result in significant thermally induced stress in the silicon including the circuitry (e.g. MOS transistors) in the silicon surrounding the TSVs, particularly during certain fab processing subsequent to the fabrication of the TSV (e.g., 360 to 410° C. sinters), during assembly and test/operations as may occur during solder reflow (e.g., up to about 260° C.) or during thermo-compressive bonding (e.g., up to 400° C.), during certain temperature cycle reliability testing (e.g., –55° C. to 125° C.), or even during long-term field operation of the IC.” *West*, [0005]. A POSA thus would have appreciated the need to balance the anchor vias’ benefit in securing conductive layers to the substrate against their potential adverse effect to the chip packaging reliability. To that end, a POSA would have been motivated to “increase the anchor vias’ “spacing ... [to] reduce[] stress,” (*West*, [0006]), while using AAPA’s three-layer backside metal stack to supplement the adhesion. Although AAPA discloses that the three-layer stack is not capable of completely preventing the backside metal layer peeling from the semiconductor substrate during fabrication of the chip, (’826 patent, 1:30-38), this problem can be cured by placing *Conn*’s anchor vias only at certain strategic locations, such as “near the

edges and/or corners of the die” where the backside metal is easy to peel off. ’826 patent, 1:30-33. As such, combining *Conn* and AAPA would yield a solution that ensures backside metal adhesion at both the fabrication and usage stages of the chip, while free of the respective potential drawbacks of the anchor vias and three-layer backside metal stack. Indeed, the AAPA discloses that the art had recognized “the backside metal layer must remain securely attached to the substrate **throughout the entire fabrication process and then for years during operation.**” ’826 patent, 1:30-38 (emphasis added). This goal can be achieved by combining *Conn* and AAPA.

128. The above proposed combination is predictable because it only requires combining the known elements from the prior art—*Conn*’s anchor vias and AAPA’s three-layer stack of backside metal—without modification to each element’s structure or manufacturing process. Structure wise, the combination only requires substituting AAPA’s three-layer backside metal stack to *Conn*’s conductive layer, without changing the existing anchor via structure. And, process wise, the combination only requires adding additional steps of depositing the additional layers of backside metal. The steps would not interfere with the anchor via formation. Moreover, as discussed in §§VI.C (*Cronin*) and VI.E (*Sharma*), the multi-layer backside metal stack was a mature technique dating back to the 1980s.

A POSA would have thus had a reasonable expectation of success in adding AAPA's three-layer stack to *Conn*, which would result in the claimed combination.

2. Claim 18

The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of: forming an interface layer; forming a conduction layer; forming a packaging layer.

129. Claim 18 differs from claim 8 only by reciting steps for “forming” the three-layer backside metal stack. *Supra*, §VII.B. Thus, claim 18 would have been obvious over *Conn* in view of a POSA's knowledge and AAPA for the same reasons discussed for claim 11 and 8.

XIII. GROUND SET 3: *GAMBINO*-BASED OBVIOUSNESS

A. Overview of the *Gambino* Combinations

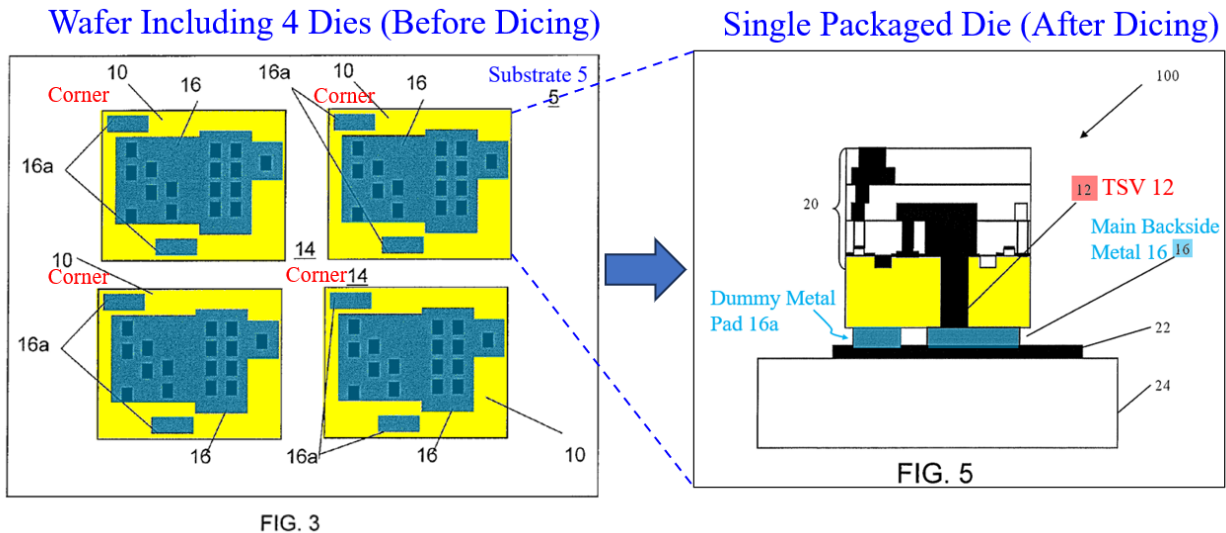
1. *Gambino*

130. *Gambino* discloses that a backside metal layer can be formed on a wafer to provide ground connections to TSVs, but it is prone to peeling from the semiconductor substrate during dicing process when the wafer is cut into individual dies. *Gambino*, [0016]. As shown below, to address this problem, *Gambino* proposes patterning the backside metal layer to avoid the dicing channels 14 and cover only selected locations in each die 10. *Gambino*, [0015], [0017], [0023]-[0027]. Consequently, the resulting die (Figure 5, after dicing) includes a main backside metal 16 covering an area including the TSVs 12, and dummy metal

pads 16a “at strategic locations on the dies 10 to provide mechanical support,”

“such that the die 10 will sit flatly on the package substrate, during packaging.”

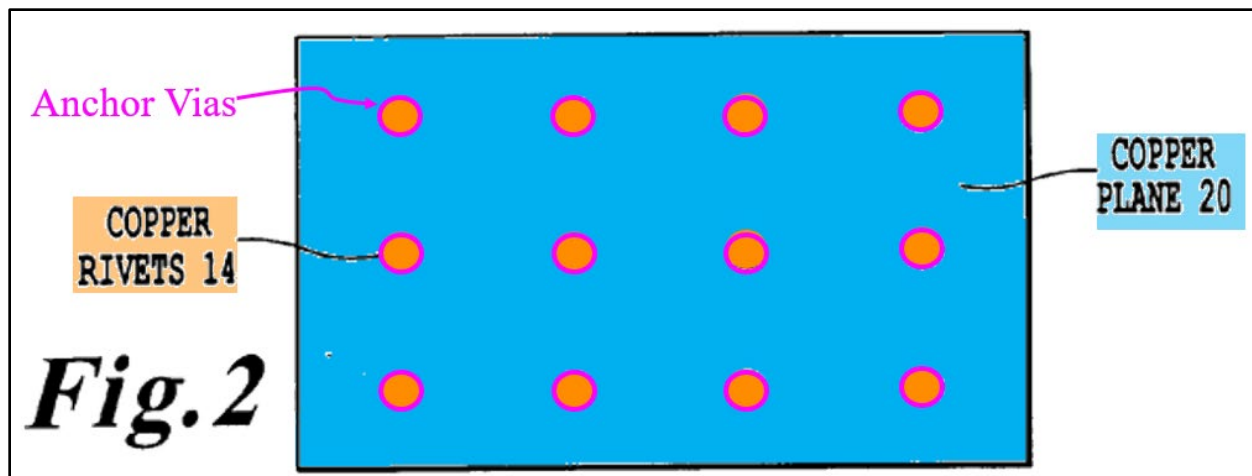
Gambino, [0027]-[0028].



Gambino, Figs. 3 and 5.

2. Conn

131. *Conn*, as discussed in §XI.A, discloses using anchor vias to secure a metal layer to a semiconductor substrate surface. *Conn*, Abstract, [0028], [0035].

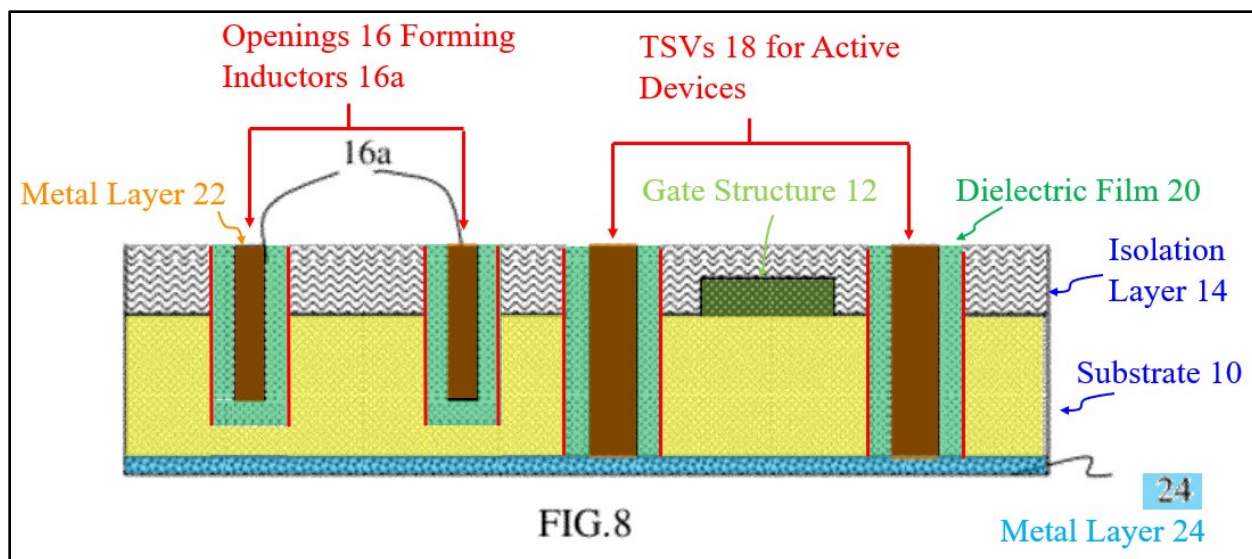


Conn, Fig. 2.

3. *Ding*

132. *Ding* proposes utilizing TSV processing to manufacture high-Q value inductors, to reduce cost.⁷ *Ding*, [0003], [0015]. Figure 8 shows that **openings 16** and traditional **TSVs 18** are created using the same TSV processing technique. *Ding*, [0016], [0018]-[0019], [0021]-[0025]. **TSVs 18** are used for connecting active devices like **gate structure 12**, while **openings 16** are used to make inductors, a type of passive device. *Ding*, [0002], [0015], [0024].

⁷ “High-Q” standards for high quality, meaning the inductor has low power loss and is suitable for high-frequency applications. *Ding*, [0003].



Ding, Fig. 8.

133. In my opinion, *Gambino*, *Conn*, and *Ding* are all analogous to the '826 patent because they are in the same field of endeavor as the '826 patent—semiconductor devices having via structures and methods of manufacturing them. Specifically, *Gambino* pertains to packaged devices with TSVs and discloses methods of patterning backside metal for use with the TSVs. *Gambino*, Abstract. *Conn* is directed to using anchor vias in semiconductor device packages. *Conn*, Abstract. *Ding* proposes using TSV-manufacturing methods to simultaneously fabricate TSVs and inductors. *Ding*, Abstract, [0005], [0008]-[0009]. These are all in the same field of endeavor as the '826 patent, which describes a semiconductor device with both electric TSVs (e.g., electrical [TSV group 120](#)) and anchor vias (e.g., [anchor vias 132, 133](#)). *Supra*, §VII.A.

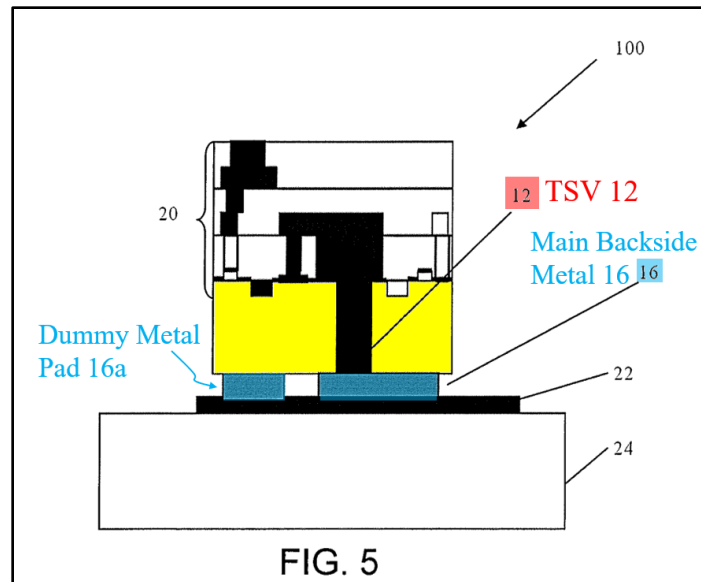
B. Ground 3A: *Gambino* in View of *Conn* Renders Obvious Claims 1, 2, 4-7, 11, 12, and 14-17

1. Rationale for combining *Gambino* with *Conn*

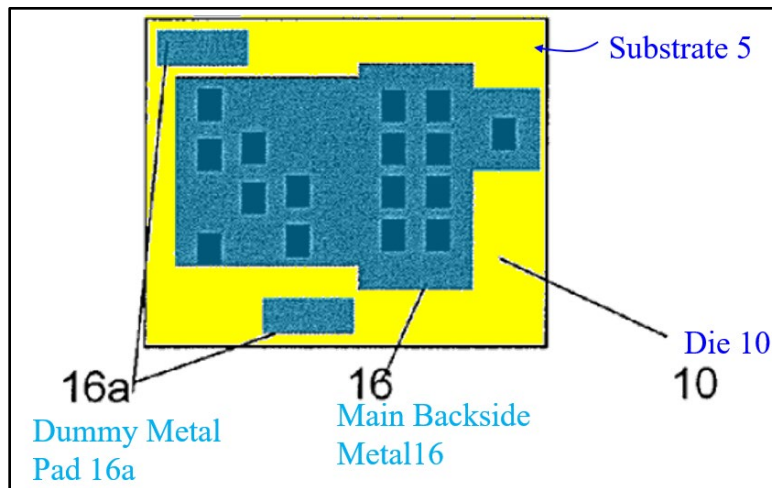
a. Proposed combination

134. Figure 5 of *Gambino* “shows a packaged module with a **backside metal ground plane** attached to a substrate.” *Gambino*, [0013], [0030]. The packaged module is based on a die generated after dicing a wafer. *Gambino*, [0005], [0017]. The package module includes **TSVs 12** “in electrical communication with” wiring layers 20, which include “active or passive devices.”⁸ *Gambino*, [0030]. Figure 3 (excerpted) shows the module’s **backside metal ground plane** includes a **main backside metal 16** covering the **electrical TSVs**, and one or more **dummy metal pads 16a** located at the corners and peripheries of the substrate “to provide mechanical support” to the module. *Gambino*, [0027]-[0028].

⁸ The **TSVs 12** in *Gambino* will be referred to as **electrical TSVs** hereafter.

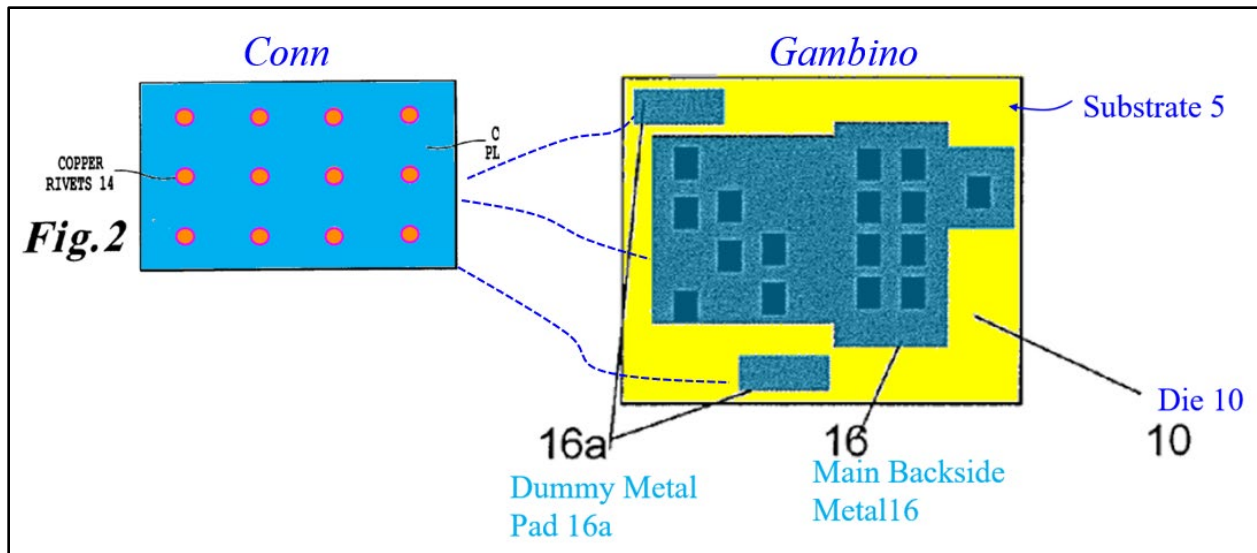


Gambino, Fig. 5.



Gambino, Fig. 3 (excerpted).

135. As shown below, a POSA would have found it obvious to apply *Conn*'s teachings, to create **anchor vias** in *Gambino*'s **dummy metal pads 16a** and/or **main backside metal 16**, to secure **them** to the substrate and prevent delamination during singulation.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

b. A POSA would have been motivated to combine *Gambino* and *Conn*

136. A POSA would have been motivated to combine the teachings of *Gambino* and *Conn* at least because both references are directed to improving structural integrity of packaged devices. *Gambino*, [0001] (“improved metal adhesion”), [0017] (“reducing the overall cost of the packaged module”); *Conn*, [0011] (“an electronic package includes a carrier substrate” and “to secure the [] conducting layer to the carrier substrate”). Since *Gambino* and *Conn* address the same problem (metal adhesion to substrate) in semiconductor packaging, a POSA would have considered them to be closely related and would have consulted both references’ teachings.

137. Moreover, a POSA would have found it desirable to combine the advantages proffered by *Gambino* and *Conn*. These two references tackle metal

adhesion problems occurring at different stages. *Gambino* concerns the backside metal peeling problem during dicing (i.e., at the manufacturing stage), while *Conn* addresses the metal delamination issue due to thermal fatigue during the usage of the packaged device. *Gambino*, [0016]; *Conn*, [0005]. It is thus attractive to combine *Gambino* and *Conn* to offer a metal adhesion solution covering the entire life cycle of a semiconductor device, from its manufacturing to usage. Particularly, in view of *Conn*'s teachings, a POSA would understand that the **dummy metal pads 16a** and **main backside metal 16** in *Gambino*'s packaged module have a high chance to delaminate from the substrate when the module is used in a computing device. *Conn*, [0005]-[0008]. Therefore, there would have been a desire to improve *Gambino* by adding *Conn*'s **anchor vias** at the **dummy metal pads 16a** and **main backside metal 16**, to ensure **they** remain secured to the substrate during the module's useful life.

138. Additionally, despite *Gambino*'s solution being able to “solve[] the metal peeling problem” during dicing, (*Gambino*, [0017]), a POSA would have understood that *Gambino*'s **dummy metal pads 16a** located at the corners and peripheries of the die are the most vulnerable during the dicing process. Yet, the **dummy metal pads 16a** are “at strategic locations on the dies” and indispensable to the module's structural “stability.” *Gambino*, [0028]. Therefore, a POSA would have wanted to use *Conn*'s **anchor vias** at the **dummy metal pads 16a** to reinforce

their adhesion, to provide a fail-safe or error-proof measure. This is important to ensuring the “die yield and reliability.” *Gambino*, [0016].

139. Moreover, *Gambino* is ready for improvement because it already uses **electrical TSVs** and employs a TSV manufacturing process. *Gambino*, [0020]. The anchor vias could be made using the same process.

140. Further, *Gambino* and *Conn* attack the backside metal adhesion problem from two different angles. *Gambino* patterns the **backside metal**, while *Conn* uses **anchor vias**. *Gambino*, [0015] (“patterned backside metal ground planes for improved metal adhesion”); *Conn*, [0030] (“the anchor via maintain the utility of the carrier substrate laminate to continue to dissipate heat and be a viable support”). A POSA would have been interested in combining these two techniques to maximize the backside metal adhesion.

c. The combination of *Gambino* and *Conn* would have yielded a predictable result

141. First, the structure of the resulting combination is predictable because it merely requires a simple incorporation of *Conn*’s **anchor vias** to *Gambino*’s substrate, and does not require any modification to *Gambino*’s overall die structure. Particularly, since the **anchor vias** are only formed at the backside of the substrate, they do not require redistribution of the active devices and wiring layers on the front side of the substrate. Moreover, *Gambino*’s **dummy metal pads 16a** are located at the corners and peripheries of the substrate, which are less crowded

areas that are not usually for planting active/passive devices, so adding the **anchor vias** here would not affect other elements in the devices.

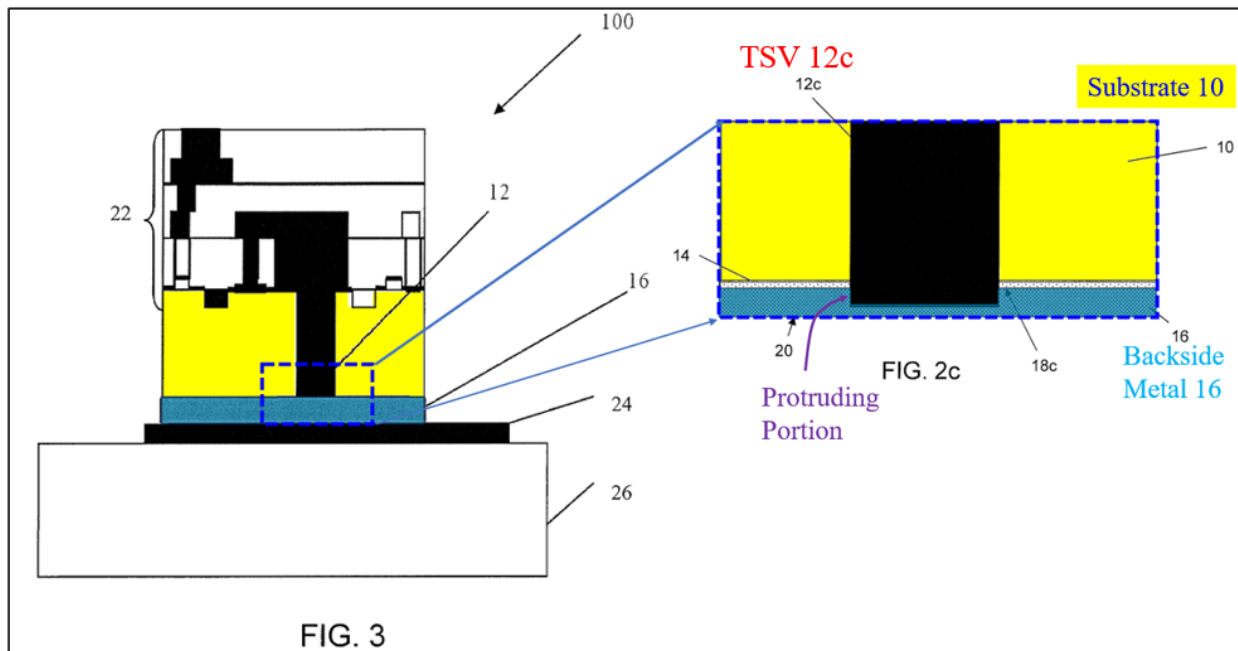
142. Second, the process of making the proposed combination is predictable because the same process used for manufacturing *Gambino*'s **electrical TSVs** can be used to manufacture the **anchor vias**. As discussed in §XII.A.2, *Gambino*'s manufacturing method (*Gambino*, [0020] – depositing the via **metal** before forming the **backside metal**) can yield the same rivet-like **anchor via** structure contemplated by *Conn*—the resulting **via conductors** will form **protruding portions** bonded to the **backside metal**. Thus, the proposed combination does not require modification to *Gambino*'s existing manufacturing method.

143. Third, the function of the resulting combination is predictable because the introduction of *Conn*'s **anchor vias** to *Gambino* will not affect the packaged module's electrical functions. The **anchor vias** themselves do not need to be connected to active or passive devices. *Supra*, §XI.B.5. *Gambino*'s **dummy metal pads 16a** also do not serve electrical functions. Thus, the **anchor vias**' presence will not change these devices' functioning.

144. Fourth, there would have been a reasonable expectation of success for the resulting combination because *Conn* discloses the **anchor vias** can secure **conducting layers** with sizes ranging from 10% to 100% of the substrate's total surface area. *Conn*, [0030]-[0031]. *Gambino*'s patterned **dummy metal pads 16a**

and **main backside metal 16** have sizes in this range, and thus can be securely held by the **anchor vias**.

145. Fifth, the proposed combination was well-known. For example, *Burnham* had already used via structures with protrusion portions to improve backside layer adhesion. *Supra*, §VI.E. A POSA would have appreciated that the proposed combination is simply replicating prior art and would have succeeded.



Burnham, Figs. 2c and 3.

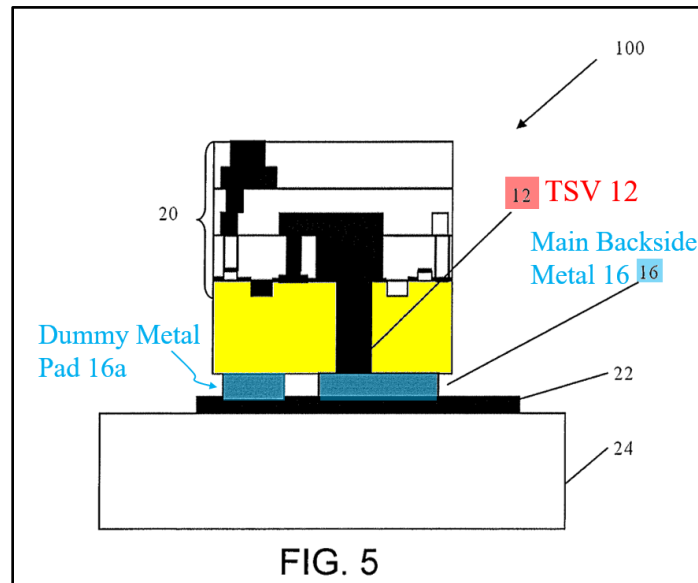
2. Independent Claim 1

a. [1pre] A structure comprising:

146. I was informed by counsel that the preamble of a claim is not necessarily limiting. Nonetheless, to the extent the preamble is limiting, in my opinion the combination of *Gambino/Conn* discloses a structure by disclosing a

packaged semiconductor device module as shown in *Gambino*'s Figure 5.

Gambino, [0030].



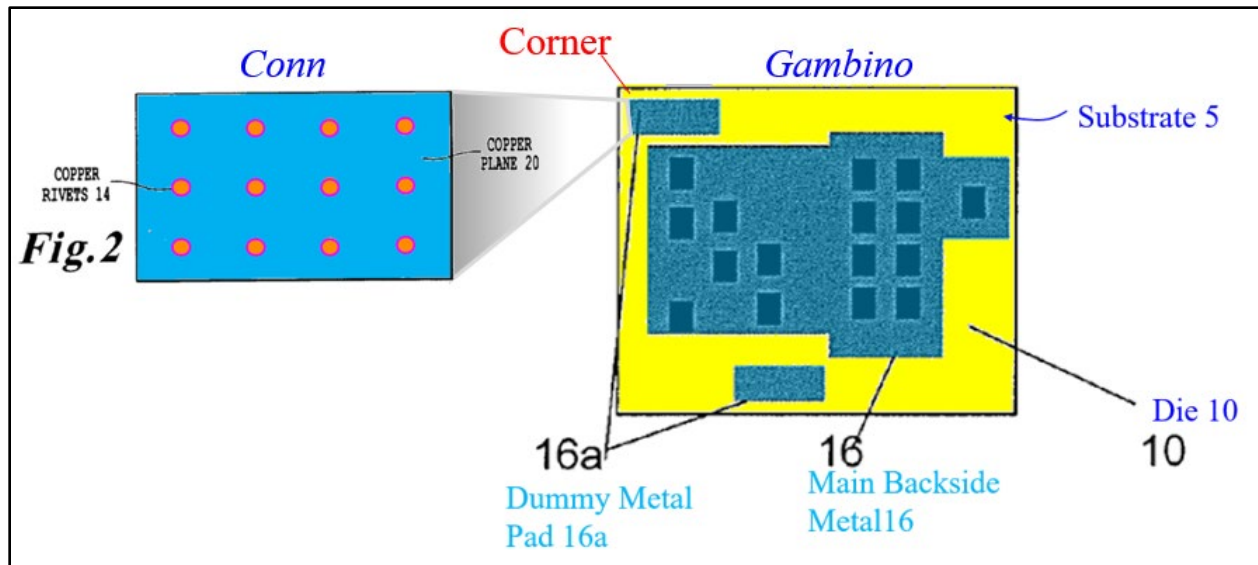
Gambino, Fig. 5.

- b. [1a] at least one **anchor via** disposed in at least one **corner** of a semiconductor substrate;

147. *Gambino/Conn* satisfies it by disclosing the **dummy metal pad 16a** is located in at least one **corner** of the substrate “to provide mechanical support.”

Gambino, [0028]; *see also Gambino*, [0019], [0027], [0030]. *Gambino* discloses the **dummy metal pads 16a** are placed “at strategic locations” to provide “stability on the backside of the die 10,” “such that the die 10 will sit flatly on the package substrate.” *Gambino*, [0028]. The **corner** is one of these strategic locations.

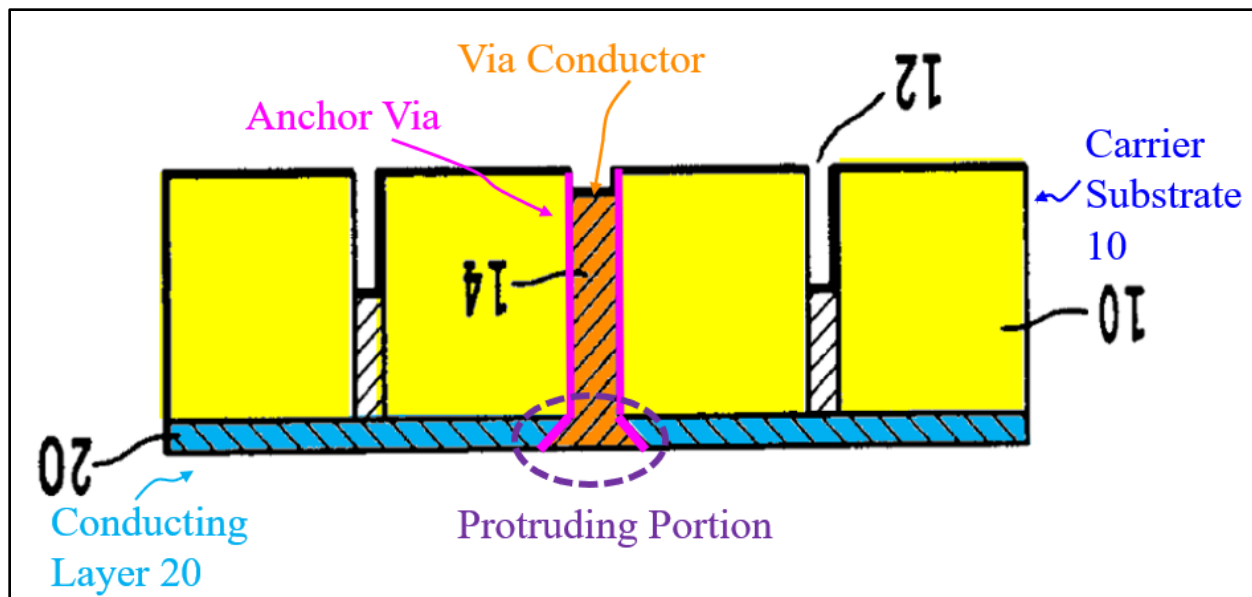
Therefore, *Gambino/Conn*'s **anchor vias** at the **corner**-located **dummy metal pad(s) 16a** meet claim [1a].



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

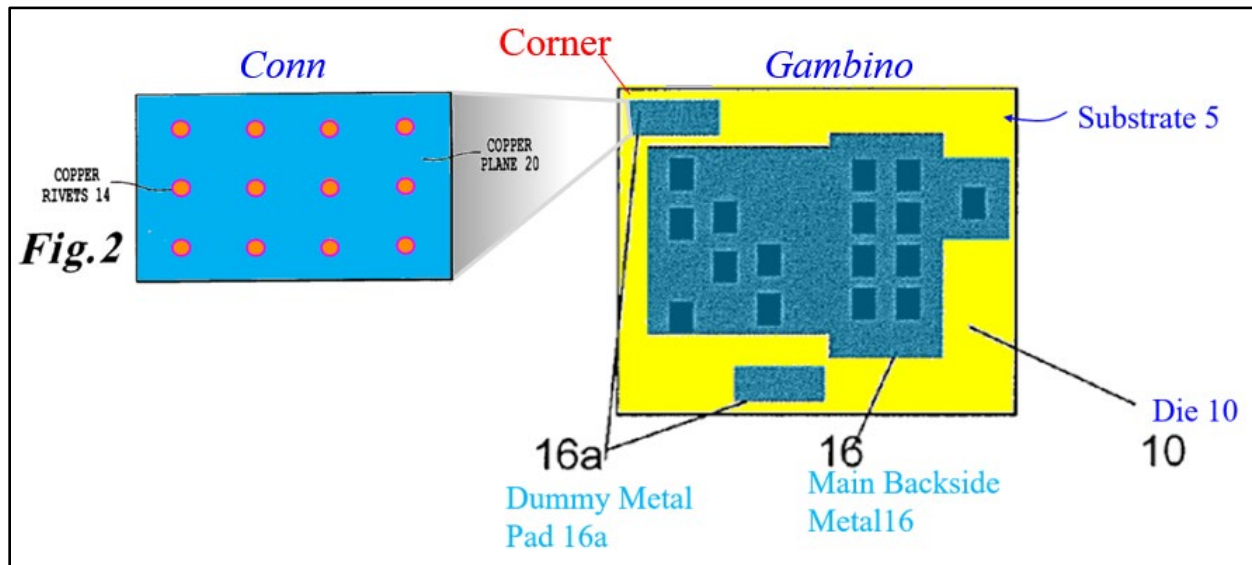
- c. [1b] a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

148. *Gambino/Conn* satisfies it because *Conn* discloses the via conductors in the anchor vias form protruding portions that are connected to a conducting layer. *Supra*, §XI.B.3.



Conn, Fig. 1 (rotated by 180°).

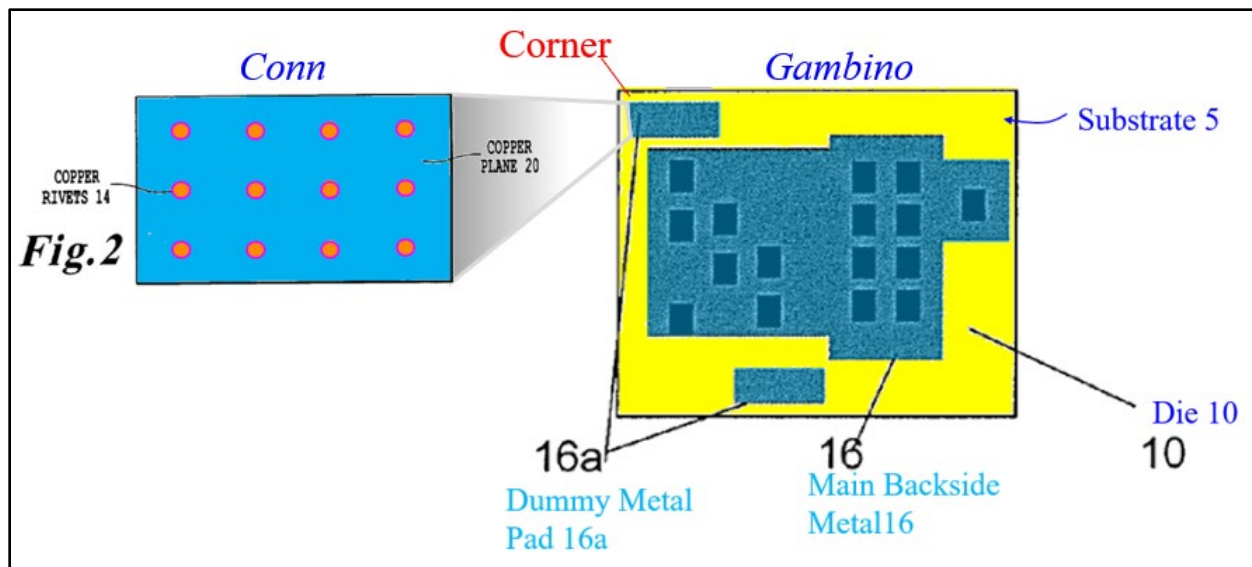
149. Applying *Conn*'s teachings to *Gambino*, a POSA would understand that the **anchor vias** in *Gambino/Conn* have **via conductors** forming **protruding portions** connected to the **corner-located dummy metal pad(s) 16a**.



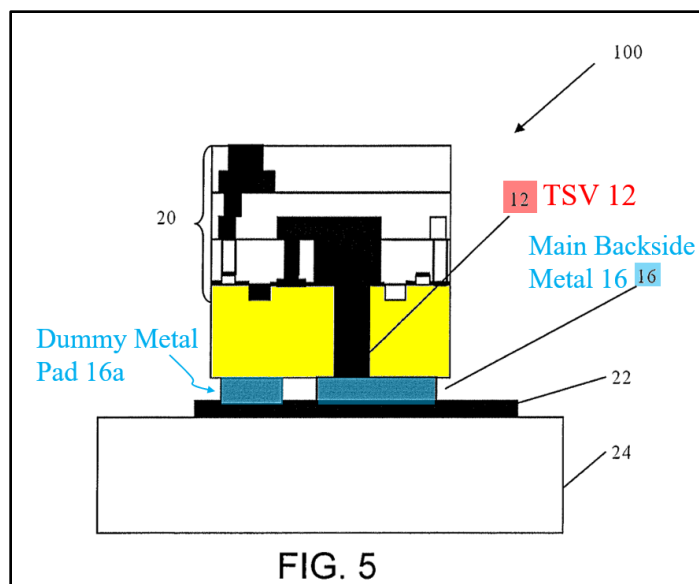
Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

- d. [1c] a **backside metal layer** on a bottom surface of said semiconductor substrate, said **backside metal layer** being bonded to said **protruding portion** of said **metal filler** of said at least one **anchor via**;

150. *Gambino/Conn* satisfies it because **corner**-located **dummy metal pad(s) 16a** discloses the claimed “**backside metal layer**.” Moreover, applying *Conn*’s teachings regarding the **anchor vias**, a POSA would understand the **protruding portions** are “bonded to” the **corner**-located **dummy metal pad(s) 16a**.
Supra, §XI.B.4.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Gambino, Fig. 5.

- e. [1d] wherein said **metal filler** within said at least one **anchor via** does not provide ground connection to one or more active devices in said semiconductor substrate.

151. *Gambino/Conn* satisfies it because the **corner**-located **dummy metal pad(s) 16a** is only used for mechanical support—not used for electrical connection, which means the **anchor vias** therein do not provide ground connection to active devices. *Gambino*, [0028], [0030].

3. Claims 2 and 4-7

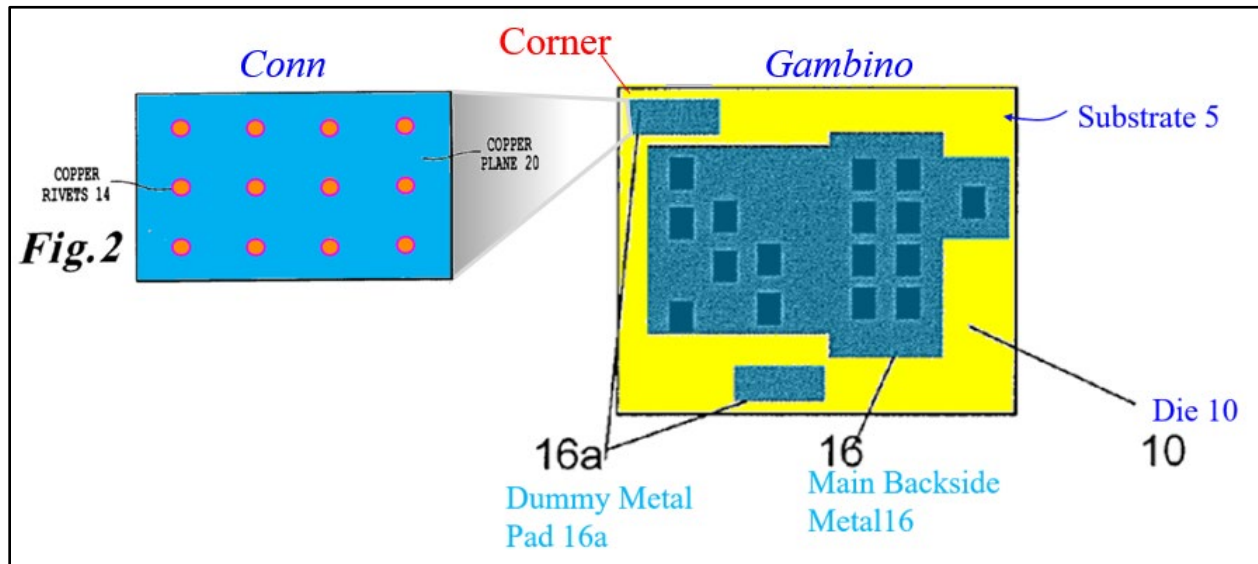
a. Claim 2

The structure of claim 1, wherein said at least one **anchor via comprises a cluster of **anchor vias**.**

152. Claim 2 recites the at least one **corner anchor via** “comprises a cluster of **anchor vias**.” ’826 patent, 8:4-5. *Gambino/Conn* meets it because *Conn*

discloses the **anchor vias** at the **corner**-located **dummy metal pad(s) 16a** are distributed in a pattern (i.e., “a cluster of **anchor vias**”) with certain densities.

Conn, [0035]-[0036]; *supra*, §XII.C (discussing *Conn*’s disclosure of claim 2).



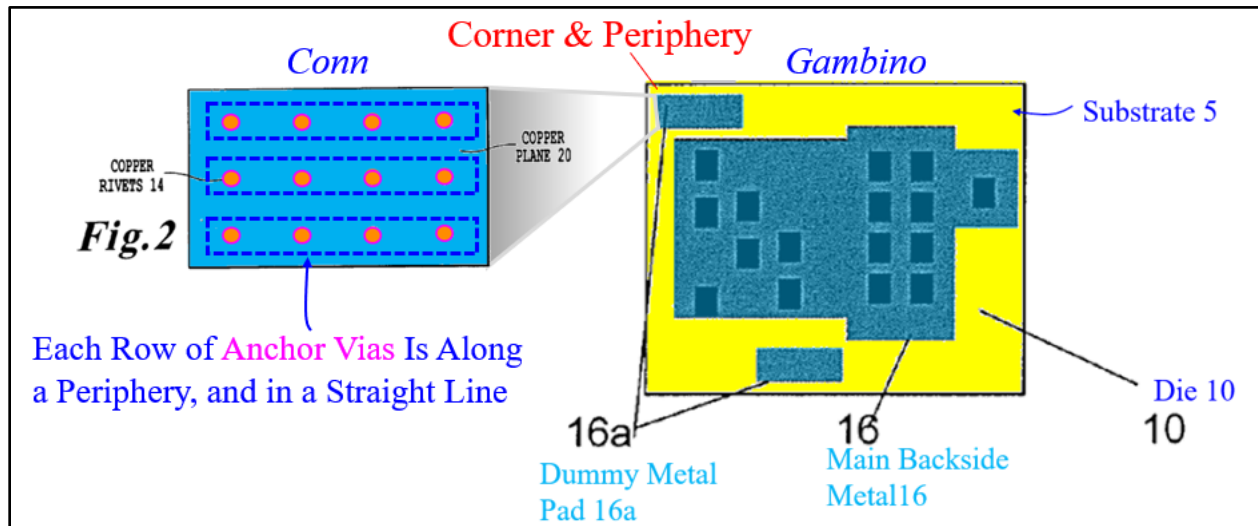
Gambino, Fig. 3 (excerpt); *Conn*, Fig. 2.

b. Claim 4

The structure of claim 1, wherein said at least one **anchor via** comprises a plurality of **anchor vias** disposed in a straight line along a periphery of said semiconductor substrate.

153. Claim 4 recites the at least one **corner**-located **anchor via** in claim 1 “comprises a plurality of **anchor vias** disposed in a straight line along a **periphery** of said semiconductor substrate.” ’826 patent, 8:10-12 (emphasis added). As illustrated below, *Gambino/Conn* meets it because *Gambino*’s **corner**-located **dummy metal pad(s) 16a** is located at a **periphery** of the substrate and *Conn* discloses the **anchor vias** therein can have a regular pattern (*Conn*, Fig. 2), in which

each row of the **anchor vias** is disposed in a straight line along a **periphery**. *Conn*, [0035]-[0036], Fig. 2; *see supra*, §XI.D (discussing *Conn*'s disclosure of claim 4).



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

c. Claim 5

The structure of claim 4, wherein a linear density of said plurality of **anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.**

154. Claim 5 recites the peripheral **anchor vias** in claim 4 has a linear density “less than approximately 10%.” ’826 patent, 8:13-16. *Gambino/Conn* meets it because *Conn* discloses the **anchor via** pattern at the periphery **corner-**located **dummy metal pad(s) 16a** has a linear density meeting this requirement. *Supra*, §XI.E (discussing *Conn*'s disclosure of claim 5).

d. Claim 6

The structure of claim 1, wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

155. Claim 6 recites the at least one corner-located anchor via in claim 1 “comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.” ’826 patent, 8:17-20 (emphasis added). *Gambino/Conn* discloses this feature because *Gambino*’s corner-located dummy metal pad(s) 16a is located at a periphery of the substrate and *Conn* renders obvious the anchor vias therein being staggered. *Conn*, [0035]; *supra*, §XII.A.4 (discussing *Conn*’s disclosure of claim 6).

e. Claim 7

The structure of claim 1, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

156. Claim 7 recites the corner anchor vias have a total area “less than approximately 0.5% of a total area of said semiconductor substrate.” ’826 patent, 8:21-23. *Gambino/Conn* discloses this feature because *Conn* discloses the anchor via pattern at the corner-located dummy metal pad(s) 16a has a total area meeting this requirement. *Supra*, §XI.F (discussing *Conn*’s disclosure of claim 7).

f. Rationale for obviousness

157. In addition to the reasons provided in §XIII.B.1, a POSA would have been motivated to apply *Conn*'s teachings regarding the patterns, linear densities, and total areas of the **anchor vias** because they are suitable for achieving *Conn*'s stated purpose of securing backside metal and preventing delamination. *Conn*, Abstract, [0011], [0030], [0035]-[0036].

158. A POSA would also have a reasonable expectation of doing so. First, since *Gambino*'s **corner**-located **dummy metal pad(s) 16a** does not provide electrical connection, applying *Conn*'s teachings would have no effect on the electrical functions of the chip. Second, both *Gambino* and *Conn* teach using Bosch deep reactive ion etching (DRIE) to form the vias. *Gambino*, [0020]; *Conn*, [0049], [0055]. Thus, a POSA would have reasonably expected that the same process used for creating *Gambino*'s TSVs can also be used to create the **anchor vias**, with the patterns, linear densities, and total areas specified by *Conn*. Third, *Conn*'s **anchor vias** and *Gambino*'s TSVs share similar parameters. *Gambino*, [0020] ("TSVs with almost any diameter, from the submicrometer level to hundreds of micrometers"); *Conn*, [0035] ("The vias 12 can have a diameter between 30 and 150 μm "). Thus, the sizes of *Conn*'s **anchor vias** fit for *Gambino*'s packaged module.

4. Independent Claim 11

a. “Forming,” depositing,” and “forming” steps

159. *Gambino/Conn* discloses the claimed method because *Gambino* discloses a TSV manufacturing method. *Gambino*, [0020]-[0021]. Specifically, *Gambino* discloses the claimed [11a] “forming at least one **anchor via**,” [11b] “depositing a **metal filler**,” and [11c] “forming a **backside metal layer**,” by disclosing:

- “a **via** can be formed in a front side of the die 10 using conventional lithography and etching processes” (*Gambino*, [0020]);
- “[a]fter formation of the via, **metal** can be deposited therein using conventional deposition processes such as, for example, electroplating or chemical vapor deposition techniques” (*Gambino*, [0020]); and
- “a **backside metal 16** is formed on the backside of the die 10, in contact with the TSVs 12” (*Gambino*, [0021]).

160. Although *Gambino* describes the above method as being used to make the **electrical TSVs**, a POSA would have been motivated to use it to also manufacture the **anchor vias**. By using the same process, the **electrical TSVs** and **anchor vias** would be formed at the same time. As such, the **anchor vias** can be added to the **dummy metal pad(s) 16a** for no additional processing or cost, and a POSA would have thus had a reasonable expectation of success in doing so.

Further, as discussed in §XIII.B.1.c, *Gambino*'s method can yield the same **anchor via** structure contemplated by *Conn*.

b. Remaining limitations of claim 11

161. The remaining limitations of claims 11 are substantially similar to those structural features recited in claim 1. *Supra*, §VII.B. Thus, given the similarity between claims 1 and 11, the remaining limitations of claim 11 are respectively taught by *Gambino* and *Conn* for the same reasons discussed above for the corresponding features of claim 1 in §§XIII.B.2.b through XIII.B.2.e.

C. Claim 12

The method of claim 11, wherein said forming said at least one **anchor via comprises forming a cluster of **anchor vias**.**

162. Aside from depending on claim 11, claim 12 is substantially similar to claim 2. *Supra*, §VII.B. Thus, claim 12 is taught by *Gambino* in view of *Conn* for the reasons discussed for claims 11 and 2. *Supra*, §§XIII.B.2 and XIII.B.3.a.

D. Claim 14

The method of claim 11, wherein said forming said at least one **anchor via comprises forming a plurality of **anchor vias** in a straight line along a periphery of said semiconductor substrate.**

163. Aside from depending on claim 11, claim 14 is substantially similar to claim 4. *Supra*, §VII.B. Thus, claim 14 is taught by *Gambino* in view of *Conn* for the reasons discussed for claims 11 and 4. *Supra*, §§XIII.B.2 and XIII.B.3.b.

E. Claim 15

The method of claim 14, wherein a linear density of said plurality of anchor vias is less than approximately 10% of a total linear distance of said straight line along said periphery of said semiconductor substrate.

164. Aside from depending on claim 11, claim 15 is substantially similar to claim 5. *Supra*, §VII.B. Thus, claim 15 is taught by *Gambino* in view of *Conn* for the reasons discussed for claims 11 and 5. *Supra*, §§XIII.B.2 and XIII.B.3.c.

F. Claim 16

The method of claim 11, wherein said forming said at least one anchor via comprises forming a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.

165. Aside from depending on claim 11, claim 16 is substantially similar to claim 6. *Supra*, §VII.B. Thus, claim 16 is taught by *Gambino* in view of *Conn* for the reasons discussed for claims 11 and 6. *Supra*, §§XIII.B.2 and XIII.B.3.d.

G. Claim 17

The method of claim 11, wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.

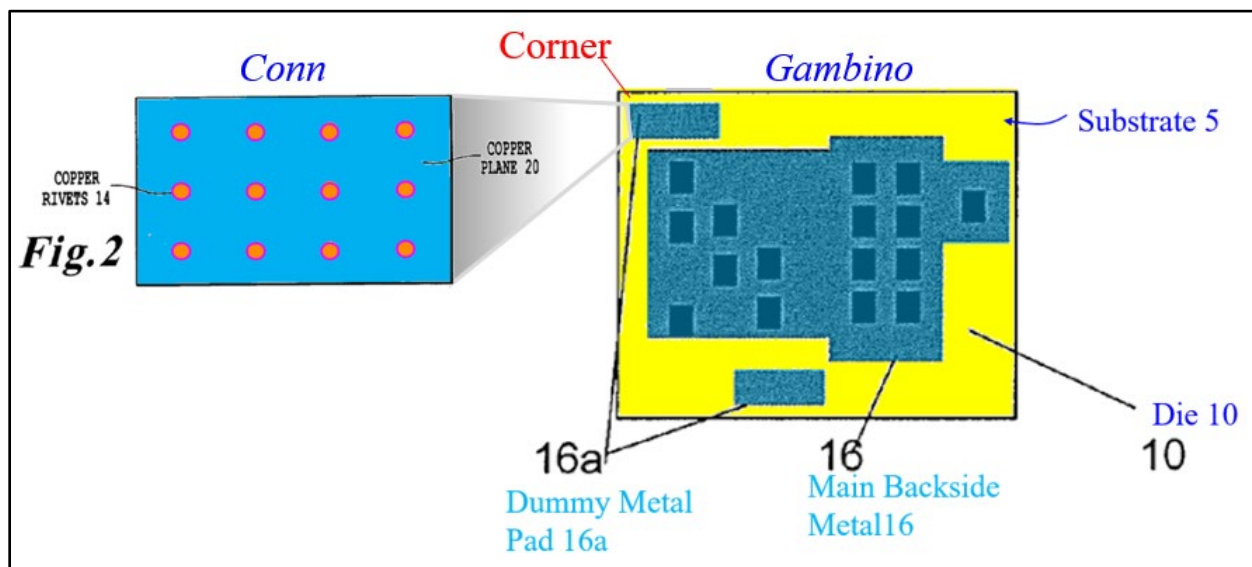
166. Aside from depending on claim 11, claim 17 is substantially similar to claim 7. *Supra*, §VII.B. Thus, claim 17 is taught by *Gambino* in view of *Conn* for the reasons discussed for claims 11 and 7. *Supra*, §§XIII.B.2 and XIII.B.3.e.

H. Ground 3B: *Gambino* in View of *Conn* and *Ding* Renders Obvious Claims 10 and 20

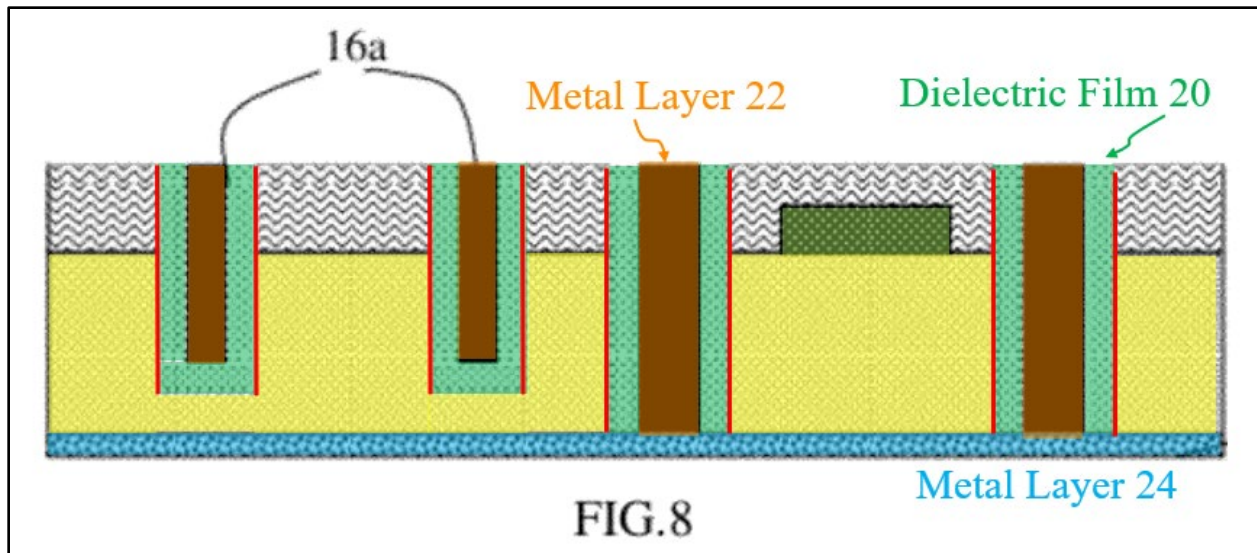
1. Rationale for combining *Gambino/Conn* with *Ding*

a. Proposed combination

167. *Gambino/Conn* discloses its packaged module can be used as “RF analog chips,” and contains “a host of different active or passive devices.” *Gambino*, [0002], [0030]. Inductors are typical passive devices used in RF analog chips. *Ding*, [0015]. *Ding* proposes using TSV-forming process to make inductors in RF chips. *Ding*, [0015]. A POSA would have been prompted by *Ding*’s teachings to modify *Gambino/Conn*’s method of forming electrical TSVs and anchor vias, to add a step of forming a dielectric film on the TSVs/anchor-vias, such that the modified method can be used to simultaneously make *Ding*’s high-quality inductor.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Ding, Fig. 8.

**b. A POSA would have been motivated to combine
Gambino/Conn with *Ding***

168. Using the same process to manufacture all the above components in an RF chip simplifies fabrication and reduces cost. Particularly, both *Gambino* and *Ding* aim to improve RF chip function/manufacturing in an inexpensive way. *Gambino*, [0016] (“the peeled metal ... can cause problems with die yield and reliability”), [0017] (“[b]y using a patterned backside metal ground plane, a less expensive dicing process can be used, thereby reducing the overall cost of the packaged module”); *Ding*, [0003] (“there remains a need for high quality factor inductor formation with an inexpensive method”), [0015] (“[t]his significantly reduces the costs”). A POSA would have been motivated to combine their teachings to maximize the benefits.

169. Moreover, *Gambino/Conn* would have led a POSA to combine it with *Ding*. *Gambino* discloses its packaged module includes “passive devices,” and can be “RF analog chips” that uses passive devices like inductors. *Gambino*, [0002], [0030]. And, *Conn* discloses its carrier substrate may be formed with “[p]assive components (as capacitors, resistors, and inductors),” suggesting its electronic package is suitable for RF applications. *Conn*, [0026]. Thus, *Gambino/Conn* would have prompted a POSA to adopt *Ding*’s teaching about making high-quality inductors.

170. Further, *Gambino/Conn* already includes electrical TSVs and anchor vias, so a POSA would have been attracted by *Ding*’s proposal of using the TSV/anchor-via processing to manufacture the high-quality inductors. *Ding*, [0015]. This means that the manufacturing process can be greatly simplified for RF chips. Additionally, a POSA would have appreciated that using *Ding*’s dielectric film would reduce signal interference between the electrical TSVs (providing power and input/output for active devices) and the inductors (passive devices), so making the combination would result in better RF chips. *E.g.*, *Volant* (Ex. 1030), [0007] (“In a conventional TSV, isolation from the signal to the substrate and/or adjacent structures is generally determined by the thickness and properties of the sidewall passivation. In the prior art, it is normally a thin oxide, preferably 1 μm or less.”).

c. The combination of *Gambino/Conn* with *Ding* would have yielded a predictable result

171. *Gambino/Conn*'s and *Ding*'s via-forming methods use the same steps: forming vias at the front side; depositing metal filler in the vias; and forming backside metal. Compare *Gambino*, [0020]-[0021], with *Ding*, [0019]-[0025], Figs. 3-8. Thus, the proposed combination does not require any change to *Gambino/Conn*'s existing way of forming the TSVs/anchor-vias and backside metal. Rather, it only requires adding an additional step of depositing the dielectric film, before the metal filler is deposited into the vias. This is a simple modification, and a POSA would have had a reasonable expectation of success in it.

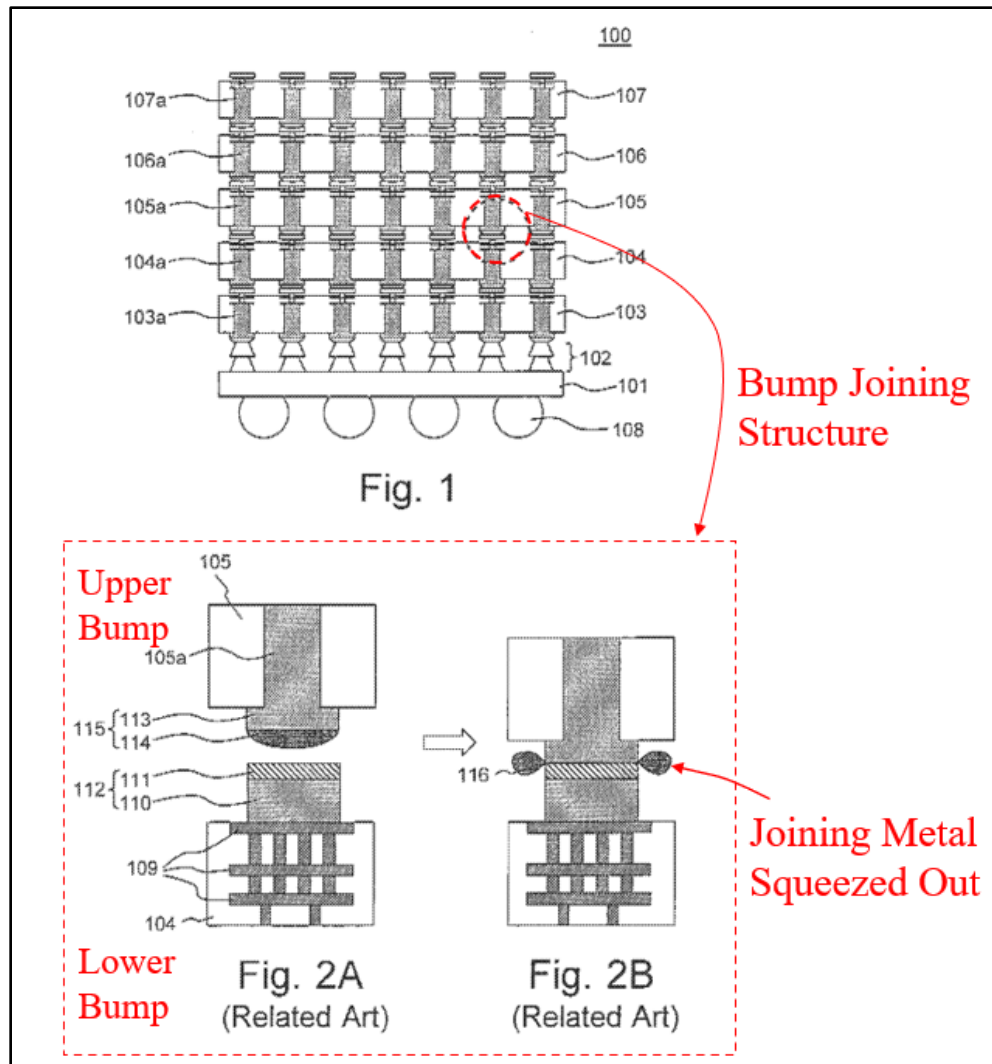
172. The modification to *Gambino/Conn*'s via-forming method would yield a predictable result—a dielectric film would be formed on the sidewall of the electrical TSVs and anchor vias. As discussed in §XIII.H.1.b, such dielectric film would reduce signal interference and yield better-functioning RF chips.

2. Claims 10 and 20: “an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via”

173. The *Gambino/Conn/Ding* combination discloses this limitation because *Gambino/Conn*'s via-forming method, as modified by *Ding*, would result in a dielectric film formed in the electrical TSVs and anchor vias. *Supra*, §XIII.H.1.a; *Ding*, [0021]-[0023], Fig. 4 and 8.

XIV. GROUND 4: *TORII* ANTICIPATES CLAIMS 1, 8-11, AND 18-20**A. Overview of *Torii***

174. *Torii* discloses structures and methods for joining multiple semiconductor chips along a vertical direction. *Torii*, Abstract, [0004], [0008]. Figure 1 shows an exemplary semiconductor device 100 (e.g., a memory) including a stack of semiconductor chips 103, 104, 105, ... *Torii*, [0006]. The chips are connected by a bump joining structure at their interfaces. *Torii*, [0007]. As shown in Figures 2A and 2B, *Torii* recognizes a problem that, when the upper and lower bumps are joined, the joining metal may be squeezed out, causing bad physical and electrical connections. *Torii*, [0007].

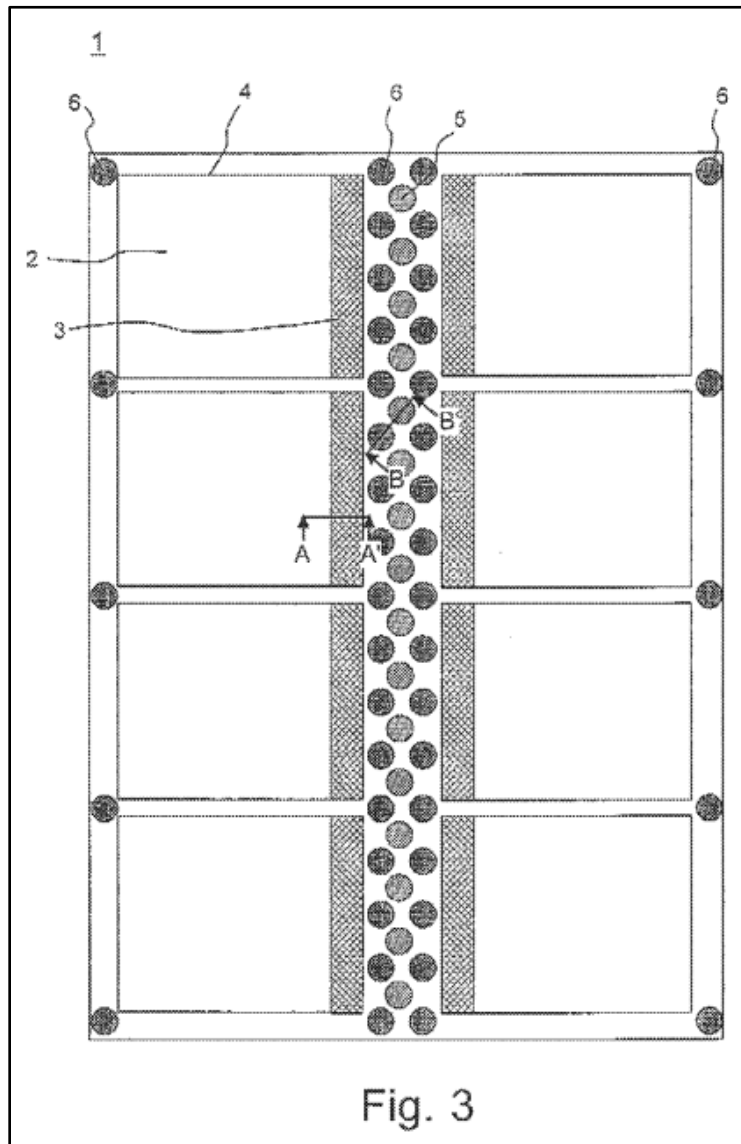


Torii, Figs. 1, 2A, 2B.

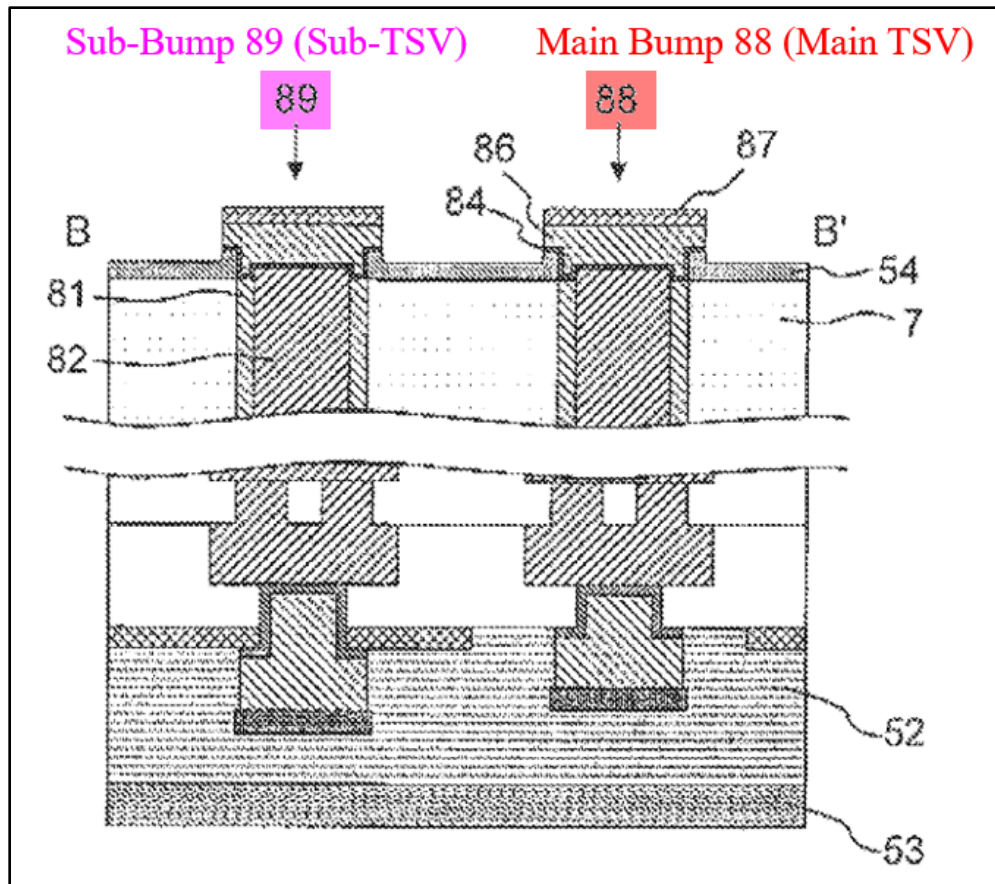
175. To solve the problem, *Torii* proposes adding sub-bumps (a.k.a., sub-TSVs) along with the usual bump structure (main bumps). *Torii*, [0008]. “[S]ub-bumps [are] greater in height than main bumps.” *Torii*, [0027]. Thus, “the sub-bumps come into contact with one another earlier than the main bumps at the time of joining semiconductor chips, thereby securing margins of joint between the main bumps.” *Torii*, [0027]; *see also* *Torii*, [0047]. Figure 3 is a plan view

showing the placement of main bumps 5 and main bumps 6. *Torii*, [0031], [0045].

And Figure 46 is a cross-sectional view of the main bumps and sub-bumps. *Torii*, [0040], [0100].



Torii, Fig. 3.



Torii, Fig. 46.

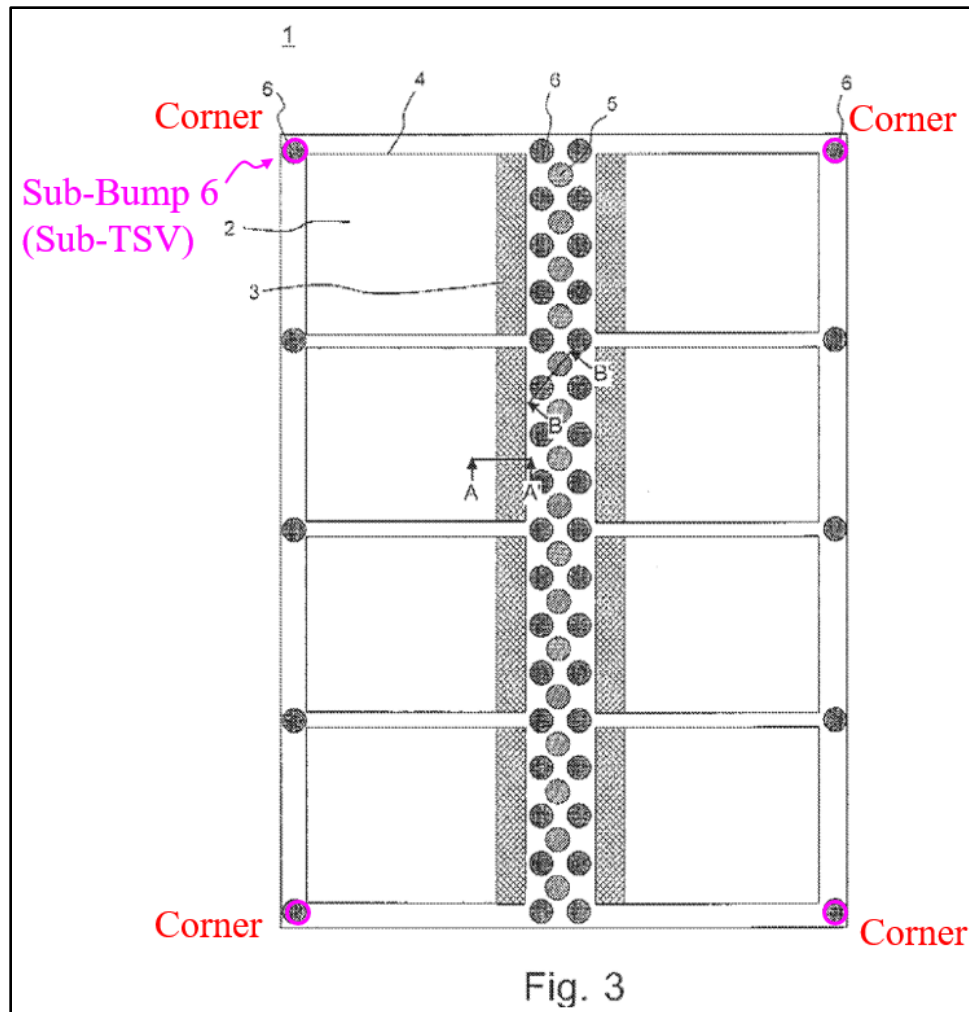
B. Independent Claim 1

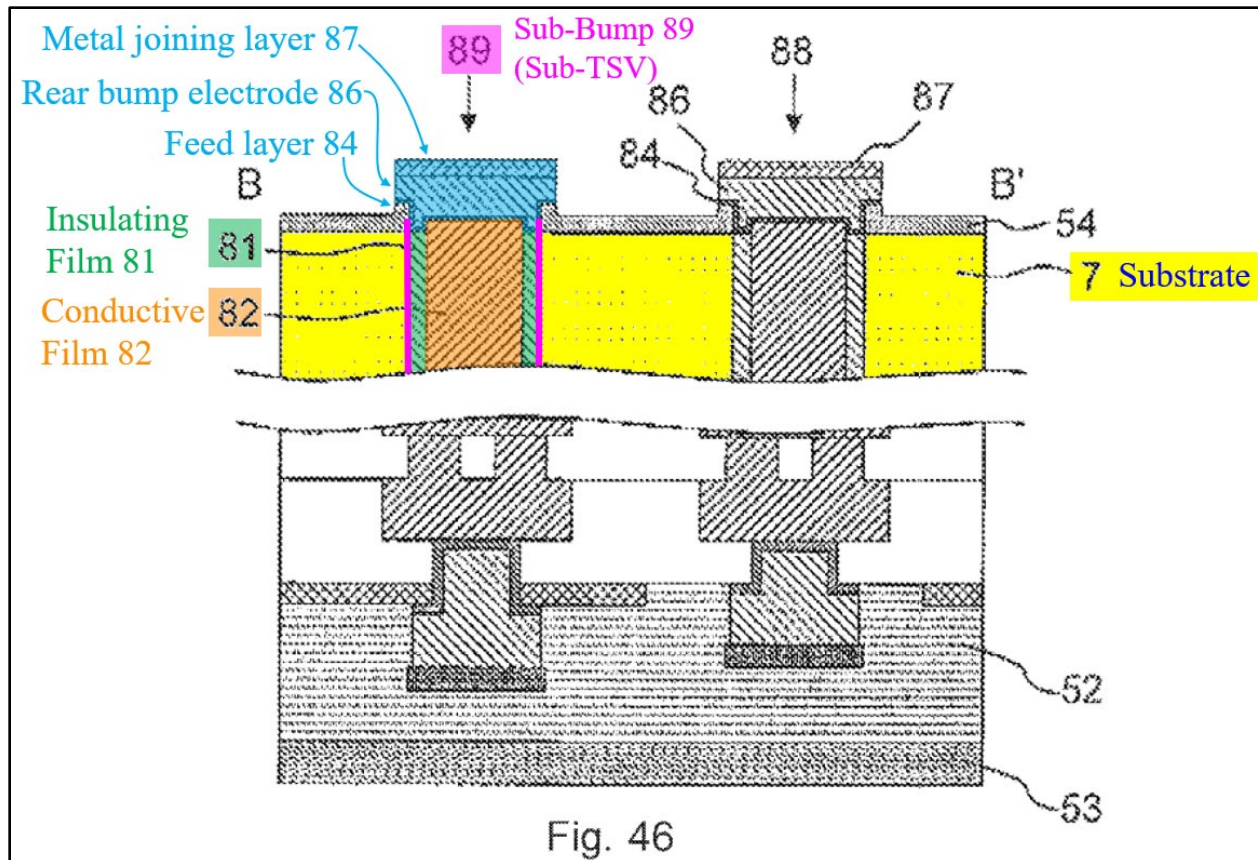
1. [1pre] A structure comprising:

176. I was informed by counsel that the preamble of a claim is not necessarily limiting. Nonetheless, to the extent the preamble is limiting, in my opinion *Torii* discloses it by disclosing a semiconductor chip. *Torii*, [0002], [0031], [0045], [0040], Fig. 3, Fig. 46.

2. [1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;

177. Figure 3 of *Torii* provides a plan view showing “[s]ub-bumps 6 are [] arranged in the outer circumference of semiconductor chip 1,” including corners of the chip. *Torii*, [0045]. *Torii* discloses “a sub-bump is formed as part of a sub-TSV” and uses these two terms interchangeably, so the sub-bumps 6’ positions in Figure 3 represent the sub-TSVs’ positions. *Torii*, [0090]; *see also Torii*, [0048] (“a TSV provided with sub-bumps is referred to as a sub-TSV”). *Torii* discloses the sub-TSVs are used for joining adjacent semiconductor chips, so they serve as anchor points. *Torii*, [0083], [0090]; ’826 patent, 3:12-17 (“metal filler within anchor vias 132 and 133 ... provides physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150”). *Torii* further discloses that elements of the chip are formed on a semiconductor substrate. *Torii*, [0043]. Figure 46 shows a cross-sectional view in which a sub-bump 89 (TSV) is disposed in a substrate 7. *Torii*, [0094], [0100]-[0101]. Therefore, in my opinion, *Torii* satisfies claim [1a].

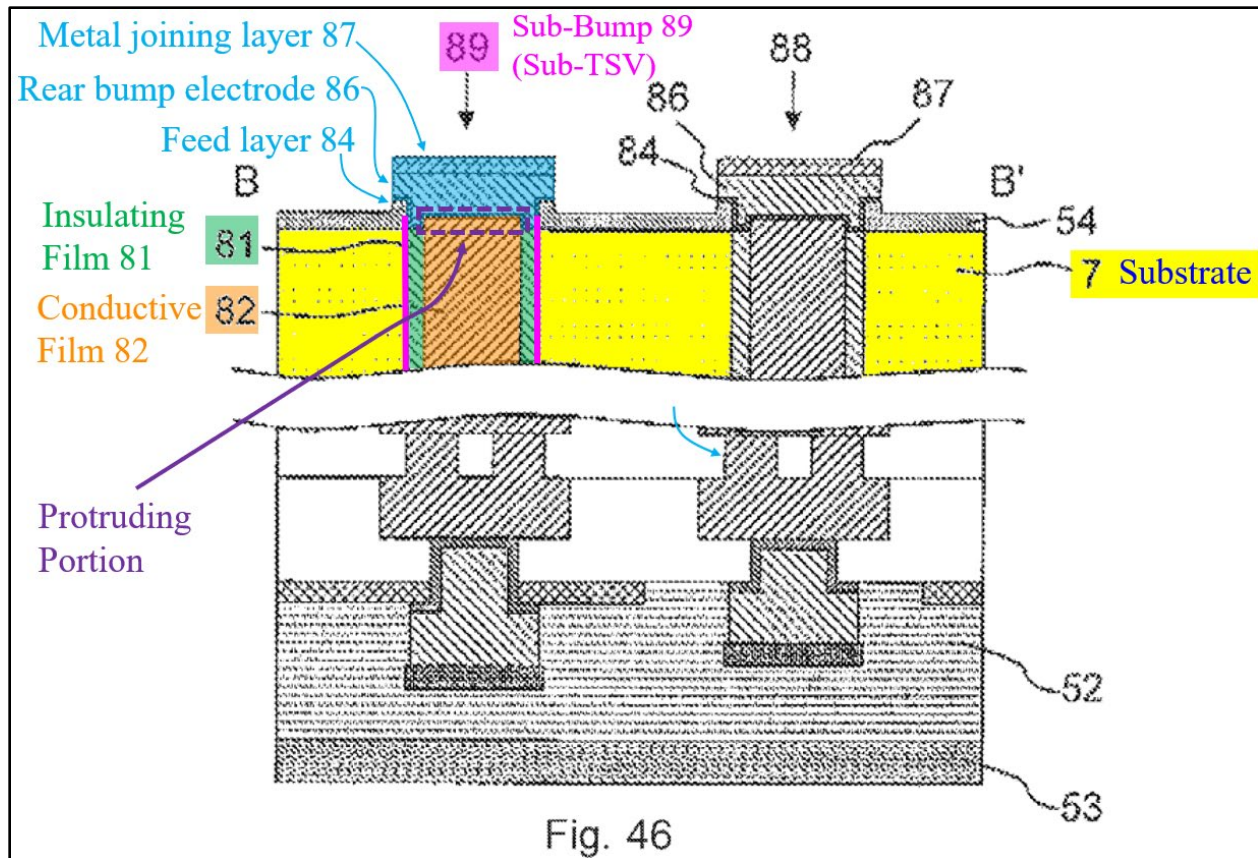
*Torii*, Fig. 3.



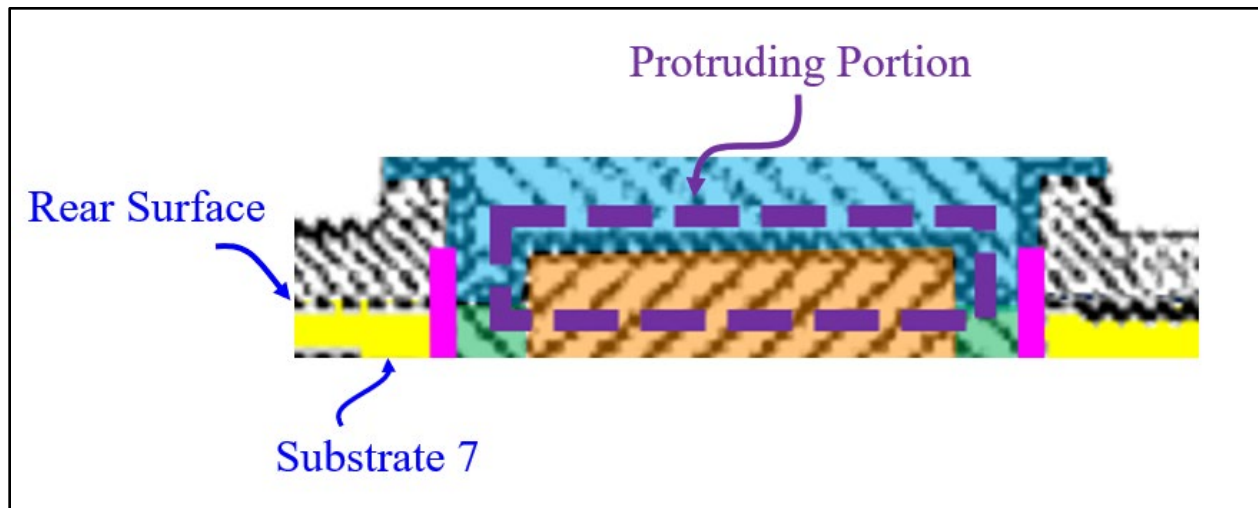
Torii, Fig. 46.

3. [1b] a **metal filler** within said at least one **anchor via**, said **metal filler** having a **protruding portion** extending from a backside of said semiconductor substrate;

178. Torii's Figure 46 shows a **conductive film 82**, e.g., a **copper film**, is within the **sub-bump 89 (TSV)**. Torii, [0096]-[0097], [0099]-[0100]. Torii discloses "the bottom of **conductive film 82** slightly **protrudes** from the rear surface of the substrate." Torii, [0099], Figs. 39, 46. Torii therefore satisfies claim [1b].

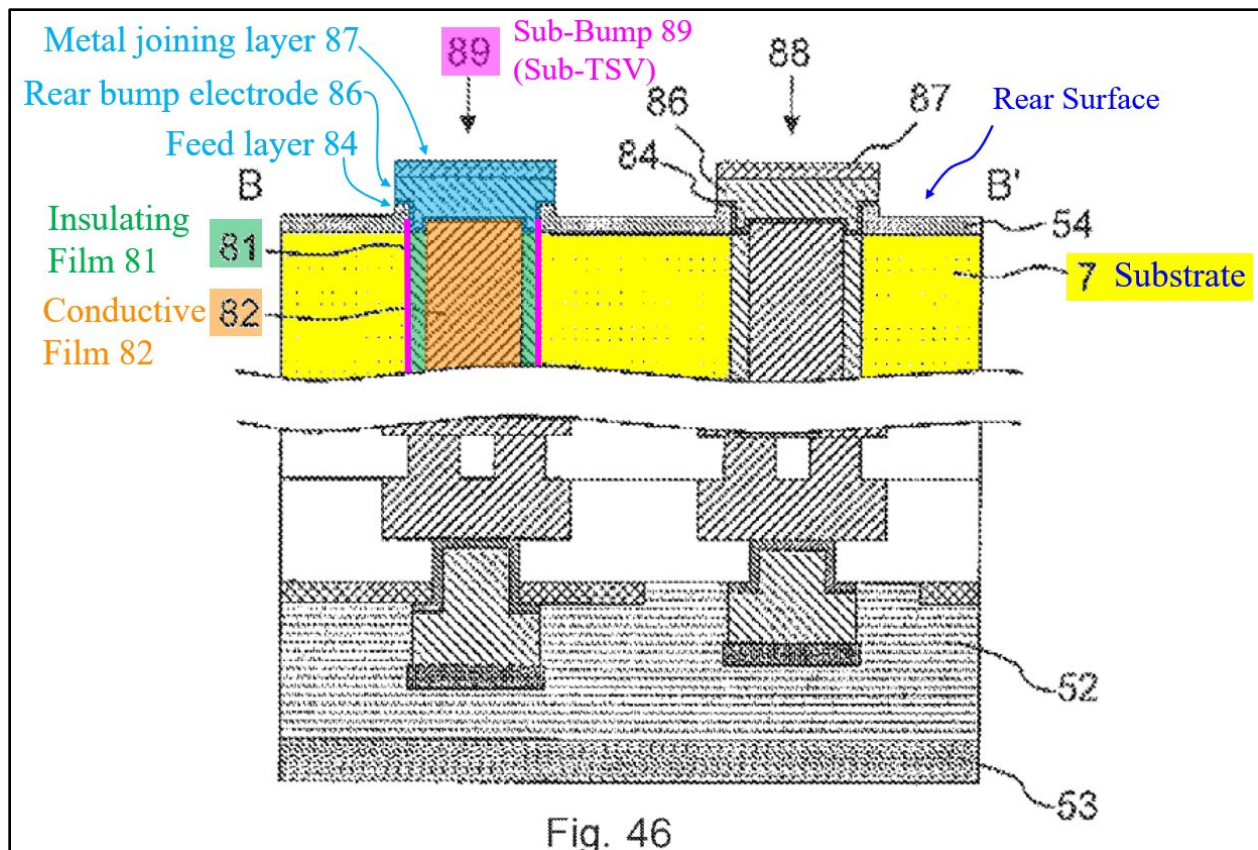


Torii, Fig. 46.

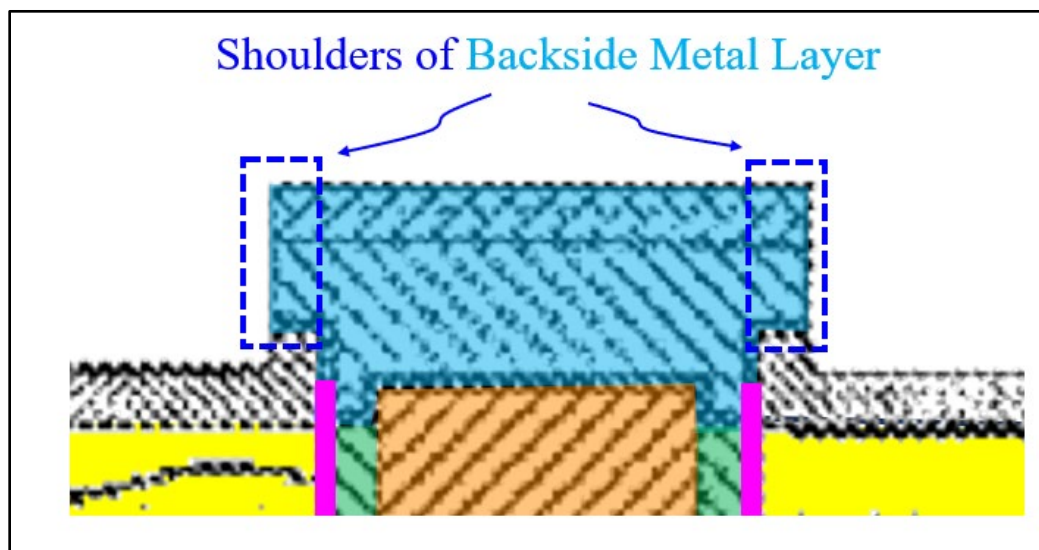


4. [1c] a **backside metal layer** on a bottom surface of said semiconductor substrate, said **backside metal layer** being bonded to said **protruding portion** of said **metal filler** of said at least one **anchor via**;

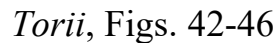
179. *Torii*'s Figure 46 discloses a “[s]econd feed layer 84 is formed on the rear surface” of the substrate and the **protruding position** of the **conductive film 82**. *Torii*, [0100], Figs. 40-46. Notably, Figure 46 shows that the **feed layer 84** forms a shoulder region on the substrate surface. *Torii*, Fig. 46. This is a result of the fabrication process described in Figures 40-46. Specifically, as illustrated below by the fabrication flow in Figures 42-46, the **shoulder** region results from a portion of the rear-surface protective film 54 formed on the sidewall of the insulating film 81. *Torii*, [0100]. Thus, the **shoulder** region is not on the **sub-TSV**, but rather it is on the substrate surface.



Torii, Fig. 46.



Torii, Fig. 46 (excerpted, zoomed).



Samsung Exhibit 1003, Page 147 of 188

the **second feed layer 84** and the **conductive film 82**. See, e.g., *Farooq* (Ex. 1029), 5:34-42 (“Solder layer 54 may be dispensed by plating (most preferred), evaporating, sputtering or even in paste form. Use of the solder layer 54 has the advantage of achieving the bonding at a lower temperature such as 183-300° C. (depending on whether eutectic tin/lead, other tin/lead or lead-free alloys are used), whereas copper or gold solid state bonds are typically at temperatures greater than 350° C., and even approaching 400° C. In addition, no pressure is required in solder bonding.”). Moreover, “**rear bump electrode 86** and **second metal joining layer 87** are formed by electrolytic plating” and are disposed on the **second feed layer 84**. *Torii*, [0100], Figs. 45-46. Here, the **second feed layer 84** alone constitutes the claimed “**backside metal layer**.” Alternatively, the **second feed layer 84**, **rear bump electrode 86**, and **second metal joining layer 87** collectively constitute the claimed “**backside metal layer**.”

5. [1d] wherein said **metal filler** within said at least one **anchor via** does not provide ground connection to one or more active devices in said semiconductor substrate.

181. *Torii* discloses this limitation by disclosing “[t]he sub-TSV is a dummy [] is normally not used as a current pathway.” *Torii*, [0048]. Although *Torii* discloses the sub-TSV “can be used as a subsidiary current pathway,” *Torii*, [0048], a POSA would understand this is just an optional embodiment of *Torii*. As *Torii* expressly discloses “[t]he sub-TSV is a dummy which is **normally not** used

as a current pathway,” a POSA would understand that the sub-TSV is normally not used for electric connection, let alone ground connection. *Torii*, [0048] (emphasis added).

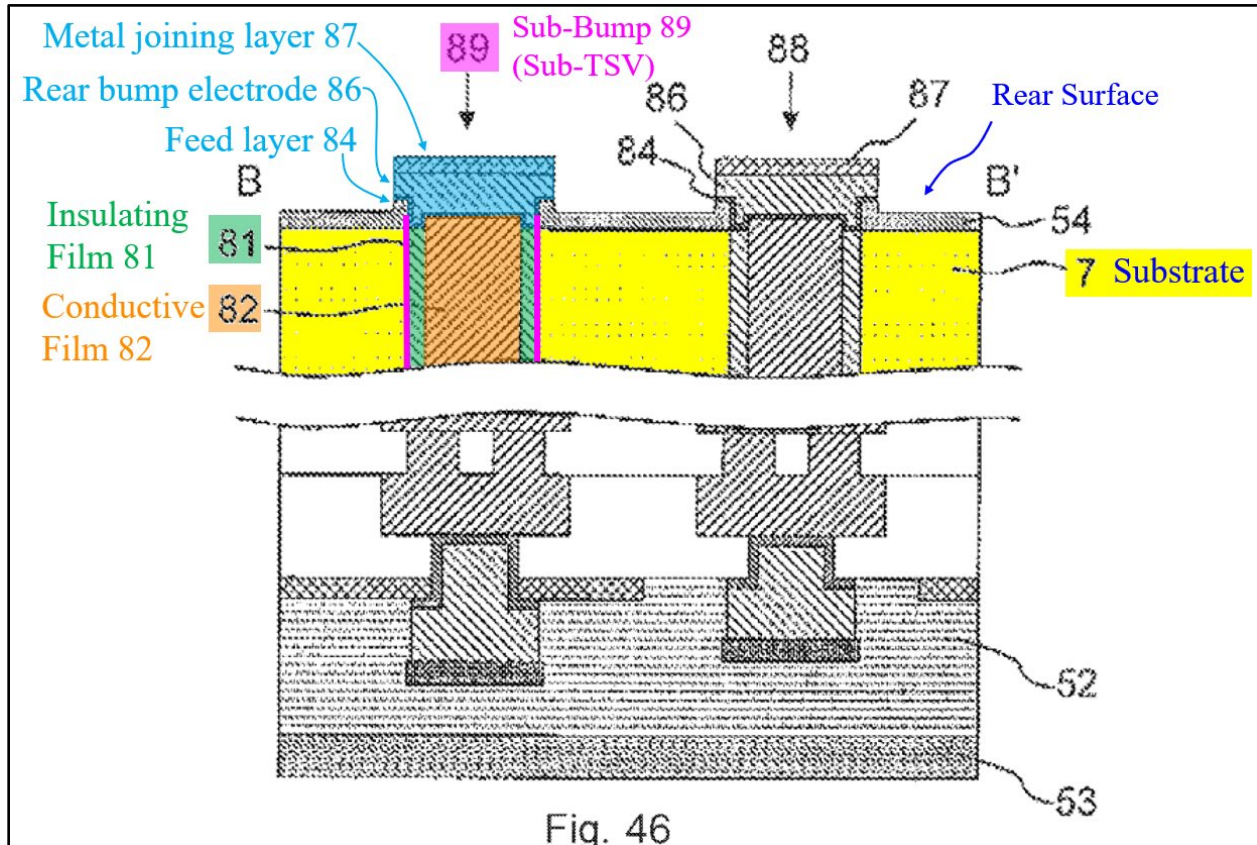
C. Claim 8

The structure of claim 1, wherein said backside metal layer comprises at least one of an interface layer, a conduction layer, and a packaging layer.

182. As discussed in §XIV.B.4, the second feed layer 84, rear bump electrode 86, and second metal joining layer 87 collectively constitute the claimed “backside metal layer,” and respectively correspond to the claimed “interface layer,” “conduction layer,” and “packaging layer.” Specifically, *Torii*’s second feed layer 84 is understood in the art to facilitate the bonding the rest of the backside metal and to increase the adhesion thereof, and therefore plays the role of the claimed “interface layer.” *Torii*’s rear bump electrode 86 is used for conducting electrical current,⁹ and therefore is the claimed “conduction layer.” And *Torii*’s

⁹ Although *Torii* discloses the sub-TSVs are “normally not used as a current pathway,” Figure 46 shows that the rear bump electrode 86 is also used in second main bumps 88 “used mainly as a current pathway.” *Torii*, [0048]. Therefore, the rear bump electrode 86 need to have good conductivity.

second metal joining layer 87 is used for joining adjacent semiconductor chips, and therefore plays the role of “**packaging layer**.”



Torii, Fig. 46.

D. Claim 9

The structure of claim 1, wherein said **metal filler** within said at least one **anchor via** is bonded to a **metal layer** overlying said semiconductor substrate.

183. As discussed in §XIV.B.4, the semiconductor device in Figure 46 is placed upside down to show a backside-grinding process. Correspondingly, the semiconductor device in Figure 36B is flipped from Figure 46 and shows a front side process to create the TSVs. *Torii*, [0093], [0098]. Thus, in Figure 36B, the

semiconductor device is in its normal orientation with the front surface facing up.

Figure 36B shows that the **conductive film 82** in the **sub-bump 89 (TSV)** is bounded to a **third interconnect pad 32a** overlaying the semiconductor substrate.

Torii, [0054]. The **third interconnect pad 32a** is “composed of a conductive material such as metal.” *Torii*, [0055]. Therefore, in my opinion, *Torii* meets claim 9.

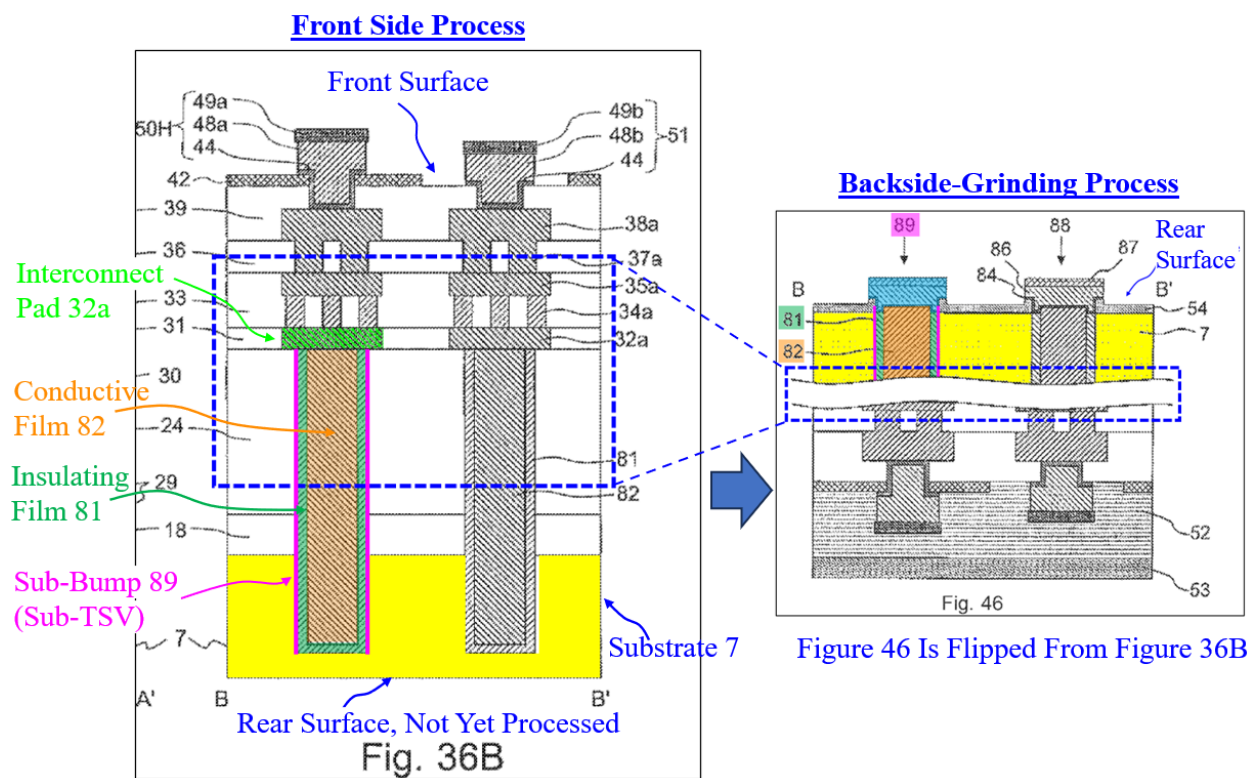


Figure 46 Is Flipped From Figure 36B

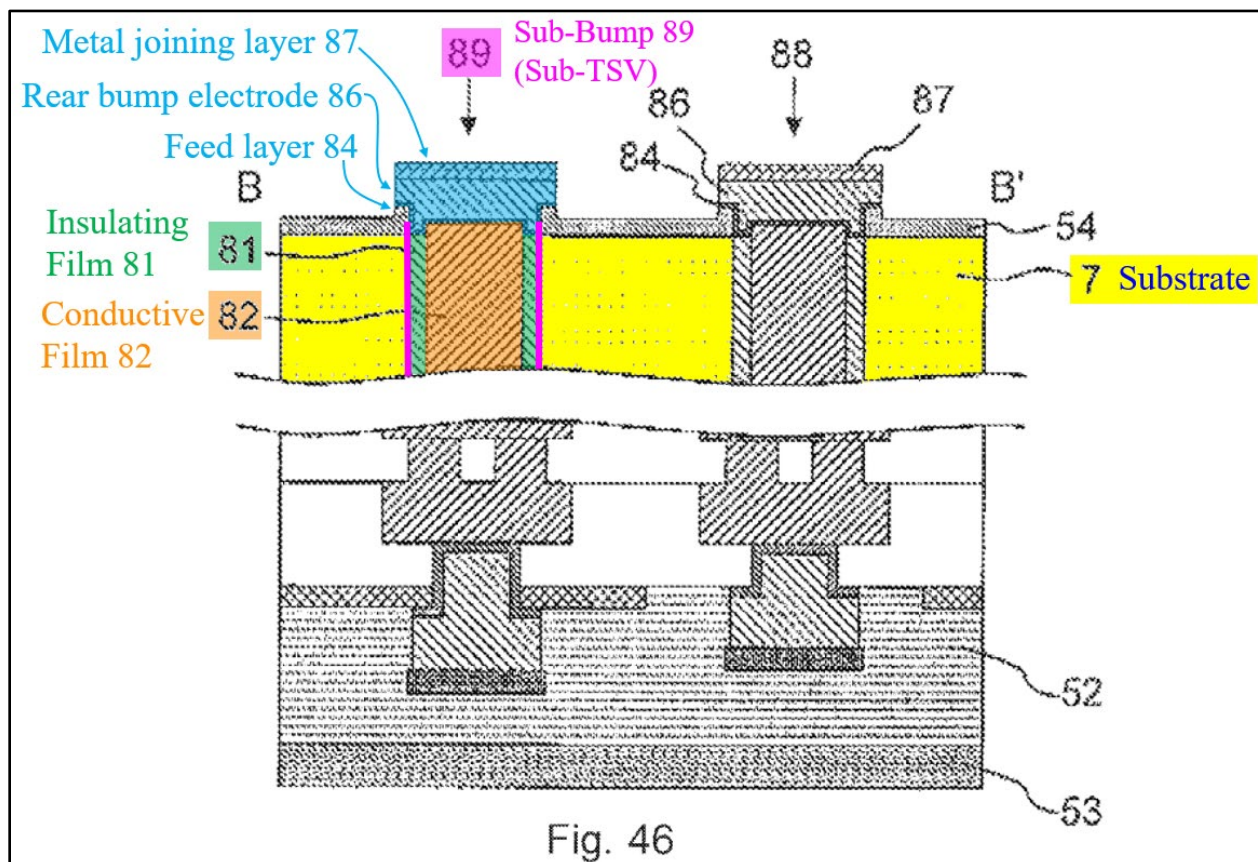
Torii, Figs. 36B, 46.¹⁰

¹⁰ The front side process (Figure 36B) occurs before the backside-grinding process (Figure 46), so the rear surface in Figure 36B is not yet processed.

E. Claim 10

The structure of claim 1, further comprising an **insulating layer** disposed between said semiconductor substrate and said **metal filler** in said at least one **anchor via**.

184. *Torii*'s Figure 46 discloses claim 10 by disclosing an **insulating film 81** is formed on the sidewall of the **sub-bump 89 (TSV)**, and between the **conductive film 82** and the substrate. *Torii*, [0095], [0097], [0099]-[0100].

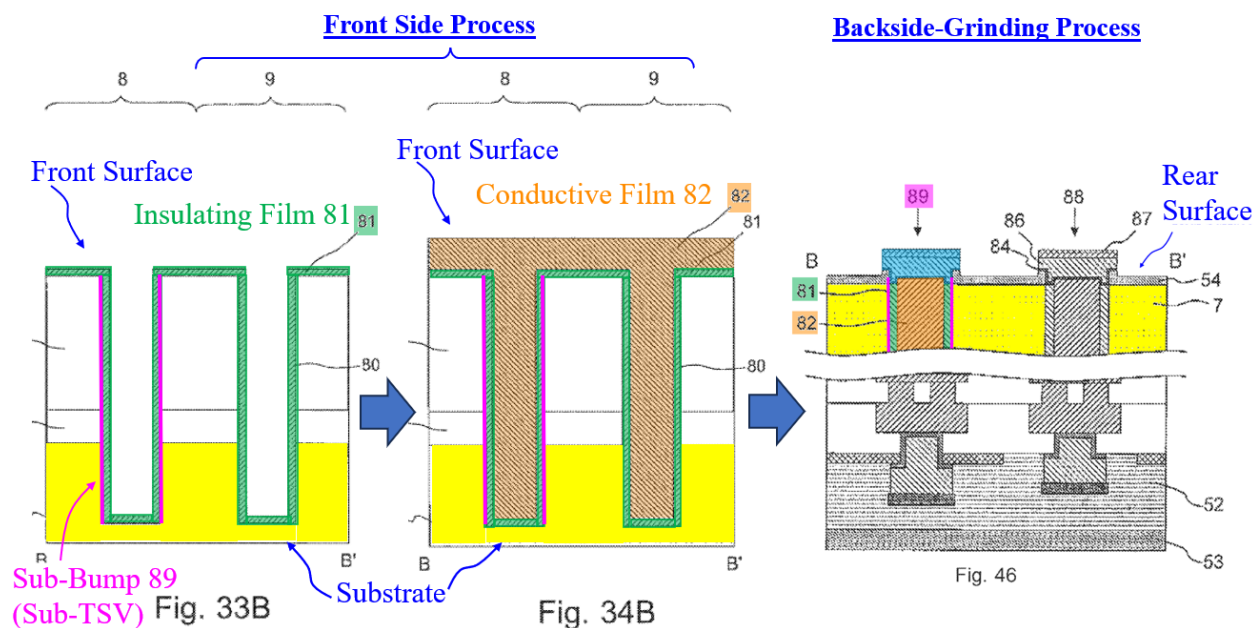


Torii, Fig. 46.

F. Independent Claim 11

1. “Forming,” depositing,” and “forming” steps

185. *Torii* discloses a method for making the semiconductor device in Figures 3 and 46. *E.g.*, *Torii*, [0093]-[0101], Figs. 32A through 36B (front side process), Figs. 37-46 (backside-grinding process). As shown below, *Torii* discloses each of the claimed [11a] “forming at least one anchor via,” [11b] “depositing a metal filler,” and [11c] “forming a backside metal layer.” *Torii*, [0093], [0095]-[0096], [0100]. Figures 33B and 34B show a front side process to form the sub-bump 89 (TSV) and deposit the conductive film 82 in the sub-bump 89 (TSV). Figure 46 shows a backside-grinding process in which the stack of second feed layer 84, rear bump electrode 86, and second metal joining layer 87 is formed on and bonded to the rear surface of the conductive film 82.



Torii, Figs. 33B, 34B, 46.

2. Remaining limitations of claim 11

186. The remaining limitations of claims 11 are substantially similar to those structural features recited in claim 1. *Supra*, §VII.B. Thus, given the similarity between claims 1 and 11, the remaining features of claim 11 are respectively disclosed by *Torii* for the same reasons discussed above for the corresponding features of claim 1 in §§XIV.B.2 through XIV.B.5.

G. Claim 18

The method of claim 11, wherein said forming said backside metal layer on a bottom surface of said semiconductor substrate comprises at least one of: forming an interface layer; forming a conduction layer; forming a packaging layer.

187. Aside from depending on claim 11, claim 18 is substantially similar to claim 8. *Supra*, §VII.B. Thus, claim 18 is anticipated by *Torii* for the reasons discussed for claims 11 and 8. *Supra*, §§XIV.F and XIV.G.

H. Claim 19

The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate.

188. Aside from depending on claim 11, claim 19 is substantially similar to claim 9. *Supra*, §VII.B. Thus, claim 19 is anticipated by *Torii* for the reasons discussed for claims 11 and 9. *Supra*, §§XIV.F and XIV.H.

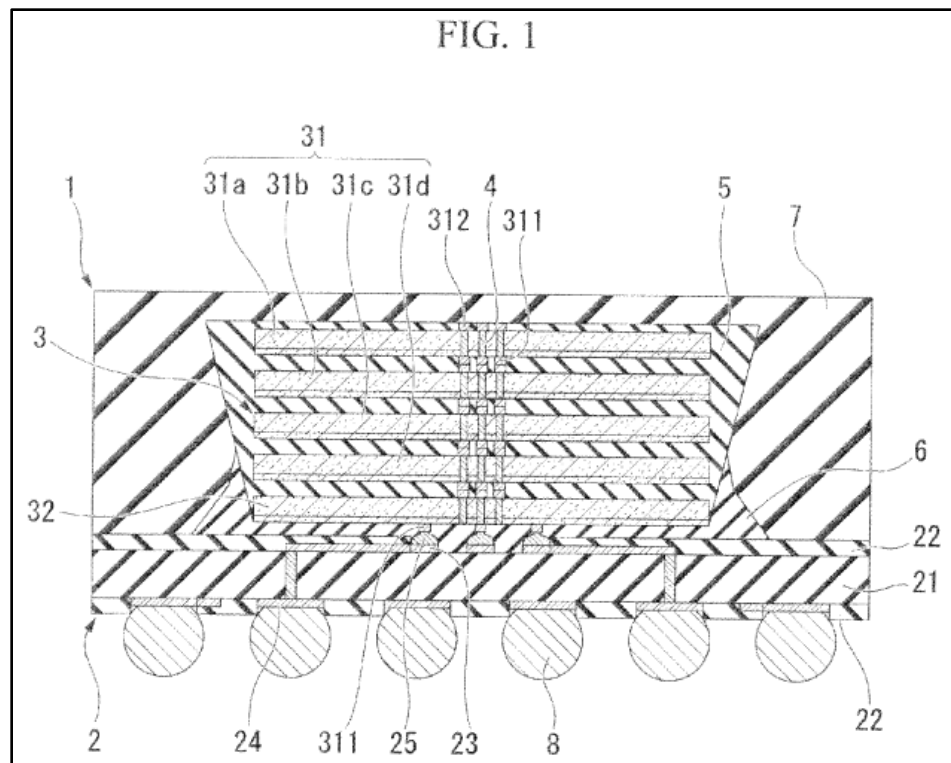
I. Claim 20

The method of claim 11, further comprising forming an **insulating layer** between said semiconductor substrate and said **metal filler** in said at least one **anchor via**.

189. Aside from depending on claim 11, claim 20 is substantially similar to claim 10. *Supra*, §VII.B. Thus, claim 20 is anticipated by *Torii* for the reasons discussed for claims 11 and 10. *Supra*, §§XIV.F and XIV.I.

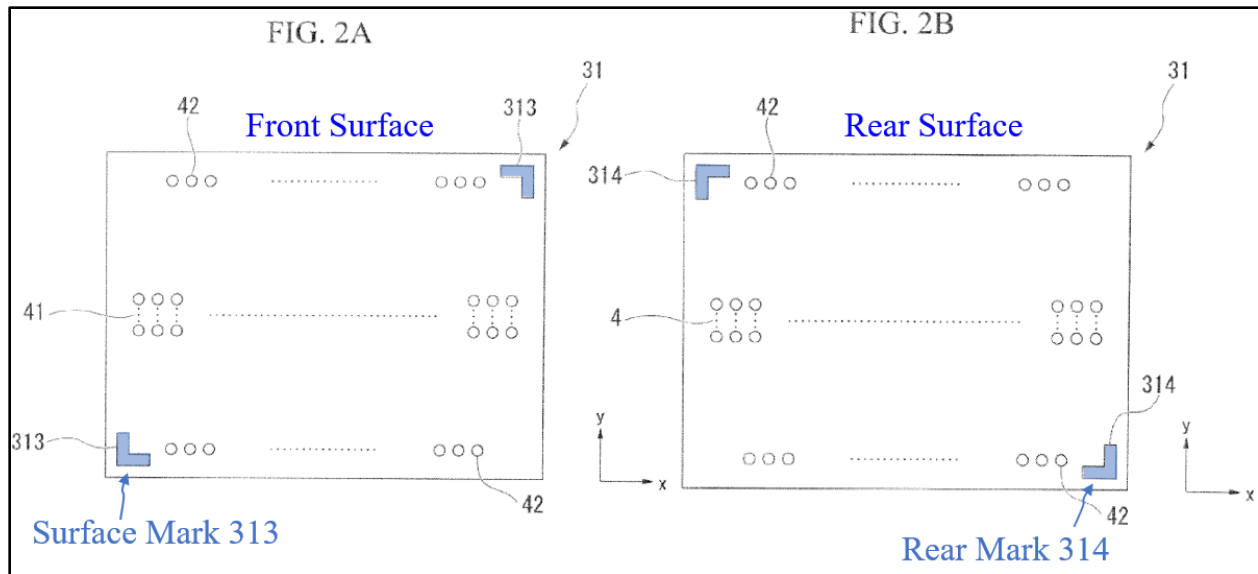
XV. GROUND 5: IDE ANTICIPATES CLAIMS 1, 2, 3, 9, 11, 12, 13, AND 19**A. Overview of *Ide***

190. *Ide* relates to alignment marks used for aligning vertically stacked semiconductor chips, e.g., memory chips 31a, 31b, 31c, and 31d in Figure 1. *Ide*, [0005]-[0006], [0010].



Ide, Fig. 1.

191. Figures 2A and 2B show a chip's front and rear surfaces, respectively. *Ide*, [0033]-[0034], [0112]. On the front surface, "surface marks 313 are arranged in a pair of corners which are located diagonally to each other." *Ide*, [0113]. And, on the rear surface, rear marks 314 are located at locations corresponding to the surface marks 313. *Ide*, [0114].



Ide, Figs. 2A-2B.

192. During chip stacking, each chip's surface and rear marks are photographed by cameras and their position information is obtained from the photos. *Ide*, [0010]. Based on the position information, the surface marks of a chip are aligned with the rear marks of a vertically adjacent chip's rear marks. *Ide*, [0010]. Recognizing that the surface marks tend to have a degraded contrast in the photos, *Ide* proposes forming dummy patterns in the vicinity of the surface marks to improve the contrast. *Ide*, [0020]-[0021], [0128], [0168]-[0169].

B. Independent Claim 1

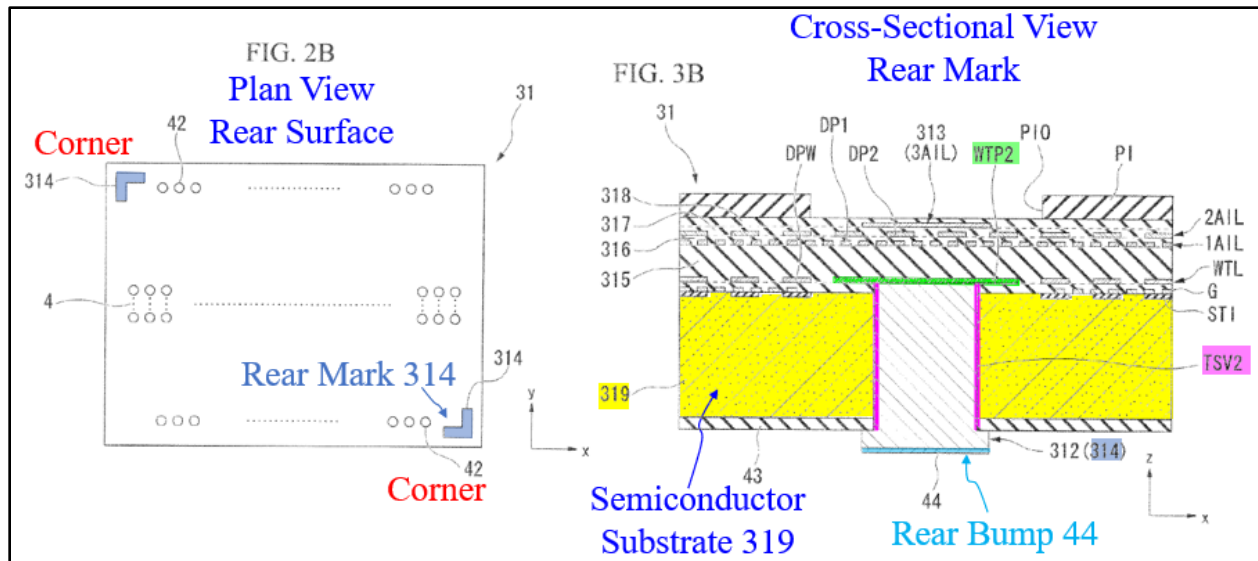
1. [1pre] A structure comprising:

193. I was informed by counsel that the preamble of a claim is not necessarily limiting. Nonetheless, to the extent the preamble is limiting, in my

opinion *Ide* discloses it by disclosing a semiconductor chip. *Ide*, [0033]-[0036], [0112]-[0127], Figs. 2A-2B, Figs. 3A-3B.

2. [1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;

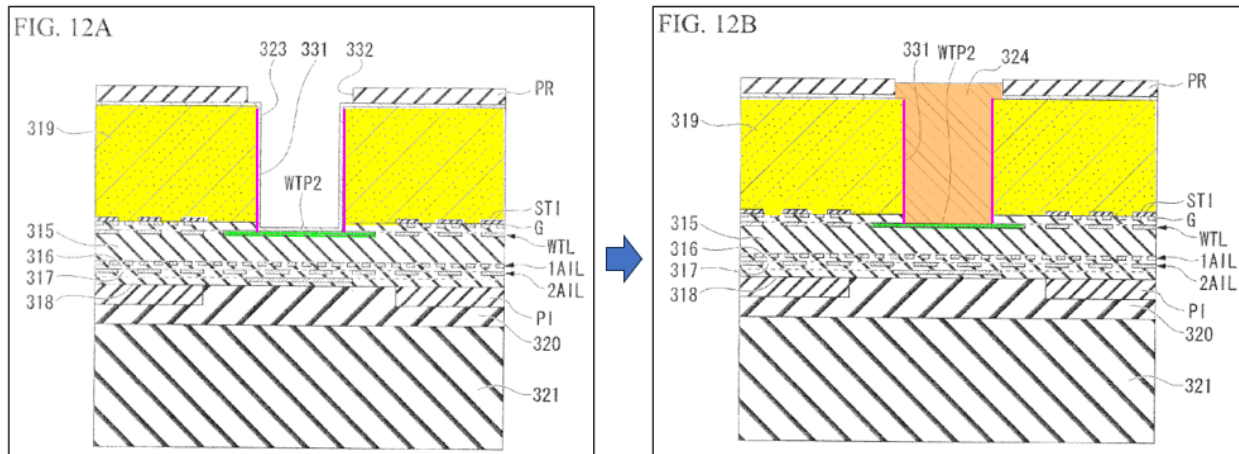
194. Figure 2B of *Ide* provides a plan view showing “rear marks 314 are arranged in a pair of corners which are located diagonally to each other.” *Ide*, [0114]. And Figure 3B provides a corresponding cross-sectional view showing each rear mark 314 is formed below a through electrode TSV2, so the TSV2s corresponding to the pair of rear marks 314 are also located at the corners of the chip in plan view. *Ide*, [0125]. Figure 3B also shows “[t]he through electrode TSV2 for a mark penetrates the semiconductor substrate 319.” *Ide*, [0130]. The TSV2 connects to a rear bump 44 on the front side of the substrate and a wiring tungsten pad WTP2 on the rear side of the substrate, thereby providing an anchor point for affixing and aligning the rear bump 44 and wiring tungsten pad WTP2. *Ide*, [0125]. Therefore, *Ide*’s TSV2 constitutes the claimed “anchor via.”



Ide, Figs. 2B, 3B.

3. [1b] a **metal filler** within said at least one **anchor via**, said **metal filler** having a **protruding portion** extending from a backside of said semiconductor substrate;

195. As shown in Figures 12A and 12B, during fabrication of the **TSV2**, “a **Cu plating 324** is grown using a seed layer 323 as an electrode to fill a via of the through electrode **TSV2** for a mark and form a pillar of the rear bump electrode 312.” *Id*, [0156].

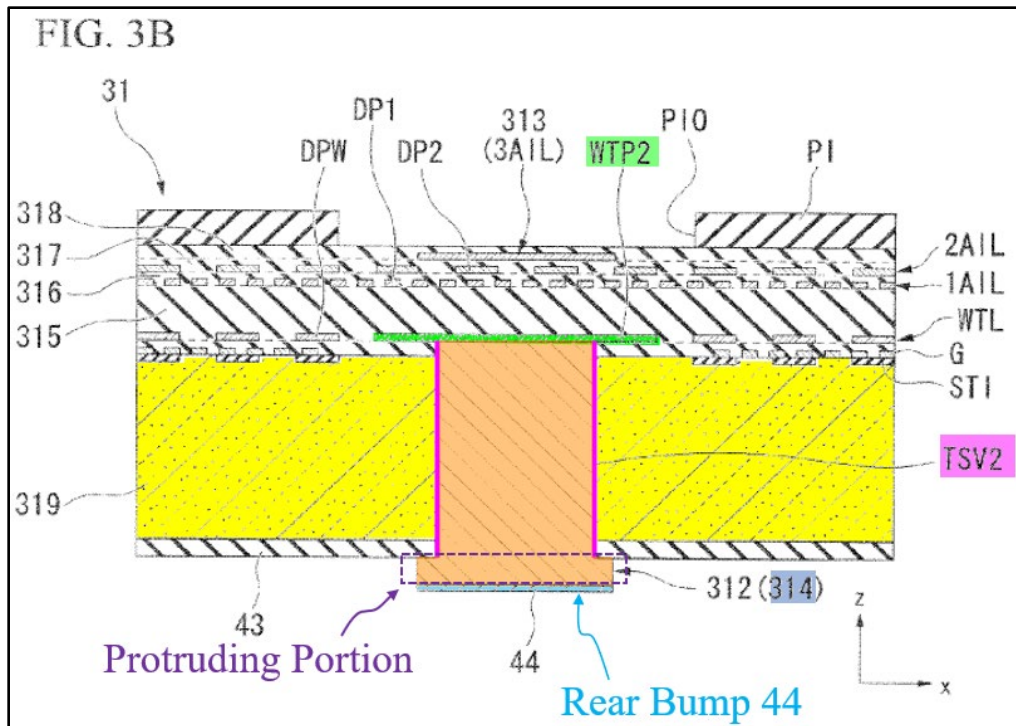


Ide, Figs. 12A-12B.¹¹

196. And, as shown in Figure 3B, in the finished device, the **Cu plating 324** filler results in a “**protruding portion**” (i.e., the pillar of the rear bump electrode 312¹²) extending from the rear surface (i.e., backside) of the semiconductor substrate 319. *Ide*, [0130], [0155]-[0157].

¹¹ During fabrication of the rear-side features, the device is placed “upside down.” *Ide*, [0150]. So, the device in Figures 12A and 12B is displayed as been inversed from the finished product in Figure 3B.

¹² The rear bump electrode 312 includes two portions: the pillar portion formed by the protruding portion of the Cu plating 324, and the electrode portion formed by the rear bump 44. *Ide*, [0156]-[0157], Figs. 12B, 13A.

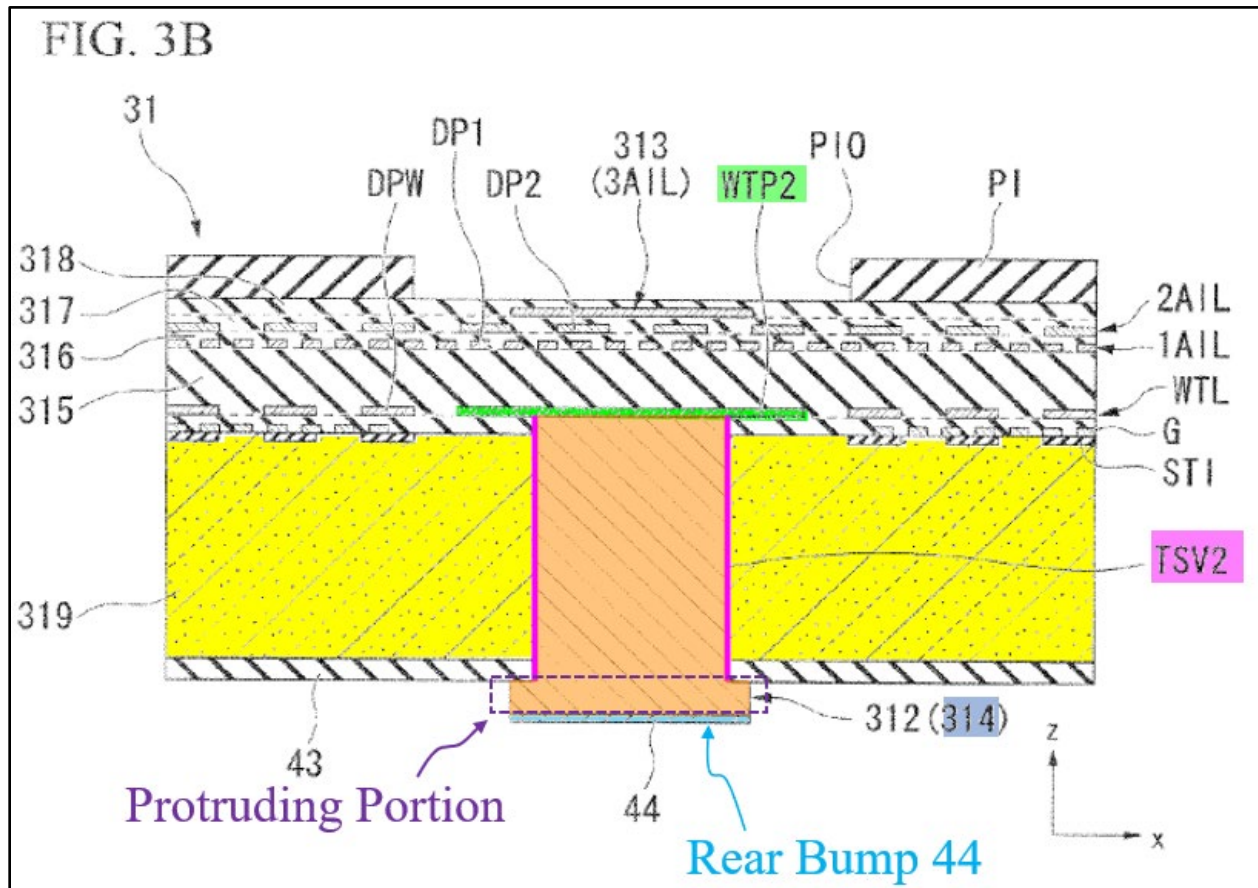


Ide, Fig. 3B.

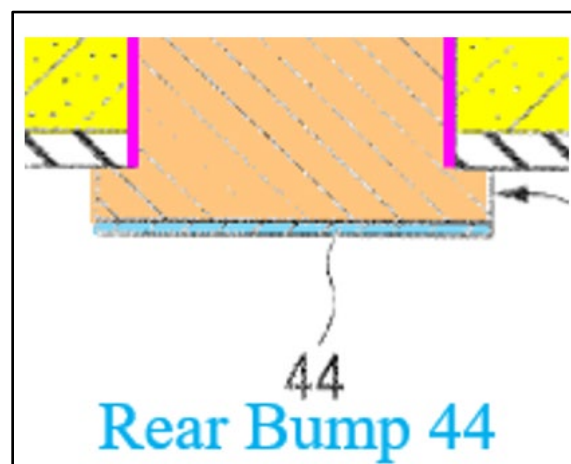
4. [1c] a **backside metal layer** on a bottom surface of said semiconductor substrate, said **backside metal layer** being bonded to said **protruding portion** of said **metal filler** of said at least one **anchor via**;

197. As shown in Figure 3B, *Ide* discloses that rear bump 44 is “formed in a surface (a rear surface) of the semiconductor substrate” and “below the through electrode TSV2.” *Id.*, [0120], [0125], Figs. 3B, 13A. Notably, Figure 3B shows that at least part of the rear bump 44 is on the rear surface. Moreover, the bottom view in Figure 4C shows that the protruding portion of the Cu plating 324, i.e., number 312 in the figure, has a larger area than the TSV2s’ opening. Since the rear bump 44 is formed on the protruding portion of the Cu plating 324, i.e., number 312, it follows that the rear bump 44 has a larger area than the TSV2s’ opening and

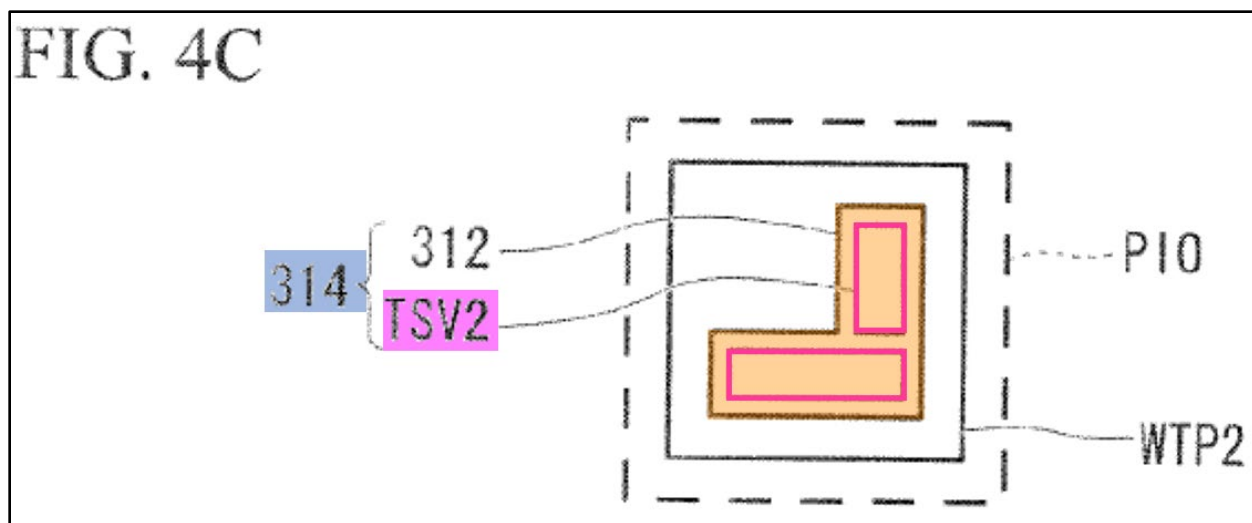
the portion of the **rear bump 44** not overlapping with the **TSV2s'** opening is on the rear surface of the semiconductor substrate 319.



Ide, Fig. 3B.

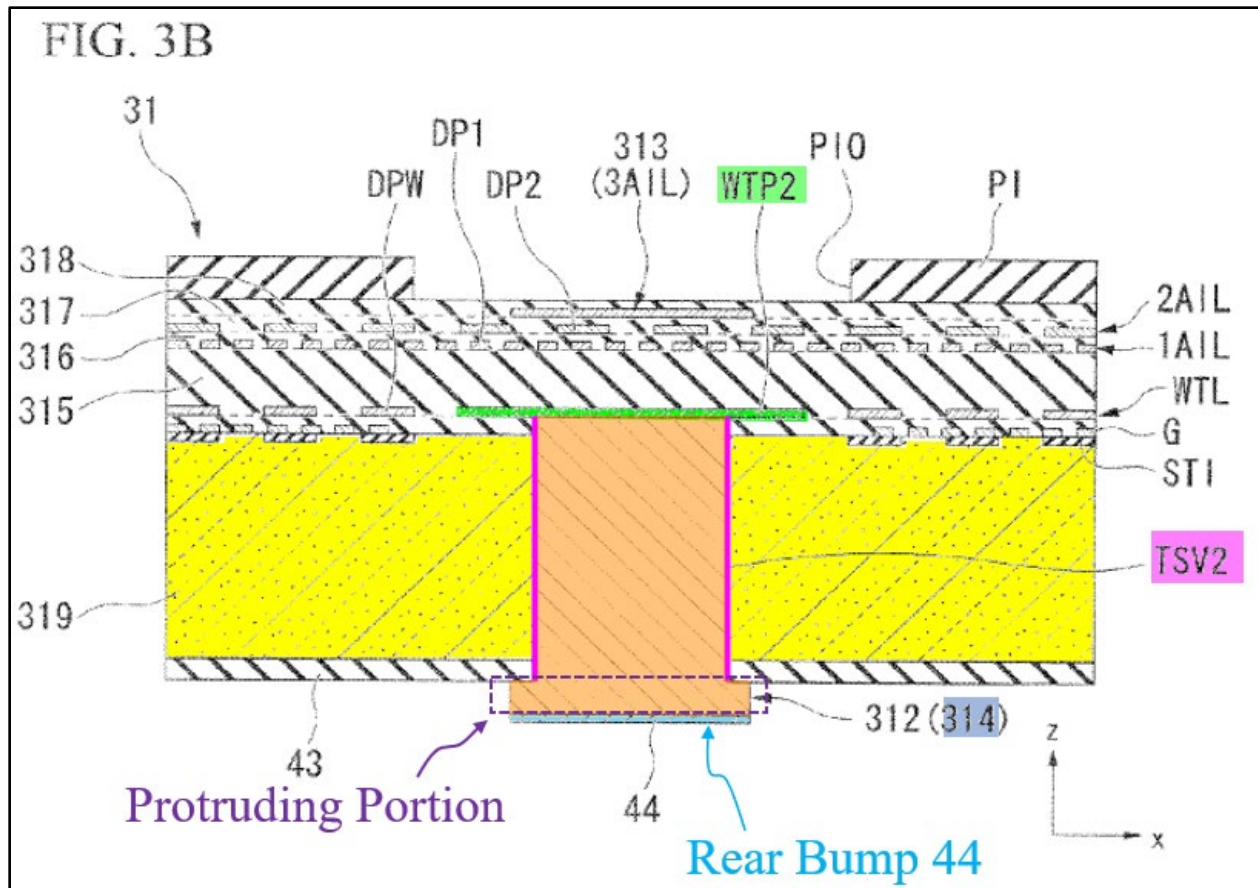


Ide, Fig. 3B (excerpted, zoomed).

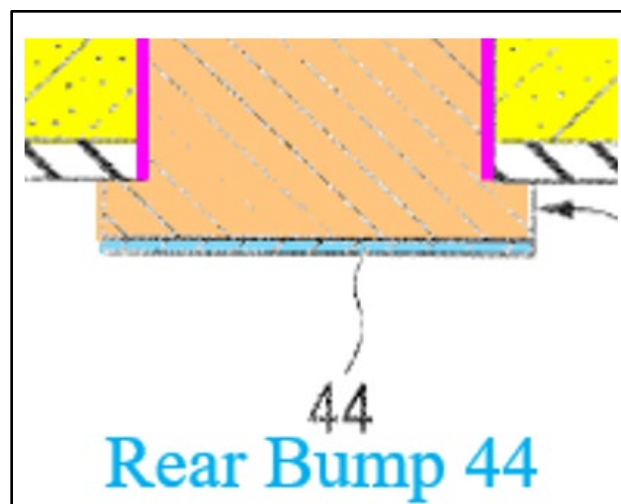


Ide, Fig. 4C.

198. *Ide* also discloses that the rear bump 44 is “bonded to” the protruding portion of the Cu plating 324. The rear bump 44 is made of “SnAg” (tin-silver alloy), i.e., a metal, and formed on the Cu plating 324 “by plating.” *Ide*, [0157], Fig. 13A. A POSA would understand that plating the tin-silver alloy on copper will cause them to form a metallic bond. *See, e.g., Farooq* (Ex. 1029), 5:34-42 (“Solder layer 54 may be dispensed by plating (most preferred), evaporating, sputtering or even in paste form. Use of the solder layer 54 has the advantage of achieving the bonding at a lower temperature such as 183-300° C. (depending on whether eutectic tin/lead, other tin/lead or lead-free alloys are used), whereas copper or gold solid state bonds are typically at temperatures greater than 350° C., and even approaching 400° C. In addition, no pressure is required in solder bonding.”). Thus, the rear bump 44 is bonded to the protruding portion of the Cu plating 324 in the TSV2.



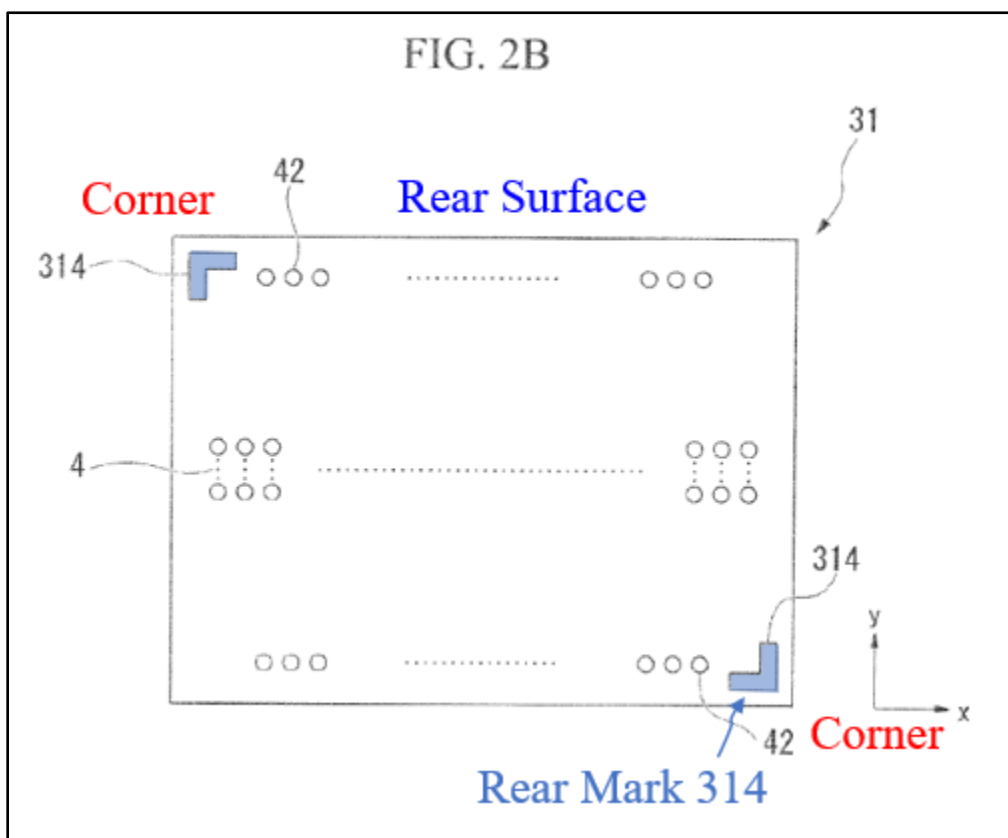
Ide, Fig. 3B.



Ide, Fig. 3B (excerpted, zoomed).

5. [1d] wherein said **metal filler** within said at least one **anchor via** does not provide ground connection to one or more active devices in said semiconductor substrate.

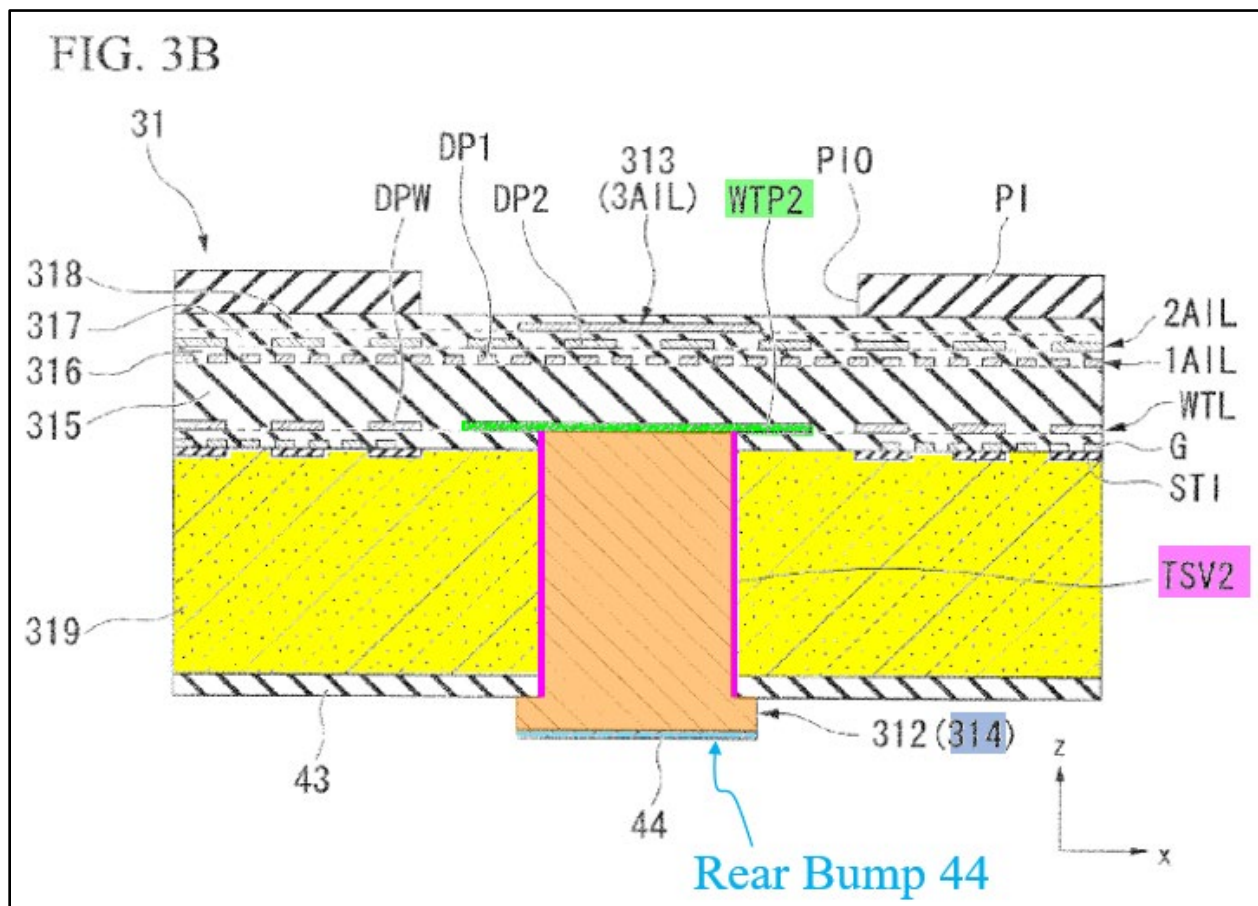
199. As shown in Fig. 3B, *Ide* meets [1d] by disclosing “the **rear marks 314** are arranged within an area in which the plurality of dummy bump through electrodes 42 are arranged.” *Ide*, [0115]. Thus, the **rear marks 314**, and the associated **TSV2s**, are located in a dummy region of the chip and not intended for electrical connections.



Ide, Fig. 2B.

200. Also, *Ide* discloses that the **Cu plating 324** in the **TSV2** is connected to the **wiring tungsten pad WTP2** on the front side of the substrate. *Ide*, [0125]. As

shown in Figure 3B, The **wiring tungsten pad WTP2** is below “a lower dummy pattern” (i.e., first aluminum wiring layer 1AIL) and “an upper dummy pattern” (i.e., second aluminum wiring layer 2AIL), both of which are not for electrical connections. *Ide*, [0126]. *Ide* further discloses that “**the functional wirings are not** arranged in the first and second aluminum wiring layers 1AIL and 2AIL of an area on the **wiring tungsten pad WTP2**.” *Ide*, [0127] (emphasis added). This means that the **wiring tungsten pad WTP2** cannot function as a path to electrically connect the **Cu plating 324** in the **TSV2** to any active devices.

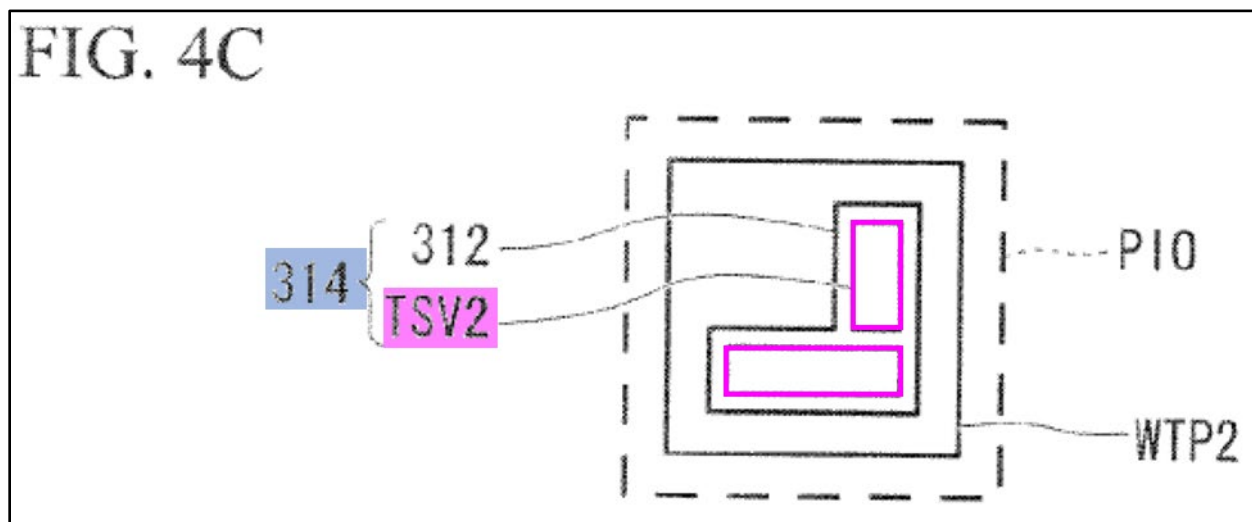


Ide, Fig. 3B.

C. Claim 2

The structure of claim 1, wherein said at least one anchor via comprises a cluster of anchor vias.

201. In my opinion, *Ide* discloses claim 2 because Figure 4C (plan view of rear surface) shows that each “rear mark 314 ha[s] an L shape” including a cluster of two perpendicularly arranged TSV2s. *Ide*, [0039], [0129]-[0130]; *see also Ide*, [0059]-[0060], [0152]-[0153], Figs. 11A-11B.



Ide, Fig. 4C.

D. Claim 3

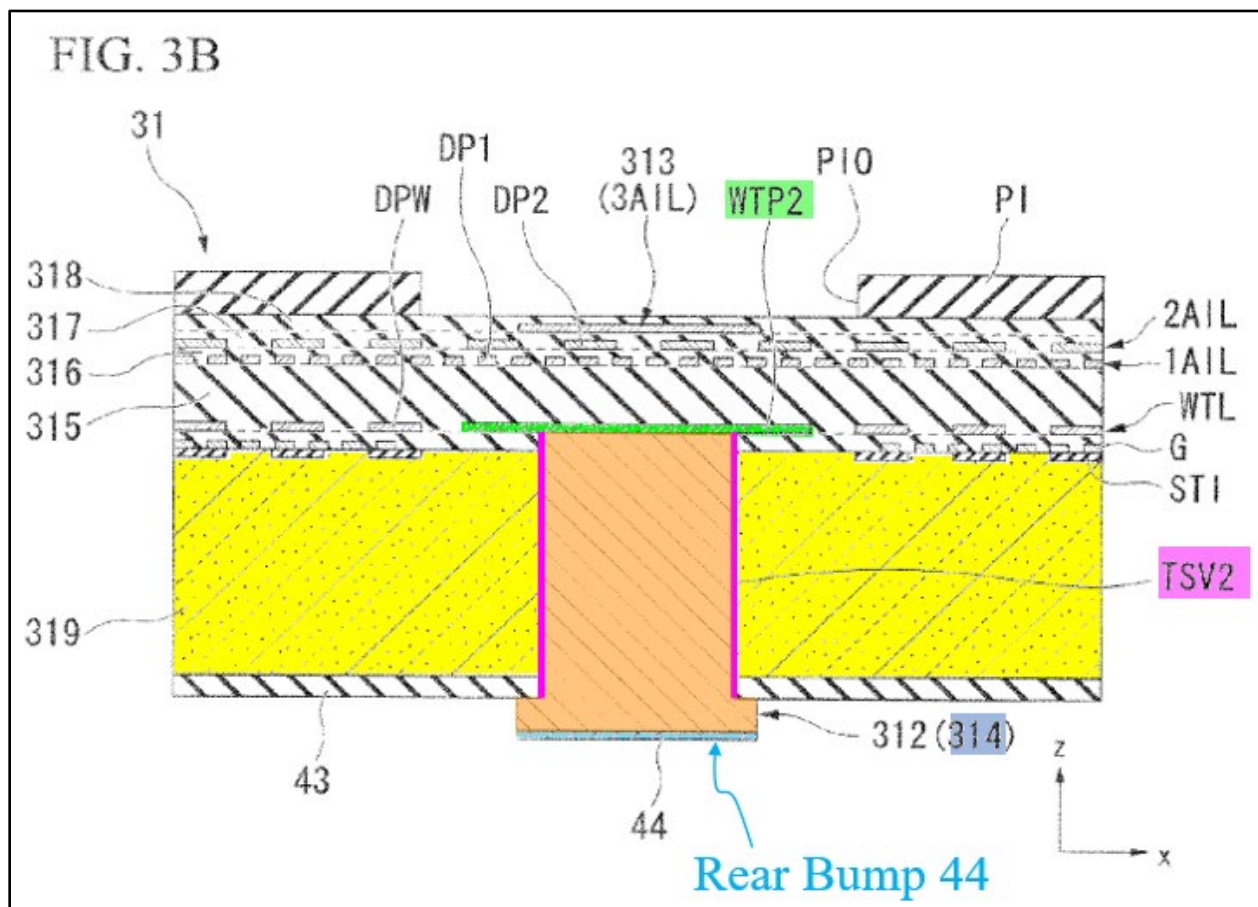
The structure of claim 2, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

202. Claim 3 depends from claim 2. In my opinion, *Ide* discloses claim 3 for the reasons discussed for claim 2. *Supra*, §XV.C. As shown in *Ide*'s Figure 4C, the two adjacent TSV2s in the rear mark 314 are oriented perpendicular to each other.

E. Claim 9

The structure of claim 1, wherein said **metal filler** within said at least one **anchor via** is bonded to a **metal layer** overlying said semiconductor substrate.

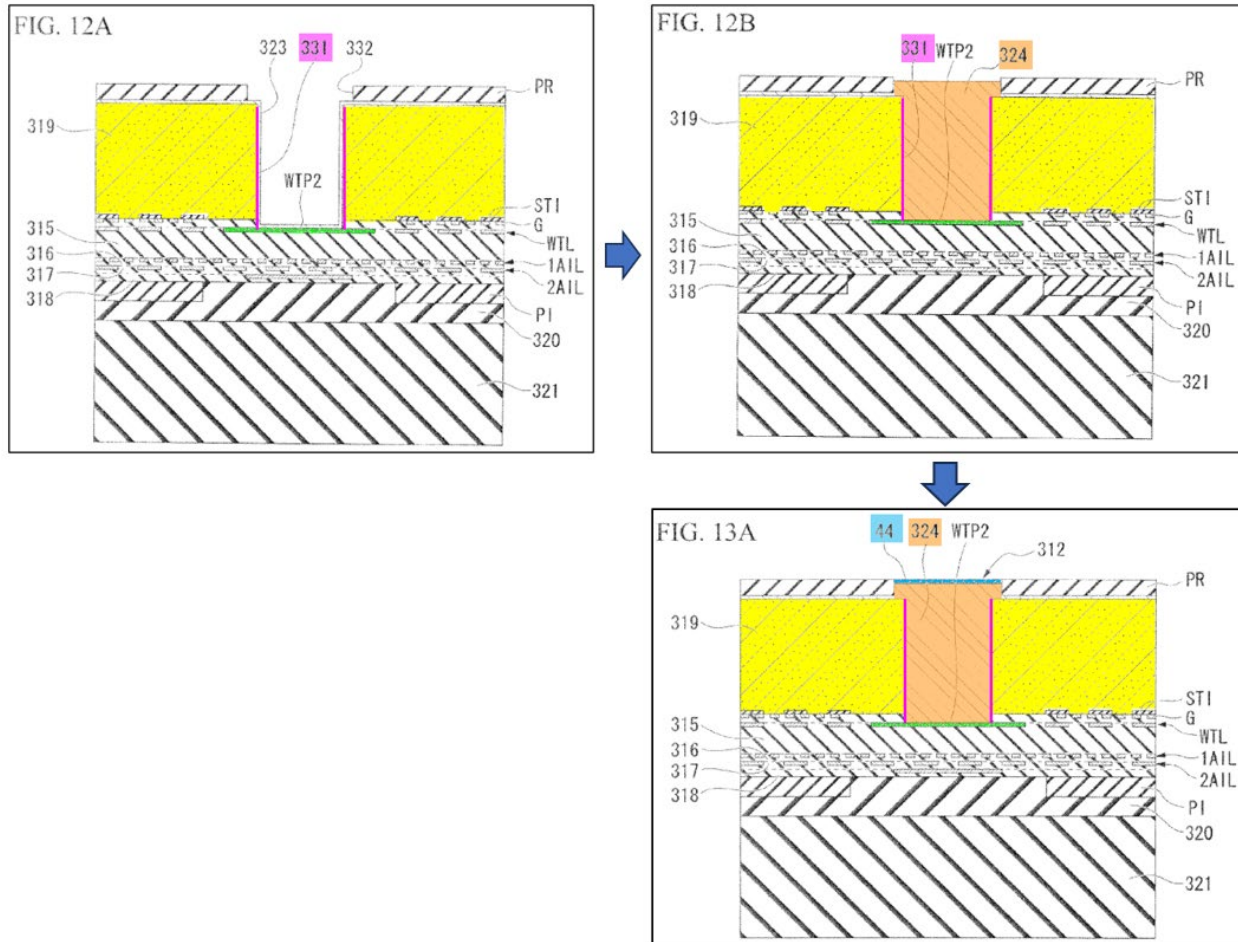
203. In my opinion, *Ide* discloses claim 9 by disclosing the **wiring tungsten pad WTP2** overlying the semiconductor substrate 319 and bonded to the **Cu plating 324** in the **TSV2**. *Ide*, [0125], [0130], [0154]-[0156], Figs. 3B, 12B.



Ide, Fig. 3B.

F. Independent Claim 11**1. “Forming,” depositing,” and “forming” steps**

204. *Ide* discloses a method for making a semiconductor device. *Ide*, [0137], Figs. 6A through 14. As shown below, *Ide* discloses each of the claimed [11a] “forming at least one anchor via,” [11b] “depositing a metal filler,” and [11c] “forming a backside metal layer.” *Ide*, [0152]-[0159], Figs. 11A through 13C. Namely, *Ide* discloses “a dry etching process is performed using the photoresist PR as a mask to form an opening 331 of the through electrode TSV2” (Figure 12A), “a Cu plating 324 is grown using a seed layer 323 as an electrode to fill a via of the through electrode TSV2” (Figure 12B), and “SnAg is formed as the rear bump electrode 312 including the rear bump 44 by plating” (Figure 13A). *Ide*, [0152], [0156]-[0157].



Ide, Figs. 12A-12B, 13A.

2. Remaining limitations of claim 11

205. The remaining limitations of claims 11 are substantially similar to those structural features recited in claim 1. *Supra*, §VII.B. Thus, given the similarity between claims 1 and 11, the remaining features of claim 11 are respectively disclosed by *Ide* for the same reasons discussed above for the corresponding features of claim 1 in §§XV.B.2 through XV.B.5.

G. Claim 12

The method of claim 11, wherein said forming said at least one anchor via comprises forming a cluster of anchor vias.

206. Aside from depending on claim 11, claim 12 is substantially similar to claim 2. *Supra*, §VII.B. Thus, claim 12 is anticipated by *Ide* for the reasons discussed for claims 11 and 2. *Supra*, §§XV.F and XV.C.

H. Claim 13

The method of claim 12, wherein each anchor via within said cluster of anchor vias is oriented perpendicular to an adjacent anchor via within said cluster of anchor vias.

207. Aside from depending on claim 11, claim 13 is substantially similar to claim 3. *Supra*, §VII.B. Thus, claim 13 is anticipated by *Ide* for the reasons discussed for claims 11 and 13. *Supra*, §§XV.F and XV.D.

I. Claim 19

The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate.

208. Aside from depending on claim 11, claim 19 is substantially similar to claim 9. *Supra*, §VII.B. Thus, claim 19 is anticipated by *Ide* for the reasons discussed for claims 11 and 19. *Supra*, §§XV.F and XV.E.

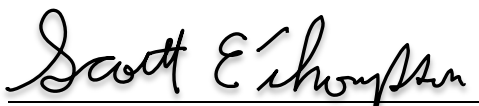
XVI. CONCLUSION

209. For the reasons set forth in Sections XI–XV, it is my opinion that one skilled in the art would have found claims 1-20 of the '826 patent anticipated by or obvious over the prior art.

210. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

211. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 20, 2024

By: 
Dr. Scott E. Thompson, Ph.D.

APPENDIX A

SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

- 1992 Ph.D. (Electrical Engineering), University of Florida
- 1988 Master of Science in Electrical Engineering, University of Florida
- 1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- ❑ Tenured Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- ❑ Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
 - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- ❑ Researcher on advanced chip technology at University of Florida totaling \$4M worth of research contracts.
 - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- ❑ Consultant (non litigation) last 5 years: Xperi Corporation
- ❑ **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- ❑ Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- ❑ Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- ❑ Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- ❑ National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

C. Legal cases

- ❑ Bold is the client
 - Godo Kaisha IP Bridge v/ **Xilinx/TSMC**
 - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017

- **KAIST IP v. Apple**
 - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
 - Case in Korea : Intellectual Property Trial and Appeal Board (“IPTAB”) regarding Korean Patent No. 10-0458288 (hereinafter, “KR ‘288 patent”).
- **Godo Kaisha IP Bridge, Inc. v. NVIDIA**
 - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1
- **Chinese Academy of Sciences v. Intel**
 - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
 - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
 - Beijing Court Testimony IME vs Lenovo 11/21/2021
 - Beijing court Testimony IME vs Intel China 1/12/2022
- **IFT v. TSMC (ITC case)**
 - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
 - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- **NXP v. Impinj**
 - 9,495,631, IPR2020-00543 - filed 2/10/2020
 - 9,633,302, IPR2020-00516 - filed 2/5/2020
 - 6,680,523, IPR2020-01630 - filed 9/17/2020
 - 7,538,444, IPR2021-00003 - filed 10/5/2020
 - Oakland District Court Case No. 4:19-cv-03161-YGR
- **Katana Silicon Technology LLC v. GlobalFoundries 2022**
 - IPR2022-01083
- **Ericsson v. Apple** Brazil Patent BRPI 9811639-8 filed 2022
- **Greenthread v. Intel** Case 6:22-cv-105-ADA filed 12/2022
- **ITC Daedalus v. TSMC** Case 337-TA-1336 filed 10/2022
- **Oasis Tooling, Inc v. GlobalFoundries** C.A. No. 22-312-CJB 3/2023
- **BiTMICRO LLC v. Intel** IPR2023-00781 filed 3/31/2023
- **Longitude Licensing LTD, v Western Digital Technologies, Inc.** IPR2023-01286 filed 8/08/2023

D. Honors and Awards

- ❑ 100 granted US patents, 60 publications and 1 book on semiconductors
- ❑ Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- ❑ Elected to Intel Fellow in 2003
- ❑ Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- ❑ 2008 SEMI award North American Recipient
- ❑ 2014 TiE 50: Top Startup (SuVolta)

- ❑ 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- ❑ 2011 EuroAsia IC Industry Award for start-up
- ❑ 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

E. Publications/Patents

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