

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.;
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,245,826
Filing Date: January 27, 2014
Issue Date: January 26, 2016

Inventors: Hadi Jebory, David J. Howard, and Scott B. Stetson
Title: ANCHOR VIAS FOR IMPROVED BACKSIDE METAL
ADHESION TO SEMICONDUCTOR SUBSTRATE

PATENT OWNER'S PRELIMINARY RESPONSE

Case No. IPR2024-01405

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung's Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants' Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)

I. INTRODUCTION

On September 20, 2024, Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) submitted a Petition (Paper 1, “Petition” or “Pet.”) to institute *inter partes* review (“IPR”) of U.S. Patent No. 9,245,826 (Ex. 1001, the “’826 Patent”), challenging Claims 1-20 (the “Challenged Claims”). The Petition asserts that: (i) Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 are anticipated by United States Patent Application Publication No. US 2009/0079056 to Conn (“Conn” or Ex. 1004); (ii) Claims 1, 2, 4-7, 9, 11, 12, 14-17, 19 are rendered obvious over Conn in view of knowledge of a person of ordinary skill in the art (“POSA”); (iii) Claims 8 and 18 are rendered obvious over Conn in view of knowledge of a POSA and applicant admitted prior art; (iv) Claims 1, 2, 4-7, 11, 12, 14-17 are rendered obvious over U.S. Patent Application Publication No. US 2014/0138844 to Gambino et al. (“Gambino” or Ex. 1005) in view of Conn; (v) Claims 10 and 20 are rendered obvious over Gambino in view of Conn and U.S. Patent Application Publication No. US 2012/0104546 to Ding et al. (“Ding” or Ex. 1008); (vi) Claims 1, 8-11, and 18-20 are anticipated over U.S. Patent Application Publication No. US 2013/0082382 to Torii (“Torii” or Ex. 1009); and (vii) Claims 1-3, 9, 11-13, and 19 are anticipated over U.S. Patent Application Publication No.

US 2012/0256310 to Ide (“Ide” or Ex. 1010). The Board should deny the Petition for at least the reasons described briefly below.

In Ground 1, *Conn* does not disclose the claimed anchor via located in a corner of a semiconductor substrate, and Petitioner attempts improperly to cure this deficiency with annotations that assume disclosures not present in *Conn*. *Conn* also fails to anticipate because it does not disclose the claimed “metal filler having a protrusion” and does not disclose that the anchor vias cannot be used to provide a ground connection.

In Ground 2, Petitioner attempts to combine *Conn* with the knowledge of a POSA to cure two deficiencies in *Conn*: the disclosure of a metal layer on the “backside” and the use of “active devices.” But, even assuming the Petitioner is correct regarding the knowledge of a POSA, Ground 2 does not cure the deficiencies of *Conn* explained in Ground 1.

In Ground 3, Petitioner combines *Gambino* with *Conn* (and, for two dependent claims, adds *Ding* to this combination), but this combination does not result in the claimed invention because, even assuming for the purposes of this Preliminary Response only that *Gambino*’s metal pads could be replaced with the vias in *Conn*, the resulting combination would provide a ground connection to the

active devices disclosed in *Gambino*, and would therefore be expressly different from the Challenged Claims which require no such connection.

In Ground 4, *Torii* does not anticipate the claims because the Petition fails to show that the vias in one embodiment of *Torii* that are relied upon in the Petition are present in a corner of a semiconductor die as required by the Challenged Claims. Additionally, *Torii* fails to disclose the claimed backside metal layer that is on a semiconductor surface, and further expressly discloses that the vias can be used to provide electrical connections to discharge static electricity, *i.e.*, grounding.

In Ground 5, *Ide* fails to disclose the claimed “backside metal layer” for several reasons, including that the alleged metal layer is not on the semiconductor surface.

As discussed below, the Petition should also be denied in the discretion of the Director under 35 U.S.C. § 314(a), as the projected Final Written Decision date of March 30, 2026 is after the January 5, 2026 trial date in the underlying litigation.

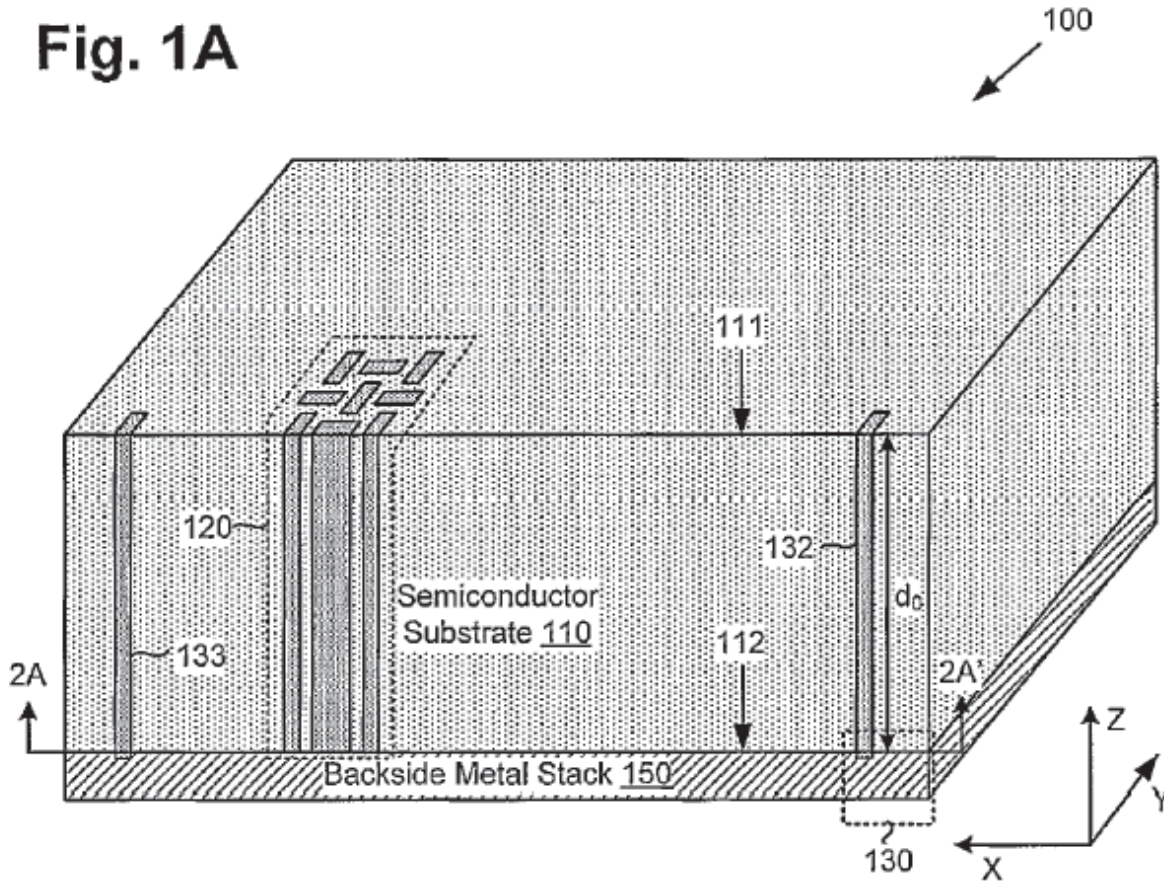
II. THE '826 PATENT

The '826 Patent describes and claims an improvement in semiconductor design. More specifically, the present invention relates to “anchor vias for improved backside metal adhesion to a semiconductor substrate.” '826 Patent, 1:42-46. The

'826 Patent describes problems in the art. When a backside metal layer is attached to a semiconductor substrate using an adhesive, as conventionally done, “unacceptably low yields are often achieved during fabrication due to the backside metal layer peeling from the semiconductor substrate.” *Id.*, 1:36-38. This is because “fabrication procedures, such as semiconductor die singulation and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die.” *Id.*, 1:30-34.

The invention of the '826 Patent is to place one or more through-silicon vias, called an “anchor via,” in the corner of the semiconductor die where these stresses are the greatest, and to use anchor vias “to improve backside metal adhesion.” *Id.* 2:44-47. Figures 1A and 1B of the '826 Patent, reproduced below, are exemplary:

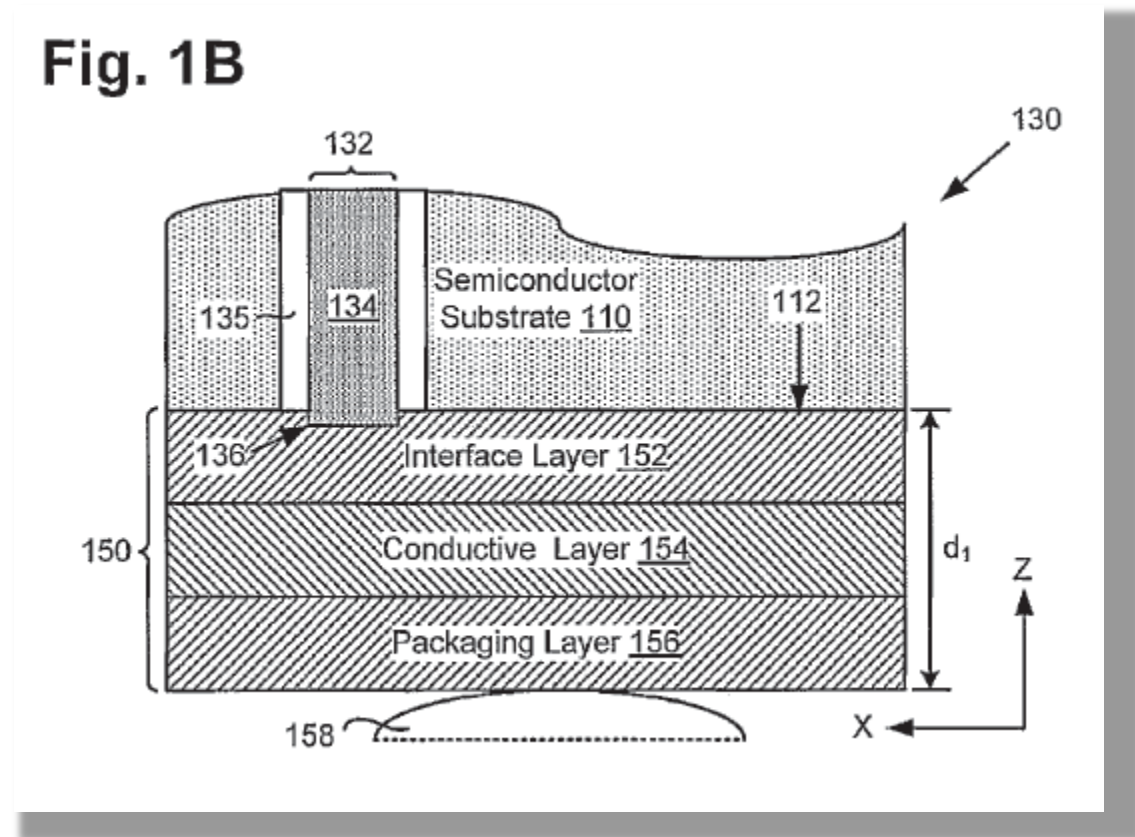
Fig. 1A



'826 Patent, FIG. 1A. In Figure 1A, the '826 Patent discloses two anchor vias, 132 and 133, which are formed in the semiconductor substrate in “a peripheral region” as well as a group of vias 120 which are not anchor vias, but rather are formed “in a core region of semiconductor substrate 110.” *Id.*, 3:2-5. The core vias 120 “provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110.” *Id.*, 3:5-11. One example is given of an active device that is grounded using the core vias, which is “the emitters

of bipolar transistors.” *Id.*

The anchor vias, on the other hand, do not provide ground connection but “instead provide[] physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150.” *Id.* 3:12-17. The bottom of an anchor via 132 is shown below in Figure 1B:



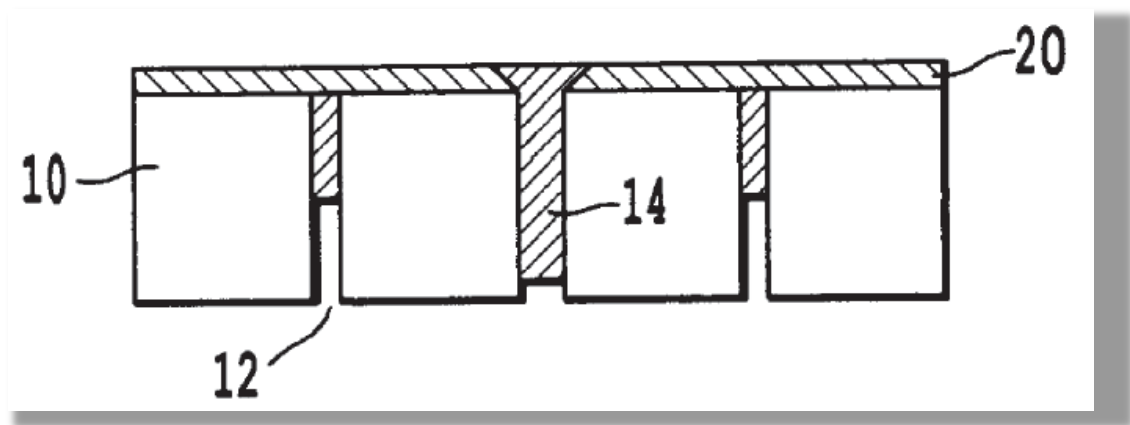
’826 Patent, FIG. 1B. This anchor via contains a protrusion 136 that extends into the metal layer, “such that when interface layer 152 is deposited on bottom side 112 of semiconductor substrate 110, the additional contact between metal filler 134 and

interface layer 152 form a very strong physical, metal-on-metal bond.” *Id.* 3:43-48.

III. THE ALLEGED PRIOR ART

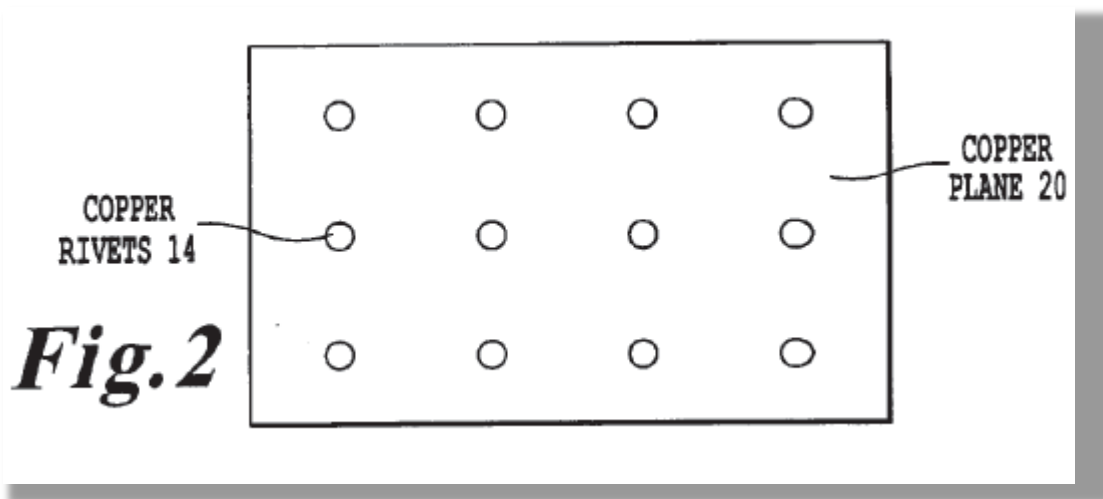
A. Conn

U.S. Patent Application Publication No. US 2009/0079056 to Robert O. Conn is titled “Large Substrate Structural Vias.” *Conn* relates to “a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.” Ex. 1004, [0003]. According to *Conn*, problems existed in the art where “extensive and repeated temperature changes cause fatigue of the package and the structure including the package.” *Id.* [0005]. *Conn* recognizes that “[o]ne place where this fatigue occurs is between the layers of a package laminate, or between a packaged part and a PCB.” *Id.*



Ex. 1004, Fig. 1. *Conn* discloses in Fig. 1, above, a “conducting layer” 20 that is connected to a “via conductor 14” which is formed in “via 12” to provide an anchor

via, which is “considered a rivet formed in the carrier substrate and in contact with the conducting layer 20 by which the conducting layer 20 maintains its structure under thermal stress.” *Id.* [0028]. *Conn*’s Figure 2 shows the conducting layer 20 being penetrated by twelve of the via conductors 14, which are annotated as “copper rivets”:



Ex. 1004, Fig. 2. *Conn* also discloses that, although only the copper plane 20 is shown in Figure 2, that the semiconductor substrate is larger in surface area than the copper plane. *Id.* [0030], [0031] (“In one embodiment, the major part of the first surface covered by the conducting layer covers at least 10% of an entirety of the surface area of the carrier substrate.”).

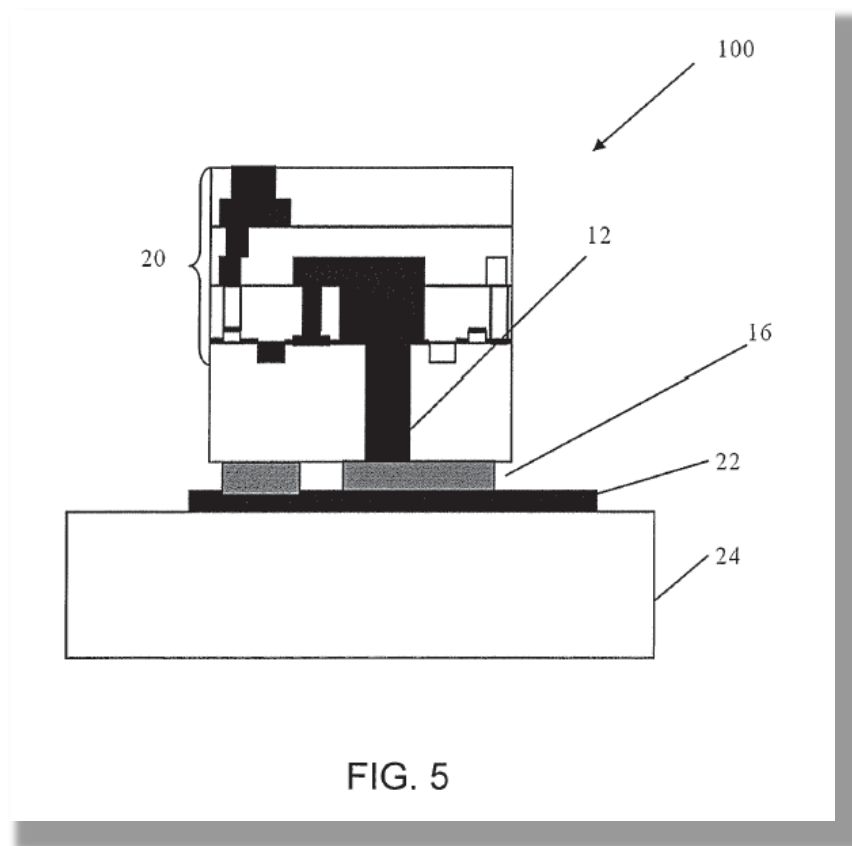
Conn does not mention placing the anchor vias in the corner of the semiconductor substrate, and the only mention of a corner in *Conn* is the corner of

the via itself. Ex. 1004, [0054]. *Conn* also does not state that the vias are used for structural protection during fabrication. Notably, *Conn* also discloses that the via conductors 14 disclosed in Figure 1 and Figure 5 “can have a volume less than a volume of the via in which the conductor is formed” (*Id.* [0043]), and that different layers of the substrate “can be connected to one or many second via conductors . . . similar to the via conductor 14” and can be “supplied with a control signal/electrical potential . . .”. *Id.* [0046], [0047].

B. Gambino

U.S. Patent Application Publication No. US 2014/0138844 to Jeffrey P. Gambino et al. is titled “Patterned Backside Metal Ground Plane For Improved Metal Adhesion.” *Gambino* discloses a die including a metal ground plane 16 that includes through-silicon vias (TSV’s). Ex. 1005, Abstract. *Gambino* describes a problem with existing designs for RF analog chips, namely that the emitter ground leads used in SiGe heterojunction bipolar transistor (HBT) RF designs “are normally contacted to the package either using multiple wire bonds or flip chip solder bumps.” *Id.* [0002]. Wire bond leads have high inductance, and while flip chip solder bumps have low inductance, “they increase packaging complexity and are expensive.” *Id.*

Gambino proposes a solution to the problem of grounding emitters in RF analog chips, which is to place through-silicon vias (TSVs) in a semiconductor die, forming a metalized ground plane on a backside of the substrate, and placing the TSVs in contact with the ground plane. *Id.* [0005]. “Grounded through silicon vias (TSVs) can be used to reduce ground lead inductance and reduce the bond pad area on the chip surface.” *Id.* [0016]. *Gambino* shows an example of one of these TSV’s 12, grounded to the metals 16 and 22 in Figure 5:

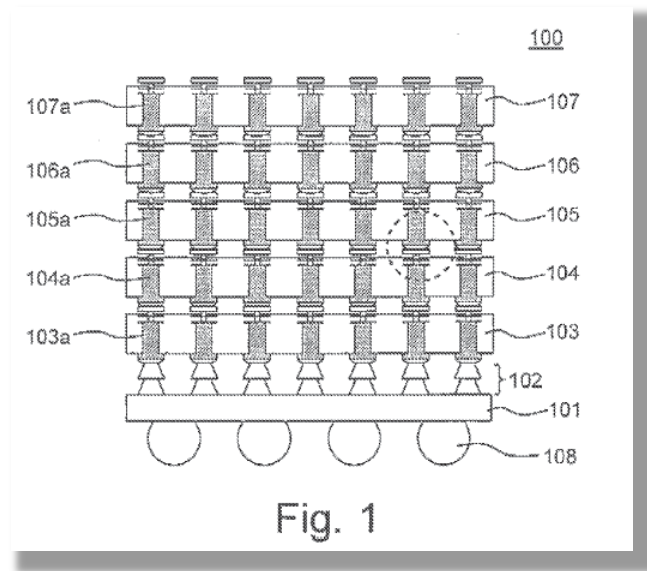


Ex. 1005, FIG. 5. Nowhere does *Gambino* disclose or contemplate using vias for a

purpose other than providing ground connections, and *Gambino* explicitly discloses the use of a metal pad 16a “to provide mechanical support.” *Id.* [0028]. *Gambino* does not disclose or contemplate any problems or solutions having to do with anchoring a semiconductor substrate to a metal layer.

C. Torii

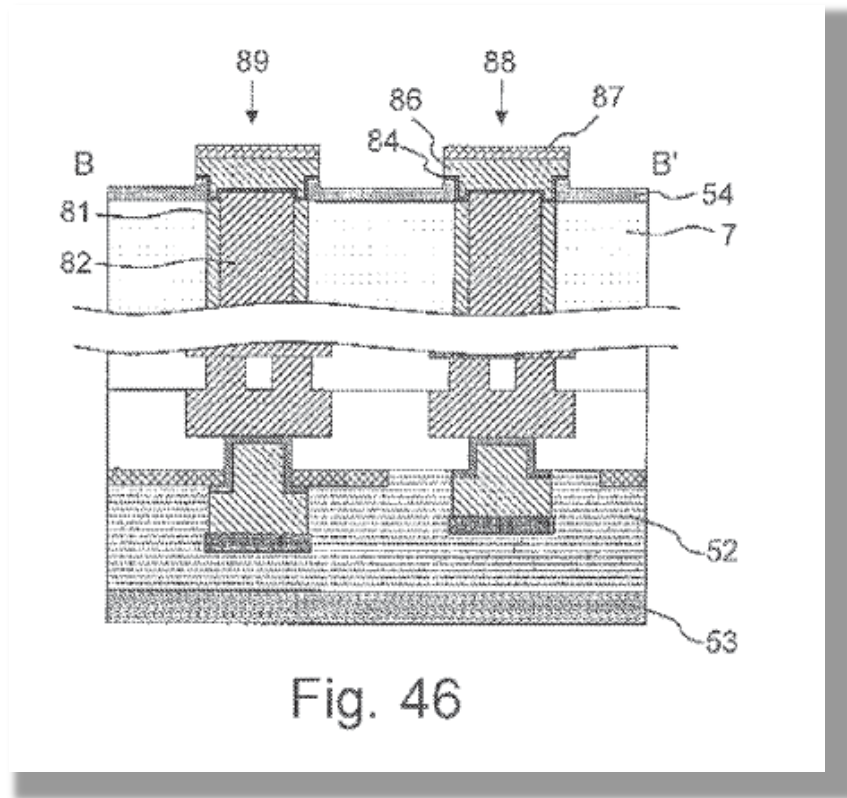
U.S. Patent Application Publication No. US 2013/0082382 to Koji Torii is titled “Semiconductor Device.” *Torii* discloses “a semiconductor device provided with an electrode penetrating through a substrate.” Ex. 1009, [0002]. The problems discussed in *Torii* arise in semiconductor devices which are vertically stacked, where through silicon vias (TSVs) are used to create the electrical connections between vertically-stacked chips. *Id.* [0004]. Figure 1 of *Torii*, shown below, discloses a group of stacked semiconductor chips that are connected by TSVs 104a, 105a, 106a, and 107a:



Ex. 1009, Fig. 1. *Torii* describes that when joining the chips, the metal “becomes liable to segregation at the interface” which “may decrease joint strength and induce bump cracks.” *Id.* [0007].

Torii describes the creation of two types of through-silicon vias: a “main TSV” and a “sub-TSV.” *Id.* [0045], [0048]. The main TSV is used “mainly as a current pathway” and a sub-TSV “can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.” *Id.* [0048]. In one embodiment, *Torii* describes that the TSVs can be formed from the front surface of the substrate, rather than the rear. *Id.* [0093] (Exemplary Embodiment 5). In this embodiment, as shown in Figure 46 which is heavily cited in the Petition, there exists a “second main bump 88” and a “second sub-bump 89” that are on the back side of

the device:

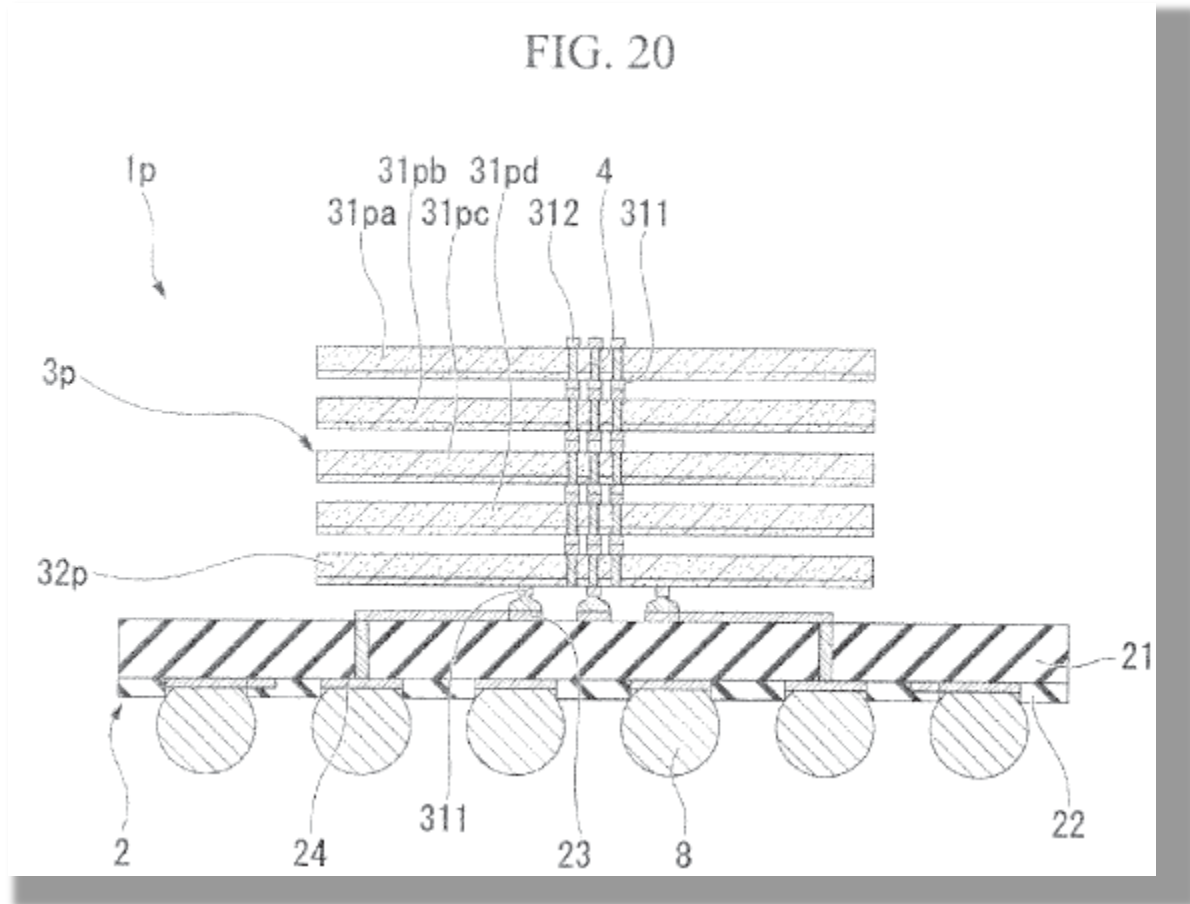


Ex. 1009, Fig. 46, [0100]. Also located on the rear of the device is a “rear-surface protective film 54,” (*Id.*) but the bumps that form elements 88 and 89 are not shown connected to a metal layer.

D. Ide

U.S. Patent Application Publication No. US 2012/0256310 to Akira Ide (is titled “Semiconductor Device.” *Ide*, like *Torii*, also describes a multi-level vertically

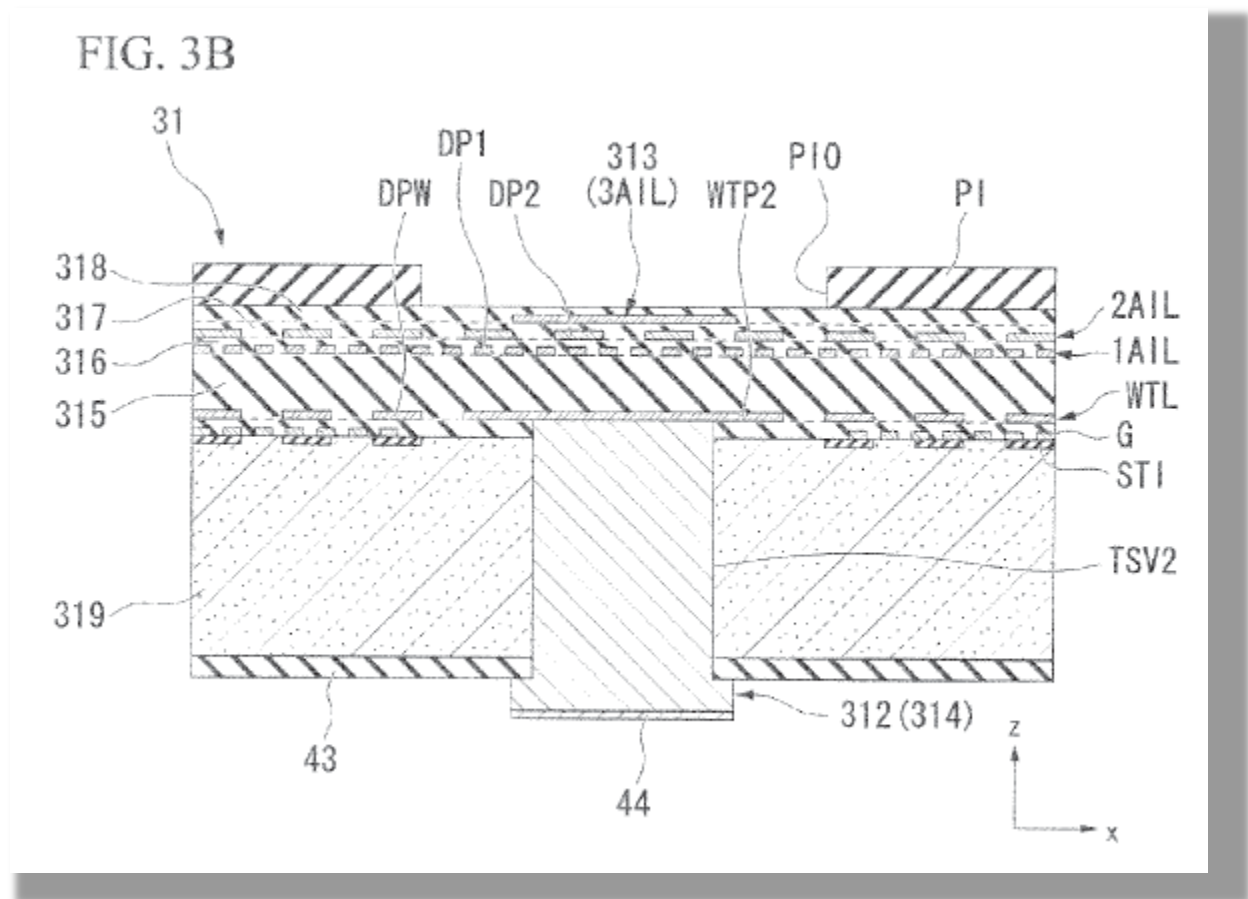
stacked semiconductor structure. Ex. 1010, Abstract. *Id*e discloses a plurality of memory chips 31pa to 31pd and an interface chip 32p, as shown in FIG. 20:



Ex. 1010, FIG. 20, [0006]. Each of the memory chips and the interface chips include a “surface mark” and a “rear mark” on each side of the chip, which “are used for alignment when semiconductor chips are stacked.” *Id*. [0010]. The various marks are photographed by the equipment used to assemble the chips. *Id*. The inventor recognized a problem, which is that “a recognition error of the surface mark 313

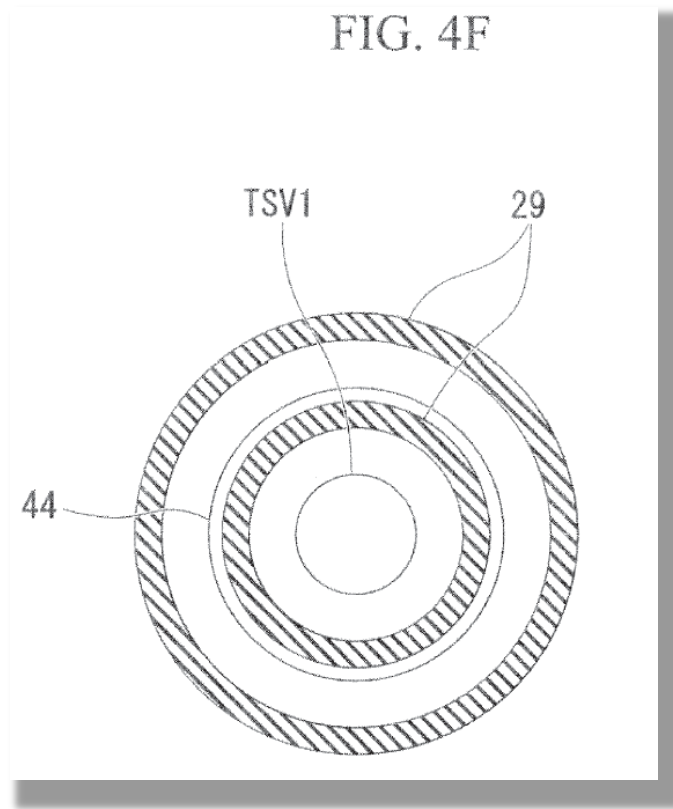
occurs in a TSV stacking process and a throughput of the above-described assembly process is considerably degraded.” *Id.* [0022].

Ide also discloses Figure 3B, reproduced below:



Ex. 1010, FIG. 3B. According to *Ide*, Figure 3B discloses a “surface mark 313” that is formed from aluminum, and a “through electrode TSV2 for a mark.” *Id.* [0125]. The “rear bump 44 in which a rear mark is formed is formed below the through electrode TSV2 for a mark.” *Id.* The rear bump 44 is circular, with the TSV

penetrating through it, as shown from the bottom view of Figure 4F:



Ex. 1010, FIG. 4F. The rear bump 44 is shown, as well as the TSV and insulating trench 29. *See Id.* at [0119] (“an insulating trench 29 is formed in a portion of the wiring through electrode.”). *Id.* also does not disclose the use of a via for the purpose of anchoring, but rather focuses on creating a rear mark that is more visible to the equipment used for fabricating stacks of vertically-connected chips. *Id.* [0128].

IV. LEVEL OF ORDINARY SKILL IN THE ART

For the purposes of this Preliminary Response only, Patent Owner utilizes

Petitioner’s proposed level of skill in the art: “at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Additional relevant work experience can compensate for less education, and vice versa.” Pet. at 23 (citations omitted).

V. CLAIM CONSTRUCTION

Petitioner presents one claim construction argument, which is that the method steps of Challenged Claim 11 should not be read to require steps [11b] and [11c] to be performed in their recited order. Pet. at 21-22. As discussed below, even assuming the broad interpretation of this claim as advanced by Petitioner, each of Petitioner’s grounds for anticipation and obviousness fail. Therefore, it is not necessary for the Board to construe Claim 11 or reach this issue in order to deny institution.

VI. PETITIONER HAS NOT DEMONSTRATED A REASONABLE LIKELIHOOD OF SUCCESS FOR THE GROUNDS ADVANCED IN THE PETITION, AND THE PETITION SHOULD BE DENIED

In order to anticipate the claimed invention, a prior art reference must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “However, a reference can

anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983).

The Board has held that a failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. *See, Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Decision Denying Institution of *Inter Partes* Review, Paper 9 at 9-10 (P.T.A.B. June 26, 2015)

(denying institution for failure to identify the differences between the claimed subject matter and the prior art).

In arriving at an obviousness determination, the Board must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims and a relevant, skilled artisan not only could have made, but would have been motivated to combine all the prior art references in the way the patent claims and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have the motivation to combine those references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual finding as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a person of skill in the art would have had a reasonable expectation of success from such a combination). This combinability determination, as supported by an

articulated motivation to combine, requires a plausible rationale as to why those prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references” *Innogenetics, N.V. v. Abbott Lab’ys.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

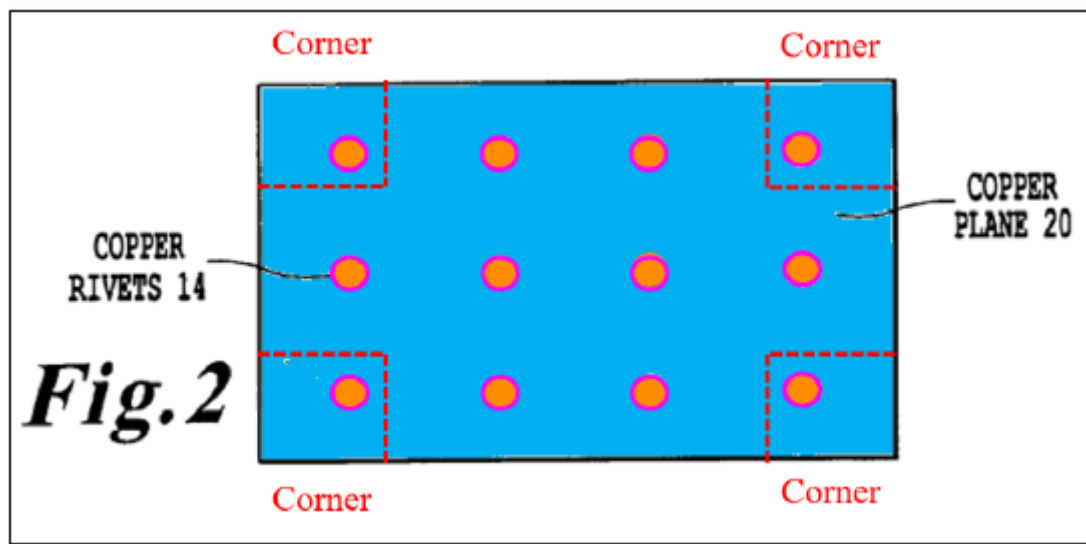
To demonstrate inherent obviousness, an inherent limitation must necessarily be present in the combination of references. *See Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376 (Fed. Cir. 2019); *LBT IP I LLC v. Apple Inc.*, No. 2022-1613, 2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023). It is not enough to merely show that it is likely to be present. *Id.*

A. Ground 1: The Challenged Claims Are Not Anticipated By *Conn*

1. The Petition Does Not Show That *Conn* Discloses an Anchor Via Disposed at the Corner of the Semiconductor Substrate

The Challenged Claims each require “at least one anchor via disposed in at least one corner of a semiconductor substrate.” ’826 Patent, cls. 1, 11. The Petition

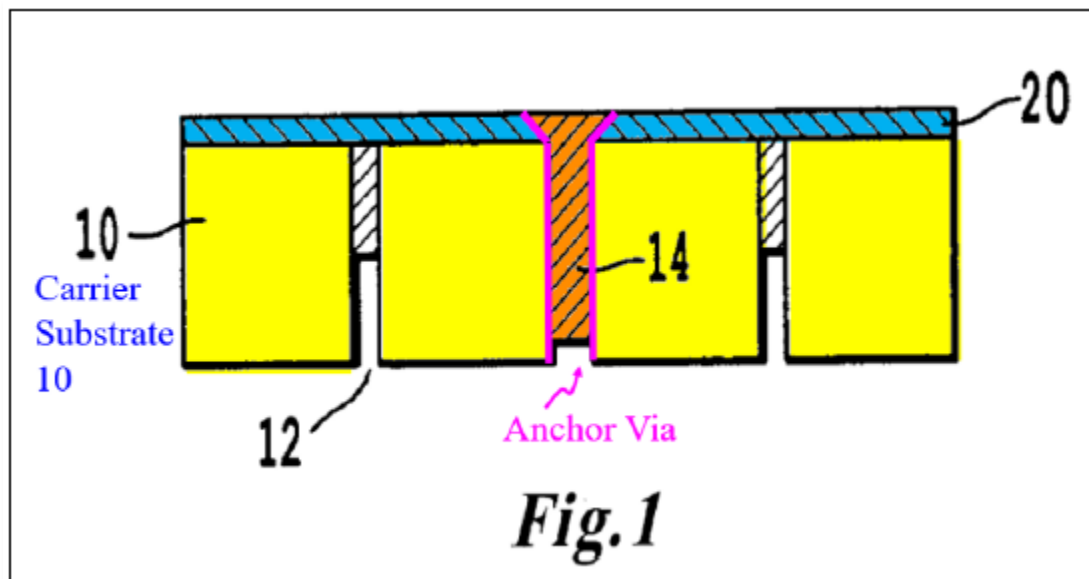
fails to show that *Conn* discloses this claim element. Instead, Petitioner invents this disclosure by annotating Figure 2 of *Conn* to draw dotted lines delineating the “corner” of the copper plane and orienting them in such a way to enclose one copper rivet in each corner. Pet. at 29. This artificial annotation of Figure 2 is shown below:



Id.

This interpretation of *Conn* fails for several reasons. First, it artificially draws the “Corner” of *Conn*’s Copper Plane 20 large enough to enclose one copper rivet in each corner. But the disclosure of a copper rivet in a corner is absent from *Conn*. Petitioner’s only citations to *Conn* for this claim element do not support its interpretation. Petitioner cites to Paragraph 29, which states only that the carrier substrate in Figure 1 includes “a plurality of anchor vias (e.g., via conductor 14).”

Pet. at 28 (quoting Ex. 1004 at [0029]). But Figure 1 only discloses one anchor via 14, and it is located in the middle of the substrate, rather than the corner (even Petitioner's annotations note this):

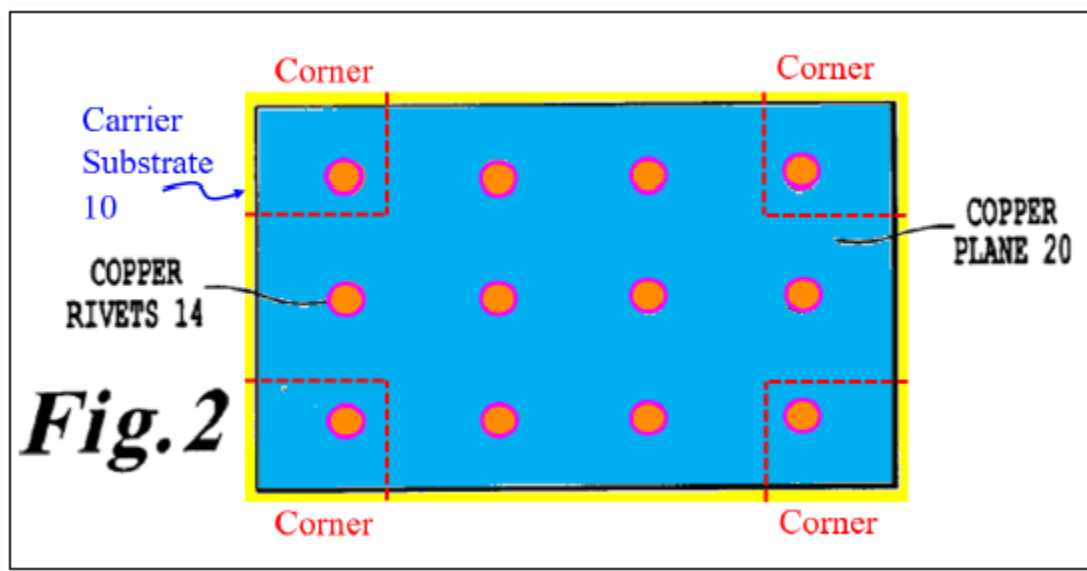


Second, Petitioner cites to the plan view in Figure 2 which, according to Petitioner, “shows the plurality of anchor vias (*see* copper rivets 14 in Figure 2) are “distributed relative to the conducting layer 20 in a pattern.” Pet. at 28 (quoting Ex. 1004 at [0035]). But merely noting that the anchor vias are distributed in “a pattern” does not disclose that the anchor vias are disposed at the corners. Petitioner also cites to its expert declaration, which merely parrots back the previous citations and states that “those skilled in the art seeing Figure 2 would understand that the depicted

anchor via pattern is intended to repeat across the length and width directions of the conducting layer 20” and that this includes putting anchor vias in the corners. Ex. 1003 ¶ 83. Neither Petitioner nor its expert note that *Conn* never uses the term “corner,” except when referencing the corner of the via. *See* Ex. 1004 at [0054].

Petitioner’s analysis of the Figures in *Conn* fails because it interprets dimensionality from an exemplary figure, and attempts to fill the gaps in that figure through the use of the understanding of the person of skill in the art, which is improper in an anticipation analysis. Absent disclosure in the specification to the contrary, patent drawings cannot be used to show specific sizes of elements. *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“The [patent] is devoid of any indication that the proportions of the groove and fins are drawn to scale. . . . Under our precedent . . . patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”). The Petition makes no attempt to analyze the spacing or formatting the vias in relation to the size or shape of the conducting layer, and *Conn* contains multiple embodiments of different densities, sizes, and shapes. Ex. 1004 at [0035]-[0036], [0039]. This lack of analysis alone is fatal to the Petition.

Petitioner's analysis is fatally flawed for another independent reason, which is that its (mistaken) interpretation of *Conn* puts the anchor vias in the corner of the Copper Plane 20, but the Challenged Claims require that the anchor vias be disposed in at least one corner "of a semiconductor substrate." '829 Patent, cls. 1, 11. Here, Petitioner attempts to cure the deficiency in the prior art, by noting that *Conn* discloses that the conducting layer can cover "more than 90% of an entirety of the surface area of the carrier substrate" and creating the annotated figure below which shows Petitioner's interpretation of the carrier substrate (in yellow) poking out from behind the edges of the copper plane:



Pet. at 29-30 (citing Ex. 1004 at [0031], Ex. 1003 ¶ 84. But this interpretation assumes disclosure in *Conn* that does not exist, and ignores the previous paragraph

of *Conn* which states that in one embodiment, “the major part of the first surface covered by the conducting layer covers at least 10% of an entirety of the surface area of the carrier substrate.” Ex. 1004 [0030]. Petitioner merely selects an embodiment where the copper plane covers 90% of the carrier substrate, then assumes without support that the carrier substrate is arranged in its annotated version of Figure 2. But “[p]rior art that must be modified to meet the disputed claim limitation does not anticipate the claim.” *Enplas Display Device Corp. v. Seoul Semiconductor Co.*, 909 F.3d 398, 405 (Fed. Cir. 2008). Anticipation requires that the prior art must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim’.” *Net MoneyIn*, 545 F.3d at 1369 (quoting *Connell*, 722 F.3d at 1548). Petitioner’s attempt to backfill the disclosure in *Conn* with annotations and additional expert testimony alone is evidence that the disclosure in *Conn* is insufficient for an anticipation analysis.

This situation is similar to that in *Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1062 (Fed. Cir. 2017), where the Petitioner in an anticipation analysis argued that a statement in the specification that embodiments of the prior art “may be implemented by program instructions stored in a memory medium” meant that a claim element requiring a storage medium to be encoded with a set of instructions

was disclosed. The Board found, and the Federal Circuit affirmed, that the language in the prior art applied to only one embodiment, and the POSA would not “at once envisage” the combination of the claimed invention given the disconnected teachings in the prior art. *Id.* at 1070.

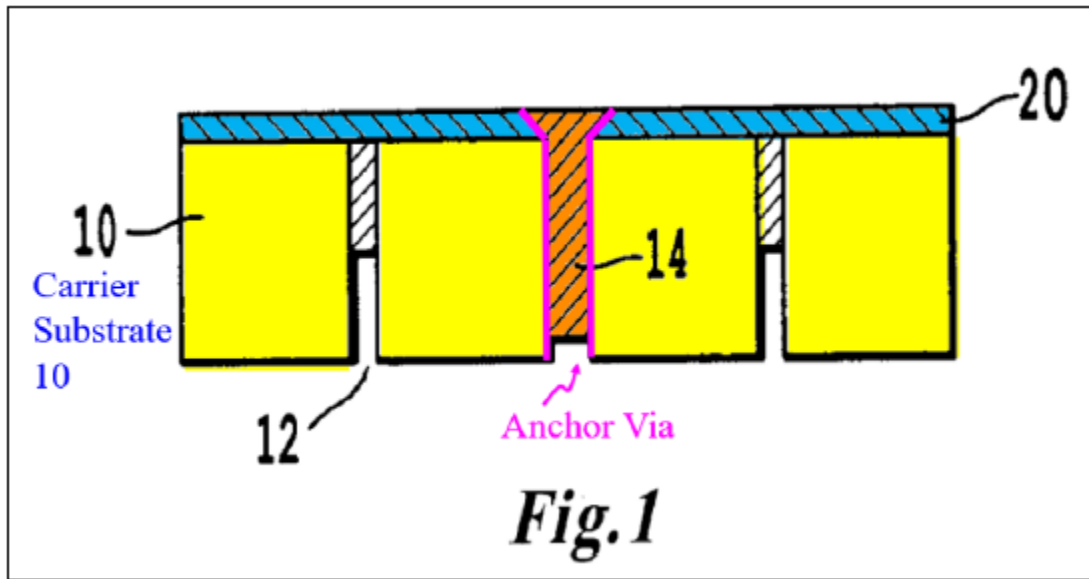
This failure of the Petition is particularly apparent here, where the anchor vias in the '826 Patent and the anchor vias in *Conn* are designed for vastly different purposes. The '826 Patent describes that anchor vias are arranged at the corners to protect the semiconductor die from stresses that occur during fabrication. “[F]abrication procedures such as semiconductor die singulation and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die.” '826 Patent, 1:30-34. *Conn*, however, concerns itself with stresses that occur from thermal expansion, such that the anchor vias must be distributed evenly, rather than at the corners. “[E]xtensive and repeated temperature changes cause fatigue of the package and the structure including the package.” Ex. 1004, [1005]. The Petition’s attempt to use disclosure of anchor vias designed to prevent a different type of stress than those in the invention claimed in the '826 Patent further evidences how strained Petitioner’s interpretation of the “corner” in *Conn* is.

Because the Petition has not shown that the claimed anchor vias are located in the corners of the substrate as required by independent Claims 1 and 11, Ground 1 of the Petition fails.

2. The Petition Does Not Show That *Conn* Discloses a Corner Anchor Via with a Metal Filler Having a Protrusion

As discussed immediately above, *Conn* does not anticipate any of the Challenged Claims because the Petition does not show how it discloses anchor vias located in the corners of the substrate, the Petition also fails to show that the corner anchor vias are filled with metal, and that the metal filler has a “protruding portion extending from a back-side of said semiconductor substrate.”

Additionally, *Conn* only discloses such a protrusion with respect to an anchor via that is squarely in the center of the copper plane, and nowhere discloses that a corner via has any protrusion at all:

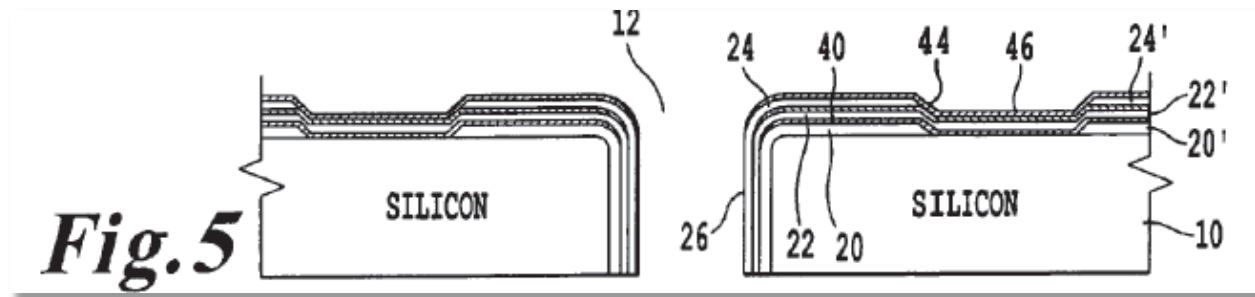


Pet. at 30-31 (annotating Ex. 1004 at Fig. 1). Aside from this figure, as the Petition admits, *Conn* only discloses that the rivets are mechanically “connected to” and “in contact with” the conducting layer 20. *Id.* at 31 (citing Ex. 1004 [0028]-[0030], [0038], [0040], [0055], Figs. 1-3). But none of these citations or figures show an anchor via protruding into the copper plane except for Figure 1, and this only disclosure is in the middle of the substrate, not at the corner. For this additional reason, the Petition fails to show that Claims 1 and 11 (and thus any of the Challenged Claims) are anticipated by *Conn*.

3. The Petition Does Not Show That *Conn* Discloses Metal Filler That Does Not Provide Ground Connection to Active Devices

The Challenged Claims have a specific requirement that the metal filler in the anchor vias is used *solely* for anchoring, and “does not provide ground connection to one or more active devices in said semiconductor substrate.” ’826 Patent, cls. 1, 11. The Petition argues that this claim element is met as “*Conn* discloses [this claim element] by *not* disclosing that any anchor vias provide any ground connection but instead disclosing the anchor vias or the via conductors therein do not need to reach the opposite side of the carrier substrate, thus recognizing the purposes of the anchor vias is *not* to provide any ground connection.” Pet. at 36-37.

But *Conn* specifically discloses and claims that the anchor vias, which contain conducting metal and are attached to a copper ground plane, can also be used to provide electrical connections and, therefore, provide grounding to active devices. *Conn* discloses, in Figure 5 and its associated discussion, that a via 12 can be supplied with conducting layers 20 and 24 that connect between dielectric layers (such as dielectric layer 44):



Ex. 1004, Fig. 5, [0044]. *Conn* discloses that “the conducting layer 20 has two regions 20 and 20’ electrically discontinued that can be supplied with different signals/electrical potentials.” *Id.* [0045]. These potentials are supplied by the vias: “[t]he conducting layers 20’, 22’ and 24’ can be connected to one or many second via conductors (not shown) similar to the via conductor 14 and thus, the conducting layers 20’, 22’ and 24’ can be supplied with a control signal/electrical potential independent of the control signal/electrical potential supplied to layers 20, 22, and 24.” *Id.* [0047].

What’s more, *Conn* specifically claims the use of a via to electrically connect segments of the die that are separated by dielectric. Claim 19 of *Conn* claims: (1) a substrate having plural anchor vias; (2) a first set of conducting layers having “plurality dielectric layers disposed between respective ones of the first set of first conducting layers,” and (3) “a first via conductor disposed in one of the first anchor vias and connected to the first set of conducting layers.” Ex. 1004, cl. 19.

This claim, coupled with the disclosure in Figure 5 and associated text, shows that *Conn* uses the anchor vias both for mechanical support and to transmit electrical potential between dielectric layers and, therefore, the Petition's unsupported statement that the via conductors in *Conn* cannot be used to provide a ground connection because they do not "go all the way through" the via does not establish that the anchor vias are not used for grounding of active devices. The Petition also states that *Conn* does not disclose the lack of grounding of active devices because *Conn* states that the carrier substrate "may only have '[p]assive components.'" Pet. at 37 (citing Ex. 1004 [0026]). But *Conn*'s use of the term "may" clearly means that active devices may also exist in the substrate, therefore opening the via conductors for grounding these active components. Therefore, the Petition additionally fails for this reason.

B. Grounds 2A and 2B: The Challenged Claims Are Not Rendered Obvious by *Conn* in View of the Knowledge of a POSA and/or AAPA

The Petition, as best understood, attempts to combine *Conn* with the knowledge of a POSA to argue that the disclosure of "backside" or "active devices" would have been obvious based on *Conn* and a POSA's knowledge. Pet. at 45. The Petition appears to be arguing: (1) that the POSA would have understood that *Conn*'s

metal layer is on the backside; and (2) that the POSA would have understood that, if active devices were shown mounted in the chip described in *Conn*, that they would not be grounded.

To the first point, for the purposes of this Preliminary Response, Patent Owner does not dispute that *Conn*'s copper plane can be considered the "backside" of the device and, thus, the obviousness analysis is unnecessary. *Conn* fails to render any of the Challenged Claims obvious for the same reasons it does not anticipate, namely: (1) that *Conn* does not disclose anchor vias located in the corner of the semiconductor device; (2) that *Conn* does not disclose corner anchor vias containing a protrusion; and (3) that *Conn* expressly discloses that the vias can be used for electrical connections and, therefore, grounding. *See supra* at VI.A. To the extent the Petition is arguing that certain of these missing features may not be anticipated by *Conn* but would be obvious, the Petition only specifically mentions the "backside" and "active devices" claim elements. Pet. at 45. The Petition makes no argument, for example, that the POSA would have understood that the vias are placed in the corner of the substrate, despite no explicit disclosure of this claim element and, therefore, the obviousness argument fails for the same reasons as the anticipation argument.

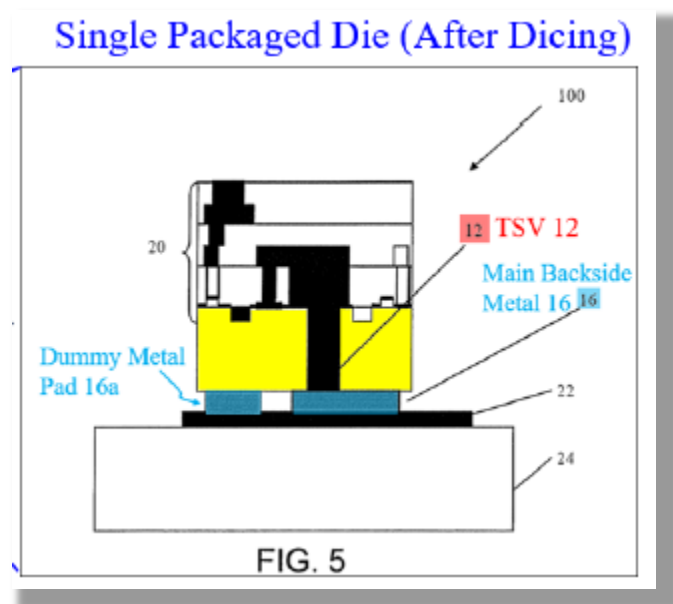
To the second point, the Petition makes no effort to explain how or why it would have been obvious to the POSA to replace *Conn*'s conducting vias with the non-conducting vias disclosed in *Wang*. The Petition merely states that "*Wang* . . . provides a use case for *Conn*'s carrier substrate" and that the substrate in *Wang* "includes multiple heat-dissipating dummy TSVs 64." Pet. at 45-46. But, like in *Conn*, the TSV's in *Wang* can be used for electrical connection: "Through-substrate vias (TSVs) 64 are formed in substrate 62, and electrically connect features on opposite sides of substrate 62." Ex. 1019, 3:16-19. The Petition makes no other attempt to explain or analyze how either *Conn* or *Wang* would be modified by the POSA to isolate the TSVs and use them to provide anchoring only, as required by the claims.

Petitioner's remaining arguments for Grounds 2A and 2B relate to either the recited order of steps in Claim 11, or dependent claims. Because, as discussed *supra*, the Petition fails to show that Claim 11 is anticipated or obvious under the broadest reading of Claim 11 (that performing the steps in the recited order is not required), analysis of this claim construction is not necessary. And because the prior art cited by Petitioner fails to render obvious the independent claims, discussion of the dependent claims is also not necessary for institution of this Petition to be denied.

C. Grounds 3A and 3B: The Challenged Claims Are Not Rendered Obvious by *Gambino* in View of *Conn* and/or *Ding*

1. The Combination of *Gambino* and *Conn* Does Not Result in the Claimed Invention Because the Resulting Vias Would Provide Ground Connection

Gambino discloses a through-silicon via (TSV) located in the middle of the semiconductor die, and a “metal pad 16a” that is located in the corner of the die. Petitioner’s annotated version of *Gambino*’s Figure 5 is shown below:

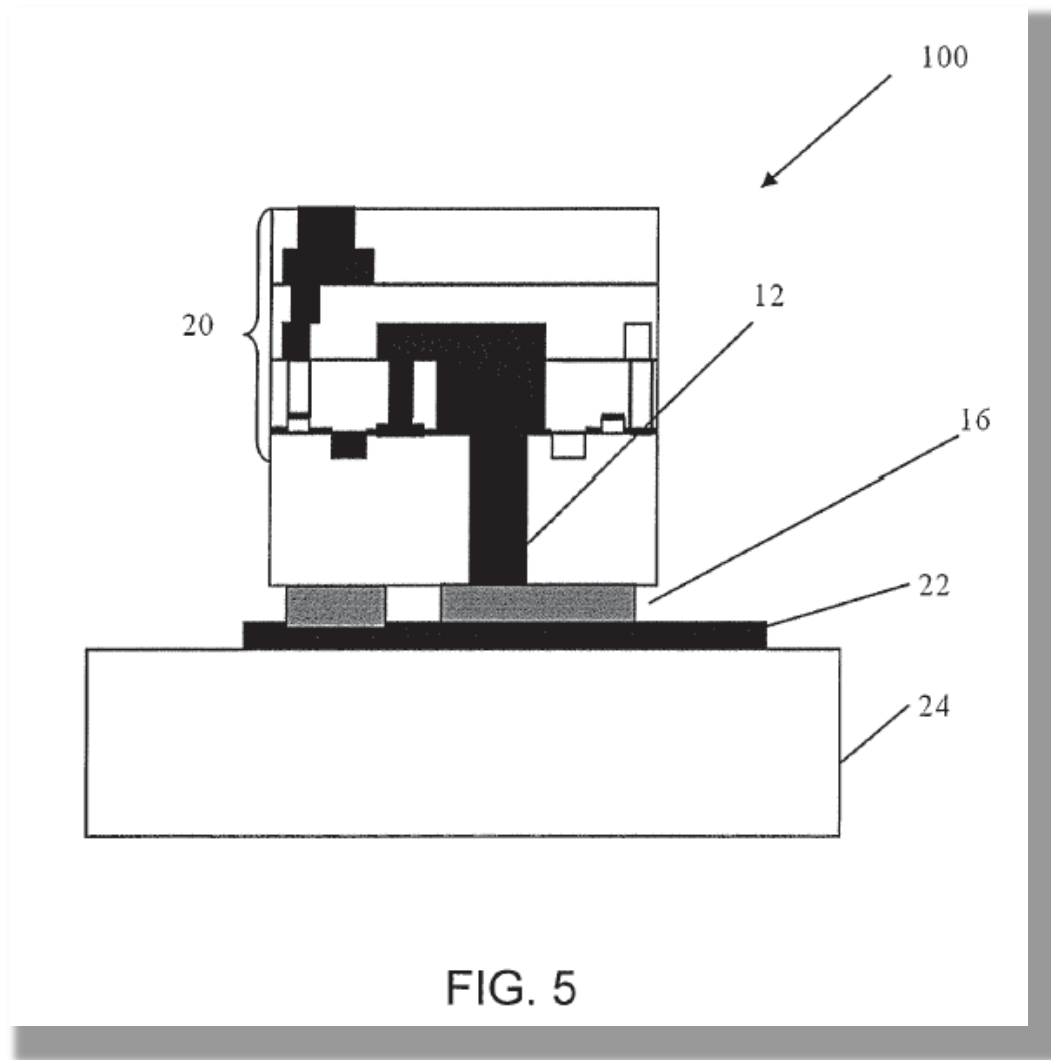


Ex. 1005, FIG. 5. *Gambino* explains that the TSV 12 shown in Figure 5 is in “mechanical and electrical communication” with both the metal grounding plane 22 and wiring layers 20, which “can include vias, wires, and a host of different active or passive devices.” *Id.*, [0030]. The metal pad 16a in Figure 5 is provided “at

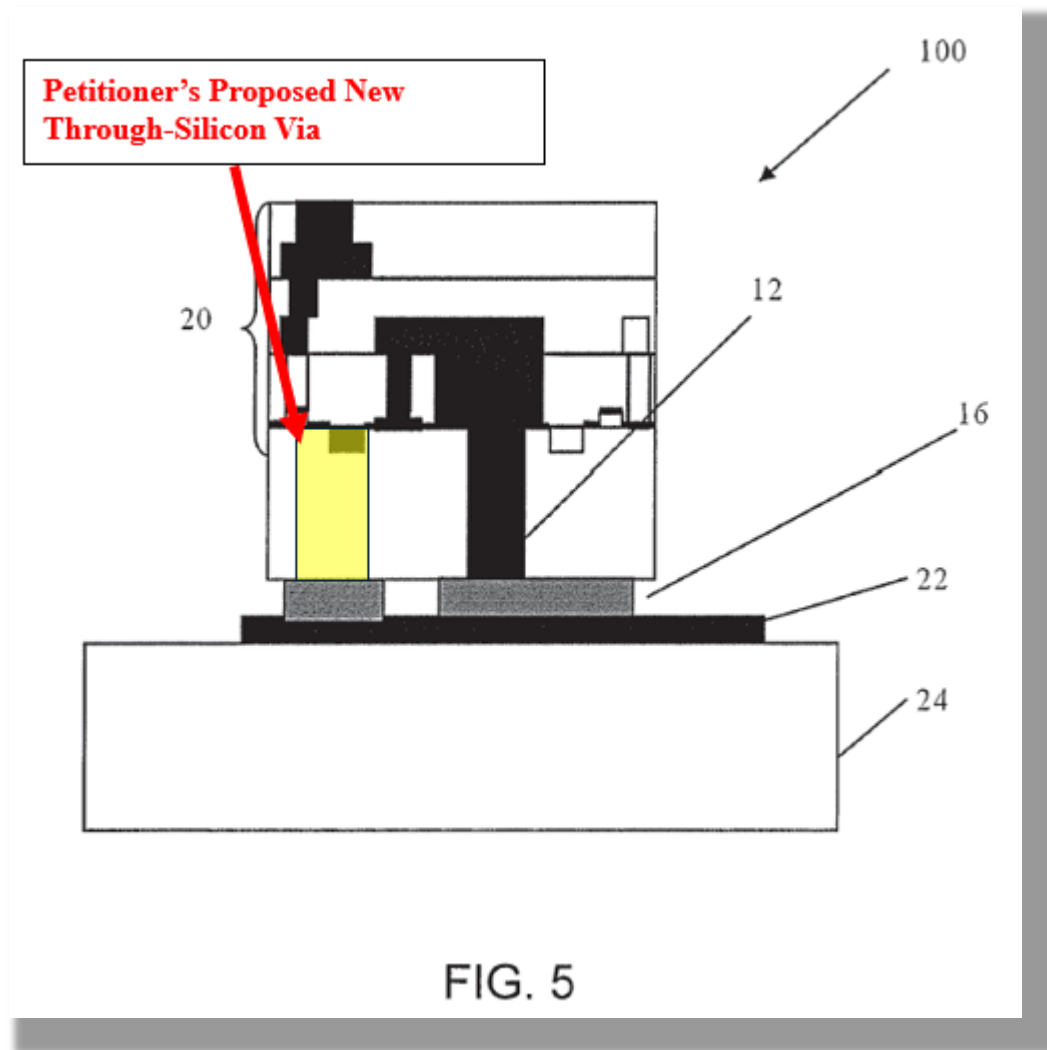
strategic locations on the dies 10 to provide mechanical support” and are “formed and placed such that the die 10 will sit flatly on the package substrate, during packaging.” *Id.* [0028]. The Petition states that “a POSA would have found it obvious to apply *Conn*’s teachings to create anchor vias in Gambino’s dummy metal pads 16a and/or main backside metal 16, to secure them to the substrate and prevent delamination during singulation.” Pet. at 60. The Petition contends that it would have been obvious to replace *Gambino*’s dummy metal pad with the via disclosed in *Conn* to arrive at the claimed invention. *Id.*

The Petition is incorrect that the combination of *Gambino* and *Conn* would result in the claimed invention, because if the dummy metal pad 16a in *Gambino* was replaced with the vias disclosed in *Conn*, the result of the combination would be a via that provides connection to the ground plane, which is directly prohibited by the Challenged Claims of the ’826 Patent. Claims 1 and 11 both require that the metal filler within the anchor via “does not provide ground connection to one or more active devices in said semiconductor substrate.” ’826 Patent, cls. 1, 11. The backside metal 16 in *Gambino*, which includes the metal pad 16a, “will act as a metalized ground plane” and is connected to the “substrate ground plane 22.” Ex.

1005, [0021], [0030]. Therefore, replacing the metal pad 16a in *Gambino* with the metal-filled via from *Conn* would provide direct connection to the ground plane.



Ex. 1005, FIG. 5. Replacing the metal pad 16a in *Gambino*'s Figure 5 (shown above without Petitioner's annotations) would also connect the devices above to the new TSV in the wire layers 20 directly to the ground plane as well, as shown below:



Ex. 1005, Fig. 5 (annotated). The Petition provides no explanation as to how a metal pad connected directly to the ground plane could be replaced with a via and not provide grounding. The Petition's only mention of this claim element is to state that "*Gambino/Conn* satisfies [1d] because corner-located dummy metal pad(s) 16a is [sic] only used for mechanical support—not used for electrical connection, which

means the anchor vias therein do not provide ground connection to active devices.” Pet. at 70. But replacing the metal pads with vias, as proposed by Petitioner’s obviousness combination, *would* provide ground connection and, thus, this combination does not result in the claimed invention. Therefore, Ground 3A fails.

2. The Remaining *Gambino/Conn/Ding* Combinations

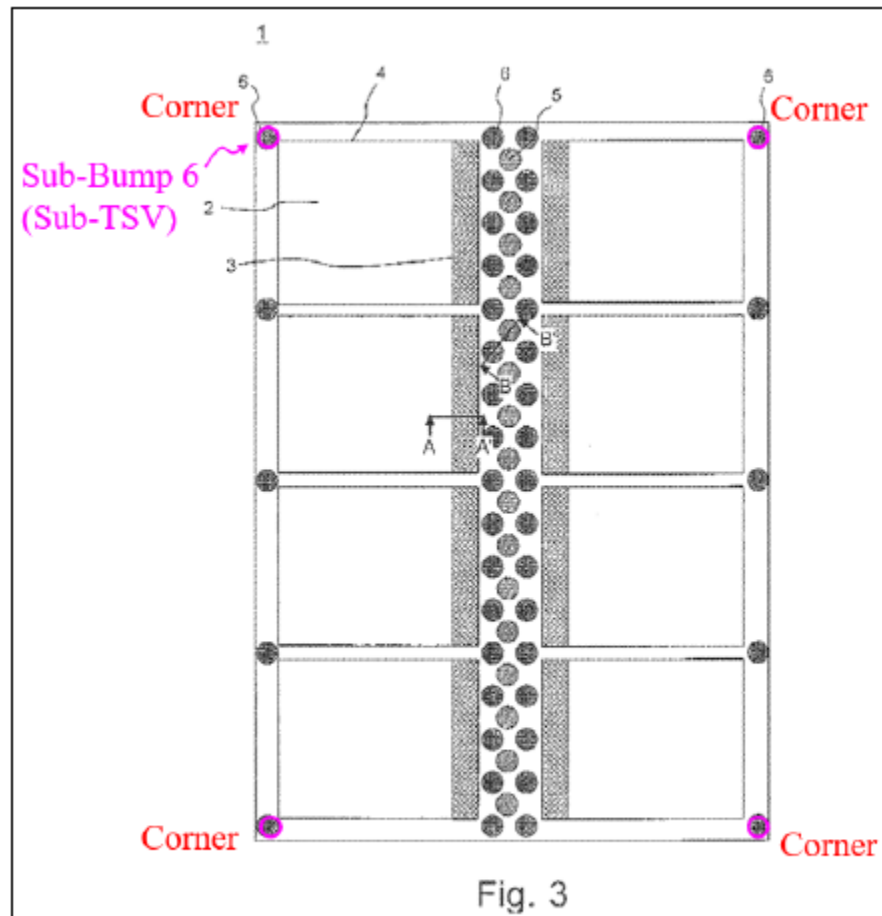
Petitioner only relies on the combination of *Gambino*, *Conn*, and *Ding* in Ground 3B to attempt to render obvious Claims 10 and 20. Because, as discussed above, the combination of *Gambino* with *Conn* fails to teach the inventions of Claims 1 and 11, the addition of *Ding* to allegedly disclose dependent claims only does not cure the deficiency in the Petition with respect to Claims 1 and 11 and, therefore, Ground 3B also fails.

D. Ground 4: The Challenged Claims Are Not Anticipated by *Torii*

1. The Petition Does Not Show That *Torii* Discloses an Anchor Via Disposed in a Corner of a Semiconductor Substrate

The Challenged Claims each require “at least one anchor via disposed in at least one corner of a semiconductor substrate.” ’826 Patent, cl. 1, 11. The Petition argues that this disclosure is met by *Torii*’s disclosure in Figure 3, showing “sub-bumps 6 are arranged in the outer circumference of a semiconductor chip 1,

including corners of the chip.” Pet. at 80 (citing Ex. 1009, [0045] (internal quotation omitted)). The Petition also annotates Figure 3 of *Torii*, as shown below:



Torii, Fig. 3.

Pet. at 81. *Torii* explains that the embodiment shown in Figure 3 is “a planar layout on the main surface of semiconductor chip 1 as a core chip which is a DRAM (Dynamic Random Access Memory) provided with memory cell regions 2 including

storage elements . . .”. Ex. 1009, [0045]. The Petition relies on the sub-bump 6 “arranged in the outer circumference of semiconductor chip 1” to show the claimed anchor vias located in the corners. Pet. at 80 (citing Ex. 1009, [0045]).

But for the actual structure of the anchor via itself, the Petition relies on *Torii*’s disclosure in Figure 46. .See Pet. at 82-85. The embodiment in Figure 46 is only used inside a memory cell, not on the corner of the DRAM chip. Ex. 1009, [0094] (“after storage-node pad 21, capacitor 22, storage-node plate 23, and first via plug 25 are provided *in memory cell region 2 . . .*”) (emphasis added). *Torii* also specifically discloses that “FIGS. 37 to 46 are cross-sectional process drawings corresponding to the B-B’ cross section of FIG. 3.” *Id.* [0093]. Critically, the B-B’ cross section of Figure 3 is nowhere near the corner of the substrate:

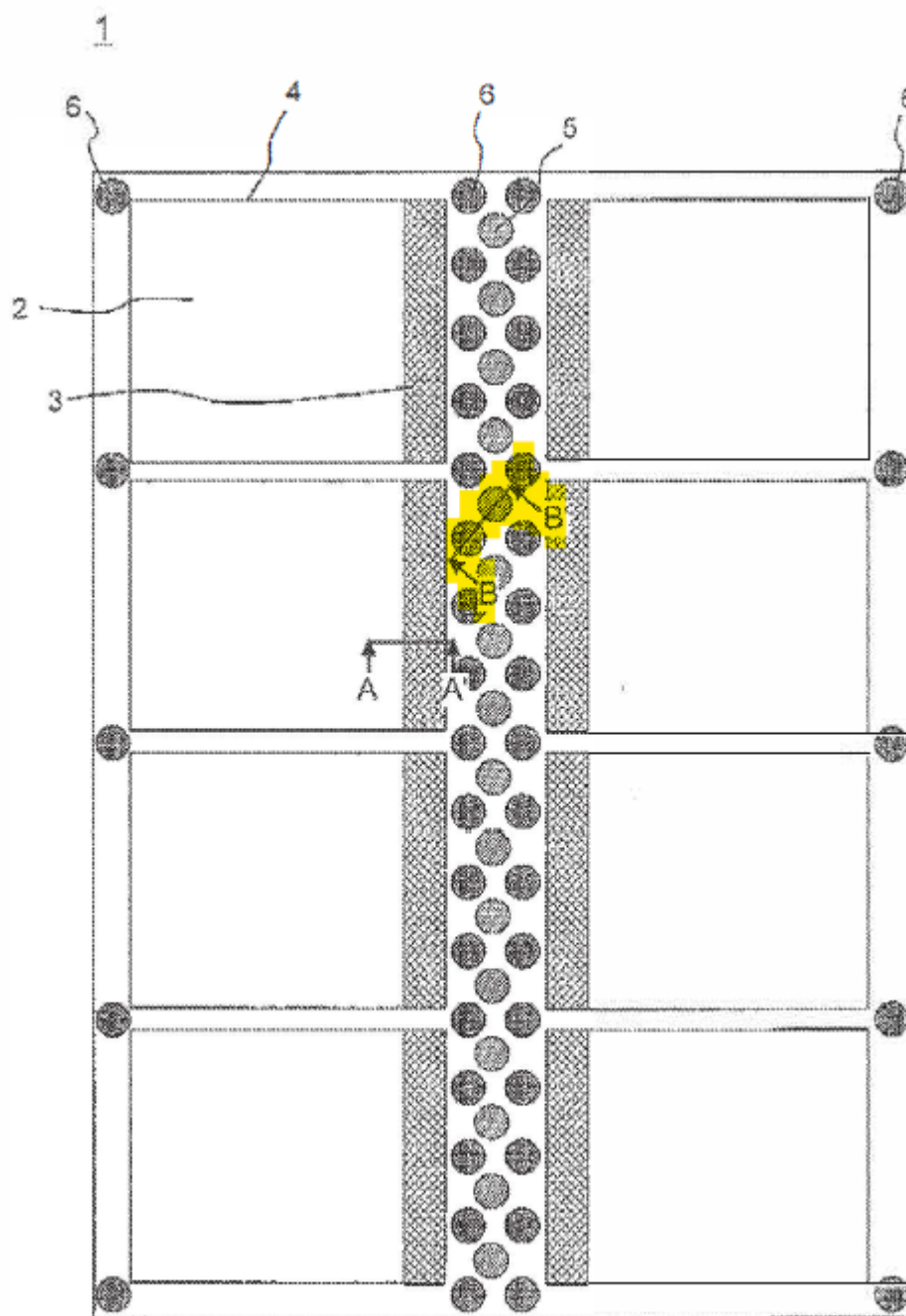


Fig. 3

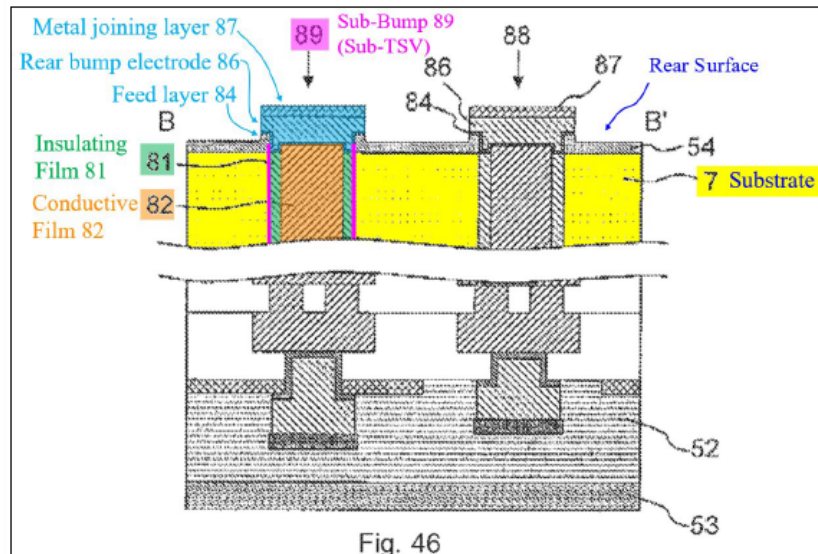
Ex. 1009, Fig. 3 (annotated). *Torii* explains that “main bumps 5 of TSVs are disposed between two rows of memory mats 4” and that “[s]ub-bumps 6 are also arranged in the outer circumference of semiconductor chip 1.” *Id.* [0045]. *Torii* never discloses that the structure disclosed and described in Figure 46 is present in the corner of the DRAM chip disclosed in Figure 3, because it is not. Petitioner’s expert also does not attempt to close this gap (even though such an attempt would be improper in an anticipation analysis), merely stating that *Torii* uses the terms sub-bump and sub-TSV interchangeably, and that the “sub bumps 6’ positions in Figure 3 represent the sub-TSVs’ positions” and that “Figure 46 shows a cross-sectional view in which a sub-bump 89 (TSV) is disposed in a substrate 7.” Ex. 1003, ¶ 177. The Petition does not even attempt to explain how the structure in Figure 46 that is shown in the middle of the DRAM chip could be replicated in the corners, and this failure dooms the anticipation analysis.

2. The Petition Does Not Show That *Torii* Discloses a Backside Metal Layer

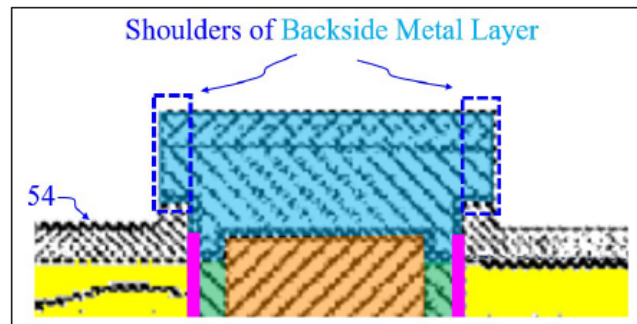
Each Challenged Claim of the ’826 Patent requires “a backside metal layer on a bottom surface of said semiconductor substrate . . .”. ’826 Patent, cl. 1, 11. *Torii* does not disclose the required backside layer, instead disclosing bumps that are

limited to the bottom of the TSV. Therefore, *Torii* does not disclose this claim element.

To show this claim element, the Petition states that *Torii*'s "second feed layer 84 alone, or together with rear bump electrode 86 and second metal joining layer 87, constitutes the claimed 'backside metal layer.'" Pet. at 84-85 (citing Ex. 1003 ¶ 180). The Petition also provides two annotated figures, which appear to illustrate its faulty position:



Torii, Fig. 46.



Torii, Fig. 46 (excerpted, zoomed).

Pet. at 85. This analysis fails for three reasons.

First, the structure identified as the backside layer by Petitioner is not “on a bottom surface of said semiconductor substrate,” because there is an additional layer in between the substrate and is structure. *Torii* discloses that “Rear-surface protective film 54 is formed on the entire rear surface (FIG. 40), and silicon oxide

film 83 is further formed on the protective film (FIG. 41).” Ex. 1009, [0100]. Figure 46 cited by Petitioner and annotated above also clearly shows the protective film 54 between the semiconductor substrate and what Petitioner claims is the backside metal layer. Petitioner’s expert claims that “the shoulder region results from a portion of the rear-surface protective film 54 formed on the sidewall of the insulating film 81” and “[t]hus, the shoulder region is not on the sub-TSV, but rather it is on the substrate surface.” Ex. 1003 ¶ 179. This is incorrect, as even Petitioner’s expert admits that the shoulder region never touches the semiconductor substrate.

Second, the tiny bump extending from the bottom of the TSV in *Torii* is not a “backside metal layer” as required by the Challenged Claims. The bumps disclosed in *Torii* are used in the semiconductor fabrication process for connecting chips to one another. Ex. 1009, [0008] (“The present inventor has found a structure in which the thin-filming of layers . . . is suppressed by providing sub-bumps along with a usual bump structure (main bumps) so that the sub-bumps come into contact with one another earlier than the main bumps at the time of joining semiconductor chips, thereby securing margins of joint between the main bumps.”). The bumps are not used for structural rigidity but rather to enable connections between semiconductor

chips. *Id.* Because the “bumps” in *Torii* are so small, an anchor via as claimed in the ’826 Patent is not necessary to secure the semiconductor substrate to them.

Third, there is no disclosure in *Torii* or discussion in the Petition that the feed layer 84 as disclosed in the fifth embodiment of *Torii* is “metal.” Petitioner relies on either the “second feed layer 84 alone” or the feed layer in combination with “rear bump electrode 86 and second metal joining layer 87” for this claim element. Pet. at 84-85. But the Petition relies on other disclosures in other embodiments for the structure of layer 84, citing to paragraph 67 (which discusses Figure 17 and describes “second feed layer 60”). *Id.* Neither the Petition nor Petitioner’s expert makes any attempt to connect this other feed layer in other embodiments to the “second feed layer 84” from the Fifth embodiment that is relied upon in the Petition. *See* Ex. 1003 ¶ 181. Moreover, *Torii* specifically notes that the layer 87 is a “metal joining layer” and that it and the rear bump electrode 86 are “formed by electrolytic plating,” but it is silent as to the composition of the feed layer 84. Ex. 1009, [0100]. The Petition’s failure to show that the element specifically relied upon to show the “backside metal layer” is actually metal is fatal to the anticipation analysis.

For these reasons, the Petition does not show that *Torii* anticipates “a backside metal layer on a bottom surface of said semiconductor substrate . . .”. ’826 Patent, cls. 1, 11.

3. The Petition Does Not Show That *Torii* Discloses Metal Filler That Does Not Provide Ground Connection to Active Devices

The Petition improperly mixes embodiments in *Torii* to show this claim element, which is improper for an anticipation analysis. The Challenged Claims of the ’826 Patent each require that the metal filler in the anchor vias is used *solely* for anchoring, and “does not provide ground connection to one or more active devices in said semiconductor substrate.” ’826 Patent, cls. 1, 11. The Petition states that “[t]he sub-TSV is a dummy . . . normally not used as a current pathway.” Pet. at 86 (citations omitted). The Petition places a period at the end of this quote, but fails to note that the quote disingenuously removed the second half of the sentence which explicitly states that the sub-TSV can be used to conduct current, including static electricity, which of course is discharged to ground. The full, unedited quote is:

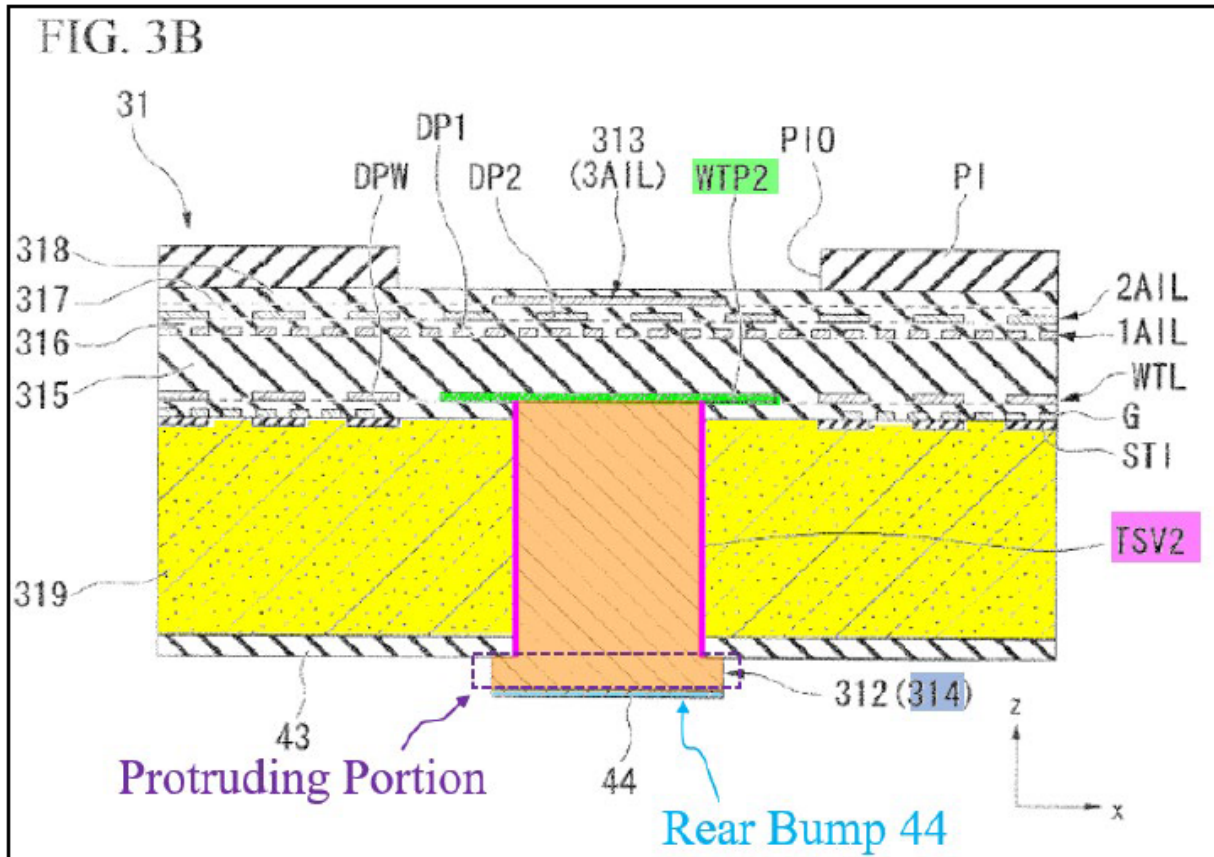
The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

Ex. 1009, [0048]. The requirement of the Challenged Claims that the anchor via not be used to provide ground connection to one or more active devices is directly contradicted by this disclosure in *Torii*, stating that the sub-TSV's can, in fact, be used as current pathways. For this additional reason, the Petition's anticipation analysis fails.

E. Ground 5: *Ide* Does Not Anticipate the Challenged Claims

1. The Petition Does Not Show That *Ide* Discloses a Backside Metal Layer on a Bottom Surface of a Semiconductor Substrate

Each Challenged Claim of the '826 Patent requires “a backside metal layer on a bottom surface of said semiconductor substrate . . .”. '826 Patent, cls. 1, 11. *Ide* does not disclose the required backside layer; instead, like *Torii* above, discloses bumps that are limited to the bottom of the TSV. Therefore, *Ide* does not disclose this claim element. The Petition annotates *Ide*'s Figure 3B as below, with “Rear Bump 44” allegedly satisfying the claimed “backside metal layer”:



Ide, Fig. 3B.

Pet. at 94-95. As with *Torii*, the Petition notes in a footnote that there is an “intervening rear insulating layer 43 and rear bump electrode 312” between the copper fill (annotated in orange) and the rear bump 44 (annotated in blue). Pet. at 94 n.15. This insulating layer 43 in between the substrate 319 and the rear bump 44 that Petitioner claims is the “backside metal layer” therefore means that the backside

metal layer is not “on a bottom surface of said semiconductor substrate” and, therefore, *Ide* does not anticipate Claims 1 or 11.

Rear Bump 44 in *Ide* is also not the claimed “backside metal layer” because it is not a layer at all, just a tiny bump of metal. The rear bump disclosed in *Ide* is “connected to wiring through electrode TSV1” (Ex. 1010, [0120]) and is not a “layer” but merely an electroplated connector which is designed to connect memory chips to an interface chip (*id.*, [0010]). The bumps are not used to provide structural rigidity, and therefore an anchor via as claimed in the ’826 Patent is not necessary to secure the semiconductor substrate to them.

VII. THE PETITION SHOULD BE DENIED IN THE DISCRETION OF THE DIRECTOR UNDER 35 U.S.C. § 314(A)

Based on Petitioner’s reasons regarding § 314(a), the Board should exercise its discretion to deny this Petition. As shown above, the Petition does not present a compelling unpatentability challenge.

The circumstances of the parallel District Court Litigation, *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) necessitate denial of the Petition under the Board’s precedent, as every factor considered in relation to efficiency, fairness, and the merits supports denial. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 6 (P.T.A.B. Mar. 20, 2020)

(precedential) (considering (a) “whether the petitioner and the defendant in the parallel proceeding are the same party”; (b) “overlap between issues raised in the petition and in the parallel proceeding” (c) “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision”; (d) “investment in the parallel proceeding by the court and the parties”; (e) “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted”; and (f) “other circumstances that impact the Board’s exercise of discretion, including the merits.”).

As set forth below, these factors collectively demonstrate that efficiency and integrity of the AIA are best served by denying review. First, the Petitioner is the Defendant in the parallel proceeding. *See infra* Section VII.A. Second, the asserted claims in the District Court Litigation are all at issue in the Petition. *See infra* Section VII.B. Third, trial in the District Court Litigation is set for January 5, 2026, which is three months before projected statutory deadline for a Final Written Decision of this Petition on March 30, 2026. *See infra* Section VII.C. Fourth, the parties (and Patent Owner in particular) have invested significant resources in developing legal and factual issues of validity and infringement in the District Court Litigation and will have invested substantially more resources before any decision on this Petition.

See infra Section VII.D. Fifth, the Court has already denied a stay pending this Petition. *See infra* Section VII.E. Finally, no other factors favor institution. *See infra* Section VII.F.

Accordingly, the Board should exercise its discretion under § 314(a) and deny the Petition because institution of this proceeding would not be consistent with the objective of the AIA to “provide an effective and efficient alternative to district court litigation.” *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8, at 20 (P.T.A.B. Sept. 12, 2018) (quoting *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, at 16–17 (P.T.A.B. Sept. 6, 2017) (precedential)).

**A. The Parallel District Court Litigation and the Petition
Involve the Same Parties**

As Petitioner notes, there exists a parallel District Court Litigation between the same parties regarding the same subject patent (the '826 Patent). Pet. at 74. Petitioner is a party to the District Court Litigation captioned as *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.). Accordingly, this factor weighs in favor of discretionary denial.

B. The District Court Litigation Involves Substantially the Same Claims

All of the asserted claims of the '826 Patent in the District Court Litigation are at issue in this Petition. “In at least these ways, the parallel proceedings would duplicate effort. This is an inefficient use of Board, party, and judicial resources and raises the possibility of conflicting decisions.” *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020-00122, Paper 15 at 10 (P.T.A.B. May 15, 2020). Accordingly, this fact weighs in favor of discretionary denial.

C. Proximity of the District Court’s Trial Date

The proximity of the District Court Litigation’s trial date to the Board’s projected statutory deadline for a Final Written Decision strongly weighs in favor of discretionary denial.

The parties’ trial is scheduled for January 5, 2026. Ex. 2001 (Docket Control Order, Dkt. 38, *Harbor Island Dynamic LLC v. Samsung Elecs. Co.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)). Pursuant to 35 U.S.C. §§ 314(b)(1) and 316(a)(11), the projected statutory deadline for a Final Written Decision of this

Petition is March 30, 2026.¹ As the District Court’s trial will be three months before the projected statutory deadline, this factor weighs strongly in favor of denying institution. *See Supercell Oy v. Gree, Inc.*, IPR2020-00513, Paper 11 at 10-12 (P.T.A.B. June 24, 2020) (denying institution where the jury trial was scheduled to conclude approximately ten months before the statutory deadline); *Edward LifeSciences Corp. v. Evalve, Inc.*, IPR2019-01479, Paper 7, at 6-13 (P.T.A.B. Feb. 26, 2020) (denying institution where jury trial would conclude more than nine months before a final decision would be due); *Samsung Elecs. Am., Inc. v. Uniloc 2017 LLC*, IPR2019-01218, Paper 7, at 7-10 (P.T.A.B. Jan. 7, 2020) (denying institution where jury selection was scheduled for approximately six months before trial in the Board proceeding would conclude); *Next Caller Inc. v. TrustID, Inc.*, IPR2019-00961, -00962, Paper 10, at 8-16 (P.T.A.B. Oct. 16, 2019) (denying

¹ The statutory deadline for institution is March 30, 2025, “three months after receiving a preliminary response to the petition under section 313.” *See* 35 U.S.C. § 314(b)(1). If instituted, the statutory deadline for Final Written Decision is March 30, 2026, “not later than 1 year after the date on which the Director notices the institution of a review.”

institution where trial was scheduled to conclude “several months,” before a final decision would be due); *Cisco Sys., Inc.*, IPR2020-00122, Paper 15 at 8 (“Because the trial date is substantially earlier than the projected statutory deadline for the Board’s final decision, this factor weighs in favor of discretionary denial.”).

Petitioner does not contest that the proximity of the trial favors denial of institution. Thus, this factor also weighs in favor of discretionary denial.

D. Significant Investment and Petitioner’s Delay in Filing the Petition

The parties’ investment in the parallel proceeding weighs in favor of discretionary denial. In the District Court Litigation, the Court has already entered a Docket Control Order (Dkt. 38), Discovery Order (Dkt. 39), and Protective Order (Dkt. 44). Discovery is also well under way. The parties have already exchanged infringement contentions pursuant to P.R. 3-1 and invalidity contentions pursuant to P.R. 3-3. Ex. 2001 (Docket Control Order). A trial date is also set for January 5, 2026. *Id.* Thus, the parties’ and Court’s substantial investment in this proceeding weighs in favor of denial of institution under this factor.

E. No Stay of the Parallel District Court Litigation

There is no stay of the parallel District Court Litigation and, in fact, a motion for a stay by Petitioner has already been denied. *See* Dkt. 62, *Harbor Island*

Dynamic, LLC v. Samsung Elecs. Co., No. 2:24-cv-00140-JRG-RSP (E.D. Tex. December 19, 2024). Ex. 2002. Even if the Petition were instituted and Petitioner filed another motion to stay the District Court Litigation, prejudice, tactical disadvantage to Patent Owner, the late stage of the litigation, and the lack of potential simplification would weigh strongly against such a motion. *See Lennon Image Techs., LLC v. Macy's Retail Holdings, Inc.*, 2:13-CV-00235-JRG, 2014 WL 4652117, at *1 (E.D. Tex. Sept. 18, 2014).

Moreover, a stay would not decrease the burden on the Court and the parties since any instituted IPR would not cover all of the obviousness challenges that Petitioner has raised in the District Court Litigation, and do not include Petitioner's challenges under § 101, § 102, or § 112. *See generally* Ex. 2003 (Invalidity Contentions), at 46, 53-54. *Intell. Ventures II LLC v. FedEx Corp.*, No. 2:16-cv-00980-JRG, Dkt. 141 at 3-4 (E.D. Tex. Oct. 24, 2017) (“[T]he instituted IPRs only cover a narrow slice of the invalidity arguments Defendants have raised in this case. For example, Defendants have argued that the ’715 Patent is invalid under § 102 with respect to at least eight references . . . under § 103 with respect to at least twenty-six combinations . . . under § 112 [], and under § 101.”).

Accordingly, it would be unlikely for the Court to hold that a stay would streamline the litigation and this factor supports denial of institution.

F. Other Factors Favor Discretionary Denial

Petitioner does not present a strong case on the merits, further supporting denial of institution. *See supra* Section VI. Petitioner also does not identify any other factors which weigh against discretionary denial. Pet. at 102-103.

Thus, when viewing the factors together, the Petition should be denied in the Director's discretion under 35 U.S.C. § 314(a).

VIII. THE BOARD SHOULD REJECT ANY LATE SOTERA STIPULATION

Petitioner has not made a *Sotera*-style stipulation that “if IPR is instituted, [Petitioner] will not pursue in the District Court Litigation any ground raised or that could have been reasonably raised in an IPR” in its Petition, which weighs further in favor of discretionarily denying institution. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12, 13-14 (P.T.A.B. Dec. 1, 2020) (designated Dec. 17, 2020).

The Board should not accept any late *Sotera* stipulation after this Patent Owner Preliminary Response. Petitioner has known about the related District Court Litigation since Patent Owner filed a Complaint asserting infringement of the '826

Patent against Petitioner (February 27, 2024) over six months before the Petition (Sept. 20, 2024) and has had a docket control order for the District Court Litigation, anticipating a trial date for January 5, 2026. Ex. 2001 (Docket Control Order). Any withholding of the *Sotera* stipulation in its Petition is gamesmanship and prejudicial to Patent Owner in this proceeding and is inconsistent with 37 C.F.R. § 42.1(b)'s mandate to "secure the just, speedy, and inexpensive resolution of every proceeding."

Both the Board and the Director are abundantly clear that Petitioner cannot wait until after the Board renders its Institution Decision to address the issue of *Fintiv*, the Board's discretionary authority, and to submit a *Sotera* stipulation. *NXP USA, Inc. v Impinj, Inc.*, IPR2021-01556, Paper 12, 5-6 (P.T.A.B. Aug. 25, 2022); *see also id.*, IPR2021-01556, Paper 13, 3-4 (P.T.A.B. Sept. 7, 2022) (the Director finding "that the Board correctly determined that a stipulation, offered by a petitioner for the first time after a decision denying institution, is not a proper basis for granting rehearing of the decision on institution;" "[p]ermitting a petitioner to wait and see if the Board denies institution under *Fintiv*, and then offer such a stipulation for the first time on rehearing, frustrates these goals [of avoiding conflicting decisions] and would open the door to gamesmanship;" "*the only appropriate time for a petitioner*

to offer a stipulation related to the Fintiv factor 4 analysis is prior to the Board's decision of whether to institute review.") (emphasis added).

IX. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution of the Petition in its entirety.

Respectfully submitted,

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IPR2024-01405
PATENT NO. 9,245,826

CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S PRELIMINARY RESPONSE specified in 37 C.F.R. § 42.24 has 9,598 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

Respectfully submitted,

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