

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01405
Patent 9,245,826 B2

Before WILLIAM V. SAINDON, GREGGI. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively “Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1–20 (“the challenged claims”) of U.S. Patent No. 9,245,826 B2 (“the ’826 patent,” Ex. 1001). Paper 1 (“Pet.”). Petitioner filed a Declaration of Dr. Scott E. Thompson, Ph.D., in support of the Petition. Ex. 1003. Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(a). *See* 37 C.F.R. § 42.4(a) (2023) (“The Board institutes the trial on behalf of the Director.”). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Considering the Petition, the Preliminary Response, as well as all supporting evidence, we conclude that the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail in its challenge of at least one claim of the ’826 patent as unpatentable. Pursuant to 35 U.S.C. § 314, we hereby institute an *inter partes* review of all challenged claims of the ’826 patent on all grounds stated in the Petition.

Our factual findings, claim construction, and legal conclusions at this stage of the proceeding are based on the evidentiary record developed thus far. This decision to institute trial is not a final decision as to the

unpatentability of the claims for which *inter partes* review is instituted. Our final decision will be based on the full record developed during trial.

A. Related Matters

The parties identify the following proceeding as a related matter: *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) (“District Court Litigation”). Pet. 104; Paper 6 (Patent Owner’s Mandatory Notices), 2.

B. Real Parties in Interest

Petitioner identifies “Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.” as the real parties-in-interest. Pet. 104. Patent Owner identifies “Harbor Island Dynamic, LLC” as the real parties-in-interest. Paper 6.

C. The ’826 patent (Ex. 1001)

The ’826 patent relates “to anchor vias for improved backside metal adhesion to a semiconductor substrate.” Ex. 1001, 1:42–44. The disclosure states “miniaturization and increased density in semiconductor substrates has typically relied on a backside metal layer attached to the substrate.” *Id.* at 1:15–17. A conventional method of adhering a backside metal layer to a substrate includes bonding via adhesive which can result in reduction of fabrication yields due to the backside metal layer peeling away from the semiconductor substrate. *Id.* at 1:24–27, 1:36–38.

Figure 1A is reproduced below:

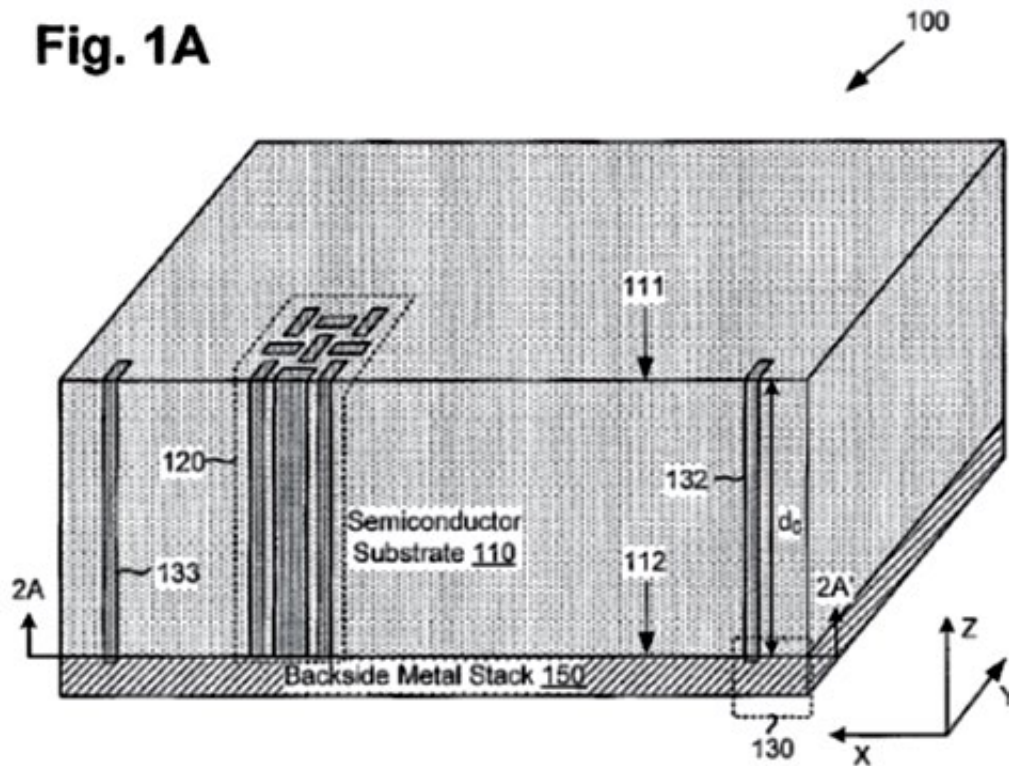


Figure 1A is a “cross-section of a semiconductor structure having anchor vias for improved backside metal adhesion.” Ex. 1001, 1:50–52. The semiconductor structure 100 includes a semiconductor substrate 110 having a top surface 111 (“front side”), polished bottom surface 112 (“backside”), backside metal stack 150, a group 120 of through silicon vias (TSVs) formed in a core region, and anchor vias 132, 133 formed in a peripheral region. *Id.* at 2:57–66, 3:2–5. Metal filler of the TSV group 120 provides ground connection to devices in the core region. *Id.* at 3:5–7. By contrast, metal filler within the anchor vias 132, 133 does not provide ground connections but rather physical anchor points between semiconductor substrate 110 and the backside metal stack 150. *Id.* at 3:12–17.

Figure 1B is reproduced below:

Fig. 1B

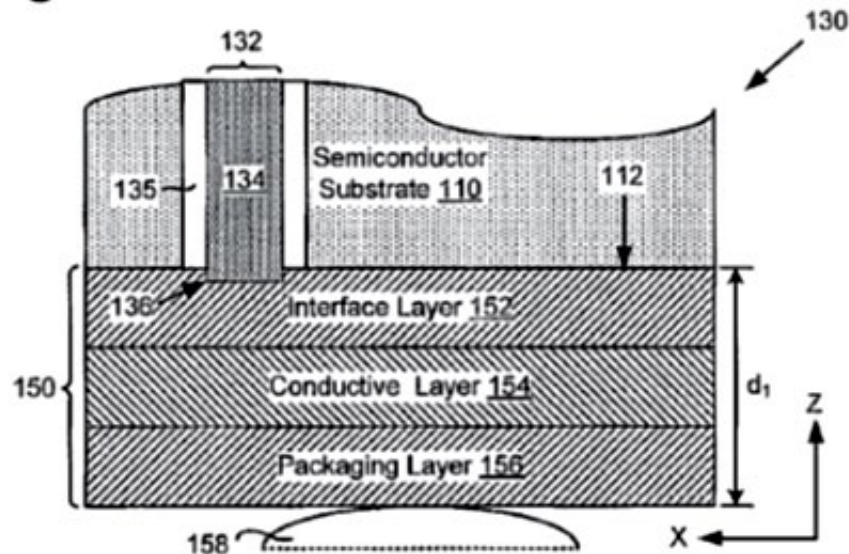


Figure 1B is “a magnified cross-section of a portion of an anchor via for improved backside metal adhesion.” Ex. 1001, 1:54–56. The magnified view 130 shows anchor via 132, backside metal stack 150 formed on bottom side 112 of semiconductor substrate 110, insulating silicon dioxide layer 135 on the sidewalls of anchor via 132, and metal filler 134 in anchor via 132. *Id.* at 3:36–43. The metal stack 150 includes an interface titanium layer 152, a nickel conduction layer 154, and a gold packaging layer 156 adjoining a printed computer board (PCB) contact 158 of another device. *Id.* at 3:49–59. A portion 136 of metal filler 134 protrudes past bottom side 112 of semiconductor substrate 110 to provide additional contact and, thereby, a stronger physical, metal-on-metal bond between the metal filler 134 and interface layer 152. *Id.* at 3:43–48.

D. Illustrative Claim

Claims 1 and 10 are independent claims. Claim 1 is reproduced, below, with Petitioner’s limitation identifiers in brackets (Pet. 1):

1. [1pre] A structure comprising:

[1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;

[1b] a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

[1c] a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

[1d] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

Ex. 1001, 7:58–6:3.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–20 would have been unpatentable on the following grounds (Pet. 23):

Ground	Claim(s) Challenged	35 U.S.C. § ¹	References/Basis
1	1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	102	Conn ²
2A	1, 2, 4–7, 9, 11, 12, 14–17, 19	103(a)	Conn
2B	8, 18	103(a)	Conn in view of AAPA
3A	1, 2, 4–7, 11, 12, 14–17	103(a)	Gambino ³ in view of Conn

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103. Because the ’826 patent claims priority to an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of §§ 102, 103 applies.

² U.S. Patent Application Publication No. 2009/0079056 to Conn (Ex. 1004).

³ U.S. Patent Application Publication No. 2014/0138844 to Gambino et al. (Ex. 1005).

Ground	Claim(s) Challenged	35 U.S.C. § ¹	References/Basis
3B	10, 20	103(a)	Gambino in view of Conn and Ding ⁴
4	1, 8–11, 18–20	102	Torii
5	1–3, 9, 11–13, 19	102	Ide

II. ANALYSIS

A. Overview

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). At this stage of the proceeding, Petitioner bears the burden of demonstrating a reasonable likelihood that it would prevail with respect to at least one challenged claim for a petition to be granted. 35 U.S.C. § 314(a).

To establish anticipation under 35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyConn, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be “considered together with the knowledge

⁴ U.S. Patent Application Publication No. 2012/0104546 to Ding et al. (Ex. 1008).

of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable as obvious “if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains.” 35 U.S.C. § 103; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained in *KSR International Co. v. Teleflex Inc.* that

[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary

⁵ No evidence of secondary considerations has been presented at this stage of the proceeding.

skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original)).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art “would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems” and “[a]dditional relevant work experience can compensate for less education, and *vice versa*.” Pet. 23 (citing Ex. 1003 ¶¶ 73–74).

Patent Owner agrees with Petitioner’s proposed level of ordinary skill in the art for the purposes of the Preliminary Response. Prelim. Resp. 16–17.

For the purposes of this Decision, we apply Petitioner’s proffered level of skill in the art because it appears consistent with the problems addressed in the ’826 patent and the prior art.

C. Claim Construction

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b) (2023). Accordingly, we construe each challenged claim of the ’826 patent to generally be “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

If the specification “reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is “when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Uship Intellectual Props., LLC v. United States*, 714 F.3d 1311, 1313 (Fed. Cir. 2013) (quoting *Thornerv. Sony Comput. Ent. Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Petitioner does not present a claim construction aside from asserting “[i]ndependent method claim 11 does not require the steps therein to be performed in their recited order.” Pet. 20. Patent Owner does not present a claim construction. Prelim. Resp. 17.

We determine that no express construction of any claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”)(quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

The parties are free to address the construction of any claim term in subsequent authorized briefing during trial. If either party chooses to do so, they should do so in a separately delineated portion of the brief labelled accordingly.

*D. Ground 1: Alleged Anticipation of
Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 by Conn*

Petitioner contends that claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 are anticipated by Conn. Pet. 24–45. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003.

We begin with a brief summary of Conn. We then address the parties’ respective contentions.

1. Conn (Ex. 1004)

Conn is titled “Large Substrate Structural Vias.” Ex. 1004, code (54). Conn “relates to a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.” *Id.* ¶ 3.

Addressing the background of the invention, Conn states computing devices can require a large amount of power that largely increases the temperature of the devices. Ex. 1004 ¶ 5. These temperature changes cause

fatigue of the electronic “package” structure, e.g., between the layers of a package laminate or between a packaged part and a PCB. *Id.*

In the invention, an electronic package includes a carrier substrate having first and second surfaces and a plurality of anchor vias having a via material extending from the first surface toward the second surface. Ex. 1004 ¶ 11. The anchor vias have plural attachments along the length and the width of the first conducting layer to secure the first conducting layer to the carrier substrate. *Id.*

Figure 1 is reproduced below:

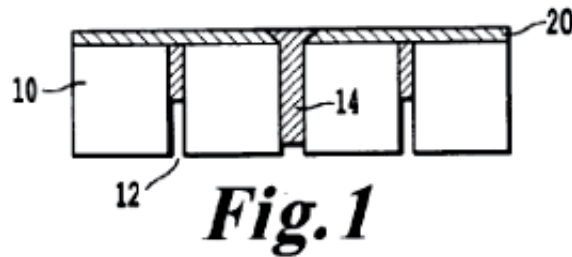


Figure 1 is a diagram depicting a side view of an electronic package. Ex. 1004 ¶ 17. The package includes a carrier substrate 10, a conducting layer 20 formed on a first main surface of the carrier substrate 10, and passive components (e.g., capacitors, resistors, and inductors) within the carrier substrate 10. *Id.* ¶ 26. The conducting layer 20 is connected to a via conductor 14 formed in a via 12 and thereby providing an “anchor via” into the carrier substrate. *Id.* ¶ 28. The anchor via acts as a “rivet” whereby the conducting layer 20 maintains its structure under thermal stress. *Id.* The plural vias 12 can be “through-vias” or not span to the opposite surface of the carrier substrate 10. *Id.* The via conductor 14 enters at least partially into the via 12, but not necessarily all the way through the via 12, to form an

array pattern of rivets securing the conducting layer 20 to the carrier substrate 10. *Id.* ¶¶ 29, 35; Fig. 2.

2. Claim 1

Petitioner provides a limitation-by-limitation analysis of claim 1, mapping each claim limitation to Conn. Pet. 28–38.

Patent Owner argues this challenge fails to show Conn teaches an anchor via disposed at the corner of the carrier substrate 10. Prelim. Resp. 20–28. Patent Owner also argues the challenge fails to show Conn teaches metal filler with a protrusion that does not provide a ground connection to active devices. *Id.* at 29–31.

a) “[1pre] A structure comprising:”

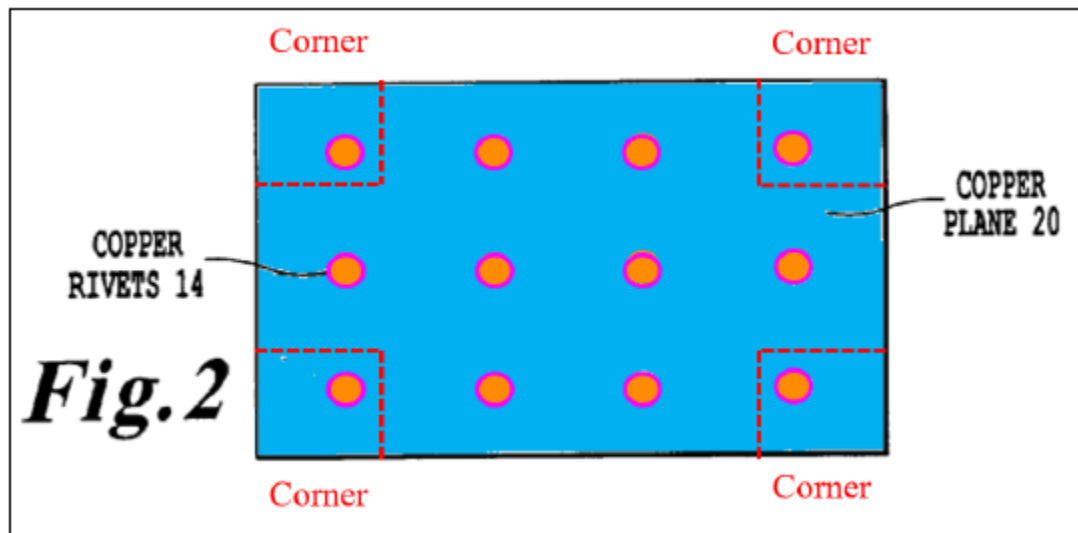
Petitioner contends Conn discloses “an electronic package structure” that “includes ‘a carrier substrate 10 having at least a conducting layer 20 formed on a first main surface of the carrier substrate 10.’” Pet. 28 (citing Ex. 1003 ¶ 82; Ex. 1004 ¶¶ 17, 26, 29, Fig. 1).

Patent Owner does not address the preamble of claim 1 in the Preliminary Response. *See* Prelim. Resp. 20–31.

We have reviewed Petitioner’s contentions and evidence and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Conn discloses the subject matter of the preamble. Consequently, we need not address whether the preamble of claim 1 is limiting.

b) “[1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;”

Petitioner provides the following annotated version of Figure 2 of Conn:



Pet. 29. Figure 2 “depict[s] a top view of [an] electronic package according to an embodiment of the invention.” Ex. 1004 ¶ 18. Petitioner annotates Figure 2 by highlighting copper plane 20 blue, copper rivets 14 orange with a red circular border, four dashed rectangles in red, red text reading “Corner” outside each corner of rectangular copper plane 20. Pet. 29.

Petitioner contends Conn discloses carrier substrate 10 comprising “a plurality of anchor vias (e.g., via conductor 14).” Pet. 28 (citing Ex. 1004 ¶ 29). Petitioner further contends that Conn’s “Figure 2 shows the plurality of anchor vias . . . are ‘distributed relative to the conducting layer 20 in a pattern . . . cover[ing] the entire surface of conducting layer 20, such that [] anchor vias are disposed at the corners of conducting layer 20.” *Id.* at 28–29 (citing Ex. 1003 ¶ 83; Ex. 1004 ¶ 35, Fig. 2). Petitioner concedes that Figure 2 “does not show carrier substrate 10, but Conn discloses that conducting layer 20 can cover more than ‘90% of an entirety of the surface area of the carrier substrate,’ even approaching ‘100%.’” *Id.* at 29 (citing Ex. 1003 ¶ 84; Ex. 1004 ¶ 31). According to Petitioner, because of this disclosed coverage of the conducting layer, “the corners of conducting layer 20 are

also the corners of carrier substrate 10” and “the anchor vias located at the corners of conducting layer 20 are also located at the corners of carrier substrate 10.” *Id.* at 29–30 (citing Ex. 1003 ¶ 84).

Patent Owner argues that Petitioner’s annotated version of Conn’s Figure 2 “artificially draws the ‘Corner’ of Conn’s Copper Plane 20 large enough to enclose one copper rivet in each corner” but that there is no explicit disclosure in Conn to support this interpretation. Prelim. Resp. 21. According to Patent Owner, paragraph 29 of Conn “states only that the carrier substrate in Figure 1 includes ‘a plurality of anchor vias (e.g., via conductor 14).’” *Id.* Patent Owner further argues that Figure 1 of Conn “only discloses one anchor via 14, and it is located in the middle of the substrate, rather than the corner.” *Id.* at 22 (citing Pet. 31 (Petitioner’s annotated Figure 1)). Patent Owner next argues that Petitioner hasn’t shown that Conn’s anchor vias are “disposed in at least one corner ‘of a semiconductor substrate.’” *Id.* at 24. According to Patent Owner, “Petitioner merely selects an embodiment where the copper plane covers 90% of the carrier substrate, then assumes without support that the carrier substrate is arranged in its annotated version of Figure 2.” *Id.* at 25.

For the following reasons, Patent Owner’s arguments are unavailing based on the present record.

Figure 2A of the ’826 patent is reproduced below:

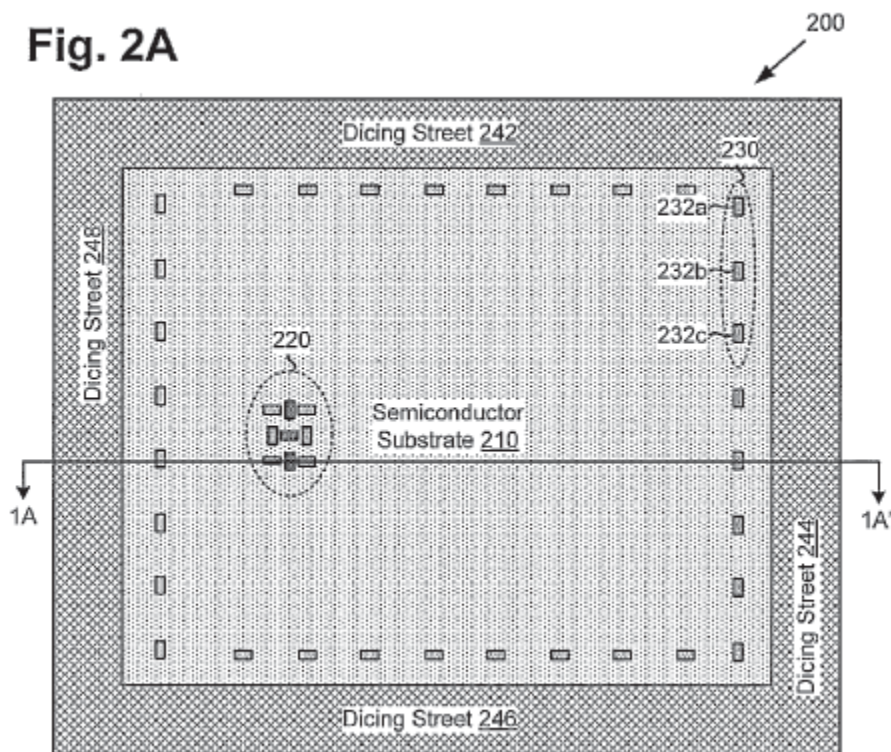


Figure 2A is “a backside view of a semiconductor structure having anchor vias.” Ex. 1001, 1:58–59. The ’826 patent describes that “several anchor vias [232a, 232b, 232c] are shown along the edges and in the *corners* of semiconductor substrate [210].” *Id.* at 4:21–23 (emphasis added). This description of “corners” in the ’826 patent supports Petitioner’s position and Dr. Thompson’s testimony that Figure 2 of Conn shows anchor vias in the “corners” of copper plane 20. Pet. 29; Ex. 1003 ¶ 83.

Patent Owner’s argument that Figure 1 of Conn shows anchor vias in the middle, not in the corners, and that Petitioner has not shown that the anchor vias are disposed in the corner vias of the substrate are attorney argument. We acknowledge Patent Owner’s reference to Figure 1 of Conn, showing 3 vias and the middle via is the only one with a rivet. Ex. 1004, Fig. 1. Conn’s Figure 3, like Figure 2, shows 4 vias and indicates that

copper rivets 14 are in the left most edge, providing a reasonable basis for Petitioner’s contention that anchors vias are in the corners. *Id.* at Figs. 3, 4. Petitioner’s argument that Conn discloses anchor vias in the corner is also supported by Dr. Thompson’s testimony concerning how an ordinarily skilled artisan would understand Conn’s disclosure. Ex. 1003 ¶¶ 83–84. Based on the current evidentiary record, we preliminarily find that Dr. Thompson’s testimony that Conn discloses anchor vias in the corners is reasonably supported by the disclosure of Conn.

We have reviewed Petitioner’s contentions and evidence in light of Patent Owner’s arguments and find that, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Conn discloses this limitation.

c) “[1b] a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;”

Petitioner contends that Conn’s “via conductors in the anchor vias form rivet structures (i.e., ‘copper rivets 14’ in Figure 2) that protrude from a side of the substrate surface.” Pet. 30 (citing Ex. 1003 ¶¶ 85–90). According to Petitioner, Conn’s via conductor 14 corresponds to the recited metal filler because it “may be formed of copper, aluminum, gold, silver or other conductor.” *Id.* (citing Ex. 1004 ¶¶ 28, 29, 33).

Petitioner next contends that Conn’s via conductors 14 form rivets “that are mechanically ‘connected to’ and ‘in contact with’ conducting layer 20.” Pet. 31 (citing Ex. 1004 ¶¶ 28–30, 38, 40, 55, Figs. 1–3). According to Petitioner, because Conn’s copper rivets 14 are visible in Figure 2, “the anchor vias form openings in conducting layer 20.” *Id.* (citing Ex. 1003 ¶ 86; Ex. 1004, Fig. 2). Petitioner further contends that an ordinarily skilled

artisan “would understand that Conn’s anchor via rivet is a conductor that has an end entering conducting layer 20 and forming ‘a protruding portion extending from . . . said semiconductor substrate’” and that “conducting layer 20 is on a side of the substrate corresponding to the claimed ‘backside.’” *Id.* at 33 (citing Ex. 1003 ¶¶ 89–90; Ex. 1004, Fig. 1).

Patent Owner first repeats its argument for limitation [1a] that the anchor vias are not in the “corners.” Prelim. Resp. 27–28. At this stage of the proceeding, this argument is unavailing for the reasons discussed above for limitation [1a].

Patent Owner next argues, without explanation, that Petitioner fails to show that Conn’s anchor vias are filled with metal. Prelim. Resp. 27. This argument is unavailing, at this stage of the proceeding, based on Conn’s explicit disclosure that conductor 14 “may be formed of copper, aluminum, gold, silver or other conductor.” Ex. 1003 ¶ 33.

Patent Owner next argues that “Petitioner merely selects an embodiment where the copper plane covers 90% of the carrier substrate, then assumes without support that the carrier substrate is arranged as in its annotated version of [Conn’s] Figure 2.” Prelim Resp. 25 (referring to Pet. 30 showing annotated Figure 2 of Conn). Conn’s disclosure relied on by Petitioner in support of its annotated Figure 2 provides “at least 90% of an entirety of the surface area of the carrier substrate” is covered by the conducting layer but also states that “[w]hile the integrity of the carrier substrate laminate of the invention remains in tact for even higher area coverage, design rules will likely in practice never reach as high as 100%.” Ex. 1004 ¶ 31. Petitioner’s annotated version of Conn’s Figure 2 shows a yellow border, representing carrier substrate 31, extending outward from the

edges of conducting layer 20. Petitioner's position is supported by paragraph 31 of Conn, i.e., at least 90% of the carrier substrate, but less than 100%, is covered by the conducting layer. *See* Pet. 30. Consequently, Patent Owner's argument is unavailing based on the present record.

We have reviewed Petitioner's contentions and evidence in light of Patent Owner's arguments and find that, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Conn discloses this limitation.

d) “[1c] a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;”

Petitioner contends “Conn’s conducting layer 20 is on the backside” and corresponds to the recited backside metal layer “and the substrate surface on which conducting layer 20 is disposed” corresponds to the recited bottom surface. Pet. 35 (citing Ex. 1003 ¶ 91). Petitioner further contends that Conn’s “via conductors in the anchor vias form protruding portions that are mechanically ‘connected to’ and ‘in contact with’ conducting layer 20.” *Id.* at 36 (citing Ex. 1004 ¶¶ 28–30, 38, 40, 55, Figs. 1–3). Petitioner next contends that “[t]o manufacture such connections, Conn discloses that via conductors 14 and conducting layer 20 are ‘formed to be a unitary, single, monolithic structure’ or ‘formed in separate process steps out of a single material’ (e.g., copper or tungsten).” *Id.* (citing Ex. 1004 ¶¶ 33–34, 37, 41). According to Petitioner, an ordinarily skilled artisan “would understand that both methods will cause via conductors 14 to form a metallic bond with conducting layer 20.” *Id.* (citing Ex. 1003 ¶ 92).

Patent Owner does not address limitation [1c] in the Preliminary Response. *See* Prelim. Resp.

We have reviewed Petitioner’s contentions and evidence and find, on the present record at this stage of the proceeding, Petitioner sufficiently establishes that Conn discloses this limitation.

e) “[*Id*] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.”

Petitioner contends that Conn discloses this limitation “by *not* disclosing that any anchor vias provide any ground connection but instead disclosing the anchor vias or the via conductors therein do not need to reach the opposite side of the carrier substrate, thus recognizing the purpose of the anchor vias is *not* to provide any ground connection.” Pet. 36–37 (citing Ex. 1003 ¶ 93; Ex. 1004, Fig. 1). In support of this contention, Petitioner argues the “‘via conductors 14 do[] not necessarily have to go all the way through’ the anchor vias.” *Id.* at 37 (citing Ex. 1004 ¶ 28). According to Petitioner, “[t]his means the anchor vias and via conductors 14 are *not* designed for providing electrical connection (including ground connection) to any active device on that side” and “via conductors 14 do not provide ground connection to any active device in the carrier substrate because it may only have ‘[p]assive components,’ not active devices.” *Id.* (citing Ex. 1003 ¶ 93; Ex. 1004 ¶ 26).

Patent Owner doesn’t directly address Patent Owner’s contentions that Figure 1 of Conn shows that the anchor vias 14 do not extend through substrate 12 and, therefore, do not provide a ground connection for active devices. *See* Prelim. Resp. 29–31. Rather, Patent Owner argues that Conn’s Figure 5 embodiment (and claim 19) show that “the anchor vias, which contain conducting metal and are attached to a copper ground plane, can also

be used to provide electrical connections and, therefore, provide grounding to active devices.” *Id.* at 29–30.

We note that Conn’s Figure 5 is described as “another embodiment” and appears to differ from the Figure 1 embodiment in that it contains “dielectric layers disposed between . . . conductive layers” and “two regions . . . electrically discontinued that can be supplied with different signals/electrical potentials.” Ex. 1004 ¶¶ 42–45. Therefore, even if we were to agree with Patent Owner that Conn’s Figure 5 shows an embodiment where anchor vias provide a ground connection for active devices, that would not undercut Petitioner’s showing with respect to the embodiment shown in Figure 1 where anchor via 14 does not extend entirely through substrate 12.

After reviewing Petitioner’s contentions in light of Patent Owner’s arguments, we find, based on the present record at this stage of the proceeding, that Petitioner sufficiently establishes that Conn discloses this limitation.

f) Summary of Claim 1

For all the foregoing reasons, Petitioner establishes a reasonable likelihood that claim 1 is anticipated by Conn.

3. Claims 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19

Petitioner cites to additional disclosures in Conn that it contends corresponds to the limitations in claims 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19. Pet. 2–45.

Patent Owner does not address these claims separately from the arguments raised regarding claim 1. *See* Prelim. Resp.

We reviewed the evidence cited by Petitioner and find it sufficient for the reasons provided by Petitioner.

E. Grounds 2A and 2B: Alleged Obviousness of Claims 1, 2, 4–7, 8, 9, 11, 12, 14–17, 18, and 19 over Conn

Petitioner presents these alternative grounds to Ground 1. Pet. 45–56. Given our preliminary determination of Ground 1 discussed above, we do not reach these alternative grounds at this time.

F. Ground 3A: Alleged Obviousness of Claims 1, 2, 4–7, 11, 12, and 14–17 over Gambino in view of Conn

Petitioner contends claims 1, 2, 4–7, 11, 12, and 14–17 would have been obvious over Gambino in view of Conn. Pet. 56–79.

Patent Owner argues that Ground 3A fails to show Gambino or Conn teaches the claimed metal filler that does not provide a ground connection to active devices. Prelim. Resp. 34–38.

We begin with a brief summary of Gambino. We then address the parties' contentions.

1. Gambino (Ex. 1005)

Gambino “relates to semiconductor structures and, more particularly, to patterned backside metal ground planes for improved metal adhesion and methods of manufacture.” Ex. 1005 ¶ 1. Gambino states “[p]ackaging lead inductance is a major design issue,” e.g., whereby the emitter ground leads of some HBT designs contact the package via wire bonds or flip-chip solder bumps. *Id.* ¶ 2. Wire bond package ground leads have an undesirably high inductance. *Id.* Flip chips have undesirably high packaging complexity and cost. *Id.*

Gambino discloses patterning metal on a backside surface of a substrate and these limited regions “contact through-silicon vias.” Ex.

1005 ¶ 15; *see also id.* ¶¶ 23–26 (patterning process). The backside metal is formed only on the die (e.g., not in any dicing channel) and “patterned differently than wiring” to form patches of metal coupled to the same potential (e.g., ground). *Id.* Because the patterned backside metal ground plane is not deposited in the dicing channel, the invention solves a prior problem that dicing of a substrate having blanketed metal can stress the metal-silicon interface in the dicing channel and thereby cause peeling of the metal from the corners and edges of the die. *Id.* ¶¶ 16–17.

Figure 3 is reproduced below:

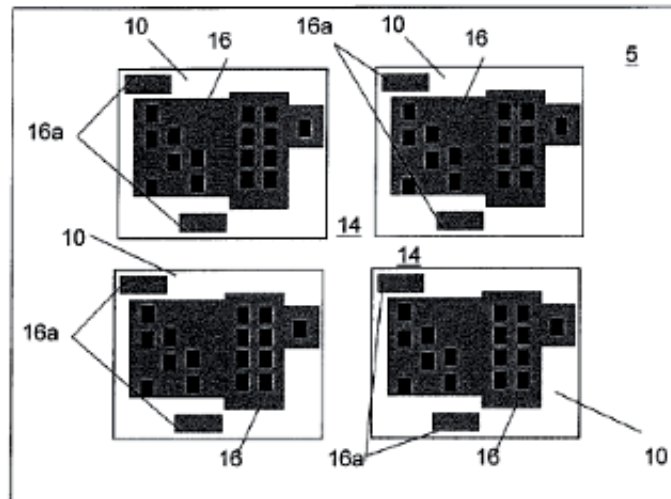


Figure 3 “shows a patterned backside metal with metal pads and methods of manufacture in accordance with additional aspects of the present invention.”

Ex. 1005 ¶ 11. Backside metal 16 is patterned into metal pads 16a over TSVs⁶ 12. Ex. 1005 ¶¶ 27–28. The metal pads 16a are configured (e.g., located and shaped) such that the dies 10 sit flatly on the package substrate and add mechanical support to the dies 10. *Id.* ¶ 28.

⁶ “TSV” is an acronym for “through silicon vias.” Ex. 1005 ¶ 4.

2. Claim 1

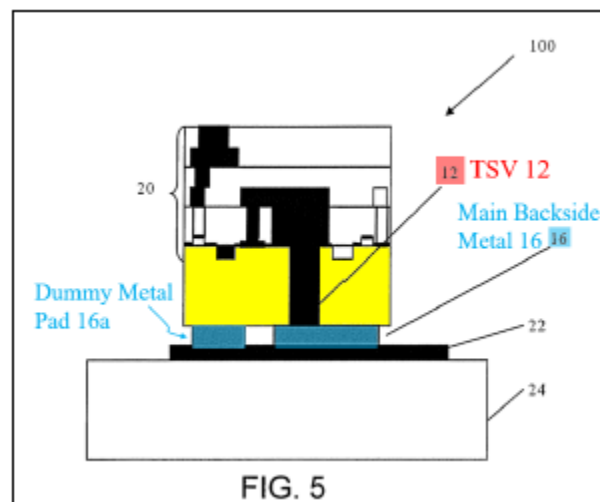
Petitioner provides a limitation-by-limitation analysis of claim 1, mapping each claim limitation to the combination of Conn and Gambino and setting forth reasons why an ordinarily skilled artisan would have been motivated to combine the teachings of Conn and Gambino with a reasonable expectation of success. Pet. 59–70.

We have reviewed Petitioner’s contentions and evidence for the preamble of claim 1 and limitations 1[a]–[1c]. We find that, based on the present record at this stage of the proceedings, Petitioner sufficiently establishes that the combination of Gambino and Conn teaches the preamble of claim 1 and limitations 1[a]–1[c].

We now turn to the dispute raised by Patent Owner which relates to limitation 1[d]. We begin by analyzing Petitioner’s contentions concerning motivation to combine Gambino and Conn and then address limitation 1[d].

Motivation to Combine and Reasonable Expectation of Success

Petitioner provides the following annotated version of Gambino’s Figure 5:



Pet. 60. Figure 5 is “a packaged module with a backside metal ground plane attached to a substrate.” Ex. 1005 ¶ 13. Petitioner adds blue text to the left side of Figure 5, “Dummy Metal Pad 16a” with a blue arrow pointing to element 16a, blue text to the lower right, “Main Backside Metal 16,” and red text to the upper right of Figure 5, “TSV 12.”

Petitioner contends that Gambino discloses a packaged module comprising metal wiring layers 20 in communication with TSV 12, back side metal 16 connected to substrate ground plane 22 which is bonded to substrate 14, and dummy metal pads 16a located at the corners and peripheries of the substrate “to provide mechanical support.” Pet. 59 (citing Ex. 1005 ¶¶ 13, 27, 28, 30, Figs. 3, 5). Petitioner further contends that back side metal 16 covers the electrical TSV’s. *Id.* Petitioner further contends that an ordinarily skilled artisan “would have found it obvious to apply Conn’s teachings to create anchor vias in Gambino’s dummy metal pads 16a and/or main backside 16, to secure them to the substrate and prevent delamination during singulation.” *Id.* (citing Ex. 1003 ¶ 135).

In support of the motivation to combine argument, Petitioner argues, *inter alia*, Gambino and Conn are both directed to improving structural integrity of packaged devices (*id.* at 61 (citing Ex. 1003 ¶ 136; Ex. 1004 ¶ 11; Ex. 1005 ¶ 1)), “there would have been a desire to improve Gambino by adding Conn’s anchor vias at dummy metal pads 16a and main backside metal 16, to ensure they remain secured to the substrate” (*id.* at 62 (citing Ex. 1003 ¶ 137)), and an ordinarily skilled artisan would have been interested in combining the techniques of Gambino (backside dummy metal pads) and Conn (anchor vias) “to maximize backside metal adhesion” (*id.* at 63 (citing Ex. 1003 ¶ 140)).

Petitioner next contends that there would have been a reasonable expectation of success for the combination. Pet. 64. In support of reasonable expectation of success, Petitioner contends that “Conn discloses the anchor vias can secure conducting layers with sizes ranging from 10% to 100% of the substrate’s total surface area” and Gambino’s “dummy metal pads 16a and main backside metal 16 have sizes in this range, and thus can be securely held by the anchor vias.” *Id.* at 64–65 (citing Ex. 1003 ¶ 144; Ex. 1005 ¶¶ 30–31).

We have reviewed Petitioner’s contentions and evidence and, based on the present record at this stage of the proceeding, find that Petitioner sufficiently establishes that an ordinarily skilled artisan would have been motivated to combine the teachings of Gambino and Conn and would have had a reasonable expectation of success in doing so.

For limitation [1d], Petitioner contends that the combination of Gambino and Conn teach this limitation “because corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection, which means the anchor vias therein do not provide ground connection to active devices.” Pet. 70 (citing Ex. 1003 ¶ 151; Ex. 1004 ¶¶ 28–30).

Patent Owner first argues “[t]he Petition contends that it would have been obvious to *replace* Gambino’s dummy metal pad with the via disclosed in Conn to arrive at the claimed invention.” Prelim. Resp. 35 (emphasis added). According to Patent Owner, “if the dummy metal pad 16a in Gambino was replaced with the vias disclosed in Conn, the result of the combination would be a via that provides connection to the ground plane, which is directly prohibited by the Challenged Claims of the ’826 Patent.”

Id.; *see also id.* at 36 (“Replacing the metal pad 16a in Gambino with the metal-filled via from Conn would provide direct connection to the ground plane.”); *id.* (“Replacing the metal pad 16a in Gambino’s Figure 5 . . . would also connect the devices above to the new TSV in the wire layers 20 directly to the ground plane.”); *id.* at 37 (“The Petition provides no explanation as to how a metal pad connected directly to the ground plane could be replaced with a via and not provide grounding.”).

Contrary to Patent Owner’s contentions, the Petition does not propose *replacing* Gambino’s metal dummy pads 16a with Conn’s anchor vias. Rather, Petitioner proposes “to apply Conn’s teachings to create anchor vias in Gambino’s dummy metal pads 16a.” Pet. 60. Gambino discloses “metal pads 16a are provided at strategic locations on the dies 10 to provide mechanical support.” Ex. 1005 ¶ 28.

Gambino discloses that “wiring layers 20 can include vias, wires, and a host of different active or passive devices.” Ex. 1005 ¶ 30. Patent Owner does not direct us to any disclosure in Gambino that dummy metal pads 16a are electrically connected to wiring layers 20 or any of the active devices therein. *See* Prelim. Resp. 34–38. Petitioner proposes Conn’s anchor vias in Gambino’s ground plane 22 with the “protruding portion” disposed in Gambino’s ground plane 22 and the straight portion extending from the protruding portion into dummy metal pad 16a. *See* Pet. 68 (Conn Fig. 1 annotated). Because Gambino’s dummy metal pads 16a are not electrically connected to wiring layers 20, placement of Conn’s anchor vias as described will not electrically connect anchor vias to wiring layers 20 (or any active devices therein) and will not provide a ground connection for the active devices.

For all the foregoing reasons, we find that Petitioner's showing is sufficient at this stage of the proceeding.

3. *Claims 2, 4–7, 11, 12, and 14–17*

Petitioner cites to additional disclosures in Gambino and Conn as corresponding to the limitations in claims 2, 4–7, 11, 12, and 14–17. Pet. 70–75. Patent Owner does not address these claims separately from the arguments raised regarding claim 1. *See* Prelim. Resp. We have reviewed the evidence cited by Petitioner and find it sufficient for the reasons provided by Petitioner.

G. Ground 3B: Alleged Obviousness of Claims 10 and 20 over the combination of Gambino and Conn in view of Ding

Petitioner contends claims 10 and 20 would have been obvious over the combination of Gambino and Conn in view of Ding. Pet. 58. 75–79.

Patent Owner does not address these claims separately from the arguments raised regarding claim 1. *See* Prelim. Resp.

Given our preliminary determination concerning claim 1 discussed above and in the absence of any separate argument by Patent Owner, we do not reach this ground at this time.

H. Ground 4: Alleged Anticipation of Claims 1, 8–11, and 18–20 by Torii

Petitioner contends that claims 1, 8–11, and 18–20 are anticipated by Torii. Pet. 79–89. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003.

We begin with a brief summary of Torii. We then address the parties' contentions.

1. Torii (Ex. 1009)

Torii is titled “Semiconductor Device.” Ex. 1009, code (54). Torii “relates to a semiconductor device, and more particularly, to a semiconductor device provided with an electrode penetrating through a substrate.” *Id.* ¶2.

Torii discloses that a vertical stacking of semiconductor chips may include TSV electrodes penetrating through the substrate of each semiconductor chip and thus providing electrical conduction between respective semiconductor chips. Ex. 1009 ¶4.

Figures 2A and 2B are reproduced below:

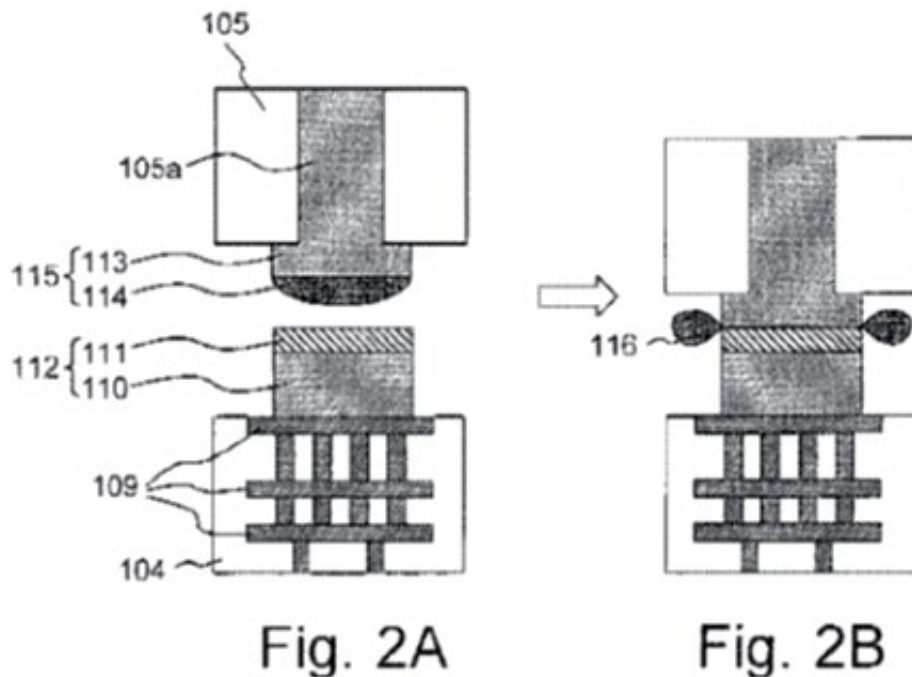


Figure 2A and 2b illustrate a “method of joining TSVs” of stacked semiconductor chips, “wherein FIG. 2A illustrates a state before joint and FIG. 2B illustrates a state after joint.” Ex. 1009 ¶ 30; *see also id.* ¶¶ 6–7 (describing Figure 1’s illustration of stacked semiconductor chips and Figure 2’s view after joining).

As shown in Figure 2A, a first chip 104 includes a front bump 112 and an interconnect layer 109 of a TSV (element 104a in Figure 1) and between the front bump 112 and TSV. Ex. 1009 ¶ 7. The front bump 112 includes a metal joining layer 111 and a first metal bump 110 between the interconnect layer 109 and metal joining layer 111. *Id.* A second chip 105 includes a rear bump 115. *Id.* The rear bump 115 includes a second metal joining layer 114 and a second metal bump 113 of a TSV 105a and between the second metal joining layer 114 and TSV 105a. *Id.*

As shown in Figure 2A, the front bump 112 of the first chip 104 and rear bump 115 of the second chip 105 are heated to solder-flow the second metal joining layer 114 and thereby join the first metal joining layer 111 and second metal joining layer 114. Ex. 1009, Fig. 2A. The second metal joining layer 114 transforms into a thin film and is consequently susceptible to damage from thermal stresses. *Id.*

The invention provides structure whereby the above “thin-filming of layers, such as a solder layer . . . fluidized by heating[,] is suppressed by providing sub-bumps . . . [that] come into contact with one another . . . [to] secur[e] margins of joint between the main bumps [110, 113].” Ex. 1009 ¶ 8.

Figure 3 is reproduced below:

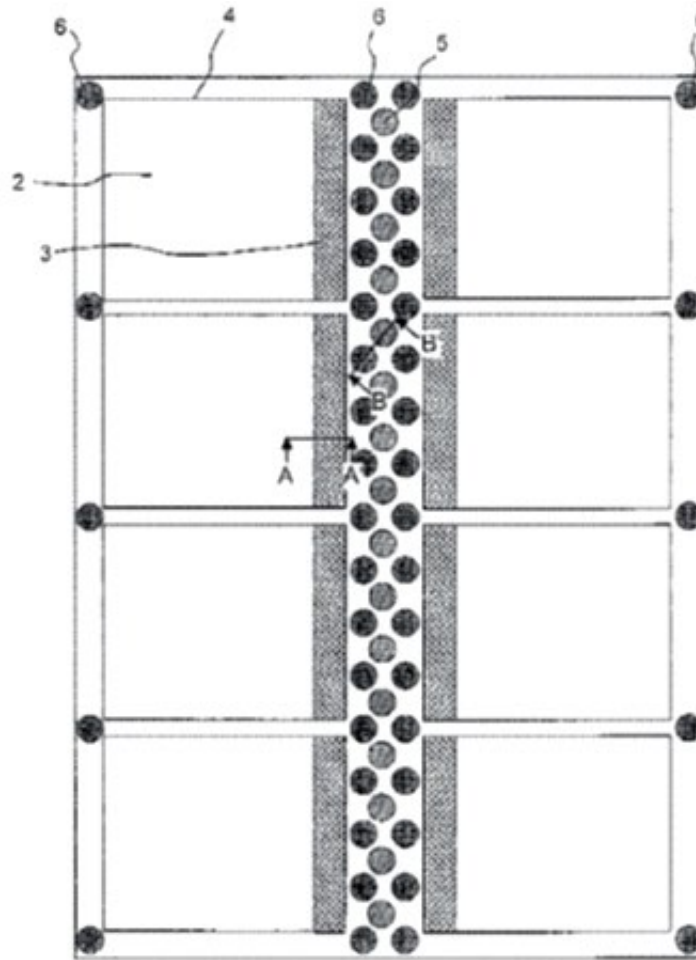


Figure 3A “is a layout plan view illustrating one example of a semiconductor chip according to one exemplary embodiment of the present invention.” Ex. 1009 ¶ 31. A memory mat 4 includes a memory cell region 2 and peripheral circuit region 3. *Id.* ¶ 45. Main bumps 5 of TSVs are disposed between two rows of the memory mats 4. *Id.* Sub-bumps 6 are disposed in proximity to main bumps 5 and along the outer circumference of semiconductor chip 1. *Id.*

A “main TSV” has main bumps and “is used mainly as a current pathway.” Ex. 1009 ¶ 48. A “sub-TSV” is a “dummy which is normally not used as a current pathway[] but can be used as a subsidiary current pathway, [e.g.,] . . . for releasing static electricity.” *Id.*

2. Claim 1

We focus on Patent Owner’s argument that Petitioner fails to show Torii teaches an anchor via with metal filler that does not provide a ground connection to active devices as required by limitation 1[d]. Prelim. Resp. 47–48.

“[1d] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.”

Petitioner contends that Torii discloses this limitation because it discloses that “[t]he sub-TSV is a dummy . . . normally not used as a current pathway.” Pet. 86 (citing Ex. 1009 ¶ 48).

Patent Owner contends that Petitioner’s quote “disingenuously removed the second half of the sentence which explicitly states that the sub-TSV can be used to conduct current, including static electricity, which of course is discharged to ground.” Prelim. Resp. 47 (citing Ex. 1009 ¶ 48). We agree with Patent Owner, at this stage of the proceeding, that a person of ordinary skill in the art would interpret paragraph 49, when read in its entirety, as disclosing a ground connection.

For all the foregoing reasons, Petitioner does not establish a reasonable likelihood that claim 1 is anticipated by Torii.

I. Ground 5: Alleged Anticipation of Claims 1, 2, 3, 9, 11, 12, 13, and 19 by Ide

In light of our preliminary determinations discussed above for Grounds 1, 3, and 4, we do not reach this ground at this time.

III. DISCRETIONARY DENIAL

Patent Owner argues that, because of co-pending district court litigation between Patent Owner and Petitioner, we should exercise our

discretion to deny institution under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). Pet. 21–27.

We consider the advanced state of a parallel district court action as a factor that may weigh in favor of denying a petition under § 314(a). *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018) (precedential). The following factors inform our assessment of “whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding”:

- 1) whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
- 2) proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
- 3) investment in the parallel proceeding by the court and the parties;
- 4) overlap of issues raised in the petition and in the parallel proceeding;
- 5) whether the petitioner and the defendant in the parallel proceeding are the same party; and
- 6) other circumstances that impact the Board’s exercise of discretion, including the merits.

Fintiv, IPR2020-00019, Paper 11 at 5–6.

1. Fintiv Factor 1

Patent Owner contends this factor supports exercising our discretion to deny institution because “[t]here is no stay of the parallel District Court Litigation and, in fact a motion for a stay by Petitioner has already been

denied.” Prelim. Resp. 55 (citing Ex. 2002, 1). Petitioner argues that this factor is “at worst neutral.” Pet. 102.

Petitioner’s motion for a stay of the District Court Litigation was denied as premature because “the Patent Trial and Appeal Board has not yet acted on a petition for *inter partes* review.” Ex. 2002, 1.

Although no stay of the District Court Litigation has been issued, it appears that the district court would entertain a renewed request by Petitioner for a stay after this Decision on Institution is entered. Consequently, we find that this factor is neutral.

2. *Fintiv Factor 2*

Patent Owner contends that this factor “strongly weighs in favor of discretionary denial.” Prelim. Resp. 54. Patent Owner argues that trial in the District Court Litigation “is scheduled for January 5, 2026” which is three months before the projected statutory deadline for a Final Written Decision in this proceeding. *Id.* (citing Ex. 2001). Petitioner argues that this factor is “at worst neutral.” Pet. 102.

The District Court’s Docket Control Order, filed in the district court on August 5, 2024, sets January 5, 2026 as the date to commence Jury Selection in the column labelled “Original Date.” Ex. 2001, 1. The column next to “Original Date” is labelled “Amended Date” and that column is blank. *Id.* The Docket Control Order is prefaced with the statement “it is hereby **Ordered** that the following schedule of deadlines is in effect until further order of this Court.” *Id.* The Docket Control Order also contemplates that the trial date may be continued under certain circumstances. *See id.* at 6 (“Motions for Continuance”). Based on this, it appears that January 5, 2026 date is not a firm date for starting jury selection

in the District Court Litigation but contemplates the possibility of a continuance. Nonetheless, there remains the possibility that a trial could be concluded within approximately 2 to 3 months after January 5, 2026 and prior to our statutory deadline in this case.

Fintiv instructs us that “the decision to institute will likely implicate other factors” when “the court’s trial date is at or around the same time as the projected statutory deadline.” *Fintiv*, IPR2020-00019, Paper 11 at 9. Given that the originally-scheduled trial date is far away and the final decision date in this case will be approximately three months after the originally scheduled trial date, we find that this factor weighs slightly in favor of exercising our discretion to deny institution.

3. *Fintiv Factor 3*

Patent Owner contends that this factor weighs in favor of exercising our discretion because the district court has issued various orders, discovery is under way, and the parties exchanged infringement contentions and invalidity contentions. Prelim. Resp. 55.

Petitioner contends that this factor favors institution because it “acted diligently and almost no parallel investment has occurred.” Pet. 102. According to Petitioner, Patent Owner served infringement contentions on July 18, 2024, fact discovery does not close until August 18, 2025, expert discovery closes on September 22, 2025, claim construction efforts by the parties begins on March 4, 2025, and the *Markman* hearing will not take place until July 8, 2025. *Id.* at 73–74 (citing Ex. 1016; Ex. 1017, 3–4).

Although the parties and district court have invested some minimal time in the District Court Litigation, substantial work remains to be done including the completion of fact and expert discovery, claim construction

briefing, pretrial motions, and preparation of a joint pretrial order. *See* Ex. 2001, 1–5.

For these reasons, we find that this factor weighs in favor of not exercising our discretion to deny institution.

4. *Fintiv Factor 4*

After the Preliminary Response was filed, Petitioner submitted a stipulation stating that it will not pursue, in the District Court Litigation, any ground that was raised or could have reasonably been raised in this proceeding. Paper 8, 1. Petitioner’s stipulation, thus, aligns with the stipulation relied on by the Board in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12, 18–19 (PTAB Dec. 1, 2020) (precedential).

Patent Owner argues that we should reject any “late” *Sotera* stipulation. Prelim. Resp. 57. The only authority cited for this argument are Board decisions concerning stipulations filed *after* a Decision on Institution was entered. *Id.* at 58–59. Petitioner’s stipulation was filed prior to this Decision being entered, is not “late,” and, thus, we decline to reject Petitioner’s stipulation.

In *Sotera Wireless*, the Board found that a stipulation such as the one proffered here by Petitioner addressed “concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions” and “ensures that an *inter partes* review is a ‘true alternative’ to the district court proceeding.” *Sotera*, IPR2020-01019, Paper 12 at 19. For these reasons, we find that this factor weighs “strongly in favor of not exercising discretion to deny institution.” *Id.*

5. *Fintiv Factor 5*

Patent Owner contends this factor weighs in favor of exercising our discretion to deny institution because Petitioner and Patent Owner are parties in the District Court Litigation. Prelim. Resp. 52. Petitioner argues that this factor is “at worst neutral.” Pet. 102.

Because Petitioner is the defendant in the District Court Litigation, this factor weighs in favor of exercising our discretion to deny institution.

6. *Fintiv Factor 6*

Patent Owner contends that “Petitioner does not present a strong case on the merits, further supporting denial of institution.” Prelim. Resp. 57. Petitioner contends that the merits support institution. Pet. 102.

As discussed above, the Petition sets forth challenges that meet the reasonable likelihood standard for institution based on the present record. We find that this factor is neutral.

7. *Fintiv Conclusion*

When we evaluate the *Fintiv* factors, we take “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv*, Paper 11 at 6. As discussed above, factor 4 weighs strongly in favor of not exercising our discretion to deny institution and factor 3 also weighs in favor of not exercising our discretion to deny institution while factors 2 and 5 weigh in favor of exercising our discretion. After consideration of all factors, we determine that efficiency, fairness, and integrity of the system are best served by not exercising our discretion to deny institution.

IV. CONCLUSION

Based on the present record, we determine that Petitioner demonstrates a reasonable likelihood that it would prevail in establishing that at least one challenged claim of the '826 patent is unpatentable. We, thus, institute an *inter partes* review of all challenged claims of the '826 patent based on all grounds in the Petition. At this stage of the proceeding, we have not made a final determination under 35 U.S.C. § 318(a) with respect to the unpatentability of any challenged claim.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '826 patent is instituted with respect to all challenged claims and grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4(b), *inter partes* review of the '826 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2024-01405
Patent 9,245,826 B2

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