

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,245,826
Filing Date: January 27, 2014
Issue Date: January 26, 2016

Inventors: Hadi Jebory, David J. Howard, and Scott B. Stetson
Title: ANCHOR VIAS FOR IMPROVED BACKSIDE METAL
ADHESION TO SEMICONDUCTOR SUBSTRATE

PATENT OWNER'S RESPONSE

Case No. IPR2024-01405

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LIST OF EXHIBITS

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung’s Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants’ Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	Declaration of John Berg
2005	CV of John Berg
2006	“Die Singulation Technologies for Advanced Packaging: A Critical Review” (Lei 2012)
2007	“3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages” (Ho et al., 2013)
2008	“Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks” (Rabie et al., 2021)
2009	Deposition of Scott E. Thompson, taken June 9, 2025.

I. INTRODUCTION

On September 20, 2024, Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Petitioner”) submitted a Petition (Paper 1, “Petition” or “Pet.”) to institute *inter partes* review (“IPR”) of U.S. Patent No. 9,245,826 (Ex. 1001, the “’826 Patent”), challenging Claims 1-20 (the “Challenged Claims”). The Petition asserts that: (i) Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 are anticipated by United States Patent Application Publication No. US 2009/0079056 to Conn (“Conn” or Ex. 1004); (ii) Claims 1, 2, 4-7, 9, 11, 12, 14-17, 19 are rendered obvious over Conn in view of knowledge of a person of ordinary skill in the art (“POSA”); (iii) Claims 8 and 18 are rendered obvious over Conn in view of knowledge of a POSA and applicant admitted prior art; (iv) Claims 1, 2, 4-7, 11, 12, 14-17 are rendered obvious over U.S. Patent Application Publication No. US 2014/0138844 to Gambino et al. (“Gambino” or Ex. 1005) in view of Conn; (v) Claims 10 and 20 are rendered obvious over Gambino in view of Conn and U.S. Patent Application Publication No. US 2012/0104546 to Ding et al. (“Ding” or Ex. 1008); (vi) Claims 1, 8-11, and 18-20 are anticipated over U.S. Patent Application Publication No. US 2013/0082382 to Torii (“Torii” or Ex. 1009); and (vii) Claims 1-3, 9, 11-13, and 19 are anticipated over U.S. Patent Application Publication No.

US 2012/0256310 to Ide (“Ide” or Ex. 1010). The Board should issue a final written decision finding all claims not proven invalid for the reasons set forth below.

In Ground 1, *Conn* does not disclose the claimed anchor via located in a corner of a semiconductor substrate, and Petitioner attempts improperly to cure this deficiency with annotations that assume disclosures not present in *Conn*. *Conn* further does not disclose claim 9’s limitation of a metal filler that is bonded to both sides of a substrate while also not providing a ground connection.

In Ground 2, Petitioner attempts to combine *Conn* with the knowledge of a POSA to cure two deficiencies in *Conn*: the disclosure of a metal layer on the “backside” and the use of “active devices.” But, even assuming the Petitioner is correct regarding the knowledge of a POSA, Ground 2 does not cure the deficiencies of *Conn* explained in Ground 1.

In Ground 3, Petitioner combines *Gambino* with *Conn* (and, for two dependent claims, adds *Ding* to this combination), but this combination does not result in the claimed invention because Gambino’s process, on which Petitioner expressly relies, cannot form *Conn*-style anchor vias that meet the claims.

In Ground 4, as the Board found in its Institution Decision, *Torii* does not anticipate any claims because its alleged anchor vias are used to provide electrical

connections to discharge static electricity, *i.e.*, grounding. Moreover, *Torii* does not disclose the backside metal layer as claimed.

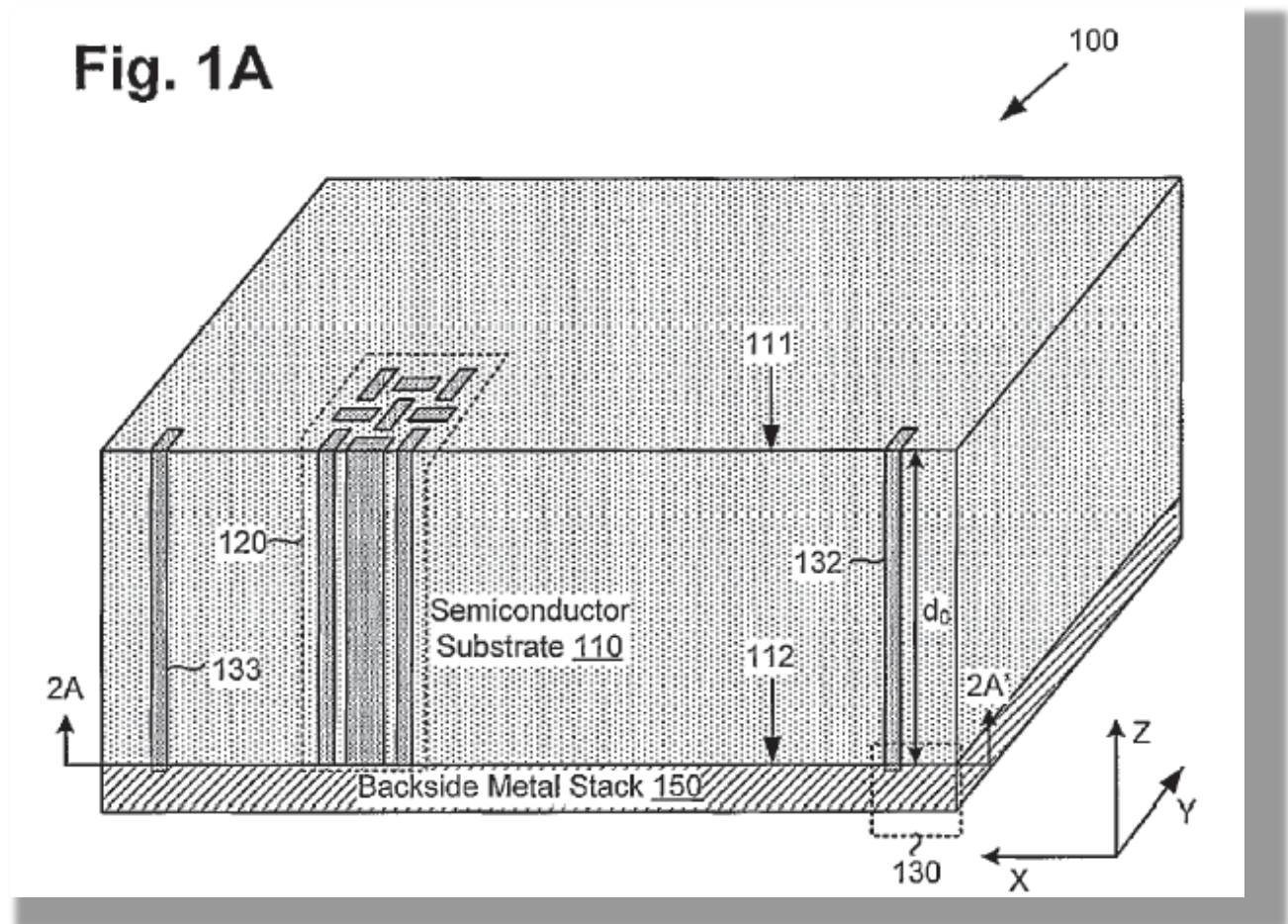
In Ground 5, *Ide* similarly fails to disclose the claimed “backside metal layer” because the alleged metal layer is not on the semiconductor surface.

Accordingly, as explained below and by the testimony of Patent Owner’s expert, Mr. John Berg, the Board should issue a Final Written Decision finding all Challenged Claims not unpatentable.

II. THE ’826 PATENT

The ’826 Patent describes and claims an improvement in semiconductor design. More specifically, the present invention relates to “anchor vias for improved backside metal adhesion to a semiconductor substrate.” ’826 Patent, 1:42-46. The ’826 Patent describes problems in the art. When a backside metal layer is attached to a semiconductor substrate using an adhesive, as conventionally done, “unacceptably low yields are often achieved during fabrication due to the backside metal layer peeling from the semiconductor substrate.” *Id.*, 1:36-38. This is because “fabrication procedures such as semiconductor die singulation and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die.” *Id.*, 1:30-34; Ex. 2004, ¶ 29.

The inventors of the '826 Patent overcame this problem by placing one or more through-silicon vias, called an “anchor via,” in the corner of the semiconductor die where these stresses are the greatest, and using those anchor vias “to improve backside metal adhesion.” '826 Patent, 2:44-47. Figures 1A and 1B of the '826 Patent, reproduced below, are exemplary:

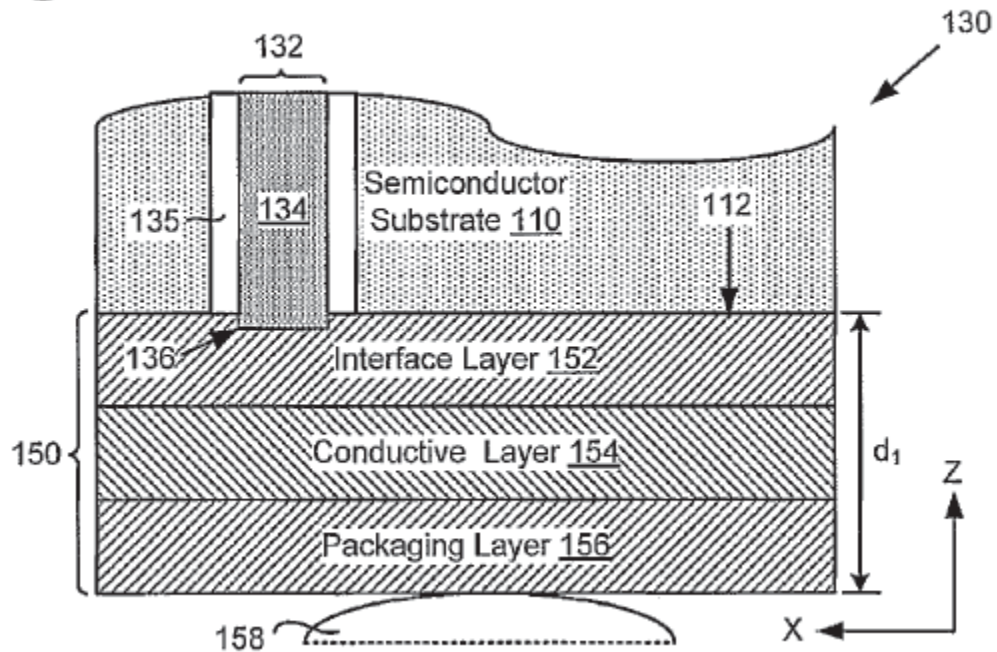


'826 Patent, FIG. 1A. Ex. 2004, ¶ 30. In Figure 1A, the '826 Patent discloses two anchor vias, 132 and 133, which are formed in the semiconductor substrate in “a

peripheral region,” as well as a group of vias 120 which are not anchor vias, but rather are formed “in a core region of semiconductor substrate 110.” ’826 Patent, 3:2-5. The core vias 120 “provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110.” *Id.*, 3:5-11. One example is given of an active device that is grounded using the core vias, which is “the emitters of bipolar transistors.” *Id.*; Ex. 2004, ¶ 31.

The anchor vias, on the other hand, do not provide ground connection but “instead provide[] physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150.” ’826 Patent, 3:12-17; Ex. 2004, ¶32. The bottom of an anchor via 132 is shown below in Figure 1B:

Fig. 1B

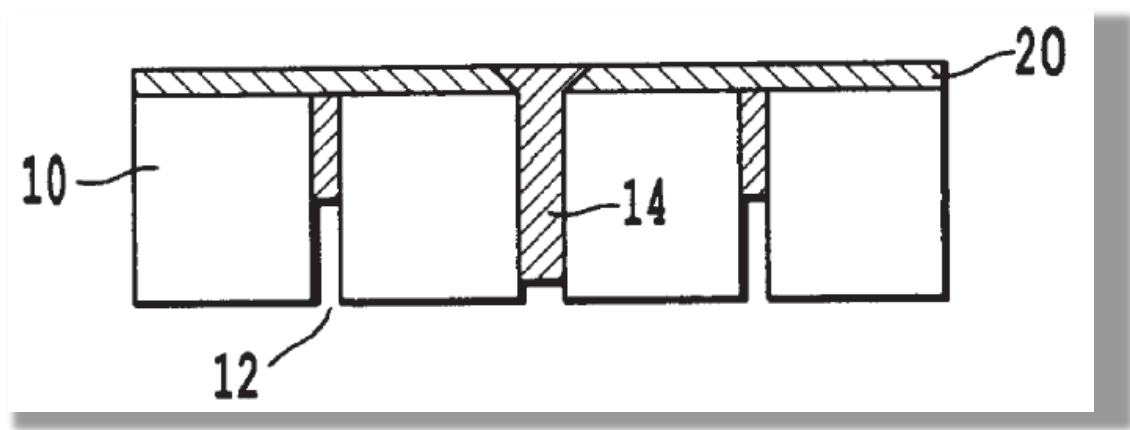


'826 Patent, Fig. 1B. This anchor via contains a protrusion 136 that extends into the metal layer, “such that when interface layer 152 is deposited on bottom side 112 of semiconductor substrate 110 the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond.” *Id.* 3:43-48. Ex. 2004, ¶ 33.

III. THE ALLEGED PRIOR ART

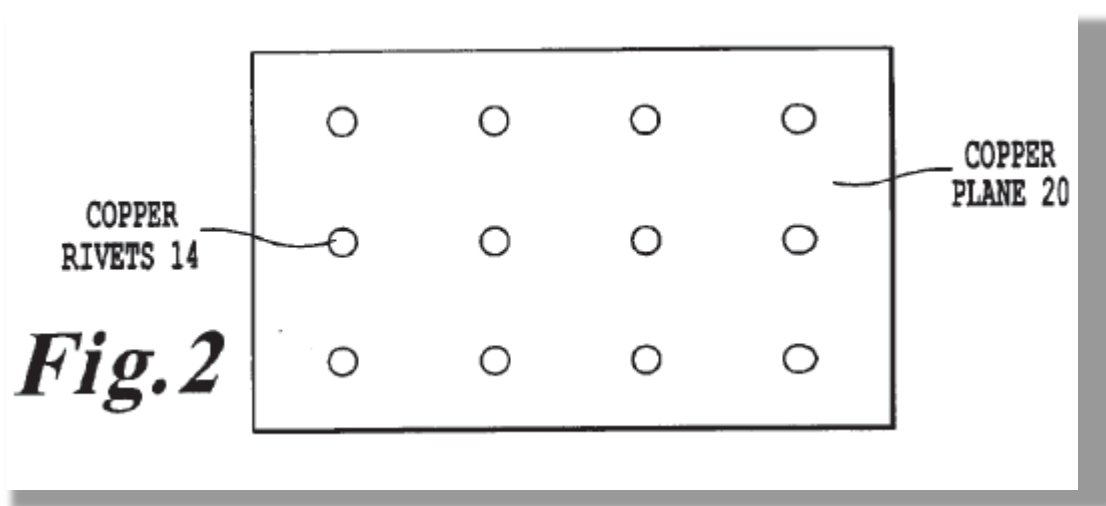
A. Conn

U.S. Patent Application Publication No. US 2009/0079056 to Robert O. Conn is titled “Large Substrate Structural Vias.” *Conn* relates to “a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.” Ex. 1004, [0003]. According to *Conn*, problems existed in the art where “extensive and repeated temperature changes cause fatigue of the package and the structure including the package.” *Id.* [0005]. *Conn* recognizes that “[o]ne place where this fatigue occurs is between the layers of a package laminate, or between a packaged part and a PCB.” *Id.* Ex. 2004Berg, ¶ 65.



Ex. 1004, Fig. 1. *Conn* discloses in Fig. 1, above, a “conducting layer” 20 that is connected to a “via conductor 14” which is formed in “via 12” to provide an anchor via, which is “considered a rivet formed in the carrier substrate and in contact with

the conducting layer 20 by which the conducting layer 20 maintains its structure under thermal stress.” *Id.* [0028]. *Conn*’s Figure 2 shows the conducting layer 20 being penetrated by twelve of the via conductors 14, which are annotated as “copper rivets”:



Ex. 1004, Fig. 2. Ex. 2004, ¶ 66. *Conn* also discloses that, although only the copper plane 20 is shown in Figure 2, the semiconductor substrate is larger in surface area than the copper plane. *Id.* [0030], [0031] (“In one embodiment, the major part of the first surface covered by the conducting layer covers at least 10% of an entirety of the surface area of the carrier substrate.”). Ex. 2004, ¶ 67.

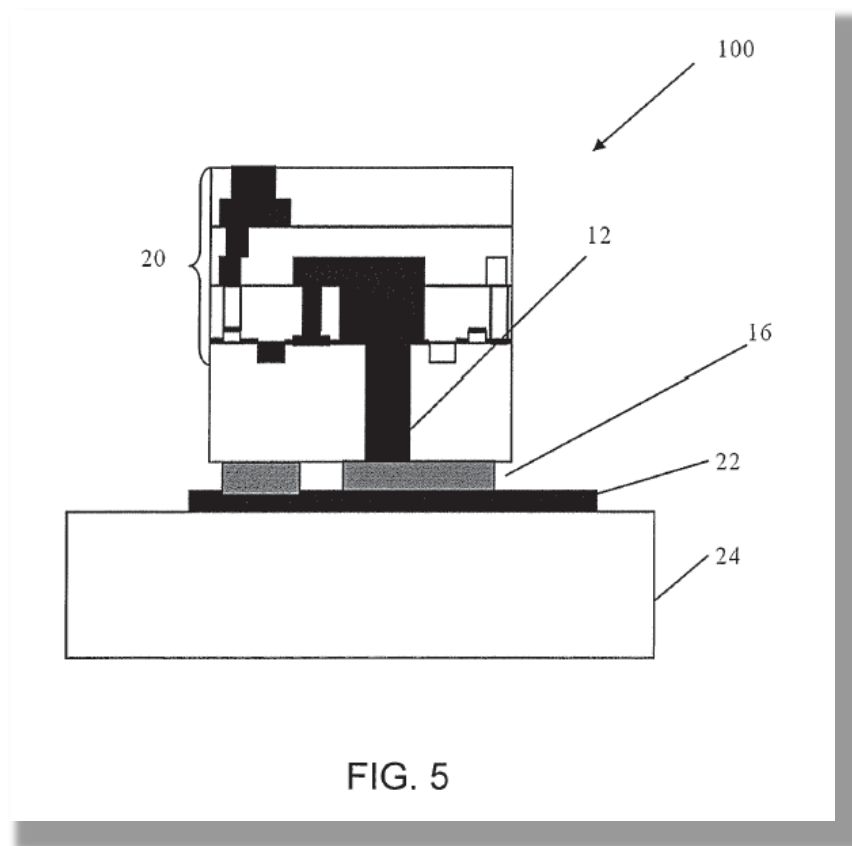
Conn does not mention placing the anchor vias in the corner of the semiconductor substrate, and the only mention of a corner in *Conn* is the corner of the via itself. Ex. 1004, [0054]. *Conn* also does not state that the vias are used for

structural protection during fabrication. Notably, *Conn* also discloses that the via conductors 14 disclosed in Figure 1 and Figure 5 “can have a volume less than a volume of the via in which the conductor is formed” (*Id.* [0043]), and that different layers of the substrate “can be connected to one or many second via conductors . . . similar to the via conductor 14” and can be “supplied with a control signal/electrical potential” *Id.* [0046], [0047]. Ex. 2004, ¶ 68.

B. Gambino

U.S. Patent Application Publication No. US 2014/0138844 to Jeffrey P. Gambino et al. is titled “Patterned Backside Metal Ground Plane For Improved Metal Adhesion.” *Gambino* discloses a die including a metal ground plane 16 that includes through-silicon vias (TSV’s). Ex. 1005, Abstract. *Gambino* describes a problem with existing designs for RF analog chips, namely that the emitter ground leads used in SiGe hetero-junction bipolar transistor (HBT) RF designs “are normally contacted to the package either using multiple wire bonds or flip chip solder bumps.” *Id.* [0002]. Wire bond leads have high inductance, and while flip chip solder bumps have low inductance, “they increase packaging complexity and are expensive.” *Id.* , ¶ 69.

Gambino proposes a solution to the problem of grounding emitters in RF analog chips, which is to place through-silicon vias (TSVs) in a semiconductor die, forming a metalized ground plane on a backside of the substrate, and placing the TSVs in contact with the ground plane. Ex. 1005, [0005]. “Grounded through silicon vias (TSVs) can be used to reduce ground lead inductance and reduce the bond pad area on the chip surface.” *Id.* [0016]. *Gambino* shows an example of one of these TSV’s 12, grounded to the metals 16 and 22 in Figure 5:

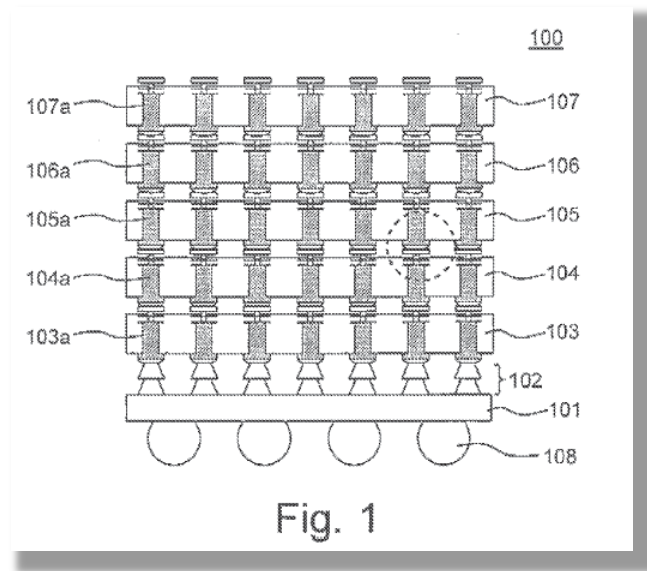


Ex. 1005, FIG. 5. Ex. 2004, ¶ 70. Nowhere does *Gambino* disclose or contemplate

using vias for a purpose other than providing ground connections, and *Gambino* explicitly discloses the use of a metal pad 16a “to provide mechanical support.” Ex. 1005, [0028]. *Gambino* does not disclose or contemplate any problems or solutions having to do with anchoring a semiconductor substrate to a metal layer. Ex. 2004, ¶ 71.

C. Torii

U.S. Patent Application Publication No. US 2013/0082382 to Koji Torii is titled “Semiconductor Device.” *Torii* discloses “a semiconductor device provided with an electrode penetrating through a substrate.” Ex. 1009, [0002]. The problems discussed in *Torii* arise in semiconductor devices which are vertically stacked, where through silicon vias (TSVs) are used to create the electrical connections between vertically-stacked chips. *Id.* [0004]. Figure 1 of *Torii*, shown below, discloses a group of stacked semiconductor chips that are connected by TSVs 104a, 105a, 106a, and 107a:



Ex. 1009, Fig. 1. Ex. 2004, ¶ 72. *Torii* describes that when joining the chips, the metal “becomes liable to segregation at the interface” which “may decrease joint strength and induce bump cracks.” Ex. 1009, [0007]. Ex. 2004, ¶ 73.

Torii describes the creation of two types of through-silicon vias: a “main TSV” and a “sub-TSV.” Ex. 1009, [0045], [0048]. The main TSV is used “mainly as a current pathway” and a sub-TSV “can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.” *Id.* [0048]. In one embodiment, *Torii* describes that the TSVs can be formed from the front surface of the substrate, rather than the rear. *Id.* [0093] (Exemplary Embodiment 5). In this embodiment, as shown in Figure 46 which is heavily cited in the Petition, there exists a “second main bump 88” and a “second sub-bump 89” that are on the back side of

the device:

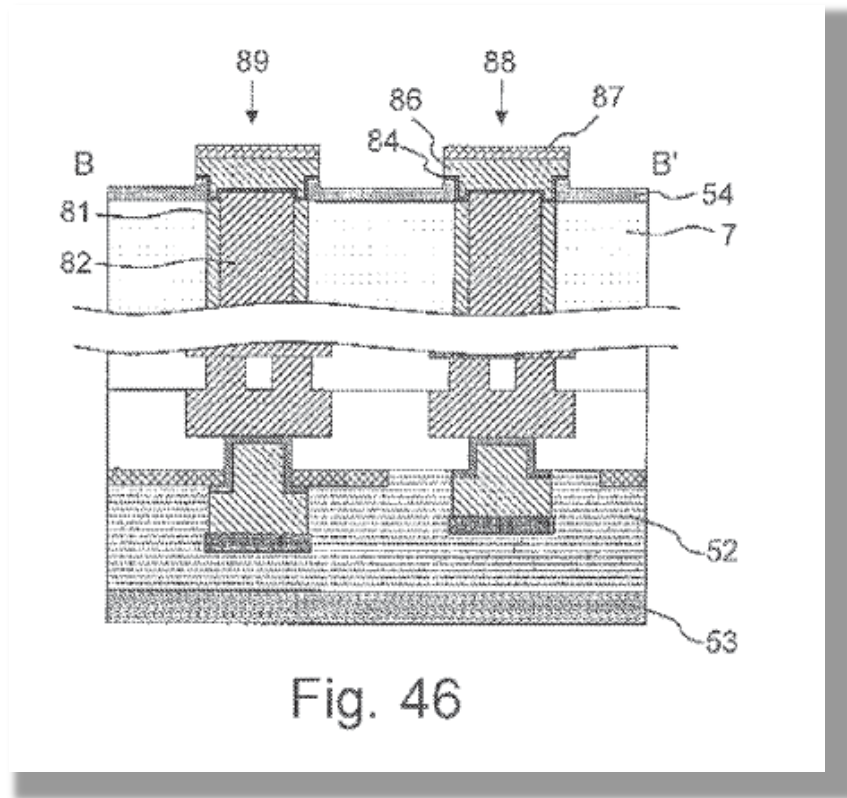


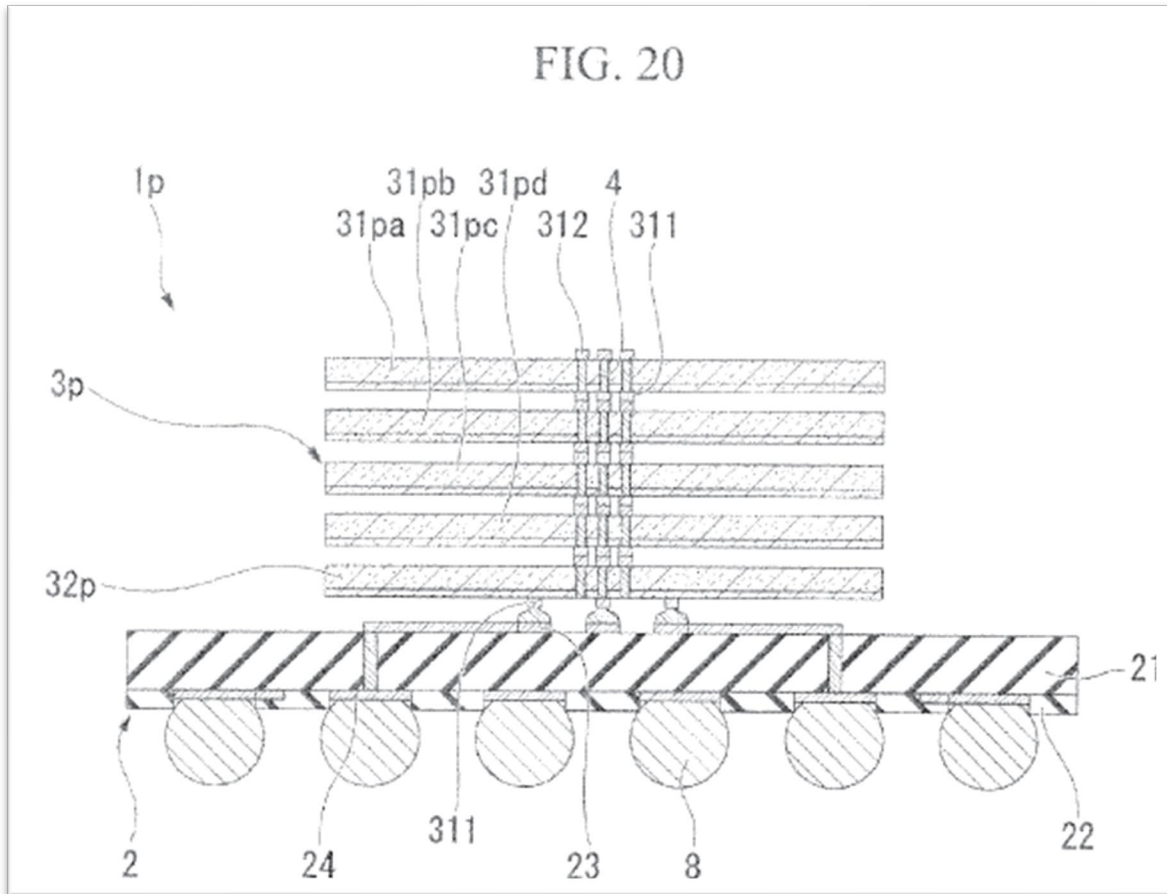
Fig. 46

Ex. 1009, Fig. 46, [0100]. Also located on the rear of the device is a “rear-surface protective film 54,” (*Id.*) but the bumps that form elements 88 and 89 are not shown connected to a metal layer. Ex. 2004, ¶ 74.

D. Ide

U.S. Patent Application Publication No. US 2012/0256310 to Akira Ide is titled “Semiconductor Device.” *Ide*, like *Torii*, also describes a multi-level vertically

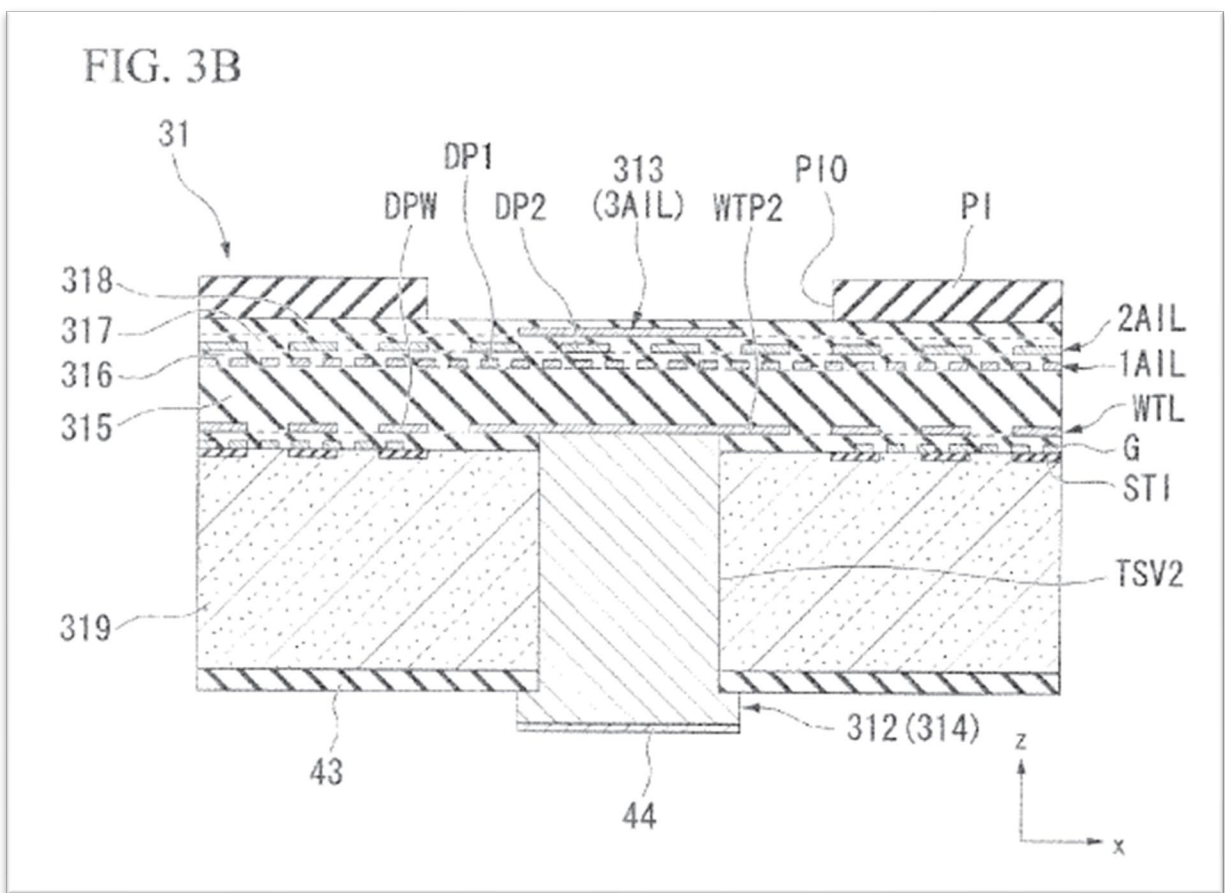
stacked semiconductor structure. Ex. 1010, Abstract. *Ide* discloses a plurality of memory chips 31pa to 31pd and an interface chip 32p, as shown in FIG. 20:



Ex. 1010, FIG. 20, [0006]. Ex. 2004, ¶ 75. Each of the memory chips and the interface chips include a “surface mark” and a “rear mark” on each side of the chip, which “are used for alignment when semiconductor chips are stacked.” Ex. 1010, [0010]. The various marks are photographed by the equipment used to assemble the chips. *Id.* The inventor recognized a problem, which is that “a recognition error of

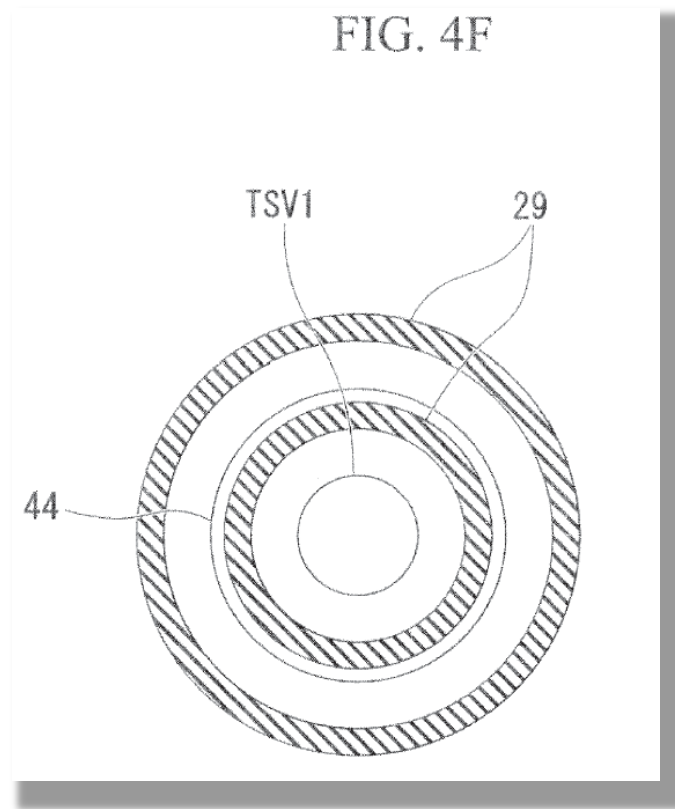
the surface mark 313 occurs in a TSV stacking process and a throughput of the above-described assembly process is considerably degraded.” *Id.* [0022]. Ex. 2004, ¶ 76.

Ide also discloses Figure 3B, reproduced below:



Ex. 1010, FIG. 3B. Ex. 2004, ¶ 77. According to *Ide*, Figure 3B discloses a “surface mark 313” that is formed from aluminum, and a “through electrode TSV2 for a mark.” Ex. 1010, [0125]. The “rear bump 44 in which a rear mark is formed is

formed below the through electrode TSV2 for a mark.” *Id.* The rear bump 44 is circular, with the TSV penetrating through it, as shown from the bottom view of Figure 4F:



Ex. 1010, FIG. 4F. Ex. 2004, ¶ 78. The rear bump 44 is shown, as well as the TSV and insulating trench 29. *See* Ex. 1010, [0119] (“an insulating trench 29 is formed in a portion of the wiring through electrode.”). *Id.* also does not disclose the use of a via for the purpose of anchoring, but rather focuses on creating a rear mark that is more visible to the equipment used for fabricating stacks of vertically-connected

chips. *Id.* [0128]. Ex. 2004, ¶ 79.

IV. LEVEL OF ORDINARY SKILL IN THE ART

As Mr. Berg explains, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. Additional formal education (such as Master of Science degrees) would compensate for less technical experience and vice versa. Ex. 2004, ¶¶ 23-26.

Petitioner's proposed level of skill in the art – “at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems”—imposes a requirement of a master's degree. Pet., 23. As Mr. Berg explains, engineers working in this field, and implementing designs such as that described in the '826 Patent, typically have bachelor's degrees. Ex. 2004, ¶ 26. Such engineers are the target audience for the '826 Patent, and thus, a POSITA need not have a master's degree. *Id.*

V. CLAIM CONSTRUCTION

A. “disposed in at least one corner of a semiconductor substrate”

Patent Owner’s Construction	Petitioner’s Construction
“located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”	District Court: Indefinite This Proceeding: no construction necessary

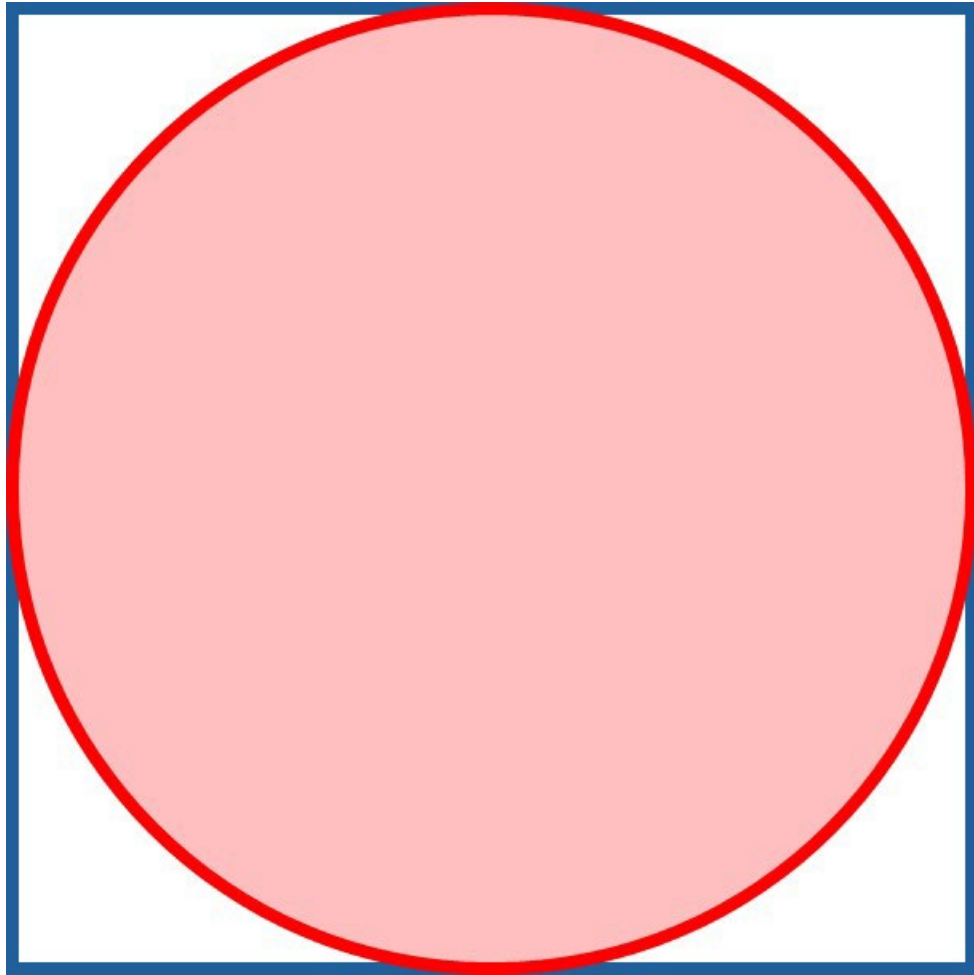
The Board should construe “disposed in at least one corner of a semiconductor substrate” as “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.” Ex. 2004, ¶¶ 34-56. While Petitioner states that no construction is necessary for this term, it argued that the term is indefinite in the District Court Litigation.

The ’826 Patent repeatedly explains that the purpose of locating the anchor vias in the corners of the die is to prevent the die from cracking due to stresses created during manufacturing. *See* ’826 Patent, Abstract; 1:14-38; 2:44-53; 6:1-4; 6:39-46. Ex. 2004, ¶¶ 36-42.

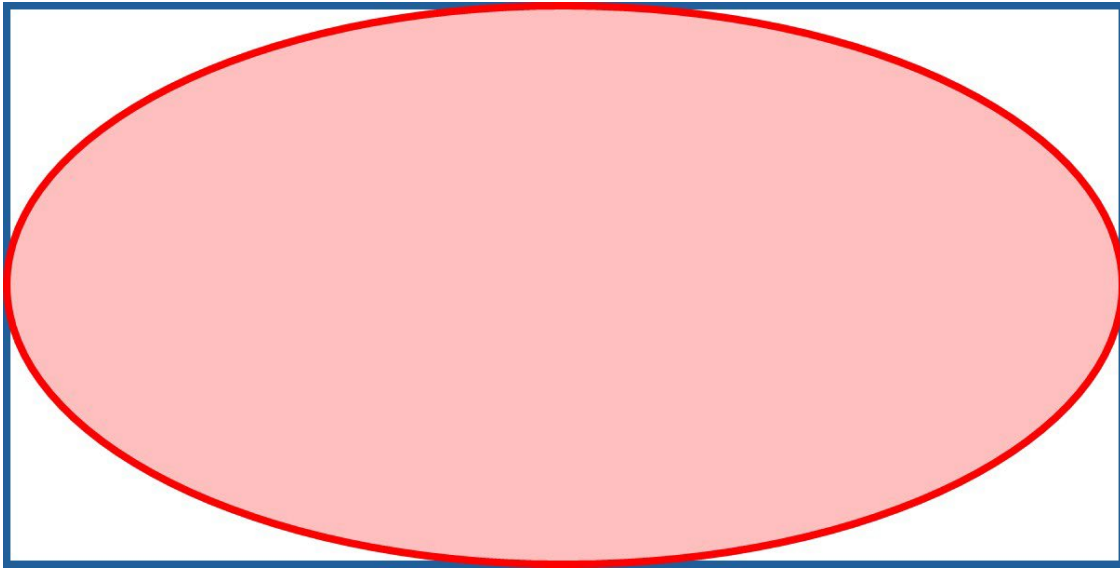
“Die Singulation Technologies for Advanced Packaging: A Critical Review” (Lei 2012) (Ex. 2006) explains that Metal/ILD delamination and peeling occur at die corners due to “the more severe stress state at die corners.” Ex. 2006 at 5. Lei describes several known die singulation technologies (pages 6-23), and discusses

stresses caused by die singulation in detail. *Id.* at 6-23. Rather than the anchor vias of the '826 Patent, Lei proposes the use of an “edge sealing ring” also known as a “guard ring” or “crack stop” that is built surrounding each die. *Id.* at 5. Ex. 2004, ¶ 45.

Lei also proposes some mathematics for calculating die strength, which the POSITA would have known to use in order to calculate how much force would cause a particular semiconductor die to crack at the corner. Ex. 2006 at 5-6. Particularly, Lei notes the calculation of die fracture strength using the 3PB tests of thin film silicon dies in the SEMI standard G86-0303 (where the die fracture strength is calculated as a derivation from linear beam theory), as well as the need for additional mathematics with respect to very thin silicon chips. *Id.* at 5. However, as Mr. Berg explains, engaging with these mathematics is unnecessary because the POSITA would have understood that something is located in the corner of a semiconductor die if it is located outside of a round or ovoid geometrical shape inscribed within the edges of the semiconductor die. Ex. 2004, ¶¶ 46-48. An example of this rounded geometrical shape would be a circle located inside a square semiconductor die:



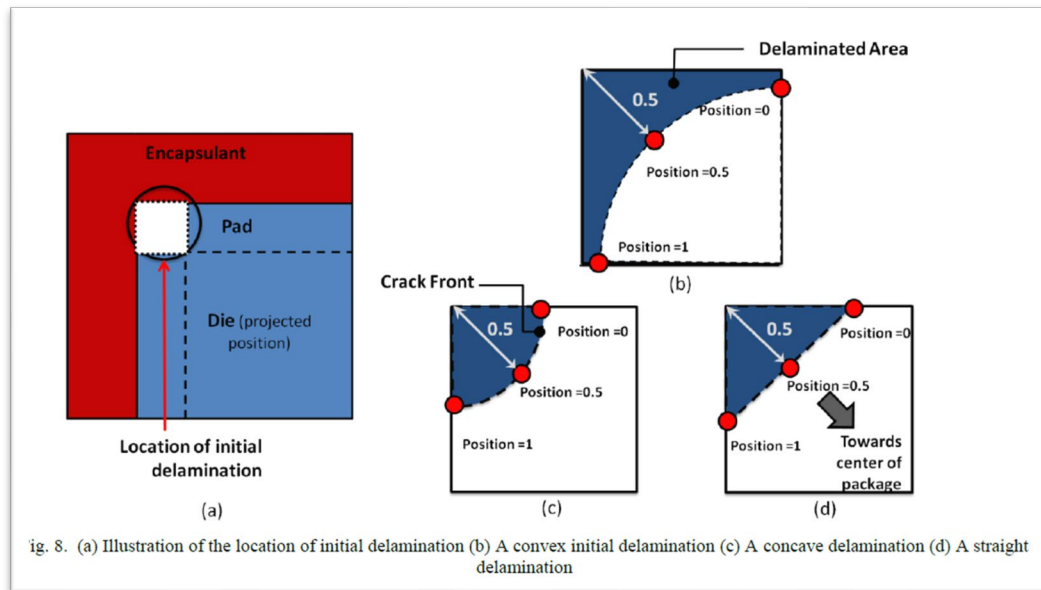
Another example is an oval inscribed within a rectangular semiconductor die with a 2:1 aspect ratio (common geometry for semiconductor dies:



Ex. 2004, ¶¶ 48-50.

Extrinsic evidence confirms that Patent Owner's construction was well-known and accepted at the time of the invention. For example, the paper entitled "3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages" (Ho et al., 2013) (Ex. 2007) performs a 3D finite element analysis to model corner delamination in semiconductor dies. "It was found that in 3D analysis, different shapes of initial delaminations result in similar trends in the propensity to delaminate from the corners. From the results of the 3D analyses of a package with an initial corner delamination, it was found that increasing the die size leads to an increase in ERR, and hence an increase in the likelihood of delamination from the corners of a package." Ex. 2007, 807. The Ho authors used fracture mechanics (used

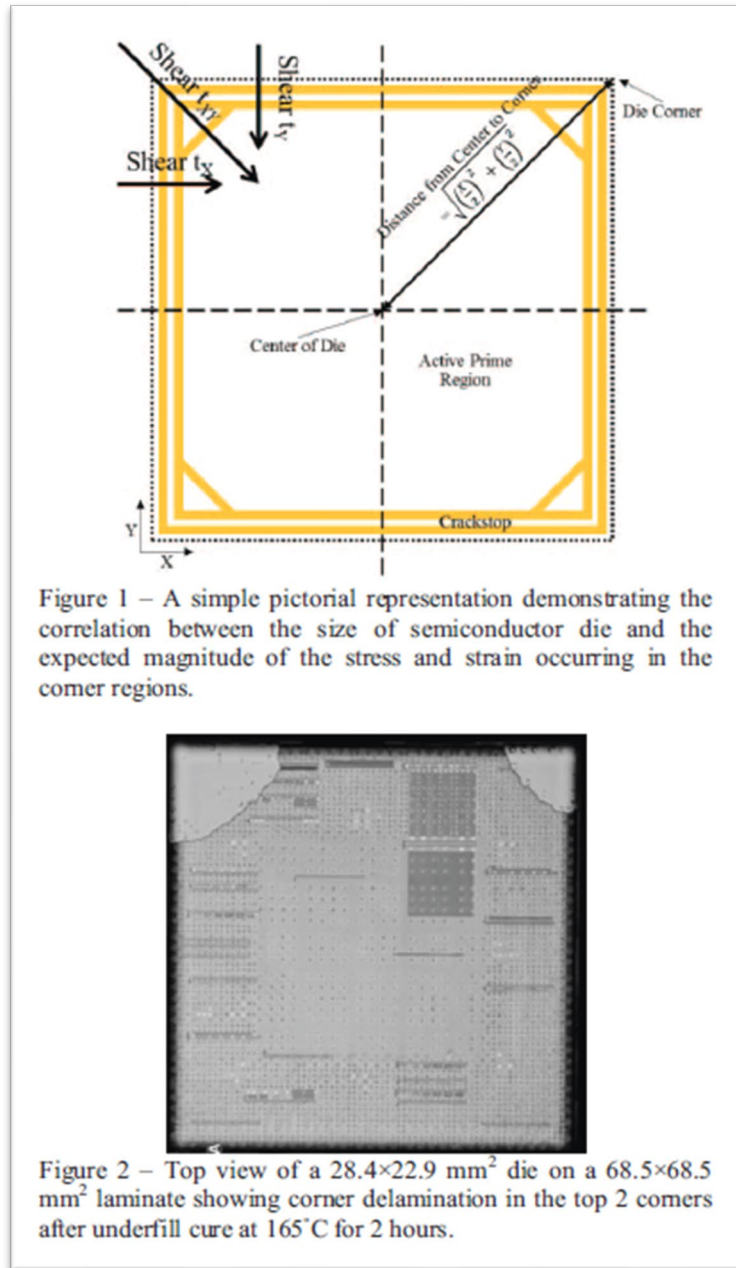
to evaluate the likelihood of delamination and crack propagation in a die) to calculate the strain energy release rate (ERR). The ERR is the rate at which potential energy decreases as a function of fracture surface area. The paper confirms that the die is most likely to fracture near corner edges, when 3D analysis, and not just 2D analysis, is used. Ex. 2004, ¶ 52.



Ex. 2007, 810; Ex. 2004, ¶ 52.

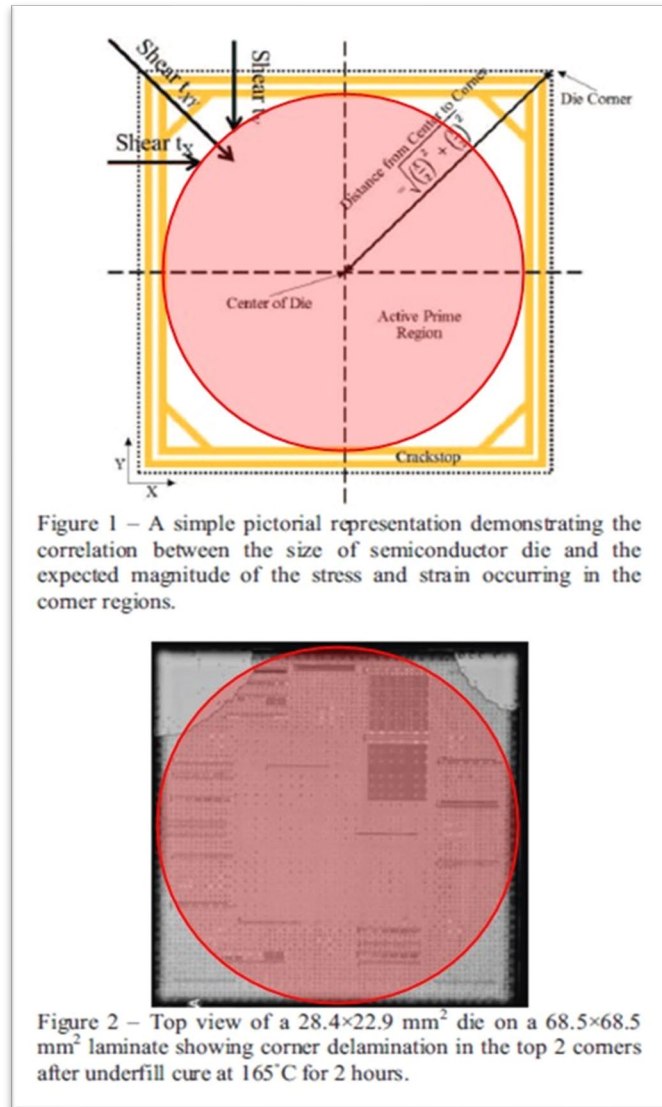
The paper “Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks” (Rabie et al., 2021) (Ex. 2008), although dated after the priority date of the ’826 Patent, provides additional confirmation as to understandings of the meaning of the “corner” of the semiconductor die. For example, Rabie notes that corner delamination is caused by

high shear forces, and discloses a pictorial representation and an actual image of a delaminated semiconductor die:



Ex. 2008, Figs. 1, 2. Ex. 2004, ¶ 53.

As Mr. Berg explains, Rabie utilizes corner in the same way as Patent Owner's construction. Ex. 2004, ¶¶ 54-55.



Ex. 2008, Figures 1 and 2 (annotated). Ex. 2004, ¶ 54.

As shown in Figure 2, the delamination on the top left of the semiconductor die is partially inside the circle and, therefore, the delamination is not completely in the corner. Ex. 2004, ¶ 55. However, a POSITA reading the '826 Patent would realize that an anchor via or other suitable delamination protection mechanism located within the corner would have prevented this delamination. *Id.*

Accordingly, based on the combination of the disclosures in the intrinsic record which clearly define the problem solved by the inventions in the '826 Patent, as well as a POSITA's knowledge regarding the location of the corner of a semiconductor die, confirms that the term “disposed in at least one corner of a semiconductor substrate” should be construed to mean “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.” Ex. 2004, ¶ 56.

B. “a backside metal layer on a bottom surface of said semiconductor substrate”

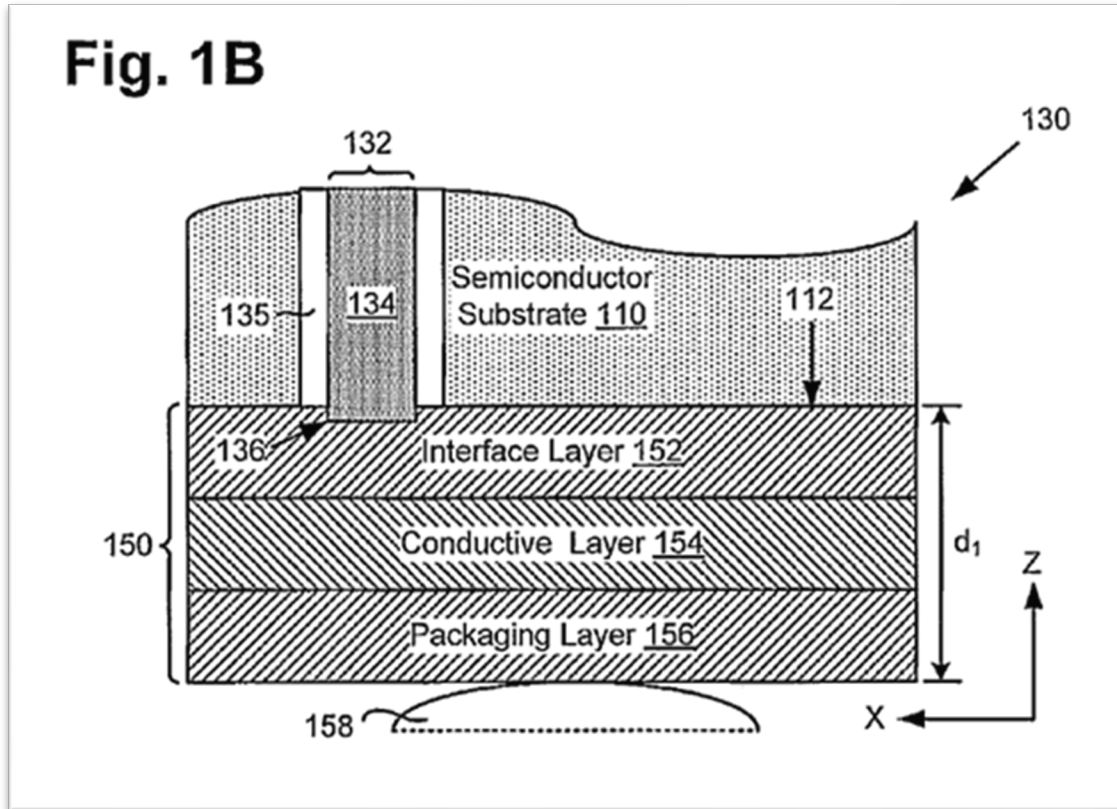
The Board should construe this term as “a backside metal layer in contact with a bottom surface of said semiconductor substrate.” This is the plain meaning of “on” as recited in the claims, and a POSITA, reading the claims in view of the specification, would understand that the claims require such contact. Ex. 2004, ¶ 57.

The claim language itself makes clear that the backside metal layer is in contact with the substrate by explaining that the backside metal layer is on the “bottom surface” of the substrate. A POSITA would understand that if the metal layer could be on the substrate but not in direct contact, then the use of “surface” would be irrelevant. *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950-51 (Fed. Cir. 2006) (rejecting construction that rendered claim terms meaningless and noting that “claims are interpreted with an eye toward giving effect to all terms in the claim”).

Moreover, Claims 9 and 19 draw a distinction between a layer “on” the bottom surface of the substrate, and a layer “overlying” the substrate. The use of two different terms would indicate to a POSITA that “overlying” and “on” have different scope. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (*en banc*) (“Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.”); *Nystrom v. TREX Co.*, 424 F.3d 1136, 1143 (Fed. Cir. 2005) (“When different words or phrases are used in separate claims, a difference in meaning is presumed.”). As a layer can overlie (or underlie) a substrate while not being in contact with its surface, a POSITA would understand that use of “on the bottom surface” in Claims 1 and 11 denotes direct contact. Ex. 2004, ¶ 59.

The specification confirms Patent Owner's construction. The specification explains that the purpose of the '826 Patent's invention is to improve the adhesion of a metal layer to a substrate. '826 Patent, 1:16-39, 1:40-46 ("The present disclosure is directed to anchor vias for improved backside metal adhesion *to a semiconductor substrate.*") (emphasis added). An example of a backside metal stack is "an interface layer [that] may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer." *Id.*, 1:27-30. A key problem the inventors sought to overcome was the reliance "on the adhesive qualities between the substrate and interface layer." *Id.*, 1:33-36. Failure of those qualities resulted in "the backside metal layer peeling from the semiconductor substrate." *Id.*, 1:36-39. Ex. 2004, ¶ 60.

To achieve that aim, the '826 Patent's anchor vias protrude into a metal layer directly in contact with the bottom surface of the substrate. This is shown, for example in Figure 1B, where the anchor vias reach only into the interface layer that is directly in contact with the substrate. Ex. 2004, ¶ 61.



As the specification explains, the interface layer is “deposited on bottom side 112 of semiconductor substrate.” ’826 Patent, 3:43-48. Critically, the conduction layer is “then formed *on interface layer 152.*” *Id.*, 3:51-53 (emphasis added). Similarly, the packaging layer is then “formed *on conduction layer 154.*” *Id.*, 3:53-55 (emphasis added). Each layer is in direct contact with the layer which it is “formed on.” Ex. 2004, ¶ 62. The specification’s description of the backside metal stack thus further confirms that the use of “on the bottom surface” requires direct contact. *Id.*, ¶ 63.

Accordingly, a POSITA would understand that “a backside metal layer on a bottom surface of said semiconductor substrate” means “a backside metal layer in contact with a bottom surface of said semiconductor substrate.”

C. Petitioner’s Claim Construction Argument

Petitioner presents one claim construction argument, which is that the method steps of Challenged Claim 11 should not be read to require steps [11b] and [11c] to be performed in their recited order. Pet. at 21-22. As discussed below, even assuming the broad interpretation of this claim as advanced by Petitioner, each of Petitioner’s grounds for anticipation and obviousness fail. Therefore, it is not necessary for the Board to construe Claim 11 or reach this issue in order to issue a final written decision.

VI. PETITIONER’S CITED ART DOES NOT ANTICIPATE OR RENDER OBVIOUS THE CHALLENGED CLAIMS

To anticipate a claimed invention, a prior art reference must “disclose all elements of the claim within the four corners of the document,” and it must “disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). “However, a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as

in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (C.C.P.A. 1962)).

The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence. *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1537 (Fed. Cir. 1983).

The Board has held that a failure to identify the differences between the claimed subject matter and the prior art is fatal to an obviousness challenge. *See, Apple, Inc. v. Contentguard Holdings, Inc.*, IPR2015-00355, Decision Denying Institution of *Inter Partes* Review, Paper 9 at 9-10 (P.T.A.B. June 26, 2015) (denying institution for failure to identify the differences between the claimed

subject matter and the prior art).

In arriving at an obviousness determination, the Board must sufficiently explain and support the conclusions that the prior art references disclose all the elements recited in the Challenged Claims and a relevant, skilled artisan not only could have made, but would have been motivated to combine all the prior art references in the way the patent claims and reasonably expected success. *Pers. Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). That is, even if all the claim elements are found across a number of references, an obviousness determination must consider whether a person of ordinary skill in the art would have the motivation to combine those references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016); *Los Angeles Biomedical Rsch. Inst. at Harbor-UCLA Med. Ctr. v. Eli Lilly & Co.*, 849 F.3d 1049, 1067 (Fed. Cir. 2017) (vacating and remanding an obviousness determination, in part, because the Board did not make factual finding as to whether there was an apparent reason to combine all three prior art references to achieve the claimed invention and whether a person of skill in the art would have had a reasonable expectation of success from such a combination). This combinability determination, as supported by an articulated motivation to combine, requires a plausible rationale as to why those

prior art references would have worked together. *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1335 (Fed. Cir. 2013). Absent some articulated rationale, a “common sense” finding is no different than the conclusory statement “would have been obvious.” *In re Van Os*, 844 F.3d 1359, 1361 (Fed. Cir. 2017). Of additional importance, “knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references” *Innogenetics, N.V. v. Abbott Lab’ys.*, 512 F.3d 1363, 1373 (Fed. Cir. 2008).

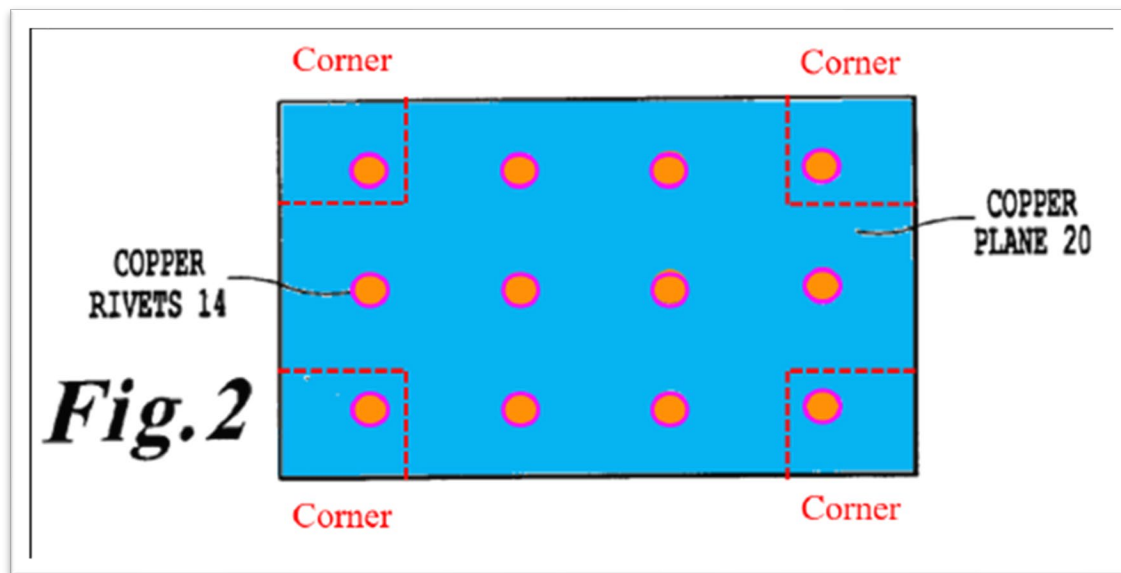
To demonstrate inherent obviousness, an inherent limitation must necessarily be present in the combination of references. *See Pers. Web Techs., LLC v. Apple, Inc.*, 917 F.3d 1376 (Fed. Cir. 2019); *LBT IP I LLC v. Apple Inc.*, No. 2022-1613, 2023 WL 3914920, at *3 (Fed. Cir. June 9, 2023). It is not enough to merely show that it is likely to be present. *Id.*

A. Ground 1: The Challenged Claims Are Not Anticipated By *Conn*

1. *Conn* Does Not Disclose an Anchor Via Disposed at the Corner of the Semiconductor Substrate Under the Plain Meaning

The Challenged Claims each require “at least one anchor via disposed in at least one corner of a semiconductor substrate.” ’826 Patent, Cls. 1, 11. *Conn* does not disclose this claim element. Instead, Petitioner invents this disclosure by

annotating Figure 2 of *Conn* to draw dotted lines delineating the “corner” of the copper plane and orienting them in such a way to enclose one copper rivet in each corner. Pet. at 29. This artificial annotation of Figure 2 is shown below:



Id. Ex. 2004, ¶¶ 80-81. As Dr. Thompson testified, the annotation was added by Petitioner counsel. Ex. 2009, Thompson Dep., 36:21-37:7.

Conn does not suggest that Fig. 2 represents any portion near the corner of a die. It merely states that “{t}he via conductors can be distributed relative to the conducting layer 20 in a pattern as shown for example in FIG. 2.” Ex. 1004, [0035]. Other than one reference to the corner of a single via, *Conn* does not use the term “corner” at all. *See id.*, [0054]. Ex. 2004, ¶ 81.

According to Petitioner, Figure 2 “shows the plurality of anchor vias (*see* copper rivets 14 in Figure 2) are “distributed relative to the conducting layer 20 in a pattern.” Pet. at 28 (quoting Ex. 1004 at [0035]). But describing that the anchor vias are distributed in “a pattern” does not disclose that the anchor vias are disposed at the corners. Petitioner also cites to its expert declaration, which merely parrots back the previous citations and states that “those skilled in the art seeing Figure 2 would understand that the depicted anchor via pattern is intended to repeat across the length and width directions of the conducting layer 20” and that this includes putting anchor vias in the corners. Ex. 1003 ¶ 83. Petitioner’s parrotting of the exact statement from the Petition, without additional analysis or support, is entitled to little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper No. 9, 15 (P.T.A.B. Aug. 24, 2022) (precedential) (expert statement that “merely repeats, verbatim, the conclusory assertion for which it is offered to support” without additional evidence or technical reasoning “is entitled to little weight”).

Conn is entirely silent as to the corners and edges of its semiconductor. For example, while *Conn* provides examples of distances between each via, it does not describe the distance between the vias and edges of the substrate. *See* Ex. 1004, [0035]; Ex. 2004, ¶ 83. *Conn* also does not disclose or suggest that each via shown

is an anchor via. It merely states that, for example, conducting layers are connected by “at least one via conductor 14, which acts as a rivet to hold the conducting layers 20 and 30 mechanically connected to the substrate. The conducting layers 20 and 30 can be connected by a plurality of via conductors 14 such that a stress caused by high changes in temperature in the main surfaces of the carrier substrate does not break the composite structure formed by the conducting layers and the via conductors.” Ex. 1004, [0038]. Ex. 2004, ¶ 84.

Conn does not discuss the corners because its anchor vias are used for a different purpose than those of the '826 Patent. The '826 Patent uses anchor vias to compensate for mechanical stresses occurring during die singulation. '826 Patent, 1:30-34. Ex. 2004, ¶ 85. *Conn*, however, is focused on stresses caused by thermal expansion, which is not localized to corners and edges. Ex. 1004, [0003] (“This invention relates to a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.”); [0005] (“[E]xtensive and repeated temperature changes cause fatigue of the package and the structure including the package.”); [0028] (“The anchor via can (for purposes of illustration) be considered a rivet formed in the carrier substrate

and in contact with the conducting layer 20 by which the conducting layer 20 maintains its structure under thermal stress.”); *id.* [0030]. Ex. 2004, ¶ 86.

A POSITA reading *Conn* would understand that it is silent, and therefore does not disclose, anchor vias in the corners. *Id.*, ¶ 87.

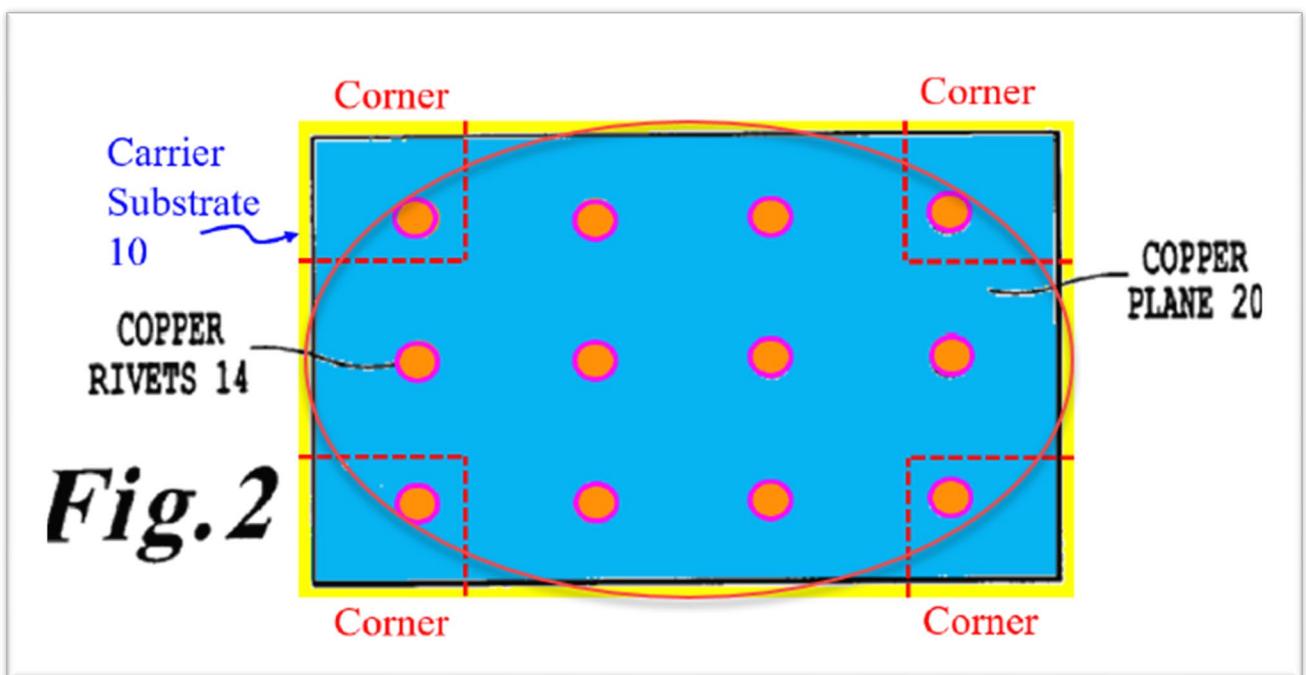
Petitioner’s analysis of the Figures in *Conn* also fails because it interprets dimensionality from an exemplary figure. Absent disclosure in the specification to the contrary, patent drawings cannot be used to show specific sizes of elements. *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000) (“The [patent] is devoid of any indication that the proportions of the groove and fins are drawn to scale. . . . Under our precedent . . . patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.”). The Petition makes no attempt to analyze the spacing or formatting the vias in relation to the size or shape of the conducting layer, and *Conn* contains multiple embodiments of different densities, sizes, and shapes. Ex. 1004 at [0035]-[0036], [0039].

Accordingly, *Conn* does not anticipate any claims.

2. *Conn* Does Not Disclose an Anchor Via Disposed at the Corner of the Semiconductor Substrate Under the Proper Construction

If the Board is inclined to consider Petitioner’s Figure-based argument, it still fails under the proper construction of “disposed in a corner...” Ex. 2004, ¶ 89. As discussed above, the proper construction of the term is “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.”

Applying that construction to Petitioner’s modified Figure 2 (Pet. 30, shows that all the shown copper rivets fall outside of the inscribed shape. Ex. 2004, ¶¶ 90-92.



Ex. 2004, ¶ 91-92.¹

Thus, even if the Board considers Petitioner’s Figure 2-based argument, it does not show anticipation.

3. Claim 9: *Conn* Does Not Disclose “wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate”

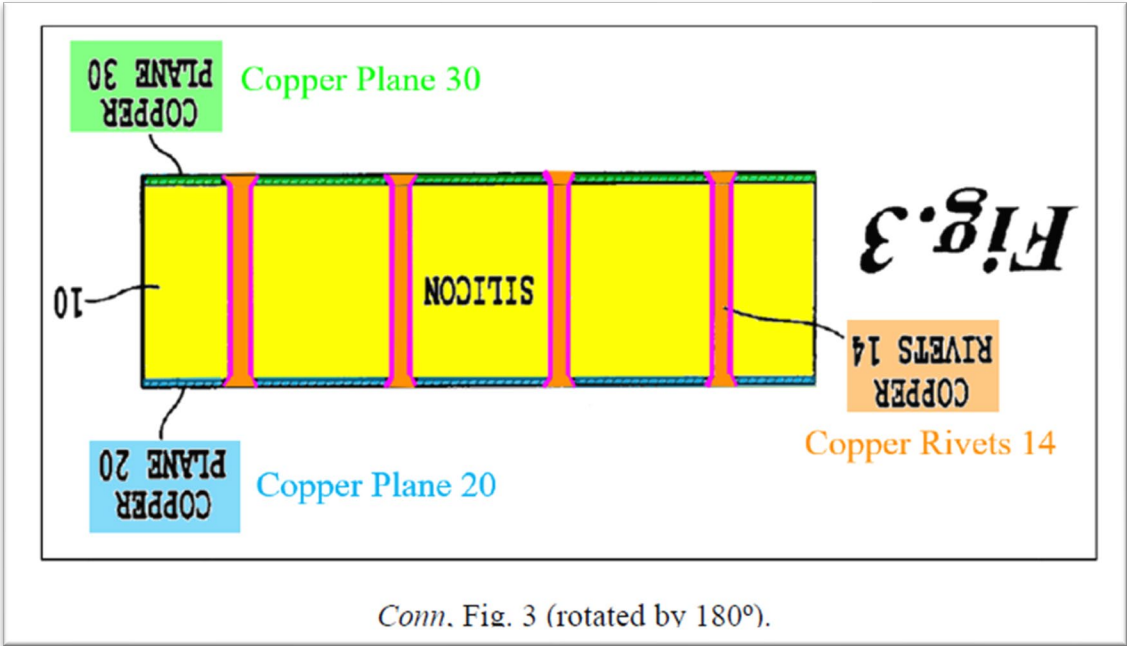
Claim 9 depends on Claim 1 and adds the limitation “wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.” “Said metal filler” refers back to “a metal filler within said at least one anchor via” recited in Claim 1, and is thus subject to all of Claim 1’s limitations. Limitation 1[d] of Claim 1 requires “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.” Read in conjunction, the metal filler must be bonded to metal layers on both sides of the substrate *and* not provide ground

¹ The magenta circles surrounding the vias were drawn by Petitioner outside the drawn circles shown in *Conn*. The orange filled circles show the *Conn* rivets. Ex. 2004, ¶ 93.

connection to one or more active devices. *Conn* does not disclose claim 9's metal filler. Ex. 2004, ¶¶ 95-97.

For its discussion of limitation 1[d], Petitioner relies on *Conn*'s bare statements that some of its anchor vias “do not reach the opposing second main surface of the carrier substrate” and that its via conductors “do not necessarily have to go all the way through the anchor vias.” Pet., 37 (quoting Ex. 1004, [0028]). These statements are the sum of Petitioner's argument. *See id.*

However, in its discussion of Claim 9, Petitioner relies on *Conn*'s Figure 3, which shows “another conducting layer 30” formed on the opposite side of the substrate. Pet., 43. Figure 3 shows the two conducting layers, and characterizes them as “copper plane[s].” Ex. 1004, Fig. 3.



Pet., 43.

On cross-examination, Petitioner's expert admitted that at least one side of the substrate would contain active devices connected to the copper plane. Ex. 2009 at 42:21-43:5; 47:2-15. Ex. 2004, ¶ 105. The other side would contain a ground plane or eventually connect to ground. Ex. 2009, 43:6-13; Ex. 2004, ¶ 103. By connecting the two copper planes, *Conn*'s anchor vias provide a ground connection to at least one of the active devices on the active side. *Id.*, ¶¶ 99-107. Those devices would be connected to the vias through the conducting layer or copper plane 30, and current would flow to ground through the vias and copper plane 20. *Id.*, ¶ 105. Indeed, *Conn* makes no disclosure that the conducting layers do not lead to active devices on one side and ground on the other; a POSITA would have no reason to think otherwise. *Id.*, ¶ 106. A POSITA would therefore understand that the Figure 3 conductors provide a ground connection. *Id.*, ¶ 107.

Petitioner, and its expert, made no effort to show that a POSITA would understand Fig. 3 vias as not providing a ground connection. Pet., 43. Instead, they simply relied on Fig. 1 and *Conn*'s accompanying discussion that the conductors shown in Fig. 1 need not reach the other side of the substrate. Pet. 37. Silence is not sufficient to show that Fig. 3's via conductors do not provide ground connection. *Intel. Bus. Mach. v. Iancu*, 759 Fed. App'x. 1002, 1011 (Fed. Cir. 2019) (holding

that silence is not sufficient to prove disclosure of negative limitation); *Snap Inc. v. Vaporstream, Inc.*, IPR2018-00416, 2019 WL 3504153, at *12 (P.T.A.B. Aug. 1, 2019) (silence in prior art not sufficient); *Google, Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01715, 2019 WL 4733640, at *8 (P.T.A.B. Sep. 27, 2019) (Petitioner’s failure to provide explanation of “concerning why a skilled artisan would have understood this absence of express disclosure to mean that pre-registering is not required” was insufficient to meet its burden).

Core Wireless is directly on point. There, the limitation at issue was “without pre-registering.” *Id.* Petitioner Google simply relied on the reference’s silence as to whether pre-registration was required. *Id.* The Board, citing *IBM*, explained that such silence was not sufficient. *Id.* The situation here is similar, except that Samsung did not even assert that *Conn*’s silence as to its Fig. 3 vias would lead a POSITA to understand them not to provide a ground connection.

Because Petitioner has failed to show that *Conn* discloses Claim 9’s required metal filler that is both “bonded to a metal layer overlying said semiconductor substrate contacts” and “does not provide ground connection to one or more active devices in said semiconductor substrate,” Claim 9 is not anticipated for this independent reason.

4. Claim 19: *Conn* Does Not Disclose “bonding said metal filler within said at least one anchor via to a metal layer overlying said semiconductor substrate”

Petitioner relies on its discussion of Claims 1 and 9 for its anticipation arguments relating to Claim 19. For the same reasons discussed above with respect to Claim 9, *Conn* does not disclose Claim 19’s metal filler. Accordingly, *Conn* does not anticipate Claim 19.

B. Grounds 2A and 2B: The Challenged Claims Are Not Rendered Obvious by *Conn* in View of the Knowledge of a POSA and/or AAPA

With respect to Claim 1, Ground 2A provides obviousness arguments for the limited purpose of overcoming alleged predicted arguments that *Conn* does not disclose “backside” or “active devices.” Pet. at 45. Dr. Thompson confirmed this limited scope on cross-examination. E.g., Ex. 2009, 51:22-52:5 (“Q. Right, and with respect to claim 1, that’s your use of knowledge of a POSITA. Just to make sure I understand the borders of this. A. For claim 1 I’m using knowledge of a POSITA with support from Wang to show that backside metal and active devices would be obvious elements to modify Conn with.”; *see also id.* 48:7-15; 50:4-13; 50:25-12; 51:13-21.

As to Claim 11, Petitioner provides the same obviousness arguments as for Claim 1, as well as arguments relating to any ordering of the Claim 11 steps. Pet., 49. Dr. Thompson confirmed this scope as well. Ex. 2009, 52:7-16.

For all other limitations of Claims 1 and 11, as well as all limitations of Claims 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19, Petitioner relies solely on its anticipation arguments. Pet., 51. Ex. 2009, 52:25-53:7.

Patent Owner's arguments under Ground 1 are not related to any lack of disclosure relating to "backside" or "active devices," nor to any ordering of steps in Claim 11. *See supra*. Accordingly, Petitioner's Ground 2A arguments do not remedy the deficiencies of Ground 1.

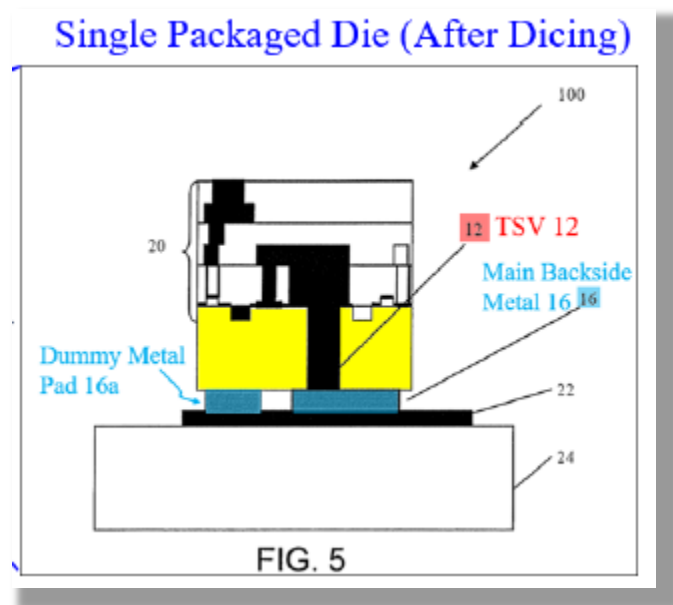
Petitioner's Ground 2B arguments are limited to dependent Claims 6 and 16. The Ground 1 deficiencies are not specific to those claims, and are not remedied by Petitioner's Ground 2B arguments.

Therefore, no claims are obvious under Grounds 2A or 2B.

C. Grounds 3A and 3B: The Challenged Claims Are Not Rendered Obvious by *Gambino* in View of *Conn* and/or *Ding*

1. The Combination of *Gambino* and *Conn* Does Not Result in the Claimed Invention Because the Resulting Via Conductor/Metal Filler Would Either Provide Ground Connection or Not Be Bonded to the Backside Metal Layer

Gambino discloses a through-silicon via (TSV) located in the middle of the semiconductor die, and a “metal pad 16a” that is located in the corner of the die. Petitioner’s annotated version of *Gambino*’s Figure 5 is shown below:



Ex. 1005, FIG. 5. *Gambino* explains that the TSV 12 shown in Figure 5 is in “mechanical and electrical communication,” with both the metal grounding plane 22 and wiring layers 20, which “can include vias, wires, and a host of different active

or passive devices.” *Id.*, [0030]. The metal pad 16a in Figure 5 is provided “at strategic locations on the dies 10 to provide mechanical support” and are “formed and placed such that the die 10 will sit flatly on the package substrate, during packaging.” *Id.* [0028]. The Petition states that “a POSA would have found it obvious to apply *Conn*’s teachings to create anchor vias in Gambino’s dummy metal pads 16a and/or main backside metal 16, to secure them to the substrate and prevent delamination during singulation.” Pet. at 60. The Petition contends that it would have been obvious to modify *Gambino* to bond *Conn*’s anchor vias to the dummy metal pad to arrive at the claimed invention. *Id.* While the Petitioner mentions connecting anchor vias to the main backside metal, the only identified backside metal layer is the dummy metal pads 16a. *Id.*, 67-70 (“Gambino/Conn satisfies [1c] because corner-located dummy metal pad(s) 16a is the claimed ‘backside metal layer.’”). Ex. 2004, ¶¶ 119-120.

Petitioner’s combination claims to use Gambino’s via process described at Gambino [0020] to create its proposed anchor vias. Pet., 64 (“the same process used for manufacturing Gambino’s electrical TSVs can be used to manufacture the anchor vias” (emphasis added) (citing Ex. 1003, ¶ 142)). Petitioner’s expert further states:

As discussed in § XII.A.2, Gambino’s manufacturing method (Gambino, [0020] – depositing the via metal before forming the

backside metal) can yield the same rivet-like anchor via structure contemplated by Conn—the resulting via conductors will form protruding portions bonded to the backside metal. Thus, the proposed combination does not require modification to Gambino’s existing manufacturing method.

Ex. 1003, ¶ 142.²

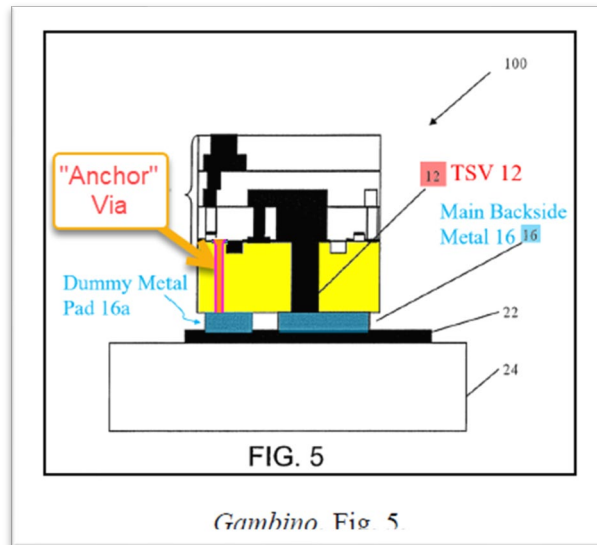
The proposed use of Gambino’s [0020] process is a key element of Petitioner’s obviousness arguments because it is the sole offered reason that making the vias would lead to a predictable result and would not require undue experimentation. Pet., 64.

Gambino creates its TSVs by etching holes from the *front side* of the substrate. Ex. 1005, [0020]. The TSVs extend partially through the unfinished die or substrate. *Id.* The via is then filled with metal from the front side. *Id.* After the via is filled, the backside is polished (or otherwise removed) to expose the filled via. *Id.* Ex. 2004, ¶121.

² Dr. Thompson refers to §XII.A.2 of his declaration. That section relates to Ground 2 and whether Claim 11 recites an order of the steps. Ex. 1003, ¶¶ 116 et seq. Assuming Dr. Thompson meant some part of §XIII.A, no portion discusses Gambino’s manufacturing method.

Utilizing Gambino's method to create *Conn* anchor vias would result in one of two outcomes, neither of which meet the claims. Either the anchor vias would be filled entirely, like Gambino's TSVs, or the anchor vias would not reach the backside metal layer. Ex. 2004, ¶¶ 122-123. This is because Gambino creates holes in the front side and fills them. Thus, any anchor via created using Gambino's process would be filled from its maximum depth to the surface of the front side. Ex. 1005, [0020]. Ex. 2004, ¶¶ 121-124.

If the anchor vias were filled entirely, they would provide a ground connection. Petitioner explains, that in its combination, the anchor vias would contact the dummy metal pads 16a. Pet., 67-70. Adding a filled anchor via to Gambino Figure 5 shows that the anchor via conductor would reach the wiring level and connect it to the ground plane 22. Mr. Berg has further annotated Figure 5 by adding an anchor via where Petitioner suggests. Ex. 2004, ¶ 124.



Ex. 2004, ¶ 124 (quoting Pet., 70) (further annotation added). *Gambino* explains that its dummy metal pad 16a is connected to the ground plane 22. Ex. 1005, [0030]. Thus, adding a filled anchor via would result in another of Gambino’s “grounded TSVs.” *Id.*, [0016]. A grounded TSV would provide a ground connection, either directly or indirectly, to an active device. *Id.*, [0030]. Ex. 2004, ¶ 125.

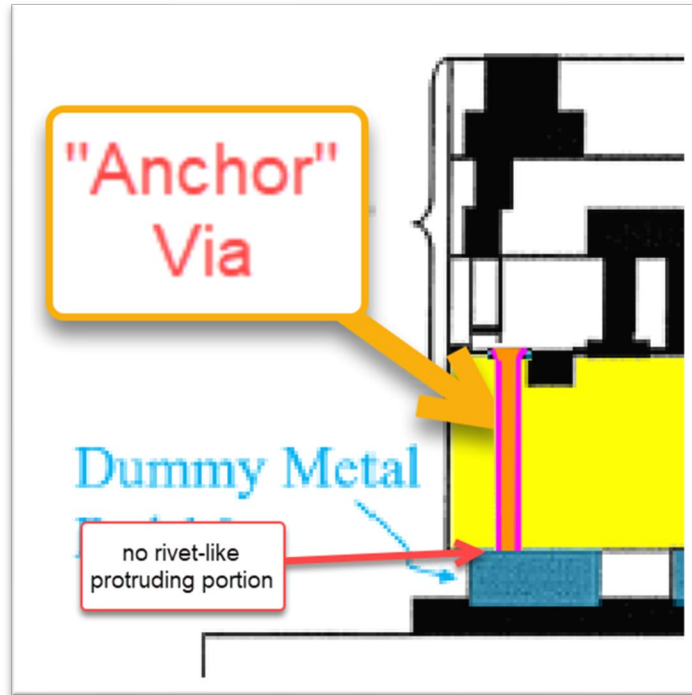
The Petition does not address this issue. With respect to limitation [1d], the Petition merely states:

Gambino/Conn satisfies [1d] because corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection, which means the anchor vias therein do not provide ground connection to active devices. *Gambino*, [0028], [0030]; Thompson, ¶151.

Pet., 70. Thompson merely parrots the same statement. Ex. 1003, ¶ 151.

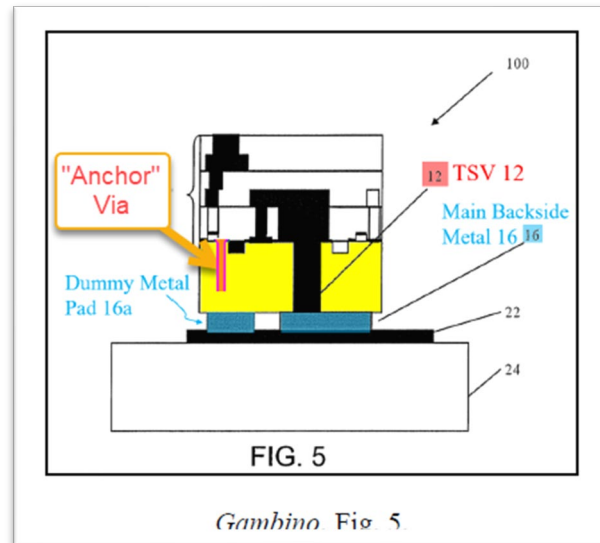
A POSITA, however, would recognize that the only reason the dummy metal pads 16a do not provide electrical connection is because they are not connected to any TSVs. Ex. 2004, ¶ 127; Ex. 1005, [0027] (“That is, the backside metal 16 does not entirely cover the dies 10; instead, the backside metal 16 covers the TSVs 12.”); *id.*, [0028], [0030]. Indeed, Figure 5 shows dummy metal pad 16a directly connected to the ground plane 22. Ex. 2004, ¶ 127. If the “anchor vias” reach the dummy metal pad, the pads would provide ground connections just as the electrical TSVs do. *Id.*, ¶ 127.

Moreover, Gambino’s process would not result in the filled vias including a “protruding portion extending from a backside of said semiconductor substrate” as claimed. Gambino’s process polishes the backside of the substrate until the via is exposed. Ex. 1005, [0020]. At that point, the conductors in the via are flush with the surface of the substrate. Thus, no portion of the conductor would protrude. Ex. 2004, ¶ 128.



Detail view of Annotated Fig. 5, *supra*. Ex. 2004, ¶ 128.

In the second case, the via would only be partially etched and would not reach the dummy metal pad, thus not forming an anchor via. Mr. Berg provides further annotations to Petitioner's annotated Figure 5 showing the result.



Ex. 2004, ¶ 129 (quoting Pet., 70) (further annotations added).

In this version, the “anchor” via conductor does not reach the backside surface and thus cannot meet limitations [1b] (requiring the filler to have a protruding portion extending from the backside surface) or [1c] (requiring the filler to be bonded to the backside metal layer). The proposed “anchor via” is also not an anchor via because it does not anchor anything. Ex. 2004, ¶ 130.

Petitioner makes no argument that it would be obvious to modify Gambino’s process. Indeed, as discussed above, using Gambino’s process unchanged is Petitioner’s primary evidence that the results would be predictable. Pet., 64.

To the extent Petitioner is allowed to argue it would be obvious to modify Gambino to etch the vias from the backside, Petitioner is mistaken. At the outset, Petitioner provides no evidence that such a modification would be feasible or within

the abilities of a POSITA. Instead, Petitioner argues that a POSITA would use Gambino's process unchanged. Pet., 64. Dr. Thompson makes the same statement. Ex. 1003, ¶ 142.

To build an unconnected “anchored” via in Gambino, a POSITA would, at least, need to add a 2nd via mask, 2nd etch process, a 2nd TSV fill process, and a 2nd CMP process step. Ex. 2004, ¶ 132. Such additional processing steps are not explained in either Conn or Gambino, and would add additional manufacturing costs to the die. *Id.*

Such a modification would require additional semiconductor manufacturing equipment and steps because such equipment cannot etch from two sides simultaneously; the die lays on a platen and, a mask is applied to the top of the die. Ex. 1005, [0020]; Ex. 1004, [0049]; Ex. 2004, ¶ 133.³ The top of the die and mask are then etched away, leaving a pattern in the substrate. *Id.* Ex. 2004, ¶ 133.

³ Conn's etching process is similar to Gambino's and similarly could not achieve a Conn/Gambino device that meets the claims. Ex. 2004, ¶ 133. Indeed, both Conn and Gambino use Bosch deep reactive ion etching. Ex. 1004, [0049]; Ex. 1005, [0020]. Ex. 2004, ¶133.

Modifying Gambino to etch the vias from the backside would require flipping the die in the middle of processing, thereby adding process steps and thus, process costs, as well as additional opportunities for defects, which would decrease yield and increase manufacturing costs. *Id.*, ¶ 134. Semiconductor dies are inherently sensitive to mechanical stresses, and flipping a die would subject it to additional stress and yield loss. *Id.* The necessary modifications are not within the knowledge of a POSITA, nor are they taught in the references at issue in this IPR. *Id.*, ¶ 133. A POSITA (under either Petitioner's or Patent Owner's definition) would not be capable of altering the process without numerous additional process steps, process costs, and risk to yield loss. *Id.* The results of these modifications would not be predictable to a POSITA; indeed, adding process steps to any semiconductor manufacturing process requires significant experimentation and testing. *Id.*, ¶ 134. Petitioner has provided no evidence that a POSITA would be motivated or able to make such modifications.

Accordingly, Gambino does not render any claim obvious.

2. The Remaining *Gambino/Conn/Ding* Combinations

Petitioner only relies on the combination of *Gambino*, *Conn*, and *Ding* in Ground 3B to attempt to render obvious Claims 10 and 20. Because, as discussed above, the combination of *Gambino* with *Conn* fails to teach the inventions of Claims 1 and 11, the addition of *Ding* to allegedly disclose dependent claims only does not cure the deficiency in the Petition with respect to Claims 1 and 11 and, therefore, Ground 3B also fails.

D. Ground 4: The Challenged Claims Are Not Anticipated by *Torii*

1. *Torii* Does Not Disclose a Metal Filler That Does Not Provide Ground Connection to Active Devices

The Petition improperly mixes embodiments in *Torii* to show this claim element, which is improper for an anticipation analysis. The Challenged Claims of the '826 Patent each require that the metal filler in the anchor vias is used *solely* for anchoring, and “does not provide ground connection to one or more active devices in said semiconductor substrate.” '826 Patent, Cls. 1, 11. The Petition states that “[t]he sub-TSV is a dummy . . . normally not used as a current pathway.” Pet. at 86 (citations omitted). The Petition places a period at the end of this quote, but fails to note that the quote disingenuously removed the second half of the sentence which

explicitly states that the sub-TSV can be used to conduct current, including static electricity, which of course is discharged to ground. The full, unedited quote is:

The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

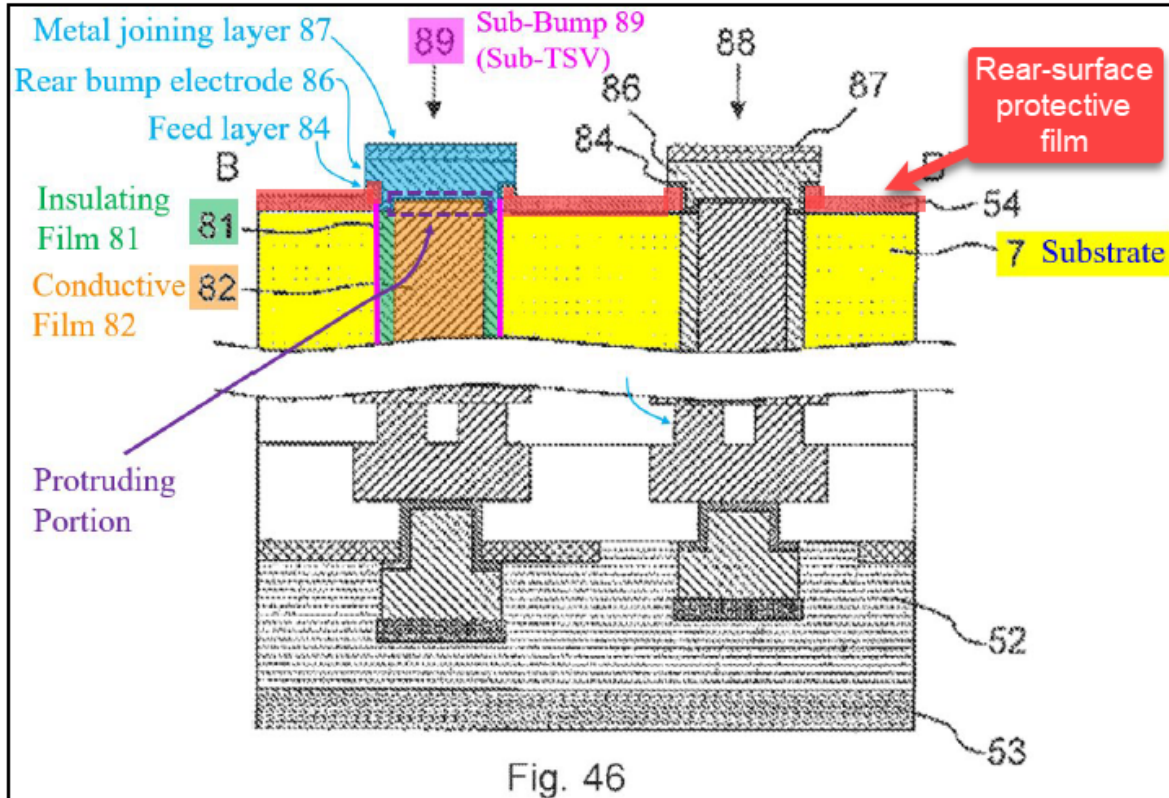
Ex. 1009, [0048]. A POSITA would therefore recognize that the sub-TSVs provide ground connections. Ex. 2004, ¶ 138. The requirement of the Challenged Claims that the anchor via not be used to provide ground connection to one or more active devices is directly contradicted by this disclosure in *Torii*, stating that the sub-TSV's can, in fact, be used as current pathways. *Id.*, ¶¶ 136-139. As the Board properly found in its institution decision, *Torii* cannot anticipate for this reason.

2. *Torii* Does Not Disclose a Backside Metal Layer

Each Challenged Claim of the '826 Patent requires “a backside metal layer on a bottom surface of said semiconductor substrate” '826 Patent, Cls. 1, 11. *Torii* does not disclose the required backside layer because Petitioner's identified backside metal layer—feed layer 84 (without or without rear bump electrode 86 and second metal joining layer 87)—is not on the bottom surface of the semiconductor substrate. Ex. 2004, ¶ 140.

As discussed above, the plain meaning of “on a bottom surface of said semiconductor substate” requires direct contact with the bottom surface.

To show this claim element, the Petition states that *Torii*’s “second feed layer 84 alone, or together with rear bump electrode 86 and second metal joining layer 87, constitutes the claimed ‘backside metal layer.’” Pet. at 84-85 (citing Ex. 1003 ¶ 180). As Mr. Berg shows, and Petitioner admits, there is a rear-surface protective film between the substrate and all portions of the alleged backside metal layer. *Torii*, [0100]; Pet., 84 n.12; Ex. 2004, ¶¶ 142-143.



Ex. 2004, ¶ 142 (quoting Pet., 83) (additional annotation added).

Thus, the structure identified as the backside layer (feed layer 84 alone or in combination with 86 and 87) by Petitioner is not “on a bottom surface of said semiconductor substrate,” because there is an additional layer in between the substrate and layer 84. *Torii* discloses that “Rear-surface protective film 54 is formed on the entire rear surface (FIG. 40), and silicon oxide film 83 is further formed on the protective film (FIG. 41).” Ex. 1009, [0100]. Figure 46 cited by Petitioner and annotated above also clearly shows the protective film 54 between the semiconductor substrate and what Petitioner claims is the backside metal layer. Petitioner’s expert claims that “the shoulder region results from a portion of the rear-surface protective film 54 formed on the sidewall of the insulating film 81” and “[t]hus, the shoulder region is not on the sub-TSV, but rather it is on the substrate surface.” Ex. 1003 ¶ 179. This is incorrect, as even Petitioner’s expert admits that the shoulder region never touches the semiconductor substrate.

Petitioner’s only response is to argue that “the plain and ordinary meaning of ‘on’ does not require direct contact, so the shoulder region is ‘on’ the substrate surface, as claimed.” (citing *AFG Indus., Inc. v. Cardinal IG Co.*, 239 F.3d 1239, 1251 (Fed. Cir. 2001)). Petitioner’s argument fails for multiple reasons. The cited

case did not hold that any term reciting “on” does not require direct contact. Instead, having determined that the claims at issue in that case allowed for interlayers between layers, the Court held that layers “formed on” prior layers need not be directly on the prior layer. *AFG*, 239 F.3d at 1251. That is not the case here. In any event, a claim construction holding relating to a different, unrelated patent with a different specification, inventors, and claim language is hardly relevant here. Indeed, relying on *AFG* over the intrinsic record, as Petitioner urges, would violate the Federal Circuit’s directive that “claims “must be read in view of the specification, of which they are a part.” *Phillips*, 415 F.3d at 1315.

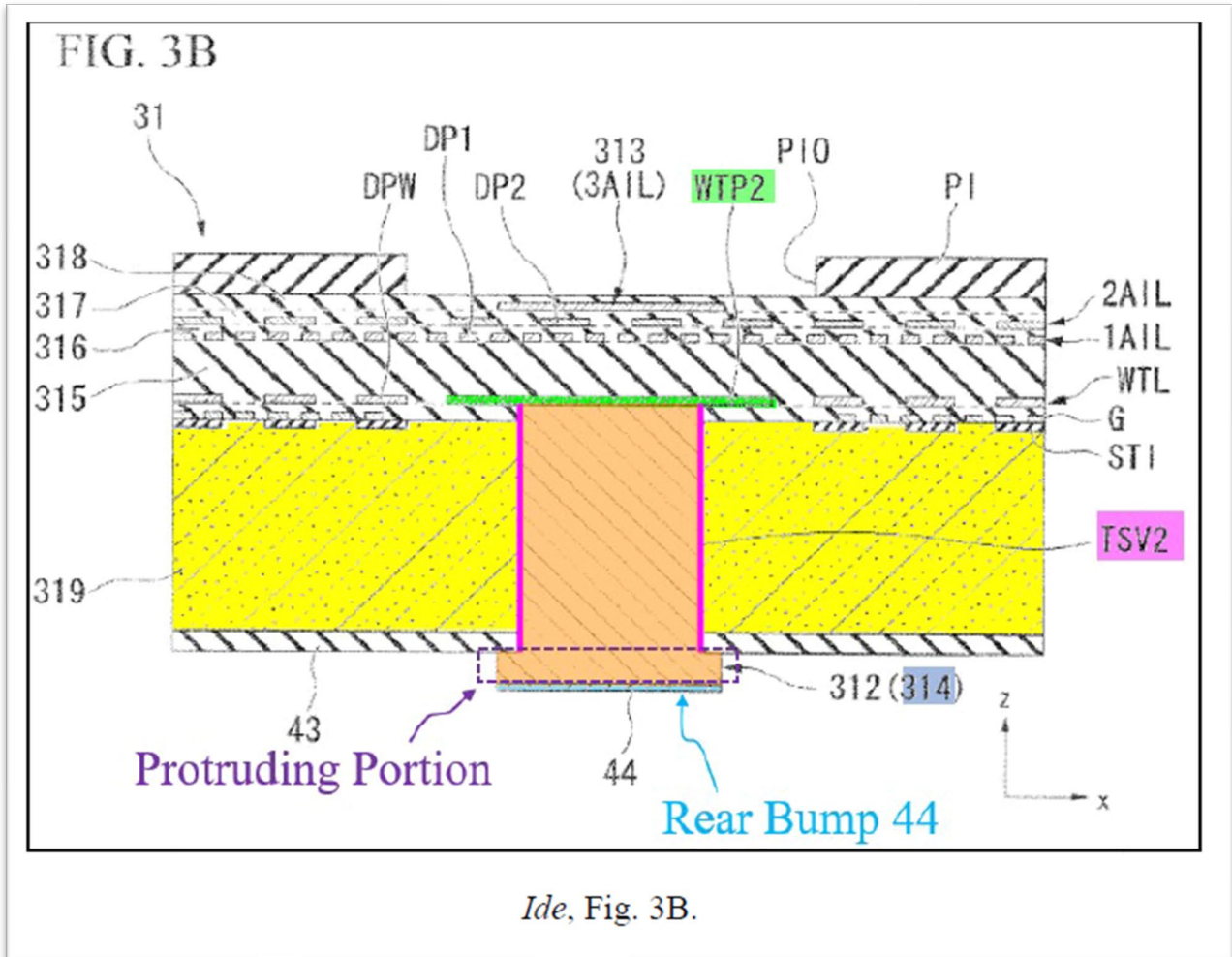
The claims here also specifically recite that the backside layer is on “a bottom *surface*” of the substrate. In *AFG*, the claims simply recited “formed on the substrate” or “formed on” a layer. 239 F.3d at 1243. By including “surface,” the drafters made clear that the backside metal layer must be directly on the substrate.

Accordingly, the Petition does not show that *Torii* anticipates “a backside metal layer on a bottom surface of said semiconductor substrate” ’826 Patent, Cls. 1, 11.

E. Ground 5: *Ide* Does Not Anticipate the Challenged Claims

1. *Ide* Does Not Disclose a Backside Metal Layer on a Bottom Surface of a Semiconductor Substrate

Each Challenged Claim of the '826 Patent requires “a backside metal layer on a bottom surface of said semiconductor substrate” '826 Patent, Cls. 1, 11. *Ide* does not disclose the required backside layer; instead, like *Torii* above, Petitioner’s identified metal layer is not on the bottom surface of the substrate, but on an intervening layer. Therefore, *Ide* does not disclose this claim element. Ex. 2004, ¶¶ 145-148. The Petition annotates *Ide*’s Figure 3B as below, with “Rear Bump 44” allegedly satisfying the claimed “backside metal layer”:



Pet. at 94-95. As with *Torii*, the Petition notes in a footnote that there is an “intervening rear insulating layer 43 and rear bump electrode 312” between the copper fill (annotated in orange) and the rear bump 44 (annotated in blue). Pet. at 94 n.15. As discussed above, the plain meaning of “on the bottom surface” requires direct contact between the substrate 319 and the rear bump 44 that Petitioner claims is the “backside metal layer.” Ex. 2004, ¶¶ 147-148. Accordingly, Ide’s backside

metal layer is not “on a bottom surface of said semiconductor substrate” and, therefore, *Ide* does not anticipate Claims 1 or 11.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding all Challenged Claims not shown to be unpatentable.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S RESPONSE specified in 37 C.F.R. § 42.24 has 9,472 words in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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