

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,245,826
Filing Date: January 27, 2014
Issue Date: January 26, 2016

Inventors: Hadi Jebory, David J. Howard, and Scott B. Stetson
Title: ANCHOR VIAS FOR IMPROVED BACKSIDE METAL
ADHESION TO SEMICONDUCTOR SUBSTRATE

DECLARATION OF JOHN BERG

Case No. IPR2024-01405

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I, John Berg, declare as follows:

I. INTRODUCTION

1. I am over eighteen years of age and I would be competent to testify as to the matters set forth herein if I am called upon to do so.

2. I have been retained by Fabricant LLP, counsel for the Patent Owner Harbor Island Dynamic LLC (hereinafter referred to as “HID” or “Patent Owner”), to review U.S. Patent No. 9,245,826 (the “’826 Patent”) entitled ANCHOR VIAS FOR IMPROVED BACKSIDE METAL ADHESION TO SEMICONDUCTOR SUBSTRATE, and to provide my technical review, analysis, insights, and opinions regarding the ’826 Patent in view of the prior art cited by Petitioners Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung” or “Petitioner”). I submit this Declaration in support of Patent Owner’s Response in this IPR proceeding. I have personal knowledge of the matters stated herein and would be competent to testify to them if required.

II. BACKGROUND AND QUALIFICATIONS

3. This section summarizes my career history, education, publications, and other relevant qualifications. My full *curriculum vitae* (“CV”) is included as **Exhibit 2005**.

4. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980. My current work focuses on CMOS circuit design, simulation, modeling, and processing.

5. I am currently an expert consultant in semiconductor design and manufacturing. Since 2010, I have performed this work as a Principal at Berg-Attenborough, Inc., a consulting firm that provides technical consulting and expert witness services to semiconductor companies and law firms. My work as an expert consultant has included developing advanced CMOS processes and multi-chip modules that incorporate logic circuits using SOI, memory devices such as dynamic random-access memory (“DRAM”) and flash memory, as well as performing device analysis and testing using scanning electron microscope (“SEM”) and transmission electron microscopy (“TEM”) technology. In addition to my work as an expert consultant, I have over 35 years of experience as an executive and as an engineer in the semiconductor industry. I obtained a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980, and now I am focusing on analog CMOS circuit design, simulation, modeling, and processing.

6. Prior to Transfer Devices, I was a Managing Director at Cypress Semiconductor, where I managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, I was Vice President of Technology Development at Zilog, where I managed both technology

development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier.

7. Because of my background, training, and experience, I am qualified as an expert to opine on the issues with which I have been tasked. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, Ex. 2005.

8. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

III. COMPENSATION

9. My compensation for time worked on this proceeding is not dependent on any issues related to the '826 Patent, the outcome of this proceeding, or the substance of my opinions. My compensation for time worked on this proceeding is at my customary rate of \$560 per hour. I have no financial interest in, or affiliation with, the Patent Owner or any of the real parties in interest.

IV. LEGAL PRINCIPLES

A. Claim Construction

10. I understand that claim terms should be given their ordinary and

customary meaning within the context of the patent in which the terms are used, *i.e.*, the meaning that the term would have to a person of ordinary skill in the art (“POSITA”) in question at the time of the invention in light of what the patent teaches, unless it appears that the inventors were using them to mean something else. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as his/her own lexicographer (*i.e.*, provided special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope).

11. I understand that a POSITA is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but also in the context of the entire patent, including the specification and the prosecution history. The prosecution file history provides evidence of how both the Patent Office and the inventors understood the terms of the patent, particularly in light of what was known in the prior art. Further, where the specification describes a claim term broadly, arguments and amendments made during prosecution may require a narrower interpretation. For these reasons, the words of the claim must be interpreted in view of, and be consistent with, the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of

what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

12. I understand that, to determine how a POSITA would have understood a claim term, one should look to those sources available that show what a POSITA would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that one looks primarily to the intrinsic patent evidence, but extrinsic evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

13. Additionally, the context in which a term is used in the Asserted Claim can be highly instructive. Likewise, other claims of the patent in question, both asserted and not asserted, can inform the meaning of a claim term. For example, because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims. Differences among claims can also be a useful guide in understanding the meaning of particular claim terms.

14. I understand that, while intrinsic evidence is of primary importance, extrinsic evidence, *e.g.*, all evidence external to the patent and prosecution history,

including expert and inventor testimony, dictionaries, and learned treatises, can also be considered. For example, technical dictionaries may help one better understand the underlying technology and the way in which one of skill in the art might use the claim terms. Extrinsic evidence should not be considered, however, divorced from the context of the intrinsic evidence. Evidence beyond the patent specification, prosecution history, and other claims in the patent should not be relied upon unless the claim language is ambiguous in light of these intrinsic sources. Furthermore, while extrinsic evidence can shed useful light on the relevant art, I understand that it is less significant than the intrinsic record in determining the legally operative meaning of claim language.

B. Anticipation

15. I understand that to anticipate a claim, a prior art reference must disclose all elements of the claim within the four corners of the document, and it must disclose those elements arranged as in the claim. I understand that a reference may anticipate even if it does not expressly disclose all the elements if a POSITA reading the reference would at once envisage the claimed arrangement or combination.

16. I understand that if a reference fails to disclose even one element, it does not anticipate that claim. I understand that references that must be modified to disclose a claim element do not anticipate that claim.

C. Obviousness

17. I understand that a patent claim is unpatentable as “obvious” if the subject matter of the claim as a whole would have been obvious to a person of ordinary skill in the art (POSITA) as of the time of the invention at issue.

18. I understand that the question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) so-called secondary considerations where in evidence.

19. I further understand that the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

V. MATERIALS CONSIDERED

20. In providing my technical review, analysis, insights, and opinions, I have considered the '826 Patent and its prosecution history.

21. I have also considered the Petition filed by the Petitioner in this proceeding and the relevant exhibits relied on by Petitioner, including the expert declaration submitted by Scott E. Thompson, Ph.D. I have also reviewed the transcript of the deposition of Dr. Thompson, dated June 9, 2025 (“Ex. 2009”).

22. I have also considered my own experience and knowledge, as discussed above, and described more fully in my CV, in areas including semiconductor design, manufacturing, and other related technologies.

VI. LEVEL OF ORDINARY SKILL IN THE ART

23. It is my understanding that I must address the issues set forth in this Declaration, from the viewpoint of a POSITA at the time of the invention to which the Asserted Patents pertain.

24. I understand that this hypothetical POSITA is considered to have the normal skills of a person in a certain technical field. I understand that factors that may be considered in determining the level of ordinary skill in the art include: (1) the education level of the inventor; (2) the types of problems encountered in the art; (3) the prior art solutions to those problems; (4) rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the education level of active workers in the field.

25. Considering the above factors, in my opinion, a POSITA would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field; and (2) at least two years of industry experience in semiconductor design and/or fabrication. I also agree that a person could also have qualified as a POSITA with some combination of (1) more formal education (such as Master of Science degrees) and less technical experience, or

(2) less formal education and more technical or professional experience in the fields listed above.

26. I understand that Dr. Thompson has opined that a POSITA would have at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems. Ex. 1003, ¶ 73. While our contentions are similar, I disagree that a master's degree represents the ordinary level of skill. The '826 Patent is directed to an audience of engineers working to implement manufacturing processes. In the industry, it is typical for such engineers to have a bachelor's degree. Indeed, I myself implemented such processes with a bachelor's degree.

27. I understand that the '826 Patent is entitled to a March 11, 2013, priority date, and that is the relevant time period from which a POSITA would evaluate its disclosure and any prior art.

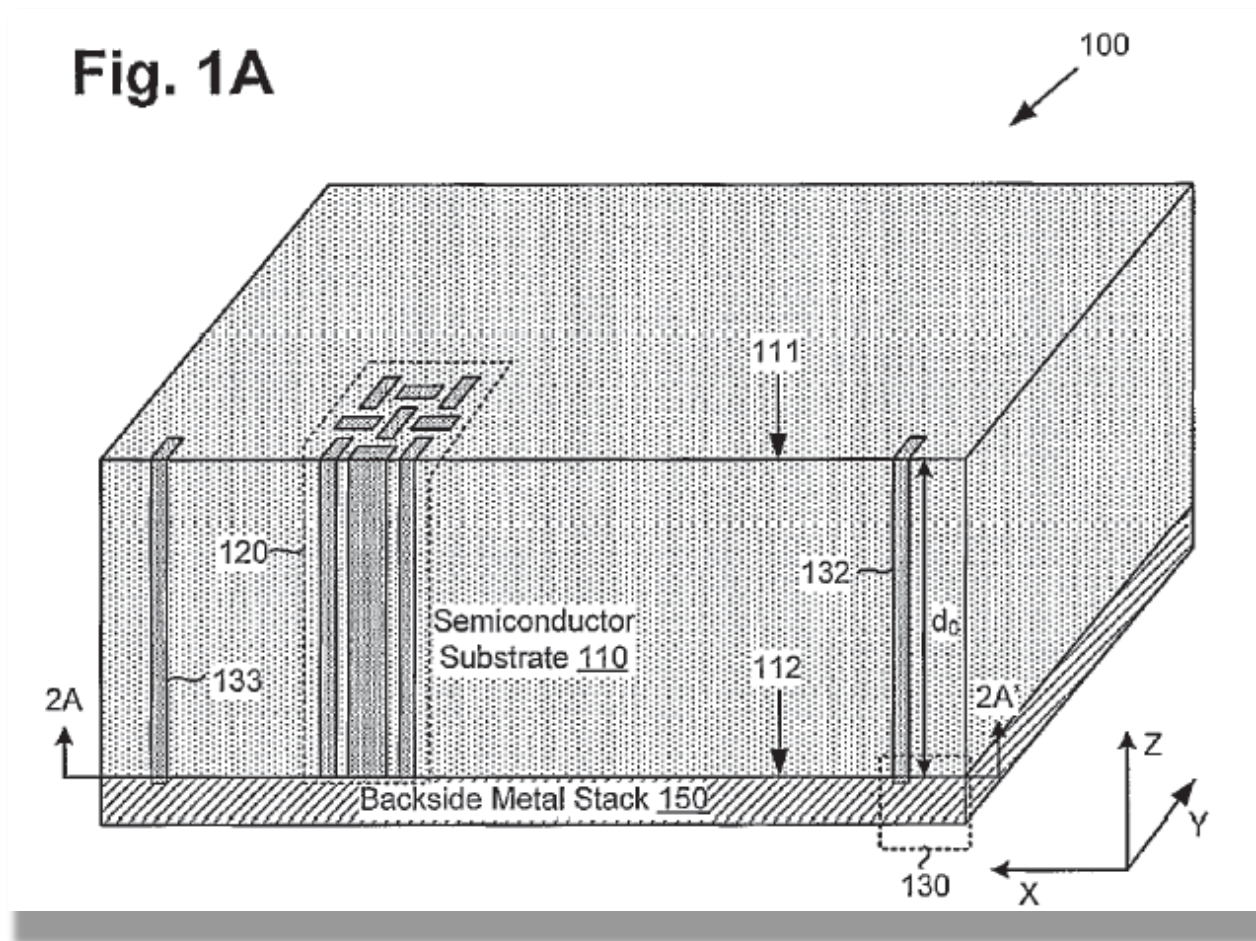
28. My qualifications and experience exceed those of a POSITA, under both my and Dr. Thompson's opinions. Nonetheless, my analysis and opinions herein regarding the Asserted Patent are given from the perspective of a POSITA.

VII. THE '826 PATENT INVENTION

29. The '826 Patent describes and claims an improvement in semiconductor design. More specifically, the invention relates to "anchor vias for improved backside metal adhesion to a semiconductor substrate." '826 Patent, 1:42-

46. The '826 Patent explains that prior art systems attached backside metal layers to semiconductor substrates using an adhesive. *Id.*, 1:36-38. This resulted in “unacceptably low yields . . . due to the backside metal layer peeling from the semiconductor substrate.” *Id.* As the specification explains, this is because “fabrication procedures such as semiconductor die singulation and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die.” *Id.*, 1:30-34.

30. The invention of the '826 Patent solves this problem by placing one or more through-silicon vias, called an “anchor via,” in the corner of the semiconductor die where these stresses are the greatest, and using the anchor vias “to improve backside metal adhesion.” *Id.* 2:44-47. Figures 1A and 1B of the '826 Patent, reproduced below, are exemplary:

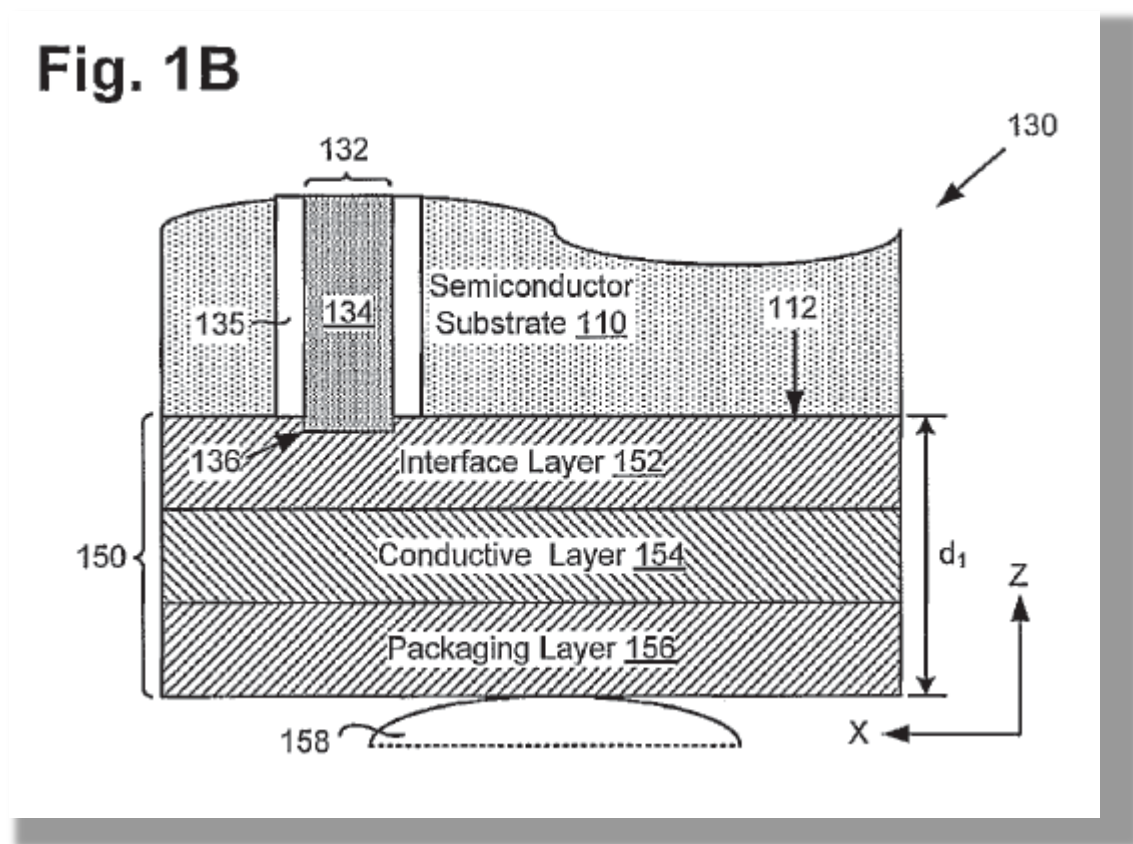


'826 Patent, FIG. 1A.

31. In Figure 1A, the '826 Patent discloses two anchor vias, 132 and 133, which are formed in the semiconductor substrate in “a peripheral region,” as well as a group of vias 120 which are not anchor vias, but rather are formed “in a core region of semiconductor substrate 110.” *Id.*, 3:2-5. The core vias 120 “provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110.” *Id.*, 3:5-11. One example is

given of an active device that is grounded using the core vias, which is “the emitters of bipolar transistors.” *Id.*

32. The anchor vias, on the other hand, do not provide ground connection but “instead provide [] physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150.” *Id.* 3:12-17. The bottom of an anchor via 132 is shown below in Figure 1B:



'826 Patent, FIG. 1B.

This anchor via contains a protrusion 136 that extends into the metal layer, “such that when interface layer 152 is deposited on bottom side 112 of

semiconductor substrate 110, the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond.” *Id.* 3:43-48

VIII. CLAIM CONSTRUCTION

A. “disposed in at least one corner of a semiconductor substrate”

33. I understand that Petitioner contends that this term requires no construction, while Patent Owner contends that it should be construed to mean “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”. I agree with Patent Owner’s proposed construction.

34. Claim 1 of the ’826 Patent recites:

1. A structure comprising:

at least one anchor via disposed in at least one corner of a semiconductor substrate;

a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

35. The specification of the ’826 Patent also describes the use of an anchor

via, as well as the specific placement of one or more anchor vias in the corner of the semiconductor substrate. For example, the specification discusses that “fabrication procedures, such as semiconductor die singulation, and pick-and-place processes subject the semiconductor substrate to very high stresses, especially near the edges and/or corners of the die. Because adhesion of the backside metal stack to the substrate is almost entirely dependent on the adhesive qualities between the substrate and the interface layer, unacceptably low yields are often achieved during fabrication due to the backside metal layer peeling from the semiconductor substrate.” ’826 Patent, 1:24-38.

36. Because conventional adhesion techniques cannot stand up to the stresses caused by these fabrication processes at the corner of the die, the ’826 Patent proposes that anchor vias be placed at the corners of the die. An example of two of these anchor vias in two corners of a die is shown in Figure 1A of the ’826 Patent, with the vias being labeled as 132 and 133, respectively:

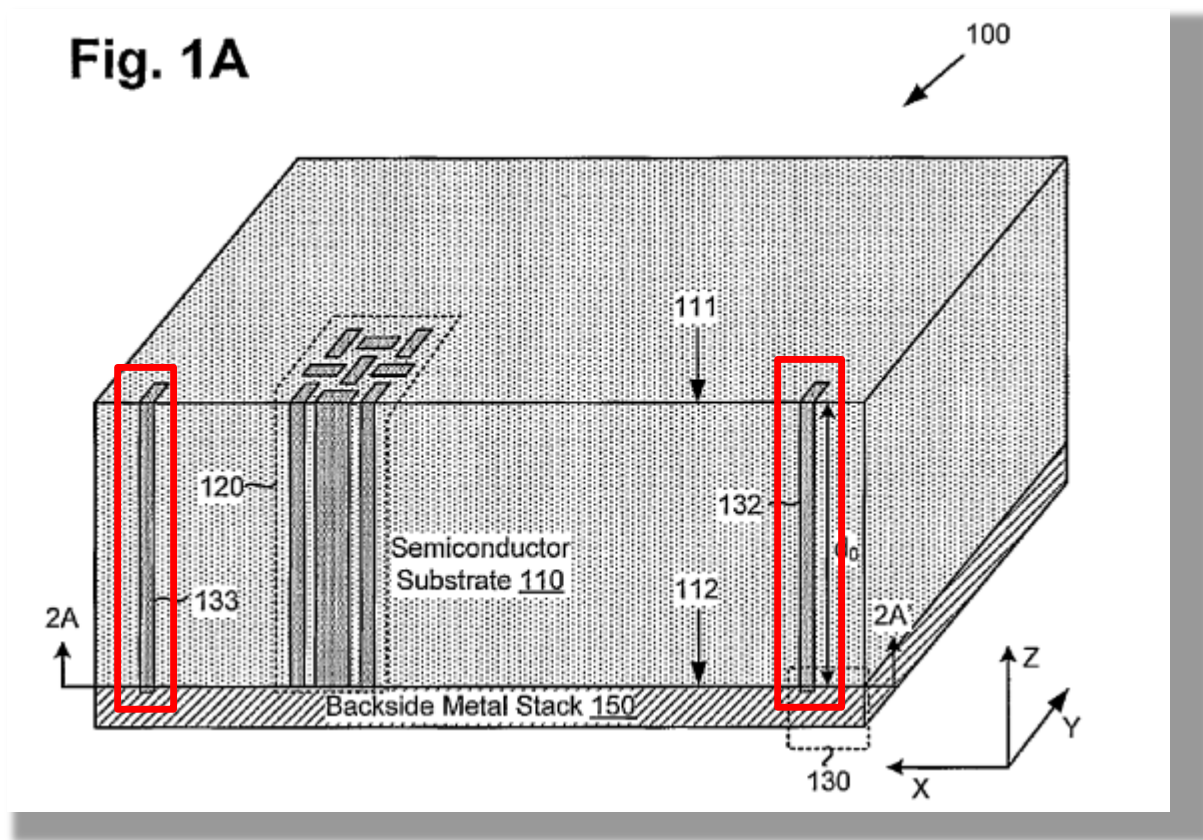


Figure 1A, annotated

37. Figure 3A of the '826 Patent shows a top view of the semiconductor die (including the dicing street which is removed during semiconductor singulation), and notes that in this Figure the cluster of anchor vias 330 is fabricated “proximate to a corner of semiconductor substrate 310 in order to prevent the backside metal stack from peeling at the corners of the die.” '826 Patent, 6:19-25. Figure 3A is reproduced below:

Fig. 3A

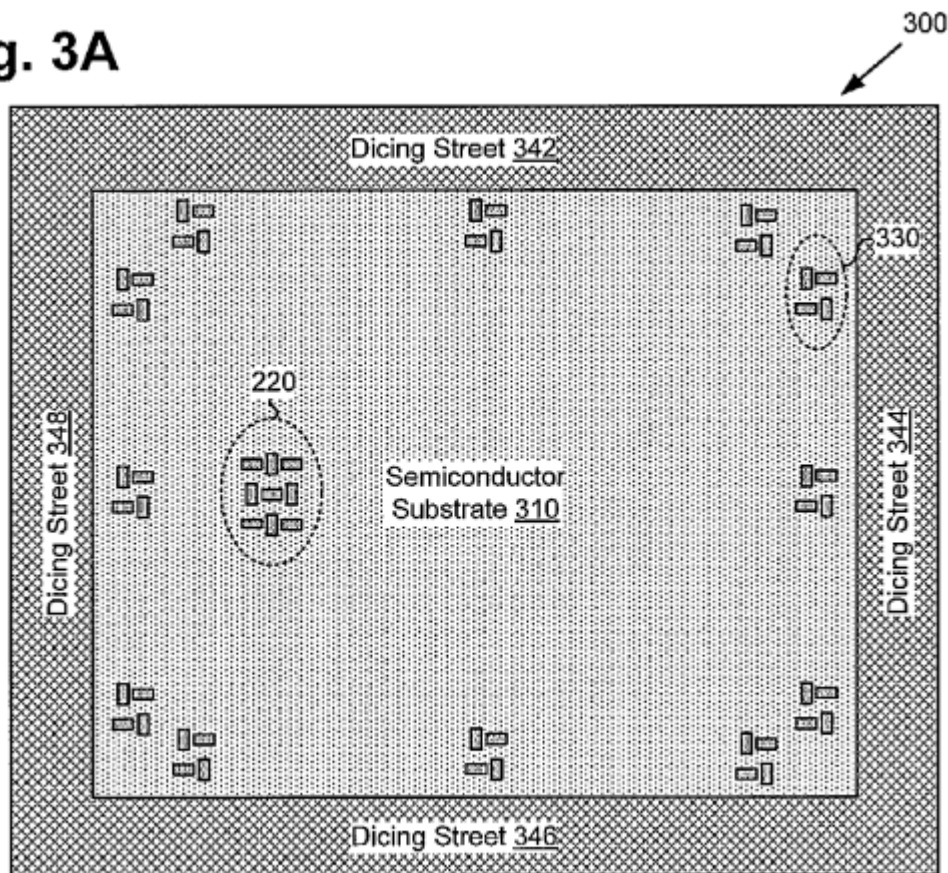
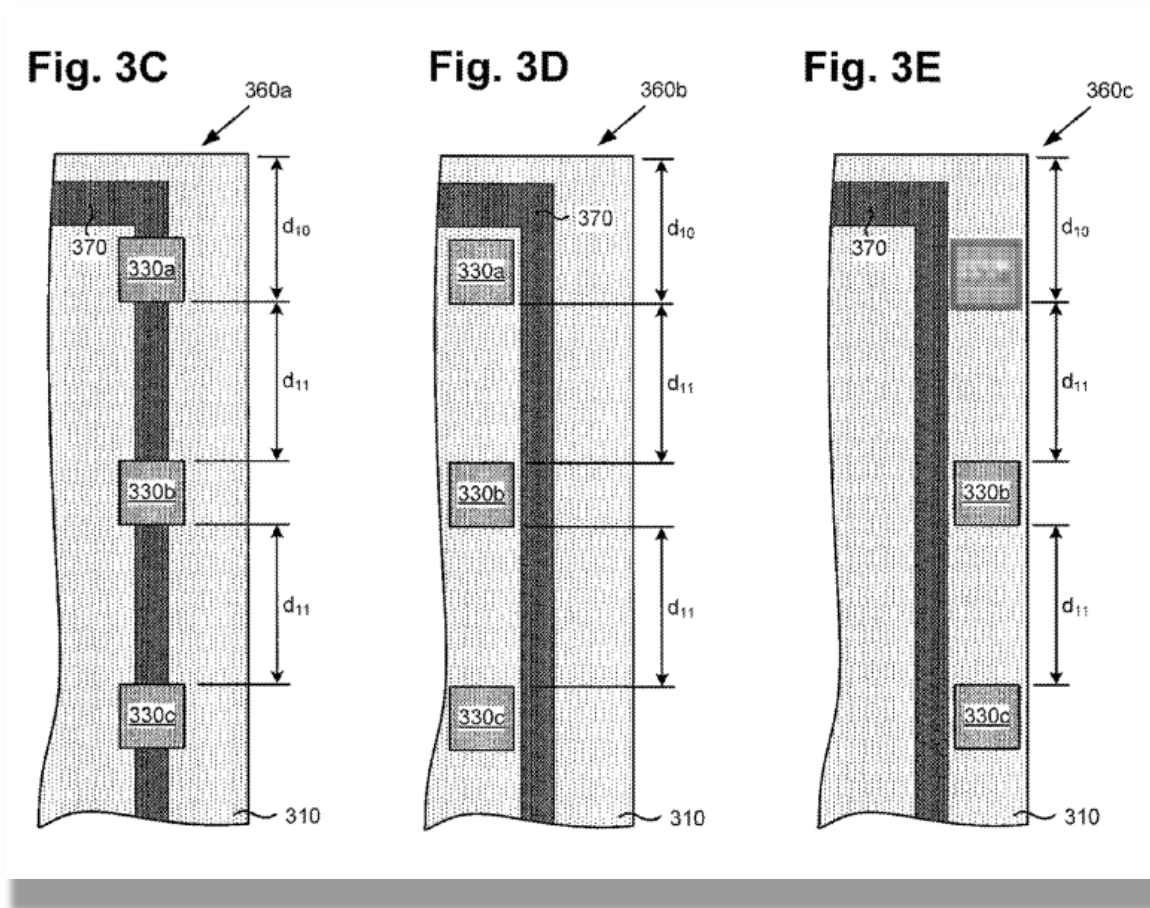


Figure 3A

38. Therefore, it is my opinion the POSITA would understand from the patent specification that the cluster of anchor vias labeled 330 in Figure 3A are disposed in the corner of the die according to the claims.

39. The specification of the '826 Patent also discloses in Figure 3C that the anchor vias “may be formed a predetermined distance d_{10} from the corner of semiconductor substrate 310 m which may vary depending on the particular application.” '826 Patent, 6:65-67. This predetermined distance d_{10} is shown in

Figures 3C-3D, reproduced below:



Figures 3C-3E

40. Therefore, it is also my opinion that the POSITA would recognize and understand from the intrinsic record that the anchor via (or cluster of anchor vias) could be located some distance from the corner and still be “disposed in” the corner for the purposes of the claims.

41. As the patent specification repeatedly states, the purpose of locating the anchor via in the corner of the semiconductor die is to prevent cracking of the die

from stresses due to fabrication processes. *See* '826 Patent, Abstract; 1:14-38; 2:44-53; 6:1-4; 6:39-46.

42. In my opinion, the POSITA at the time of the invention would have understood what constitutes the “corner” of the die for the purposes of preventing cracking and/or delamination during fabrication.

43. These problems occurring in the corners of semiconductor dies due to fabrication were known to the POSITA, and extrinsic evidence confirms both that (1) the POSITA would have been aware of the construction of a “corner” of a die; and (2) the problem of corner cracking was known.

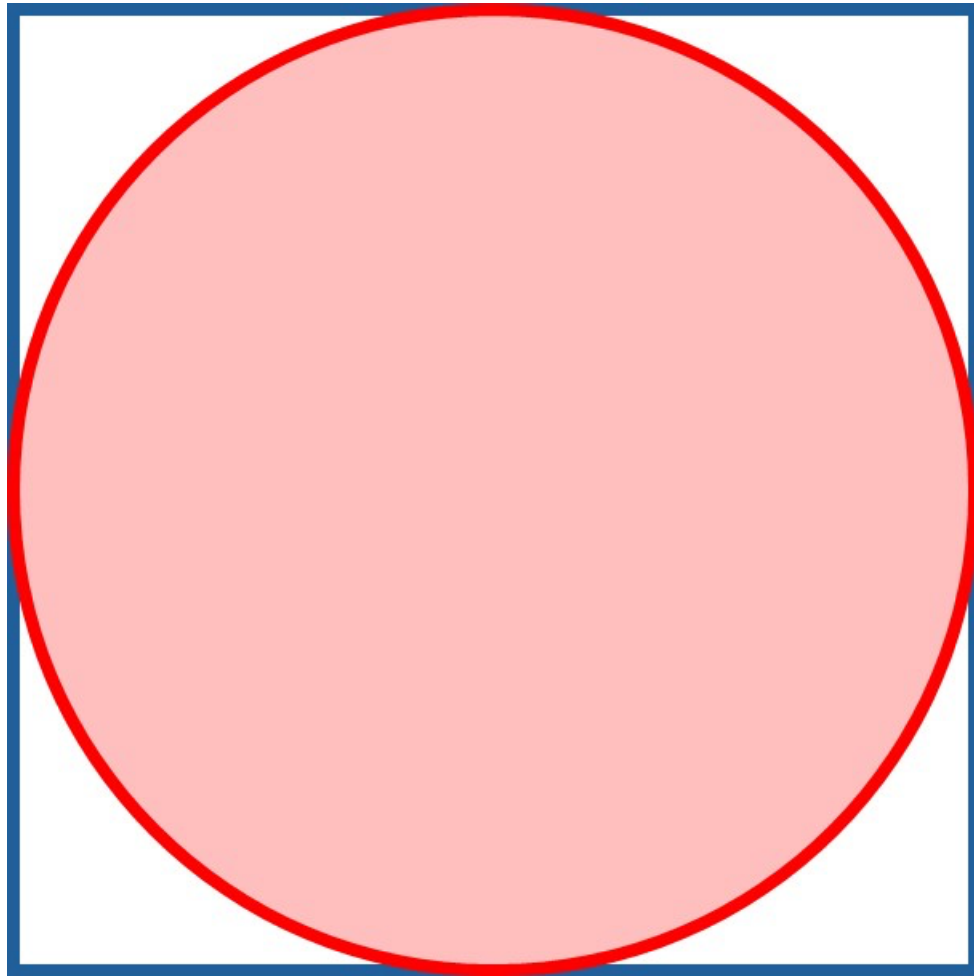
44. A paper titled “Die Singulation Technologies for Advanced Packaging: A Critical Review” (Lei 2012) (Ex. 2006, “Lei”) is instructive. In this paper, the authors note that Metal/ILD delamination and peeling occur at die corners due to “the more severe stress state at die corners.” Lei, at 5. Rather than the anchor vias of the '826 Patent, Lei proposes the use of an “edge sealing ring” also known as a “guard ring” or “crack stop” that is built surrounding each die. *Id.*

45. Lei describes several known die singulation technologies (pages 6-23), and discusses stresses caused by die singulation in detail.

46. Lei also proposes some mathematics for calculating die strength, which the POSITA would have known to use in order to calculate how much force would cause a particular semiconductor die to crack at the corner. *Id.* at 5-6. Particularly,

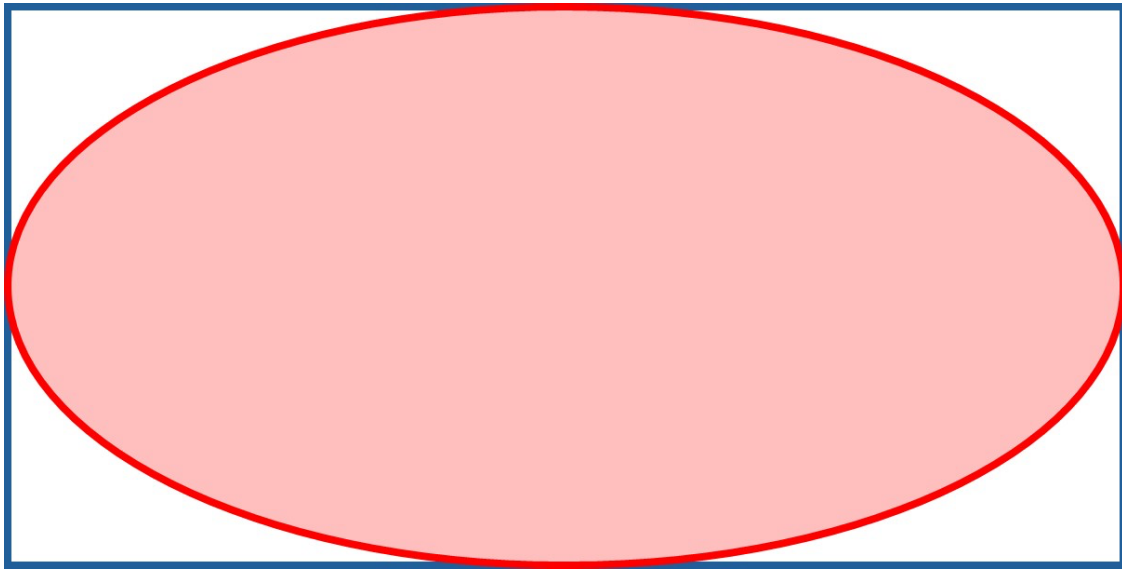
Lei notes the calculation of die fracture strength using the 3PB tests of thin film silicon dies in the SEMI standard G86-0303 (where the die fracture strength is calculated as a derivation from linear beam theory), as well as the need for additional mathematics with respect to very thin silicon chips. *Id.* at 5. However, in my opinion, engaging with these calculations is unnecessary because the POSITA would have understood whether something is located in the corner of a semiconductor die without needing such complicated mathematics.

47. In my opinion, the POSITA would have understood that the corner of a semiconductor die is everything located outside of a rounded geometrical shape inscribed within the edges of the semiconductor die. An example of this rounded geometrical shape would be a circle located inside a square semiconductor die:



48. In this example, all points located within the blue square (semiconductor die) but outside the red circle would be disposed in the corner of the semiconductor die for the purposes stated in the '826 Patent, namely, to prevent stresses due to fabrication procedures.

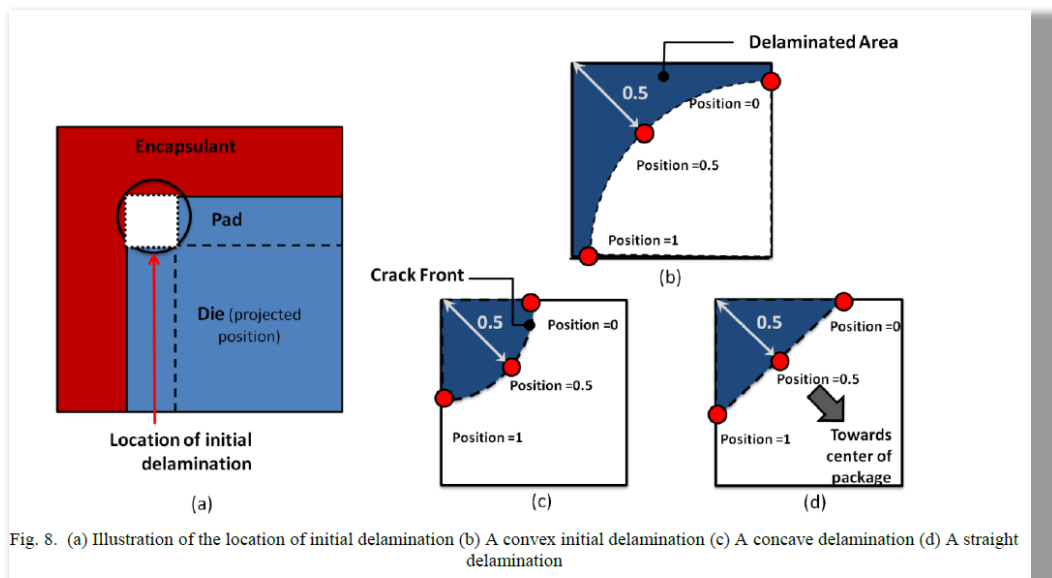
49. In the event a semiconductor die is not square, this definition is still valid. For example, in a rectangular semiconductor die with a 2:1 aspect ratio, which is a common geometry for semiconductor dies, an oval inscribed within the semiconductor die and defined by the edges would still define the corners:



50. The extrinsic evidence of record regarding die fabrication processes and the stresses caused therein support this interpretation.

51. As one example, the paper entitled “3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages” (Ho et al., 2013) (Ex. 2007, “Ho”) performs a 3D finite element analysis to model corner delamination in semiconductor dies. “It was found that in 3D analysis, different shapes of initial delaminations result in similar trends in the propensity to delaminate from the corners. From the results of the 3D analyses of a package with an initial corner delamination, it was found that increasing the die size leads to an increase in ERR, and hence an increase in the likelihood of delamination from the corners of a package.” (Ho, p. 807). Here the authors use the known technique in fracture mechanics (used to evaluate the likelihood of delamination and crack propagation in

a die) to calculate the strain energy release rate (ERR). The ERR is the rate at which potential energy decreases as a function of fracture surface area. The paper confirms that the die is most likely to fracture near corner edges, when 3D analysis, and not just 2D analysis, is used.



52. Additionally, the paper “Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks” (Rabie et al., 2021) (Ex. 2008, “Rabie”), although dated after the priority date of the ’826 Patent, also confirms known understandings of the meaning of the “corner” of the semiconductor die. For example, Rabie notes that corner delamination is caused by high shear forces, and discloses a pictorial representation and an actual image of a delaminated semiconductor die:

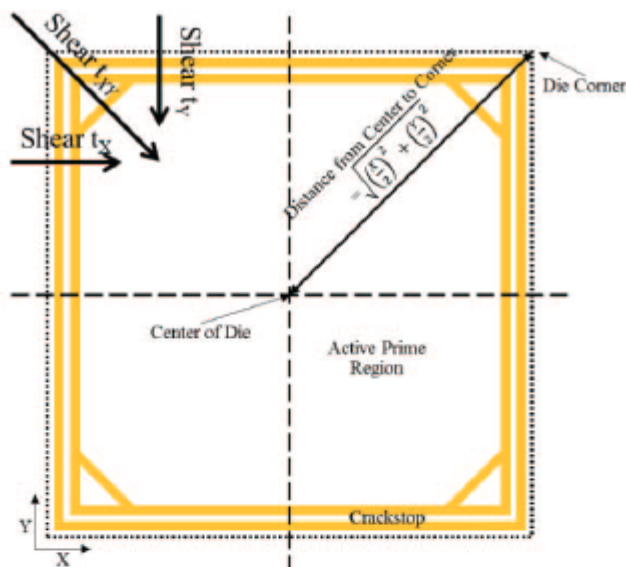


Figure 1 – A simple pictorial representation demonstrating the correlation between the size of semiconductor die and the expected magnitude of the stress and strain occurring in the corner regions.



Figure 2 – Top view of a 28.4×22.9 mm² die on a 68.5×68.5 mm² laminate showing corner delamination in the top 2 corners after underfill cure at 165°C for 2 hours.

Rabie, Figures 1 and 2

53. Importantly, Rabie’s understanding of the “corner” of the semiconductor die also comports with mine (and the POSITA’s):

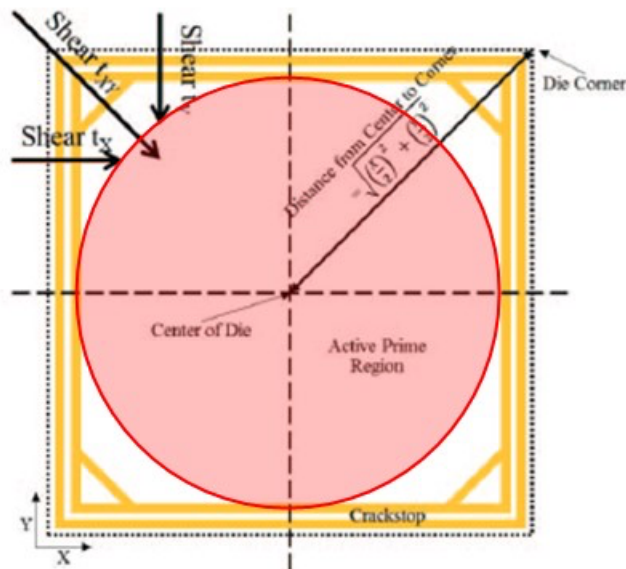


Figure 1 – A simple pictorial representation demonstrating the correlation between the size of semiconductor die and the expected magnitude of the stress and strain occurring in the corner regions.



Figure 2 – Top view of a 28.4×22.9 mm² die on a 68.5×68.5 mm² laminate showing corner delamination in the top 2 corners after underfill cure at 165°C for 2 hours.

Rabie, Figures 1 and 2, annotated

54. I note that in Figure 2, the delamination on the top left of the semiconductor die travels inside the circle and, therefore, is not completely in the

corner. However, an anchor via or other suitable delamination protection mechanism located within the corner would have prevented this delamination.

55. In my opinion, the combination of the disclosures in the intrinsic record which clearly define the problem solved by the inventions in the '826 Patent, as well as the POSITA's knowledge regarding the location of the corner of a semiconductor die, leads me to the expert opinion that the term "disposed in at least one corner of a semiconductor substrate" should be construed to mean "located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die."

B. "a backside metal layer on a bottom surface of said semiconductor substrate"

56. The Board should construe this term as "a backside metal layer in contact with a bottom surface." This is the plain meaning of "on" as recited in the claims, and a POSITA, reading the claims in view of the specification, would understand that the claims require such contact.

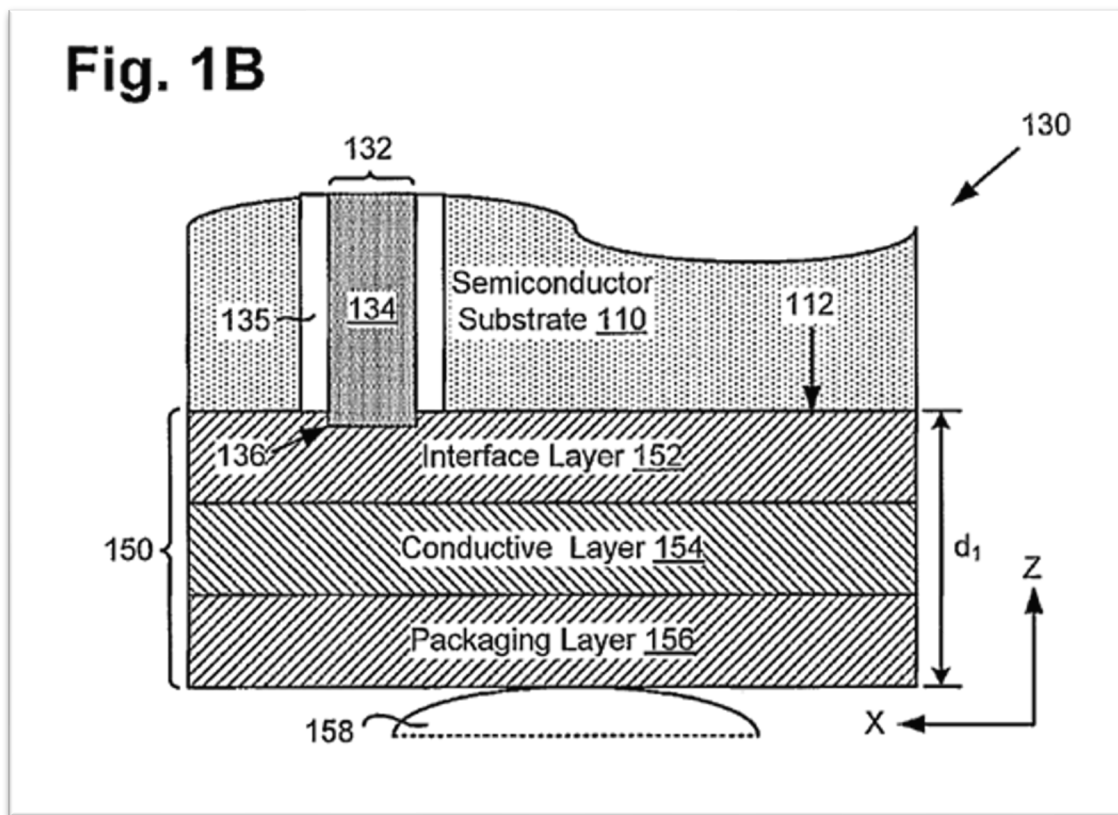
57. The claim language itself makes clear that the backside metal layer is in contact with the substrate by explaining that the backside metal layer is on the "bottom surface" of the substrate. If the metal layer could be on the substrate but not in direct contact, then the use of "surface" would be irrelevant.

58. Moreover, Claims 9 and 19 draw a distinction between a layer "on" the bottom surface of the substrate, and a layer "overlying" the substrate. The use of two

different terms would indicate to a POSITA that overlying and on have different scope. As a layer can overlie a substrate while not being in contact with its surface, a POSITA would understand that use of “on the bottom surface” in Claims 1 and 11 denotes direct contact.

59. The specification confirms my construction. The specification explains that the purpose of the '826 Patent's invention is to improve the adhesion of a metal layer to a substrate. '826 Patent, 1:16-39, 1:40-46 (“The present disclosure is directed to anchor vias for improved backside metal adhesion *to a semiconductor substrate.*”) (emphasis added). An example of a backside metal stack is “an interface layer [that] may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer.” *Id.*, 1:27-30. A key problem the inventors sought to overcome was the reliance “on the adhesive qualities between the substrate and interface layer.” *Id.*, 1:33-36. Failure of those qualities resulted in “the backside metal layer peeling from the semiconductor substrate.” *Id.*, 1:36-39.

60. To achieve that aim, the '826 Patent's anchor vias protrude into a metal layer directly in contact with the bottom surface of the substrate. This is shown, for example in Figure 1B, where the anchor vias reach only into the interface layer that is directly in contact with the substrate.



61. As the specification explains, the interface layer is “deposited on bottom side 112 of semiconductor substrate.” *Id.*, 3:43-48. Critically, the conduction layer is “then formed *on interface layer* 152.” *Id.*, 3:51-53 (emphasis added). Similarly, the packaging layer is then “formed *on conduction layer* 154.” *Id.*, 3:53-55 (emphasis added). Each layer is in direct contact with the layer which it is “formed on.”

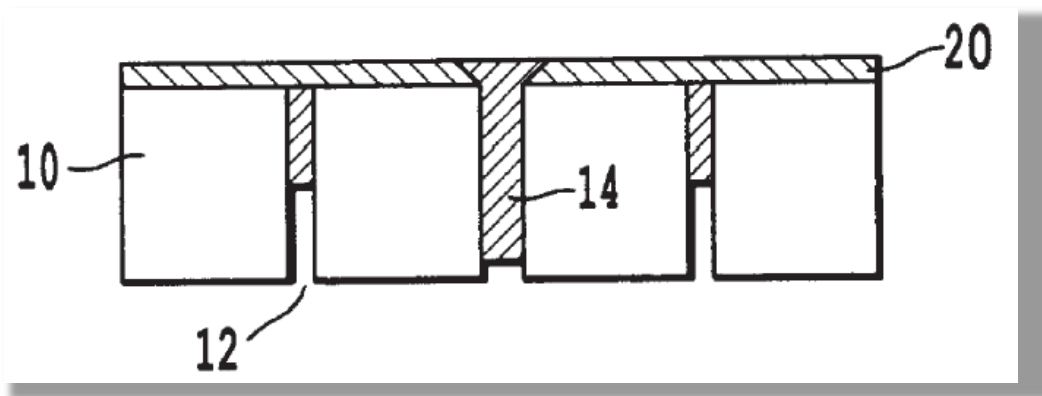
62. The specification’s description of the backside metal stack confirms that the use of “on the bottom surface” requires direct contact.

63. Accordingly, a POSITA would understand that “a backside metal layer on a bottom surface of said semiconductor substrate” means “a backside metal layer in contact with a bottom surface.”

IX. THE RELEVANT PRIOR ART

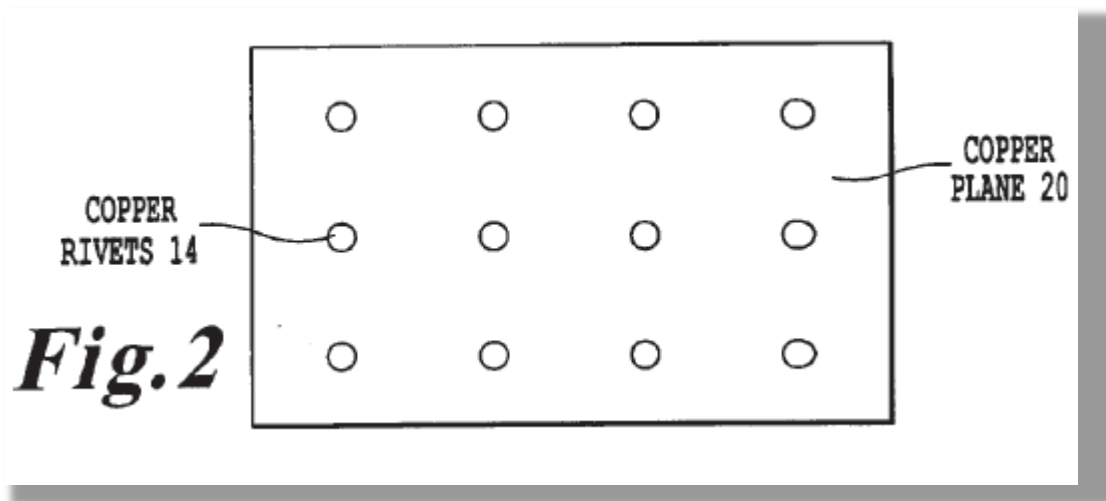
A. *Conn*

64. I have reviewed U.S. Patent Application Publication No. US 2009/0079056 to Robert O. Conn, titled “Large Substrate Structural Vias” (Ex. 1004, “*Conn*”). *Conn* relates to “a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.” Ex. 1004, [0003]. According to *Conn*, problems existed in the art where “extensive and repeated temperature changes cause fatigue of the package and the structure including the package.” *Id.* [0005]. *Conn* recognizes that “[o]ne place where this fatigue occurs is between the layers of a package laminate, or between a packaged part and a PCB.” *Id.*



Ex. 1004, Fig. 1.

65. *Conn* discloses in Fig. 1, above, a “conducting layer” 20 that is connected to a “via conductor 14” which is formed in “via 12” to provide an anchor via, which is “considered a rivet formed in the carrier substrate and in contact with the conducting layer 20 by which the conducting layer 20 maintains its structure under thermal stress.” *Id.* [0028]. *Conn*’s Figure 2 shows the conducting layer 20 being penetrated by twelve of the via conductors 14, which are annotated as “copper rivets”:



Ex. 1004, Fig. 2.

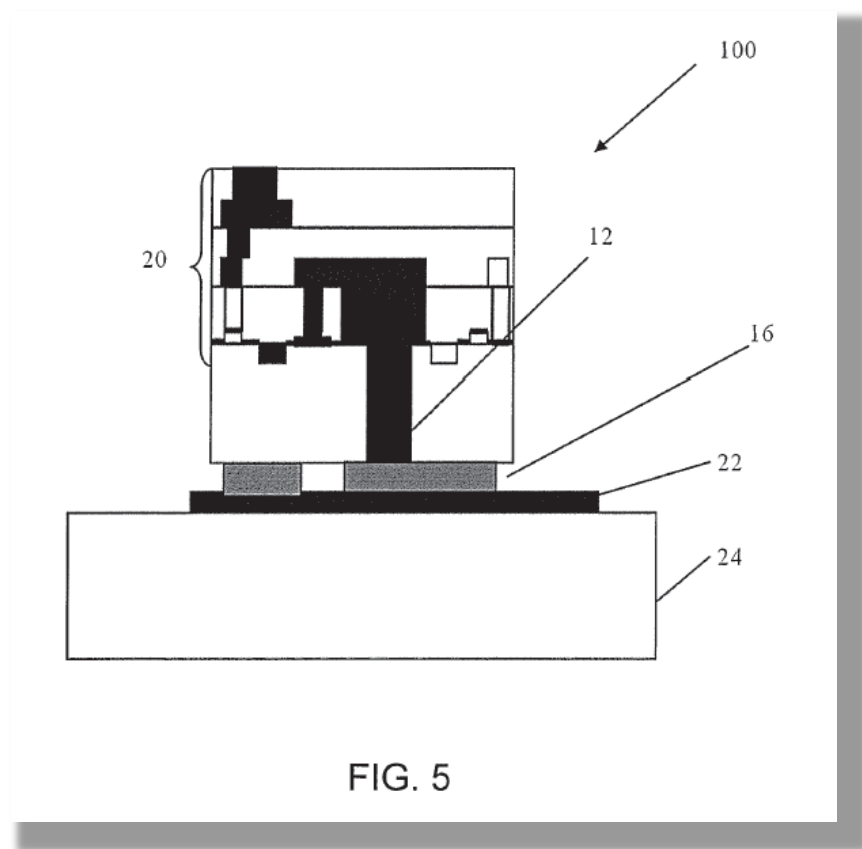
66. *Conn* also discloses that, although only the copper plane 20 is shown in Figure 2, that the semiconductor substrate is larger in surface area than the copper plane. *Id.*, [0030], [0031] (“In one embodiment, the major part of the first surface covered by the conducting layer covers at least 90% of an entirety of the surface area of the carrier substrate.”).

67. *Conn* does not mention placing the anchor vias in the corner of the semiconductor substrate, and the only mention of a corner in *Conn* is the corner of the via itself. Ex. 1004, [0054]. *Conn* also does not state that the vias are used for structural protection during fabrication. Notably, *Conn* also discloses that the via conductors 14 disclosed in Figure 1 and Figure 5 “can have a volume less than a volume of the via in which the conductor is formed” (*Id.* [0043]), and that different layers of the substrate “can be connected to one or many second via conductors . . . similar to the via conductor 14” and can be “supplied with a control signal/electrical potential . . .”. *Id.* [0046], [0047].

B. *Gambino*

68. I have reviewed U.S. Patent Application Publication No. US 2014/0138844 to Jeffrey P. Gambino et al., titled “Patterned Backside Metal Ground Plane For Improved Metal Adhesion” (Ex. 1005, “*Gambino*”). *Gambino* discloses a die including a metal ground plane 16 that includes through-silicon vias (TSV’s). Ex. 1005, Abstract. *Gambino* describes a problem with existing designs for RF analog chips, namely that the emitter ground leads used in SiGe hetero-junction bipolar transistor (HBT) RF designs “are normally contacted to the package either using multiple wire bonds or flip chip solder bumps.” *Id.*, [0002]. Wire bond leads have high inductance, and while flip chip solder bumps have low inductance, “they increase packaging complexity and are expensive.” *Id.*

69. *Gambino* proposes a solution to the problem of grounding emitters in RF analog chips, which is to place through-silicon vias (TSVs) in a semiconductor die, forming a metalized ground plane on a backside of the substrate, and placing the TSVs in contact with the ground plane. *Id.* [0005]. “Grounded through silicon vias (TSVs) can be used to reduce ground lead inductance and reduce the bond pad area on the chip surface.” *Id.* [0016]. *Gambino* shows an example of one of these TSV’s 12, grounded to the metals 16 and 22 in Figure 5:

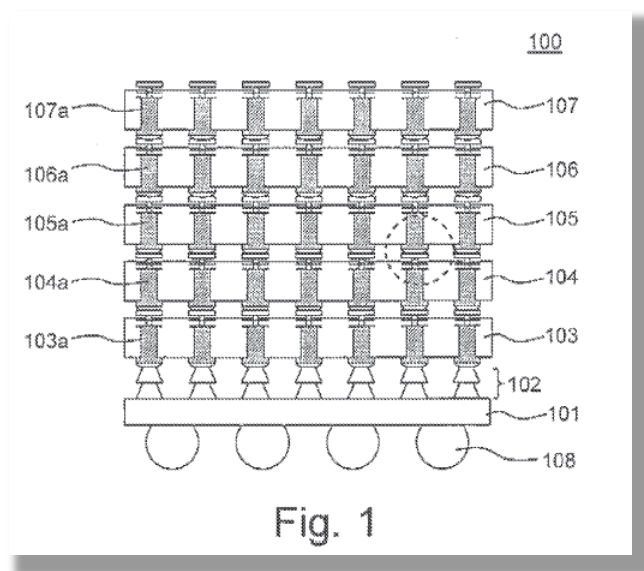


Ex. 1005, FIG. 5.

70. Nowhere does *Gambino* disclose or contemplate using vias for a purpose other than providing ground connections, and *Gambino* explicitly discloses the use of a metal pad 16a “to provide mechanical support.” *Id.* [0028]. *Gambino* does not disclose or contemplate any problems or solutions having to do with anchoring a semiconductor substrate to a metal layer.

C. *Torii*

71. I have reviewed U.S. Patent Application Publication No. US 2013/0082382 to Koji Torii, titled “Semiconductor Device” (Ex. 1009, “*Torii*”). *Torii* discloses “a semiconductor device provided with an electrode penetrating through a substrate.” Ex. 1009, [0002]. The problems discussed in *Torii* arise in semiconductor devices which are vertically stacked, where through silicon vias (TSVs) are used to create the electrical connections between vertically stacked chips. *Id.* [0004]. Figure 1 of *Torii*, shown below, discloses a group of stacked semiconductor chips that are connected by TSVs 104a, 105a, 106a, and 107a:

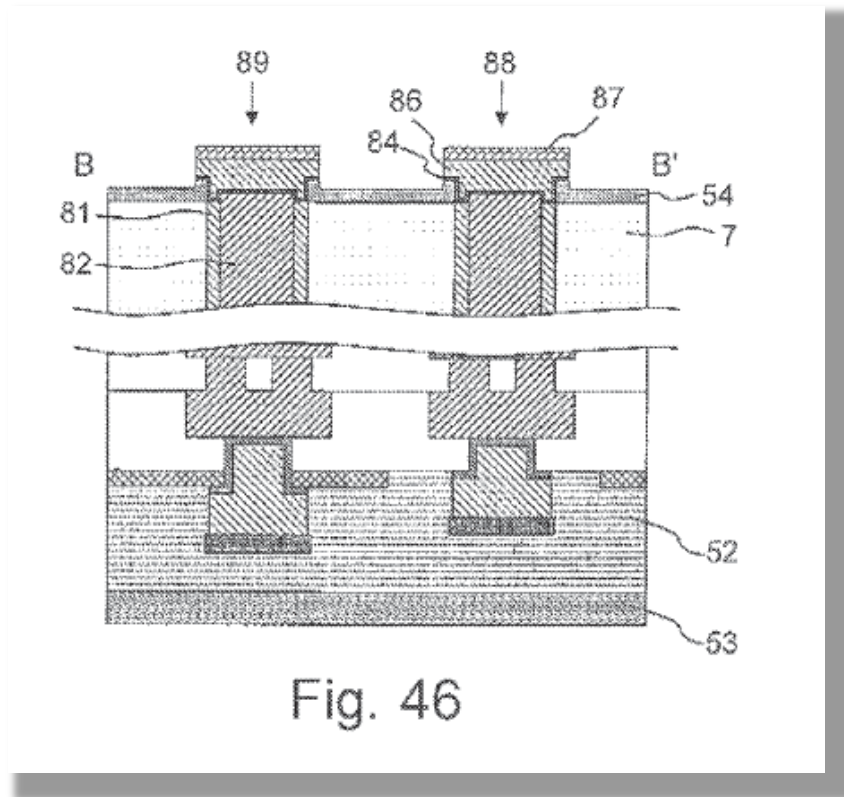


Ex. 1009, Fig. 1.

72. *Torii* describes that when joining the chips, the metal “becomes liable to segregation at the interface” which “may decrease joint strength and induce bump cracks.” *Id.*, [0007].

73. *Torii* describes the creation of two types of through-silicon vias: a “main TSV” and a “sub-TSV.” *Id.* [0045], [0048]. The main TSV is used “mainly as a current pathway” and a sub-TSV “can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.” *Id.* [0048]. In one embodiment, *Torii* describes that the TSVs can be formed from the front surface of the substrate, rather than the rear. *Id.* [0093] (Exemplary Embodiment 5). In this embodiment, as shown in Figure 46 which is heavily cited in the Petition, there exists

a "second main bump 88" and a "second sub-bump 89" that are on the back side of the device:

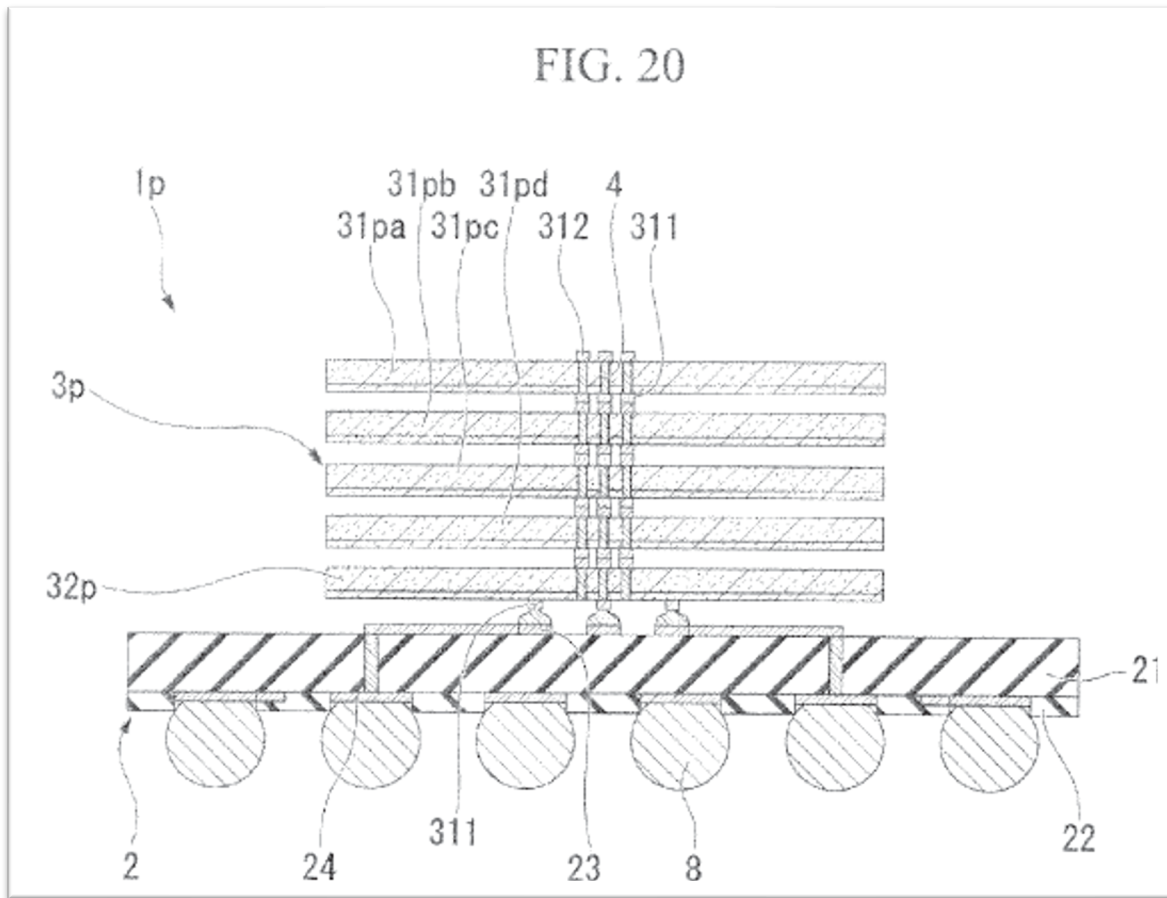


Ex. 1009, Fig. 46, [0100]. Also located on the rear of the device is a “rear-surface protective film 54,” (*Id.*) but the bumps that form elements 88 and 89 are not shown connected to a metal layer.

D. Ide

74. I have reviewed U.S. Patent Application Publication No. US 2012/0256310 to Akira Ide, titled “Semiconductor Device” (Ex. 1010, “*Ide*”). *Ide*, like *Torii*, also describes a multi-level vertically stacked semiconductor structure.

Ex. 1010, Abstract. *Id* discloses a plurality of memory chips 31pa to 31pd and an interface chip 32p, as shown in FIG. 20:

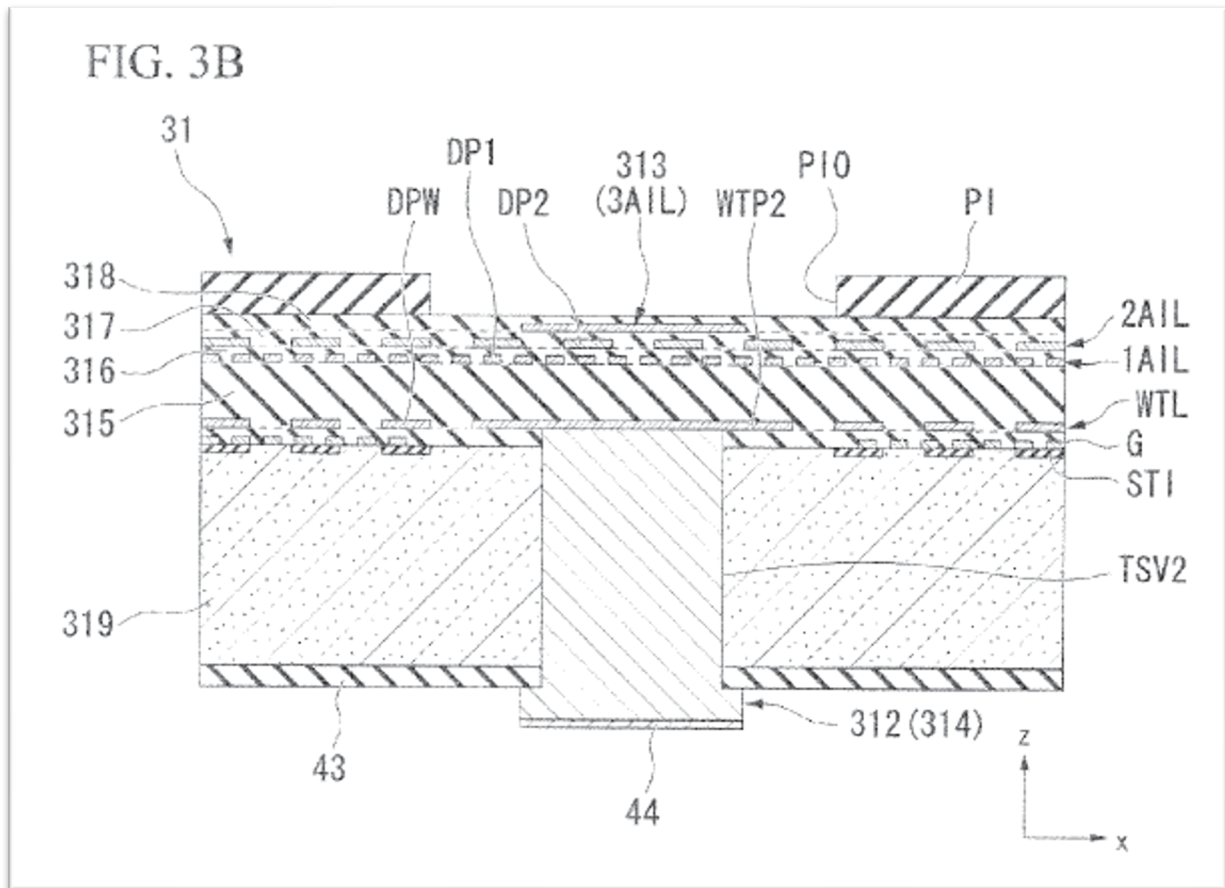


Ex. 1010, FIG. 20, [0006].

75. Each of the memory chips and the interface chips include a “surface mark” and a “rear mark” on each side of the chip, which “are used for alignment when semiconductor chips are stacked.” *Id.* [0010]. The various marks are photographed by the equipment used to assemble the chips. *Id.* The inventor recognized a problem, which is that “a recognition error of the surface mark 313

occurs in a TSV stacking process and a throughput of the above-described assembly process is considerably degraded.” *Id.* [0022].

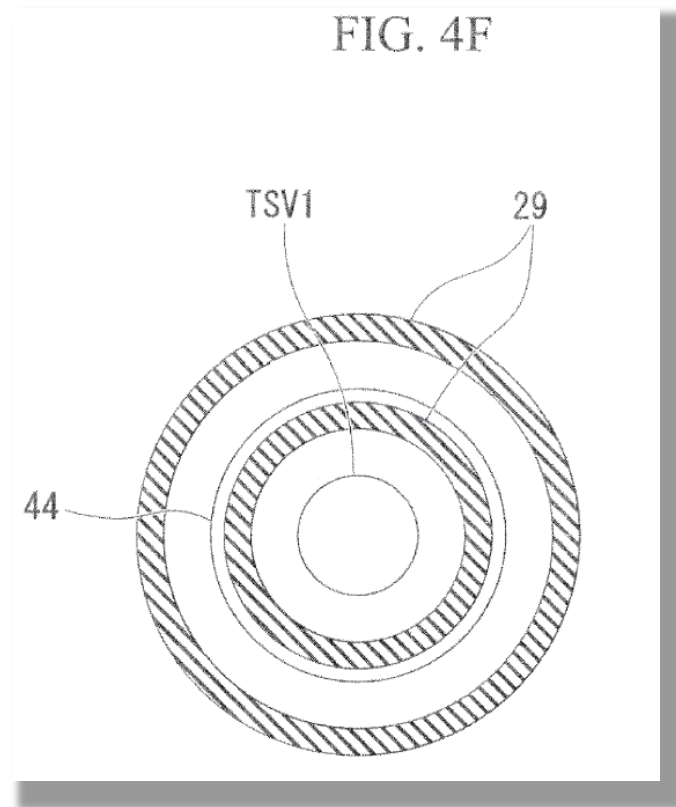
76. *Ide* also discloses Figure 3B, reproduced below:



Ex. 1010, FIG. 3B.

77. According to *Ide*, Figure 3B discloses a “surface mark 313” that is formed from aluminum, and a “through electrode TSV2 for a mark.” *Id.* [0125]. The “rear bump 44 in which a rear mark is formed is formed below the through electrode

TSV2 for a mark.” *Id.* The rear bump 44 is circular, with the TSV penetrating through it, as shown from the bottom view of Figure 4F:



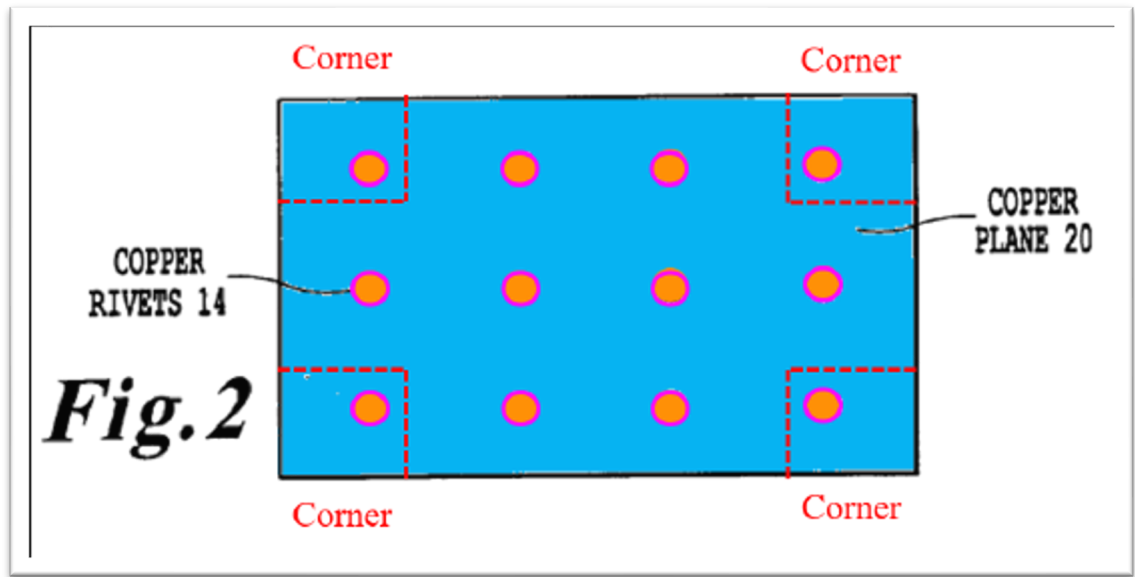
Ex. 1010, FIG. 4F.

78. The rear bump 44 is shown, as well as the TSV and insulating trench 29. *See id.* at [0119] (“an insulating trench 29 is formed in a portion of the wiring through electrode”). *Id.* also does not disclose the use of a via for the purpose of anchoring but rather focuses on creating a rear mark that is more visible to the equipment used for fabricating stacks of vertically connected chips. *Id.* [0128].

X. GROUND 1: NO CLAIMS ARE ANTICIPATED BY *CONN*

A. *Conn* Does Not Disclose at Least One Anchor Via Disposed in the Corner of the Semiconductor Substrate, as Required by Claims 1 and 11

79. A POSITA would not understand *Conn* to disclose at least one anchor via disclosed in the corner of the substrate. Petitioner and Dr. Thompson rely on a modification to Figure 2:



Pet., 29.

80. The “corner” annotations and dotted lines are not present in *Conn*; counsel for Petitioner drew them later. Ex. 2009, 36:21-37:7. *Conn* itself does not suggest that Figure 2 is near any corner of a semiconductor die; instead, *Conn* merely states that “The via conductors can be distributed relative to the conducting layer 20 in a pattern as shown for example in FIG. 2.” *Conn*, [0035].

81. Other than one reference to the corner of a via, *Conn* does not use the term “corner” at all. *See Conn*, [0054].

82. Indeed, *Conn* is silent as to the edges and corners of its semiconductor. For example, while *Conn* provides examples of distances between each via, it does not explain the distance between the vias and edges of the substrate. *See Conn*, [0035].

83. Moreover, *Conn* does not suggest that each via is an anchor via. Instead, it merely states that, for example, conducting layers are connected by “at least one via conductor 14, which acts as a rivet to hold the conducting layers 20 and 30 mechanically connected to the substrate. The conducting layers 20 and 30 can be connected by a plurality of via conductors 14, such that a stress caused by high changes in temperature in the main surfaces of the carrier substrate does not break the composite structure formed by the conducting layers and the via conductors.” *Conn*, [0038].

84. *Conn* uses its anchor vias for a different purpose than the '826 Patent. The '826 Patent uses anchor vias to compensate for mechanical stresses occurring during die singulation. Ex. 1001, 1:30-34.

85. *Conn*, however, is focused on stresses caused by thermal expansion, which is not localized to corners and edges. *Conn*, [0003] (“This invention relates to a carrier substrate for mounting of semiconductor chip devices and components

where the carrier substrate is resistant to thermal fatigue problems.”); [0005] (“[E]xtensive and repeated temperature changes cause fatigue of the package and the structure including the package.”); *Conn*, [0028] (“The anchor via can (for purposes of illustration) be considered a rivet formed in the carrier substrate and in contact with the conducting layer 20 by which the conducting layer 20 maintains its structure under thermal stress.”); *Conn* [0030].

86. A POSITA, reading *Conn*, would understand it to be silent, and thus, not disclose, anchor vias in its corners.

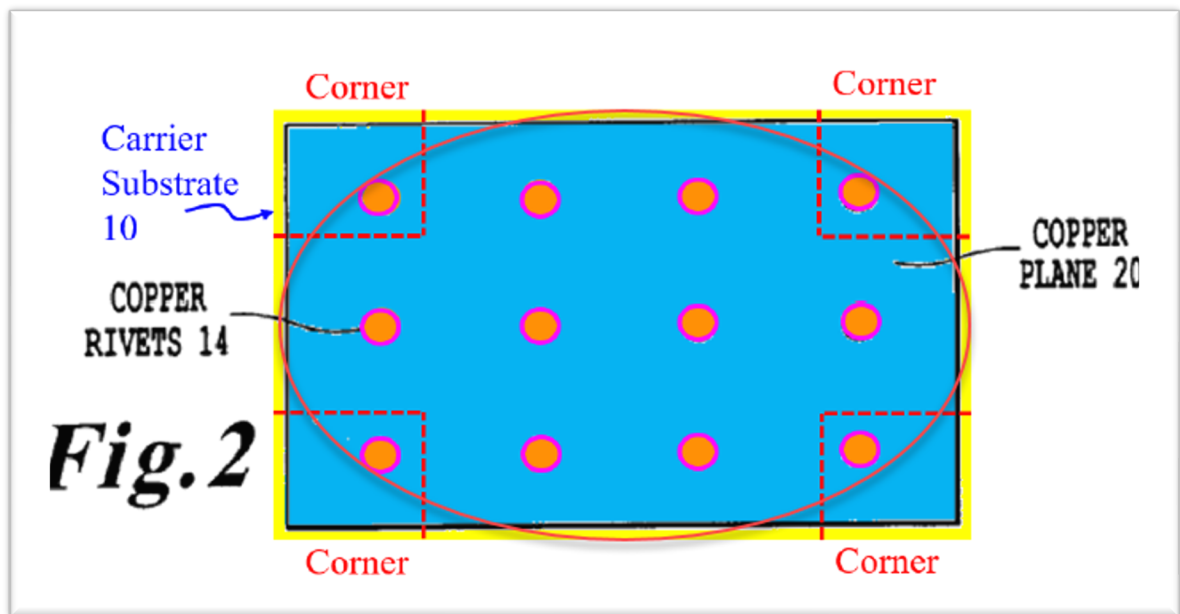
87. Accordingly, *Conn* does not anticipate Claims 1 and 11.

B. *Conn*’s Figure 2 Does Not Disclose Anchor Vias in the Corner of the Substrate Under the Proper Construction

88. As I explain above, a POSITA would not understand *Conn* to disclose at least one anchor via in the corner of the substrate. Even if the POSITA were to consider Figure 2 to show an entire conducting layer, as Petitioner and Dr. Thompson suggest, they would not understand it to disclose anchor vias in the substrate under the proper construction.

89. As I explain above, the proper construction of “disposed in at least one corner of a semiconductor substrate” is “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.”

90. To determine whether Figure 2 shows anchor vias in the corner, I utilized Petitioner's modified Figure 2, which includes a yellow area outside the copper plane. Petitioner identifies this yellow area as the carrier substrate. Pet., 30.



91. I then inscribed an oval touching the edges of “substrate.” As can be seen above, the “corner” vias are inside the oval.

92. I also note that the magenta circles surrounding the vias, drawn by Petitioner's counsel, increase the apparent size of the vias. The actual size of the vias, as drawn in *Conn*, are limited to the orange filled circles.

93. Accordingly, if a POSITA considered the dimensions and scale of Figure 2, they would not find that it discloses at least one anchor via disposed in a corner of the substrate.

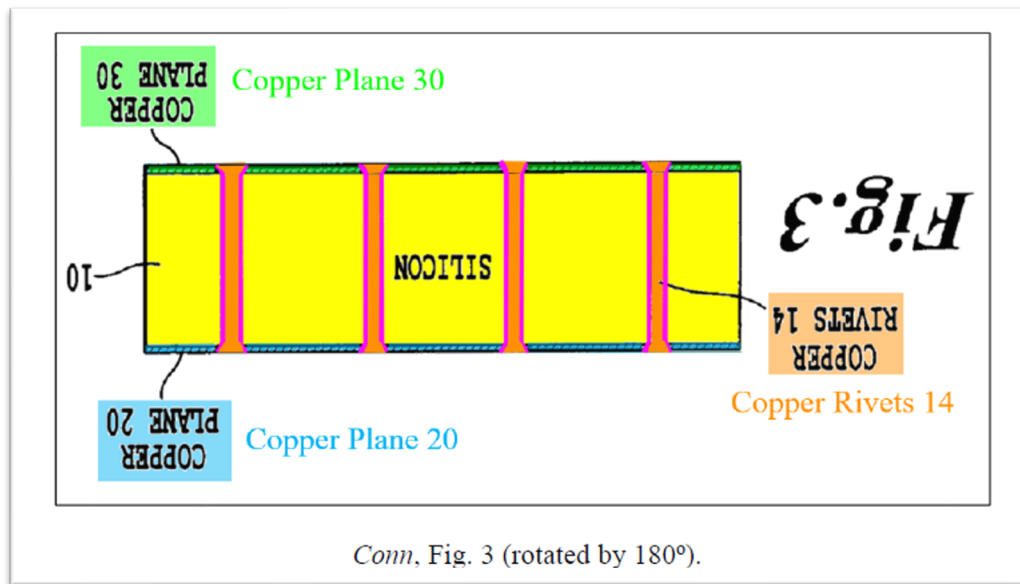
C. Conn Does Not Disclose Claim 9’s Limitation “wherein said metal filler within said at least one anchor via is Bonded to a metal layer overlying said semiconductor substrate”

94. Claim 9 is dependent on Claim 1 and adds the limitation “wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.” “Said metal filler” is recited in Claim 1, and requires (among other things), limitation 1[d]: “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.”

95. Therefore, I understand that the metal filler of Claim 9 must be bonded to a metal layer overlying the substrate *and* also not provide a ground connection to one or more active devices in the substrate.

96. In my opinion, *Conn* does not disclose the metal filler of Claim 9.

97. Petitioner relies on the embodiment shown in Figure 3 of *Conn* for its Claim 9 arguments. I reproduce Petitioner’s modified Figure 3 below.



Pet., 43.

98. In its discussion of limitation 1[d], Petitioner relies on Figure 1, which shows the metal filler not reaching both sides of the substrate, and *Conn*'s discussion that the vias and via conductor need not reach both sides of the substrate. Pet., 37 (quoting *Conn*, [0028]). Because the Figure 1 via conductors do not connect to both sides of the substrate, Petitioner concludes that the Figure 1 via conductors do not provide ground connections. Pet., 37. Petitioner does not discuss Figure 3's embodiment in its discussion of 1[d]. *Id.*

99. Petitioner does not separately discuss whether the Figure 3 via conductors would provide a ground connection. Its Claim 9 analysis is silent on this point. Pet., 43.

100. A POSITA would not understand *Conn* to disclose a metal filler that contacts both metal layers while not providing a ground connection to an active device.

101. As Dr. Thompson explained, a silicon wafer has two sides. The “front side” is where active devices are fabricated. The “backside” is the opposite side. . 2009, 42:18-43:5.

102. A POSITA would know that the backside metal layer in *Conn* is used to provide a ground or power plane. *Conn*, [0030] (discussing use of conducting layer as power plane). A POSITA would understand that the same type of conducting layer can be used as either a ground plane or power plane. Moreover, a POSITA would understand that a power plane is connected eventually to ground.

103. *Conn* explains that its via conductors are composed of conductive metals such as “copper, aluminum, gold, silver, or other conductors.” *Conn*, [0033].

104. A POSITA would understand that in a device like that shown in Figure 3 of *Conn*, the via conductor 14 would provide a ground connection to one or more active devices. At least one side of the substrate would contain active devices. Those devices would be connected to the vias through the conducting layer or copper plane 30, and current would flow to ground through the vias and copper plane 20.

105. There is no disclosure in *Conn* to suggest that the conducting layers do not lead to active devices on one side and ground on the other. As this is the standard usage for copper planes, a POSITA would have no reason to think otherwise.

106. Unlike in Fig. 1, where the via conductors do not reach both sides of the substrate, the Fig. 3 vias reach both sides, and are connected to metal conducting layers on each side. Given the difference between the Figure 1 via conductors and the Figure 3 via conductors, in my opinion, a POSITA would understand that the Figure 3 conductors do provide a ground connection to an active device.

107. Accordingly, for this separate reason, *Conn* does not anticipate Claim 9.

D. *Conn* Does Not Anticipate Claim 19

108. Petitioner relies on its discussion of Claims 1 and 9 for its anticipation arguments relating to Claim 19. For the same reasons discussed above with respect to Claim 9, *Conn* does not anticipate Claim 19.

XI. GROUND 2: *CONN* DOES NOT RENDER ANY CLAIM OBVIOUS

109. Petitioner's obviousness arguments under Ground 2 do not address the deficiencies I identify with respect to Ground 1.

A. Ground 2A

110. With respect to Claim 1, Petitioner explains that its obviousness arguments under Ground 2A are directed only to address anticipated arguments that “*Conn* does not expressly disclose ‘backside’ or ‘active devices.’” Pet., 45.

111. For all other limitations of Claim 1, Petitioner relies solely on its anticipation arguments. Pet., 51. Petitioner does not argue or attempt to show that it would be obvious to modify *Conn* to overcome the deficiencies I identify above.

112. My opinions above are not related to *Conn*’s lack of disclosure of “backside” or “active devices.” Thus, Petitioner’s obviousness arguments regarding Claim 1 do not alter my opinions.

113. For the same reasons stated above, *Conn* does not render Claim 1 obvious.

114. As to Claim 11, Petitioner relies on obviousness only to address: i) “backside” and “active devices”; and ii) any arguments relating to the order of steps of Claim 11. My opinions as to Claim 11 are not related to “backside,” “active devices,” or any ordering of steps. Thus, Petitioner’s obviousness arguments regarding Claim 11 do not alter my opinions.

115. Accordingly, for the same reasons stated above, *Conn* does not render Claim 1 obvious

116. Petitioner explicitly relies only on its anticipation arguments as to Claims 9 and 19, and does not raise any obviousness arguments as to those claims. Pet., 51.

117. Accordingly, Claims 9 and 19 are separately not rendered obvious.

B. Ground 2B

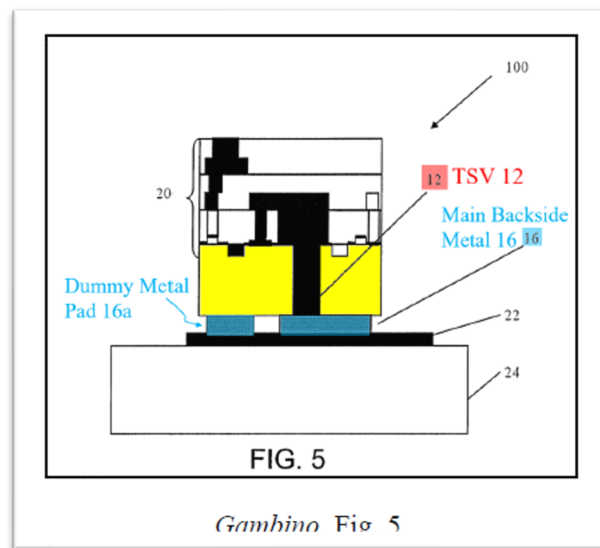
118. Ground 2B is directed solely to claims 8 and 18, and does not remedy the deficiencies of *Conn* discussed above with respect to Grounds 1 and 2A.

XII. GROUND 3: *GAMBINO* DOES NOT RENDER ANY CLAIMS OBVIOUS

A. The *Gambino/Conn* Combination Does Not Meet the Limitations of the Claims

119. Petitioner proposes combining *Gambino*'s dummy metal pads or metal layer with *Conn*'s anchor vias. However, Petitioner's proposed combination would not achieve its purpose of increasing adhesion of the metal layer to the substrate.

120. In Petitioner's proposed combination, the backside metal layer is "dummy metal pads 16a." Pet., 69-70 ("*Gambino/Conn* satisfies [1c] because corner-located dummy metal pad(s) 16a is the claimed 'backside metal layer.'").



Pet., 70.

121. *Gambino* explains that it creates its TSVs by etching holes from the front side of the substrate. Ex. 1005, [0020]. A POSITA would understand that the metal structures 20 in Fig. 5 of *Gambino* are on the front side of the wafer or die. *Id.* The TSVs extend partially through the unfinished die or substrate. *Id.* The via is then filled with metal from the front side. *Id.* After the via is filled, the backside is polished (or otherwise removed) to expose the filled via. *Id.*

122. Petitioner proposes forming *Conn*-style anchor vias using *Gambino*'s process described in [0020]. Pet., 64 (“the ***same process used for manufacturing Gambino’s electrical TSVs*** can be used to manufacture the anchor vias” (emphasis added) (citing Ex. 1003, ¶ 142)). Dr. Thompson states that:

As discussed in § XII.A.2, *Gambino*'s manufacturing method (*Gambino*, [0020] – depositing the via metal before forming the

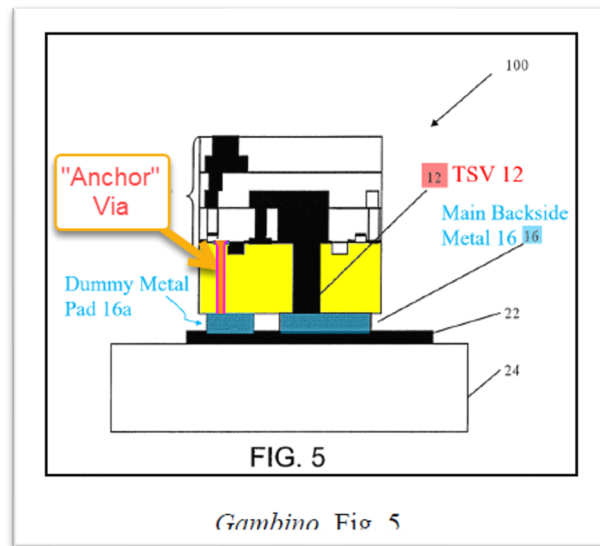
backside metal) can yield the same rivet-like anchor via structure contemplated by Conn—the resulting via conductors will form protruding portions bonded to the backside metal. Thus, the proposed combination does not require modification to Gambino’s existing manufacturing method.

Ex. 1003, ¶ 142.¹

123. Utilizing *Gambino*’s method to create *Conn* anchor vias would result in one of two outcomes. Either the anchor vias would be filled entirely, like *Gambino*’s TSVs, or the anchor vias would be etched from the frontside and not reach the backside metal layer.

124. If the anchor vias were filled entirely, they would provide a ground connection. Petitioner explains, that in its combination, the anchor vias would contact the dummy metal pads 16a. Pet., 67-70. Adding a filled anchor via to *Gambino* Figure 5 shows that the anchor via conductor would reach the wiring level and connect it to the ground plane 22. In the below Figure, I have added an anchor via where Petitioner suggests.

¹ Dr. Thompson refers to §XII.A.2 of his Declaration. That section relates to Ground 2 and whether Claim 11 recites an order of the steps. Ex. 1003, ¶¶ 116 et seq. Assuming Dr. Thompson meant some part of §XIII.A, no portion discusses Gambino’s manufacturing method.



Pet., 70 (further annotation added).

125. *Gambino* explains that its dummy metal pad 16a is connected to the ground plane 22. Ex. 1005, [0030]. Thus, adding a filled anchor via would result in another of *Gambino*'s "grounded TSVs." *Id.*, [0016]. A grounded TSV would provide a ground connection, either directly or indirectly, to an active device. *Id.*, [0030].

126. Petitioner's only discussion of limitation [1d] is to state:

e. [1d]

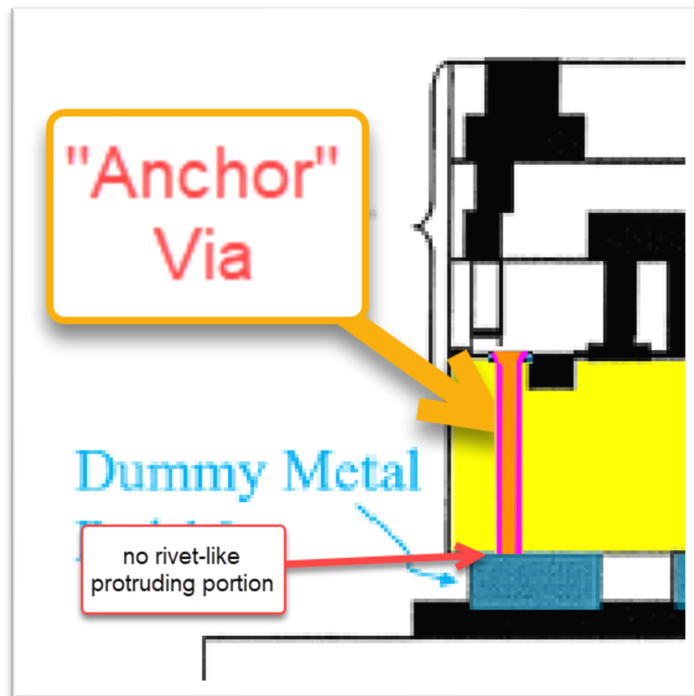
Gambino/Conn satisfies [1d] because corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection, which means the anchor vias therein do not provide ground connection to active devices.

Gambino, [0028], [0030]; Thompson, ¶151.

Pet., 70. Dr. Thompson provides no further analysis or explanation. Ex. 1003, ¶151.

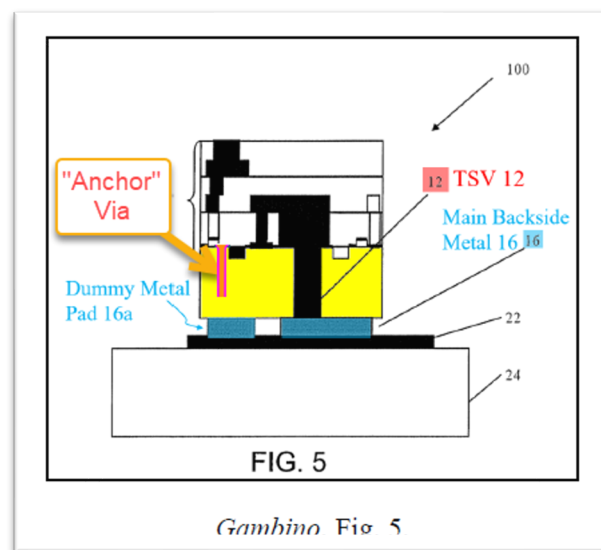
127. However, a POSITA would understand that *Gambino*’s dummy metal pads do not provide ground connection only because no TSVs reach the pads. *Gambino*, [0027] (“That is, the backside metal 16 does not entirely cover the dies 10; instead, the backside metal 16 covers the TSVs 12.”); *Gambino*, [0021], [0028], [0030]. Indeed, *Gambino*’s Fig. 5 explicitly shows the dummy metal pads in contact with the ground plane 22.

128. Further, *Gambino*’s process polishes the backside of the substrate until the via is exposed. *Gambino*, [0020]. At that point, the conductors in the via are flush with the surface of the substrate and thus, do not possess a “protruding portion extending from a backside of said semiconductor substrate” as claimed.



Detail view of Annotated Fig. 5, above.

129. In the second case, the via is only partially etched and does not reach the dummy metal pad, thus not forming an “anchor via.” I have illustrated it below.



Pet., 70 (further annotation added).

130. In this version, the “anchor” via conductor does not reach the backside surface and thus cannot meet limitations [1b] (requiring the filler to have a protruding portion extending from the backside surface) or [1c] (requiring the filler to be bonded to the backside metal layer). The proposed “anchor via” is not an anchor via because it does not anchor anything.

131. Petitioner does not suggest modifying *Gambino*’s process. Indeed, Petitioner’s sole evidence that the process of making the combination is predictable is “because the same process used for manufacturing *Gambino*’s electrical TSVs can be used to manufacture the anchor vias.” Pet., 64.

132. Furthermore, it would not be obvious to a POSITA to modify *Gambino*’s process to etch the unconnected “anchor” vias, shown in the Figure in paragraph 129, starting from the backside, which is not taught by *Gambino*, or to have the dummy metal pad to be unconnected to the ground supply, which is also not taught by *Gambino*. Likewise, to build an unconnected “anchored” via in *Gambino*, a POSITA would, at least, need to add a 2nd via mask, 2nd etch process, a 2nd TSV fill process, and a 2nd CMP process step. Such additional processing steps are not explained in either *Conn* or *Gambino*, and would add additional manufacturing costs to the die. At the outset, Petitioner provides no evidence that such a modification would be feasible or within the abilities of a POSITA. Instead,

Petitioner argues that a POSITA would use *Gambino*'s process unchanged. Pet., 64. Dr. Thompson makes the same statement. Ex. 1003, ¶ 142.

133. A POSITA would not modify the *Gambino* process to etch and fill both (i) connected vias from the frontside and (ii) unconnected “anchor” vias from the backside because it would require significant modifications to the manufacturing process. This, again, is not taught by either *Conn* or *Gambino*. This would require additional semiconductor manufacturing equipment and steps because such equipment cannot etch from two sides simultaneously; the die lays on a platen and, a mask is applied to the top of the die. *Gambino* [0020]; *Conn*, [0049].² The top of the die and mask are then etched away, leaving a pattern in the substrate. Modifying *Gambino* to etch the vias from the backside would require flipping the die in the middle of processing, thereby adding process steps and thus, process costs, as well as additional opportunities for defects, which would decrease yield and increase manufacturing costs. Semiconductor dies are inherently sensitive to mechanical stresses, and flipping a die would subject it to additional stress and yield loss. The necessary modifications are not within the knowledge of a POSITA, nor are they taught in the references at issue in this IPR. A POSITA (under either

² Conn's etching process is similar to Gambino's and similarly could not achieve a Conn/Gambino device that meets the claims. Indeed, both Conn and Gambino use Bosch deep reactive ion etching. Conn, [0049]; Gambino, [0020].

Dr. Thompson's or my definition) would not be capable of altering the process without numerous additional process steps, process costs, and risk to yield loss.

134. Adding the additional processing steps needed to create the unconnected anchor vias would not be predictable, and would require significant experimentation and testing. Indeed, adding process steps to any semiconductor manufacturing process requires significant experimentation and testing. I am not aware of any evidence that a POSITA would be motivated or able to make such modifications.

135. Accordingly, in my opinion, *Gambino* does not render any claims obvious.

XIII. GROUND 4: *Torii* DOES NOT ANTICIPATE CLAIMS 1, 8-11, 18-20

A. *Torii* Does Not Disclose [1d] “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate”

136. Petitioner relies on *Torii*'s “sub-bump (sub-TSVs)” as the anchor vias. Pet., 80-81. However, *Torii* states that “The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.” Ex. 1009, [0048].

137. I understand that the Board has already found that *Torii* does not disclose this limitation. I agree.

138. A POSITA would understand that “releasing static electricity” is providing a ground connection, as static electricity would necessarily be released to ground.

139. A POSITA would therefore recognize that *Torii* provides ground connection to one or more active devices in the substrate, and, accordingly, does not anticipate any Challenged Claims.

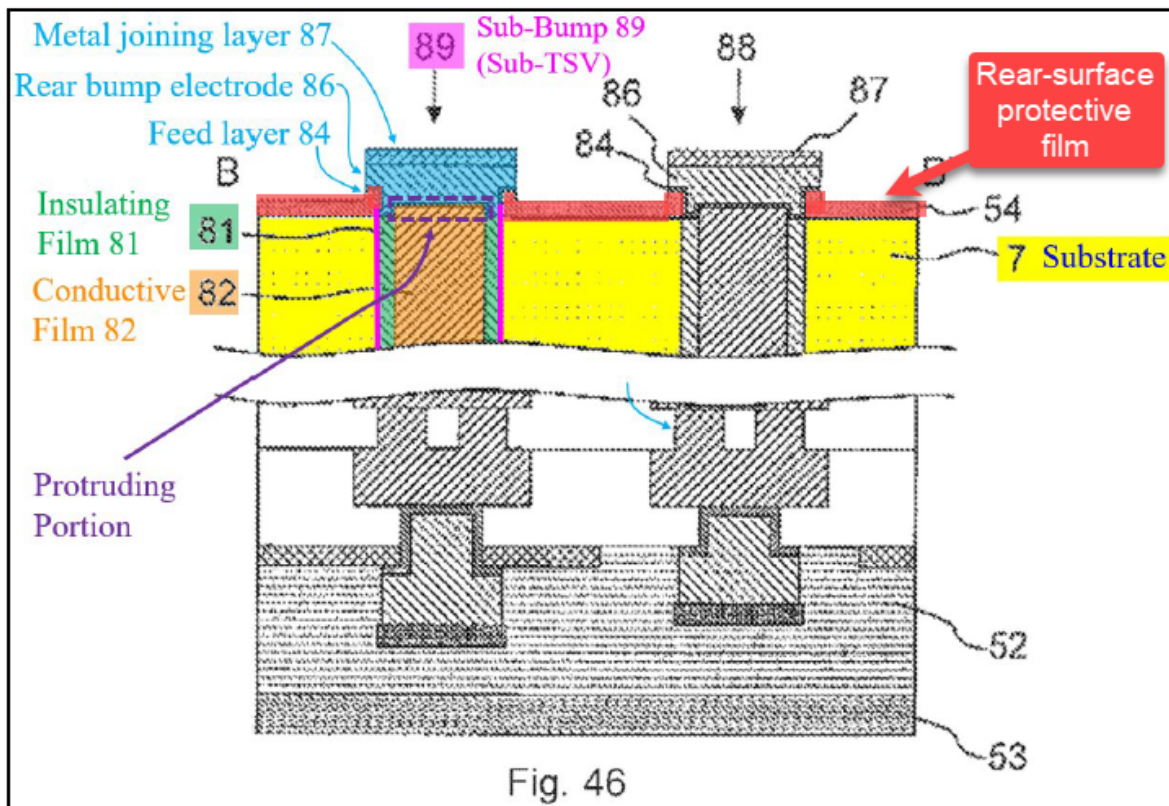
B. *Torii* Does Not Disclose “a backside metal layer on a bottom surface of said semiconductor substrate”

140. In my opinion, *Torii* does not disclose “a backside metal layer on a bottom surface of said semiconductor substrate” because Petitioner’s identified backside layer—feed layer 84 (without or without rear bump electrode 86 and second metal joining layer 87)—is not on the bottom surface of the semiconductor substrate.

141. As I explain above, the plain meaning of “on the bottom surface” requires direct contact between the metal layer and the bottom surface of the substrate. Even if the Board chooses not to construe the term, my understanding of the plain meaning is consistent with the ’826 Patent specification.

142. The Petition states that *Torii*’s “second feed layer 84 alone, or together with rear bump electrode 86 and second metal joining layer 87, constitutes the claimed ‘backside metal layer.’” Pet. at 84-85 (citing Ex. 1003 ¶ 180). Figure 46 of

Torii, on which Petitioner relies, shows that “rear-surface protective film 54” is between the surface of the substrate and the feed layer. I have annotated Petitioner’s annotated Fig. 46 to identify the film in red.



Pet., 83 (additional annotation added).

143. As *Torii* explains, the rear-surface protective film 54 is “formed on the entire rear surface.” Ex. 1009, [0100]. Petitioner acknowledges that “Rear-surface protective film 54 is between the shoulder region and the substrate surface.” Pet., 84 n.12.

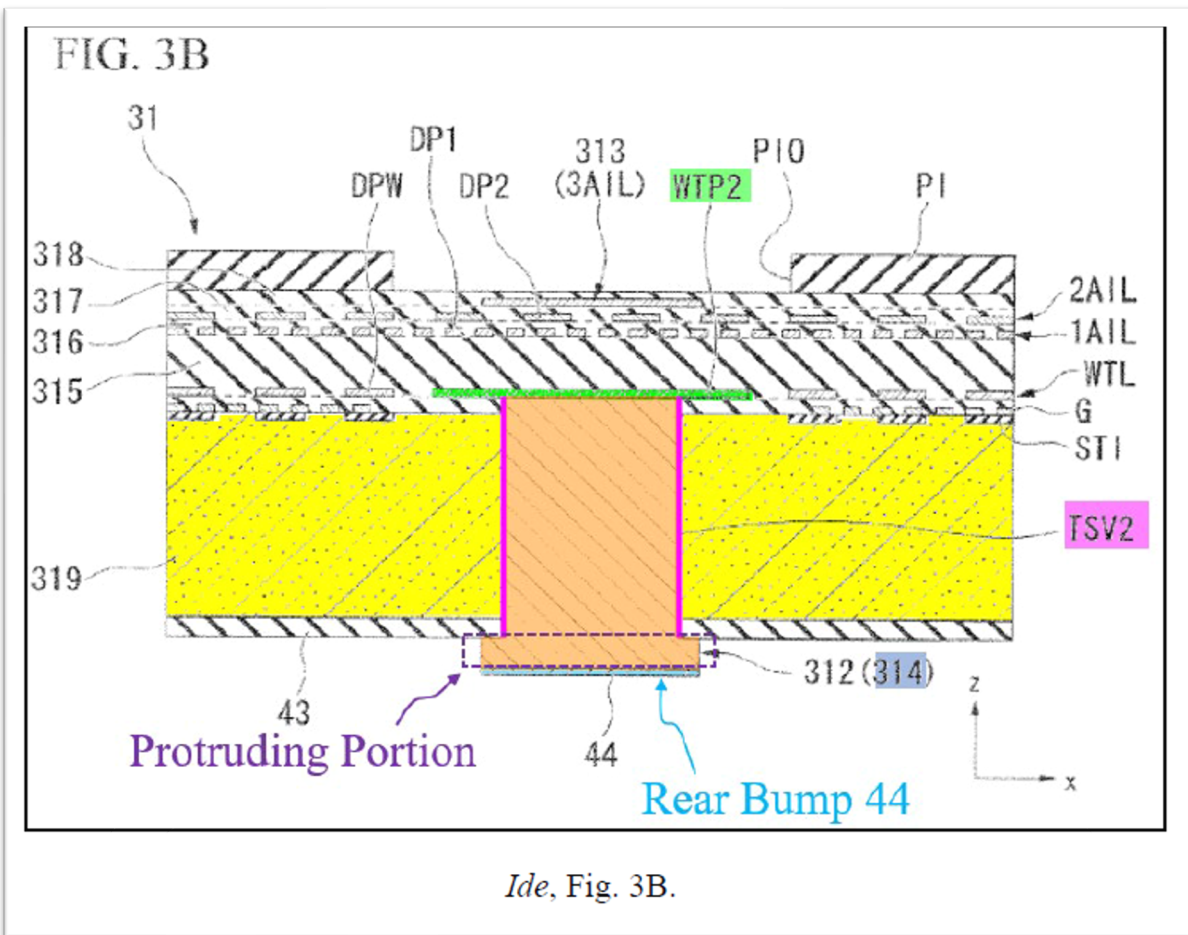
144. Accordingly, *Torii* does not disclose the backside metal layer, and therefore, for this separate reason, does not anticipate any of the Challenged Claims.

XIV. GROUND 5: *IDE* DOES NOT ANTICIPATE ANY CLAIMS

A. *Ide* Does Not Disclose “a backside metal layer on a bottom surface of said semiconductor substrate”

145. Similar to *Torii*, *Ide* does not disclose this limitation because the identified backside metal layer is not on a bottom surface of the semiconductor substrate.

146. Petitioner relies on the rear bump 44 shown in *Ide* Figure 3B as the backside metal layer. Pet., 94-95.



Pet., 94-95.

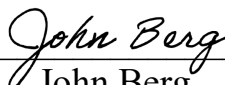
147. As Petitioner admits, the rear insulating layer 43 and rear bump electrode 312 both are interposed between the rear bump and bottom surface of the substrate. Pet., 94 n.15.

148. As the plain meaning of the term “a backside metal layer on a bottom surface of said semiconductor substrate” requires that the metal layer be in contact with the bottom surface of the substrate, *Ide* does not disclose this limitation and does not anticipate any claims.

XV. CONCLUSION

149. I declare under penalty of perjury that the foregoing is true and correct.

Dated: June 16, 2025



John Berg