JOHN BERG

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SUMMARY

As the Chief Technologist at American Semiconductor, Mr. Berg developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using 45nm double-gate FET technology. Before joining ASI, Mr. Berg developed automated tools for the nano-imprint industry at Transfer Devices. Prior to Transfer Devices, Mr. Berg was a Managing Director at Cypress Semiconductor, where he managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology.

Mr. Berg has been an expert witness in semiconductor process development, silicon device physics, semiconductor design, CAD tools, lithography, semiconductor bonding including CMP, and business practices. He served as the plaintiff's expert witness in the Palmchip v. Ralink (Mediatek) microprocessor patent infringement. He was an expert witness for the plaintiff in Semi-Materials Co. Ltd. v. MEMC Pasadena Inc, in which he testified at jury trial twice and was deposed twice. In both cases, the plaintiff won, with more than $19M being awarded to Mr. Berg's client. Mr. Berg also has testified in front of the US Patent Office in the re-examinations of three patents, all of which were successfully defended, and has been an expert in numerous IPR cases. He was deposed as a Cypress employee in Cypress Semiconductor v. Altera Corp., where Altera was sued for interference with contract, trade secret misappropriation, and unfair competition involving programmable logic devices. At Standard Microsystems, he did reverse engineering analysis on competitors' products; these analyses led to three successful licensing agreements with other semiconductor companies.

PROFESSIONAL EXPERIENCE

BERG-ATTENBOROUGH, INC. **SEPTEMBER 2010 - PRESENT**

PRINCIPAL (2 EMPLOYEES)

Berg-Attenborough, Inc. is a consulting firm, which does technical consulting for Top 50 semiconductor companies and does expert witness work for patent and business issues.

Key Achievements:

- Developed wafer bonding and CMP for advanced photonics integrated circuit processing.
- Fan-Out Wafer Level Packaging, FO-WLP consulting for Draper Laboratories
  - Successfully developed a 60+ chip multi-chip module including MPU, FPGA, DRAM, and FLASH.
  - Uncovered two temperature cycle reliability problems with the existing FO-WLP technology and instituted corrective actions to the process and design to eliminate these.
    - Modified interlayer dielectric and solder mask to correct die cracking
      - Problem uncovered by SEM and verified via SEM and reliability testing
    - Modified metal bus rules using Ansys and empirical data to ameliorate die cracking

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PROFESSIONAL EXPERIENCE (CONT.)

AMERICAN SEMICONDUCTOR, INCORPORATED **2005-2014**

CHIEF TECHNOLOGIST (22 EMPLOYEES)

American Semiconductor is fabricating radiation-hard CMOS products for military and aerospace customers.

Key Achievements:

- Hands-on in-fab development the front-end & back-end full wafer scale process for an antenna array product, which resulted in a Top Supplier of the Year Award from Boeing. A low temperature substrate-to-substrate bonding technique was developed specifically for this product.
- Hands-on in-fab development of the company's double-gate FET process, and successful transfer of the company's double-gate FET CMOS process from university laboratory into a CMOS production facility. This included CMP, lithography, and etching processes.
- Design of MCU/analog RF/sensor/memory flexible system-on-chip reference products:
  - Products includes hardware and software/firmware for system control and security/encryption
  - Process development included direct low temperature and high temperature direct wafer-to-wafer bonding techniques with and without through silicon vias (TSV's) to reduce system form factor.
  - Flip-chip, ball-bond, and wire-bonding used to assemble product.

TRANSFER DEVICES, SANTA CLARA, CA **2004-2005**

CHIEF OPERATING OFFICER (12 EMPLOYEES)

Transfer Devices is a lithography start-up, which is commercializing technology developed in Professor Fabian Pease's laboratory at Stanford University.

Key Achievements:

- Built a class 10 manufacturing clean room and delivered product to customers.
- Launched the ExaGlide 10r nano-patterning production tool development program
- Improved tool uptime from <10% to 95% and product yields from 50% to 99.9%

NANTERO, WOBURN, MA **2003-2004**

VICE PRESIDENT, NEW PRODUCT DEVELOPMENT (50 EMPLOYEES)

Nantero is developing non-volatile random-access memory using carbon nanotube switches.

Key Achievements:

- Hired and led the design team that taped out a 4Mb non-volatile memory chip, which resulted in a radiation-hardened non-volatile memory technology.

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PROFESSIONAL EXPERIENCE (CONT.)

CYPRESS SEMICONDUCTOR, SAN JOSE, CA **1998-2002**

MANAGING DIRECTOR, PROGRAMMABLE LOGIC (5500 EMPLOYEES)

Cypress Semiconductor, a public company, is a broad line supplier of semiconductor components.

Key Achievements:

- Program manager for Delta39K, 37K product lines, including hardware development, and software/firmware development on systems instantiated by customers.
- First Cypress multi-chip module product, using flip-chip and ball-bonding technologies.
- Hired, trained, and managed the ESD team at Cypress (3 technology and design engineers). Reduced the number of corporate ESD-related design errors from 50% to <5% by standardizing ESD design rules, testing and incorporating secondary breakdown into the ESD design, standardizing ESD design methodology, and instituting formal ESD design reviews into Cypress's design flow. Purchased test systems for in-house ESD testing.
- Integrated NAND FLASH IC and SRAM-based CPLD IC into 1st Cypress multichip module
- Developed and put into production the company's 0.25um BiCMOS and 0.18um SiGe HBT processes used for Datacommunications Products. Substantial materials and CMP work.
  - Provided PDK, CAD, and Device support.
- Increased revenues from $38M to $72M by increasing the number of PLD/FPGA product families to 6, including the Ultra37000, Delta39K, Quantum38K and PSI product families
- Designed CPLD products in TSMC's 0.13um technology which used copper interconnect.

ZILOG CORPORATION NAMPA, ID **1990-1998**

VICE PRESIDENT, TECHNOLOGY DEVELOPMENT (1600 EMPLOYEES)

Zilog was a pre-IPO company that successfully went public in 1991 and was later acquired by IXYS.

Key Achievements:

- Trained and led the Nampa site's 15-person Design Department and 30-person Technology Development Department; delivered memory cells (SRAM, EEPROM, EPROM, NOR Flash), memory block compilers, and I/O cells for the company's design library for its system-on-chip and application-specific standard products.
- Designed, built, and qualified the $175M 200mm fabrication facility: 1st silicon yield.
  - 0.25um CMOS technology, including CMP, tungsten plugs, trench isolation, and low k dielectric. First dry-in/dry-out CMP metals and dielectric tools brought into production.
  - Solved the temperature cycle problem with the 200mm line within 90 days after initial observation. Solution involved modifying design rules for metallization and improved planarization.
- Hired, trained, and led the design team that taped out 6 system-on-chip products per year for 8 years for the $120M Z8 microcontroller business unit.
- Worked with outside laboratories to ensure hardware design compliance to FCC's EMF/EMI requirements.
- Modified design rules and design clocking scheme to improve 1st pass yields.

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PROFESSIONAL EXPERIENCE (CONT.)

STANDARD MICROSYSTEMS CORPORATION, HAUPPAUGE, NY **1980-1990**
ENGINEERING DIRECTOR (500 EMPLOYEES)

Standard Microsystems was a public company in 1980, and later, was acquired by Microchip, Inc.

Key Achievements:

- Began career as a hands-on manufacturing CVD engineer working with Applied Materials deposition tools.
- Solved the company's Highly Accelerated Temperature/Humidity Stress Test (HAST) problem, that had been plaguing the company for five years, using optimizing thin film dopant concentration.
- Instituted DOE and six sigma process development practices in 1986.
- Hired, trained, and managed 26 sustaining and development engineers in the company's 2500 wpm wafer fab. Developed and transferred five 2um/sub-2um CMOS technologies into production.
- Reversed engineered Intel, TI, and National Semiconductor products to provide evidence of infringement against Standard Microsystem's patents. This included working with and coordinating external laboratories to provide deconstruction analysis.

EDUCATION

2002-2003 **STANFORD UNIVERSITY** **PALO ALTO, CA**
M.S. Management, Graduate School of Business. Sloan Fellow.

1998-2002 **STANFORD UNIVERSITY** **PALO ALTO, CA**
16 graduate credits in Electrical Engineering (GPA = 4.1) in circuit design

1975-1980 **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** **CAMBRIDGE, MA**
BS Physics. Four-year National Merit Finalist and Scholar. Intercollegiate crew

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PUBLICATIONS

"MOS Transistor Technology from Planar to Nanowire Transistors," Mantha, B. and Berg, J., Silicon Valley Engineering Council Journal, Volume 1, 2009, Pages 23-32.

"Substrate Bias Effects on Transiently Triggered Latchup in Bulk CMOS," Chang, L. and Berg, J.; IEEE Transactions on Electron Devices, Volume 33, Issue 1, Jan. 1986 Pages 165 - 167

"A Derivative Method to Determine a MOSFET's Effective Channel Length and Width Electrically**,"** Chang, L. and Berg, J.; IEEE Electron Device Letters, Volume 7, Issue 4, Apr 1986 Pages 229 – 231.

"A Simplified Model to Predict the Linear Temperature Coefficient of a CMOS Inverter's Delay Time," Chang, L., Khoa Vo and Berg, J.; IEEE Transactions on Electron Devices, Volume 34, Issue 8, Aug 1987 Pages 1834 – 1837.

CONFERENCE LEADERSHIP AND PRESENTATIONS

Co-Chairman, 2007 IEEE San Francisco Bay Area Nanotechnology Symposium, July 2007.

"Rad-Hard Reconfigurable Bidirectional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet 0.18um SOI CMOS Technology," K. DeGregorio, D. Wilson, S. Parke, J. Berg, M. Goldston, R. Hayhurst, D. Hackler 12th NASA Symposium on VLSI Design

Committee Member, Programmable Logic Sub-Committee, 2003 IEEE Solid State Circuits Conference, San Francisco, CA

"Measuring the Effective Channel Length of the Deep Submicron MOSFET and the Channel Broadening Effect," S.H. Chung, Tim Carns, S.K. Lee, L. DeBruler, and J. Berg, Proceedings of the Thirteenth Biennial University/Government/Industry Symposium, IEEE Press, pp. 176-181, 1998.

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PATENTS

Patent Number	Title
8,913,402	Triple-damascene interposer
7,595,527	Non-volatile electromechanical field effect devices and circuits and methods of forming same
6,476,635	Programmable number of metal lines and effective metal width along critical paths in a programmable logic device
6,436,195	Method of fabricating a MOS device
6,190,973	Method of fabricating a high quality thin oxide
6,165,846	Method of eliminating gate leakage in nitrogen annealed oxides
6,156,653	Method of fabricating a MOS device
5,978,127	Light Phase Grating Device
5,631,180	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,498,896	High threshold metal oxide silicon read-only-memory transistors
5,389,565	Method of fabricating high threshold metal oxide silicon read-only-memory transistors
5,338,423	Method of eliminating metal voiding in a titanium nitride/aluminum processing
5,317,187	Ti/TiN/Ti contact metallization
5,244,831	Method of doping a polysilicon layer on a semiconductor wafer
5,240,880	Ti/TiN/Ti contact metallization
4,895,520	Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant
4,824,803	Multilayer metallization method for integrated circuits

PROFESSIONAL MEMBERSHIPS

• National Science Foundation, Electronics & Nanotechnology Phase I & II SBIR Reviewer •
• Gerson, Lehrman Group: Leader (Top 5%) Council member •
• Chair Emeritus, and Founding Member, IEEE San Francisco Bay Area Nanotechnology Council •
• IEEE National Chapter of the Year Award, 2013 •
• Executive Committee Member, IEEE Santa Clara Valley Section •
• Member, Silicon Valley Engineering Council Steering Committee •
• Senior Member, IEEE •
• Member, Sigma Xi •
• Member, New York Academy of Science •
• Chair, Vistage International 2010-2015 •
• Security Clearance: Secret •

SEMINARS, TUTORIALS & WORKSHOPS

• ESD Association Tutorial: "Prevention of Electrostatic Discharge to Electronic Devices, Assemblies, and Systems." 1998 •
• Juran Institute, "Juran Management Systems," 1989 •

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SOFTWARE

DESIGN TOOLS:

SYNOPSYS: GALAXY DESIGN PLATFORM: DESIGN COMPILER, CUSTOM DESIGNER SE/DE/SDL, PRIMETIME, IC COMPILER, HSPICE, IC VALIDATOR, POWER COMPILER

CADENCE: AMS DESIGNER, ASSURA, SPECTRE, VIRTUOSO

MENTOR GRAPHICS: CALIBRE

TCAD:

SILVACO: ATHENA, ATLAS, VICTORY

OTHER TOOLS: VHDL, PYTHON, JSON, JMP, MATLAB, MICROSOFT OFFICE SUITE