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Die singulation technologies for advanced packaging: A critical review

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Die singulation, also known as wafer dicing, is reviewed in terms of the brief history, critical challenges, characterization of singulation quality, different singulation technologies and underlying mechanisms, and post-singulation die strength enhancement. Mechanical blade dicing has been the workhorse of die separation in the semiconductor manufacturing process. It faces growing challenges due to the adoption of copper/low- k dielectric interconnect structures, thin and ultra-thin wafers, die attach films, narrow dicing streets, and complex stacked structures on the dicing streets. Key dicing quality characteristics are chipping, delamination, kerf geometry, die side wall damage, die surface contamination, and die strength degradation. Various die singulation technologies have been developed to address these challenges and quality issues, including dicing by thinning, laser based approaches, laser and mechanical hybrid method, and plasma dicing. Die strength is a critical parameter for thin and ultra-thin dies. Post-dicing die strength enhancement is becoming the complement of most dicing technologies to achieve dies with high fracture strength. Plasma dicing has the potential to achieve much higher die strengths than all the other dicing approaches. © 2012 American Vacuum Society. [<http://dx.doi.org/10.1116/1.3700230>]

I. INTRODUCTION

Die singulation is also known as wafer dicing. It is a manufacturing process to separate apart the individual dies on a finished wafer via wafer dicing for further packaging and assembly (Fig. 1). Today, die singulation has been used for packaging and assembly of integrated semiconductor devices [e.g., memory, processors, and radio frequency integrated circuit (RFIC) devices], discrete semiconductor devices [e.g., small-signal transistors and diodes, resistors, and light emitting diodes (LEDs)], solar cells, and microelectromechanical systems (MEMS).

Wafer dicing dates back to around 1955, with its first format being scribing and breaking with diamond and later with laser.¹ During the 1960s and the 1970s, IBM used toothless gang saws in SiC slurry to dice silicon wafers.^{2,3} In the early 1970s, diamond blade sawing was introduced as the second format of wafer dicing. By 1983, fully automated in-line blade sawing systems were introduced to the market.¹ Over the years, blade sawing has been the workhorse of wafer dicing in the semiconductor manufacturing process, with continuous improvement being made to address process challenges and accommodate new design and application requirements. Since the last decade, the mechanical dicing approach has been facing many growing challenges from the development in wafer fab and advanced packaging technologies, emerging applications such as LEDs and MEMS, and the more stringent yield-driven quality control. A variety of new wafer dicing technologies have been developed to address these tough challenges, particularly for thin and ultrathin wafers.⁴ The early 2000s witnessed the emergence

of several important dicing technologies: Laser ablation based wafer dicing systems were offered to the industry for dicing via full-thickness laser cutting⁵ or by hybrid laser scribing/blade sawing.⁶ The dicing before grinding (DBG) process⁷ and “stealth dicing,” a laser induced subsurface separation technology,⁸ were also commercialized. Around the same time, the idea of applying plasma etching for wafer dicing was proposed.⁹ This contribution presents an extensive review of die singulation processes with an emphasis on the major challenges to wafer dicing, characterization of dicing quality, various dicing technologies and post-dicing die strength enhancement practice.

II. CHALLENGES TO DIE SINGULATION

A. Transition from Al/SiO₂ to Cu/low- k interlayer dielectric interconnect structures

Interconnects are charge carriers made of metal lines separated by an insulating interlayer dielectric (ILD). Due to the effective resistance (R) and capacitance (C) of the interconnect structures, the capacitive coupling of the metal lines to the ILD produces the RC delay. The advanced ICs are driven towards higher interconnect density and better interconnect performance (lower RC delay) in support of increased function integration and speed. Increasing interconnect density can be achieved by increasing the number of metal layers while shrinking interconnect dimensions. However, smaller metal cross sections and reduced wire spacing lead to a significant increase in R and C , causing a higher RC delay. In addition, higher resistance also induces increased power consumption and heat generation, reduced metal line spacing causes more crosstalk.^{10,11}

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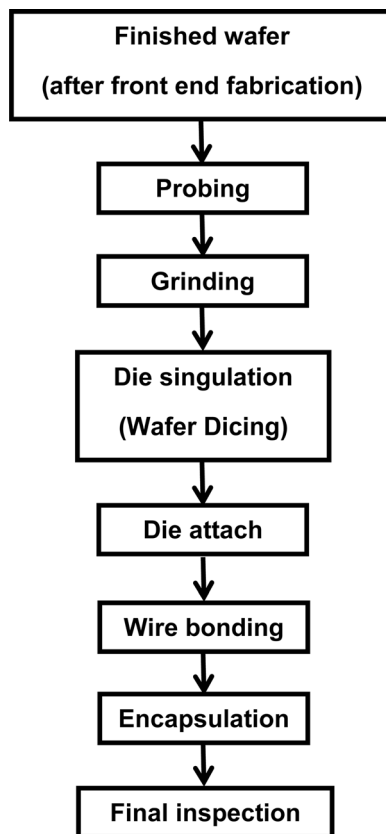


Fig. 1. Principal assembly process flow from finished wafer to final package.

As the interconnect structures transition from Al/SiO₂ ILD to Cu/low-*k* ILD, the RC delay can be effectively reduced due to the reduction of resistivity from aluminum (Al, 2.65–2.82 $\mu\Omega\text{-cm}$) to copper (Cu, 1.6 $\mu\Omega\text{-cm}$) and that of dielectric constant from SiO₂ ILD ($k=4.1$) to low-*k* ILD ($k\leq 3$). The introduction of Cu also significantly reduces power loss due to resistivity and improves the heat dissipation due to thermal conductivity.^{11,12} The International Technology Roadmap for Semiconductors (ITRS) has projected the adoption of low-*k* ILDs matching with the technology node shrinkage.¹³

The low-*k* materials have inherently weak thermomechanical properties. The elastic modulus of low-*k* dielectrics are typically below 10 GPa, while that of SiO₂ is ~ 70 GPa. The coefficient of thermal expansion (CTE) of low-*k* films are $\sim 10\text{--}17$ ppm/K versus 0.6 ppm/K for SiO₂.^{12,14,15} Particularly, the low-*k* films have very low fracture toughness and poor adhesion to adjacent films in upper and lower layers.^{14,16,17} This raises the concerns on the thermomechanical integrity during fab processing, wafer dicing, die packaging, and service. In fact, the poor adhesion induced thin film delamination and cracking issue has been identified as one of the key failure modes in chemical mechanical polishing (CMP)^{14,17–20} and packaging processes, including wafer dicing, die attach, wire bonding and molding. The delamination and cracking driving forces can come from the residual stresses within each layer, the thermal mismatch stresses in the low-*k* stacks, the global thermal mismatch of the package and the external loads.^{19–24}

Also, copper is more ductile than aluminum and will enhance the premature clogging of dicing blade, which adds additional loading to the blade to cause excessive chipping.²⁵

B. Thin wafers for thin dies

Dies for common microprocessor devices are typically 300 μm or thicker. Discrete devices (e.g., transistors, diodes, LEDs), devices for IC cards and mobile products (e.g., memory, logic, and microprocessors) have been moving rapidly from 150–200 μm thickness range to 50–75 μm or even thinner regime.

Basically, thin silicon dies enable two categories of applications: three-dimensional (3D) ICs and systems-in-foil (SiF).^{26,27}

Primarily, thin dies are needed to support 3D IC chip stacking in system-in-package (SiP) solutions for continued miniaturization and improved package functionality. In 3D system integration, multiple active dies that bear active and lateral interconnects as in the conventional planar ICs are vertically connected via through silicon vias (TSVs). Minimizing chip thickness will increase the planar TSV density by reducing TSV pitch and via parasitics; thus increase the effectiveness of TSV interconnects.²⁸ ITRS has projected the SiP technology trend with the number of chips per SiP and Si wafer thickness requirement.¹³

Secondly, thin dies enable flexible electronics and display development. Flexible electronics builds flip-chip packaging and chip assembly on flexible substrates and on textiles and therefore demands mechanically flexible chips,^{27–29} such as contactless smart cards and radio frequency identification (RFID) cards, biochips, and robot sensors/actuators.

Moreover, reducing wafer thickness improves heat dissipation of dies.^{25,27}

Thinner wafers are more flexible and tend to warp. Also, for a given die strength value, a thinner die translates into a lower value of allowable maximum load to avoid die fracture. This implies that handling of thin dies becomes very challenging and cannot simply follow the standard process steps for conventional thick die placement.^{30,31} Schnegg *et al.* listed the challenges and problems for thin die handling for die pickup, transfer and placement processes. These challenges include die cracking, no pickup, impact on neighboring die, die peel-off, ejection tool topography design, slow ejection, die bending, die warpage, die surface contamination, tool contamination, and poor recognition quality in visual die alignment if die warpage causes illumination issue.³¹ McCabe also pointed out the challenge to detach large, thinned dies from the tape without cracking.³²

In principle, the wafer thinning and dicing processes need to be optimized to ensure that a thinner die has an even higher strength than that for a regular thick die (i.e., to increase cracking/fracture resistance of the die) so that it can tolerate a relatively larger variation of the handling load during assembly. On the other hand, the assembly tools and processes need to be improved also in order to reduce the cracking/fracture driving force to achieve tighter control over the handling load.

C. Die attach films

Die attach films (DAFs), also called die bonding films, are thermoplastic die attach adhesives in dry film form and

are supplied in two different formats: A DAF laminated with a dicing tape which is called a D-DAF and a DAF without dicing tape. Regular DAFs can be used for die stacks incorporating dies of varying dimensions and/or configurations where the wire-bonds are completely encapsulated by mold compound. The so-called flow-over-wire (FOW) materials are another form of DAF materials that are used for stacking same-size dies where wire-bonds are partially in mold compound and partially in film adhesive. FOW films are formulated to incorporate die-attach film and dicing tape into one product. Since FOW films are designed to flow over the wire bonds of the die below the one being placed, the need for spacer die or sequential die staggering is eliminated.^{33–35} According to the way to release the dicing tape adhesive from DAF layer prior to die pickup, there are UV-curable DAFs and pressure sensitive DAFs.^{33–36}

There are thermally and electrically conductive DAFs, known as conductive DAFs, which contain silver (Ag) particles, and thermally-conductive but nonelectrically conductive DAFs, known as nonconductive DAFs, which contain aluminum nitride (AlN) particles or others to address different applications.^{37,38}

DAFs have become a preferred die attach material over conventional die-attach pastes in thin or ultrathin single die packages and multichip stacked packages featuring thin and ultrathin dies for the following reasons.^{33,39–43}

- (1) DAF material provides mechanical support to eliminate die warpage and breakage during post-dicing thin die handling (pickup, transfer and placement).
- (2) DAF offers better control of a series of die attach related issues, including: die tilt, resin bleed, creeping effect to die edge, bond line thickness, percentage of coverage and fillet around die side wall, and bubble at bonding interface.
- (3) DAF helps to reduce manufacturing steps and improve productivity.

Dicing through both the wafer and the laminated DAF layer can be more difficult than dicing through wafer only. For mechanical dicing of thin wafers laminated with DAF, the two common issues are DAF debris (“whiskers”) and die side wall cracking.^{39–41,43} DAF debris are smearing of DAF against the die side wall. Wang and Yo evaluated the performance of blade saw dicing a 100 μm thick silicon wafer.³⁸ The wafer is attached to either a conductive or a nonconductive DAF tape. It was found that due to the presence of Ag element in conductive DAF, the percentage of lateral cracking in the wafer with conductive DAF is 4 times higher than that with nonconductive DAF. The polymeric material and Ag filler in DAF are prone to be laminated onto blade surface during dicing under the local high temperature environment, which causes the blade to dull and hinders the exposure of new diamond grits to the blade surface. The dulling effect causes the blunt blade and its debris to push against the die being diced, creating additional load to the blade for more chipping.⁴¹ For smaller dies ($\leq 2\text{ mm} \times 2\text{ mm}$) with DAF, during pick and place process for die attach, severe die nonpick, loose dies and double dies pickup can happen. These issues can be improved to a certain extent through dicing process optimization.⁴⁴

Carbonization of laser induced polymeric materials is a well-known phenomenon.⁴⁵ For laser ablation based dicing, in addition to DAF debris, laser induced DAF carbonization is another concern to be understood.

D. Dicing street width reduction

Maximizing wafer real estate is an effective approach to cost reduction. Shrinking die size and narrowing dicing street width translate into more dies on a given wafer diameter. Ganesh and Lee estimated the benefit from dicing street reduction for a 300 mm wafer.⁴⁶ When the dicing street width reduces from 90 to 60 μm , keeping edge exclusion constant at 3 mm, for chip area of 6, 10, and 20 mm^2 the chip gain is 200, 120, and 40, respectively. For a typical 2 in. blue LED wafer on sapphire with die size of 250 $\mu\text{m} \times 250\text{ }\mu\text{m}$, reducing the street width from 50 to 20 μm will add 14% dies.⁴⁷ Fox reported that for their GaAs wafer products, street width reduction increases the amount of dies per wafer by 10–40%.⁴⁸

Reducing the dicing street width demands tighter control on kerf width and defect size (e.g., chipping) in order to meet the specified defect free zone (DFZ). DFZ is the distance from the edge of the street toward the kerf, within which chipping, cracking or other defects are not acceptable. When the aspect ratio of wafer thickness to dicing street width gets high, it becomes more complex for any wafer dicing technology, as both the amount of material removal and mechanical constraint increase accordingly.⁴⁶

E. Metal structures along dicing streets

On the front side of a wafer, there are commonly nonuniformly distributed alignment patterns and test element groups (TEGs) along the dicing streets. TEGs are test patterns that include representative devices and structures, such as transistors, diodes, capacitors, resistors, etc., and are designed to evaluate processes, circuit characteristics and reliability by cutting out and focusing on a certain section instead of directly testing the actual device patterns.^{49,50} TEGs for process evaluation are also known as process control monitoring (PCM) structures. TEGs are destroyed when the wafer is diced prior to packaging.

On the other hand, wafer backside metallization in combination with solder based die attach is widely adopted for high power semiconductor applications, such as discrete power devices, RF power amplifiers, high brightness LEDs, and laser diodes.^{51–53}

Moreover, with the introduction of TSV interconnect technology for 3D IC chip stacking, it is common to find TSV electrodes along the dicing streets.

The impact of all these metal stacks on wafer dicing differs for specific dicing technologies and needs to be understood.

F. Other more specific challenges

Wafer dicing also faces some other more specific challenges in the emerging applications as follows.

- (1) Free-shape dicing for dies with nonrectangular shapes, such as polygonal and circular dies as being used in some LED applications.^{54–56}

- (2) Dicing of 3D wafer scale integrated devices, in which multiple ultrathin wafers are vertically bonded together.^{57–59} Dicing process needs to go through different layers like metal-metal bond, epoxy adhesive wafer to wafer bond and very thin Si layers down to 10 μm . Potential defects would be delamination of bonded layers either due to the dicing process or due to poor adhesion between bonded layers.⁴⁶
- (3) Dicing of various MEMS devices: ITRS 2005 has broadly classified MEMS into RF MEMS, Bio MEMS, Inertial MEMS, and Optical MEMS.¹³ MEMS devices are fabricated in Si substrate using standard IC fabrication processes combined with various micromachining processes. These devices are very sensitive to mechanical pressure, contamination and electrostatic discharges.^{60–63} When the wafer scale capping is done using glass wafer as in some Bio MEMS and RF MEMS, it needs to dice through both glass and Si wafers, which is very challenging.^{46,64,65}

III. SINGULATION QUALITY CHARACTERIZATION

Wafers have the highest value at the die separation stage. Dicing does not add value to the finished dies, but it has a significant impact to die packaging and assembly yield. In many applications, wafer dicing has become the most challenging process to meet both yield and cost targets. Post-dicing package reliability tests have shown that severe dicing defects can cause die-level interconnection failures and/or structural integrity failures including die cracking and fracture.^{66–68} So, the quality of dicing process is measured by the yield loss it may cause.

Dicing quality factors attributed to potential dicing yield loss are summarized as follows.

A. Chipping

Chipping refers to a machining damage from dicing in which small fragments are removed alongside the die edge. Under monotonous or cyclic stresses induced by back-grinding, blade saw and/or laser dicing processes, microcracks are initiated. When these microcracks propagate along dislocation planes and join together, they cause a small fragment to flake off the die, resulting in a “chip-out” on the die.⁶⁹

Depending on its occurrence either at the top or bottom surface of the die, edge chipping is further partitioned into top side chipping (TSC) and bottom side chipping (BSC).^{70–76}

TSC, when propagating into the active circuitry area of the die, leads to a device failure. Small-sized TSC outside the sealing ring of the die may not cause immediate electrical failures, but can lead to a reliability failure later on. It may serve as an initiation point for full-blown die crack during subsequent packaging and assembly processes wherein the device is subjected to thermomechanical stresses.^{66–68}

BSC occurs on the bottom surface of the wafer. Over-sized BSC increases the sensitivity of the devices to thermal cycling and lower their reliability, especially for flip chip packages. When the back side of a die is exposed to the molding material during packaging, BSC can cause imperfect

molding, such as air bubbles near the chipping. During the packaging process, these bubbles may cause mold cracking, which can reduce yield.

BSC is more pronounced in polyimide-coated wafers where there are heavy metal layers in the streets, or where heavy back-grinding has produced high tensile residual stress at the bottom of the wafer.⁷⁰

TSC can be screened by post-dicing optical inspection after die attach easily.⁷⁵ However BSC cannot be easily detected after die attach as it will be covered by an epoxy compound.

Chipping specifications depend on specific applications and are largely determined by the wafer street width and kerf width. For example, in MIL-STD-883G METHOD 2010.11, a visible crack extending from the backside of the die upwards to a height more than 50% of die thickness is rejected irrespective of its absolute length.⁷⁷ Typically, in mechanical blade dicing, the maximum allowable TSC is essentially half the saw street width minus half the blade thickness.⁷⁸

B. Kerf geometry

Kerf geometry includes kerf width, kerf perpendicularity and kerf straightness.⁷² For high yield packaging and assembly, it is essential to control the variations of kerf geometry.

Kerf width is of primary interest in terms of its achievable minimum size and the tolerance of its variation, i.e., kerf width consistency. A consistent and minimized kerf width capability enables the reduction of dicing street width; thus increasing the potential for the addition of dies on a wafer.

Kerf perpendicularity is a depth-wise measure of the tilt of a cut and the kerf width consistency (e.g., kerf taper, top-side chamfer, and bottom-side U-shape lip). It is important for applications where the die sidewall is functional in the end product.⁷²

Kerf straightness measures the eccentricity or the waviness (lateral deviation) of the kerf from dicing direction, i.e., the offset from the center of the kerf to the center of dicing street. In the extreme case, an over-sized die can be generated, which, even perfectly free of defects, is too large to fit in the package or obstructs the bond wires.⁷⁵

Kerf straightness is also known as cutting offset,^{79,80} or cut placement accuracy.⁷¹ The cut placement accuracy is a major root cause of the kerf eccentricity.

C. Die side wall damage^{81,82}

The side walls of a die have both detectable and non-detectable defects induced by a dicing process. These defects include scratches, microcracks, microdeformations and microstructural modifications, resulting from the mechanical or thermal stresses associated with the dicing process used. The depth and severity of die side wall damage in the case of mechanical dicing, is similar to the damage caused by mechanical grinding. While in the case of laser dicing, a detailed characterization of the heat affected zone (HAZ) will be helpful to estimate the side wall damage.

D. Die surface contamination

Contamination of die surface comes in different ways. Dust residue on the terminal pads can reduce the reliability of wire bonds to these pads.⁶⁹ Burrs or debris are formed on the front and back surfaces as well as the side walls of a die, especially when dicing wafers with metallization layers or wafers laminated to DAFs and dicing tapes.^{72,81–83} The polymeric residues from the DAF or dicing tape material left on the die are sometimes called whiskers.^{39,40}

Laser induced pyrolysis and carbonization of polymers is a well-known phenomenon in laser ablation of polymers such as laser microvia drilling in printed circuit boards.^{43,84} When a wafer laminated to DAF is diced via laser ablation process, it is expected that laser irradiation can cause carbonization of DAF in addition to DAF splashes. The resulting electrical conductivity of the carbon and carbon-rich residues can cause device failures. Deposition of minute particles is directly proportional to the electric field from the electrostatic charges due to the Coulomb forces.⁶⁰

E. Electrostatic discharge

In mechanical blade dicing, electrostatic charges may originate from the movement of the substrate between the different stations in the saw. For example, these electrostatic charges can be developed in high pressure cleaning stations due to high resistivity deionized water sprayed onto wafer during high speed sawing.⁷⁰

Electrostatic discharge (ESD) is known to be harmful for the devices. In MEMS devices, ESD can cause physical damage in the form of localized scorching which then can lead to malfunction of sensitive electronic components. In mechanical dicing, deionized (DI) water is often used as the coolant for its purity and lack of dissolved ions. However, this low conductivity water can lead to electrostatic charges build-up, due to its inability to carry electrostatic charges away from the substrate being diced.⁶⁰

F. Metal/ILD delamination and peeling

Metal/ILD delamination and peeling are the unique failure patterns for low- k wafer dicing. Peeling results from very severe delamination. They are attributed to the significantly low mechanical strength of low- k dielectric material and its poor adhesion with adjacent materials.^{85–87} Another unique failure pattern for low- k wafer dicing is discoloration of top metal layer. The physical mechanism is unknown.⁸⁶ However, its occurrence at die corner may be associated to the more severe stress state at die corners.

In order to mitigate or stop the propagation of metal/ILD delamination and peeling into the active device area, edge sealing ring, also known as guard rings or crack stops, are built surrounding each die. The crack stops are essentially trenches formed in the dielectric layer along the periphery of the chip and filled with copper during the electroplating process.^{46,88–92} These approaches will also help to prevent the moisture penetration into the devices which is not desired.⁹²

G. Die strength and dispersion

Chip strength is dramatically degraded by various defects originated from wafer grinding and dicing processes. Die strength characterization helps to understand the severity of various defects, including chipping, side wall damage, and delamination, etc. It can be also used to define the susceptibility to die fracture failure during assembly processes or reliability tests. For example, die may fail due to fracture or cracking during pickup at die attach process,⁸³ during molding process with extremely high molding pressure, or during wire bonding onto thin stack structure.⁹³

Uniaxial flexure tests, such as three- or four-point bending (3PB or 4PB), and biaxial flexure tests such as ball-on-ring bending (BOR) are commonly used for fracture load determination of brittle materials and has been adopted for die strength measurement.^{79,81–83,94–97} Uniaxial flexure tests are used for dicing process evaluation to determine the influence of both the surface and edge flaws. Biaxial flexure tests mainly involve the surface flaw effect and so are often used for wafer thinning process evaluation.⁹⁸ Specifically, technical instructions for 3PB tests of thin film silicon dies are given in the SEMI standard G86-0303.⁹⁹

In the 3PB measurement, usually die fracture strength σ_f is calculated by Eq. (1) derived from linear beam theory:

$$\sigma_f = \frac{3FL}{2Bh^2}, \quad (1)$$

where F is the loading force at fracture, L is the loading span, B is die width, and h is die thickness.

Information in the following sections helps with interpreting the die strength data from both direct experiments and literature.

1. Validity of Eq. (1)

Equation (1) is based on the classical linear beam theory. For very thin silicon chips, due to its high flexibility, the loading force versus deflection response curve may become highly nonlinear and the deflection at fracture can be several times larger than the die thickness. This leads to a nonlinear relationship between force and stress and Eq. (1) becomes invalid. Numerical approaches taking into account the geometrical and structural nonlinearity effects are needed to translate force value at fracture into die strength σ_f ,¹⁰⁰ which is not always easily available.

2. Dispersion of die strength

Brittle fracture theory applies to silicon and sapphire based dies at ambient conditions. Brittle fracture is of statistical nature, which means that the strength varies unpredictably from die to die even if a set of nominally identical dies out of a same wafer are tested under the same conditions.¹⁰¹ Therefore, both its mean value and its dispersion are needed to better characterize die strength. Weibull theory states that $P_f(\sigma_f)$, the fracture probability at the strength level σ_f , follows¹⁰¹

$$P_f(\sigma_f) = 1 - \exp \left[- \left(\frac{\sigma_f - \sigma_{th}}{\sigma_0} \right)^m \right], \quad (2)$$

where σ_0 is a characteristic strength, σ_{th} is the threshold stress (below which no failure will occur), and m is the Weibull modulus. When $\sigma_{th} = 0$, Eq. (2) reduces to two-parameter (σ_0, m) Weibull statistics.

Here, the Weibull modulus is a measure of the degree of strength dispersion, and is also called the shape factor. A high m value corresponds to a narrow dispersion or scattering of the strength data and vice versa. Therefore, the m value can be used to gauge whether the dicing quality is consistent or not for a given dicing technology. On the other hand, the values of average die strength (σ_f) and the Weibull modulus (m) can be also used to compare the severity of damage to die resulting from different dicing technologies. This can be done because the degree of strength dispersion inherently corresponds to the defect population in a die introduced by a specific dicing process.

In industrial applications, the so-called minimum die strength, which is the die strength at a failure probability of 1%, is often used to characterize the die strength.¹⁰²

3. Dependence of die configuration and loading condition

Brittle fracture can be initiated from volume and/or surface flaws. For the convenience of discussion, assuming that it is initiated from surface defects only and the two-parameter Weibull statistics applies, Eq. (2) can be further expressed as¹⁰¹

$$P_f(\sigma_f) = 1 - \exp \left[-k_0 \frac{A}{A_0} \left(\frac{\sigma_f}{\sigma_0} \right)^m \right], \quad (3)$$

where A_0 is a characteristic area and can be taken as a unit area, A is the effective die surface area and k_0 is a nondimensional parameter. k_0 is a function of the physical (material) properties, geometrical configuration, the dominant fracture mechanism reflected by the specific fracture criterion selected,¹⁰³ the flaw distribution and the loading condition.

The dependence of die strength on its physical (material) and geometrical configuration, fracture mechanism, flaw distribution and loading condition highlighted by Eq. (3) can explain the die size effect on die strength on a given type of die.^{94,104} In addition, Eq. (3) also sheds light on the difference of die strength from an expensive functional device wafer versus from a low cost dummy wafer,¹⁰⁴ 3PB versus 4PB,⁹⁴ as well as the difference between die front side strength (device layer in tension) and its back side strength (device layer in compression).⁹³

For very small dies such as LED dies which are typically less than 1 mm × 1 mm, the conventional 3PB, 4PB, and BOR tests are not applicable to determine their strength. Chen *et al.* evaluated LED die strength using the point-load test (PLT) and line-load test (LLT),¹⁰⁵ which are associated with a plate-on-elastic-foundation configuration.¹⁰⁶

IV. DIE SINGULATION TECHNOLOGIES

A. Scribe and break

The scribe and break approach is a two-step process, where a scribe line is created first with certain depth and sharpness in the wafer surface along a dicing street to establish a stress concentration factor. Next the wafer is cleaved along the scribe line under applied static or impact loading via noncontact (exposed air bridges) or contact (“anvil”) mechanism.

Scribing methods include diamond scribing, diamond blade sawing, wet or dry etching,^{107–109} and laser scribing.^{110,111}

The reported yield of dicing GaAs and LED sapphire wafers using diamond-scribe and break is in the range of 90–98%.^{48,112–114} In essence, the yield is determined by the geometrical accuracy of separated dies and therefore depends heavily on how well the stress concentration/crack initiation is prepared in scribing step and how accurately cleavage propagation in the breaking step is controlled. Major factors affecting yield are as follows.

- (1) Discontinuity or interruption of the scribe line misdirecting the break. This can happen at the locations of PCM structures, nitride films and metal layers on dicing streets.^{111,115} Backside street trench etching is needed prior to scribing for wafers with backside metal.¹¹⁶
- (2) Edge cracking and chipping. In the case of diamond scribing, both radial and lateral cracks are also introduced, in addition to the median crack being created underneath the scribe line for controlled cleavage propagation in the break step. These are responsible for chipping and are very sensitive to scribe tip geometry and load.^{117,118} Figure 2 is an example of subsurface median crack and lateral crack induced by scribing a GaAs wafer, reported by Wasmer *et al.*¹¹⁹ The median crack is induced under the surface along the {110} cleavage plane, while the subsurface lateral cracks and the microcrack just below the scratch develop randomly.

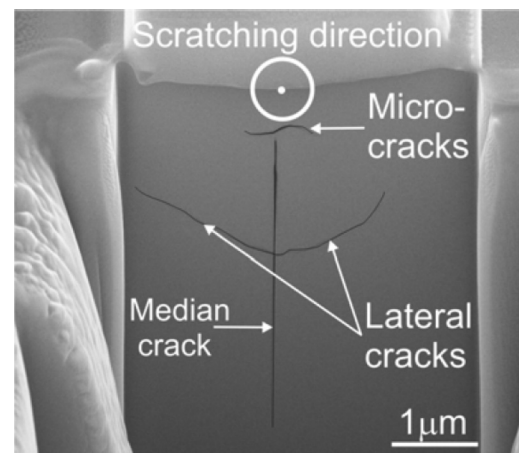


FIG. 2. SEM cross-section prepared by a focused ion beam (FIB) of a scribe made by a diamond tip on a GaAs wafer. Lateral, median, and microcracks underneath the scribe are shown. Courtesy of K. Wasmer, Laboratory for Advanced Materials Processing, Empa—Swiss Federal Laboratories for Materials Science and Technology, Switzerland (Feb. 2012). Details of the related description refer to Ref. 119.

(3) Depth and sharpness of the scribe line. A higher scribe depth to notch radius aspect ratio translates into a higher stress concentration factor and ensures a well guided and clean break. On III-V materials, typically, diamond scribing produces a cut of 3–5 μm in both depth and width with a sharp median crack being formed at the bottom of scribe at 10–50 mm/s.^{111,115,120} Diamond blade sawing typically delivers a cut of 30 μm or more in width and 10 μm or more in trench radius at 3–15 mm/s for an acceptable cutting quality.^{115,120,121} A diode pumped solid state (DPSS) ultraviolet (UV) laser can create less than 3 μm wide and 15–40 μm deep V-notch shaped scribe at a speed of 100 mm/s or more.¹¹¹

In the past 10 years, DPSS UV laser scribing has gained popularity in scribe and break applications since it delivers much better scribe line continuity, less chipping and side cracking, and a higher scribe depth to notch radius aspect ratio over diamond scribing techniques.

Since the early 1970s, the scribe and break process has been replaced by blade sawing in mainstream semiconductor device production with much consistent die geometrical accuracy. Nevertheless, scribe and break approach has also found some niche applications in separating thin discrete III-V compound semiconductor devices. The mechanical blade saw dicing is less cost-effective for GaAs devices and GaN-LEDs on sapphire substrates due to the following reasons.^{1,115,120,122}

- (1) Wafers made out of sapphire and III-V materials are very difficult to saw because they are inherently brittle and chip easily.
- (2) Sapphire and III-V semiconductor wafers have much narrower dicing streets compared to Si semiconductor wafers, to conserve these expensive materials. Dicing streets are as narrow as 20 μm with die size 350 $\mu\text{m} \times 350 \mu\text{m}$ or less on the compound semiconductor and LED wafers today.
- (3) The scribe lines are aligned to the cleavage plane for GaAs wafers, because single crystal GaAs has the *zinc-blende* structure, similar to the *diamond* structure of silicon [Fig. 3(a)]. Its preferential cleavage planes are the $\{110\}$ family, which are orthogonal to the $\{100\}$ crystal planes. GaAs devices are commonly produced in the (100) crystal plane configuration in favor of the optimum electronic properties in the wafer surface. When scribing a (100) surface along the $\langle 110 \rangle$ directions, the median crack being created underneath the scribe line propagates in the $\{110\}$ cleavage planes to form straight fractures leading to rectangular dies.

Scribe and break of silicon wafers is more complicated due to its crystallographic anisotropy. Silicon has the *diamond* structure with two principal cleavage planes, $\{111\}$ and $\{110\}$. The $\langle 110 \rangle$ propagation directions, as the easiest slip direction family, are preferred on both cleavage planes. The crack propagation on the $\{110\}$ plane is very anisotropic, whereas the cleavage anisotropy on the $\{111\}$ plane is very minor.^{123,124} So the $\{111\}$ planes are the preferred or natural cleavage planes.¹²⁵

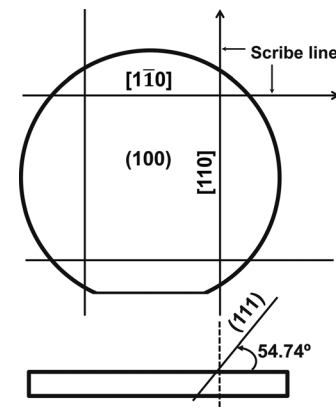


Fig. 3. Cleavage planes $\{110\}$ of (100)-plane GaAs and Si wafers. Note that the scribe lines are aligned with the $\langle 110 \rangle$ directions.

On a (100)-plane silicon wafer, the preferred cleavage planes $\{111\}$ intersect with the surface plane (100) along the $\langle 110 \rangle$ directions at an angle of 54.74° (Fig. 3). Crack naturally propagates also along $\langle 110 \rangle$ directions to form rectangular dies when scribing along the $\langle 110 \rangle$ directions.¹²⁵ However, crack propagation can deflect out of the $\{110\}$ planes onto the $\{111\}$ planes, resulting in the angle between the side wall of die and its front or back surface to be $\sim 55^\circ$ – 60° .^{98,126} On a (111)-plane silicon wafer, the three other natural cleavage planes $\{111\}$ intersect with each other at an angle of 60° and with the surface plane (111) at 70.53° along the $\langle 110 \rangle$ directions as shown in Fig. 4.^{74,125} When dicing along $[11\bar{2}]$ horizontally and $[\bar{1}10]$ vertically to get rectangular dies, only two sides along $[\bar{1}10]$ directions follow straight fracture along cleavage planes. The other two sides of the die along $[11\bar{2}]$ directions will have jagged edges and ladderlike shell appearance of chipping as cleavage propagation tends to deflect onto the easiest slip directions $\langle 110 \rangle$ in the natural cleavage planes $\{111\}$.^{74,125}

B. Mechanical blade dicing

Mechanical blade dicing is a grinding process in which material is sheared away from a wafer by diamond grit abrasive embedded on the edge of a rotary annular blade (disc). In other words, a blade saw machine for wafer dicing is a derivative of precision grinding tools. During dicing process, the dicing blade as a thin grinding wheel is rotated at a high speed (30 000–60 000 rpm) to grind the wafer leading to the formation of a complete cutting (full cutting) or incomplete cutting (half cutting). Mechanical blade dicing has evolved into the predominant wafer dicing technology for semiconductor die singulation since 1970s.

1. Blade dicing quality

Thanks to numerous studies on the dicing process, the associated quality issues for potential yield losses have been well understood, as summarized in Sec. III.

Grinding of a wafer made of highly brittle materials (e.g., Si, GaAs, and sapphire) with a dicing blade is categorized as brittle-mode machining which causes chipping in the front

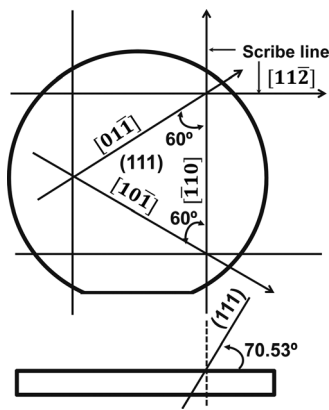


FIG. 4. Cleavage planes $\{111\}$ of (111)-plane Si wafers. Note that the scribe lines are aligned with the $\langle 112 \rangle$ and $\langle 110 \rangle$ directions.

and back surfaces of the wafer. Chipping can impact packaging reliability and yield as it functions as a stress concentration site to cause die cracking and fracture under the external loading during die pick and place operations and due to the thermal stresses from the thermal expansion mismatches of packaging materials. Chipping can be reduced but hardly eliminated and therefore has remained as a major quality item for improvement.¹²⁷ However, very few fundamental studies have been found investigating the chipping mechanisms in dicing silicon wafers. Since blade dicing is a mechanical grinding process in its physical nature, each multifaceted grain of abrasive bears an analogy to a microscopic single-point cutting edge, a microindenter and a microscratcher. So understanding of dicing-induced chipping mechanism can benefit from previous studies on grinding,^{128–130} indentation^{131,132} and scribing/scratching^{117–119,133} of hard and brittle materials.

Lundt *et al.* stated that grinding of silicon wafers would cause unavoidable subsurface damage.¹²⁹ Pei *et al.* observed six different configurations of subsurface cracks in ground silicon wafers, namely, median, lateral, “umbrella,” “chevron,” “branch,” and “fork” cracks.¹³⁰ It was reported that the indentation-induced median and radial cracks in (111) surface oriented silicon crystal and other brittle materials during loading and unloading cycles can be attributed to sessile dislocation reactions that are initiated at micro-slip system intersections.^{131,132}

Similar to the cases of GaAs wafer scribing,^{117–119} studies also found three types of cracks created in diamond scribing of silicon wafers namely, median, lateral and radial (or chevron) cracks.¹³³ The median crack propagates downwards, which is the objective of the scribing process. Lateral and chevron cracks may lead to chipping on either side of the scribed trench. Moreover, the chevron cracks can guide the median crack out of the scribing direction onto a preferred cleavage plane due to the crystallographic anisotropy of silicon, leading to undesired fracture or chipping.

Luo and Wang studied the chipping mechanisms for blade dicing of silicon wafers.⁷⁴ During the blade dicing process, the multifaceted diamond grits also induce both radial and lateral cracks similar to the cases in grinding, indentation

and scribing processes. In addition, median cracks are formed underneath the diamond grit tip within the dicing trench. The dicing direction dependence of chipping size was investigated on $\{100\}$ and $\{111\}$ plane oriented Si wafers. The chipping modes were broadly classified into four types including 30° chipping, 60° chipping, 90° chipping, and irregular chipping according to the angle between the shell appearance of chipping and the dicing direction (die edge). It was concluded that as the 30° -, 60° -, and 90° -oriented radial cracks along the preferred slip direction family $\langle 110 \rangle$ meet with the lateral cracks along the preferred cleavage plane family $\langle 111 \rangle$, different chipping modes are generated.

Miwa and Inasaki considered the dicing force to understand the mechanism of dicing.⁷³ It was confirmed that the dicing processes are more concerned with the material removed by both sides of a blade in comparison with single side removal in the conventional grinding. Also, wafer chipping and blade wear increase as the cutting force on a silicon wafer increases. The dicing force itself increases as feed rate and dicing depth increase or blade speed decreases in the down-cutting mode. Conventional blade dicing systems adopt a constant feed rate mechanism and the dicing force inevitably varies during the dicing process with the dynamic change of blade and wafer surfaces. Factors such as dislodgment or dullness of diamond grits, and the transition from regular street location to TEGs or metal layers affect the dicing force. The dicing force has been also characterized by the blade torque.^{71,134–136} Chipping size increases with blade torque. Blade torque is correlated to all process parameters such as blade speed, blade vibrations and wear rate, cooling condition, feed rate, wafer thickness and sensitive materials in dicing street. For each set of process parameters, there is a torque value limit, above which dicing quality deteriorates and severe BSC appears. Therefore, online measurement of blade torque has been implemented to monitor the dynamic process variations.^{135,136}

Semiconductor wafers by nature are inhomogeneous due to the presence of passivation layers (oxides, nitrides, and polymers), metal films, and TEGs. This heterogeneity is further enhanced by the foreign materials adhered to the wafers, such as DAF and mounting tapes at the backside of a wafer and the polymeric protective mask layers on the active side of a wafer. During the dicing process, the thermally softened metals and polymeric materials are inclined to remain on the blade by laminating into the microscopic “gullet,” i.e., the free space in between the abrasive grits on the electroplated nickel matrix (binder). This is called blade clogging or blade overloading.^{72,127,137} The blade clogging brings about two negative consequences. First, it makes the worn and loosened abrasive grits hard to come off and fresh grits difficult to expose; thus blunts or dulls the blade edge. Second, it blocks the free paths for cutting debris or chipping removal and the trapped debris are pushed against the surfaces of the dicing trench being formed. These create local stress-risers at the dicing trench and overload the blade edge which can lead to more severe chipping, wavy cuts, slanted cuts, blade side vibrations, microcracking, and blade failure.⁷²

Another major defect is the metal/ILD delamination and peeling in blade dicing of low- k dielectric silicon wafers. Volinsky *et al.* used a cube corner indentation method to study the delamination behavior in the Cu/low- k dielectric structure.¹⁶ It was found that the delamination-induced interfacial cracks kinked into the low- k film itself; thus indicating competition between adhesive and cohesive failure mechanisms. The interfacial delamination can be reduced to certain level through process optimization, but a complete elimination is not achievable due to the nature of mechanical contact for blade dicing approach and the intrinsically very low fracture toughness and poor adhesion of low- k film to adjacent films.⁸⁶ Sealing rings are incorporated to act as a crack arrester by increasing the fracture resistance near the edge of the chip to prevent delamination/cracking from propagating into the circuitry area of a die.^{88-92,138,139}

Various factors affecting dicing quality have been widely discussed.^{72,140,141} A brief summary is given in the fishbone diagram in Fig. 5 to illustrate the complexity.

2. Blade dicing process characteristics

From the very beginning, mechanical blade dicing systems were based on a single spindle. Dual-spindle dicing systems were developed in the 1980s for dicing throughput enhancement.¹⁴² They turned out to benefit more to improve dicing quality by enabling the two-step blade dicing process. The two-step process, also known as “step cut,” has become the universal blade dicing solution to address various challenges from adopting narrow dicing streets,⁷⁸ low- k dielectric/copper interconnect structures,^{85-87,143} passivation

layers (oxides, nitrides, and polymers), front and back side metal films,⁷⁹ TEG and alignment patterns, and DAFs.^{38-41,44} In the first step, a partial cut with a first blade (thick) is made into the wafer to reduce top side chipping and delamination. In the second step, the remaining thickness of the wafer and certain portion of mounting tape is cut through using a second blade (thin) to achieve reduced backside chipping (see Fig. 6). The three dicing parameters for adjustment include spindle speed, wafer feed-in speed, and cut-in depth for each blade.

Wang *et al.* used the step cut process to dice 300 mm C90 dual damascene low- k (BD1) silicon wafers.⁸⁶ The first blade is a Ni bond diamond blade with low-concentration 2–4 μm grits and a relatively soft binder. It cuts into certain depth of silicon with the intention to remove low- k layers and achieve less top-side peeling/delamination and chipping. The second blade is Ni bond diamond blade with high-concentration 4–6 μm grits and a harder binder. It cuts through the silicon and reaches 1/3 of the mounting tape, with the intention to reduce backside chipping.

Jiun *et al.* used the step cut process to dice 100 μm thick wafers laminated with DAF to reduce backside chipping.¹²⁷ Both conductive and nonconductive DAFs were investigated. In a single pass dicing process, silver fillers in the conductive DAF causes blade overloading. This leads to more severe backside chipping than in the case of using nonconductive DAF. The step cut has reduced the backside chipping when the first step diced through the wafer and cut into DAF with a low percentage (0–30%) in thickness.

The advantage of step cut lies in the freedom to select two different blades to match the specific material layers on

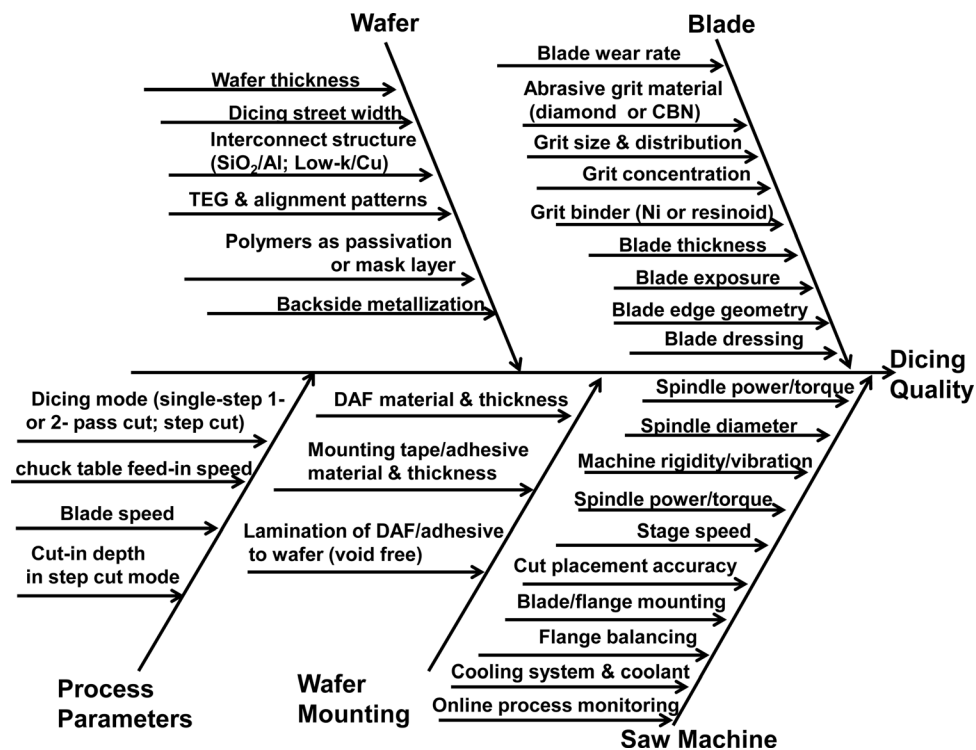


FIG. 5. Blade dicing quality fishbone diagram for dicing a silicon semiconductor wafer mounted on an adhesive tape. Factors affecting dicing quality are categorized as blade, saw machine, wafer, wafer mounting, and process parameters.

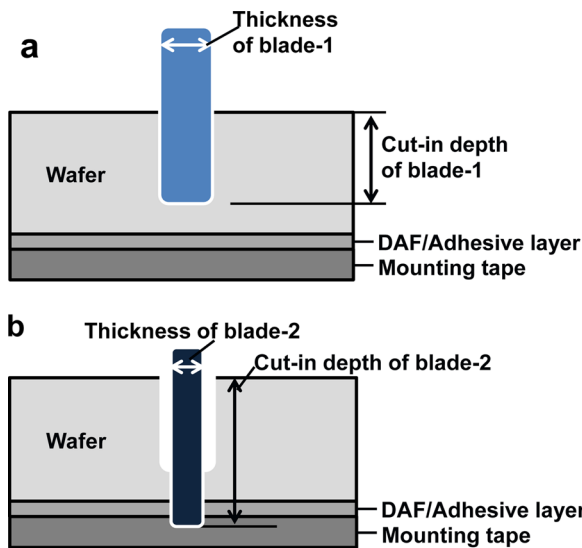


FIG. 6. (Color online) Schematic two-step blade dicing process. (a) Step 1: dicing partially into wafer substrate; (b) step 2: dicing into mounting tape.

the front and the back side of a wafer. A more optimal balance of reducing chipping on both sides, e.g., the topside chipping from TEGs and backside chipping due to the adhesive of the dicing tape, can be achieved.

Some disadvantages remain for mechanical blade dicing as follows.

- (1) The universal step cut mode reduces productivity by about 50% compared to single cut mode. The step cut process is realized on a same dicing machine. Typically at least one of the two sequential steps is set at low feed rate to cut through the specific chipping-sensitive layers. So the overall throughput decreases significantly.
- (2) Step cut mode typically delivers a wider saw kerf than single cut, as the second-step cut demands certain placement accuracy over the first-step cut. The wider kerf does not support the general trend towards a narrower dicing street. It is not economically efficient to achieve less than 30 μm kerf widths with mechanical blade dicing.
- (3) Step cut mode does not yield less topside chipping than single cut mode in the presence of TEGs and metal layers. Luo *et al.* studied the blade dicing process on wafers with 6–12 μm thick aluminum pads on the dicing street.⁷⁹ With step cut mode, top side chipping at aluminum pad sites did not meet the specifications even after the DOE-based process optimization. A low speed single cut process was developed to reduce the topside chipping.
- (4) Mechanical blade dicing can cause catastrophic wafer breakage damage for 100 μm or thinner wafers, especially for ultrathin wafers ($\leq 50 \mu\text{m}$). Blade dicing inevitably involves mechanical contact with wafers and introduces mechanical stresses in the wafer. It determines that either step cut or single cut can only reduce chipping and delamination rather than eliminate them. Moreover, as wafers get thinner, the risk rises to cause catastrophic wafer breakage. Gatzen and Guenzel used five different electroplated dicing wheels of 15 and

100 μm in thickness with different grain size and concentration of diamond grits to dice 50 μm bare silicon wafers.¹⁴⁴ A 15 μm wide blade of 2–4 μm grit size achieved less than 10 μm chipping. Such a thin blade is very susceptible for breaking. All the other combinations gave 10 to 30 μm wide chipping.

- (5) As blades wear during dicing, dicing quality becomes inconsistent. Frequent blade replacement helps to reduce the inconsistency, but it adds cost burdens and decreases the productivity.

C. Dicing before thinning

The standard semiconductor manufacturing process flow adopts the “dicing after thinning” approach. In this method, semiconductor elements are patterned on a wafer, followed by wafer thinning to its target thickness through back side grinding (BSG) processes, followed by dicing to form separated dies. For a 300 mm silicon semiconductor wafer, when wafer thickness is above 100 μm , the conventional “dicing after thinning” approach works well. However, when the wafer is thinned to below 100 μm , it easily warps and becomes very susceptible to breakage or cracking at handling and dicing. Post-grinding “mirror finishing” processes such as dry polishing, wet etching, dry etching, and CMP as stress-relief treatment reduce but do not eliminate breakage or cracking.

As an effort to resolve these issues, the dicing-before-thinning approach, also called “dicing by thinning,” has been explored for thin and ultra-thin wafers, which reverses the usual “dicing after thinning” process sequences.^{145–150} In the principal process flow for dicing-before-thinning, first a wafer is partially diced from its front side to the desired final die thickness by diamond blade sawing or scribing probe,^{145,149} laser scribing, wet etching or plasma etching or their combinations.^{146–148} Secondly, the wafer is transferred on to a carrier tape with its front side attached to the carrier tape. Thirdly, backside thinning processes take place to physically separate individual dies, in which various processes including grinding, wet etching, dry etching, and CMP can be combined. Then the separated dies are transferred onto a tape carrier for pick-and-place operation in subsequent assembly.

Currently, the commercially available dicing-before-thinning approach is the so-called “dicing before grinding” (DBG) technology.^{151–157} In an in-line DBG (Fig. 7), the wafer is precut with a blade saw and then thinned by BSG below the level of this cut. BSG starts with rough grinding at relatively high speed with coarse grinding means containing large sized diamond grains, followed by precision grinding at relatively low speed with fine grinding means containing small-sized diamond grains. DBG induces residual stress layer on the ground back side and dicing saw mark on the side wall. These can lead to die-level warpage or cracking during pick-and-place process. Therefore, as in the case of “dicing after thinning,” stress relief after BSG becomes a necessity for die strength improvement by performing “mirror finishing” processes such as dry polishing, wet etching, dry etching, and CMP.^{151,158–162} Next, the

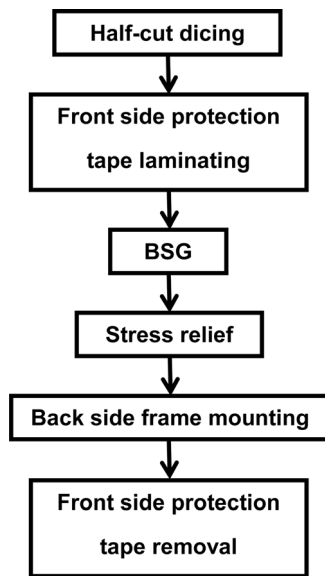


FIG. 7. Principal DBG process flow.

wafer is mounted on a DAF tape, followed by removal of the device side surface protection tape.

In DBG, transportation of thinned wafers is not needed, so wafer-level warpage and breakage are avoided. Also the backside chipping can be controlled to below $5\ \mu\text{m}$.^{151,152} With DBG, $25\ \mu\text{m}$ or thinner dies can be produced.

After DBG process, the DAF needs to be diced by a laser.¹⁶² However, dies shift from their original locations after DBG. This implies DAF must be cut by laser after measuring and aligning the die to die center position, which is time consuming.¹⁶³

D. Ablative laser dicing

Ablative laser dicing refers to the wafer dicing process by laser ablation, in which material is removed via evaporation and melt ejection under irradiation of laser pulses. Numerous studies have been conducted on ablative laser dicing, mostly on blank silicon wafers.

1. Tradeoff between laser processing speed and quality

Laser ablation process efficiency is typically measured by ablation depth per pulse known as ablation rate. The ablation rate is a function of the optical and thermal properties of material and laser beam characteristics including laser wavelength, pulse width, optical spot size, beam quality, pulse energy, pulse repetition frequency (PRF), and number of pulses overlapped. The pulse energy density, i.e., the fluence (F), as the pulse energy per unit area of optical spot, is a measure of the combined effect of pulse energy and optical spot size; while the peak optical power intensity (I), measured by the pulse fluence per unit time, quantifies the combined effect of pulse energy, pulse width and optical spot size.

For a homogeneous material, when laser wavelength and pulse width are fixed, for a given process condition, the

dependence of ablation rate on laser fluence (or intensity) approximately follows the logistic curve as illustrated in Fig. 8. This curve can be divided into three zones. Zone 1 denotes the region below the ablation threshold F_{th} . In this regime, laser irradiation can cause thermal stresses and change of material microstructures and properties (the so-called material modification or degradation), although no ablation occurs. Zone 2 is the lower shelf region between the threshold fluence F_{th} and transition point (F_c). In this region, ablation rate is very low but the processing quality is good in terms of ablation morphology such as kerf smoothness, severity of chipping or cracking, debris size and distribution, and HAZ dimension. In zone 3, ablation rate dramatically increases with the increase of laser fluence and may get saturated, while the processing quality degrades significantly and the dimensions of the ablation generated features is less controllable.

The transition curve shifts horizontally as laser wavelength, pulse width or pulse overlap changes for different materials. Nevertheless, the ablation rate versus fluence as depicted in Fig. 8 remains similar for a wide spectrum of materials and for a variety of lasers, regardless of the specific differences in the physical mechanism involved.^{163–175}

For example, zone 2 corresponds to the nonthermal ablation with optical penetration of the material as the prevailing mechanism and zone 3 represents the thermal ablation regime for crystalline silicon with reference to a femtosecond laser.¹⁷⁵ The transition from zone 2 to zone 3 can be explained by the energy transportation processes.¹⁷⁶ The density of free electrons increases with the increase of fluence. As it reaches a critical value of $10^{18}\ \text{cm}^{-3}$, collisions between the electrons begin to dominate other relaxation processes and behave collectively as plasma. This results in slower energy transfer from electrons to lattice, and energy transfer to the bulk material is governed by thermal diffusion mechanism. When the evaporation temperature of 2828 K is exceeded, thermally induced ablation leads to increased overall ablation rate.

In the nanosecond regime, laser ablation of silicon is a thermal process with the three major mass removal mechanisms namely fluid flow, evaporation and homogeneous boiling.^{177–182} Ren *et al.* studied the dynamics of different

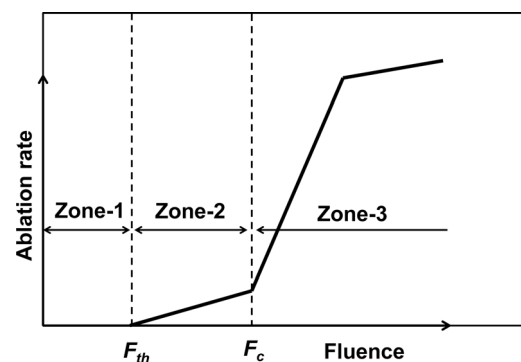


FIG. 8. Schematic illustration of ablation rate vs laser fluence (F) or intensity (I) for a given laser and a homogeneous material. Laser fluence is below F_{th} in zone 1, between F_{th} and F_c in zone 2, and above F_c in zone 3.

physical processes and ablation characteristics involved in nanosecond UV laser and silicon interaction with laser intensities ranging from 0.5 GW/cm^2 to 150 GW/cm^2 .¹⁷⁹ It was found that at low ablation intensity, silicon removal is characterized by surface evaporation and the ablation morphology is clean. At medium high ablation intensity, the increment of ablation speed with laser intensity slows down and saturates due to a strong plasma shielding effect and the quality of laser ablation generated features is degraded. At high ablation intensity, the laser ablation speed increases again beyond a certain threshold, and silicon is removed mostly in an explosive ejection format leading to the poorer quality and less controllable feature dimensions. Energy reradiated from laser heated hot plasma and plasma induced strong shock wave are found to be responsible for the acceleration in mass removal rate at high intensity.

In developing industrial ablative laser dicing technologies, the tradeoff between laser processing speed and quality has to be taken into consideration. One way is to run laser process at low pulse energy (low fluence) and high PRF to get good quality at high processing throughput. Venkatakrishnan *et al.* used a 1030 nm-wavelength femtosecond laser with an average output power of 11 W and PRF ranging from 200 kHz to 26 MHz to dice 250 μm thick (100) surface oriented silicon wafers.¹⁸³ The experimental results show that wafers in the thickness range from 75 to 130 μm can be cut through at an equivalent (single-pass) cutting speed of 40 mm/s.

Another approach that has been explored is using a line-shaped laser beam.^{175,184,185} A line-shaped laser beam allows to sufficiently use high pulse energy to realize laser ablation at low fluence regime around the transition fluence F_c (i.e. zone 2 or lower portion of zone 3 in Fig. 8). Meanwhile the improved pulse overlap allows running the process at high speed even at a relatively low PRF. As a result, a dicing process with both higher quality and throughput can be achieved.

Pulse width has significant effect on ablation rate. Typically, a femtosecond or picosecond pulse delivers a sub-micrometer ablation rate, while a nanosecond pulse can get an ablation rate of 10 μm or more per pulse. Many believe that for less than 100 μm thin wafers, the ablative laser dicing can offer competitive throughput advantages over mechanical blade dicing without catastrophic wafer breakage.^{80,175,186,187} This has led to the commercial efforts in ablative laser dicing equipment development mainly focused on thin wafer dicing.

Currently, there are three commercially available ablative laser dicing technologies namely, the “zero-overlap” dicing approach, the multibeam technology, and the water-jet guided laser technology. For cost and throughput considerations, they are all based on nanosecond lasers so far.

2. “Zero-overlap” dicing approach

The so-called “zero-overlap” dicing technique employs a galvanometer-based positioning system in combination with linear stages to spatially distribute laser pulses along a scribe line. The successive laser pulses are either contiguous or

spaced apart in a single pass, while a succeeding pass is offset along scribe line with respect to the initial pulse location of its previous pass in multiple passes of laser scribing. The purpose is to reduce the debris, heat buildup, and plume shielding to laser pulses.^{188,189} A 355 nm-wavelength nanosecond DPSS UV laser with high PRFs is used in this approach. By running at high pulse energy with zero-overlap pulse placement in multiple passes, the process can achieve an appreciable throughput.

The laser process runs at high fluence that corresponds to the middle or upper portion of zone 3 in Fig. 8, so the strategy of this dicing approach is to pursue high process throughput at a cost of severe thermal damage to separated dies leading to much lower die strength than mechanical blade dicing does. An example of the die strength comparison for 180- μm -thick blank silicon wafers diced with “zero-overlap” laser dicing and mechanical blade dicing is given in Table I.¹⁹⁰ As a part of the complete commercial solution, a conventional XeF_2 dry etch is applied after the “zero-overlap” dicing process to recover the die strength.^{188,191,192}

The technology applies mainly to ultrathin ($\leq 50 \mu\text{m}$) silicon semiconductor wafer dicing.

3. Multiple laser beam dicing technology

The multiple laser beam dicing technology is a derivative of the line-shaped beam dicing approach. The basic principle is to split the output laser beam into a plurality of laser beams, each having a lower fluence level around F_c in Fig. 8, so the processing quality is under control. As depicted in Fig. 9,¹⁹³ by aligning and scanning a group of such low fluence beams coaxially along the scribe line, the overall material removal rate is achieved to support a high dicing throughput.^{194–200} When being aligned in different ways, these multiple beams can do scribing in series as used for wafer dicing or in parallel for grooving.

Currently this technology is focused on dicing 25–50 μm wafers for silicon and III-V compound semiconductor applications typically with DPSS nanosecond pulsed lasers. The expected dicing throughput is ≥ 11 wafers per hour (WPH) for a 50 μm thick 300 mm diameter wafer on 25 μm DAF and 12 mm $\times$ 12 mm die size.¹⁹⁶ The die strength from a 50 μm thick memory wafer on a 30 μm DAF is in the range of 550–1001 MPa for front side in tension and 461–691 MPa

TABLE I. Die strength comparison for laser and mechanical blade diced wafers (Ref. 190). Reprinted from A. Boyle, D. Gillen, K. Dunne, E. F. Gomez, and R. Toftness, “Increasing Die Strength by Etching during or after Dicing,” European patent No. EP1 825 507 B1 (Sept.28, 2011). Note that dies were diced from 125 mm diameter and 180 μm thick blank silicon wafers without post-dicing treatment.

Dicing approach	Die strength, MPa					
	3PB			4PB		
	Min	Max	Average	Min	Max	Average
Blade dicing	512	1245	861	316	863	680
Dry laser dicing	100	404	223	139	234	194

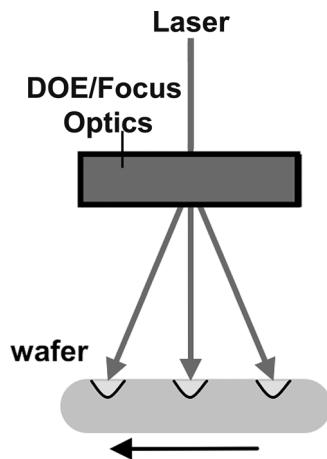


FIG. 9. Concept of the multibeam laser dicing technology. The output laser beam is split into multiple beams through diffractive optic elements (DOE) and focused onto wafer surface via a focusing device.

for backside in tension measured with 4PB flexural testing. The die strength is lower for laser diced dies than for blade diced ones if no post-dicing etch is applied.²⁰¹ The necessity of post-dicing etch treatment is explained in order to recover the strength by Evertsen and Chall¹⁹⁸ and Hendriks *et al.*¹⁹⁹

This technology can be also used for laser induced sub-surface separation,¹⁹⁹ as is introduced in the following section.

The SEM images of the top surface and side wall of a die shown in Fig. 10 will help to better understand nanosecond laser dry ablation on a device wafer with different fluences.²⁰² Low-*k* dielectric peeling on top side [Figs. 10(a)–10(c)], microcracks [Figs. 10(d) and 10(e)] and redeposition of molten material on side wall [Figs. 10(f) and 10(g)] are observed. With process optimization, these issues can be reduced but not eliminated. Post-dicing plasma etch shows improved side wall quality [Figs. 10(h) and 10(i)]. Again, improved plasma etching process will greatly recover the die side wall.

4. Water jet guided laser dicing technology

The water jet guided laser technology, also known as Laser Micro Jet (LMJ), was commercialized for precision machining in 1999.^{203–207} Over 250 technical publications on water jet guided laser for materials processing applications are available online.²⁰⁸

The concept is to couple a pulsed laser beam into a low-pressure water jet to perform precision materials machining. The laser beam is focused in a nozzle while passing through a pressurized water chamber (Fig. 11).²⁰⁹ The geometries of the chamber and nozzle are critical to energy coupling of the laser beam into the water jet and the mode of water jet guided laser beam.^{210,211} The low-pressure water jet emitted from the nozzle guides the laser beam by means of total reflection at the transition zone between water and air, in a manner similar to conventional optical fibers. The water jet can thus be described as a fluid optical waveguide of variable length.²¹² Pure DI and filtered water, pressurized at 50–600 bars depending on the nozzle diameter, is used for the water jet. The nozzles are made of sapphire or diamond with typi-

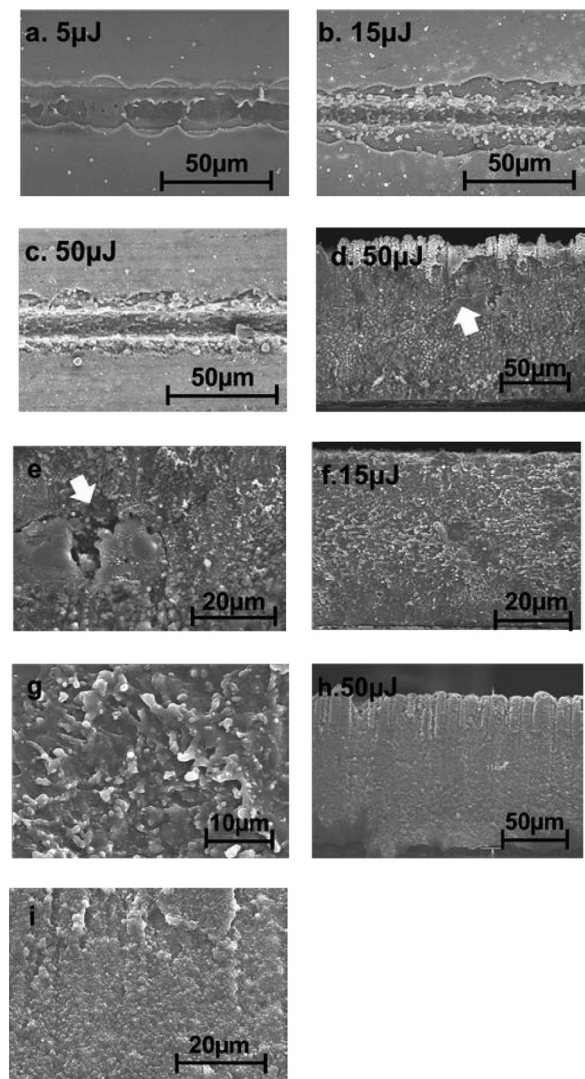


FIG. 10. SEM images for a low-*k* dielectric device wafer scribed and diced by a DPSS nanosecond UV laser (pulse width ~ 30 ns): (a)–(c) are front-side view for single-pass scribing at different pulse energies (5, 10, 50 μ J); (d)–(g) are sidewall view diced by multiple passes at different pulse energies; (h) and (i) are sidewall view after short duration of plasma etching. (a) 5 μ J, (b) 15 μ J, (c) 50 μ J, (d) cross section: 50 μ J, (e) magnified view of image (d), (f) cross section: 15 μ J, (g) magnified view of image (f), (h), cross section: 50 μ J, (i) magnified view of image (h). Reprinted with permission from W.-S. Lei, R. Yalamanchili, and A. Kumar, “Advanced Wafer Dicing,” Applied Materials Technical Report (November 2010). Courtesy of Applied Materials, Inc.

cal diameters ranging from 20 to 150 μ m. Techniques were developed for analyzing the breakup of thin high-speed water jet waveguide.^{213,214} The stable length of the water jet is about 1000 times the jet diameter. The mechanical force of the water jet onto the wafer is claimed to be less than 0.1 N.^{208,215,216} As for the laser sources, either flash-lamp pumped pulsed Nd:YAG lasers or Q-switched lasers at 1064, 532, or 355 nm can be employed. The ~ 1 μ m infrared lasers and 532 nm green lasers are usually coupled into fibers to facilitate the water jet guided laser optical head. There still lack suitable optical fibers for UV laser beam delivery, so a direct focusing scheme is needed.²¹⁷

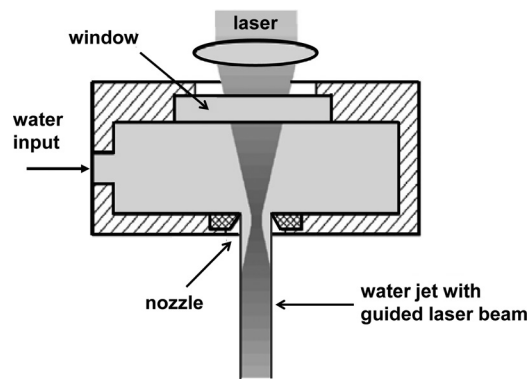


FIG. 11. Concept of water jet guided laser beam. Reprinted with permission from A. Spiegel, N. Vago, and F. R. Wagner, "High efficiency Raman scattering in micrometer-sized water jets," *Opt. Eng.* **43**, 450 (2004). Copyright 2012 Society of Photo-Optical Instrumentation Engineers (SPIE).

Laser ablation induced material removal involves two steps namely, material separation from substrate via ablation and the transport of the separated material out of the ablation site to form the desired geometrical patterns. The overall process efficiency and throughput are affected by both steps. Previously much attention has been given to the understanding and improvement of ablation step. However, if the transport process is inefficient, the laser-ablation separated molten material can either redeposit onto the sidewall to weaken the die strength or adhere onto the front surface of the work piece alongside the kerf to form debris and contamination, leading to the reduction of overall process efficiency and quality. The HAZ in the substrate adjacent to the new surfaces is also formed due to heat penetration during the laser machining process. The influence of laser pulse width on the precision and quality of 150 μm through holes in 400 μm thick bare silicon wafers formed by pulsed laser helical drilling technique was characterized by scanning and transmission electron microscopic methods.²¹⁸ For the nanosecond pulse drilled holes, the expulsion of molten material from the drilled channel is incomplete. The partial redeposition of the molten material onto the sidewall causes thermal stresses in the underlying material leading to the generation and motion of dislocations and crack formation. Therefore, reducing the sidewall redeposition and heat affected zone can be expected to improve die strength due to reduced thermal stresses and crack formation.

The continuous water jet offers much efficient thermal management in laser machining which benefits to the transport of laser-ablation separated molten material. It also helps in reduction of thermal damage by cooling down both the separated molten material and the cut immediately after each pulse. Therefore the water jet guided laser machining process can be operated at the higher fluence end of zone 3 as illustrated in Fig. 8 to pursue high processing throughput.

The remarkable debris removal capability of water jet is supported by Shimizu and Takahashi's work on applying a nanosecond 532 nm laser to ablate silicon wafer with a water microdrop.²¹⁹

Several studies reported higher die strengths from bare silicon and GaAs/Ge wafers diced by water jet guided laser

process than by mechanical blade or dry laser processes.^{220–224} For blank Si wafers, water jet guided laser dicing yielded die strength 30–50% higher than blade dicing.^{220,221,224} Schoenfelder *et al.* reported higher die strengths from 100 μm thick monocrystalline silicon wafers diced by a water jet guided continuous 1064 nm laser than by the same laser in dry dicing.²²² SEM images revealed that sample edges have molten and recrystallized material for both laser processes and these defects induce cracks and residual stresses. But the water jet guided laser was found to yield less molten material at die edge.

As discussed above, the overall laser machining process efficiency and throughput are affected by both the laser ablation step and the transport step which removes the separated molten material out of the cut. There are several limitations to the water jet-guided laser machining technology related to the laser ablation step.

To facilitate the discussion, laser absorptivity in water is given in Table II.²²⁵ More detailed information on optical absorption of water can be found in literatures.^{226,227} It can be seen that at 1030 nm, the transmission is only about 33%, and at 1064 nm, barely about 50% of the power is delivered to work surface.

Some physical limitations can impact the implementation of high power infrared and green lasers into water jet. As illustrated in Fig. 8, in order to achieve higher throughput, the straightforward way is to run the process in the higher end of zone 3, especially if the water jet can manage the process quality. Although water has very high optical transmission in the UV (355 nm) and green (532 nm) wavelength regime, the available laser power is much lower than infrared laser power and the harmonic photons cost more. The ideal scenario is to combine the less expensive high power infrared lasers with water jet. The dilemma is, on one hand as shown in Table II, the optical transmission efficiency at 1030 to 1064 nm is very low. While on the other hand, experiments have shown that the so-called "cavitation effects" at 1030 to 1064 nm limit the implementation of high power into water jet. Laser absorption creates water vapor bubbles and upon collapsing, these bubbles generate shock waves and high speed jets leading to nozzle damage. Pauchard reported damage of a 100 μm nozzle due to cavitation effects at above 350 W for a 1030 nm laser with 30 ns pulse width at 10 kHz pulse repetition rate.²²⁵ The process conditions correspond to

TABLE II. Laser absorptivity in water (Refs. 225–227). Courtesy of Swiss Photonics and Laser Network. Reprinted with permission from A. Pauchard, "High Power Applications of the Laser Microjet," Swiss Photonics and Laser Network (http://www.swisslaser.net/libraries/files/SwissLaserNet_11.09.pdf).

Laser wavelength, nm	Optical absorption coefficient, cm^{-1}	Optical transmission after 2 cm, %
355	8×10^{-5}	99.9
515	3.77×10^{-4}	99.8
532	4.45×10^{-4}	99.8
1030	0.239	33.2
1064	0.144	51.5

a fluence level of less than 446 J/cm^2 (or 15 GW/cm^2 in intensity) at the entry side of nozzle without considering optical loss through the water chamber or a fluence level of less than 149 J/cm^2 (or 5 GW/cm^2 in intensity) at the work surface considering a 33% optical transmission at exit of a 2 cm water jet.

The pronounced stimulated Raman scattering (SRS) in water jet guided laser at 510–532 nm wavelength significantly reduces the optical transmission through the water jet to the work surface and has a big impact to the adoption of costly harmonic photons.^{209,225} Spiegel *et al.* reported the unexpectedly high efficiency SRS in micrometer-sized water jets.²⁰⁹ When coupling the 532 nm green light of a 100 W frequency doubled Nd:YAG laser (pulse width 180 ns) into a thin water jet, the undirected red light (centering at 653 nm wavelength) emits from the stable portion of the jet. The intensity of the secondary red light grows as higher input (green) peak intensities are approached. The higher the peak intensity of the input beam, the lower the optical transmission due to the SRS effect as shown in Fig. 12.²⁰⁹

The laser power density limitation in the green to infrared wavelength regimes can have a larger impact on process efficiency and throughput for applications where narrower kerf (hence smaller nozzle diameter) and deep cut are demanded. This is because the applicable pulse energy has to be reduced to keep the power intensity below the limit with a smaller nozzle diameter.

The laser power density limitation also limits the adoption of shorter pulse width lasers as a shorter pulse width requires reduced pulse energy to observe the power density limitation which in turn affects material removal rate and quality.

Water jet improves the transport process of the laser-ablation separated molten material. However, it does not change the laser ablation mechanism. With a nanosecond laser, the machining process in essence is a thermal process. In the past, the water jet guided laser technology typically used very long pulsed infrared lasers such as flash lamp pumped lasers with pulse width ranging from 80 to 250 μs

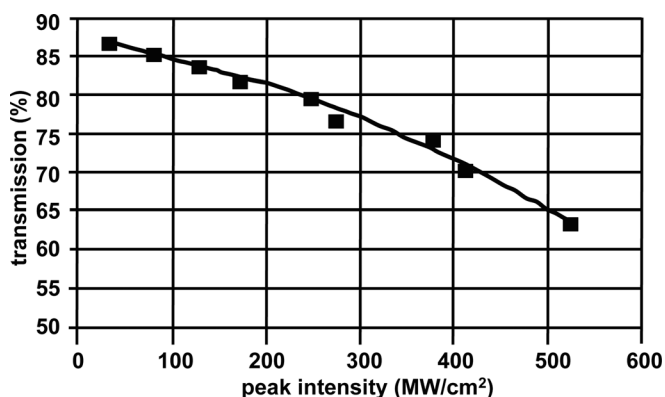


FIG. 12. Transmission of a 6-cm-long $100 \mu\text{m}$ water jet as a function of input laser peak intensity. Reprinted with permission from A. Spiegel, N. Vago, and F. R. Wagner, "High efficiency Raman scattering in micrometer-sized water jets," *Opt. Eng.* **43**, 450 (2004). Copyright 2012 Society of Photo-Optical Instrumentation Engineers (SPIE).

and DPSS lasers with pulse width ranging from 100 to 1500 ns.²¹⁶ The induced HAZ is fairly wide for a dry laser by simple calculation, but for water jet guided laser process, no detailed characterization of HAZ has been found. Semiconductor device wafers typically bear complex multiple-stack thin film layers, including dielectric layers of different dielectric constant values. Most of the dielectric layers are linearly transparent to the nanosecond lasers in the $\sim 1 \mu\text{m}$ to 350 nm wavelength regime and are hard to be ablated via nonlinear absorption mechanism at the achievable laser power intensity level. So dielectric layer removal is mainly realized by "lift-off" mechanism, with which the laser transmits through the dielectric layers and heats up and ablates the underlying metals or silicon substrate, and subsequently the dielectric layers are mechanically "lifted off."

Vittu *et al.* introduced the damage-free dicing of low- k wafers with water jet guided laser without specifying the specific laser wavelength and other parameters.²²⁸ It is reported that "The secret of chip-free dicing is, besides the LMJ (Laser Micro Jet) process, to add a copper 'grid' under the passivation layer in streets. This grid is used to provide a copper density between 20 and 80%. It is formed by squares called dummies (or tiling) of $0.9 \mu\text{m} \times 0.9 \mu\text{m}$ and a pitch space of $0.8 \mu\text{m}$. Figure 9 shows a peeling of the last passivation layer in the area where no metal grid is present. This result shows that the chipping can be completely avoided, if the area that is not used for the alignment and test pattern is filled with dummies."²²⁸ Pauchard *et al.* studied dicing of bare silicon wafers and silicon wafers with low- k layers with water jet guided UV nanosecond lasers.²¹⁷ They concluded that the UV laser process has a higher efficiency in terms of laser power utilization. For dicing $100 \mu\text{m}$ thick bare silicon wafers at 50 mm/s, only 8 W output power was required in comparison to 30 W at 532 nm and 35 W at 1070 nm. For dicing $75 \mu\text{m}$ thick low- k wafers, the UV laser cut through metal pads without cracking and chipping even on the most problematic regions of the dicing street. It is stated that "Results from previous tests with a 532 nm laser showed that grooving and cutting through low- k wafers is possible with neither cracks nor chipping in various areas of the dicing street. However, in some places, lateral cracks and chipping of the low- k layer alongside the dicing kerf could still occur, especially in dicing streets with test pads and thick glass layers (about $5 \mu\text{m}$)."²¹⁷

Figure 13 shows the front surface and side wall images of dies separated using a commercial water jet guided nanosecond IR laser dicing system.²⁰² Chipping, dielectric peeling on the front surface and heavy re-deposition of molten material can be observed. The redeposition indicates that water jet induced removal of molten material is not sufficient in this experiment.

Based on the discussions above, as the water jet guided laser technology is applied to dice semiconductor device wafers with low- k dielectric stacks, TEG patterns and thick metal layers, it is very likely that an ultraviolet nanosecond pulsed laser is demanded in order to significantly suppress the chipping and delamination issues common to mechanical dicing processes.

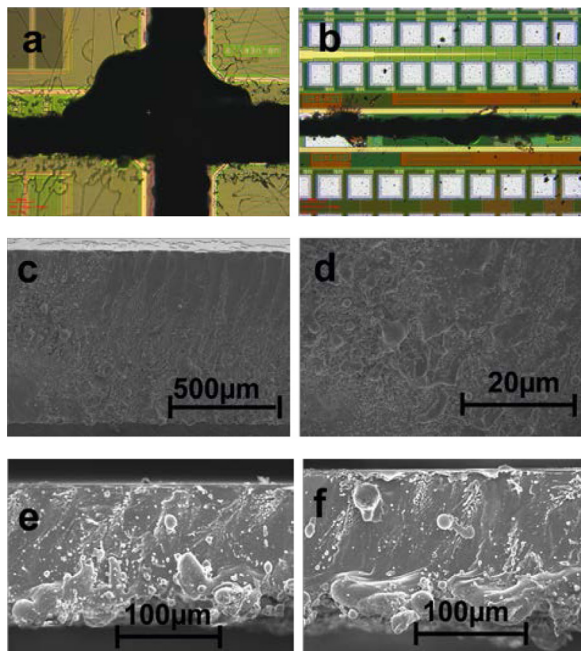


FIG. 13. (Color online) Front surface and side wall images of dies separated using a water jet guided nanosecond IR laser. (a) Top surface: 750 μm thick wafer, (b) top surface: 100 μm thick wafer, (c) side wall: 750 μm thick wafer, (d) magnified view of (c), (e) side wall: 100 μm thick wafer, (f) side wall: 100 μm thick wafer. Reprinted with permission from W.-S. Lei, R. Yalamanchili, and A. Kumar, "Advanced Wafer Dicing," Applied Materials Technical Report (November 2010). Courtesy of Applied Materials, Inc.

In addition, a water permeable dicing tape is needed to allow the water jet to pass through from the scribe line to the rear surface of the tape while the tape is not damaged by laser irradiation.²²⁹

As a further development of water jet guided laser machining process, laser chemical processing (LCP) was proposed in which a suitable liquid etchant such as KOH, instead of water, is injected radially into a small nozzle thus generating a hair-thin laminar liquid jet. A laser beam is coupled into and guided by the liquid jet via internal total reflection.^{222,230-233} Desired chemical reactions occur for gentle silicon removal as the liquid guided laser beam interacts with silicon. The LCP process is assumed to work in three steps.

- (1) Partial surface melting by laser irradiation.
- (2) Deformation and partial ejection of molten zone.
- (3) Etching of molten silicon by etchant.

So far, studies on LCP have been focused on microstructuring for solar applications (e.g., selective emitter formation) and wafering of silicon ingots. A higher die strength was reported for dies separated by LCP than by water jet guided laser dicing.²²²

5. Other relevant work

Haupt *et al.* compared die strengths of bare silicon wafers by blade saw and dry ablative laser dicing approaches.²³⁴ The lasers used covered a broad range of pulse widths including 1 μs , 20 ns, 40 ns, 56 ns, and 12 ps. It was found

that the die strengths of picosecond laser diced samples are higher than those from blade saw dicing. Among the samples made from dry ablative laser dicing, the picosecond laser yields much higher characteristic die strength than all the other nanosecond and microsecond lasers. Die strengths were evaluated from 80 μm thick bare silicon wafers diced by a high PRF (a few MHz) laser operated at femtosecond and picosecond pulse width regime.²³⁵ Higher die strength was obtained with femtosecond (214 fs) pulses than with picosecond (1.4 ps) pulses. Sidewall roughness of dies was also measured but it does not show a clear correlation with die strength.^{234,235}

Dicing with femtosecond lasers has drawn some interest as they are expected to improve the die strength and other dicing quality parameters significantly.^{183,235-237} Although femtosecond lasers yielded much higher die strength than nanosecond lasers, the processing speed still remain well below 100 mm/s even at high PRFs.

In summary, existing commercial ablative laser dicing solutions are focused on less than 100 μm thick wafers and also still based on nanosecond pulsed solid state lasers to meet the required throughput and cost targets. Furthermore UV nanosecond lasers seem to be necessary for all the three commercial laser dicing solutions. In principle, the ablative laser dicing technologies are capable of cutting through polymer passivation layers, dielectric layers, metal layers, substrate and DAF material with much less chipping than mechanical blade dicing. But they cause thermal damage leading to die strength degradation, debris and contamination as a thermal process. Other than MEMS applications which are sensitive to contamination, debris and contamination in semiconductor wafer dicing can be mitigated by adding mask layers and post dicing cleaning which are in the standard procedures already. Mai summarized some approaches for laser-induced debris removal.²³⁸ However, post-dicing die strength recovery treatment such as dry or wet etching is very likely required for thin wafer dicing and will be discussed in the following sessions below. In other words, the principal process flow as shown in Fig. 14 is needed for the ablative laser dicing approaches using a nanosecond pulsed laser.

E. Laser/mechanical blade hybrid dicing

Semiconductor device wafers typically incorporate multiple layers of metals (aluminum and copper) and fragile high performance dielectric materials such as oxides, nitrides and

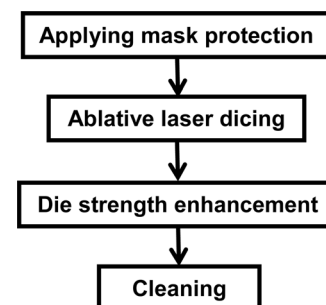


FIG. 14. Principal process flow for ablative laser dicing.

polymers. During mechanical blade dicing process, these fragile dielectric layers can easily initiate defects such as cracking, delamination, and peeling of passivation and dielectric layers, smearing or tearing of metal pads, and formation of polymer silvers, alongside the device edges. For wafers with over 100 μm in thickness, currently ablative laser dicing cannot provide competitive throughput advantage over mechanical blade dicing. As a compromise, the laser and mechanical blade hybrid dicing approach has been adopted for thick wafers with fragile passivation layers and metal stacks.

U.S. patent 6,117,347 proposed a hybrid process to dice wafers with devices made of organic thin-film multiple layers, such as thin-film sensors. A portion of the organic multiple layers is etched along a scribe line with an excimer laser to form a groove and expose a portion of the substrate before sawing the substrate along the scribe line with a saw blade.²³⁹ In the case that only mechanical blade dicing is employed, the organic layers can peel off from the substrate or the substrate can split to form a notch at the stress concentration on a weak portion of the cutting section due to the difference in coefficient of thermal expansion between the organic film layers and the substrate. This hybrid process can eliminate such defects and improve yield.

U.S. Patents 6, 420, 245 and 6, 596, 562 claimed a laser/mechanical blade hybrid dicing process in which a CO_2 laser is used to remove fragile or soft thin film layers such as low- k stacks and test/alignment patterns preceding mechanical blade dicing of silicon substrate.^{240,241}

U.S. patents 7,265,034 and 7,642,631 apply a 355 nm UV laser to scribe through low k dielectric layers followed by mechanical blade dicing for silicon semiconductor wafer singulation.^{242,243}

As schematically illustrated in Fig. 15, the laser and mechanical blade hybrid dicing process involves two steps.^{239–246} The first step is laser scribing to remove fragile materials and stops at or slightly cuts into the substrate with much less defects generated than blade sawing does; Next, mechanical blade cuts at the center of the dicing street through the remaining wafer thickness. Today, second to mechanical blade dicing, it has become another widely adopted silicon semiconductor wafer dicing technology in volume production.

Different options have been adopted for laser scribing step. Some typical ones are illustrated in Figs. 15(a)–15(c). In Fig. 15(a), two laser scribes are placed on either side of the dicing street. In Fig. 15(b), several laser scribes are placed next each other with certain overlap using same laser processing parameters so that the following blade is ensured to essentially only cut through the substrate. The multiple laser scribes can have different kerf widths and depths by adjusting laser processing parameters to achieve the optimal result for specific applications, as shown in Fig. 15(c). Laser scribing in the nanosecond pulse width regime can only reduce rather than eliminate the defects associated with fragile thin film layers. The adoption of a specific laser scribe pattern needs to be justified by the severity of the consequent thermal damage and the processing throughput in a specific application.

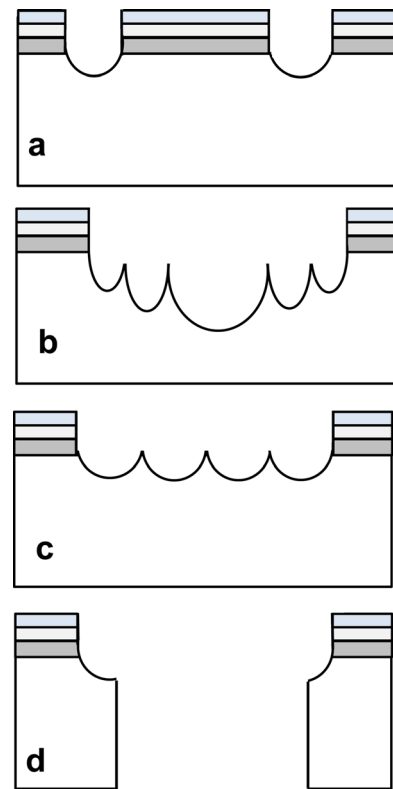


FIG. 15. (Color online) Schematic illustration of laser and mechanical blade hybrid dicing process: (a), (b), and (c) are different options for laser scribe step, (d) is the mechanical blade dicing step post laser scribing.

A hybrid wafer dicing approach was developed by combining the water jet-guided laser with a standard industrial diamond blade saw.^{247,248} The water jet-guided laser is used to remove delicate materials and layers such as low- k materials, III-V compound semiconductors, metals or oxide layers. It is also used to reduce material damage (e.g., HAZ), burrs, contamination, and chipping, etc. A blade-saw has the competitive speed advantage for cutting through bulk silicon over a water jet-guided laser. It was claimed that this combination can be much flexible to run at five different modes as follows.

- (1) Water jet-guided laser scribing followed by blade dicing: This is appropriate for wafers where the top surface consists of metal or oxide layers followed by bulk silicon. The water jet-guided laser will first cut an opening through the delicate top layers, which can then be followed by the blade dicing.
- (2) Blade dicing followed by water jet-guided laser scribing: This is used for wafers where a high quality back surface with no chipping is required.
- (3) Water jet-guided laser scribing followed by blade dicing and water jet-guided laser scribing: This is used for the case when both the top and back surfaces are required to have the highest quality and be chip and burr free. Time-consuming alignment involved for this mode can be expected.
- (4) Water jet-guided laser dicing only.
- (5) Blade dicing only.

For mainstream volume production, only the options (1) and (2) are of practical interest.

In summary, the hybrid process is a compromise between dicing quality and throughput. As a two-step process, the overall throughput is not satisfactory. Moreover, backside chipping associated with mechanical blade dicing can be still a problem.

F. Laser induced subsurface separation

When a pulsed laser radiation is tightly focused inside a transparent material, high optical intensities can be established in the vicinity of focus without damaging material surface, leading to dramatic increase in laser absorption. This in turn can cause material deterioration, thermal stress, and microcracks. This mechanism has been widely used in laser subsurface machining of transparent materials. One example is the internal marking and engraving of glasses, where nanosecond pulsed lasers at $1\ \mu\text{m}$ or $532\ \text{nm}$ are used.²⁴⁹ Another example is to apply subsurface laser scribing of sapphire substrate to roughen the substrate sidewall, which reduces the total internal reflection from light striking the sapphire/air interface, and increases the side light extraction intensity and output power of GaN-based LEDs.²⁵⁰ Most recently, the idea of laser wafering has been proposed which aims to produce silicon wafers from an ingot by focusing a pulsed laser into a silicon brick to introduce a damaged plane, from which the entire wafer can be cleaved from the brick.²⁵¹

In wafer dicing domain, the so-called “stealth dicing” technology has been commercialized as a laser induced subsurface separation approach.^{8,252–266} It consists of two steps: (1) Laser induced subsurface local degradation of substrate as a cleaving initiator with the front and back side surfaces remaining intact (Fig. 16). (2) Die separation under radial tensile stresses via tape expansion.

Ohmura *et al.* studied the mechanism of a nanosecond near-infrared laser induced subsurface degradation in silicon wafers.^{267,268} The mechanism of the subsurface laser processing in silicon for “stealth dicing” was described as follows. When a near infrared pulsed laser of $1\ \mu\text{s}$ or less pulse width is tightly focused inside a silicon wafer, it can reach the peak power intensity of more than $100\ \text{MW}/\text{cm}^2$ at the focal spot. Laser absorption occurs instantly in the vicinity of the focal spot and a localized temperature field of higher than $1000\ \text{K}$ in a confined volume of $10\ \mu\text{m}^3$ is established

within nanoseconds, due to the temperature dependence of absorption coefficient.^{255,267,268}

Voids and a high density dislocation layer are formed at the heating phase due to the highly constrained melting and vaporization. A thermal shock wave also propagates towards wafer front and back surfaces but is strongly compressed. During the cooling phase, partial recrystallization of silicon and microcracking occur in the vicinity of the focal spot (Fig. 17).^{267,269}

After the laser treatment, the wafer is mounted on a dicing tape. Expanding the tape peripherally exerts a tensile stress radially to the subsurface damaged area which in turn drives the internal cracks propagate towards both surfaces and finally separates the wafer into individual dies.

“Stealth dicing” is a completely dry and debris free process with no post-dicing cleaning needed, which makes it particularly attractive to separation of sensitive MEMS devices.^{270–272}

Dicing of wafers with DAF and low- k dielectrics was reported.²⁵² DAF is mounted onto a wafer after the laser induced subsurface treatment. During tape expansion, DAF is expected to be separated together with the dies. In the case of low- k wafers, laser irradiation is introduced from the back side of wafer. When tape is expanded, the low- k dielectric stacks are separated together with the dies. However, in the real applications, dicing of wafers with DAF and low- k dielectrics can be more challenging.

Several limitations to the “stealth dicing” technology have been noticed and presented below.^{270–272}

- (1) Doping level of substrate: Highly doped wafers induce too much absorption thickness-wise before laser beam reaches its focal plane, leading to insufficient local degradation at focal position and therefore the separation ability is lower.^{269,272} The doping level affects the resistivity of a wafer. Kumagai *et al.* correlated the absorption coefficient (μ) of silicon wafers with their resistivity (ρ) empirically and found that for easy separation of dies in the “stealth dicing” approach, the resistivity needs to be more than $0.01\ \Omega\text{cm}$.²⁶⁹

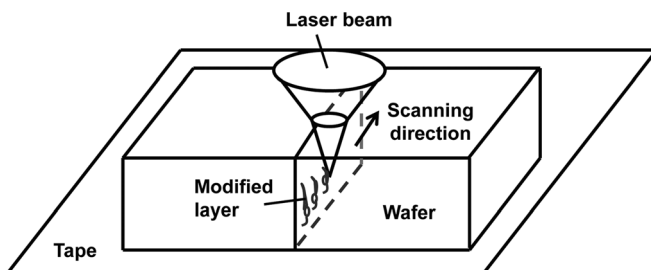


FIG. 16. Concept of “stealth dicing.” A modified layer is formed inside the wafer close to laser focus.

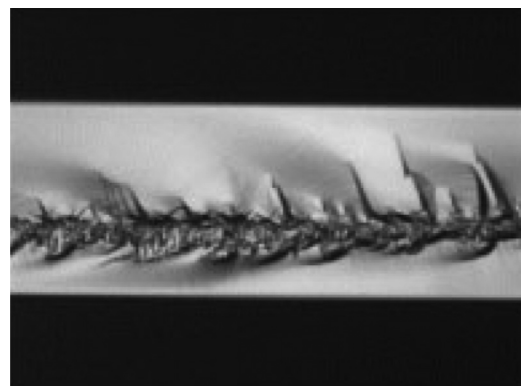


FIG. 17. Divided surface of silicon wafer showing laser induced subsurface modified layer by stealth dicing. Reprinted, with permission, from M. Kumagai, T. Sakamoto, and E. Ohmura, “Laser processing of doped silicon wafer by the stealth dicing,” Proc. Int. Symp. Semicond. Manuf. (ISSM), PT-O-086 (2007). Copyright 2012 IEEE.

- (2) Exclusion zone: The “stealth dicing” approach employs a focusing lens with a high numerical aperture to achieve sufficient laser intensity in the subsurface focal plane while avoiding any damage to the wafer surface. An exclusion zone having a width of 40% or more of the wafer thickness is needed.²⁷² This means that the dicing street width has to be 40% or more of the wafer thickness. In addition, the exclusion zone has to be free of metal, void, and polymer, etc.
- (3) Presence of opaque materials in the dicing street: The opaque materials such as metals block the laser radiation so the internal focusing is hindered.^{270,271} When the opaque layer is thick enough, even if internal laser processing is feasible, the separation step can still fail. Although suggestions are made to introduce laser beam from wafer back side, it is not always viable due to backside metallization in some cases. There were some efforts to design the metal stack patterns in a way that favors “stealth dicing.”^{273,274}
- (4) Presence of multiple different materials: Current semiconductor wafers include multiple layers of different materials. According to fracture mechanics, as a crack propagates perpendicularly towards the multiple layered stacks, it can deviate from its initial propagation direction.^{268,272}

For thick wafers, the laser processing speed keeps the same but multiple passes of laser processing are needed at different depth inside the wafer to create sufficiently large damage plane for the ease of subsequent separation. Multiple laser beams were proposed for single-pass subsurface laser processing to achieve high throughput.²⁷⁵ As wafer thickness increases, the throughput decreases dramatically. For very thin wafers such as below 30 μm , precise control of the focused laser beam inside the very thin wafer becomes challenging.²⁷⁶

The HAZ in which temperature reaches over 200 °C is about 7 μm inwards from side wall according the numerical simulation by Ohmura *et al.*^{267,268} Very limited die strength data have been found for “stealth dicing” approach. The consistency of die strength data for wafers with either the front side or the back side in tension was found to be lacking for “stealth dicing” compared to blade dicing, since the distance from the internal degradation layer to the wafer surface affects the die strength.²⁷⁶

Also, the sensitivity to wafer crystal orientation, i.e., the crystallographic anisotropy of silicon as discussed in the earlier section on scribe and break, is a concern that needs to be addressed.²⁷⁷

G. Cleavage separation by laser induced thermal stresses

Laser radiation generates thermally induced stresses in an inherently brittle material such as glass and silicon. The thermally induced stresses can lead to crack formation or cause propagation of an incipient crack at temperatures below the melting or softening temperature of the substrate. This mechanism has been adopted for cleavage separation of blank brittle materials, mostly glass sheets, by using continuous wave laser. Continuous wave CO₂ lasers emitting at $\sim 10.6 \mu\text{m}$ wavelength have been widely used from the very

beginning.^{278–280} Later on, the continuous wave solid-state lasers emitting at near-infrared ($\sim 1 \mu\text{m}$) wavelength have been adopted,^{281,282} for the so-called “thermal laser separation (TLS)” dicing technology.^{283–285} Recent efforts have attempted to transfer this technology to semiconductor wafer dicing where the continuous wave near-infrared lasers become necessary for bulk volume optical absorption in the substrates (e.g., silicon, GaAs or sapphire).^{283–287}

In principle, cleavage separation by laser induced thermal stresses includes two phases: a “seed” crack formation and controlled propagation of the “seed” crack under laser radiation.

The “seed” crack functions as a well-defined starting point for cleavage separation. It can be made by diamond tool tip scribing,^{283–285} pulsed laser scribing,^{283–285} or continuous wave laser heating.^{233,285}

The “seed” crack propagation in a silicon wafer is guided by radiating a continuous wave near-infrared laser beam along a desired path. At the $\sim 1 \mu\text{m}$ near-infrared wavelength, which is close to the indirect bandgap of silicon at room temperature ($E_g = 1.12 \text{ eV}$ or $\lambda = 1.107 \mu\text{m}$), the corresponding optical absorption depth is a few hundred micrometers. But due to the temperature dependence of absorption coefficient, a nonlinear bulk volume heating of silicon takes effect. The heated material expands and leads to the formation of compressive stresses both radially and tangentially within the laser radiation heated zone. Tangential tensile stresses are formed around the heated zone. Both of these are responsible for crack generation and propagation.²⁸⁵ In order to achieve a high energy input at high speed while narrowing the heating zone transverse to the dicing direction, the laser beam can be focused into an elliptical shape (or a line-shaped beam) with its longitudinal major axis along the dicing direction.^{278,283} A wet or dry cooling source is usually applied subsequent to laser radiation to enhance the stress difference for better control of crack propagation direction.^{278,283–285}

Haupt *et al.* introduced a method that relies on continuous wave near-infrared laser radiation for both “seed” crack generation and subsequent guided “seed” crack propagation to realize silicon wafer dicing without utilization of cooling source.^{234,286} This significantly simplifies the cleavage separation process. However, in these studies, laser focal spot sizes in the range of a few hundred micrometers, which are far more than the typical dicing street widths in semiconductor wafers, have been used to achieve the required stress profiles for crack generation and propagation.

Cleavage separation of blank silicon wafers via laser induced thermal stresses can yield much higher die fracture strengths ($\geq 3500 \text{ MPa}$) than any mechanical blade dicing and other laser based dicing technologies.^{234,283–286} However, a lot of hurdles have to be tackled before it can be considered for dicing more complicated semiconductor device wafers which bear multiple stacked sensitive layers of different materials. Below are some fundamental issues and concerns.

- (1) Presence of opaque materials such as metals in the dicing street: Opaque materials block laser radiation from

being effectively absorbed in the substrate, leading to inconsistent thermal stress field.

- (2) Presence of multiple different materials: With the existence of multiple different materials, such as polymeric passivation layers, low- k dielectric materials and metal layers, preparing the “seed” crack on the device side can be very challenging in terms of scribing process quality. The “seed” crack is preferred to be a median crack while radial and lateral cracks, which are responsible for chipping and delamination, are unwanted. Even if the laser radiation can be introduced from the backside, due to the through-thickness bulk volume absorption and heating mechanism inherent to this technology, the impact of transmitted laser photons to the sensitive device layers is yet to be known. For example, optical absorption at the silicon substrate/device layer interface may cause mechanical or structural defects. Furthermore, as the “seed” crack propagates normal to the substrate/device layer interface, crack deviation as observed in the case of “stealth dicing” can also happen.^{270,272}
- (3) Limitation to the dicing street width, die size and wafer thickness: This approach relies on volume heating effect, so the volume of heating zone and the mechanical constraint dictated by wafer thickness, laser focal spot size and die size have to be sufficiently large in order to establish required stress amplitude for guided crack propagation. Laser focal spot size sets the requirement to the widths of exclusion zone and dicing street. Understanding these limitations is particularly important when it comes

to thin wafers with small-sized dies and narrow kerf widths.

- (4) Sensitivity to wafer crystal orientation: Fig. 18 shows an example of the effect of crystal orientation on side wall appearance of dies, which are singulated by cleaving a $\langle 100 \rangle$ and $\langle 111 \rangle$ wafer in different angles to the flat under laser induced thermal stresses.^{286,287}

H. Plasma dicing

In the “dicing before thinning” approach, Landesberger *et al.* proposed to generate precut with plasma etching or the combination of blade sawing and plasma etching, where blade sawing is to remove metal patterns.^{146–148}

U.S. patent 6,642,127 proposed to use plasma etching for full-thickness-wafer dicing. A patterned mask covers the circuits and exposes dicing streets on a wafer. The wafer is mounted on a carrier and transferred into an etch reactor for plasma etching to separate dies.⁹

Arita *et al.* proposed to dice a wafer by applying plasma etching to the back side of the wafer. The principal process flow is given in Fig. 19, which includes expensive mask patterning by photolithography.^{288,289}

U.S. patent 7,906,410 proposed another process flow for plasma dicing, which applies laser scribing to remove TEGs, plasma etching from front side of the wafer to dice through both wafer substrate and DAF, while the expensive photolithography is eliminated. The principal process flow is described in Fig. 20.²⁹⁰

Key technical hurdles on high aspect ratio deep plasma etch of silicon have been explored and resolved in recent

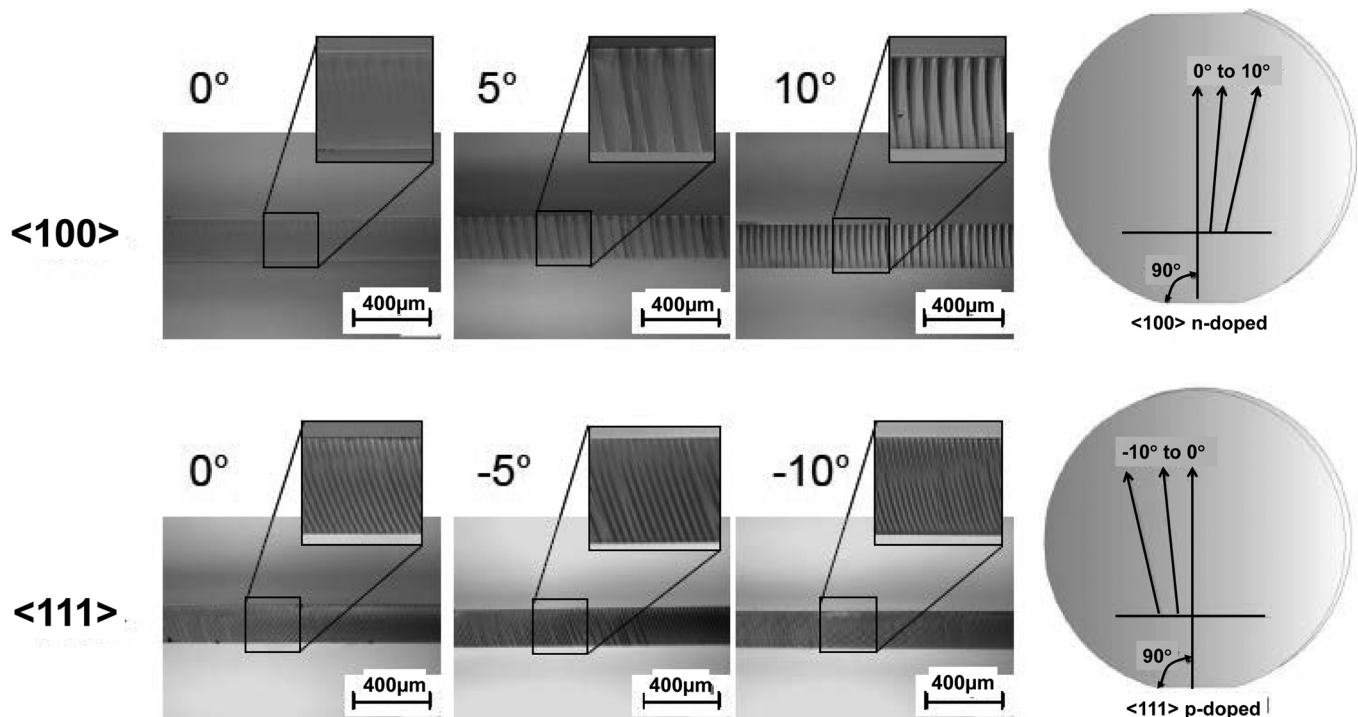


FIG. 18. Side wall appearance of dies from cleaving a $\langle 100 \rangle$ and $\langle 111 \rangle$ wafer in different angles to the flat. The side wall roughness varies with cleaving direction. Reprinted with permission from O. Haupt, V. Schuetz, A. Schoonderbeek, L. Richter, and R. Kling, “High quality laser cleaving process for mono- and polycrystalline silicon,” *Proc. SPIE* 7202, 72020 G-1 (2009). Copyright 2012 Society of Photo-Optical Instrumentation Engineers (SPIE).

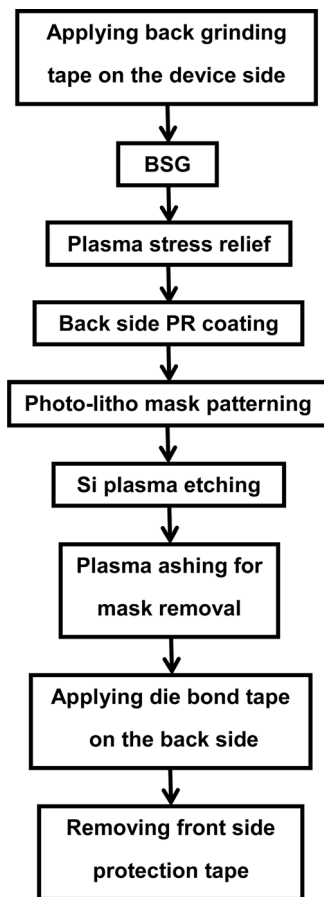


FIG. 19. Principal process flow of plasma dicing: option 1.

years as reviewed by Wu *et al.*²⁹¹ This paves the foundation for plasma dicing technology development. Examples of high aspect ratio deep silicon etch are given in Fig. 21.^{202,292}

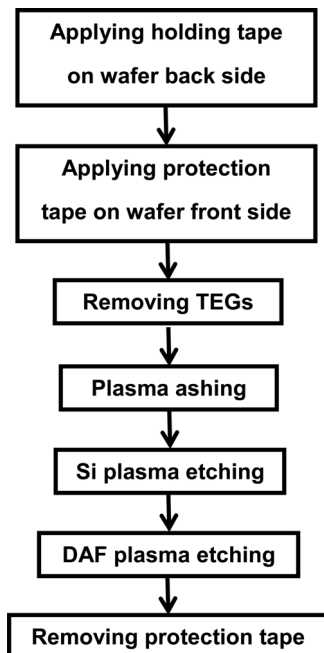


FIG. 20. Principal process flow of plasma dicing: option 2.

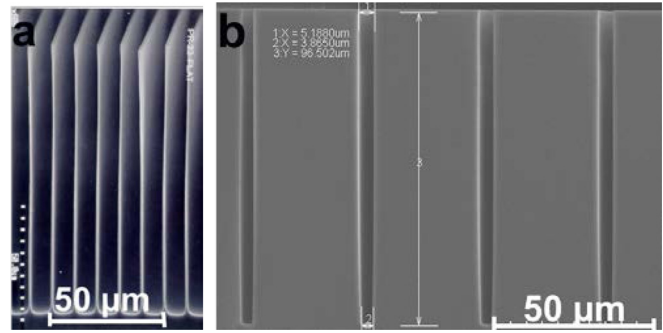


FIG. 21. (Color online) Examples of high aspect ratio trench etch in Si. Reprinted with permission from A. Kumar, “Wafer Dicing for Advanced Packaging,” Applied Materials Technical Report (Jun.2007). Courtesy of Applied Materials, Inc.

In principle, plasma dicing is a damage and stress free process. Therefore, exceptionally high die strength can be achieved. Arita reported average die strength of more than 3000 MPa with only less than 10% of 200 dies having die strength below 1000 MPa with plasma dicing, whereas the maximum die strength using mechanical blade dicing is less than 1000 MPa in all 200 measurements.²⁸⁸

Plasma dicing is an in-parallel process so its productivity is insensitive to the chip size, while all the other dicing processes are in-series processes and their productivity heavily depends on the chip size. Plasma dicing also enables free-shape die formation and separation (e.g., circular dies and hexagonal dies). Therefore, “multiproject wafers” that bear chips of different sizes and shapes on one wafer design can be easily diced. Plasma dicing is also capable of delivering much narrower dicing kerf width than all the other dicing approaches that rely on material removal to form dicing trenches.

These unique advantages combined with the gained know-hows in high aspect ratio Si etch make plasma dicing technology very attractive. The key is how to develop it into a cost-effective industrial solution.

V. POST-DICING DIE STRENGTH ENHANCEMENT

Die strength enhancement (DSE) effort dates back to mechanical grinding for wafer thinning, for which BSG is realized via a two-step process including coarse grinding (at a removal rate of $\sim 5 \mu\text{m/s}$) and fine grinding (at a removal rate of $\sim 1 \mu\text{m/s}$). Mechanical grinding causes damage to the ground surface by introducing visible and invisible defects as well as residual stresses depth wise. Takyu *et al.* showed that the die strength increases noticeably with the decrease of surface roughness, saw mark angle and saw mark depth on the back side of the wafer.⁹⁴ The so-called “mirror finishing” or “stress relief” process is introduced after BSG process to recover the die strength by removing micro-cracks and dislocations. Typical mirror finishing approaches are wet etching, dry polishing, plasma etching, and CMP.^{94,106,160,161,293–296} BOR flexural test was conducted on $15 \text{ mm} \times 15 \text{ mm}$ dies to study the effect of post-grinding plasma etching on die strength, in which wafer dicing was

done after plasma etching treatment.²⁹⁶ The result showed that a minimal Si etch removal amount of 0.5 μm from the damaged layer on the back side increased die strength by more than two times compared to the grinding-only condition. The die strength was increased by ten times after removing 3–4 μm of the damaged layer. Moreover, the effect of plasma etch on DSE was significant for dies with nominal thickness in the range of 50 to 188 μm .

Similar to mechanical grinding, mechanical dicing and laser-dicing cause damage to the side wall of a die. Consequently, die strength is remarkably decreased. According to Eq. (3), at a given die strength a thinner die corresponds to a lower threshold loading force for fracture. Therefore, the die strength degradation becomes particularly critical for thin dies, in that thin dies fail when they are unable to withstand the applied loading in the assembly processes. The thick dies with the same die strength survive the mechanical forces in die pickup process and the package reliability tests. In view of this, post-dicing DSE, also known as chip side healing, has been investigated as a valuable approach to stress relief and defect elimination.^{81,93,94,190,191,199,201,297–299}

A. DSE via wet etching

U.S. patent 7,682,937 applies wet chemical etching to remove recast layer and HAZ on laser separated dies to improve mechanical strength of dies.¹⁹⁸ Wet-etching experiment of laser singulated dies was conducted by Li *et al.* in the KOH aqueous solution (concentration: 20 wt.%) at 80°C for different etching time.⁹³ Afterwards, dies were rinsed three times by DI water and then dried by nitrogen gas. SEM examination found that the wet etching process can effectively remove the voids and the re-solidified silicon layer and thus smoothen the side walls of dies. Die strength also dramatically increases with etching time until it saturates as a result of complete defect removal. Also, the difference of front side and back side die strength may indicate that the level of laser induced side wall damage varies depth wise.

Wet etching has been used for cleaning the die edge recast on blade or laser diced RFIC compound semiconductor substrates such as GaAs. Abshire *et al.* found that this etch cleaning also makes an improvement to die edge strength on laser diced GaAs dies.²⁰¹ Wafer expanding is a process step between dicing and die pickup operation, which expands the space between the singulated dies by omnidirectionally stretching the dicing tape on which wafer is mounted. Due to the narrow kerf, stretching the wafers prior to the etch clean is critical to the effectiveness of die strength improvement and die cleaning as it allows more room for the solvent to get in between dies.

B. DSE via nonplasma based dry etching

Nonplasma based dry etching utilizes fluorine-containing gases for isotropic etching of Si. Due to its very high selectivity of silicon to photo-resist, silicon dioxide, silicon nitride and aluminum, and low cost, XeF_2 has been used as the etchant for post-dicing dry etching.^{93,190,191} The chemical reaction governing silicon removal is



The XeF_2 based dry etch improves the strength of laser separated dies with moderate to low effectiveness due to the low silicon etch rate (about 1–2 $\mu\text{m}/\text{min}$).^{83,93,191} Figure 22 shows the effect of XeF_2 dry etch on strength enhancement of dies separated by mechanical dicing and “zero-overlap” nanosecond UV laser dicing.¹⁹⁰

C. DSE via plasma etch

Plasma etching in principle is also based on the chemical reaction in Eq. (4) for silicon removal, where typically SF_6 is used as etchant.

Kroeninger and Mariani reported the effect of plasma etching on DSE.⁸¹ Dies of 125 μm thick were singulated via DBG process flow, whereas the precut was generated by mechanical dicing. The 4PB method was used to determine die strength for the cases of DBG only and “DBG+plasma etching,” respectively. The result showed that the plasma etching process removed 3 μm Si layer from ground side of the die and almost doubled the die strength.

The DBG process was used for wafer dicing, in which the precut was made also by mechanical dicing.⁹⁴ After DBG, the wafer went through either CMP only or CMP and reactive ion etching (RIE). RIE contributed to DSE by increasing the average die strength from 253 MPa in the case of “DBG+CMP” to 1312 MPa in the case of “DBG+CMP+RIE.”

However, it is hard to ascertain whether the major contribution to DSE comes from back side recovery or from side wall healing when dies were prepared by DBG.^{81,94}

Li *et al.* used plasma etching to remove defects from side walls of dies separated by laser ablation.⁹³ SEM analysis to the side wall showed that a large amount of re-solidified silicon formed during laser ablation was removed by plasma etching, but the side wall roughness is still high. TEM analysis further confirmed that plasma etching can remove the laser induced HAZ which contains many voids, air bubbles, second-phase particles and micro-cracks. As a result, DSE was realized by plasma etching.

Heinze *et al.* reported the result of die side healing via post-dicing plasma etching for 75 μm thick dies.²⁹⁸ A 3PB

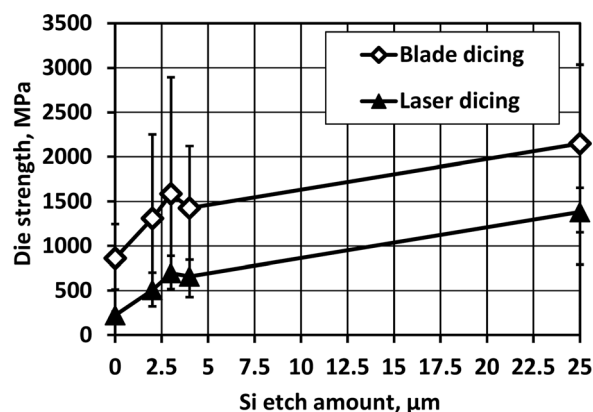


FIG. 22. Die strength comparison for the “zero-overlap” laser dicing and mechanical blade dicing. 125-mm-diameter and 180- μm -thick blank silicon wafers were used. Data were from Ref. 190.

flexural test was used to determine the back-side die strength for blade diced, laser diced, and laser diced plus plasma etched dies. Significant DSE on laser diced samples was achieved through plasma etching. The results clearly show that the quality of the side walls is a determining factor to die strength.

There are some challenges to implement plasma etching process for die side healing. Li *et al.* used RF power initiated plasma in CF_4 and O_2 gases to remove side wall defects. It was found that the front surface bearing active circuitry was damaged due to physical bombardment involved in the plasma etch process.¹⁰² Spitzer pointed out the necessity to avoid melting or degradation of adhesive tapes by the plasma etching process for post-grinding stress relief.²⁹⁶ The remote plasma technique, for which the plasma is generated outside the reaction chamber away from the wafer, was introduced to reduce the heat load on the adhesive tapes by keeping the wafer temperature below 80°C . Moreover, only neutral fluorine radicals are carried by a directed stream of argon to the work surface, providing soft surface etching without potential damage due to ion bombardment.

VI. SUMMARY

Semiconductor wafer dicing is facing tough challenges with the adoption of copper/low- k dielectric interconnect structures, thin and ultra-thin wafers, die attach films as a necessary structural material in thin device packages, narrow dicing streets, and complex structures on the dicing streets. Particularly, die strength turns to be a key quality index for thin ($\leq 100\ \mu\text{m}$) and ultrathin ($\leq 50\ \mu\text{m}$) dies. Severe dicing defects can cause die-level interconnection failures and/or structural integrity failures including die cracking and fracture.

For silicon semiconductor wafers with regular thicknesses ($\geq 100\ \mu\text{m}$, preferably $\geq 150\ \mu\text{m}$), mechanical blade dicing has been adopted for the mainstream manufacturing process. As a valuable extension of mechanical dicing technology, the laser and mechanical blade hybrid dicing approach has been adopted for regular-thickness wafers with fragile passivation layers and metal stacks. Laser scribing removes fragile materials and slightly cuts into the substrate for reduced defects followed by mechanical blade dicing through the remaining wafer thickness.

Several innovative dicing approaches have been developed and gradually adopted in industry, with an emphasis on thin wafer ($\leq 100\ \mu\text{m}$) dicing applications to achieve competitive throughput and avoid catastrophic wafer breakage that mechanical dicing is prone to. Most of them are based on laser technologies, including ablative laser dicing and nonablative laser dicing. While stealth dicing has drawn attention in MEMS device separation as a debris-free dry process, the ablative laser dicing technologies seem to be more capable in mainstream semiconductor device singulation.

Ablative laser dicing processes employ nanosecond pulsed lasers for cost and throughput considerations but they can cause severe thermal damage to separated dies leading to lower-than-expected die strength for thin and ultra-thin

dies. Therefore post-dicing die strength enhancement treatment has emerged as a necessity, and wet etch, nonplasma based dry etch and plasma etch have been explored.

Plasma dicing as a damage and stress free process can achieve exceptionally high die strength while eliminating the post-dicing die strength enhancement treatment. The high die strength characteristics, the insensitivity of its productivity to die size and the capability of free-shape die formation, in combination with the well-established knowhow on high aspect ratio deep silicon etch, makes plasma dicing a very promising solution for next generation die singulation.

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