

Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks

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ABSTRACT

An experimental correlation showing flipchip packaged larger dies more susceptible to corner delamination is, first, established in this work. Chamfer structures have been inserted into the architecture of traditional orthogonal crackstop designs with the aim to alleviate the accumulation of strains present in the corners of larger dies. Finite element modeling (FEM) was employed to uncover the optimum chamfer structure size that minimizes both the chamfer space usage as well as chip package interaction (CPI) related risks. Die size was shown to have quantifiable impact on the corner strain. The effect of die size was shown to be enhanced with lower underfill modulus. The effect of changing the crackstop corner chamfer structure size on both corner strain and strain energy release rate was studied. While varying the crackstop corner chamfer structure size had minimal effect on strain, it did have a significant effect on the strain energy release rate. It was observed that chamfer structure significantly reduces the strain energy release rate at the edge of the die near the corner. It has been determined that the optimum location for the support structure triangle vertex is to be situated at the point where the peeling strain switches from compressive to tensile at the corner square. The effectiveness of corner chamfer support structures in reducing CPI risk at the optical attach cavity used for lateral optical fiber attach was evaluated. The simulations have determined that inclusion of crackstop corner support structures at the newly created internal cavity corners of the die result in a reduction of the average corner strain by 33% at the external corner and 21% at the internal corner of the optical cavity.

Keywords—crackstop, die seal, seal ring, edge seal, CPI, reliability, 3D FEM model, chamfer structure, die size, underfill modulus, J integral

INTRODUCTION

Server applications and high performance computing require large die sizes to execute their diverse array of extensive functions. Flipchip packaging offers a variety of advantages including reduced signal inductance, higher signal density, and reduced package footprint over

traditional packaging methods. The likelihood of initial edge defects in the back end of the line (BEoL) stack sandwiched between the die and the laminate increase with die size [1] imposing a higher CPI risk on larger dies. This correlation between die size and edge defects is confirmed by experimental results detailed in the next section.

A crackstop is built on the periphery of the BEoL stack to protect the BEoL stack from crack propagation resulting in mechanical failure. A crackstop is a pure mechanical multilevel metallic wall that surrounds the periphery of chips and has no electrical function. It is a physical barrier structure that extends through the entire stack layer of an integrated circuit (IC) chip; from the front end of line (FEoL) to the far back end of line (FBEoL) of the respective stacks of each chip. The crackstop has two primary functions; first, it stops and blocks any impinging cracks that originate during the processes of dicing, packaging and assembly of the IC chip. These cracks propagate between these layers due to dynamic forces caused by dicing vibrations. The second primary function of a crackstop is to block any moisture ingress into the die prime region. The introduction of porous low K or ultra-low K (ULK) dielectric materials into the middle of the line (MOL) has inadvertently allowed a diffusion path for moisture to easily penetrate into a device. If moisture enters the active prime region, it can cause corrosion or crack formation through expansion and contraction of the dielectric material. Both scenarios result in a significant degradation of the device performance or eventual catastrophic failure of the overall device.

Several architectures of crackstops have been previously proposed [2-4] to block cracks from propagating into the weak dielectric materials. The corner of large dies, however, requires additional support structures to prevent crack propagation. A chamfer support structure has been proposed in the corner of the die as a part of the crackstop to provide additional support and prevent corner delamination [5]. In this work, finite element modeling (FEM) was employed to optimize chamfer structure size that minimizes both the chamfer space usage as well as CPI related risks. Firstly, the CPI mechanical strain developed in the corner of the die was analyzed. The simulations showed that the dominant

strain component in the corner is shear strain. This finding coincides with previous studies [6, 7]. Die size effect was shown to have quantifiable impact on the corner strain. The dependence of the die effect on underfill modulus was studied. In agreement with previous studies [1, 8], it was found that the corner failure probability increases with the underfill elasticity modulus. The FEM approach and results are discussed in the third section of this paper.

Secondly, with a clear understanding of the corner strains, the effect of changing the crackstop corner chamfer structure size on both corner strain and strain energy release rate were, then, studied. The chamfer structure side length dimension was varied. While varying the crackstop corner chamfer structure size had minimal effect on strain, it did have a significant effect on the strain energy release rate. Three locations were considered for the initial crack: a) the corner of the die, b) the edge of the die, and c) inside the crackstop corner triangle support structure. It was observed that chamfer structure significantly reduces the strain energy release rate at the edge of the die near the corner. FEM results were used to determine the optimum location for the support structure triangle vertex. Those results are discussed in the fourth section.

Finally, FEM approach has also been applied to the photonic cavity that is used for lateral optical fiber attachment as presented in the fifth section. The effectiveness of corner chamfer support structures in reducing CPI risk at this optical attach cavity was evaluated. Both the external and internal corners of the groove have higher peeling strain than anywhere else along the edge of the die. The simulations have determined that inclusion of crackstop corner support structures at the newly created internal cavity corners of the die result in a reduction of the average corner strain.

EXPERIMENTAL RESULTS FOR THE EFFECT OF DIE SIZE ON CORNER DELAMINATION

Corner delamination events are primarily due to the impact of external environmental forces such as vibration, temperature and humidity upon chip-package integration assemblies; whereby packaging assembly related stresses and strains are created and result in the formation of thermal mechanical related CPI defects such as cracking and delamination. The thermal expansion (CTE) mismatch between various materials within the BEoL of stack can also potentially induce cracking and delamination events when exacerbated by external environmental forces and energies. [1, 9] Regions that have higher stress/strain concentrations will be more susceptible to experiencing damage such as delamination or cracking. [10, 11]

Crack and delamination events that been observed experimentally and in actual products within the BEoL material stacks located at the corners of the die have been

closely associated with die size. The 90 degree corner structures create an environment where externally applied stress and strains create shear forces that have a higher concentration than anywhere else within a die. A combination of horizontal and vertical shear forces will create a diagonal shear force within the horizontal plane as shown in figure 1. These shear forces are the resultant of thermal expansion and contraction cycling of the IC package. Thusly the BEoL stack layers of the semiconductor die located at these corner regions are exposed to a higher shear force concentration that can ultimately lead to lifting, delamination and/or crack nucleation and growth. As a semiconductor die's dimension (X & Y in figure 1) increase; the distance from center of the die to the corner of the die (DCC) also increases. This increase in length from the center to corner will theoretically result in an increase in the stress/strain present at the corners. [9]

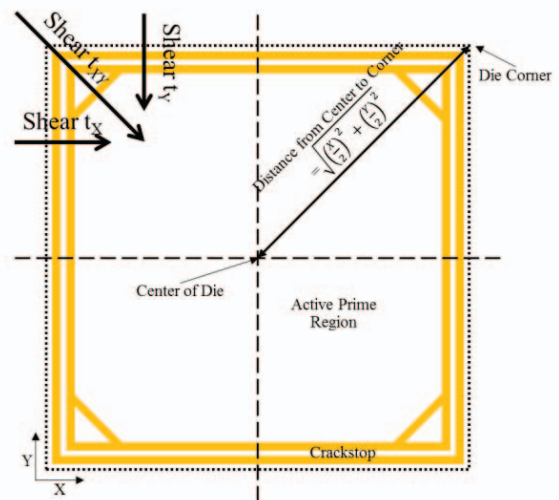


Figure 1 – A simple pictorial representation demonstrating the correlation between the size of semiconductor die and the expected magnitude of the stress and strain occurring in the corner regions.

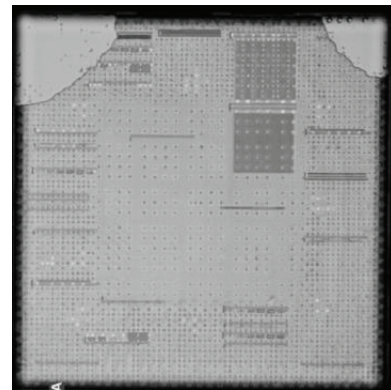


Figure 2 – Top view of a 28.4×22.9 mm² die on a 68.5×68.5 mm² laminate showing corner delamination in the top 2 corners after underfill cure at 165°C for 2 hours.

Experimentally, it has been observed that when one of the semiconductor die's edge length exceeds 12 mm on a face, the appearance of corner cracking or delamination becomes more probable. Figure 2 shows a delamination observed in a larger die. The die dimensions were $28.4 \times 22.9 \text{ mm}^2$ on a laminate of $68.5 \times 68.5 \text{ mm}^2$ surface area. Delamination was observed after underfill cure at 165°C for 2 hours. Figure 3 shows that the delamination is occurring in the corner of the die and spreading inward towards the center. Scanning electron microscopy (SEM) images showed that the separation is starting from the external edge and extending into the via layer under the lower metal level of the stack. Similar experimental conditions didn't result in any crack propagation or delamination for smaller dies especially when the die edge length was below 12 mm.

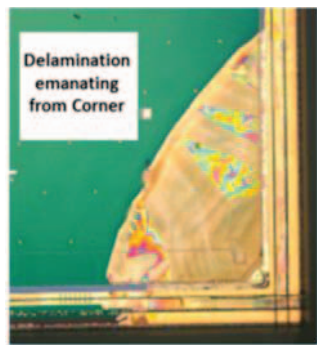


Figure 3 – An optical top down of the delamination of the lower BEoL layer originating from the corner of a large chiplet.

CORNER CPI STRAIN ANALYSIS

Corner failure is a conventional failure mechanism that has been observed in integrated circuit (IC) packages since 1985 [12]. A criterion for predicting delamination was suggested by Tay et al. in 1993 [13] since the maximum stress criterion would theoretically result in infinite stress at the corner. This criterion is based on calculating the stress intensity factors at the crack tip. The criterion takes into account the three different modes of failure: opening, shearing, and tearing modes. An alternative criterion is calculating the energy release rate which could be expressed in terms of j-integrals. J-integrals are mathematically related to stress intensity factors. Opening (mode I) and shearing (mode II) are the typical modes of failure in IC packages.

A 3D quarter FEM model for a Flipchip die on a laminate was built as shown in figure 4. The model includes the bumps connecting the die and the laminate as well as the underfill material surrounding the bumps. A 3D submodel was also built for a more detailed investigation of the corner of the die. Both models included a double rail crackstop at the edge of the die. The boundary conditions of the submodel were obtained from the global model making use of St. Venant's

principle [14]. Figure 5 shows a cross section of the submodel. All metal layers using a common dielectric material were assumed to be a single effective material in the BEoL stack. Effective mechanical material properties were calculated based on the appropriate series and parallel combinations. Stresses develop in the BEoL stack when temperature is ramped down from underfill cure temperature 165°C [1] to room temperature.

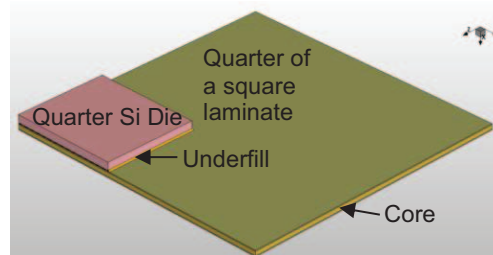


Figure 4 – Global model for a Flipchip die on a laminate.

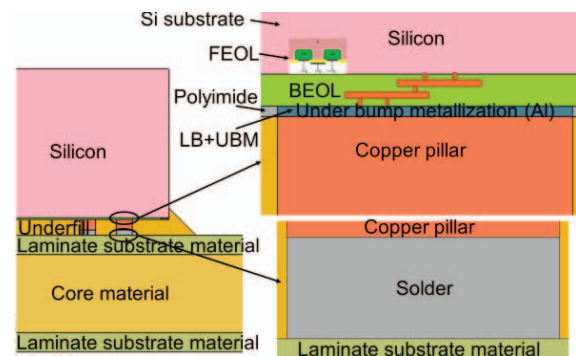


Figure 5 – Submodel cross section.

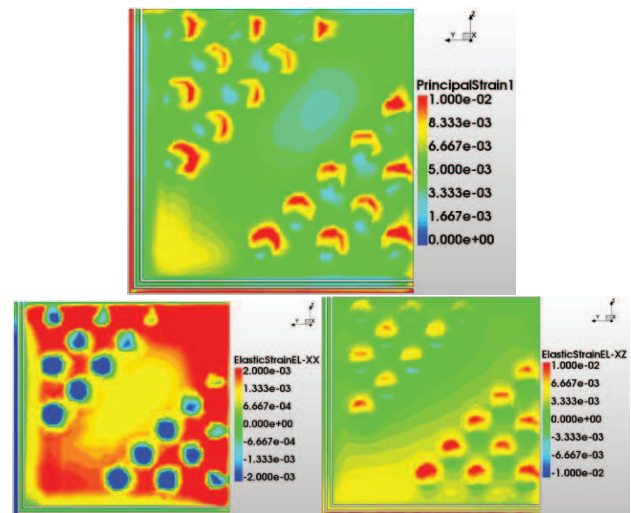


Figure 6 – Top view of Mx to Si interface in the submodel. Double rail crackstop indicates the external edges of the submodel. Top: principal strain 1 profile. Red spots have highest tensile strain. Bottom left: peeling strain profile: blue spots under the bumps have compressive strain. Bottom right: shear strain profile. Highest shear strain is in the bottom edge and under the bumps.

Principal strain 1 profile is shown in figure 6. The locations with high tensile strain are under the bumps and in the external edges as well as the corner of the die. Two main components of strain are further analyzed to understand the expected mode of failure in the corner of the die: peeling strain and shearing strain. The magnitude of peeling strain is an order of magnitude lower than shearing strain. Strain is compressive under the bump and in the edges and the corner of the die. Shear strain is highest in the edges if the die and under the bumps. The other vertical component of shear strain, not shown, is symmetric on the other edge. Those results show that the dominant strain component in the corner is shear strain coinciding with previous results suggesting that mode II is the common corner failure mode [6, 7].

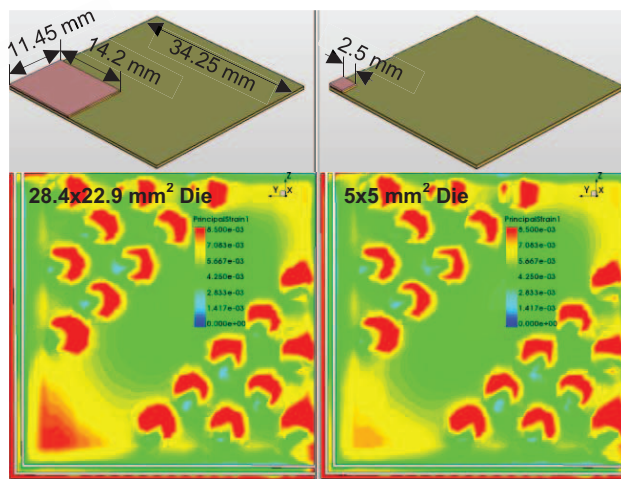


Figure 7 – Top right: quarter model for a large die (28.4x22.9 mm²) on a 68.5x68.5 mm² laminate. Top left: quarter model for a small die (5x5 mm²) on a 68.5x68.5 mm² laminate. Bottom: Principal Strain 1 profiles in a large die (left) and a small die (right) are similar with a decrease of about 10% in strain in smaller die.

Die size was varied from 5 mm edge length to 28.4 mm to evaluate the effect of the die size on the corner strain without changing the package size. Strain pattern was similar for all different die sizes, as shown in figure 7. The decrease of the die size results in a reduction in the strain in the corner inside the crackstop up to 15% in the smallest die compared to the largest die as shown in figure 8. Prior reports indicated no change in corner strain with die size. [1] The authors varied die size from 12 mm up to 20 mm side length with no effect on energy release rate in the corner. The die size effect is not significant but it was quantifiable in our simulation. The die size effect is enhanced with smaller modulus. This effect is in agreement with experimental results detailed in the previous section as well as the theoretical expectations shown in figure 1. The longer edges exposed to dicing forces results in higher initial edge defects and enhance the failure rate in larger dies. [1] The global die-laminate

CTE mismatch is the driver for the die size effect. Local forces at the corner resulting from CTE mismatch between various materials at the corner are a major contributor to the strain in that region. When the underfill modulus is higher, the local connection at the corner is strong and the die size effect is suppressed. The effect of the underfill modulus below glass temperature on the corner strain is shown in figures 9 and 10.

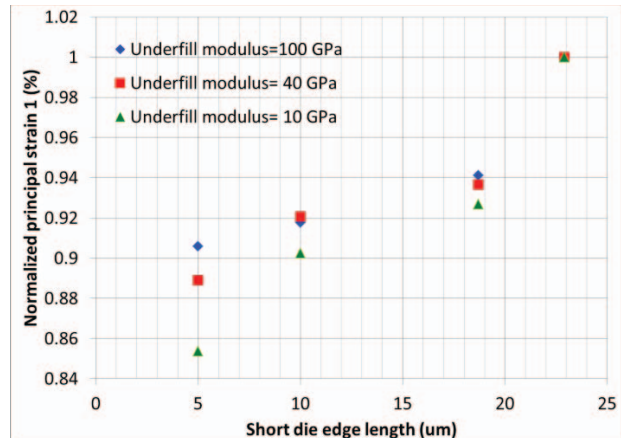


Figure 8 – Normalized principal strain 1 obtained from simulation results in the corner inside the crackstop for various underfill moduli. Strain in the large die is always normalized to 1% and the corresponding strain in smaller dies is calculated accordingly.

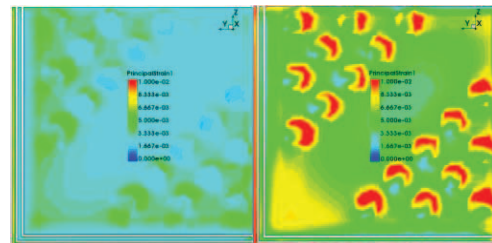


Figure 9 – Top view of the Mx to silicon interface showing principal strain 1. Left: underfill modulus is 10 GPa and right: underfill modulus is 100 GPa. Strain is significantly higher when the underfill modulus is higher.

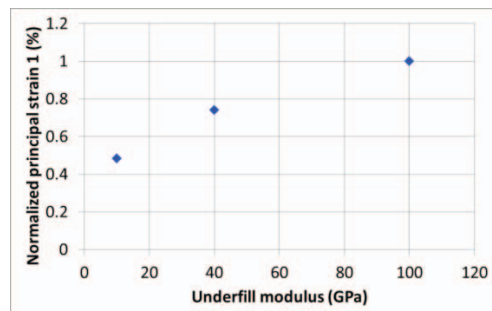


Figure 10 – Maximum principal strain 1 in the corner inside the crackstop as a function of the underfill modulus. Principal strain 1 is normalized to 1% for underfill modulus of 100 GPa.

OPTIMIZATION OF CRACKSTOP CORNER CHAMFER STRUCTURE SIZE

Traditional crackstop designs are rectangular in shape and consequently impinging crack forces and packaging stresses tend to be greater at a chip's corners than elsewhere. The correlation between the size and shape of the chips combined with inclusion of Low-K and ULK dielectric materials into chips' structure make the corners of the chips a high risk region to experience CPI activity induced stress failure. [15-17]

Liu et al. [16] considered chamfering the corner and using a chopped off design of the crackstop. This design, however, resulted in higher delamination due to the defects introduced during the dicing of the chamfered corner. An alternative design is to include additional architectural elements to supplement the crackstop design as shown below in Figure 11. [5] The aim of the inclusion of the supported corners into a crackstop's design is to deflect externally impinging crack forces and delamination as well as provide these regions with some stress relief. [16, 18] The inclusions of these features will deprive the prime region of some valuable real estate that could be used for devices or active diodes. Therefore, it is important to optimize the crackstop corner chamfer structure size.

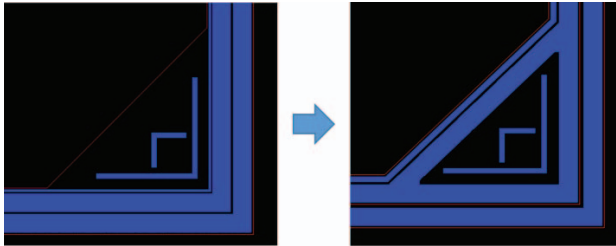


Figure 11 – The evolution of the crackstop design to address corner delamination in large chiplets. A 45 degree diagonal chamfer element has been added to the corner portions of the crackstop design to strengthen the location and reduce the impact of packaging shear stress experienced in the corner region.

A 3D finite element analysis (FEA) was set up to optimize the size of the corner chamfer element to minimize the corner CPI strain as well as the size of the chamfer element. The simulation setup is similar to the one mentioned in the previous section. The only difference is that different chamfer element sizes were considered as shown in figure 12. The change in the maximum and average principal strain caused by the variation in the chamfer element size was minimal. The lowest average strain was for the chamfer element with a side of 63 μm length resulting in about 3.5% improvement compared to the case with no chamfer element. J integral calculations were considered to compare the different sizes of the chamfer element. Three different initial crack locations were considered: at the corner, on the edge near

the corner, and inside the chamfer element triangle. The initial crack locations are shown in figure 13. The results of the j integral for both the corner and edge cracks are shown in figure 14 and the results for the inside crack are shown in figure 15. The results indicate that the edge crack has much higher probability of crack propagation compared to the corner crack. The double rail crackstop corner contributes significantly to reducing the corner strain energy density. The chamfer structure contributes to the corner strain energy density in 3 ways: a) if the crack extends to the crackstop, it decreases the probability of crack propagation significantly; b) it increases the in-plane strain inside and outside the chamfer structure; and c) if the chamfer structure is large enough it creates a pocket of strain in the chamfer structure triangle losing its effectiveness. The smaller chamfer structure increases in-plane strain as can be seen in figure 15 for the 16 μm side chamfer structure and the large chamfer structure increases the strain pocket losing the effectiveness of the chamfer structure as can be seen for the case of the corner crack for 125 μm side length chamfer structure in figure 14. All the side length chamfer structures don't reduce the probability of edge crack propagation with the exception of the larger chamfer structures: 63 μm and 125 μm side lengths as can be seen in figure 14. The optimum chamfer structure side length is such that the vertex of the chamfer triangle lies at the point where the peeling strain switches from compressive to tensile as shown in figure 16.

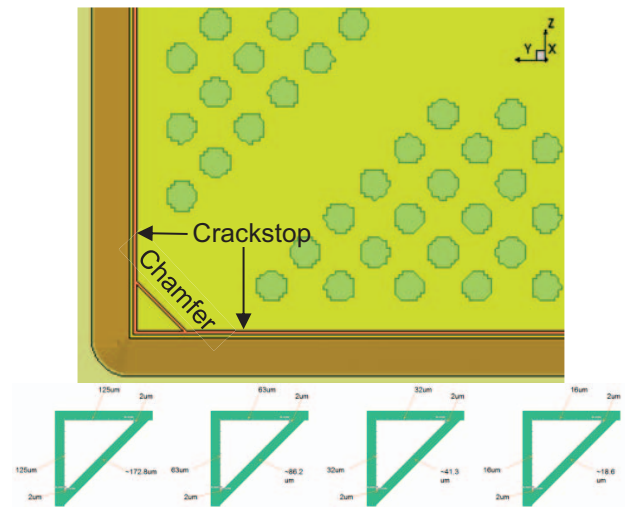


Figure 12 – Top: location of chamfer with the corner of the crackstop. Bottom: different dimensions of chamfer element considered in the simulation.

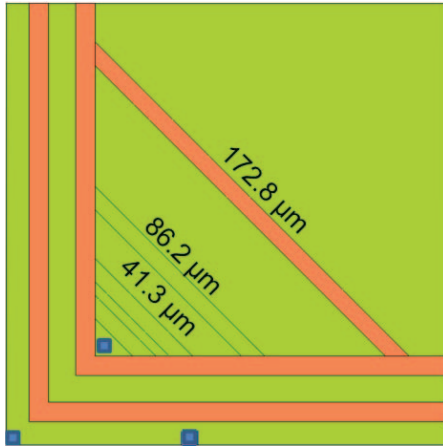


Figure 13 – Locations of initial cracks, indicated by the blue squares, considered for j integral calculations: corner, inside the chamfer triangle, and edge.

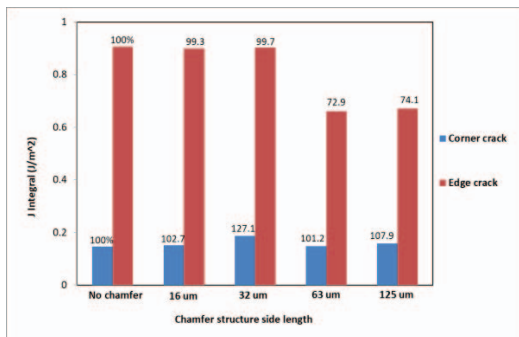


Figure 14 – J integral values for various chamfer structure side lengths for both corner crack and edge crack.

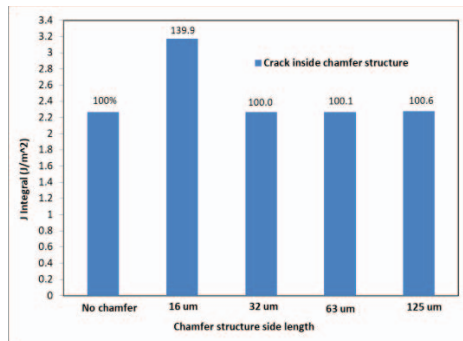


Figure 15 – J integral values for various chamfer structure side lengths for the inside crack.

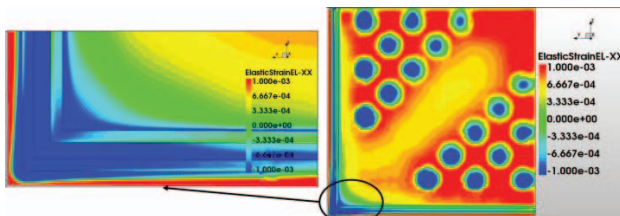


Figure 16 – The optimum chamfer structure side length is such that the vertex of the chamfer triangle is close to the point where the peeling strain switches from compressive to tensile.

EFFECT OF CHAMFER SUPPORT STRUCTURE ON ROBUSTNESS OF PHOTONIC CAVITY

Optical communication over fibers has been in use in the telecommunication industry for a few decades given its ability to carry large amounts of data at extremely high speeds. Silicon photonic ICs offer the telecommunications industry a major advantage since they can be fabricated with the existing infrastructure of the semiconductor industry, enabling low cost and mass-fabrication. The optical fibers are, typically, integrated into the silicon die through an optical cavity in the die as presented in figure 17. The internal and external corners of this cavity suffer from high thermo-mechanical CPI stresses due to the differences in coefficients of thermal expansion (CTE) between the various materials present in the cavity and around it. The results of a 3D simulation, similar to the one described in the corner CPI strain analysis section, is shown in figure 18. Peeling strain in the optical cavity corners is tensile and has much larger magnitude compared to the die corners indicating that the optical cavity is at much higher mechanical failure risk compared to the die corners. The main reason for the higher strain in the optical cavity is the absence of side support from the underfill in the cavity as shown in figure 19. The internal corner has no support from the underfill while the external corner has support only from one of two sides. On the other hand, the tensile principal strain is lowest in the internal corner.

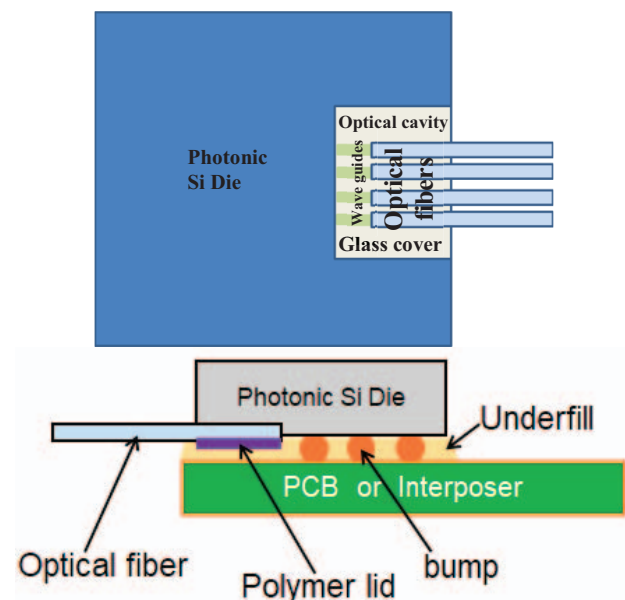


Figure 17 – Top: schematic top view of an optical die with optical fibers attached to the die through an optical groove. Bottom: cross section of the die showing the location of the fibers and the solder bumps.

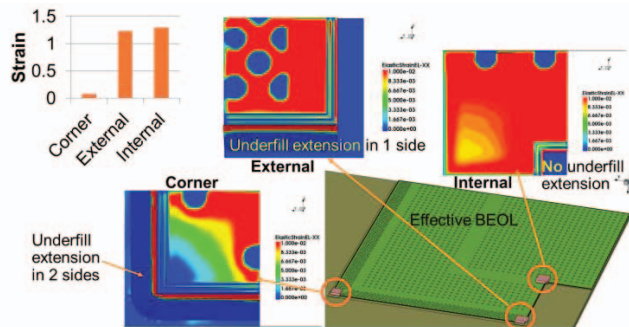


Figure 18 – Peeling strain in the optical cavity corners is tensile and has much larger magnitude compared to the die corners.

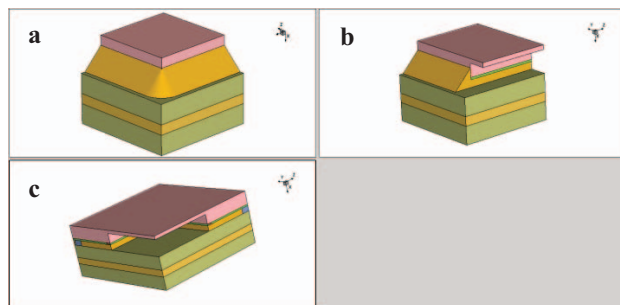


Figure 19 – a) Corner of the die surrounded with underfill extension from two sides, b) external corner of the optical cavity with underfill extension only on one side, and c) internal corner of the cavity with no underfill extension.

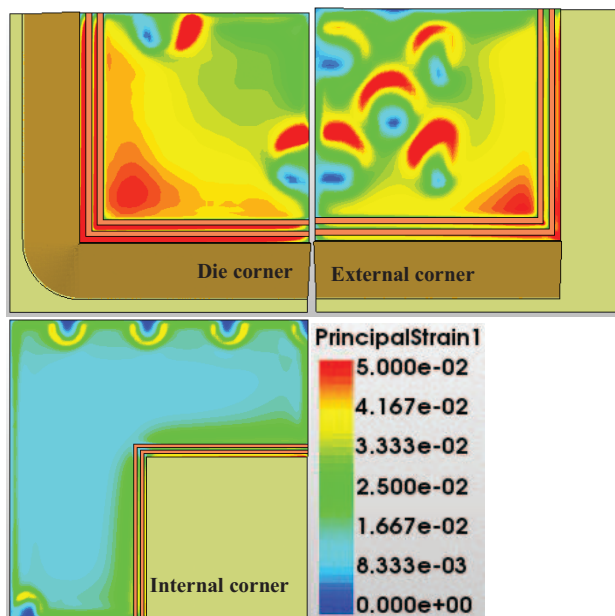


Figure 20 – Principal strain 1 is highest in die corner and external corner of the optical cavity and lowest in the internal corner of the optical cavity.

A chamfer structure was added to the external corner and the effectiveness of different sizes of chamfer structures was compared. Similar to the results presented in the previous section, the optimum chamfer size was the

largest possible size that doesn't create a pocket of high strain in the chamfer structure triangle. A side length of 70 μm reduced the average corner strain by 33% compared to the case with no chamfer structure as shown in figure 21. A support structure could reduce the peeling strain in the internal corner by 21% as shown in figure 22.

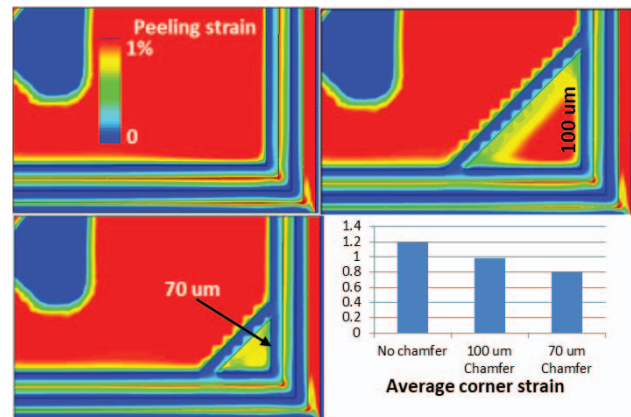


Figure 21 – Comparison of the effectiveness of various chamfer structure sizes in reducing peeling strain in the external corner of the optical cavity.

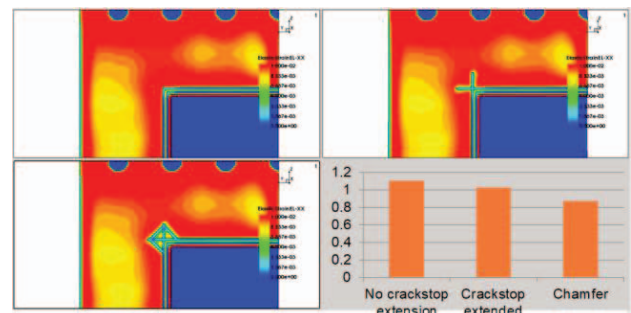


Figure 22 – Comparison of the effectiveness of various corner support structures in reducing peeling strain in the internal corner of the optical cavity.

CONCLUSION

Experimental results show that die with edge size larger than 12 mm results in higher probability of crack propagation at the corner of the die. The die size effect was confirmed using FEM simulations. The effect is more pronounced when the underfill elasticity modulus is low. On the other hand, the low underfill modulus results in lower corner strain. A chamfer structure was used to reduce probability of crack propagation at the corner. FEM simulations were used to optimize the chamfer structure size. It was found that the optimum chamfer structure side length is such that the vertex of the chamfer triangle is close to the point where the peeling strain switches from compressive to tensile. Simulations showed the effectiveness of chamfer structures in protecting internal and external corners of the optical cavity of the photonic ICs.

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