

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS
AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01405

U.S. Patent No. 9,245,826

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE

TABLE OF CONTENTS

I.	Introduction.....	1
II.	There Is No Material Dispute over the Level of Ordinary Skill in the Art	3
III.	Claim-Construction Disputes	3
	A. HID’s construction of “disposed in ... [a] corner” is detached from the intrinsic evidence and undermined by the extrinsic evidence.....	4
	B. HID’s construction of “on a bottom surface” improperly strays from this term’s plain and ordinary meaning	9
IV.	Ground 1: Anticipation by <i>Conn</i>	15
	A. “at least one anchor via disposed in at least one corner” (claims 1, 11).....	15
	1. <i>Conn</i> discloses “disposed in ... [a] corner” under its plain and ordinary meaning.....	15
	2. <i>Conn</i> discloses “disposed in ... [a] corner” under HID’s construction.....	18
	B. “said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate” (claims 9, 19).....	20
V.	Ground 2: Obviousness over <i>Conn</i>	23
VI.	Ground 3: Obviousness over <i>Gambino</i> and <i>Conn</i>	23
VII.	Ground 4: Anticipation by <i>Torii</i>	27
	A. <i>Torii</i> discloses “at least one anchor via does not provide ground connection to one or more active devices”	27
	B. <i>Torii</i> discloses “a backside metal layer on a bottom surface of said semiconductor substrate”	29
VIII.	Ground 5: Anticipation by <i>Ide</i>	30

IX.	Conclusion	30
-----	------------------	----

I. Introduction

Samsung's Petition ("Pet."), supported by the testimony of Dr. Thompson, presented five grounds showing that claims 1-20 are unpatentable as anticipated or rendered obvious. In contesting these grounds, HID's Patent Owner Response ("POR") raises two new improper claim construction arguments, mischaracterizes teachings of the prior art, and distorts Petitioner's proposed motivations to combine. As explained below, the Board should reject HID's arguments.

On Ground 1 (anticipation by *Conn*), HID disputes *Conn*'s teaching of (1) "disposed in ... [a] corner" in independent claims 1 and 11; and (2) "bonded to a metal layer overlying said semiconductor substrate" in dependent claims 9 and 19. HID argues that *Conn* does not disclose the first claim limitation under either its plain and ordinary meaning or HID's erroneous claim construction. But HID fails to address the Petition's evidence that *Conn*'s array of anchor vias is spread over the entire surface of the substrate such that some of the anchor vias are "disposed in ... [a] corner" under both interpretations of this term. Regarding the second claim limitation, HID argues that *Conn* cannot meet this limitation while still satisfying the claim requirement of "not provid[ing] ground connection to one or more active devices in said semiconductor substrate." HID is wrong because the relevant embodiment of *Conn* discloses that the anchor vias are not used for the purpose of providing electrical connection to active devices, and whether or not the

metal filler of the anchor vias is bonded to the overlying metal layer does not change this.

On Ground 2 (obviousness by *Conn*), HID relies solely on its arguments for Ground 1, leaving unchallenged and thus conceding the additional obviousness points detailed in the Petition.

On Ground 3 (obviousness by *Gambino*, *Conn*, and/or *Ding*), HID attacks the motivation to combine *Gambino* and *Conn*. It argues the anchor vias created by *Gambino*'s process would provide ground connection to active devices. But this argument ignores the fact that the anchor vias planted on *Gambino*'s corner-located dummy metal pad are designed for providing mechanical support, rather than electrical connection. HID's other arguments also mischaracterize the cited prior art and fail to confront the abundance of motivation-to-combine evidence in the Petition.

On Ground 4 (anticipation by *Torii*), HID first repeats its pre-institution argument that *Torii*'s sub-TSVs (the claimed anchor vias) are used as a subsidiary current pathway, thereby providing ground connection to active devices. But the subsidiary current pathway is only one of the disclosed embodiments, while the Petition is based on the alternative embodiment in which the sub-TSVs are not used as a current pathway at all. HID's second argument is premised entirely on its claim-construction argument that "on" requires direct contact between the backside

metal layer and substrate surface. But the Board should reject this construction because it improperly adds limitations to the term’s plain and ordinary meaning.

On Ground 5 (anticipation by *Ide*), HID presents a similar argument based on its erroneous construction of “on” and the argument likewise falls with its claim construction.

The Board should cancel all challenged claims.

II. There Is No Material Dispute over the Level of Ordinary Skill in the Art

HID argues that a person of ordinary skill in the art (“POSITA”) would hold only a bachelor’s degree, rather than the master’s degree identified in the Petition. *Compare* Paper 17 (POR), §IV, *with* Paper 1 (Pet.), §V. But HID’s proffered variation is immaterial. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). Both parties agree that a POSITA would have at least two years of experience in semiconductor design and fabrication, and nothing in HID’s POR identifies any analysis that would turn on whether a POSITA held a bachelor’s or master’s degree. *See* POR §§IV-VII.

III. Claim-Construction Disputes

HID does not dispute Petitioner’s position that independent method claim 11 does not require the steps therein to be performed in their recited order. POR, 29; Pet., 20-22. Thus, no construction is needed for this claim term. Paper 9 (“Inst. Dec.”), 10-11.

HID's Response, however, raises two new claim construction arguments about "disposed in ... [a] corner" and "on a ... surface." POR, 18-29. "[T]he words of a claim are 'generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) (citations omitted). The only exceptions are lexicography or disavowal. *Thorner v. Sony Comput. Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Neither exception applies here. As discussed below, the Board should reject both of HID's constructions, as neither finds support in the intrinsic or extrinsic record. No express construction is needed for these two terms. Inst. Dec., 11.

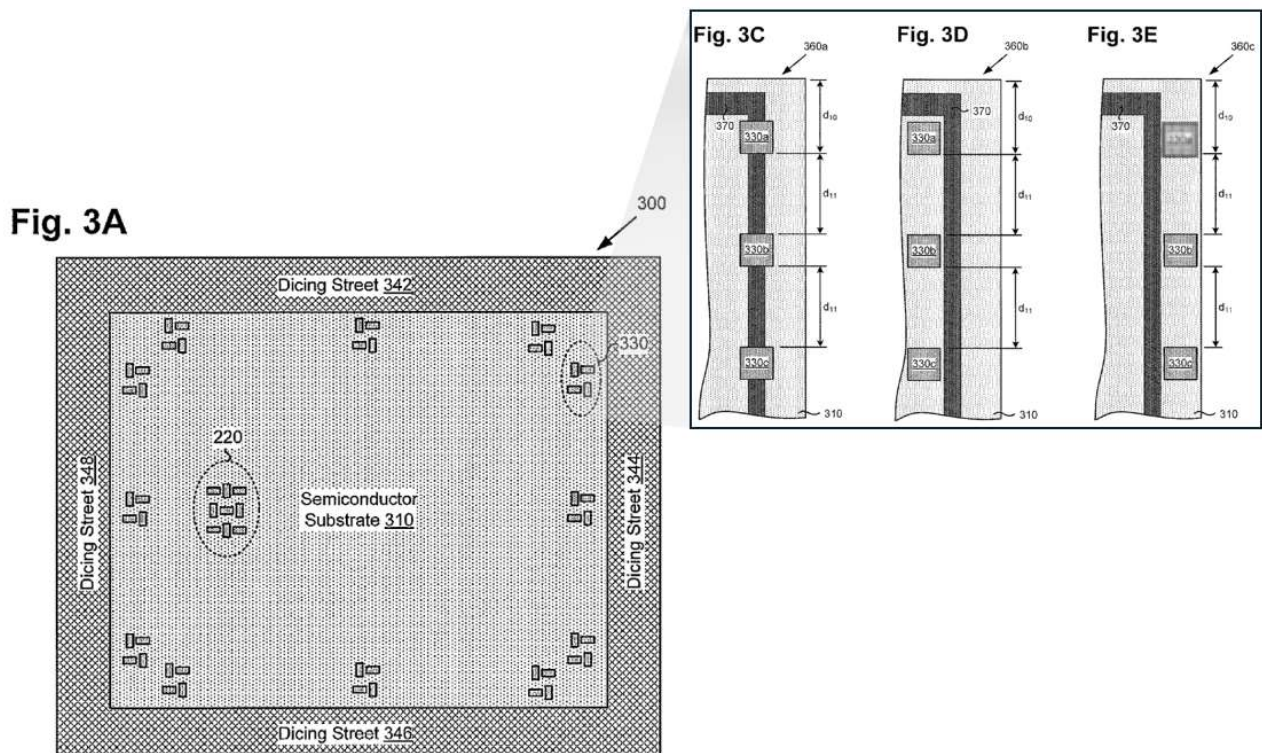
A. HID's construction of "disposed in ... [a] corner" is detached from the intrinsic evidence and undermined by the extrinsic evidence

HID proposes construing the claimed "disposed in at least one corner of a semiconductor substrate" to mean "located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die." POR, 18. Yet the intrinsic and pre-litigation extrinsic evidence cited by HID fails to define a corner this way. Only Mr. Berg's litigation-inspired hand drawings show what the alleged round and ovoid geometrical shapes look like. *Id.*, 19-21; Ex. 2004 ("Berg"), ¶¶46-50.

HID first argues its construction is derived from the '826 patent's purported purpose of disposing the anchor vias in the die corners to prevent the die from

cracking. POR, 18. But the '826 patent's claims, specification, and file history do not contain any evidence suggesting that the cracking *only* happens in the areas prescribed by HID's construction or that the anchor vias *must* be placed in these areas to prevent the cracking. *See generally* '826 patent; Ex. 1002.

Tellingly, HID and Mr. Berg are unable to cite anything from the '826 patent to suggest an area delineated by “a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.” POR, 18; Berg, ¶¶36-42. Figures 3A and 3C-3E—discussed in Mr. Berg's declaration—do not show anything resembling such a geometrical shape.



'826 patent, Figs. 3A, 3C-3E; Berg, ¶¶37-39. Rather, Mr. Berg concedes that these figures illustrate a different way to determine whether an anchor via is disposed in

a die corner. Berg, ¶¶37-39. Namely, Mr. Berg says that the cluster of anchor vias 330 in Figure 3A is disposed in a corner of the die and quotes the accompanying text of Figures 3C-3E, which describes that this cluster of anchor vias (i.e., cluster 330a, 330b, or 330c) is formed a predetermined distance from the corner. *Id.* (citing '826 patent, 6:65-67); '826 patent, 6:60-7:5, 7:15-19, 7:24-28, Figs. 3A, 3C-3E. Thus, the '826 patent at best contemplates that whether an anchor via is “disposed in ... [a] corner” is determined by its distance from the corner.¹

¹ HID mentions that Samsung “argued that the [“disposed in ... [a] corner”] term is indefinite in the District Court Litigation” but provides no further discussion as to whether this is relevant to the outcome of the present IPR. POR, 18. It is not. Samsung’s indefiniteness argument arises from the '826 patent’s description that the distance for a corner anchor via “may vary depending on the particular application,” '826 patent, 6:65-67, 7:3-5, so it is impossible to ascertain its upper limit. The present IPR does not need to address this issue because the cited prior art teaches anchor vias that are clearly within the range of distance contemplated by the '826 patent. *See, e.g., infra*, §IV.A; Ex. 2009 (“Thompson Dep.”), 39:25-40:14 (“I didn’t need to figure out where the boundary was for how far away from the corner you could be and still be in the corner.”).

This does not support, much less justify, HID's alleged round or ovoid geometrical shape inscribed within die edges.

With no intrinsic evidence supporting its construction, HID turns to extrinsic evidence, but the extrinsic evidence underscores the problems with HID's construction. HID concedes that Exhibit 2006 ("*Lei*") does not discuss "anchor vias" and does not add anything to the intrinsic evidence beyond the recognition that die singulation may induce stress at die corners. POR, 18-19; *Lei*, 5-6. Despite these deficiencies, HID asserts that *Lei* shows that a POSITA would have understood the cracking and thus the anchor vias contemplated by the '826 patent are located outside of the alleged round/ovoid geometrical shape. POR, 19-21 (citing Berg, ¶¶46-50). HID argues that Exhibits 2007 ("*Ho*") and 2008 ("*Rabie*") confirm this understanding.² POR, 21-25. In fact, they undermine HID's argument. *Ho* discloses that the corner delamination area has diverse shapes, of which the crack fronts in Figures 8(c) and 8(d) do not align with HID's alleged round/ovoid geometrical shape.

² *Ho* and *Rabie* both postdate the '826 patent and thus are irrelevant to a POSITA's understanding at the time of the alleged invention. Petitioner has objected to both exhibits. Paper 18.

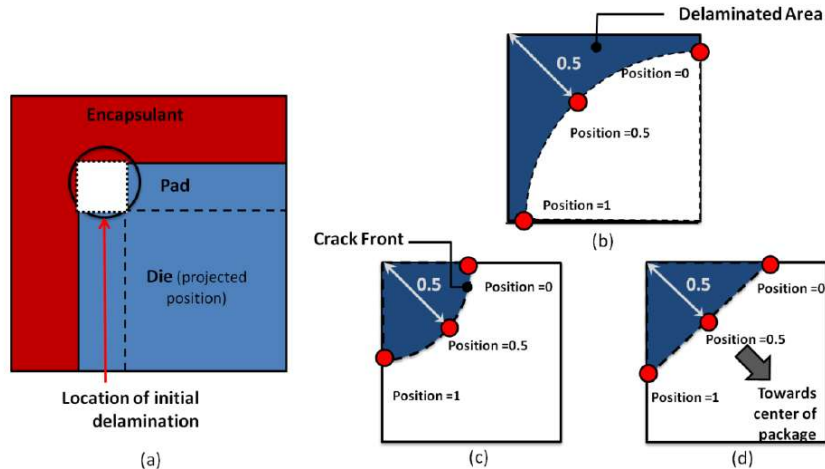


Fig. 8. (a) Illustration of the location of initial delamination (b) A convex initial delamination (c) A concave delamination (d) A straight delamination

Ho, 4 (Fig. 8). And HID agrees that the delamination areas of the semiconductor die in *Rabie*'s Figure 2 are not all located outside the alleged round/ovoid geometrical shape. POR, 24-25; Berg, ¶¶54; *Rabie*, 2 (Fig. 2).

Thus, even assuming that the locations of the cracking- or delamination-prone areas in a die dictate the locations of the claimed anchor vias, HID's purported evidence shows that the cracking- or delamination-prone areas are not limited to those located outside HID's proposed round or ovoid geometrical shape. HID provides no justification for a POSITA to exclude any particular area from the claimed "corner." POR, 18-25. Nor does Mr. Berg. Berg, ¶¶33-55. The Board should reject HID's litigation-inspired construction and apply this term's plain and ordinary meaning—disposed in a distance "proximate to a corner of [a] semiconductor substrate," as understood by a POSITA based on the patent's specification. '826 patent, 6:22-25, 6:65-67; Berg, ¶¶37, 39; Thompson Dep.,

36:21-37:7 (“A corner is just a point, but the claim language allows to be near a corner.”), 39:12-24 (“In the context of the patent, ... disposed[] ... [in] at least one corner means near the corner.”).

B. HID’s construction of “on a bottom surface” improperly strays from this term’s plain and ordinary meaning

Regarding the claim term “a backside metal layer on a bottom surface of said semiconductor substrate,” HID argues that the ’826 patent uses “on” to mean “in contact with.” POR, 25 (citing Berg, ¶57). HID is wrong. As Samsung explained in the Petition, the plain and ordinary meaning of “on” does not require direct contact. Pet., 84 n.12 (citing *AFG Indus., Inc. v. Cardinal IG Co.*, 239 F.3d 1239, 1251 (Fed. Cir. 2001)). The record does not justify deviating from this plain and ordinary meaning.

The Federal Circuit and district courts have both rejected HID’s improper limiting of the plain and ordinary meaning of “on.” In the Federal Circuit’s *AFG* decision, the disputed claim recited a multi-layer structure in which each layer is “formed on” a prior layer. *AFG*, 239 F.3d at 1243, 1251. According to the Federal Circuit, “[t]he parties dispute whether the claim language requires that each successive layer be ‘formed on’ the prior layer in such a way that nothing is interposed between each layer.” *Id.* at 1251. Finding that “the claim does not state that each layer is ‘formed directly on’ the preceding layer,” the Federal Circuit

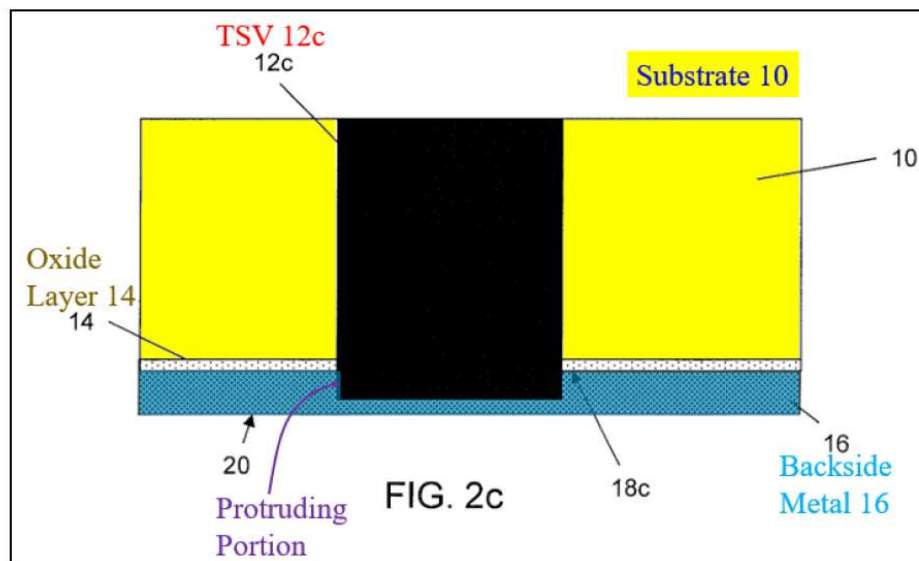
“determine[d] that ‘formed on’ does not mean ‘directly in contact with.’” *Id.* at 1251.

Attempting to distinguish *AFG*, HID argues the claim therein does not recite “bottom surface” as the ’826 claims do. POR, 59. But that does not justify a different outcome. Had “bottom surface” been inserted into the claim in *AFG*, it would recite, in part, “a first ZnO layer formed on *a bottom surface* of the substrate.” *See AFG*, 239 F.3d at 1243. The added language would merely specify which surface of the substrate the first ZnO layer is on, rather than requiring direct contact. Ex. 1034 (“Thompson Suppl.”), ¶12. It would not have changed the Court’s analysis in *AFG* regarding “formed on.”

District courts have reached a similar conclusion as *AFG*. *See, e.g., Epistar Corp. v. Lowes Companies, Inc.*, 2020 WL 771096, *8-10 (C.D. Cal. 2020) (holding that the plain and ordinary meaning of the phrase “formed on” does not require direct contact); *Trustees of Boston University v. Everlight Electronics Co., Ltd.*, 2014 WL 2117509, *6-9 (D. Mass. 2014) (similar). The claims at issue here, like those in *AFG* and similar district court cases, are not limited to being “formed directly on,” and it is therefore incorrect to read this extra limitation into the claims.

Indeed, POSITAs would understand the terms “on” or “formed on” to mean “formed against with or without intervening layers.” Thompson Suppl., ¶¶7-9. This

is consistent with the disclosure of other prior art known to a POSITA. *Id.* For example, *Burnham* discloses that it “relates to structures and methods of **forming** backside metal **on** a Si substrate (Si wafer),” in which “the backside metal is **formed on** an oxide material” and “the oxide material can be **formed on** a backside of a Si wafer.”³ Ex. 1022 (“*Burnham*”), 2:28-36. This oxide material is an intervening layer between the backside metal and Si substrate. To illustrate this structure, *Burnham*’s Figure 2c shows that “the backside metal 16 is deposited directly on the oxide layer 14,” which is in direct contact with the substrate 10 and “acts as an interface” between backside metal 16 and substrate 10.



Burnham, Figs. 2c.

Burnham, 5:1-3, 5:8-13, Fig. 2c; Ex. 1003 (“Thompson Open”), ¶54; Pet., 14-15.

As another example, *Sharma* describes a backside metalization structure in which

³ All emphases are added unless otherwise noted.

“a silver layer [is] **disposed on** the vanadium layer” and “[a]n optional **intermediate layer** ... may be **disposed between** the vanadium layer and the silver layer.” Ex. 1021 (“*Sharma*”), 1:62-2:1. As *Burnham* and *Sharma* illustrate, the plain and ordinary meaning of “on” allows both direct and indirect contact.

To justify its deviation from this plain and ordinary meaning, HID cites various parts of the specification without identifying any clear lexicography or disclaimer. First, relying on Mr. Berg’s conclusory testimony, HID argues that the term “surface” in “on a bottom surface” requires adoption of its construction because a POSITA would understand that a metal layer must directly contact a surface to be “on” it. POR, 26; Berg, ¶57. Not so. As discussed above, a POSITA would understand that forming a metal layer on a surface of a substrate means that the metal layer can indirectly contact the substrate through an intervening layer. This is similar to a tea cup resting “on” a table surface via a tea coaster. Thompson Suppl., ¶¶10-11.

Next, HID argues that claims 9 and 19 use “a metal layer overlying said semiconductor substrate” to draw a distinction between “overlie (or underlie)” (not requiring direct contact) and “on” (requiring direct contact). POR, 26. Wrong. The ’826 patent specification uses “underlying” and “on” a bottom side interchangeably. ’826 patent, 3:12-17 (“the **underlying** backside metal stack 150, which may be formed **on** bottom side 112 of semiconductor substrate 110 as

shown in more detail in FIG. 1B”); Thompson Suppl., ¶13. It follows that “overlying” and “on” a front side are also interchangeable. *Id.* The difference between “overlie” and “on” is that overlie specifies “on the front” without having to use the word “front.” *Id.*

Additionally, HID argues that the specification confirms its construction. POR, 27. Wrong again. HID cites the “purpose of the ... invention,” but this disclosure does not say the backside metal layer is in direct contact with the substrate. *Id.* (citing ’826 patent, 1:16-46). HID also asserts that Figure 1B shows a backside metal stack in which “[e]ach layer is in direct contact with the layer which it is ‘formed on.’” POR, 28. But this argument fares no better than HID’s “purpose” argument. The description of Figure 1B proves HID’s construction is improper because, like *AFG*, it merely says each layer is “formed on” or “deposited on” a prior layer—phrases that do not require direct contact, rather than using phrases that expressly require direct contact. *Compare* POR, 27-28 (citing ’826 patent, 3:43-48, 3:51-55), with *Burnham*, 2:28-31, 5:8-13 (explaining “conventional devices ... [have] the backside metal 16 [] **formed directly on** the backside of the Si wafer” while “the present invention ... **form[s]** backside metal **on** a Si substrate (Si wafer)” with “the oxide layer 14[] ... act[ing] as an **interface**”), and Ex. 1026 (“*Hsu*”), [0025] (expressly stating “metal finish 60 includes nickel layer 62 **directly on, and contacting**, RDL pad 52”); *see also*

Sharma, 1:18-22, 1:62-66 (“**disposed directly on** the backside of a wafer”); Thompson Suppl., ¶14.

Moreover, although Figure 1B does not show any intervening layer between the bottom surface of the substrate and the backside metal stack, it is improper to use this particular embodiment to limit the claimed invention. *Thorner*, 669 F.3d at 1365-66; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1346-47 (Fed. Cir. 2015). Indeed, the ’826 patent expressly teaches against limiting the purported invention to “particular implementations.” ’826 patent, 7:51-55, 7:45-49 (“a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts”). Thus, it is wrong to read “deposited on” and “formed on” to require direct contact.

As Dr. Thompson explained, a POSITA would use additional words like “directly on” or “directly contact” to describe layers that are in direct contact with each other. Thompson Suppl., ¶15; *supra*, *Burnham*, 5:1-3, 5:8-13; *Sharma*, 1:18-22, 1:62-66; *Hsu*, [0025]. The specification does not use the word “directly” when describing this embodiment, much less clearly express an intent to redefine “on” from its plain and ordinary meaning. *See AFG*, 239 F.3d at 1247, 1251 (refusing to construe “formed on” to mean “directly in contact with” because “the claim language and the specification permit the presence of interlayers between layers”

and including them “do[es] not materially affect the basic and novel properties of the invention”) (citation omitted).

The Board therefore should reject HID’s argument about “on” because the intrinsic record does not support it. HID’s only extrinsic evidence, Mr. Berg’s declaration, tracks the arguments in the HID’s Response, and hence the Board should reject his arguments for the same reasons discussed above. *See* Berg, ¶¶56-63.

IV. Ground 1: Anticipation by *Conn*

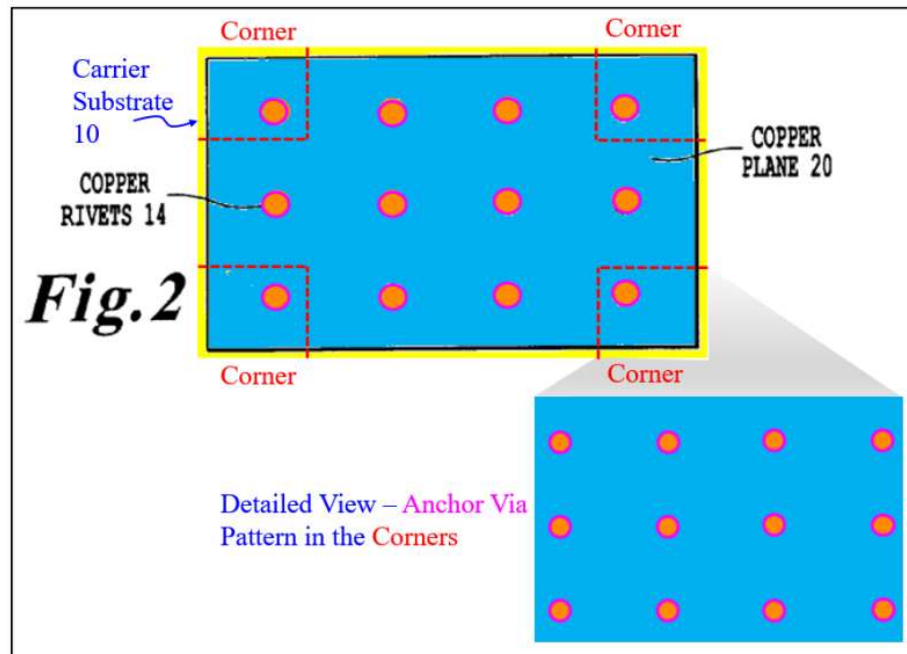
A. “at least one anchor via disposed in at least one corner” (claims 1, 11)

1. *Conn* discloses “disposed in ... [a] corner” under its plain and ordinary meaning

Regarding Ground 1, HID first recycles its pre-institution argument that *Conn* does not disclose the “disposed in ... [a] corner” limitation under its plain and ordinary meaning. POR, 32-36.

At institution, the Board correctly rejected this argument and credited “Dr. Thompson’s testimony concerning how an ordinarily skilled artisan would understand *Conn*’s disclosure.” Inst. Dec., 17. Neither HID’s post-institution response nor Mr. Berg’s declaration offers any new analysis or evidence to support HID’s attorney argument, so the Board should reject this argument for the same reasons the Board rejected it at institution. POR, 32-36; Berg, ¶¶79-87.

Particularly, HID agrees that Figure 2 of *Conn* shows a “pattern” of anchor vias. POR, 33. As the Petition demonstrated, *Conn* discloses that the pattern “spreads across the substrate and extends to its corners.” Pet., 38 (citing *Conn*, [0031], [0035], Fig. 2.)



Conn, Fig. 2 (modified).

Id., 39. The above figure shows a blow-up of a corner where the pattern reaches. Thompson Dep., 45:20-46:9. *Conn* discloses the anchor vias in this pattern have a

spacing as small as 60 micrometers.⁴ *Conn*, [0035]; Thompson Dep., 35:14-36:9, 39:25-40:14, 40:24-41:12. A POSITA would understand that this distance is “the width of a human hair,” and “under any reasonable definition, that would be near the corner of the die.” Thompson Dep., 35:14-36:9.

HID argues that the spacing between the anchor vias “does not describe the distance between the vias and edges of the substrate.” POR, 34. This contradicts a POSITA’s understanding. As Dr. Thompson explained, when a grid of anchor vias is over the die like in *Conn*, a POSITA would understand that some of the anchor vias are positioned from the die corners at a distance “pretty close to” the spacing. Thompson Dep., 40:24-42:9.

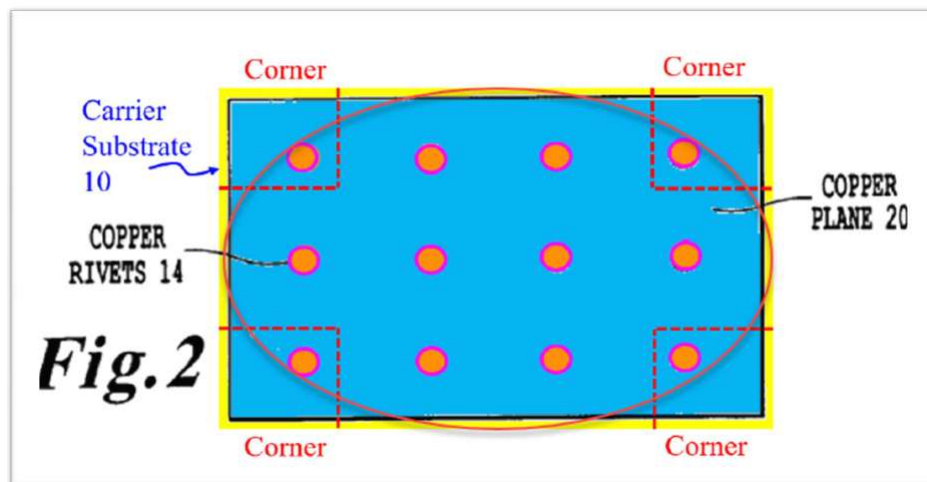
Finally, HID argues that *Conn* does not disclose “anchor vias” used for compensating mechanical stresses. POR, 34-36. But it cannot deny the fact that *Conn* expressly calls its vias “anchor vias” and says they are used to “mechanically” connect the conducting layers to the substrate. *Conn*, Abstract, [0038], [0040].

⁴ HID argues *Conn*’s figures do not show specific dimensionalities. POR, 36. This allegation erroneously ignores *Conn*’s express disclosure of the same. Thompson Dep., 35:14-36:15, 39:25-42:6, 45:6-16.

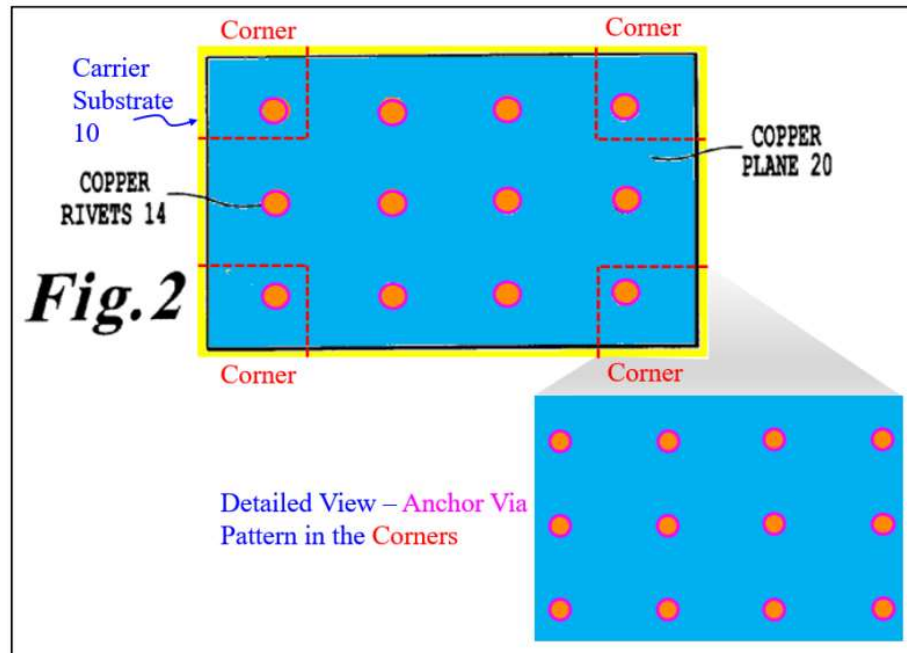
2. *Conn* discloses “disposed in ... [a] corner” under HID’s construction

Alternatively, HID argues that *Conn* does not disclose the “disposed in ... [a] corner” limitation under its proposed construction. In particular, HID draws an ovoid geometrical shape on Figure 2 of *Conn* and argues that there are no anchor vias falling outside the shape. POR, 37.

But HID fails to address the Petition’s showing that the corner, in detailed view, contains multiple anchor vias, some of which are disposed outside of the ovoid geometrical shape. Petition, 39 (citing *Conn*, [0031], [0035]-[0036], Fig. 2); *see also* Thompson Open ¶94 (explaining such corner can contain as many as 400 anchor vias). The difference between the Petition’s evidence and HID’s limited showing are compared below. HID adds the ovoid geometrical shape as the following:



POR, 37. In contrast, the Petition’s annotated figure illustrates the anchor via pattern in the corners of the carrier substrate:



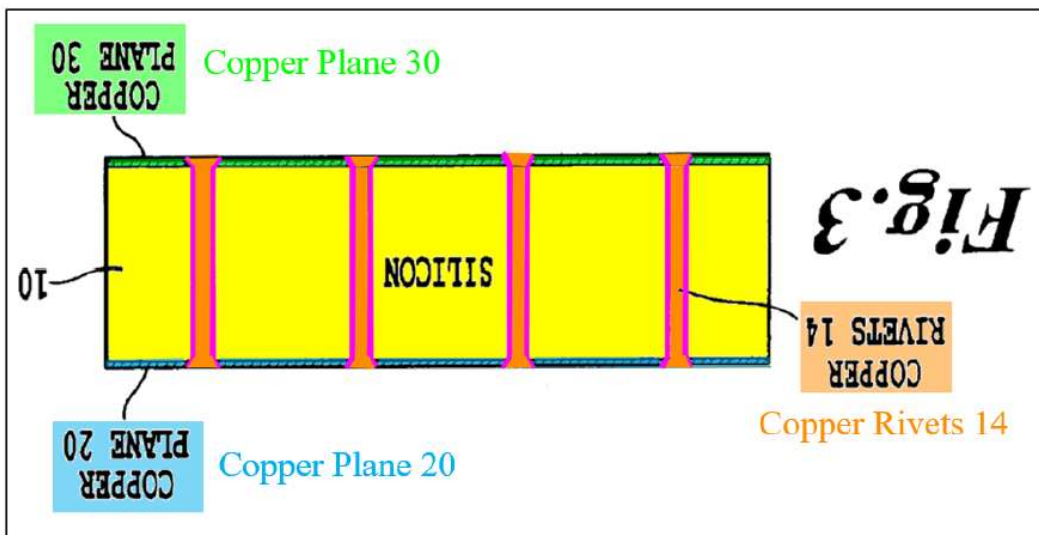
Conn, Fig. 2 (modified).

Pet., 39. As discussed in §IV.A.1, with a distance no more than 60 micrometers (i.e., hair’s width) from the die corners, *Conn*’s pattern of anchor vias fills in the regions outside the ovoid geometrical shape. Thompson Dep., 37:8-22 (“And then with a spacing of that grid, one would know that these anchor vias can be extremely close to the corner. So at least one, two, three -- some number of those would be in the corner.”); *see also id.*, 45:6-16. As such, *Conn* also discloses the “corner” limitation even under HID’s construction because *Conn*’s anchor vias lie outside HID’s ovoid geometrical shape (i.e., within the corners).

B. “said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate” (claims 9, 19)

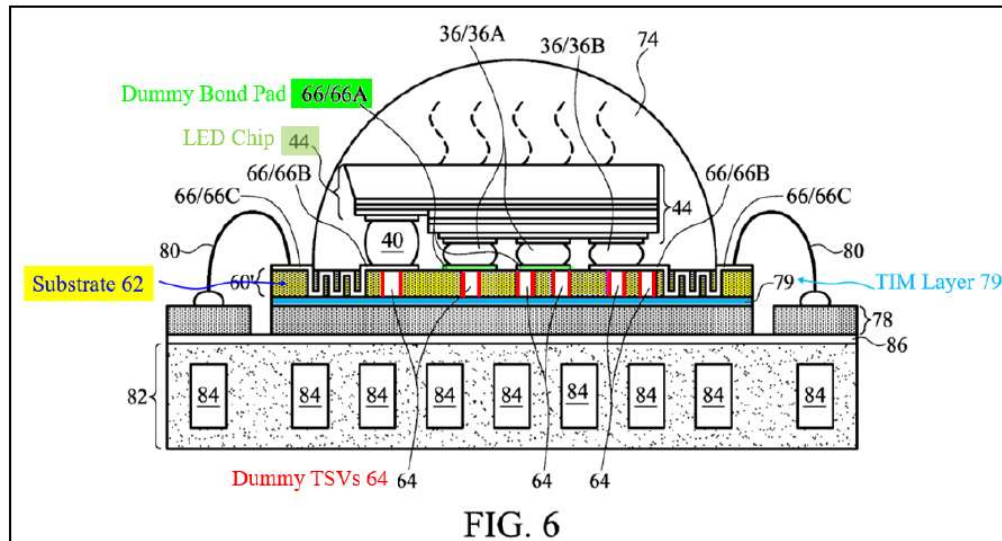
HID’s response also presents an additional argument regarding dependent claims 9 and 19 that further requires the metal filler of the anchor vias to bond to a metal layer overlying the substrate. Namely, HID argues that *Conn*’s Figure 3, on which Petitioner relies for teaching claims 9 and 19, shows the metal filler of the anchor vias connects the two copper planes on the opposing sides of the substrate and therefore it must provide ground connection to active devices. POR, 38-43. HID is wrong.

As the Petition explained, *Conn* discloses that the anchor vias (or the via conductor) extend from the first main surface of the carrier substrate but do not need to reach the opposing second main surface. Pet., 37 (citing *Conn* at [0028]). So *Conn*’s anchor vias are not used for providing electrical connection to active devices; otherwise, it would be impossible to vary the length of the anchor vias or via conductor. *Id.*; Thompson Suppl., ¶19. Figure 3 of *Conn* shows the extreme case of such variation, with both anchor vias and via conductor extending to the opposing second main surface, but that does not mean they provide electrical connection to active devices. *Conn*, [0038]; Thompson Suppl., ¶19.



Conn, Fig. 3 (rotated by 180°).

Pet. 43. The Petition provided prior-art examples in which fully extended through-vias are used for nonelectrical functions. Pet., 10-13. For example, like *Conn*, *Wang* discloses conducting layers **TIM layer 79** and **dummy bond pads 66A** disposed on the opposite sides of the substrate 62. *Id.*, 47. *Wang*'s **dummy TSVs 64** connect to both **TIM layer 79** and **dummy bond pads 66A**, but **they** are used for heat dissipation, not electrical connection. *Id.* This confirms that anchor vias can connect the metal layers on the opposing sides of the substrate, while not providing ground connection to any active devices. Thompson Suppl., ¶20.



Wang, Fig. 6.

Pet., 46.

As commonly understood in the art, merely connecting the anchor vias' metal filler to both metal layers on the opposing sides of the substrate is not sufficient to provide ground connection to active devices. Thompson Suppl., ¶21. For example, establishing the ground connection also requires the metal layers be patterned properly. The '826 patent itself acknowledges this well-accepted fact:

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or **if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the metal filler within anchor vias 132 and 133 essentially has a floating voltage potential during operation.**

'826 patent, 3:12-27; Ex. 1002, 80-81 ('826 prosecution history citing the same).

As discussed above, the anchor vias in *Conn*'s Figures 1-3 do not serve the purpose of providing electrical connection. Figure 3 does not dictate otherwise. A POSITA would understand that the anchor vias in the embodiment in Figure 3 would only be capable of providing ground connection to active devices if the metal layers were patterned to do so, and *Conn* does not disclose such patterning or otherwise suggest the anchor vias provide electrical connection in Figure 3. Thompson Suppl., ¶21; *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1367 (Fed. Cir. 2019) ("a reference need not state a feature's absence in order to disclose a negative limitation") (citation omitted).

V. Ground 2: Obviousness over *Conn*

HID does not provide additional arguments against Ground 2. POR, 43-44. As discussed in §IV.B, the Petition used *Wang* to illustrate it was well known that *Conn*'s structure in Figure 3 can be used to dissipate heat, and it would have been obvious to do so without providing any ground connection. Thus, even if *Conn* is found not to anticipate claims 9 and 19, it renders them obvious.

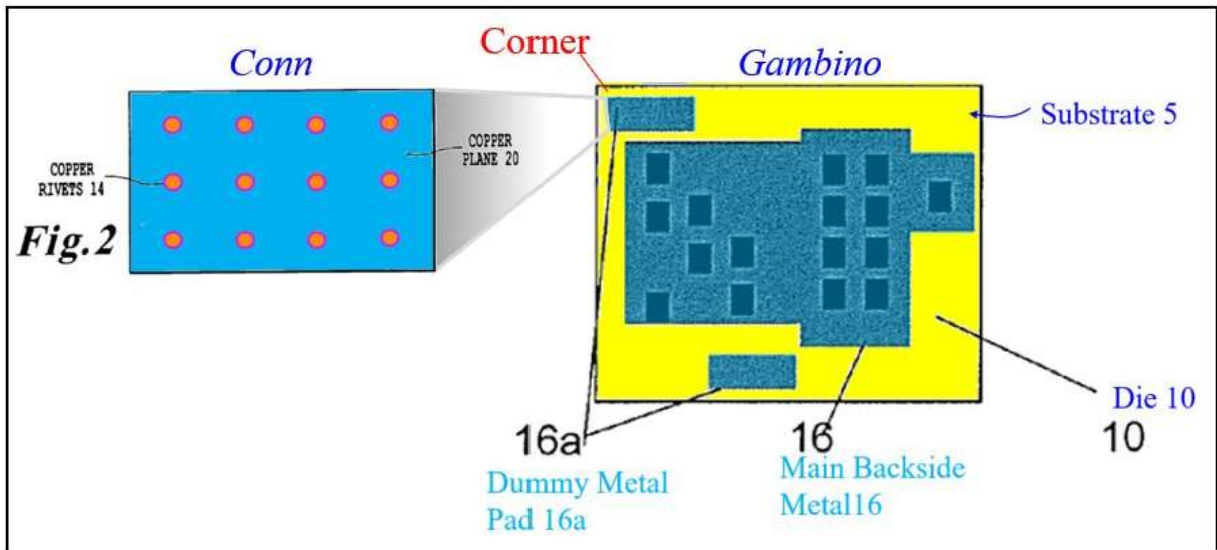
VI. Ground 3: Obviousness over *Gambino* and *Conn*

As to Ground 3, among the many obviousness rationales articulated by the Petition, HID only challenged the use of *Gambino*'s via-forming process to

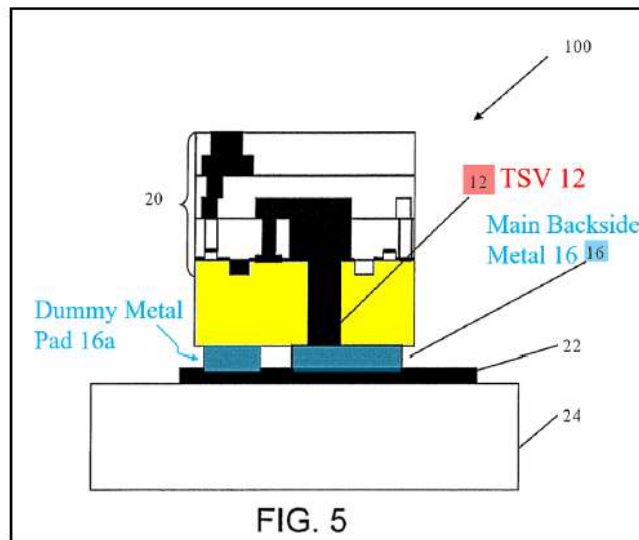
manufacture the anchor vias.⁵ Compare POR, 46-47, with Pet. 61-65. HID alleges “[u]tilizing Gambino’s method to create *Conn* anchor vias would result in one of two outcomes”: (1) “the anchor vias would be filled entirely” through the substrate, or (2) “the anchor vias would not reach the backside metal layer.” POR, 48.

Regarding the first alleged outcome, HID argues that the metal filler of the through-substrate anchor vias “would reach the wiring level and connect it to the ground plane 22,” resulting in ground connection to active devices. *Id.*, 48-50. HID is wrong. As the Petition explained, on the backside of the substrate (*Gambino*, Figure 3), “*Gambino*’s dummy metal pads 16a are located at the corners and peripheries of the substrate, which are less crowded areas that are not usually for planting active/passive devices.” Pet., 64; see also *id.*, 56. There would be no reason to place the wiring layers at the corners and peripheries, because the wiring layers are local to active devices. Thompson Suppl., ¶22. Thus, on the front side of the substrate, a POSITA would not have placed wiring layers in corner/peripheral areas directly above the dummy metal pads 16a. *Id.*; *Gambino*, Fig. 5. It follows that the metal filler of the anchor vias planted at the dummy metal pads 16a would not contact any wiring layers at the front side. Thompson Suppl., ¶22; *Gambino*, Fig. 3.

⁵ HID does not provide any separate argument based on *Ding*. POR, 55.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Gambino, Fig. 5.

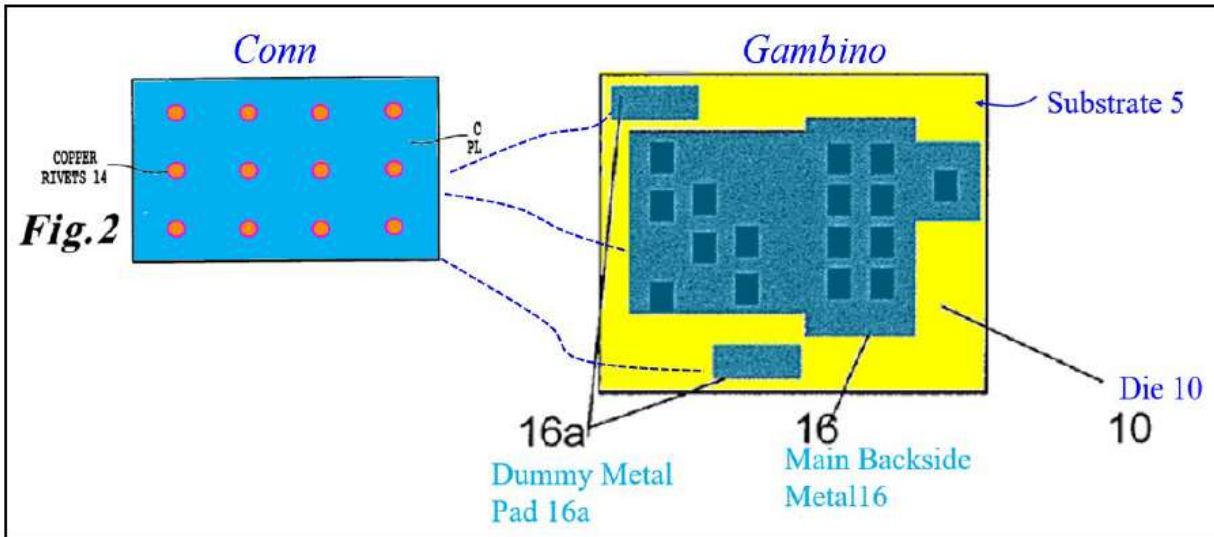
Pet., 69-70.

Moreover, even if the wiring layers were directly above the corner-located dummy metal pads 16a, applying *Gambino*'s process would not cause the metal filler in the vias to provide ground connection to active devices. For example, the

ground connection could be avoided by patterning the wiring layer (*supra*, §IV.B), or recess etching the metal filler from the front side to prevent it from electrically contacting the wiring layers. Thompson Suppl., ¶23. *Gambino* teaches both methods. *Id.* (*Gambino*, [0015], [0026]). A POSITA would have found it desirable to prevent the metal filler from providing ground connection to active devices because neither *Gambino*'s dummy metal pads nor *Conn*'s anchor vias are used for providing electrical connection, and providing the ground connection would unfavorably disturb and require redesign of *Gambino*'s existing active device circuitry. Thompson Suppl., ¶23.

HID also wrongly argues that *Gambino*'s backside polishing or grinding method process would not cause the metal filler of the anchor vias to form a protruding portion extending from the substrate's backside. POR, 50. The Petition showed that backside grinding can yield protruding portions. Petition, 84-85 (*Torii*). Dr. Thompson also confirms that a POSITA would understand *Gambino*'s process could too. Thompson Suppl., ¶24; *see also* Thompson Open, ¶¶54, 145; Thompson Dep. 55:6-17.

HID's second alleged outcome—anchor vias not reaching the backside metal—is a red herring. *See* POR, 51-52. As the following figure reproduced from the Petition shows, Samsung's proposed combination uses the metal filler in *Conn*'s anchor vias to secure *Gambino*'s backside metal.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

Pet., 60-61. Both *Conn* and *Gambino* teach vias forming mechanical connections with the backside metal. *Conn*, Abstract (“anchor vias ... to secure the first conducting layer”); *Gambino*, [0030] (“The TSV 12 is, in turn, in mechanical and electrical communication with the backside metal 16.”). Undoubtedly, applying *Gambino*’s process would create anchor vias anchoring the backside metal.

VII. Ground 4: Anticipation by *Torii*

A. *Torii* discloses “at least one anchor via does not provide ground connection to one or more active devices”

Regarding Ground 4, HID first repeats its pre-institution argument that *Torii* discloses that the sub-TSV can be used as a subsidiary current pathway, so it provides ground connection. POR, 55-56. HID mischaracterizes *Torii*.

The relevant disclosure of *Torii* states:

Note that in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

Torii, [0048]. This paragraph expressly teaches that the distinguishing point between the sub-TSVs and main TSVs is that the sub-TSVs are normally not used as a current pathway. Rather than using “and can,” the paragraph uses “but can” to indicate that the subsidiary current pathway is an exceptional case to the “normal” case. *Torii*’s “Summary” of the invention and claim 12 also state the main TSVs are “to constitute a current pathway” but do not recite the same for the sub TSVs. *Id.*, [0015]-[0016], claim 12. Thus, a POSITA reading *Torii*’s disclosure as a whole would understand that the “subsidiary current pathway” is a possible feature of the sub-TSV, but by no means mandatory, so the sub-TSV is used as a dummy (no electrical connection) *or* a subsidiary current pathway. Thompson Suppl., ¶28.

Notably, Mr. Berg does not support HID’s interpretation of *Torii* that the sub-TSVs must be both a dummy and a subsidiary pathway. All he says in his declaration is that “‘releasing static electricity’ is providing a ground connection,” nothing more. Berg, ¶138. In contrast, Dr. Thompson’s testimony squarely addresses the issue of how a POSITA would understand paragraph [0048] of *Torii*.

He testifies that a POSITA would understand that “not used as a current pathway” and “subsidiary current pathway” are alternative embodiments for the sub-TSVs. Thompson Suppl., ¶28. The “not used as a current pathway” embodiment is sufficient to anticipate the no-ground-connection limitation. *Id.*; *FMC Corp. v. Sharda USA, LLC*, 145 F.4th 1326, 1334 (Fed. Cir. 2025) (“an anticipating embodiment in a prior art reference need not be the preferred embodiment”) (citation omitted); *Vicor Corp. v. SynQor, Inc.*, 603 F. App’x 969, 974–75 (Fed. Cir. 2015) (holding an alternative embodiment disclosed by a reference anticipates the patent claim at issue).

B. *Torii* discloses “a backside metal layer on a bottom surface of said semiconductor substrate”

Second, HID argues that *Torii* does not disclose the claimed “backside metal layer on a bottom surface of said semiconductor substrate” under its construction of “on.” POR, 56-59.

For the reasons discussed in §III.B, it would be improper to construe “on” to require direct contact, so the Board should reject HID’s construction. As the Petition demonstrated, the plain and ordinary meaning of “on” does not require direct contact, so the shoulder region of *Torii*’s backside metal layer (constituting of second feed layer 84 alone, or together with rear bump electrode 86 and second metal joining layer 87) is “on” the substrate surface, as claimed. Pet., 84-85. HID does not dispute this. POR, 57-58.

VIII. Ground 5: Anticipation by *Ide*

Like Ground 4, HID argues that *Ide* does not anticipate the claimed “backside metal layer on a bottom surface of said semiconductor substrate” under its proposed construction of “on.” POR, 60-62.

For the same reasons discussed above, HID’s construction is unwarranted and *Ide* discloses this limitation under its plain and ordinary meaning. *See* Pet., 94-96; *supra*, §VII.B.

IX. Conclusion

For the reasons set forth above, and in the Petition, challenged claims 1-20 of the ’826 patent are unpatentable and should be canceled.

Respectfully submitted,

Dated: September 8, 2025

By: / Joshua L. Goldberg /
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(c)(1), the undersigned hereby certifies that the foregoing Petitioner's Reply to Patent Owner's Response contains 5,592 words, excluding the parts exempted under 37 C.F.R. § 42.24(c) as measured by the word-processing system used to prepare this paper.

Dated: September 8, 2025

By: / Joshua L. Goldberg /
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e)(4), the undersigned certifies that the foregoing **Petitioner's Reply to Patent Owner's Response** was served on September 8, 2025, via email directed to counsel of record for the Patent Owner at the following:

Joseph M. Mercadante
Alfred R. Fabricant
Richard Cowell
FABRICANT LLP
411 Theodore Fremd Avenue,
Suite 206 South
Rye, New York 10580
jmercadante@fabricantllp.com
ffabricant@fabricantllp.com
rcowell@fabricantllp.com
PTAB@fabricantllp.com

Patent Owner has consented to service by email.

Dated: September 8, 2025

/ William Esper / _____
William Esper
Senior Litigation Paralegal
Finnegan, Henderson, Farabow,
Garrett & Dunner LLP