

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case No. IPR2024-01405
U.S. Patent No. 9,245,826

**SUPPLEMENTAL DECLARATION OF DR. SCOTT E. THOMPSON, Ph.D.
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 9,245,826**

TABLE OF CONTENTS

I.	Introduction.....	3
II.	Materials Considered	3
III.	Claim Term - “on a bottom surface”	4
IV.	Ground 1: <i>Conn</i> Anticipates Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19.....	12
V.	Ground 3: <i>Gambino</i> -Based Obviousness	16
VI.	Ground 4: <i>Torii</i> Anticipates Claims 1, 8-11, and 18-20.....	22
VII.	Conclusion	24

I. Introduction

1. I, Scott E. Thompson, Ph.D., make the following supplemental declaration in connection with IPR2024-01405 concerning U.S. Patent No. 9,245,826 (“the ’826 patent”) (Ex. 1001).

2. I was retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”). Previously, I submitted an opening declaration (Ex. 1003) in support of Samsung’s Petition for *Inter Partes* Review.

3. I submit this supplemental declaration in response to the Patent Owner’s Response (“POR”) (Paper 17) filed by Harbor Island Dynamic, LLC (“Patent Owner” or “HID”). I was asked to address certain arguments raised by HID’s POR, as well as certain testimony provided by HID’s expert, Mr. John Berg, in his declaration (Ex. 2004). My lack of direct response to other points or issues raised in the POR or by Mr. Berg’s declaration should not be construed as agreement or admission. Nothing in the POR or Mr. Berg’s declaration changes the opinions that I expressed in my opening declaration.

II. Materials Considered

4. In forming my opinions in this supplemental declaration, I have reviewed and considered the Board’s Institution Decision (Paper 9), HID’s POR, Mr. Berg’s declaration, and all of the materials cited therein. I have further relied

upon my experience, professional background, and knowledge of the relevant art, as detailed in my opening declaration and curriculum vitae. All of the foregoing are incorporated herein by reference. In addition, I have relied upon the materials considered in my opening declaration (Ex. 1003, §IV), as well as the documents directly cited to in this supplemental declaration.

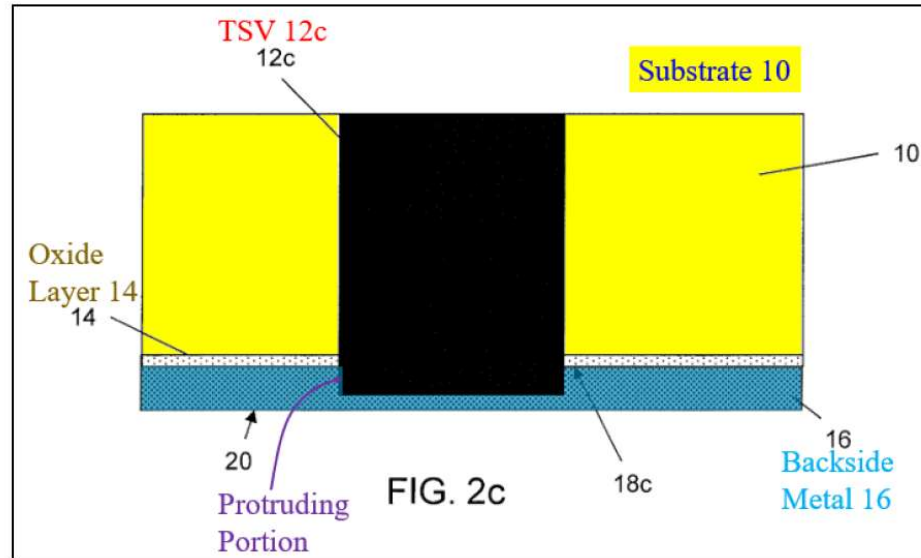
III. Claim Term - “on a bottom surface”

5. Independent claim 1 recites, in part, “a backside metal layer on a bottom surface of said semiconductor substrate.” Ex. 1001 (“’826 patent”), 7:64-65. Similarly, independent claim 11 recites, in part, “forming a backside metal layer on a bottom surface of said semiconductor substrate.” ’826 patent, 8:40-41. In my opening declaration, I applied the plain and ordinary meaning of these terms. Namely, they recite that at least a part of the backside metal layer is disposed on the bottom surface of the semiconductor substrate, with or without intervening layers. Ex. 1003 (“Thompson Open”), ¶¶179, 185, 197, 204.

6. I understand HID and Mr. Berg construe “a backside metal layer on a bottom surface of said semiconductor substrate” as “a backside metal layer in contact with a bottom surface of said semiconductor substrate.” POR, 25-26; Ex. 2004 (“Berg”), ¶56. They argue that the ’826 patent uses “on” to mean “in direct contact.” POR, 25-26; Berg, ¶57. I disagree.

7. In my opinion, POSITAs would have understood the terms “on” or “formed on” to mean “formed against with or without intervening layers.” This is consistent with how the terms were used and understood in the art, including the prior art I cited in my opening declaration.

8. For example, *Burnham* (Ex. 1022) discloses that it “relates to structures and methods of **forming** backside metal **on** a Si substrate (Si wafer),” in which “the backside metal is **formed on** an oxide material” and “the oxide material can be **formed on** a backside of a Si wafer.” *Burnham*, 2:28-36 (emphases added). This oxide material is an intervening layer between the backside metal and Si substrate. To illustrate this structure, *Burnham*’s Figure 2c shows that “the backside metal 16 is deposited directly on the oxide layer 14,” which is in direct contact with the substrate 10 and “acts as an interface” between backside metal 16 and substrate 10.



Burnham, Figs. 2c.

Burnham, 5:1-3, 5:8-13, Fig. 2c; Thompson Open, ¶54. As such, a POSITA would understand the term “forming on” in *Burnham* allows both indirect contact (e.g., “**forming** backside metal **on** a Si substrate (Si wafer)”) and direct contact (e.g., “the backside metal is **formed on** an oxide material”).

9. As another example, *Sharma* (Ex. 1021) describes a backside metalization structure in which “a silver layer [is] **disposed on** the vanadium layer” and “[a]n optional **intermediate layer** ... may be **disposed between** the vanadium layer and the silver layer.” *Sharma*, 1:62-2:1 (emphases added). A POSITA thus would understand *Shama* uses the term “disposed on” to mean the silver layer is disposed against the vanadium layer, with or without an intervening layer. In other words, the silver layer in *Sharma* can be in direct or indirect contact with the vanadium layer.

10. The above usage of “on” by the prior art is also consistent with how it is used in plain English. For example, “a tea cup resting on a table surface” encompasses the situation where a tea coaster is placed between the tea cup and table surface. Likewise, “an apple on a table surface” would permit a table cloth on the table surface.

11. Mr. Berg asserts the phrase “bottom surface” used in the ’826 claim language requires the backside metal layer to be in direct contact with the substrate because “[i]f the metal layer could be on the substrate but not in direct contact, the use of ‘surface’ would be irrelevant.” Berg, ¶57. I disagree. A POSITA would have understood that a metal layer can be formed on a surface of a semiconductor substrate by indirectly contacting it through an intervening layer, e.g., an oxidation layer. *See supra* (discussion of *Burnham*). This is similar to a tea cup resting on a table surface via a tea coaster, or an apple being placed on a table surface covered by table cloth. Thus, a POSITA would not have considered the use of “surface” to require direct contact.

12. As to the relevance of the “bottom surface” used in the ’826 claims, a POSITA would understand that it specifies which surface the backside metal layer should be formed against, rather than requiring direct contact as alleged by Mr. Berg. As I explained in my opening declaration, the surfaces of a semiconductor are not all equivalent and they may differ “on the specific structures,

manufacturing processes, and/or functions of the semiconductor devices at issue.”

Thompson Open, ¶42. Thus, semiconductor literature often used terms such as “top surface,” “rear surface,” “backside surface,” “bottom surface,” etc., to distinguish the surfaces of a substrate. Thompson Open, ¶¶42-44 (citing *Tezcan*, *Torii*, and *Cronin*). Whether a surface is a “bottom surface” is context specific. Thompson Open, ¶42. In the context of the ’826 patent claims, a POSITA would understand that the “bottom surface” refers to the surface of the substrate’s backside.

Thompson Open, ¶42. Accordingly, a POSITA would understand that this term is used to specify a particular surface of the substrate, but not direct or indirect contact. For example, a POSITA would understand that “a first ZnO layer formed on the substrate” allows the first ZnO layer to be formed on any surface of the substrate, while “a first ZnO layer formed on a bottom surface of the substrate” specifically requires the first ZnO layer be formed on the bottom surface of the substrate (as opposed to other surfaces). A POSITA would not have read the “bottom surface” in this example to require direct contact between the first ZnO layer and the bottom surface of the substrate.

13. Mr. Berg also asserts that the term “a metal layer overlying said semiconductor substrate” in claims 9 and 19 “would indicate to a POSITA that overlying and on have different scope[,] [a]s a layer can overly [*sic*] a substrate while not being in contact with the surface,” whereas the “use of ‘on the bottom

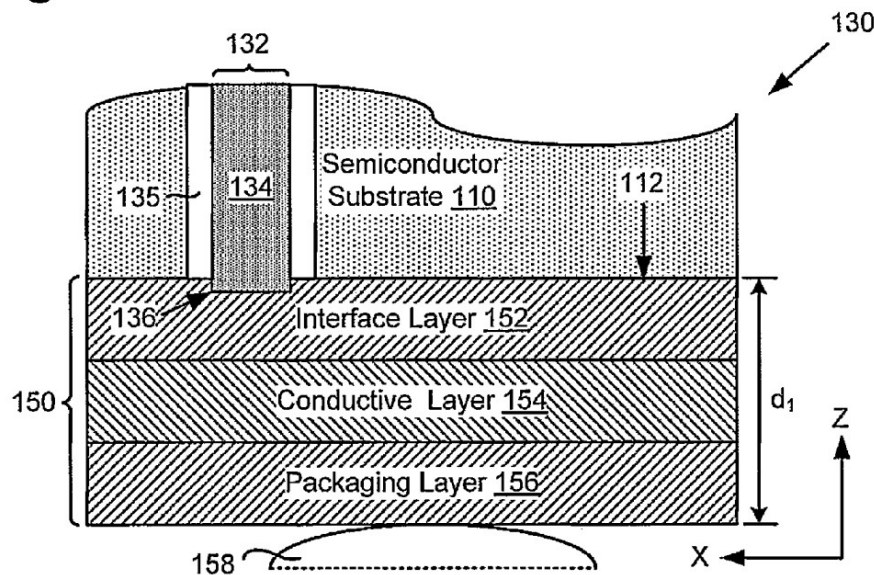
surface’ in Claims 1 and 11 denotes direct contact.” Berg, ¶58. I disagree. In my opinion, a POSITA would not have inferred from the use of “overlying” that “on” requires direct contact. The specification of the ’826 patent states “the **underlying** backside metal stack 150, which may be formed **on bottom side** 112 of semiconductor substrate 110 as shown in more detail in FIG. 1B.” ’826 patent, 3:12-17 (emphases added). Here, the ’826 patent uses “underlying” and “on” a bottom side interchangeably. In view of that, a POSITA would understand that “overlying” and “on” a front side are also interchangeable. Thus, a POSITA would understand the difference between “overlying” and “on” is that overlying specifies “on the front” without having to use the word “front,” and would not have read this difference to suggest “on” is limited to direct contact.

14. Mr. Berg also asserts that the specification of the ’826 patent confirms his construction. Berg, ¶59. Specifically, he points to the embodiment shown in Figure 1B, which describes a backside metal stack where “interface layer 152 is deposited on bottom side 112 of semiconductor substrate 110,” “[c]onduction layer 154 may then be formed on interface layer 152,” and “[p]ackaging layer 156 may then be formed on conduction layer 154.” Berg, ¶61; ’826 patent, 3:43-48, 3:51-55. Unlike Mr. Berg, I do not read the specification as suggesting direct contact between these layers. Just like the prior art and plain English

examples discussed above, “deposited on” and “formed on” used in the specification do not suggest direct contact.

15. Moreover, a POSITA would have no reason to interpret Figure 1B to exclude the prior art that forms an oxide layer between the backside metal and substrate (*supra*, *Burnham*, 2:28-36, Fig. 2c) or allows an optional intermediate layer disposed between the backside metal layers (*supra*, *Sharma*, 1:62-2:1).

Fig. 1B



'826 patent, Fig. 1B.

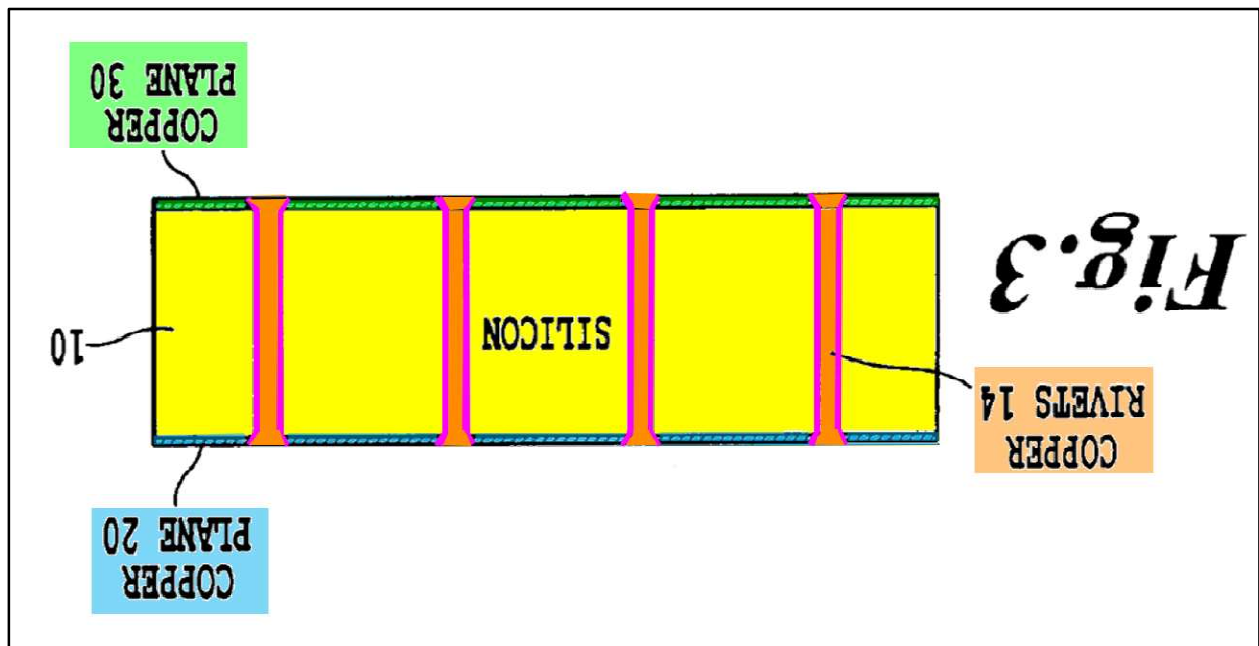
A POSITA would use additional words like “directly on” or “directly contact” to describe layers that are in direct contact with each other. *E.g.*, *Burnham*, 5:1-3 (“the backside metal 16 is deposited directly on the oxide layer 14”), 5:8-13 (“the backside metal 16 is formed directly on the backside of the Si wafer”); *Sharma*, 1:18-22, 1:62-66 (“disposed directly on the backside of a wafer”); *Hsu*,

[0025] (“directly on, and contacting, RDL pad 52). In fact, during the deposition process of a metal on a substrate, a chemical- or thermal-induced oxide would often be formed on the surface of the substrate before the metal is deposited on the substrate. Thus, unless special effort is taken, the final product by default would contain an intervening oxide layer between the metal and substrate. Similarly, without additional words expressly signaling direct contact, a POSITA would understand the metal formed on a substrate allows intervening layers. The ’826 specification does not use these additional words. Nor does it suggest any intent to redefine “on” from its plain and ordinary meaning. So there is no reason for a POSITA to read it as requiring direct contact. In addition, the ’826 specification repeatedly cautions against using any particular embodiment to limit the claimed invention. ’826 patent, 7:45-49 (“a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts”), 7:51-55 (“the present application is not limited to the particular implementations described above”). Thus, a POSITA would not have read the embodiment of Figure 1B as requiring the claimed backside metal layer to be in direct contact with the bottom surface of said semiconductor substrate.

16. For at least the above reasons, I disagree with Mr. Berg’s construction of “on.”

IV. Ground 1: *Conn* Anticipates Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19

17. Regarding Ground 1 (anticipation by *Conn*), I previously opined that *Conn*'s Figure 3 discloses "wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate," as recited in claim 9 and similarly recited in claim 19. Thompson Open, ¶¶100, 109.

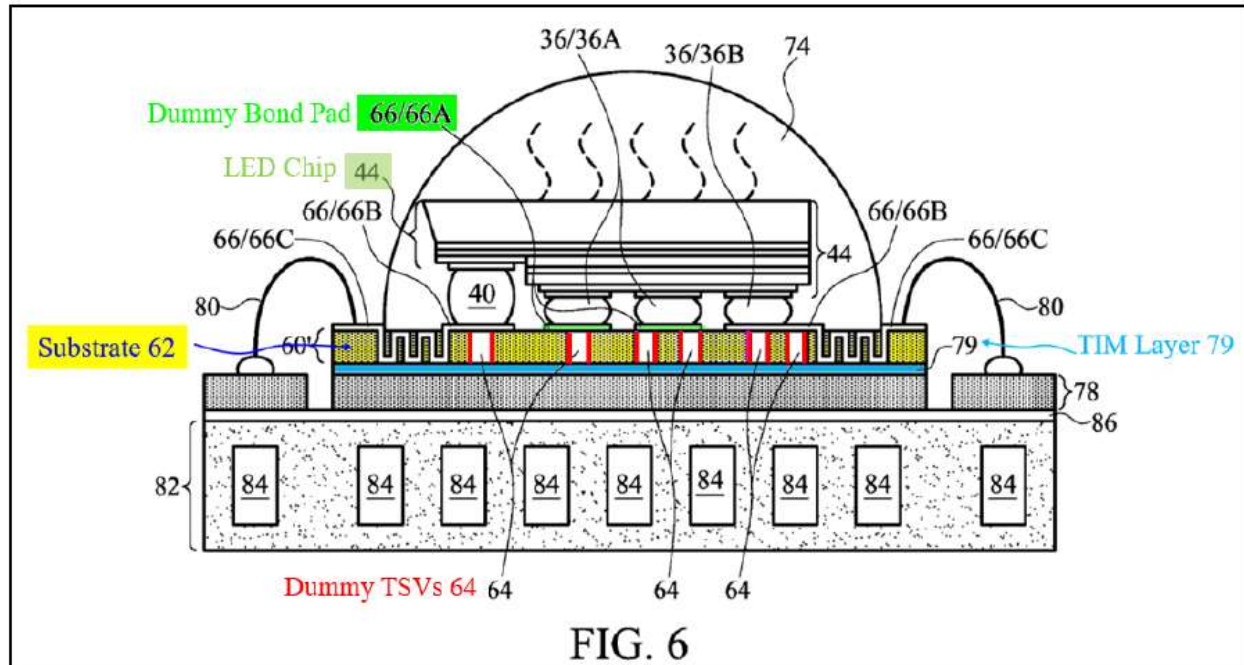


Conn, Fig. 3 (rotated by 180°).

18. Mr. Berg opines that the metal filler (via conductor 14) in Figure 3 connects the two copper planes on the opposing sides of the substrate, and "[a] POSITA would understand that ... the via conductor 14 would provide a ground connection to one or more active devices" because "[a]t least one side of the substrate would contain active devices." Berg, ¶¶100, 104. Mr. Berg mischaracterizes *Conn*.

19. As I discussed in my opening declaration, in connection with Figure 1, *Conn* discloses that the anchor vias (or the via conductor) extend from the first main surface of the carrier substrate but do not need to reach the opposing second main surface. Thompson Open, ¶93 (citing *Conn* at [0028]). Thus, a POSITA would understand that *Conn*'s anchor vias are not used for providing electrical connection to active devices because otherwise it would be impossible to vary the length of the anchor vias or via conductor. Figure 3 of *Conn* shows the extreme case of such variation, with both anchor vias and via conductor extending to the opposing second main surface. *Conn*, [0038], [0040]-[0041]. But it does not mean they provide electrical connection to active devices. This is because the elements in Figure 3 share the same numbers as those in Figures 1 and 2, and the anchor vias in Figure 3 share the same description as those in Figures 1 and 2. *Conn*, [0026]-[0041], Figs. 1-3. Thus, a POSITA would understand the anchor vias in Figures 1-3 are built on the same principles, including not providing electrical connection to active devices.

20. I previously provided various prior-art examples in which fully extended through-vias are used for nonelectrical functions. Thompson Open, ¶¶50-52. For example, as in *Conn*, *Wang* discloses conducting layers **TIM layer 79** and **dummy bond pads 66A** disposed on the opposite sides of the substrate 62. Thompson Open, ¶¶111-113.



Wang, Fig. 6.

Wang's dummy TSVs 64 connect to both TIM layer 79 and dummy bond pads 66A, but they are used for heat dissipation, not electrical connection. Thompson Open, ¶¶111-113. This confirms Conn's teaching that anchor vias can connect the metal layers on the opposing sides of the substrate, while not providing ground connection to any active devices.

21. Mr. Berg appears to assume that if the metal filler of the anchor vias connects both metal layers on the opposing sides of the substrate, then the metal filler must be electrically connected to the active device on that side. Berg, ¶104. This contradicts the common understanding in the art. It was well-known that merely connecting the anchor vias' metal filler to both metal layers on the opposing sides of the substrate is not enough to provide ground connection to

active devices. Whether the metal filler of the anchor vias provides ground connection to active devices depends on multiple factors. For example, establishing the ground connection also requires the metal layers be patterned properly. The '826 patent itself acknowledges this well-accepted fact:

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or **if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the metal filler within anchor vias 132 and 133 essentially has a floating voltage potential during operation.**

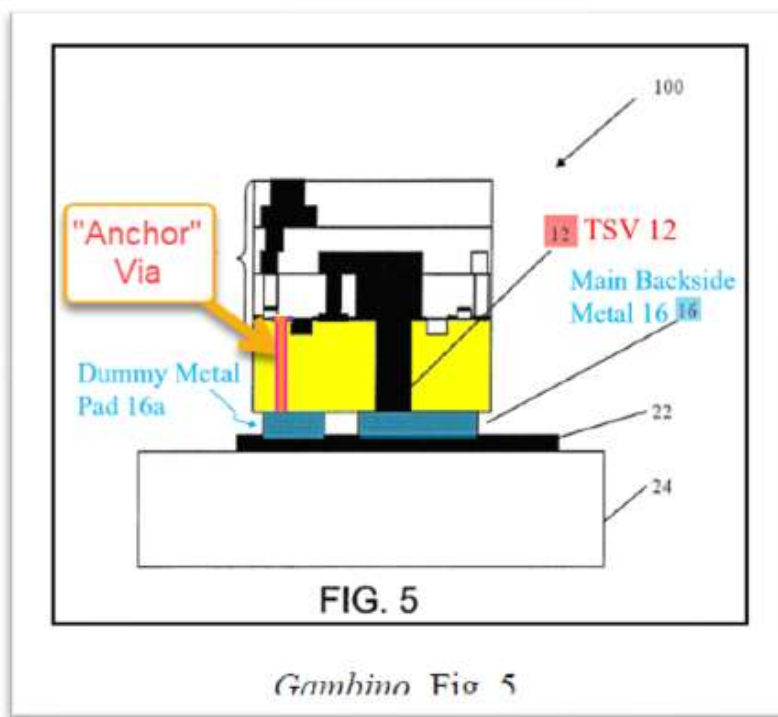
'826 patent, 3:12-27 (emphasis added); Ex. 1002, 80-81 ('826 prosecution history citing the same).¹ The above portion does not describe the purported invention of the '826 patent, but rather just describes the prior art method of patterning a metal layer to form a circuit. As I explain above, the anchor vias in *Conn*'s Figures 1-3 do not serve the purpose of providing electrical connection. Figure 3 does not dictate otherwise. A POSITA would understand that the anchor vias in the embodiment in Figure 3 would only be capable of providing ground connection to active devices if the metal layers were patterned to do so, and *Conn* does not

¹ "[F]loating voltage potential" means the metal filler within anchor vias 132 and 133 essentially is not electrically grounded.

disclose such patterning or otherwise suggest the anchor vias provide electrical connection in Figure 3. Thus, a POSITA would understand that the anchor vias in Figure 3, just like those in Figure 1, do not provide ground connection to any active devices.

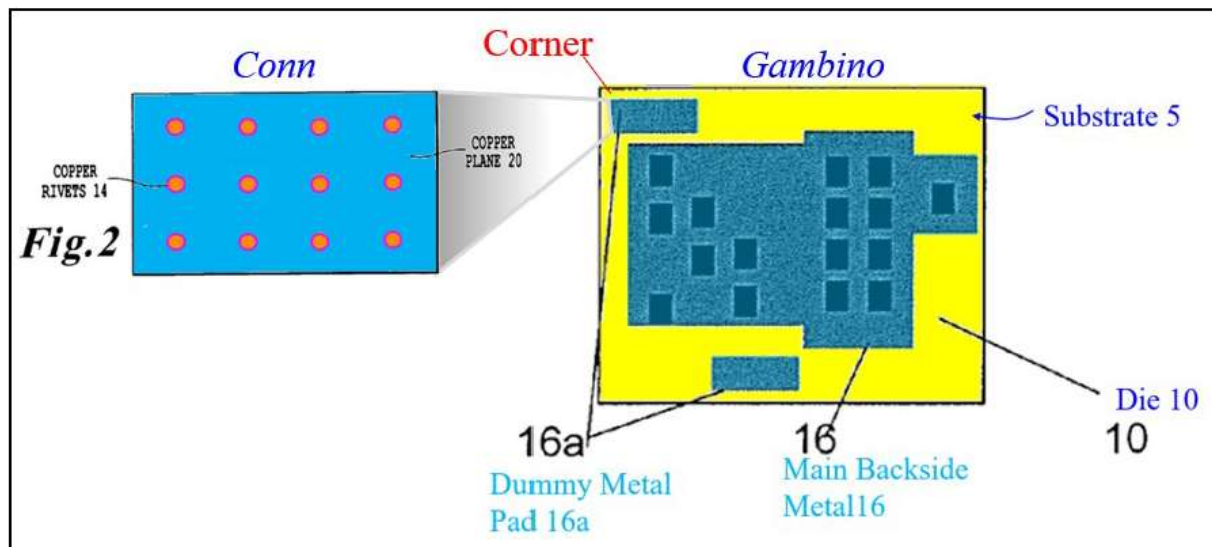
V. Ground 3: *Gambino*-Based Obviousness

22. Regarding Ground 3 (obviousness by *Gambino*, *Conn*, and/or *Ding*), Mr. Berg opines that “[u]tilizing *Gambino*’s method to create *Conn* anchor vias would result in” anchor vias that are “filled entirely, like *Gambino*’s TSVs.” Berg, ¶123. He goes on to assert that this “would provide a ground connection” because “[a]dding a filled anchor via to *Gambino* Figure 5 shows that the anchor via conductor would reach the wiring level and connect it to the ground plane 22.” Berg, ¶124. The *Gambino* Figure 5 modified by Mr. Berg is reproduced below, in which he draws a red anchor via extending from the substrate’s backside to front side, and labels it as “‘Anchor’ Via.”

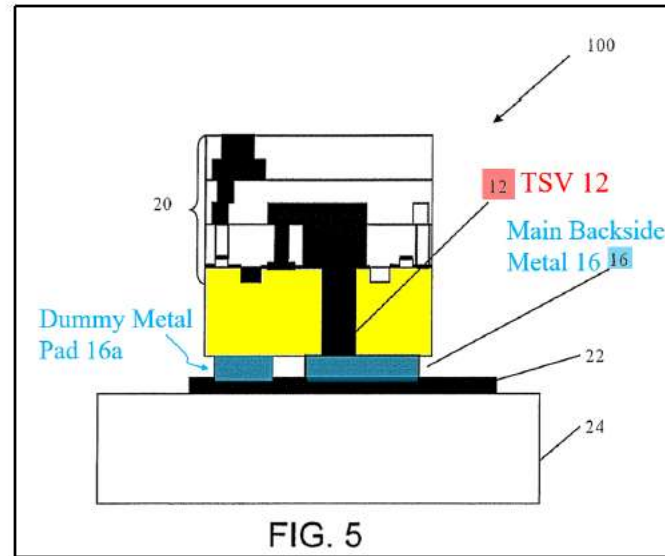


Berg, ¶124 (figure reproduced from Mr. Berg’s declaration, the annotation “‘Anchor’ Via” and associated shape being added by Mr. Berg). I find this figure misleading. The fully-filled anchor via does not need to be connected to any wiring layer on the front side. As shown in Figure 3 of *Gambino*, I previously explained that “*Gambino*’s dummy metal pads 16a are located at the corners and peripheries of the substrate, which are less crowded areas that are not usually for planting active/passive devices, so adding the anchor vias here would not affect other elements in the devices.” Thompson Open, ¶141. This means no wiring layers would be placed at the corners and peripheries, because the wiring layers are local to the active devices. *See Gambino*, [0030] (“The wiring layers 20 can include vias, wires, and a host of different active or passive devices ...”). Moreover, the

corners and peripheries of a die are close to the dicing channels. *Gambino* teaches locating the active TSVs and their connected backside metal in an area of the die so that they “do[] not interfere with dicing operations performed within the dicing channel” *Gambino*, Abstract; *see also Gambino*, [0004]-[0006], [0015]-[0017], [0021], [0029]. Motivated by the same principle, a POSITA would also have located the wiring layers in areas away from the corners and peripheries, to prevent the wiring layers from interfering with the dicing. Thus, on the front side of the substrate, a POSITA would not have placed wiring layers directly above the corner-located dummy metal pads 16a. *Gambino*, [0030], Fig. 5. As such, the metal filler of the anchor vias planted at the dummy metal pads 16a would not contact any wiring layers.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.



Gambino, Fig. 5.

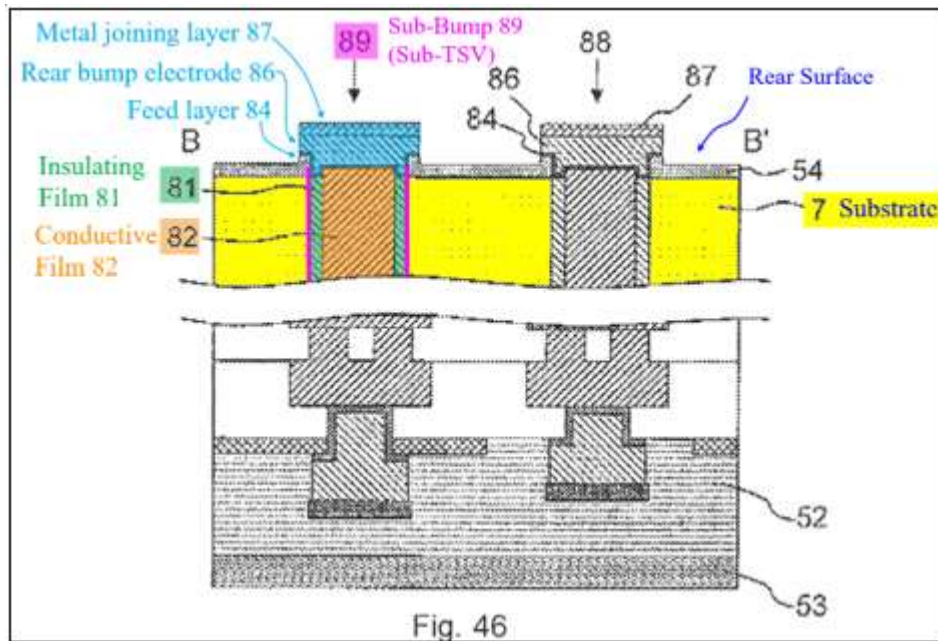
Thompson Open, ¶¶146-147.

23. Moreover, even if the wiring layers were directly above the corner-located dummy metal pads 16a, a POSITA would understand there are other ways to prevent the metal filler in the vias from providing ground connection to active devices. For example, whether the metal filler of the anchor vias provides ground connection to active devices depends on how the front-side metal layers are patterned. *Supra*, §IV. A POSITA would have known how to pattern the front-side metal layer to prevent the metal filler from being electrically connected to any active devices. Such patterning would not require modifications to *Gambino*'s manufacturing process because it already patterns the front side wiring layer and the backside metal layer. *Gambino*, [0015] ("the backside metal is patterned differently than wiring"). As another example, the metal filler of the anchor vias

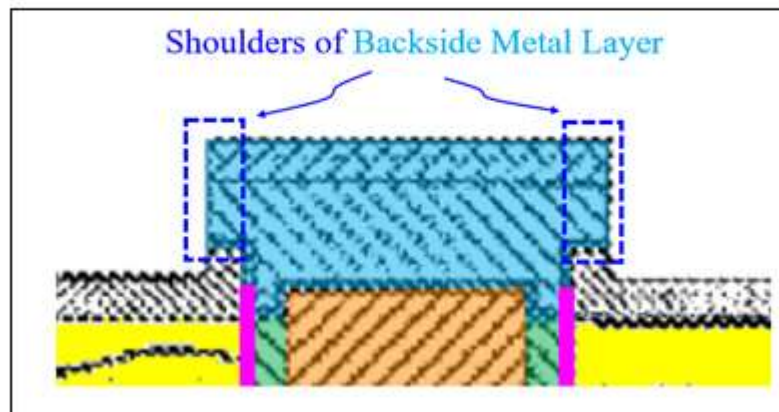
could be recess etched from the front side, making it not contact the front side metal layer. It was well understood in the art that excess metal can be selectively etched away using etchant that only reacts with metal but not the semiconductor substrate, such that no mask is required. This method, again, is already used by *Gambino*, so it would not require modification to *Gambino*'s manufacturing process. *Gambino*, [0026] (“The exposed metal is then removed using a wet etching process with a chemistry to remove the metal in the dicing channel 14.”). A POSITA would have been motivated to prevent the metal filler of the anchor vias from electrically connecting to wiring layers (including active devices) because neither *Gambino*'s corner-located dummy metal pad(s) 16a nor *Conn*'s anchor vias are designed for providing electrical connection. Namely, *Gambino*'s “corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection” Thompson Open, ¶151. And *Conn*'s anchor vias are used for anchoring the metal layers, not for providing electrical connection. *Supra*, §IV. Consistent with these teachings, my proposed combination of *Gambino* and *Conn* uses the anchor vias to secure the backside metal (e.g., corner-located dummy metal pads 16a) to the substrate and prevent delamination during singulation. Thompson Open, ¶¶135-140. Thus, in manufacturing the proposed combination, a POSITA would not have electrically connected the metal

filler of the anchor vias to wiring layers. Making the electrical connection would disturb the existing active device circuitry in *Gambino* and require redesign of it.

24. Mr. Berg further asserts that *Gambino*'s backside polishing or grinding method process would not yield a "protruding portion extending from a backside of said semiconductor substrate" as claimed. Berg, ¶128. I disagree. *Gambino* discloses using "a thinning process, e.g., a polishing and grinding process" to expose the metal filler of the anchor vias at the backside of the substrate. *Gambino*, [0020]. The backside polishing employs a chemical mechanical planarization (CMP) process to flatten and smooth the backside surface. It was well-known that the CMP process can selectively polish the substrate at a higher rate than the metal filler, thereby resulting in a metal protrusion. Ex. 1035 ("Yu"), 4:40-46 ("The second step involved a CMP process which was selective to the material of the insulation layer, although it may be desirable to remove a small amount of the tungsten as well to either to polish the tungsten or to provide a convex protruding plug. If tungsten is removed at this step, it is done at a much slower rate than the removal of the insulation material."). Moreover, I previously showed that the backside grinding process can form a protruding portion.



Torii, Fig. 46.



Torii, Fig. 46 (excerpted, zoomed).

Thompson Open, ¶¶179-180 (citing *Torii*, [0040], [0099]-[0100], Fig. 46). A

POSITA would have understood *Gambino*'s backside grinding process can achieve the same. *Gambino*, [0020].

VI. Ground 4: *Torii* Anticipates Claims 1, 8-11, and 18-20

25. Regarding Ground 4 (anticipation by *Torii*), I previously opined that *Torii*'s sub-TSV discloses the claimed "anchor via." Thompson Open, ¶177. I also

opined that *Torii* discloses claim [1d] (“wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate”), by disclosing the sub-TSV is a dummy “normally not used as a current pathway.” Thompson Open, ¶181 (citing *Torii*, [0048]).

26. The entity of *Torii*’s paragraph [0048] reads:

Note that in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

Torii, [0048] (emphasis added).

27. Mr. Berg focuses on paragraph [0048]’s discussion of using the sub-TSV “as a subsidiary current pathway,” and asserts “[a] POSITA would therefore recognize that *Torii* provides ground connection to one or more active devices in the substrate.” Berg, ¶139. I disagree.

28. Paragraph [0048] of *Torii* expressly teaches that the distinguishing point between the sub-TSVs and main TSVs is that the sub-TSVs are normally not used as a current pathway. Rather than using “and can,” the paragraph uses “but can” to indicate that the subsidiary current pathway is an exceptional case to the

“normal” case. *Torii*’s “Summary” of the invention and claim 12 also state the main TSVs are “to constitute a current pathway” but do not recite the same for the sub TSVs. *Torii*, [0015]-[0016], claim 12. Thus, a POSITA reading *Torii*’s disclosure as a whole would understand that the “subsidiary current pathway” is a possible feature of the sub-TSV, but by no means mandatory. A POSITA therefore would understand the sub-TSV is used as a dummy (no electrical connection), *or* a subsidiary current pathway. That is, “not used as a current pathway” and “subsidiary current pathway” are alternative embodiments for the sub-TSVs. It is my opinion that the “not used as a current pathway” embodiment anticipates “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate,” as claimed.

VII. Conclusion

29. For the reasons set forth here and in my opening declaration, it is my opinion that one skilled in the art would have found claims 1-20 of the ’826 patent anticipated by or obvious over the prior art.

30. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place

within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

31. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: September 8, 2025

By: 

Dr. Scott E. Thompson, Ph.D.