

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioners,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Patent No. 9,245,826

Filing Date: January 27, 2014

Issue Date: January 26, 2016

Inventors: Hadi Jebory, David J. Howard, and Scott B. Stetson
Title: ANCHOR VIAS FOR IMPROVED BACKSIDE METAL
ADHESION TO SEMICONDUCTOR SUBSTRATE

PATENT OWNER'S SUR-REPLY

Case No. IPR2024-01405

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EXHIBIT LIST

Exhibit No.	Description of Document
2001	Docket Control Order, Dkt. 38, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Aug. 5, 2024)
2002	Order Denying Samsung’s Motion to Stay Pending <i>Inter Partes</i> Review, Dkt. 62, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex. Dec. 19, 2024)
2003	Defendants’ Invalidity Contentions, served on September 26, 2024, in <i>Harbor Island Dynamic, LLC v. Samsung Elecs. Co.</i> , Case No. 2:24-cv-00140-JRG-RSP (E.D. Tex.)
2004	Declaration of John Berg
2005	CV of John Berg
2006	“Die Singulation Technologies for Advanced Packaging: A Critical Review” (Lei 2012)
2007	“3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages” (Ho et al., 2013)
2008	“Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks” (Rabie et al., 2021)
2009	Deposition of Scott E. Thompson, taken June 9, 2025

I. INTRODUCTION

Samsung's Reply cannot fix the deficiencies in its Petition. As explained in detail in the POR, Samsung's primary reference, *Conn*, does not disclose the claimed anchor in a corner. Moreover, *Conn* does not disclose Claim 9 and 19's additional limitations.

Samsung's other grounds fare no better. Ground 2 is focused on elements not at issue. Ground 3 combines *Gambino* with *Conn* but the resulting system cannot form anchor vias that meet the claims. And, Grounds 4 and 5 rely on a construction of "on a bottom surface" that is at odds with the '826 Patent's disclosure and the plain meaning of the term.

Accordingly, the Board should issue a Final Written Decision finding all claims not unpatentable.

II. CLAIM CONSTRUCTION

A. "disposed in at least one corner of a semiconductor substrate"

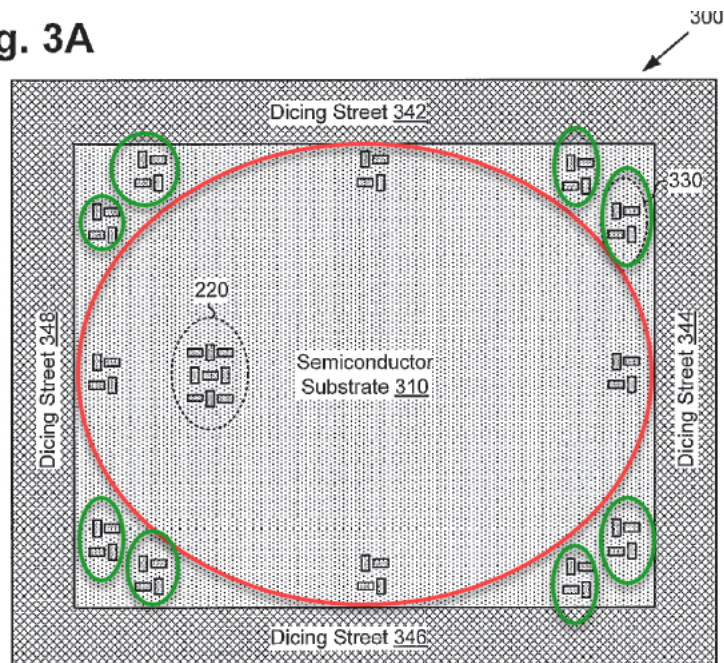
Petitioner does not dispute that: i) the purpose of locating anchor vias in the corner is to reduce cracking; and ii) locating anchor vias in the corner under Patent Owner's construction would reduce cracking.

Petitioner instead insists that Patent Owner's construction is wrong because it would not prevent *all* cracking or because there might be other ways to reduce

cracking. Reply, 5, 8-9. But that is not relevant; the relevant question is what portion of the die a POSITA would understand to be “in a corner.”

As explained in the POR, a POSITA would recognize that a via is disposed in a corner if it is “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.” Samsung argues that Fig. 3A does “not show anything resembling such a geometrical shape.” Reply, 5. But inscribing an ovoid geometrical shape in Fig. 3A reveals that the corner anchor vias are placed so as to be outside the shape.

Fig. 3A



'826 Patent, Fig. 3A (annotation added).

As can be seen above, the anchor via clusters (circled in green) are located just outside the ovoid shape and arranged to follow the curve of the shape. As the specification explains, these vias are “proximate to a corner.” ’826 Patent, 6:23-25.

HID and Mr. Berg explained that a POSITA would understand that locating these anchor vias outside the shape prevents the corner delamination. POR, 21-25. After declining to cross-examine Mr. Berg, Samsung’s Reply ignores that the issue is where to place the anchor vias, and simply notes that the cited papers show cracking and delamination that spread from the corner to the interior of the die (i.e., within the shape). Reply, 7-9. Mr. Berg and HID already addressed this point in the POR: placing an anchor via in the corner prevents the cracking that originates there. POR, 25; Ex. 2004, ¶ 55.

Accordingly, the Board should construe “disposed in at least one corner of a semiconductor substrate” as “located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die.”

B. “a backside metal layer on a bottom surface of said semiconductor substrate”

As the POR explained, the ’826 Patent is directed to improving the adhesion of metal to a semiconductor substrate. POR, 27-28; ’826 Patent, 1:16-46. If the metal cannot remain “securely attached to the substrate,” the process yield will suffer. *Id.*, 1:19-23. As the ’826 Patent notes, the chips it seeks to improve have a backside

metal stack with several layers, “the first of which must form an adhesive bond with the substrate.” *Id.*, 1:24-27. An example of this is a stack with “an interface layer may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer.” *Id.*, 1:27-30. However, “[b]ecause *adhesion of the backside metal stack to the substrate* is almost entirely dependent on the *adhesive qualities between the substrate and the interface layer*, unacceptably low yields are often achieved” *Id.*, 1:33-37 (emphasis added). The inventors of the ’826 Patent thus designed an anchor via structure to mechanically secure the backside metal to the substrate.

The invention of the ’826 Patent is thus designed to overcome insufficient adhesive qualities between the substrate and the interface layer (i.e., the backside metal layer) in these sorts of devices. *Id.*, 1:24-26, 2:44-53. It is beyond dispute that an adhesive bond between metal and substrate (*id.*, 1:24-26) requires direct contact. Otherwise, the patent would discuss the adhesive properties of some intermediate layer. The claimed anchor vias thus supplement that “adhesive bond.”

Rather than beginning with the intrinsic evidence, Samsung relies heavily on irrelevant case law and unrelated references to support twisting the claims of the ’826 Patent away from its actual invention. Indeed, Samsung focuses on how those cases and patents interpret “on,” instead of examining how the ’826 Patent itself uses “on.” Samsung’s focus on extrinsic sources, none of which would be in front of a

POSITA, exposes its construction as a hindsight-based attempt to broaden the claims away from the patent's disclosure.

As explained in the POR, the '826 Patent uses the term “on” to mean directly contacting; as opposed to overlie and underlie, which allows for indirect contact. POR, 26-29. Most critically, when explaining the layers of its example embodiment, the '826 Patent goes to great pains to show that each layer is “formed on” and in direct contact with, the preceding layer. '826 Patent, 3:43-55; Fig. 1B.¹ Samsung cannot grapple with this unambiguous disclosure except to erroneously claim that HID is seeking to limit the claims to a single embodiment.

Petitioner's sole support for its contention that the plain and ordinary meaning of “on a bottom surface” does not require contact is a Federal Circuit case and district court cases discussing entirely different claims and written description. Reply, 9-10. But the *AFG* case on which Petitioner relies did not hold that “on” must always, as a matter of law, not require direct contact. Instead, in that case, the Court found that the specific patent at issue explicitly disclosed “interlayers” that could fall between layers. *E.g., AFG Indus., Inc. Cardinal IG Co.*, 239 F3d 1239, 1245 (Fed. Cir. 2001), (“The patent specification states that interlayers, although optically insignificant, are

¹ This passage uses similar language to the background's description of layers. *Id.*, 1:24-30.

useful to protect the explicitly claimed layers: ‘For the purpose of improving the adhesion or durability of the coating layers, an interlayer having a thickness not to substantially affect the optical properties may be inserted at the interface with the substrate or at the interface between adjacent layers or at the interface with air.’” (quoting patent at issue)).²

The other cases on which Petitioner relies are similarly irrelevant. In *Epistar Corp. v. Lowes Cos., Inc.*, No. LA CV17-03219 JAK (KSx), 2020 WL 771096, at *8-*10 (E.D. Cal. Feb 11, 2020), the term (also, unlike here, “formed on”), was held to encompass intervening layers because “[t]he dependent claims refer to layers ‘formed between’ others.” *Id.* at *9. In *Trs. of Boston Univ. v. Everlight Elecs. Co.*, 23 F. Supp. 3d 50 (D. Mass. 2014), the Court found “grown on” to encompass interlayers because the specification described the possible existence of such. *Id.* at 60-61 (“The XRD pattern shows the difference between a GaN film grown directly on top of the substrate, and that grown on top of a GaN buffer layer.”). These cases are dubious extrinsic evidence, at best, and have no relevance to the term at issue: “on a bottom surface.”

² The Court also noted evidence (entirely lacking here) “that interlayers (or ‘barrier layers’) are routinely, and often necessarily, present in low-emissivity coatings that contain silver.” *Id.*

Samsung further cites to wholly irrelevant references. Both references demonstrate that an inventor who wishes to allow for intervening layers understands that such layers must be specifically described, otherwise “on” would be understood to require contact. For example, *Burnham* provides (and claims) an explicit intervening oxide layer. Ex. 1022, 8:10-18 (“an oxide layer **on** a backside of the substrate” and a “ground plane **on** the oxide layer” (emphasis added)). Indeed, the only time *Burnham* claims its metal layer is “on” the backside, it immediately clarifies that there is an intervening oxide layer. *Id.*, 1:30-35; 2:28-36. Similarly, *Sharma* explains that its invention, in one embodiment, “includes a vanadium layer disposed on the backside of a wafer and a silver layer disposed on the vanadium layer.” Ex. 1021, Abstract. In **another embodiment**, “an **optional** intermediate layer . . . may be disposed between the vanadium layer and the silver layer.” *Id.*, Abstract; *see also id.*, 1:62-2:1.

After raising irrelevant extrinsic evidence, Samsung finally addresses the intrinsic evidence and attempts to read “surface” out of the term. As explained in the POR, any doubt as to whether the metal must be in direct contact is dispelled by reciting “on a bottom **surface**.” POR, 25. Samsung argues instead that “forming a metal layer on a surface of a substrate means that the metal layer can indirectly contact the substrate through an intervening layer. This is similar to a teacup resting

‘on’ a table surface via a tea coaster.” Reply, 12. Samsung provides no argument or evidence to support this; it simply asserts it. *Id.*³

In sum, Samsung’s position is that “on a bottom ” and “on a bottom surface” have exactly the same meaning, improperly rendering “surface” superfluous. *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950-51 (Fed. Cir. 2006) (“claims are interpreted with an eye toward giving effect to all terms in the claim”).

Samsung further waves away the claims’ use of “overlying” to allow for indirect contact. Reply, 12-13. The specification notes “the underlying backside metal stack 150, which may be formed on bottom side 112 of semiconductor substrate 110 as shown in more detail in FIG. 1B.” ’826 Patent, 3:12-17. According to Samsung, this means that “underlying” and “on”⁴ have the same meaning. Reply, 12-13. But, as explained in the POR, underlying *allows* for indirect contact, but does not require it. A layer can underlie the bottom side and be in or not in direct contact. In any event, the cited passage is about the “side,” not the surface.

³ Dr. Thompson similarly provides no evidence or even reasoning to support Samsung’s construction. Ex. 1034, ¶¶ 10-11. He simply assumes that “on a surface” encompasses indirect contact, begging the actual question to be decided. *Id.*

⁴ In this case, “on [the] bottom *side*” and not “on a bottom *surface*.”

Samsung utterly ignores the specification's specific description of the patented invention, improving "metal adhesion to a semiconductor substrate" and avoiding reliance "on the adhesive qualities between the substrate and the interface layer." Reply, 13-15. Samsung's only response to these passages—which are relevant to the invention *only* if the metal directly contacts the substrate—is to simply state that they "do[] not say the backside metal layer is in direct contact." *Id.*, 13. Samsung is incapable of explaining what the passages do say or why the anchor vias at the heart of the invention reach the directly contacted metal layer. *See* POR, 27-28.

The intrinsic evidence makes clear that the '826 Patent's anchor vias only achieve their aim of obviating reliance on "adhesive qualities" while improving adhesion between a metal and a substrate necessitates direct contact between the substrate and the metal layer. Samsung's preference that the inventors recite "directly on" is not a requirement in view of the specification's clear description of the invention. The Board should therefore construe "a backside metal layer on a bottom surface of said semiconductor substrate" as "a backside metal layer in contact with a bottom surface of said semiconductor substrate."

III. GROUND 1

A. *Conn* Does Not Disclose an Anchor Via Disposed in at Least One Corner Under the Plain Meaning

As Petitioner tacitly admits, *Conn* says nothing about any corner of a semiconductor die. POR, 32-35. Instead, Petitioner relies on its counsel's annotations to *Conn*'s Figure 2 and his conclusory testimony as to what a POSITA would understand. Reply, 16. For example, Petitioner argues that *Conn* discloses that its vias are 60 micrometers from the corner. Reply, 16-17. But *Conn* actually states that its vias are spaced 60 micrometers apart. Ex. 1004, [0035] ("A distance between the via conductors is between 60 and 1000 μm ."). Dr. Thompson admitted as much in his deposition.

Q. What kind of die is Conn talking about when he says the anchor vias can be as little as 60 microns from the edge of the corner?

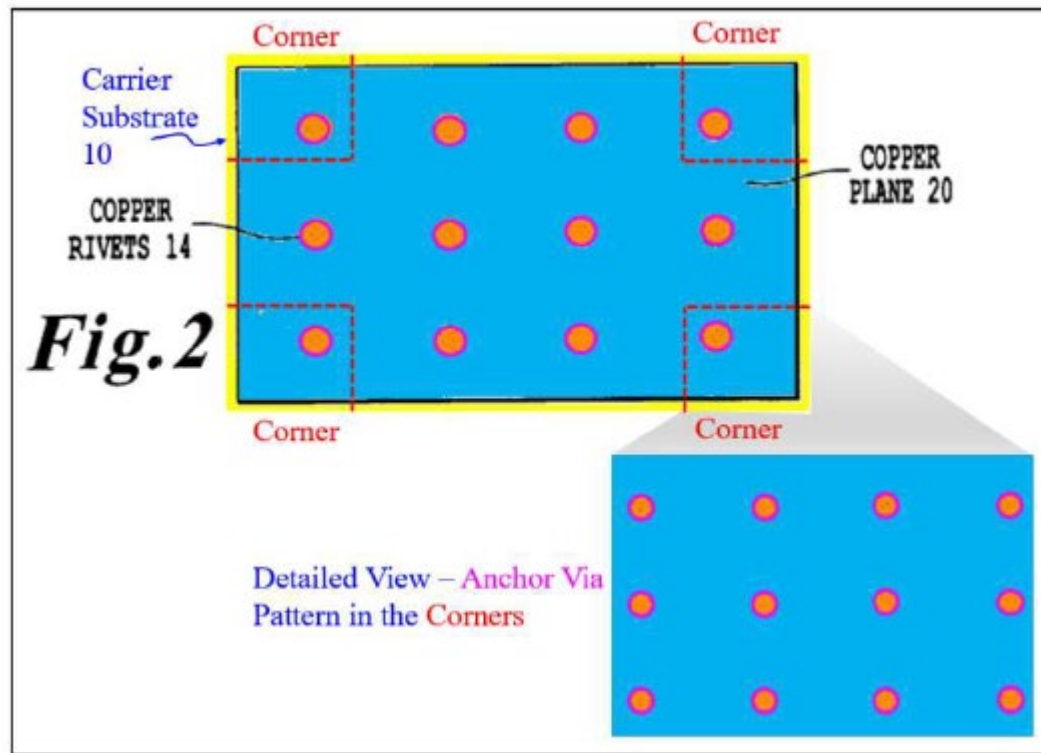
A. Conn's talking about the space between one anchor via and another.

Conn's approach works with many different size dies.

Ex. 2009, 40:15-23 (objection omitted).

While unable to point to any portion of *Conn* that discusses vias in the corner, Petitioner infers that the spacing between vias is the same as the spacing between a via and a corner or edge. Reply, 16-17. Its only support for such is Dr. Thompson's testimony. But Dr. Thompson treats *Conn*'s Fig. 2 as showing the entirety of a die. Ex. 1003, ¶ 83 ("Figure 2 shows that the anchor via pattern covers the entire surface

of the conducting layer 20, such that some anchor vias are disposed at the corners of the conducting layer 20.”); Ex. 2009, 35:14-37:7. Thus Petitioner’s counsel drew four corners onto Fig. 2.



Reply, 16.

But if that were true, and if, as Petitioner suggests, one applies the 60 micrometer distance between vias to the Figure, it would result in a wafer roughly 300 micrometers wide and 240 micrometers high, far smaller than any existing semiconductor wafer, and orders of magnitude smaller than 140 mm by 80 mm size in *Conn*’s embodiment. See Ex. 1004, [0036].

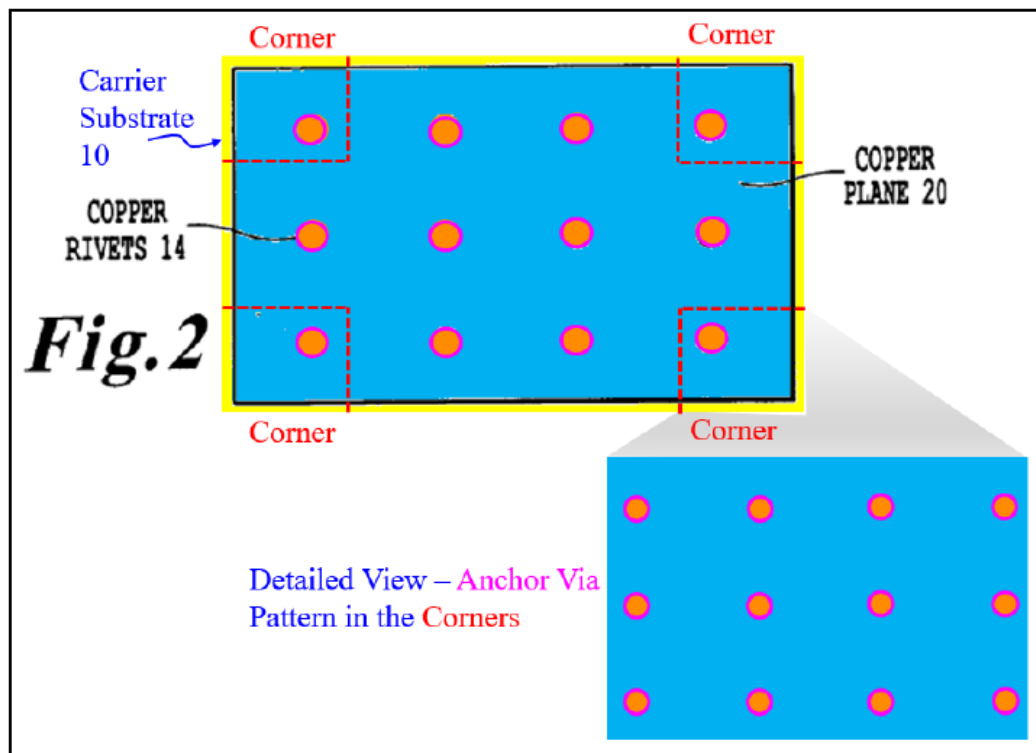
Thus Petitioner's use of *Conn*'s Fig. 2 to infer that *Conn*'s vias are in the corner should be given no weight. Even if the Board considers it, it cannot show that *Conn*'s vias must be in the corner as required.

Accordingly, *Conn* does not anticipate any claims. *Rexnord Indus., LLC v. Kappos*, 705 F.3d 1347, 1355 (Fed. Cir. 2013) (“We agree with the Board that the precise less-than-10 mm size limitation is not inherent in *Palmaer* or *Thompson*, for neither reference shows this limitation and that it would necessarily be recognized.”).

B. *Conn* Does an Anchor Via Disposed in at Least One Corner Under the Proper Construction

Petitioner apparently agrees that it did not show an anchor via disposed in the corner under the proper construction, as it relies on Dr. Thompson's opinion as to dependent Claim 2. Reply, 18-19 (citing Ex. 1003, ¶ 94).

But the Petition does not discuss that opinion other than to cite it. *See* Pet., 39. Instead, the Petition (and Reply) merely claim that *Conn* Fig. 2 itself includes numerous *copies* of Fig. 2.



Reply, 19 (quoting Pet., 39).

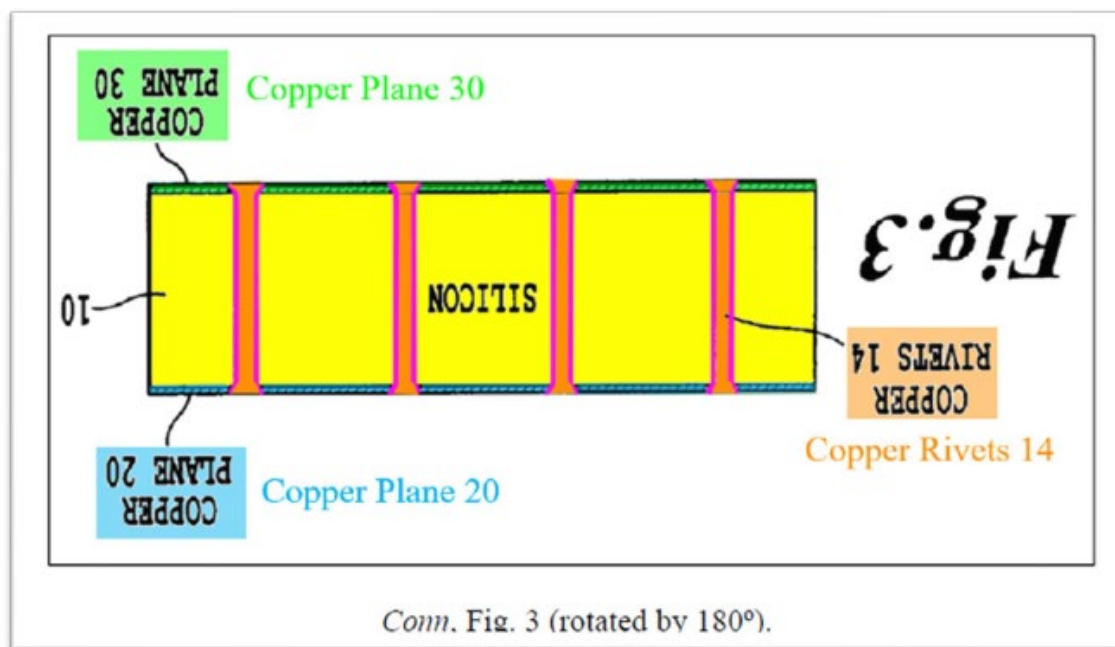
Petitioner's argument demonstrates the problems with its imputation of dimensions to Fig. 2. Is the supposed 60 micrometer distance to the corner in the upper left hand Figure? Or is it in the lower right hand Figure? Or perhaps an even further distilled copy of Fig. 2? Petitioner does not say, but merely assumes that the vias are in the corner.

Accordingly, *Conn* does not anticipate under the proper construction.

C. *Conn* does not anticipate Claims 9 and 19

As discussed in the POR, Claim 9 requires anchor vias "wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said

semiconductor substrate.”⁵ Petitioner relies on *Conn*’s Fig. 3, which shows two copper conducting layers connected by fully filled vias. As explained in the POR, a POSITA would understand that the copper plane on at least one side would contain active devices, and those devices would be connected to ground by the vias. POR, 38-42.



Pet. 43.

Petitioner does not dispute that active devices would be on one of the copper plane conducting layers or that the vias are capable of conducting electricity. Petitioner instead argues that the vias might not be used to ground devices.

⁵ Claim 19’s requirement is similar and the same analysis applies.

Petitioner first argues that other prior art shows fully-extended through-vias “used for nonelectrical functions.” Reply, 21. That is irrelevant to this anticipation ground.

Petitioner next attempts to rely on *Conn*’s lack of disclosure to rescue this ground. Reply, 23 (“[T]he anchor vias in the embodiment in Figure 3 would only be capable of providing ground connection to active devices if the metal layers were patterned to do so, and *Conn* does not disclose such patterning or otherwise suggest the anchor vias provide electrical connection in Figure 3.”). Indeed, *Conn* does not disclose patterning its conducting layers; those layers are only disclosed as having square or rectangular shapes, and thus would connect to the active devices. Ex. 1004, [0039], Fig. 2.

Conn’s lack of disclosure cannot serve to disclose this limitation. It is beyond dispute that a POSITA would know that a via, explicitly disclosed as being filled with a “conductor,”⁶ would conduct electricity between two copper planes; that is the normal function of vias. In the absence of any contrary disclosure (which Petitioner admits there is not), a POSITA would reasonably believe that the vias would conduct electricity. Indeed, *Conn* discloses embodiments where vias conduct electricity between layers and devices. *E.g.*, Ex. 1004 [0047].

⁶ *E.g.*, Ex. 1004, [0033].

The POR explained the legal framework for disclosing negative limitations in detail. POR, 41-42. Petitioner's Reply does not attempt to distinguish those cases, but responds with a bare citation to *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1367 (Fed. Cir. 2019). Reply, 23. That case, however, only found substantial evidence that the particular limitation at issue ("independently of an access of the computer unit") could be disclosed when the prior art did not discuss accessing the computer. *Id.*

The limitation and circumstances here are vastly different. To find that *Conn* discloses Claim 9, one would have to find that a POSITA would read *Conn*, note that some vias do not ground because they are not filled,⁷ and, for an unidentified reason, determine that the filled vias in Fig. 3 also would not ground devices because of an entirely undisclosed patterning of the conductive layers. It would also have to do so entirely absent any evidence or argument regarding the Claim 9 vias in the Petition.

The Board should decline to find that a POSITA would make so many unsupported inferential leaps. A POSITA would simply conclude that the vias in

⁷ The partial filling is the **only** evidence Petitioner provides to show that **any** of *Conn*'s vias might not ground a device. POR, 39-41; Pet., 37.

Fig. 3, like other vias in *Conn* and in the art, would provide ground connection for active devices.

Accordingly, *Conn* does not anticipate Claims 9 or 19.

IV. GROUND 2

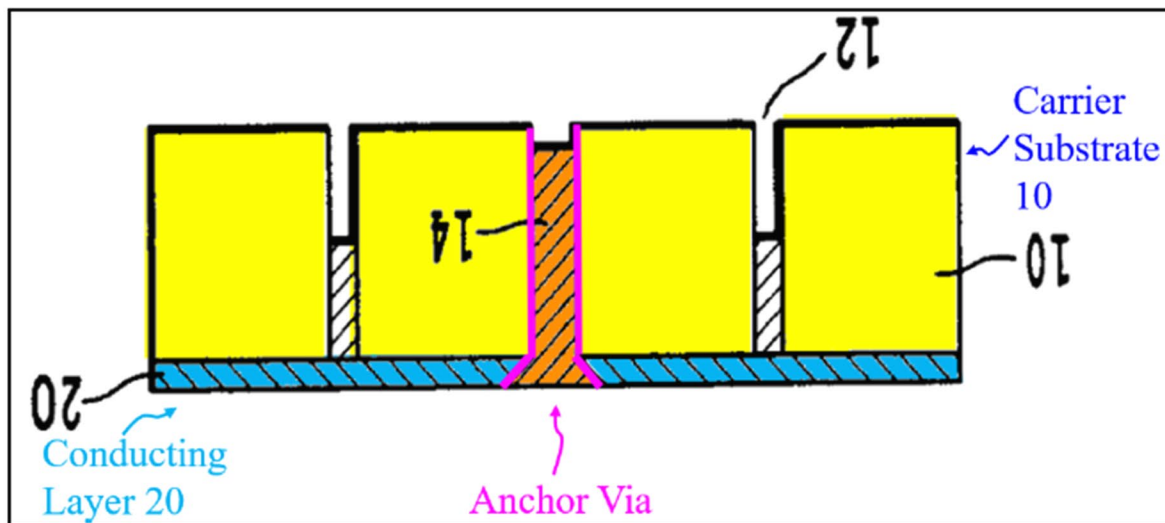
The Petition expressly used Ground 2A for the limited purpose of filling in *Conn*'s lack of disclosure as to "backside" or "active devices." Pet., 45 ("to the extent that HID may (erroneously) argue that *Conn* does not expressly disclose "backside" or "active devices," they would have been obvious based on *Conn* and a POSA's knowledge"); POR, 43-44.

Despite this clear statement, and Dr. Thompson's many admissions affirming the limited scope of Ground 2A,⁸ Petitioner now contends that Ground 2 renders Claims 9 and 19 obvious because a POSITA would modify *Conn* to use *Wang*'s structure where dummy TSVs do not provide a ground connection. Reply, 23. Substituting *Wang*'s dummy TSVs—extending fully through the substrate to another

⁸ Ex. 2009, 51:22-52:5 ("Q. Right, and with respect to claim 1, that's your use of knowledge of a POSITA. Just to make sure I understand the borders of this. A. For claim 1 I'm using knowledge of a POSITA with support from Wang to show that *backside metal and active devices would be obvious elements to modify Conn with.*" (emphasis added); see also *id.* 48:7-15; 50:4-13; 50:25-12; 51:13-21).

metal layer—for *Conn*’s vias is a new argument and modification not disclosed in the Petition. Pet., 47-48.

Indeed, it is the opposite. The Petitioner argued that “*Conn*’s electronic package structure is suitable for use in *Wang* to mount LED chip 44.” Pet., 47; *see also* Ex. 1003, ¶ 113 (“In my opinion, a POSA would have been motivated to use *Conn*’s electronic package structure for packing *Wang*’s LED chip.”). In the proposed modification, *Conn*’s anchor vias are used to perform in place of Wang’s dummy TSVs. Pet., 47 (“*Conn*’s anchor vias can substitute *Wang*’s dummy TSVs 64 to achieve the dual purpose of improving *Wang*’s heat dissipation and metal layer adhesion.”). Indeed, Petitioner uses an annotated *Conn* Fig. 1 to demonstrate its modification. The colors used to connect the Figure to the text make it clear:



Conn, Fig. 1 (rotated by 180°).

In the *Conn-Wang* use case, *Conn*'s conducting layer is disposed on a side of the carrier substrate opposite to the LED chip—active device, thereby constituting a backside metal layer. *Supra*, §II.B; Thompson, ¶114. And, the via conductors in *Conn*'s anchor vias do not provide ground connection to the LED chip, because they are dummy vias designed for dissipating heat and securing backside metal, but not for providing electrical connection. *Conn*, [0011]; *Wang*, 3:23-27; *supra*,

Pet. 48.

Accordingly, Ground 2 does not render any claims obvious.

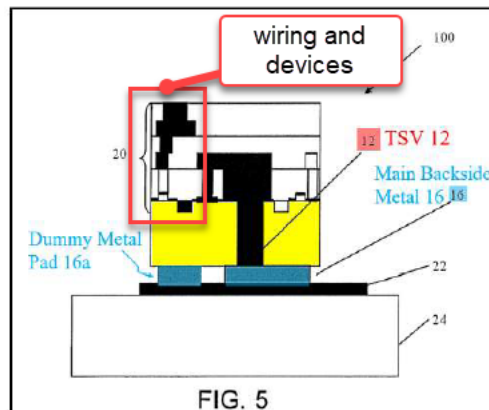
V. GROUND 3

A. *Gambino*-Based Obviousness

1. *Gambino-Conn* Vias Would Provide Ground Connections

The POR explains that *Gambino*'s process, which Petitioner explicitly adopted for its combination, forms vias starting from the front (active) side and then fills them entirely with a conductor. POR, 45-54; *see also* Pet., 64 (“the same process used for manufacturing *Gambino*'s electrical TSVs can be used to manufacture the anchor vias”); Ex. 1004, [0020]. This process can only result in either filled vias or vias that do not reach the backside. *Id.*

In Reply, Petitioner now contends that there would simply be no wiring layer over the dummy metal pads. Reply, 24. But *Gambino* itself shows both devices and wiring layers directly above the dummy metal pads. Ex. 1005, FIG. 5, [0030]. *Gambino* does not disclose manipulating the wiring layers to avoid contact with an “anchor via.”



Reply, 25 (further annotation added).

Petitioner provides no reason, either in the Petition or Reply, as to why a POSITA would alter *Gambino*'s express disclosure to move the wiring and devices away from the dummy metal pads. Indeed, the only "reason" behind doing so is a hindsight-based motivation to meet the claims.

Petitioner next argues that a POSITA would make a further alteration (not disclosed in the Petition)⁹ to *Gambino* by either "patterning the wiring layer or recess etching the metal filler from the front side." Reply, 26 (citation omitted). Despite Petitioner's statement otherwise, *Gambino* does not disclose either. Ex. 1005 [0015] discusses patterning the backside metal, not the frontside wiring layer. *Id.*, ("[T]he backside metal is patterned to form patches and/or islands of metal which are all coupled to the same potential (e.g., ground).") *Gambino*, [0026] similarly describes a subtractive etching process used to pattern the backside metal. *Id.*, [0026]. Neither citation describes etching away metal filler or the wiring layer.

⁹ Petitioner acknowledges that this alteration is not in the Petition by providing a new motivation to make it. Reply, 26 ("A POSITA would have found it desirable to prevent the metal filler from providing ground connection to active devices because . . . providing the ground connection would unfavorably disturb and require redesign of *Gambino*'s existing active device circuitry").

Moreover, if this new modification were implemented, *Gambino-Conn* could not render Claims 9 and 19 obvious as the anchor vias would necessarily not be bonded to a metal layer overlying the substrate.

Finally, Petitioner states that *Gambino-Conn* anchor vias would reach the backside metal. Reply, 26-27. As explained in the POR, *Gambino*'s process allows for fully-filled vias to reach the backside metal, but does not provide a mechanism to create partially-filled vias where the metal contacts the backside while not reaching the frontside. POR, 46-48. Petitioner does not contend otherwise.

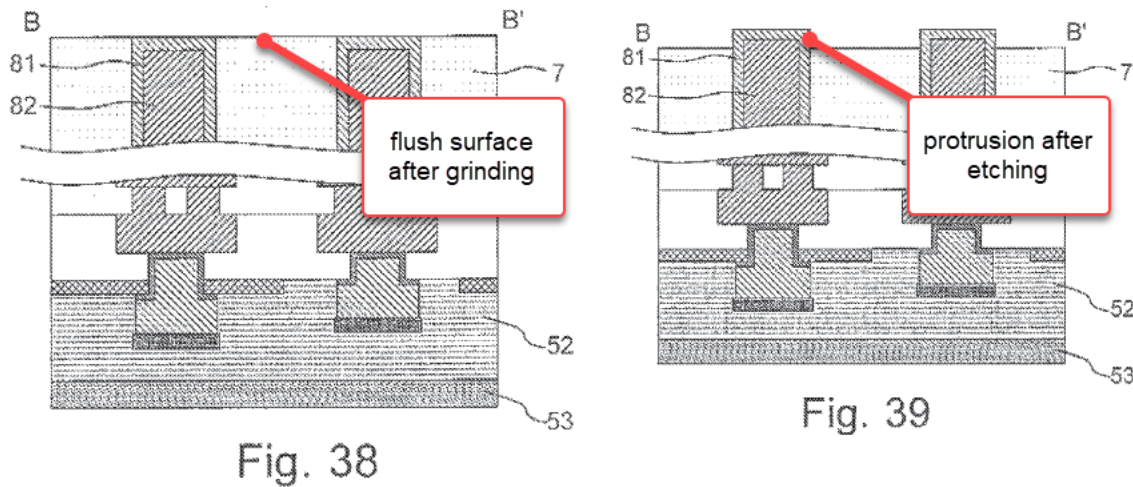
2. *Gambino-Conn* Does Not Disclose a Protruding Portion

As explained in the POR, *Gambino*'s process polishes or grinds the backside until the via is exposed, resulting in the conductors being flush with the surface of the substrate and not protruding. POR, 50; Ex. 1005, [0020] ("The backside of the substrate **5** then undergoes a thinning process, e.g., a polishing and grinding process, in order *to expose the TSVs 12.*" (emphasis added)). Petitioner does not dispute that *Gambino*'s process functions as described. See Reply, 26.

Instead, Petitioner argues that a POSITA would alter the described process similarly to *Torii* to create a protruding portion. *Id.* But *Torii*'s backside grinding process results in a flush surface; further etching creates the protruding portion. Ex. 1009, [0099], Figs. 37, 38. As *Torii* explains:

This substrate is backside-ground by mechanical grinding until the last minute whether to expose the bottom of insulating film 81. **FIG. 38 shows a state that the backside grinding was stopped at the point of just exposing the bottom of insulating film 81. Then, the substrate is etched by silicon etch-back up to a region in which the bottom of conductive film 82 slightly protrudes** from the rear surface of the substrate, as illustrated in FIG. 39.

Id., [0099] (emphasis added).



Id., Figs. 38, 39.

The Petition did not contend that it would be obvious to add another step to *Gambino*'s grinding process. Pet., 63 (“*Gambino* is ready for improvement because it already uses electrical TSVs and employs a TSV manufacturing process. *Gambino*, [0020]; Thompson, ¶139. **The anchor vias could be made using the same process.** Thompson, ¶139.” (emphasis added)), 67-68. The Board should decline to consider this new argument.

B. *Ding*

As the POR explained, adding *Ding* does not remedy the *Gambino-Conn* deficiencies. POR, 55. Petitioner implies that *Ding* somehow would modify the above description of *Gambino-Conn*. Reply, 24 n.5. But the Petition explicitly states that “the proposed combination does not require any change to *Gambino/Conn*’s existing way of forming the TSVs/anchor-vias and backside metal. Rather, it only requires adding an additional step of depositing the dielectric film, before the metal filler is deposited into the vias.” Pet., 78. Thus, the combination including *Ding* would not render any claims obvious. POR, 55.

VI. GROUND 4

A. *Torii*’s Sub-TSVs Provide Ground Connection

The Board properly found in its Institution Decision that *Torii* does not anticipate any claims because, as *Torii* explains, “The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway.” POR, 55-56.

Petitioner’s Reply argument is that the word “but” renders this unambiguous statement an “alternative embodiment.” Reply, 27-28. The Petition contains no mentions of this as an alternative embodiment; there, Petitioner chose to deceptively elide away the “subsidiary current pathway” portion of the relevant sentence. Pet.,

86. The Board should disregard this gamesmanship and change in Petitioner's theory.

Even if the Board were to consider the argument, it fails on its face. *Torii* discloses multiple embodiments and clearly describes them as such. *E.g.*, Ex. 1009, [0050]-[0072] (“Exemplary Embodiment 1”); [0073-0078] (“Exemplary Embodiment 2”); [0079]-[0081] (“Exemplary Embodiment 3”); [0082-0092] (“Exemplary Embodiment 4”); [0093-0101] (“Exemplary Embodiment 5”). In contrast, the relevant section on sub-TSVs is not limited to any embodiment. *Id.*, [0048]. Moreover, Petitioner does not point to any Figure or description showing a sub-TSV that does not carry current. In contrast, the Figures show sub-TSVs wired similarly to main TSVs.

Accordingly, *Torii* does not anticipate any claims.

B. *Torii* Does Not Disclose a “backside metal layer on a bottom surface...”

As explained above and in the POR, the claims of the '826 Patent require contact between the backside metal layer and bottom surface of the substrate. Samsung admits that *Torii* does not anticipate any claims under Patent Owner's construction of “backside metal layer on a bottom surface” Reply, 29.

VII. IDE

As with *Torii*, Petitioner admits that *Ide* does not anticipate under Patent Owner's construction of “backside metal layer on a bottom surface” Reply, 30.

VIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board issue a Final Written Decision finding no claims unpatentable.

Respectfully submitted,

Dated: October 2, 2025

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CERTIFICATE OF WORD COUNT

The undersigned hereby certifies that the portions of the above-captioned PATENT OWNER'S SUR-REPLY specified in 37 C.F.R. § 42.24 has 4,340 words in compliance with the 5,600 word limit set forth in 37 C.F.R. § 42.24. This word count was prepared using Microsoft Word for Office 365.

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