

Before The Patent Trial And Appeal Board
Oral Hearing
January 6, 2026

Harbor Island's Presentation

IPR2024-01405: U.S. 9,245,826

U.S. Patent No. 9,245,826


US009245826B2

(12) **United States Patent**
Jebory et al.

(10) **Patent No.:** **US 9,245,826 B2**
(45) **Date of Patent:** **Jan. 26, 2016**

(54) **ANCHOR VIAS FOR IMPROVED BACKSIDE METAL ADDITION TO SEMICONDUCTOR SUBSTRATE**

(71) Applicant: **Newport Fab, LLC**, Newport Beach, CA (US)

(72) Inventors: **Hadi Jebory**, Irvine, CA (US); **David J. Howard**, Irvine, CA (US); **Scott B. Stetten**, Huntington Beach, CA (US)

(73) Assignee: **Newport Fab, LLC**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/165,377**
(22) Filed: **Jan. 27, 2014**

(65) **Prior Publication Data**
US 2014/0252651 A1 Sep. 11, 2014

Related U.S. Application Data
(66) Provisional application No. 61/776,063, filed on Mar. 11, 2013.

(51) **Int. Cl.** (2006.01)
H01L 21/08 (2006.01)
H01L 21/00 (2006.01)

(52) **U.S. Cl.** (2013.01)
CPC: **H01L 22/04** (2013.01); **H01L 21/562** (2013.01); **H01L 25/04** (2013.01)

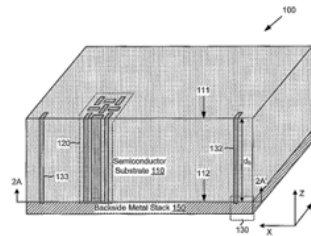
(58) **Field of Classification Search**
USPC: 257/774, 621, 121, 597, 438/629, 630, 438/637, 640, 668, 672, 675
See application file for complete search history.

(56) **References Cited**
U.S. PATENT DOCUMENTS
8,431,481 B2 * 4/2013 Dasse et al. 438/629
8,710,629 B2 * 4/2014 Ito et al. 257/618
* cited by examiner

Primary Examiner — Jasmine Clark
(74) Attorney, Agent, or Firm — Farjani & Farjani LLP

(57) **ABSTRACT**
Disclosed is a structure having anchor via for improved backside metal adhesion and an associated method for the structure's fabrication. The structure includes at least one anchor via disposed in at least one corner of a semiconductor substrate. A metal filler may be formed within the at least one anchor via, the metal filler having a protruding portion extending from a backside of the semiconductor substrate. The structure may further include a backside metal layer on a bottom surface of the semiconductor substrate, the backside metal layer being bonded to the protruding portion of the metal filler in the at least one anchor via. The at least one anchor via may include a cluster of anchor vias, a plurality of anchor vias disposed in a straight line and/or in a staggered configuration along a periphery of the semiconductor substrate.

20 Claims, 5 Drawing Sheets



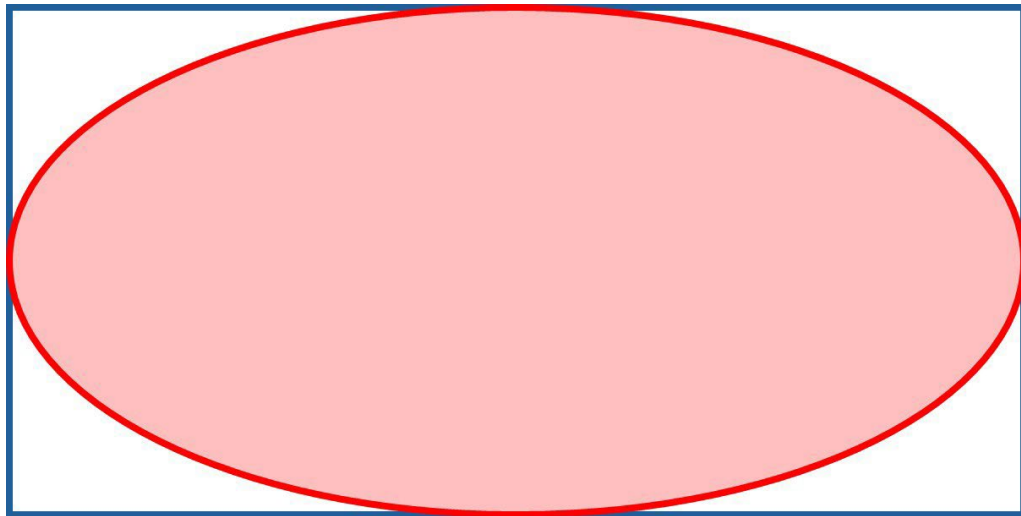
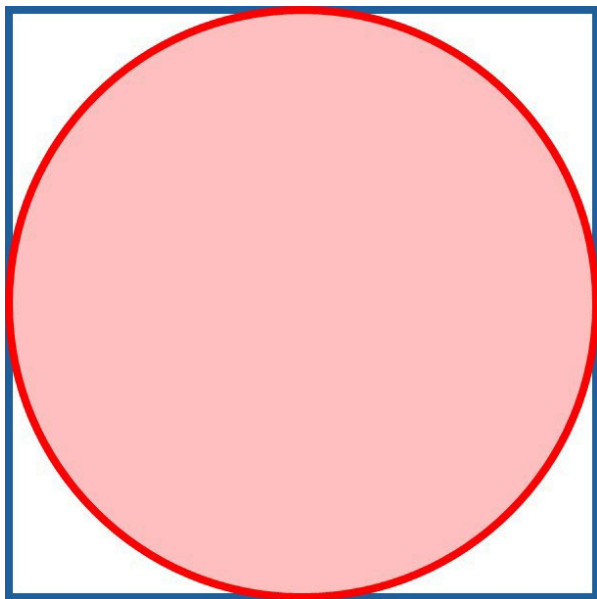
Claim Construction

Terms

Term	Patent Owner	Petition
“disposed in at least one corner of a semiconductor substrate”	“located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”	<u>District Court</u> : Indefinite <u>This Proceeding</u> : no construction necessary
“a backside metal layer on a bottom surface of said semiconductor substrate”	“a backside metal layer in contact with a bottom surface of said semiconductor substrate”	No construction necessary

“disposed in at least one corner of a semiconductor substrate”

“located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”

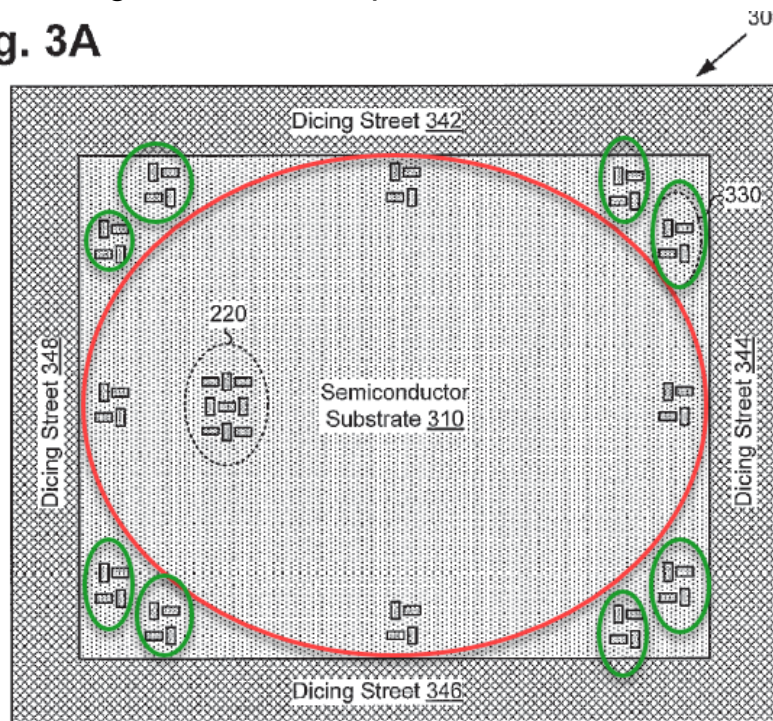


POR, 18-25

“disposed in at least one corner of a semiconductor substrate”

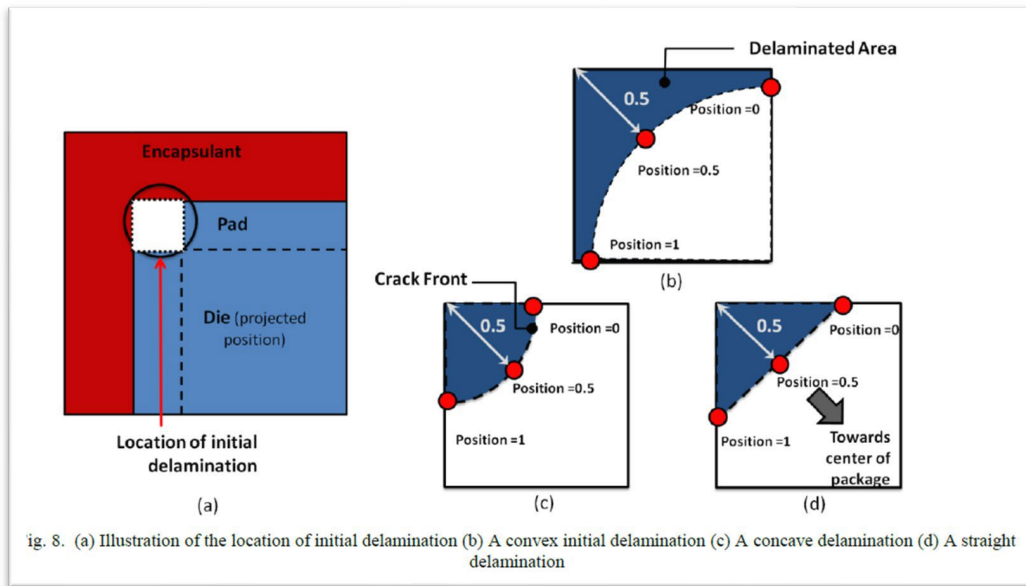
“located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”

Fig. 3A



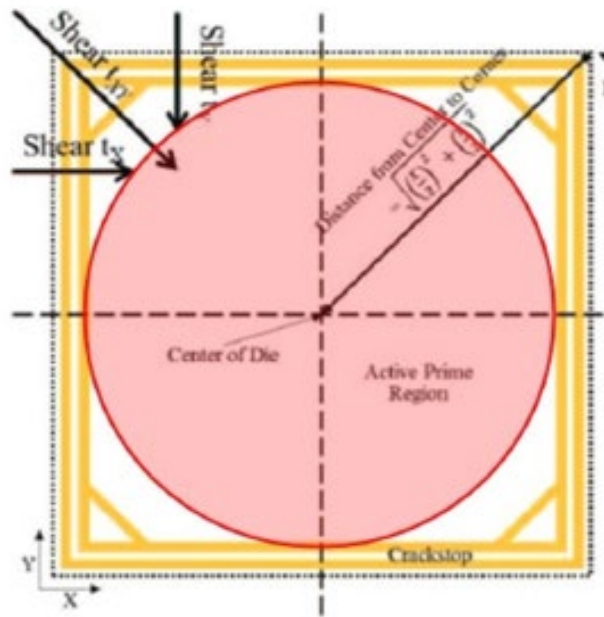
POR, 18-25
Surreply, 2

“disposed in at least one corner of a semiconductor substrate”



POR, 21-22
Ex. 2007

“disposed in at least one corner of a semiconductor substrate”



POR, 24
Ex. 2008

“a backside metal layer on a bottom surface of said semiconductor substrate”

“a backside metal layer *in contact with* a bottom surface of said semiconductor substrate”

1. A structure comprising:
at least one anchor via disposed in at least one corner of a semiconductor substrate;
a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;
wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

Ex. 1001, 7:58-8:3

9. The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

Ex. 1001, 8:27-30

POR, 26

“a backside metal layer on a bottom surface of said semiconductor substrate”

“a backside metal layer *in contact with* a bottom surface of said semiconductor substrate”

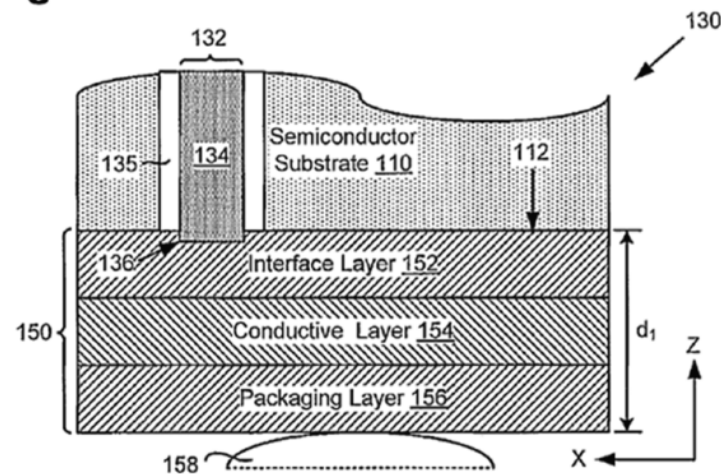
One conventional method of adhering a backside metal layer to a substrate relies on forming a backside metal stack having several layers, the first of which must form an adhesive bond with the substrate. For example, an interface layer may be deposited on a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer. However, fabrication procedures such as semi-

* * *

cially near the edges and/or corners of the die. Because adhesion of the backside metal stack to the substrate is almost entirely dependent on the adhesive qualities between the substrate and the interface layer, unacceptably low yields are often achieved during fabrication due to the backside metal layer peeling from the semiconductor substrate.

Ex. 1001, 1:24-39

Fig. 1B

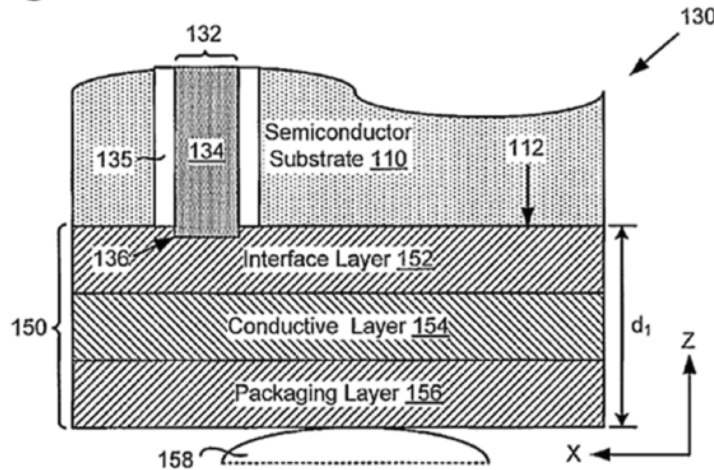


Ex. 1001, Fig. 1

“a backside metal layer on a bottom surface of said semiconductor substrate”

“a backside metal layer *in contact with* a bottom surface of said semiconductor substrate”

Fig. 1B

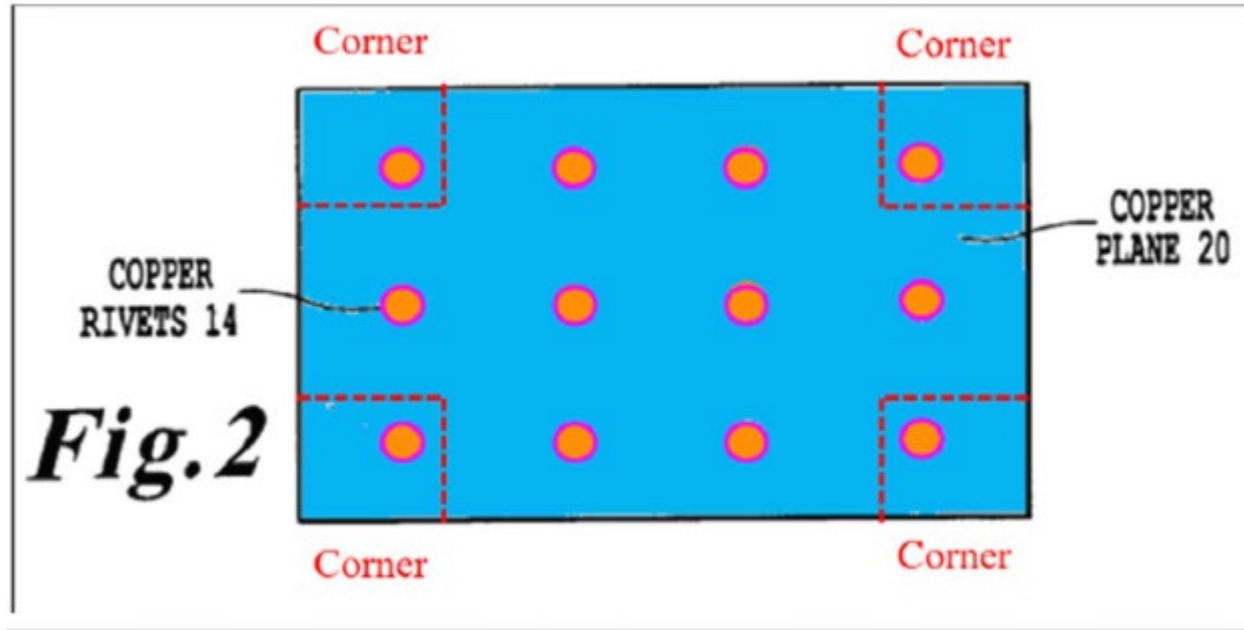


Ex. 1001, Fig. 1

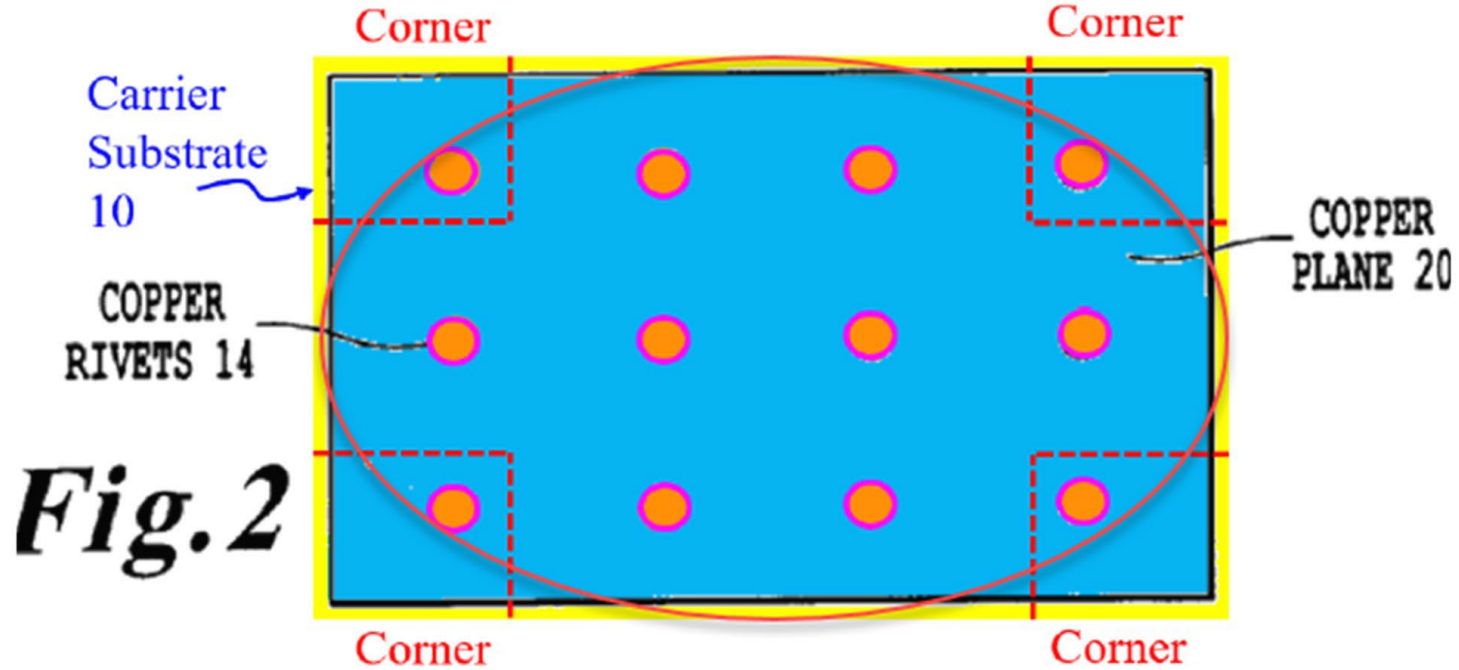
layer 135 may be a dielectric layer such as silicon dioxide, for example. As shown in FIG. 1B, metal filler 134 may protrude from bottom side 112 to form protruding portion 136 such that when interface layer 152 is deposited on bottom side 112 of semiconductor substrate 110 the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond. Metal filler 134 may be tungsten, titanium, or any other suitable metal filler. Interface layer 152 may be formed from metals such as titanium or chrome-vanadium. Conduction layer 154 may then be formed on interface layer 152 using metals such as nickel or copper. Packaging layer 156 may then be formed on conduction layer 154 using metals such as gold or silver to provide a very low resistance contact surface. Packaging layer 156 may subsequently be connected to, one or more contacts, such as contact 158 for example, which may be a solder bump on a semicon-

Ex. 1001, Fig. 1

Ground 1: Conn



Ground 1: Conn



Ground 1: Conn as to claim 9

1. A structure comprising:

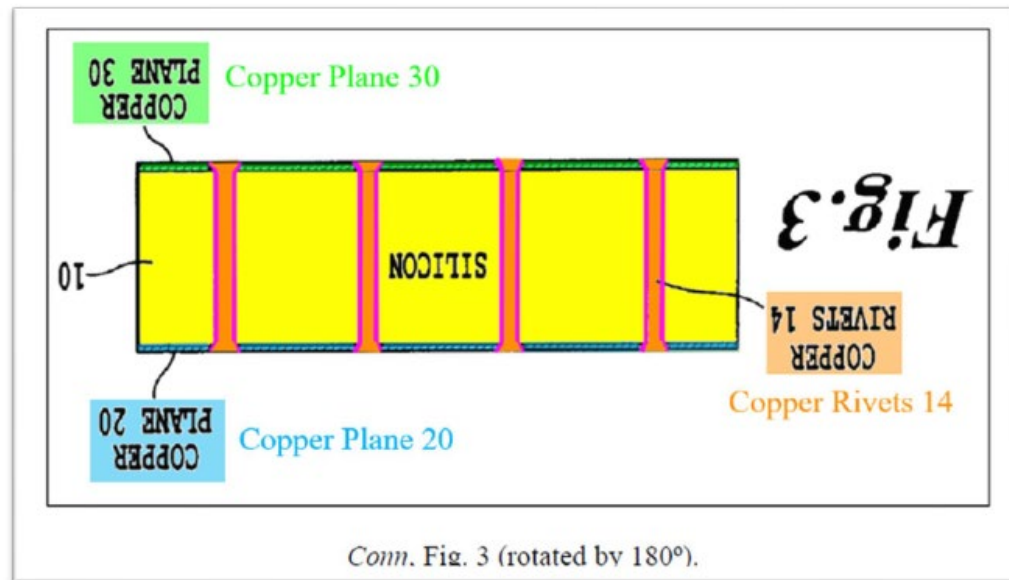
at least one anchor via disposed in at least one corner of a semiconductor substrate;

a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

9. The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

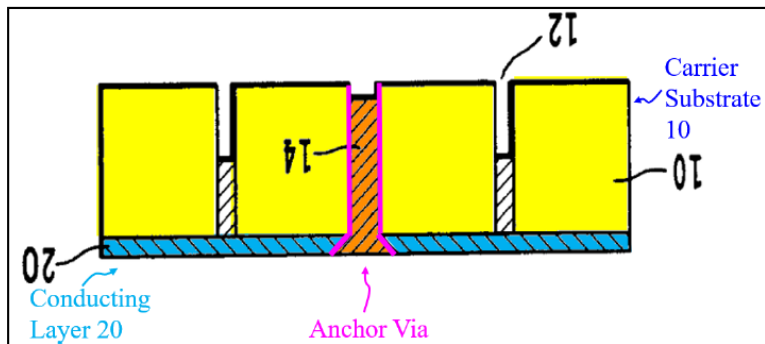


Ground 1: Conn as to claim 9

Claim 1

substrate 10.” *Conn*, [0028]. Separately, *Conn* discloses “via conductor[s] 14 do[] not necessarily have to go all the way through” the anchor vias. *Id.* This means the

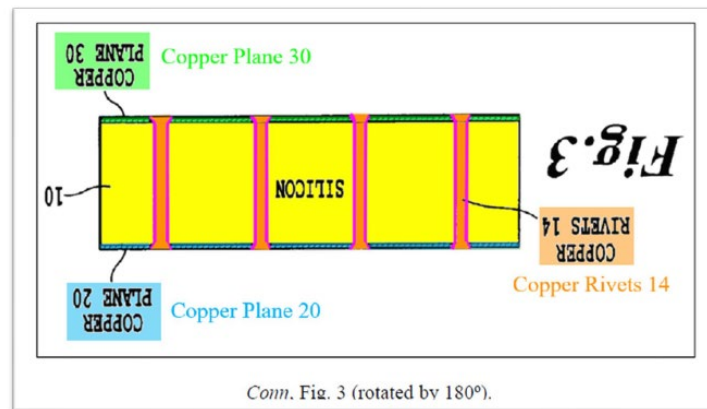
anchor vias and via conductors 14 are *not* designed for providing electrical connection (including ground connection) to any active device on that side.



Pet., 37-38

Claim 9

Conn discloses “another conducting layer 30 is formed on the second main surface of the carrier substrate 10, as shown in FIG. 3.” *Conn*, [0037]. Like conducting layer 20, conducting layer 30 is similarly bonded to the anchor vias. *Conn*, [0038], [0040]-[0041]. Thus, conducting layer 30 constitutes the claimed overlying “metal layer.” Thompson, ¶100.

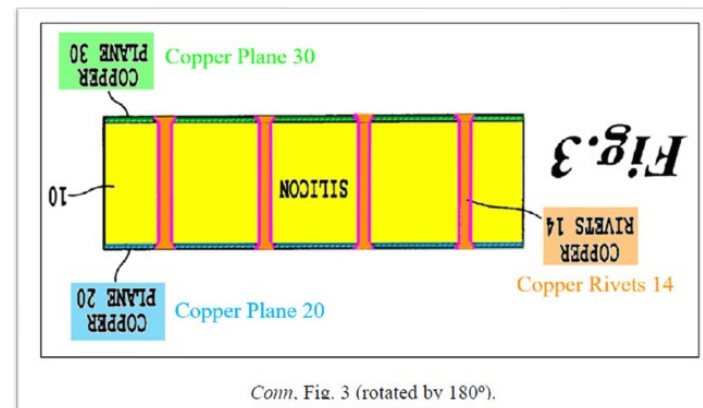


Conn. Fig. 3 (rotated by 180°).

Ground 1: Conn as to claim 9

Claim 9

Conn discloses “another **conducting layer 30** is formed on the second main surface of the carrier substrate 10, as shown in FIG. 3.” *Conn*, [0037]. Like **conducting layer 20**, **conducting layer 30** is similarly bonded to the **anchor vias**. *Conn*, [0038], [0040]-[0041]. Thus, **conducting layer 30** constitutes the claimed overlying “**metal layer**.” Thompson, ¶100.



Ex. 2009 (Thompson Dep.) 47:2-15

Ground 2A and 2B

or more active devices in said semiconductor substrate.” Nevertheless, to the extent that HID may (erroneously) argue that *Conn* does not expressly disclose “backside” or “active devices,” they would have been obvious based on *Conn* and a POSA’s knowledge. Thompson, ¶110.

Pet., 45

4 Q. Okay, and so you're using that
5 knowledge of a POSITA to fill in any
6 possible gaps in *Conn* relating to either
7 backside or active devices, is that right?
8 A. Right, I think *Conn* doesn't
9 have these gaps. But to the extent someone
10 would argue a backside metal is missing or
11 active device is missing, a POSITA would
12 know based on their knowledge of integrated
13 circuits they would not be missing.

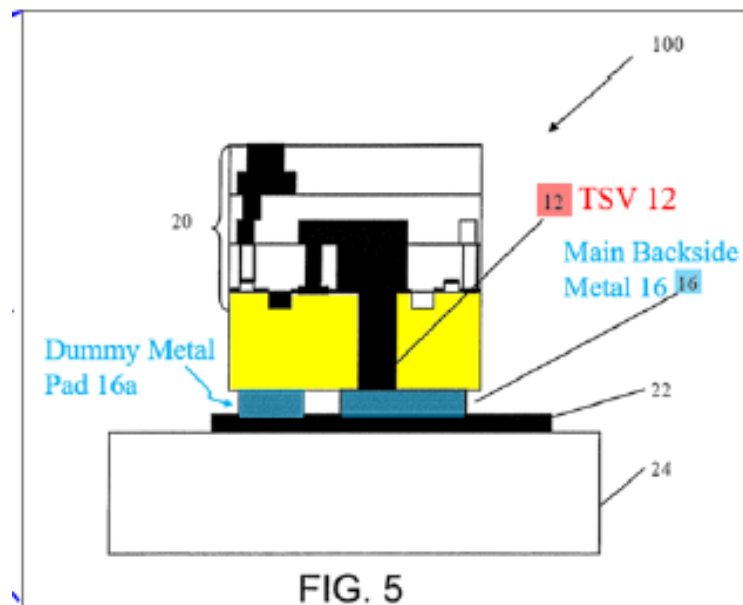
22 | Q. Right, and with respect to
23 claim 1, that's your use of knowledge of a
24 POSITA. Just to make sure I understand the
25 borders of this.
1 A. For claim 1 I'm using knowledge
2 of a POSITA with support from Wang to show
3 that backside metal and active devices
4 would be obvious elements to modify *Conn*
5 with.

Ex. 2009 (Thompson Dep.) 50:14-13

Ex. 2009 (Thompson Dep.) 51:22-52:5

Ground 3A and 3B: *Gambino*

Single Packaged Die (After Dicing)



POR, 45-54

Ground 3A and 3B: *Gambino*

Second, the process of making the proposed combination is predictable

because the same process used for manufacturing *Gambino*'s **electrical TSVs** can be used to manufacture the **anchor vias**. Thompson, ¶142. As illustrated by

Dr. Thompson, *Gambino*'s method can yield the same rivet-like **anchor via** structure contemplated by *Conn*—the resulting **via conductors** will form **protruding portions** bonded to the **backside metal**. *Id.* Thus, the proposed combination does not require modification to *Gambino*'s existing manufacturing method. *Id.*

Pet., 64

POR, 46-47

Ground 3A and 3B: *Gambino*

142. Second, the process of making the proposed combination is predictable because the same process used for manufacturing *Gambino*'s electrical TSVs can be used to manufacture the anchor vias. As discussed in §XII.A.2, *Gambino*'s manufacturing method (*Gambino*, [0020] – depositing the via metal before forming the backside metal) can yield the same rivet-like anchor via structure contemplated by *Conn*—the resulting via conductors will form protruding portions bonded to the backside metal. Thus, the proposed combination does not require modification to *Gambino*'s existing manufacturing method.

Ex. 1003 (Thompson Dec.), ¶ 142

POR, 46-47

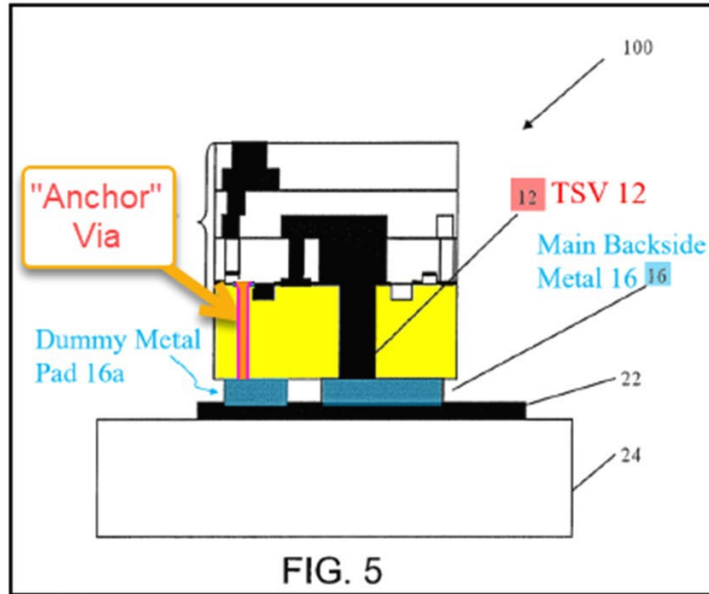
Ground 3A and 3B: *Gambino*

[0020] As one example, Bosch deep reactive ion etching (DRIE) can be used to fabricate the TSVs with almost any diameter, from the submicrometer level to hundreds of micrometers. In more specific embodiments, a via can be formed in a front side of the die 10 using conventional lithography and etching processes. The via would typically extend only partially through the die 10 (or substrate 5). After formation of the via, metal can be deposited therein using conventional deposition processes such as, for example, electroplating or chemical vapor deposition techniques. In embodiments, the metal can be any appropriate metal used in semiconductor manufacturing processes for TSVs such as, for example, copper. The backside of the substrate 5 then undergoes a thinning process, e.g., a polishing and grinding process, in order to expose the TSVs 12.

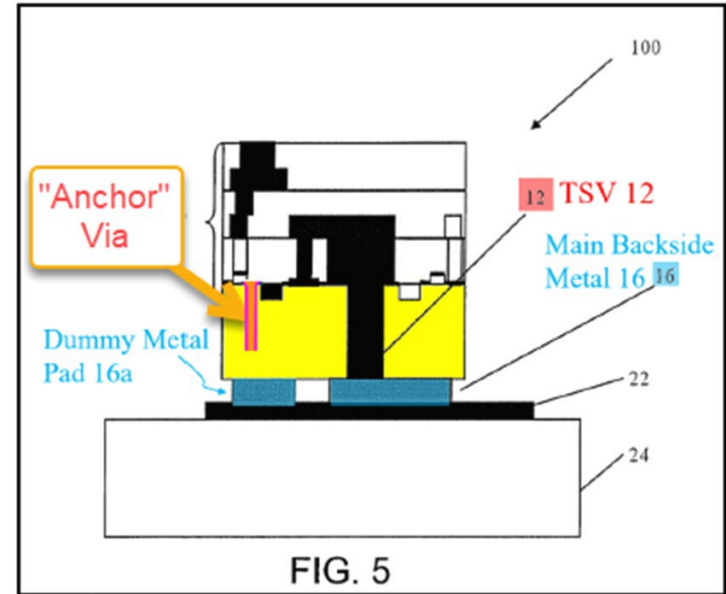
Ex. 1005 (Gambino), ¶ 20

POR, 47-48

Ground 3A and 3B: *Gambino*



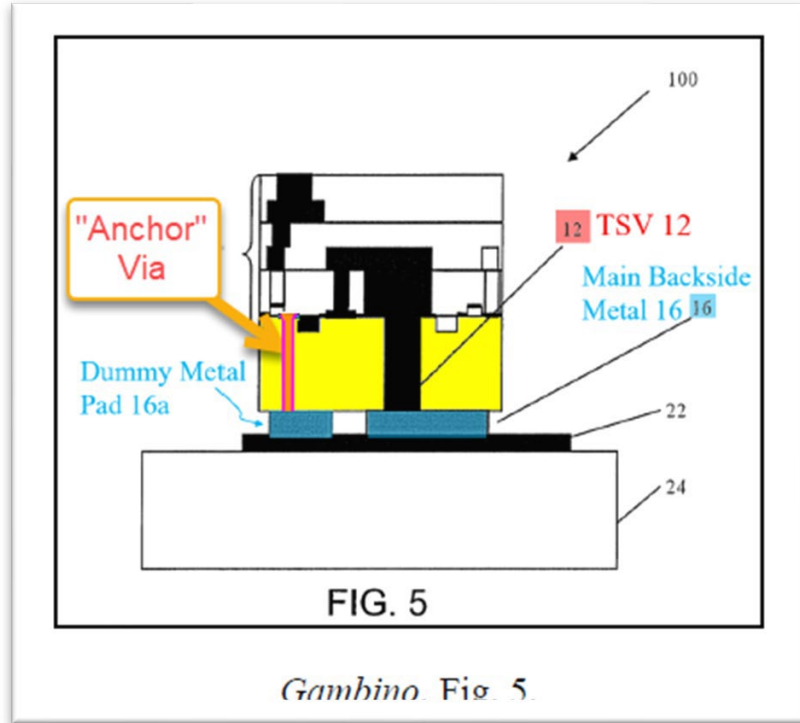
Gambino Fig. 5



Gambino Fig. 5

POR, 49-52

Ground 3A and 3B: *Gambino*

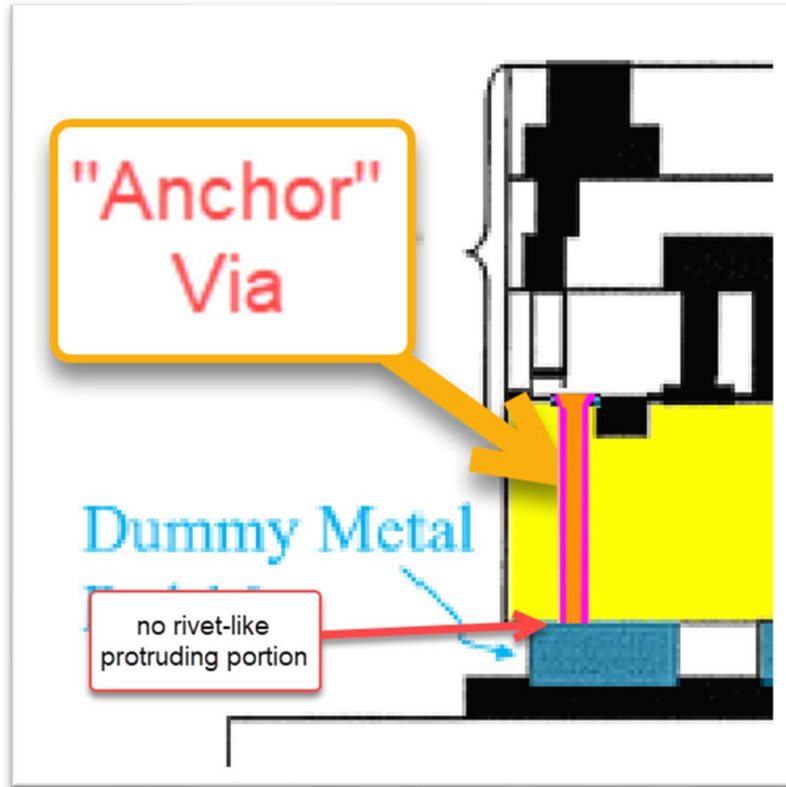


TSV 12 is, in turn, in mechanical and electrical communication with the backside metal 16. In embodiments, the backside metal 16 has a planar surface, which connects to a substrate ground plane 22. The substrate ground plane 22 is bonded to the substrate 24. In embodiments, the construction of the device 100 does not require wirebonding techniques.

Ex. 1005 (Gambino), ¶ 30

POR, 49-50

Ground 3A and 3B: *Gambino*



[0020] As one example, Bosch deep reactive ion etching (DRIE) can be used to fabricate the TSVs with almost any diameter, from the submicrometer level to hundreds of micrometers. In more specific embodiments, a via can be formed in a front side of the die 10 using conventional lithography and etching processes. The via would typically extend only partially through the die 10 (or substrate 5). After formation of the via, metal can be deposited therein using conventional deposition processes such as, for example, electroplating or chemical vapor deposition techniques. In embodiments, the metal can be any appropriate metal used in semiconductor manufacturing processes for TSVs such as, for example, copper. The backside of the substrate 5 then undergoes a thinning process, e.g., a polishing and grinding process, in order to expose the TSVs 12.

Ex. 1005 (Gambino), ¶ 20

POR, 51

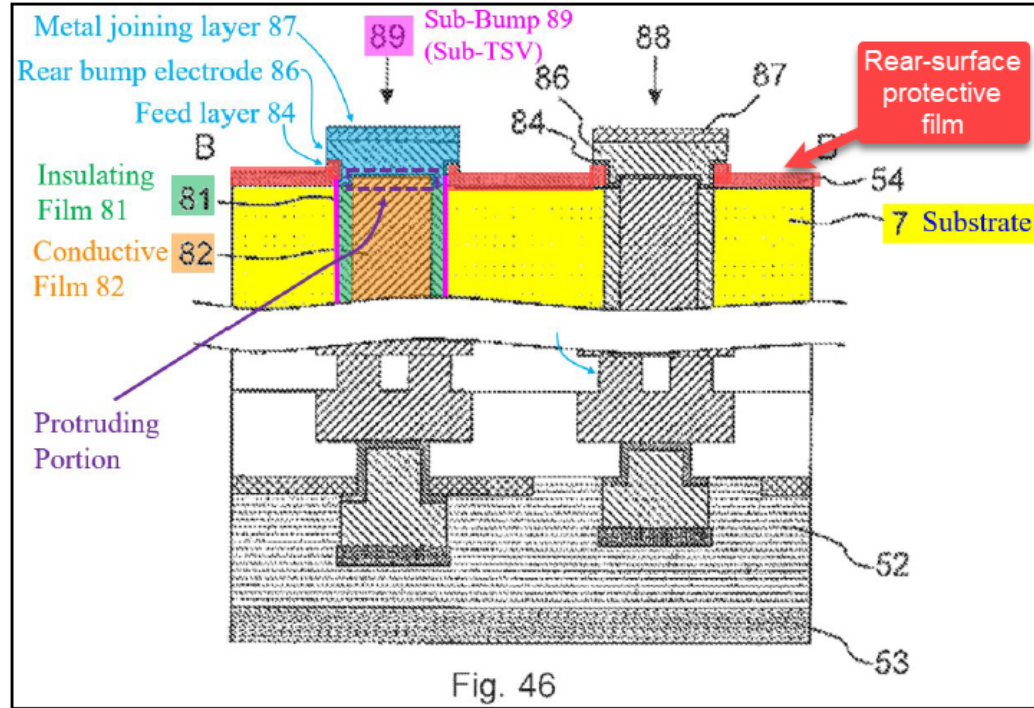
Ground 4: *Torii*

[0048] Note that in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

Ex. 1009 (Torii), [0048]

POR, 55-56

Ground 4: *Torii*



Ground 5: *Ide*

