

Petitioner's Demonstratives

Samsung Electronics Co., Ltd., and Samsung
Electronics America, Inc.,

Petitioner

v.

Harbor Island Dynamic, LLC,

Patent Owner

IPR2024-01405 - Patent No. 9,245,826

Claims of the '826 Patent - Overview

[1pre] “A structure comprising:”

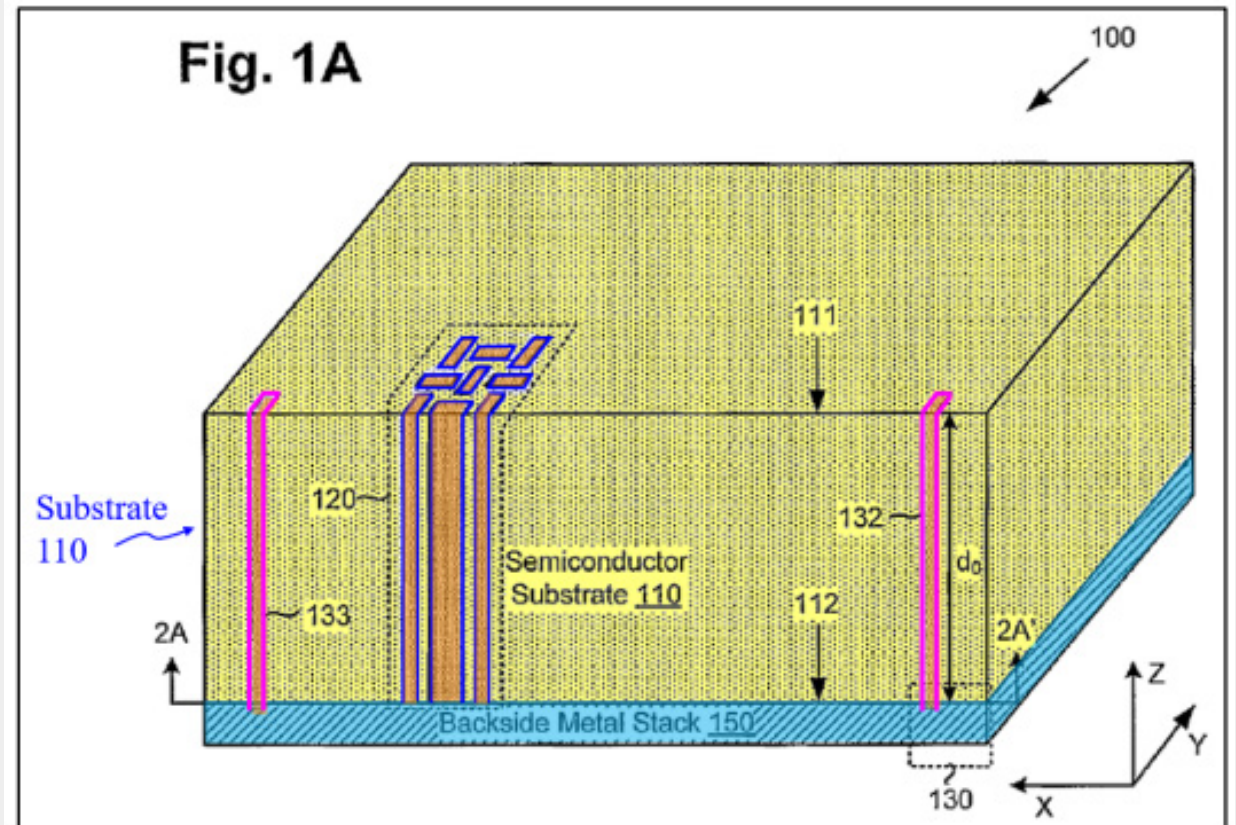
[1a] “at least one **anchor via** disposed in at least one **corner** of a semiconductor substrate;”

[1b] “a **metal filler** within said at least one **anchor via**, said **metal filler** having a **protruding portion** extending from a backside of said semiconductor substrate;”

[1c] “a **backside metal layer** on a bottom surface of said semiconductor substrate, *said backside metal layer being bonded to said protruding portion* of said **metal filler** of said at least one **anchor via**;”

[1d] “wherein said **metal filler** within said at least one **anchor via** *does not provide ground connection to one or more active devices* in said semiconductor substrate.”

(Petition 1.)



(’826 patent, Fig. 1A.)

Claims of the '826 Patent - Overview

- Claims 1-10: device
- Claims 11-20: fabrication method

1. A structure comprising:

at least one anchor via disposed in at least one corner of a semiconductor substrate;

a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

11. A method comprising:

forming at least one anchor via in at least one corner of a semiconductor substrate;

depositing a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

forming a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

('826 patent, 7:58-8:3, 8:34-46.)

Topics

- Instituted Grounds
- Technology Overview
- Ground 1: *Conn* Anticipation
- Ground 2: *Conn* Obviousness
- Ground 3: *Gambino* Obviousness
- Ground 4: *Torii* Anticipation
- Ground 5: *Ide* Anticipation

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Instituted Grounds

- All claims of the '826 patent are challenged based on 5 grounds:

Ground	Claim(s) Challenged	35 U.S.C. § ¹	References/Basis
1	1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	102	Conn ²
2A	1, 2, 4–7, 9, 11, 12, 14–17, 19	103(a)	Conn
2B	8, 18	103(a)	Conn in view of AAPA
3A	1, 2, 4–7, 11, 12, 14–17	103(a)	Gambino ³ in view of Conn
3B	10, 20	103(a)	Gambino in view of Conn and Ding ⁴
4	1, 8–11, 18–20	102	Torii
5	1–3, 9, 11–13, 19	102	Ide

(Institution Decision 6-7.)

Topics

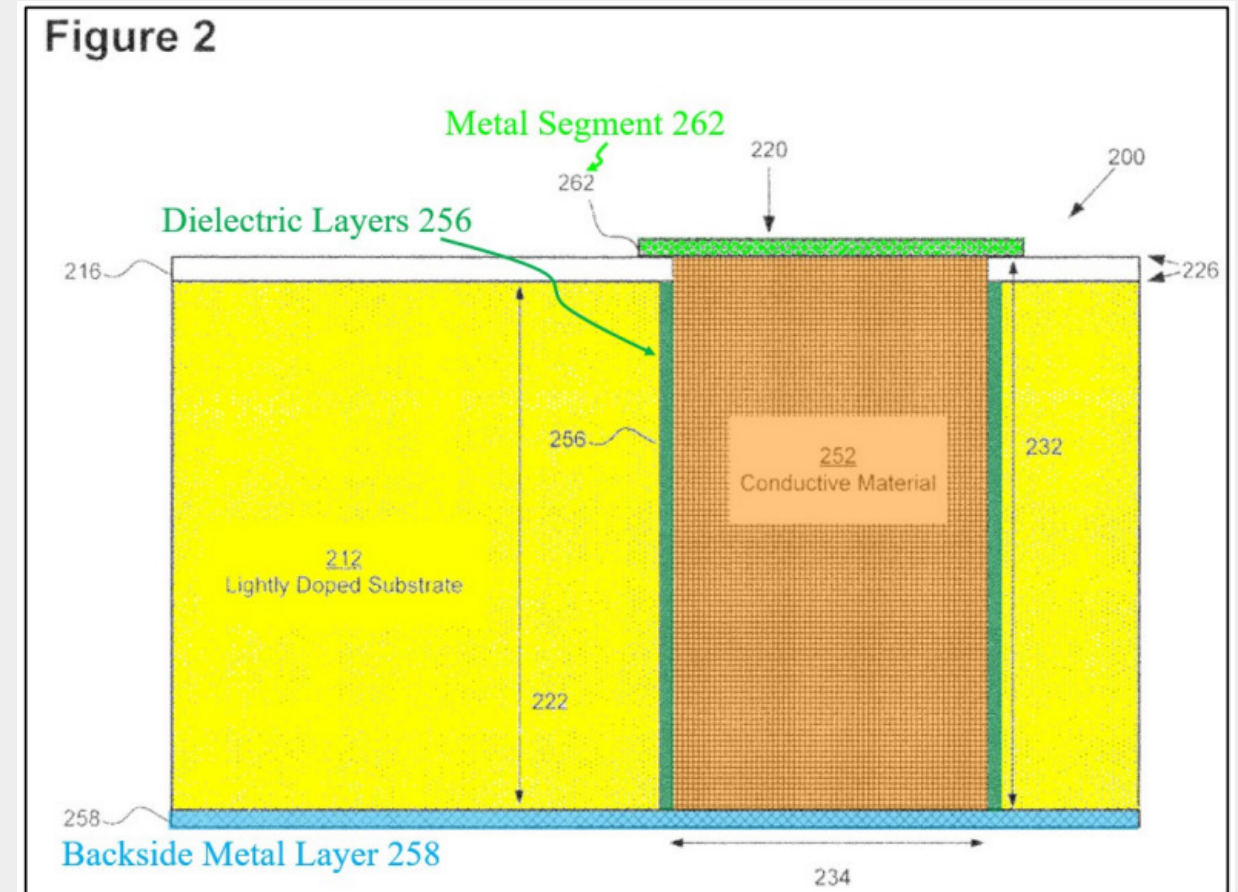
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Vias: Electrical and Non-Electrical

1. Electrical Functions

47. As to the electrical functions, through silicon vias (TSVs), also called through wafer vias (TWVs) in the art, had been used to provide electrical connections along the vertical direction, e.g., connecting devices on the front side of the substrate to the backside metal layer. For example, the following figure

(Thompson Open (Ex. 1003), ¶47.)



Blaschke, Fig. 2.

Non-Electrical Vias

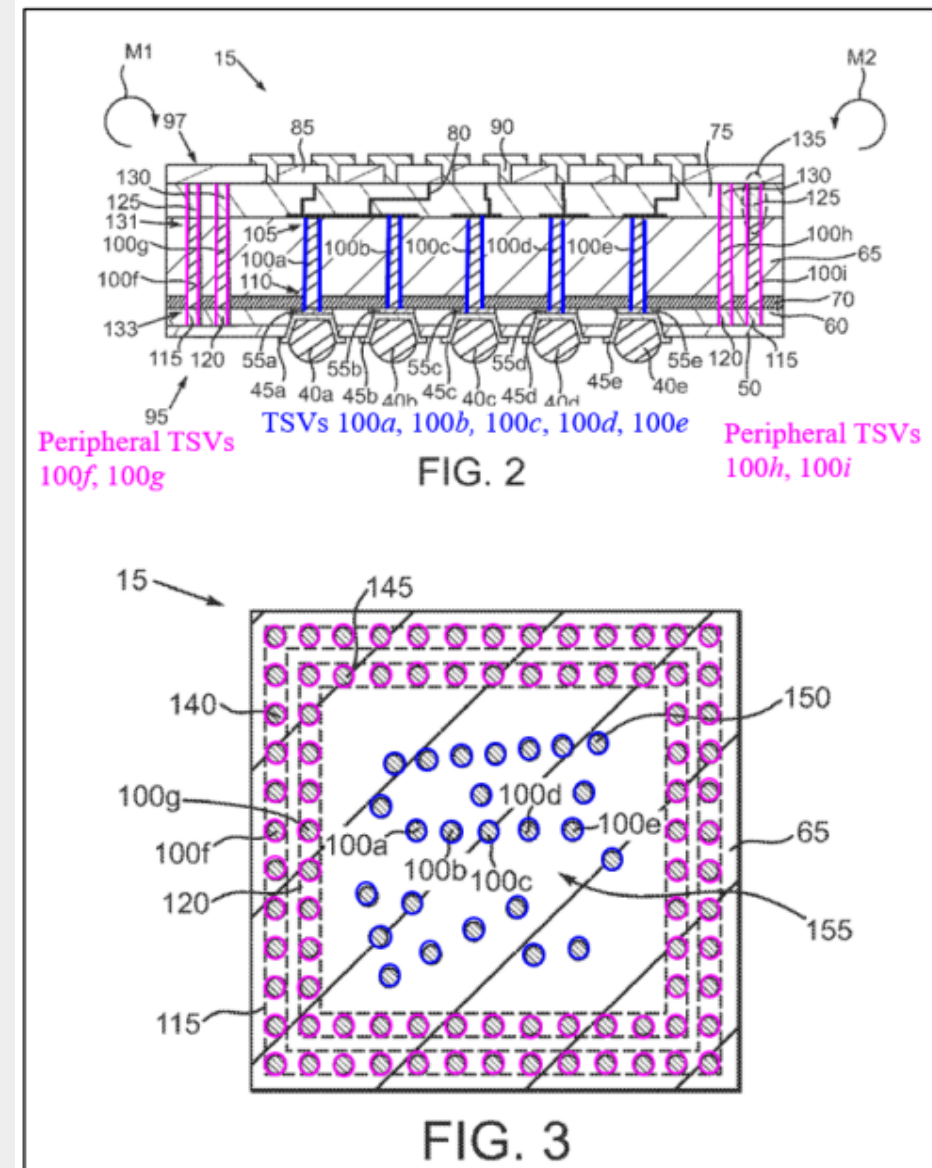
① The vias are not connected to any metal layer.

2. Non-Electrical Functions

50. Regarding the non-electrical functions, via structures had been used to improve the structural integrity of the wafer or die. For example, as shown in the

The traditional TSVs serve the traditional functions for providing electrical connections, whereas the peripheral TSVs perform non-electrical functions such as to “stiffen the semiconductor chip 15 and resist bending due to” thermal cycling, or to serve “a crack stop role in that the TSVs provide interspersed barriers to crack propagation towards an interior portion 155 of the semiconductor chip 15.” *Su*, 6:1-8, 6:60-64, 7:33-37.

(Thompson Open (Ex. 1003), ¶50.)



Su, Figs. 2-3.

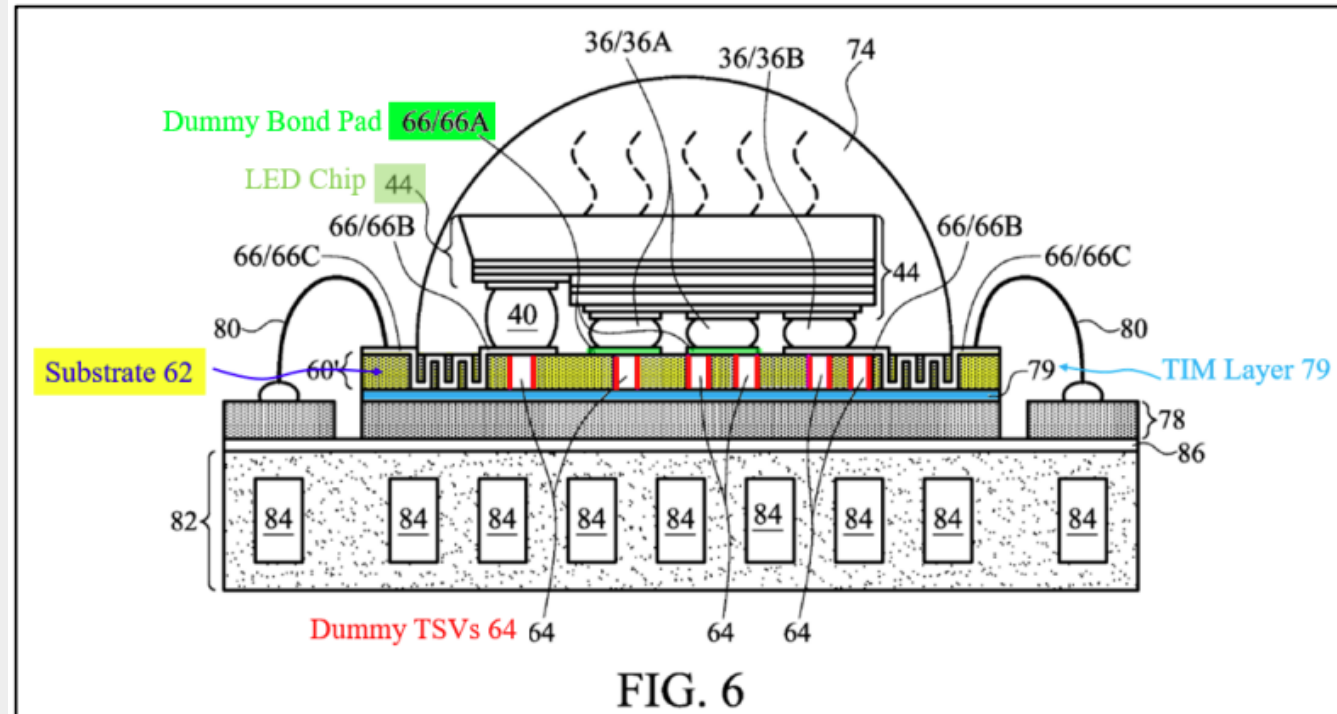
Non-Electrical Vias

② The vias are connected to metal layers, but the metal layers are not connected to any active devices.

52. Via structures had also been used to dissipate heat generated by semiconductor devices. For example, the following figure illustrates a “carrier

Wang, 3:14-19. “TSVs 64 are dummy TSVs since they are not used to conduct [electrical] currents, although voltages may be applied thereon.” *Wang*, 3:23-24. Rather, “dummy TSVs 64 ... have the function of dissipating heat.” *Wang*, 3:25-27. Dummy “TSVs 64 may be formed of copper or other metals, such as tungsten, or alloys thereof.” *Wang*, 3:19-20. The carrier chip 60' is adhered to a lead frame

(Thompson Open (Ex. 1003), ¶52.)



Wang, Fig. 6.

(Petition 46.)

Non-Electrical Vias

- ② The vias are connected to metal layers, but the metal layers are not connected to any active devices.

This contradicts the common understanding in the art. It was well-known that merely connecting the anchor vias' metal filler to both metal layers on the opposing sides of the substrate is not enough to provide ground connection to active devices.

(Thompson Suppl.(Ex. 1034), ¶21.)

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices and instead provides physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150, which may be formed on bottom side 112 of semiconductor substrate 110 as shown in more detail in FIG. 1B. Each of anchor vias 132 and 133 may be formed to a depth d_0 of 100 μm into semiconductor substrate 110. However, anchor vias 132 and 133 are not so limited and d_0 may be greater or less than this value, according to the particular application. In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the metal filler within anchor vias 132 and 133 essentially has a floating voltage potential during operation. Where the metal filler within anchor vias is connected to an overlying metal layer, the anchor vias may provide increased holding strength due to the additional physical connection to the overlying metal layer.

('826 Patent, 3:12-31.)

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Disputed Issues

- Claims 1, 11: “at least one anchor via disposed in at least one corner”
 - Construction of “disposed in ... [a] corner”
 - *Conn* discloses “disposed in ... [a] corner” under its plain and ordinary meaning
 - *Conn* discloses “disposed in ... [a] corner” under HID’s erroneous construction
- Claims 9, 19: “said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate”

Construction of “Disposed in ... [a] Corner” (Claims 1, 11)

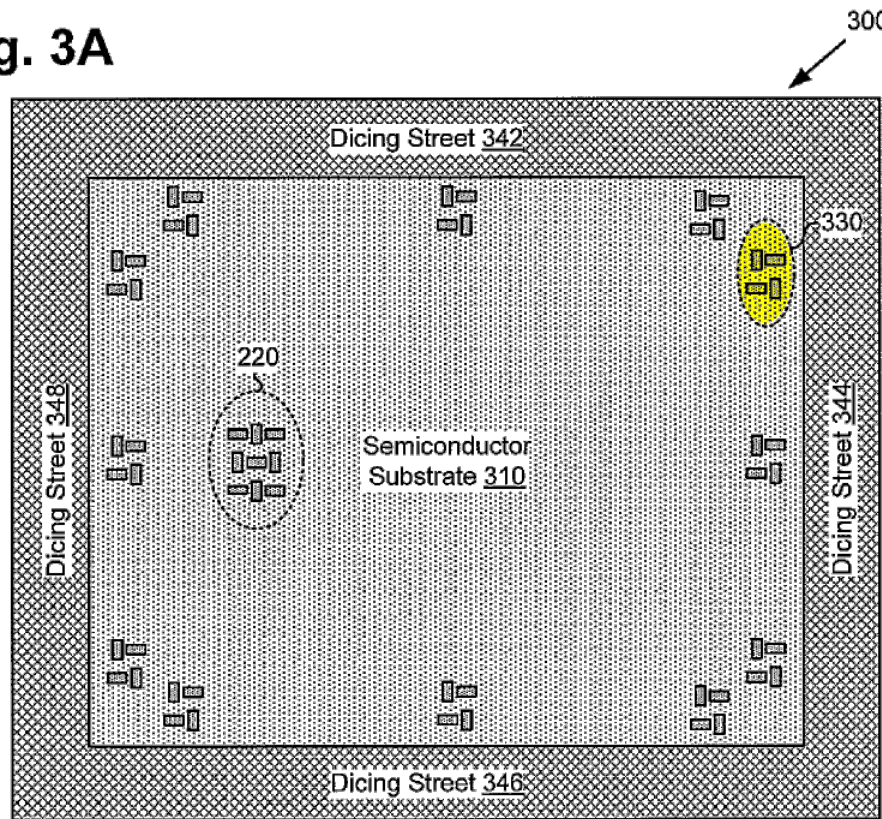
Claim Term	Samsung	HID
“disposed in ... [a] corner” (all claims)	plain and ordinary meaning	“located outside a round or ovoid geometrical shape inscribed within the edges of the semiconductor die”

Plain and Ordinary Meaning

peeling from the edges and/or corners of the die. Thus, cluster 330 of anchor vias may be fabricated proximate to a corner of semiconductor substrate 310 in order to prevent the backside metal stack from peeling at the corners of the die.

(’826 patent, 6:22-25.)

Fig. 3A



(’826 patent, Fig. 3A.)

Cluster 330a of anchor vias may be formed a predetermined distance d_{10} from the corner of semiconductor substrate 310m which may vary depending on the particular application.

(’826 patent, 6:65-67.)

Fig. 3C

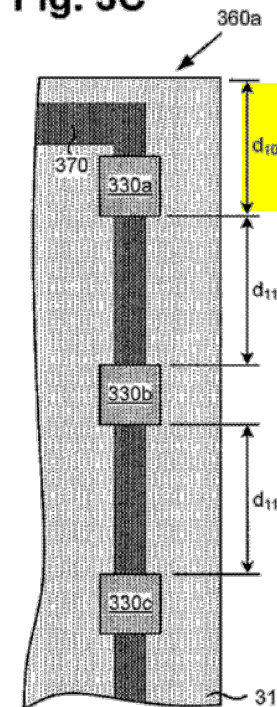


Fig. 3D

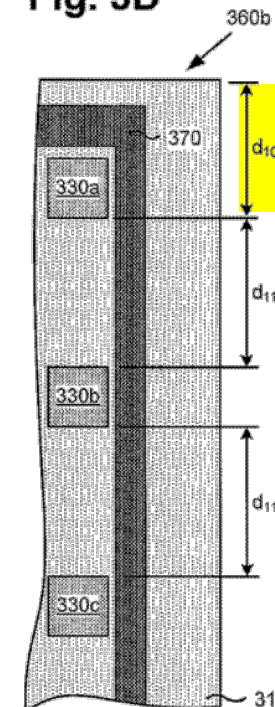
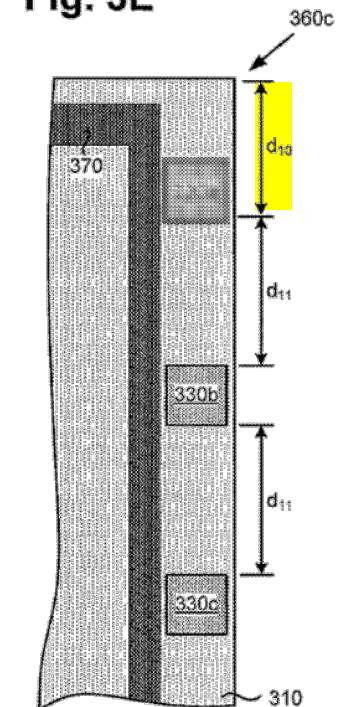


Fig. 3E



(’826 patent, Figs. 3C-3E.)

Plain and Ordinary Meaning

4 were talking about by a corner. A corner
5 is just a point, but the claim language
6 allows to be near a corner. So we show a

(Thompson Depo. (Ex. 2009), 36:21-37:7.)

12 Q. Within the context of the '826
13 patent, what does "in the corner" mean?

14 MR. ZANG: Objection; form.

15 A. In the context of the patent,
16 the claim says anchor via disposed in at
17 least one corner. So the corner is a point
18 disposed, and at least one corner means
19 near the corner.

20 If I look at figure 2-A of the
21 '826 patent, you see anchor vias 232-A,
22 232-B, and 232-C. None of them are in the
23 absolute corner of the die, so it means
24 near the corner of the die.

(Thompson Depo. (Ex. 2009), 39:12-24.)

Conn Discloses “Disposed in ... [a] Corner” Under its P&O Meaning

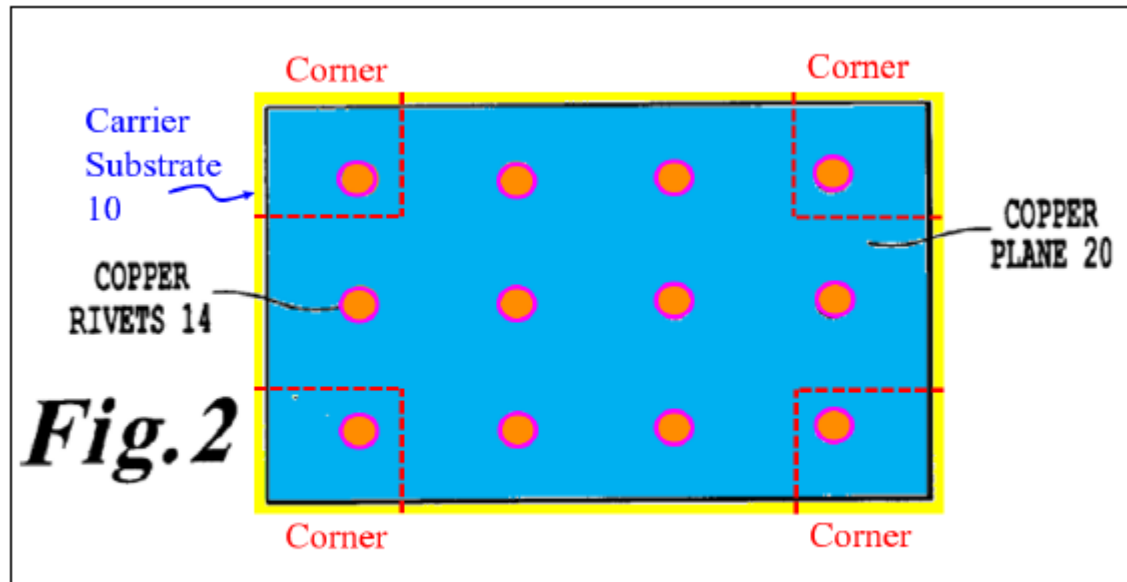


Fig. 2

Conn, Fig. 2 (modified),

(Thompson Open (Ex. 1003), ¶84.)

[0035] The via conductors can be distributed relative to the conducting layer 20 in a pattern as shown for example in FIG. 2. Other distribution patterns and irregular distribution patterns are also permissible and may be needed to accommodate chip attachment. The vias 12 can have a diameter

(*Conn*, [0035].)

Conn, [0035]. Figure 2 shows that the anchor via pattern covers the entire surface of the conducting layer 20, such that some anchor vias are disposed at the corners of the conducting layer 20. *Conn*, [0035]. In my opinion, those skilled in the art

(Thompson Open (Ex. 1003), ¶83.)

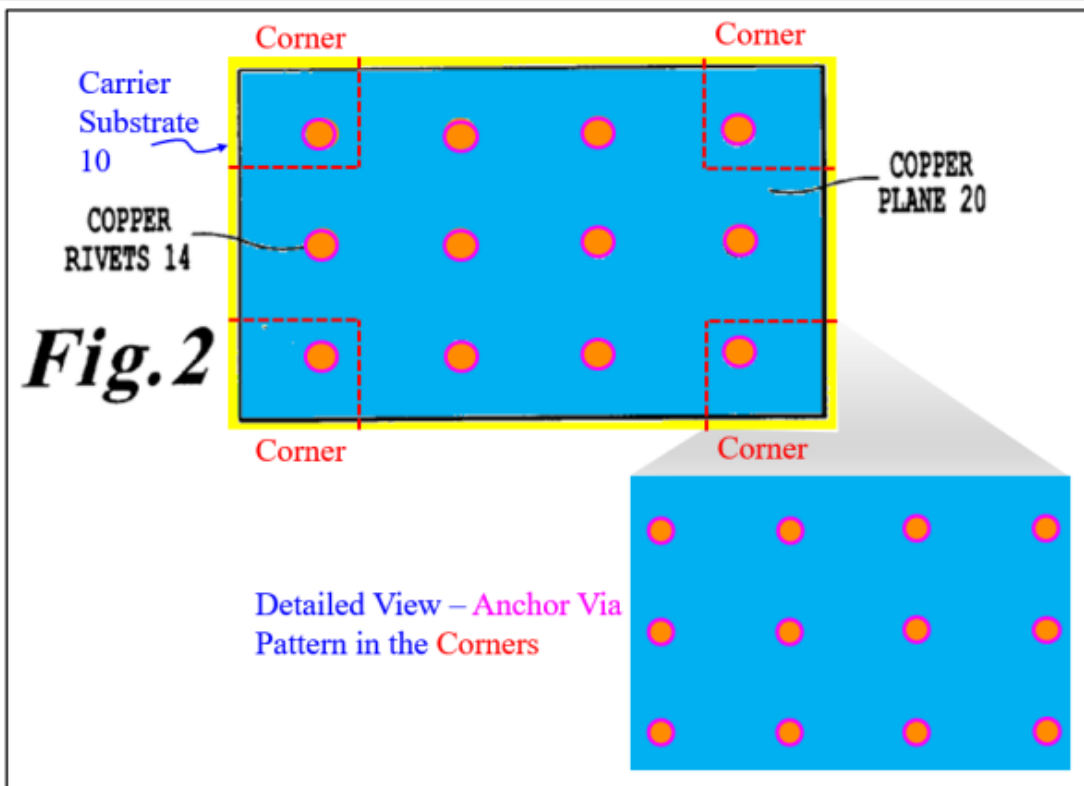
Conn Discloses Various Via Conductor Densities and Patterns

[0035] The via conductors can be distributed relative to the conducting layer 20 in a pattern as shown for example in FIG. 2. Other distribution patterns and irregular distribution patterns are also permissible and may be needed to accommodate chip attachment. The vias 12 can have a diameter between 30 and 150 μm . A distance between the via conductors is between 60 and 1000 μm . A density of the via conductors in the pattern is between 0.01 and 400 via conductors per unit square millimeter.

[0036] This density of the via conductors can be uniform across the entire conducting layer 20. Thus, for a conducting layer having approximate sizes of 140 mm by 80 mm, the number of via conductors can reach 100,000 per conducting layer. The number of via conductors for the above noted size of the conducting layer 20 has a minimum of 5000 and a maximum of 200,000.

(Conn, [0035]-[0036].)

Conn Discloses “Disposed in ... [a] Corner” Under P&O Meaning



Conn, Fig. 2 (modified).

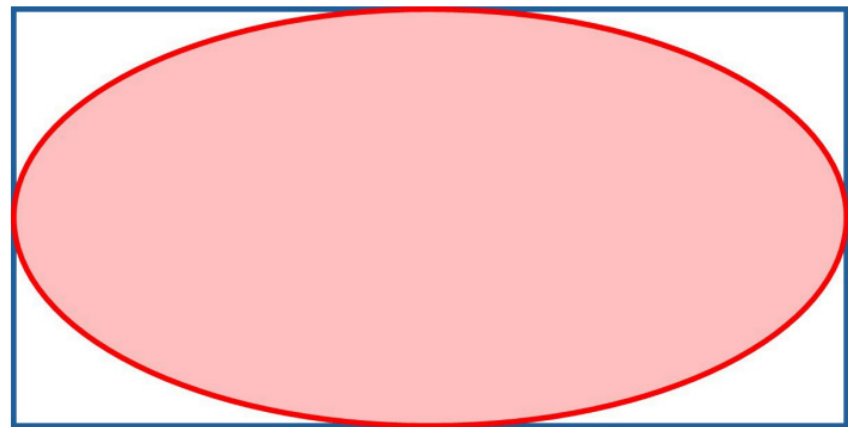
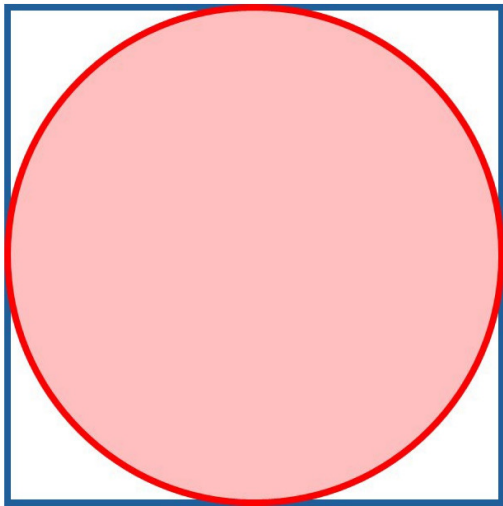
(Petition 39.)

6 Q. Where did that detailed view
7 come from?
8 MR. ZANG: Objection; form.
9 A. It comes from the spec of Conn
10 where figure 2 is just showing four -- it's
11 showing 12 anchor vias. But he envisions
12 much higher density. And so the spec of
13 Conn is saying you can, as I said earlier,
14 can have much higher density and space
15 these anchor vias 60 micrometers apart on a
16 grid.

(Thompson Depo. (Ex. 2009), 45:6-16.)

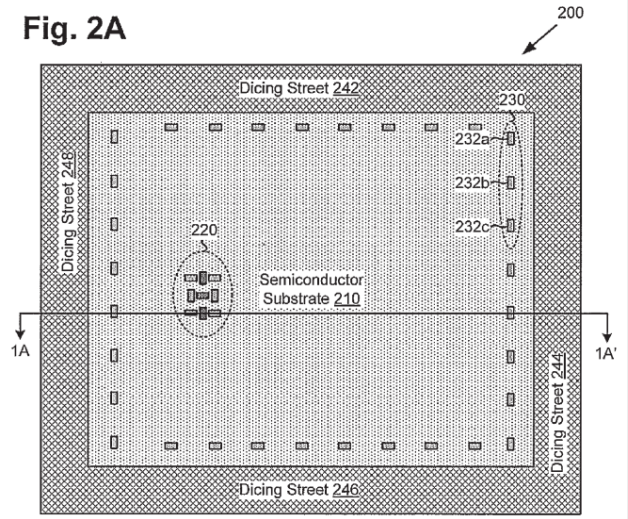
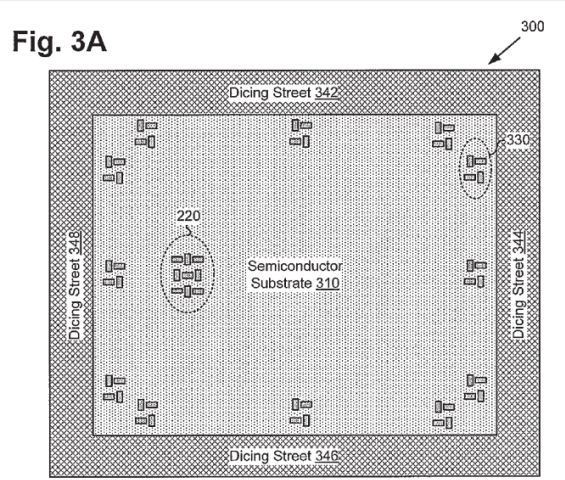
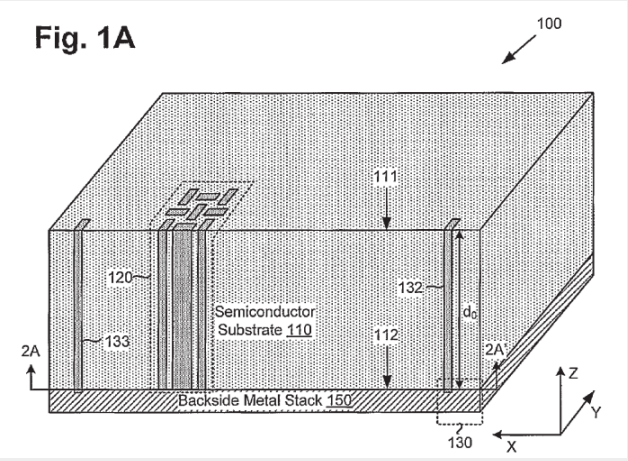
No Intrinsic Evidence Supports HID's Construction

HID's Construction



(POR 20-21.)

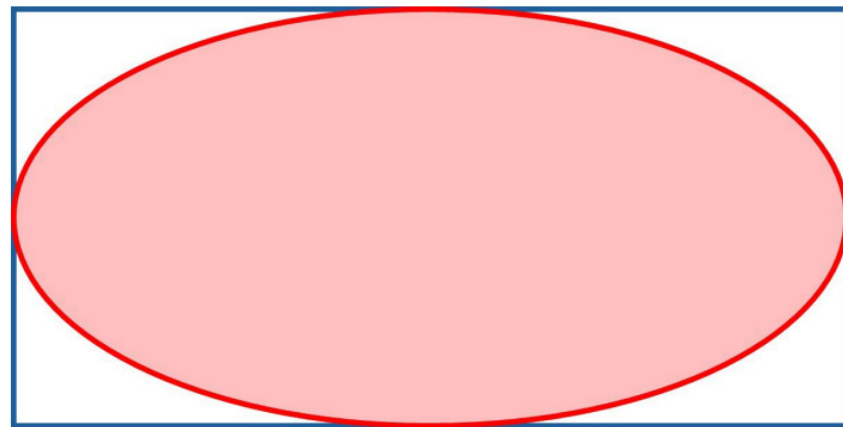
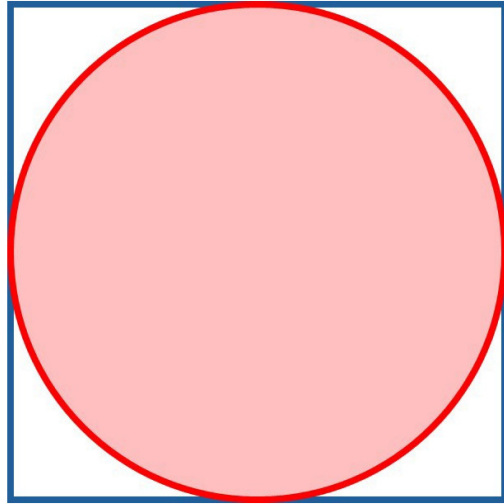
'826 Patent



('826 patent, Figs. 1A, 2A, 3A.)

No Intrinsic Evidence Supports HID's Construction

HID's Construction



(POR 20-21.)

HID's Expert

39. The specification of the '826 Patent also discloses in Figure 3C that the anchor vias “may be formed a predetermined distance d_{10} from the corner of semiconductor substrate 310 *m* which may vary depending on the particular application.” '826 Patent, 6:65-67. This predetermined distance d_{10} is shown in

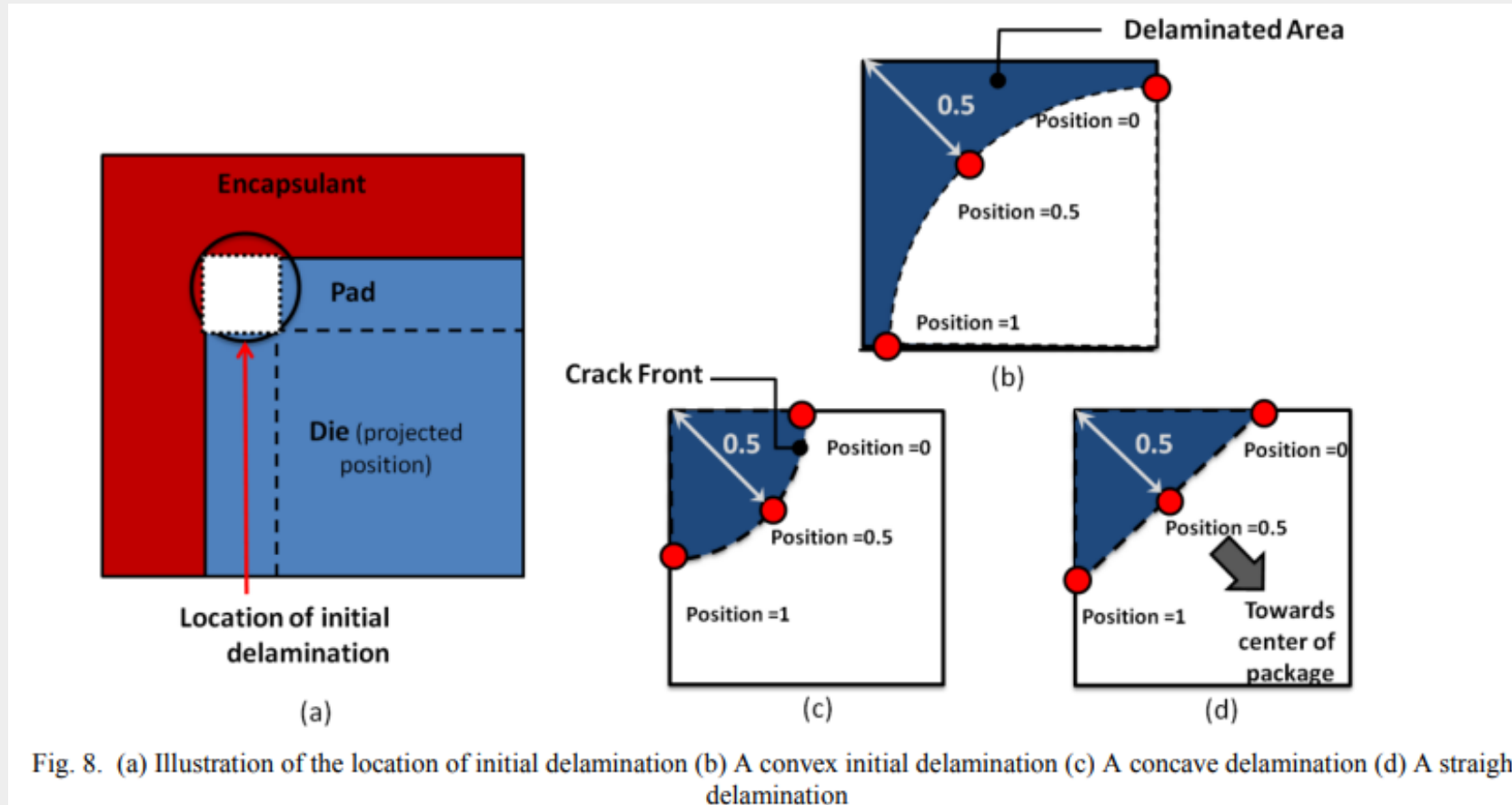
(Berg Decl. (Ex. 2004), ¶39.)

HID's Extrinsic Evidence Undermines its Construction

PETITIONER'S MOTION TO EXCLUDE EVIDENCE

(Paper 27.)

Ex. 2007 (*Ho*)



(POR 22.)

HID's Extrinsic Evidence Undermines its Construction

PETITIONER'S MOTION TO EXCLUDE EVIDENCE

(Paper 27.)

Ex. 2008 (*Rabie*)

52. Additionally, the paper “Optimizing Die Corner and Optical Groove Corner Crackstop Support Structures for Mitigating Dicing and CPI Risks” (Rabie et al., 2021) (Ex. 2008, “Rabie”), although dated after the priority date of the '826 Patent, also confirms known understandings of the meaning of the “corner” of the semiconductor die. For example, Rabie notes that corner delamination is caused by

• • • • •

54. I note that in Figure 2, the delamination on the top left of the semiconductor die travels inside the circle and, therefore, is not completely in the corner. However, an anchor via or other suitable delamination protection mechanism located within the corner would have prevented this delamination.

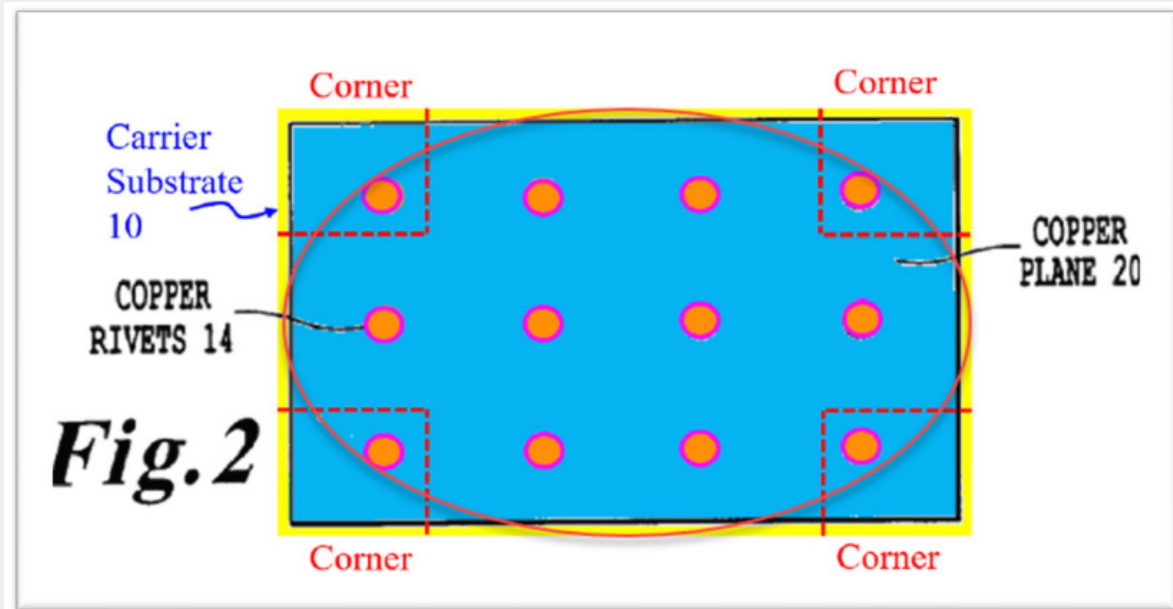


Figure 2 – Top view of a 28.4×22.9 mm² die on a 68.5×68.5 mm² laminate showing corner delamination in the top 2 corners after underfill cure at 165°C for 2 hours.

(Berg Decl. (Ex. 2004), ¶¶52, 54.)

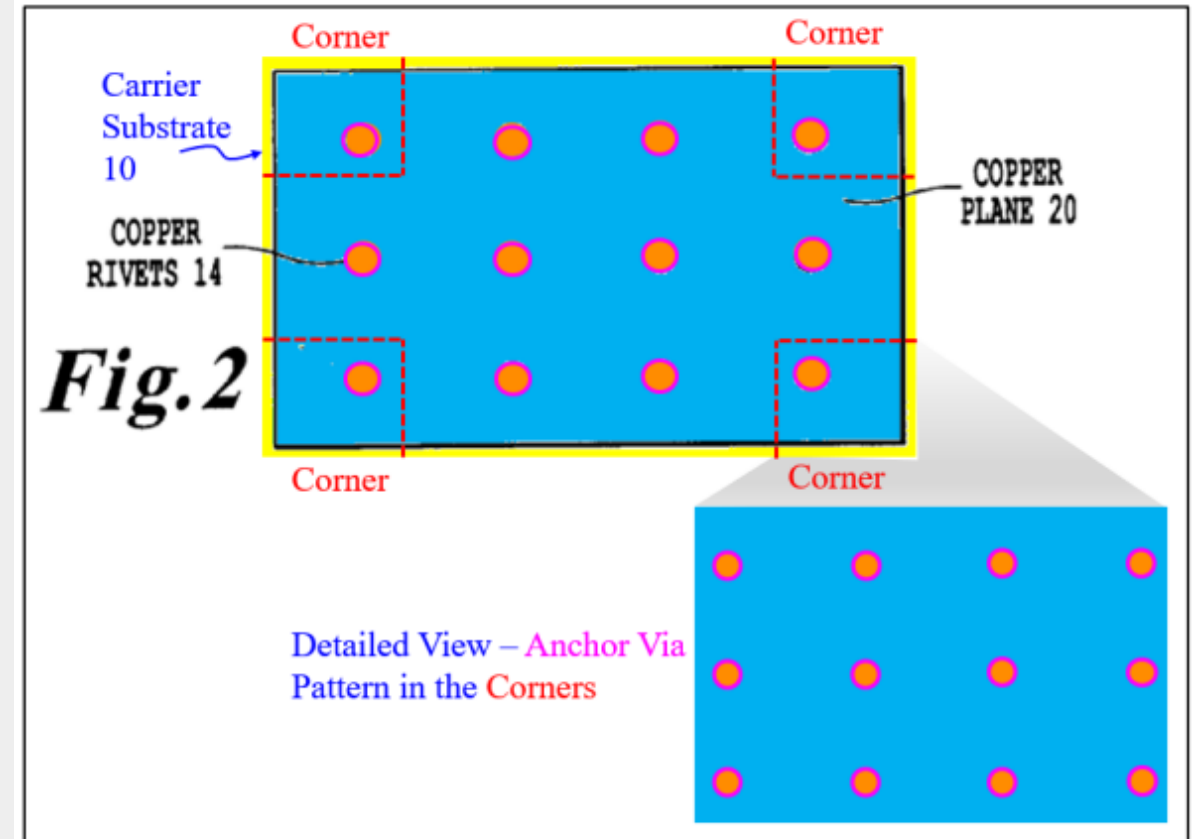
Conn Discloses “Disposed in ... [a] Corner” Under HID’s Construction

HID



(POR 37.)

Samsung

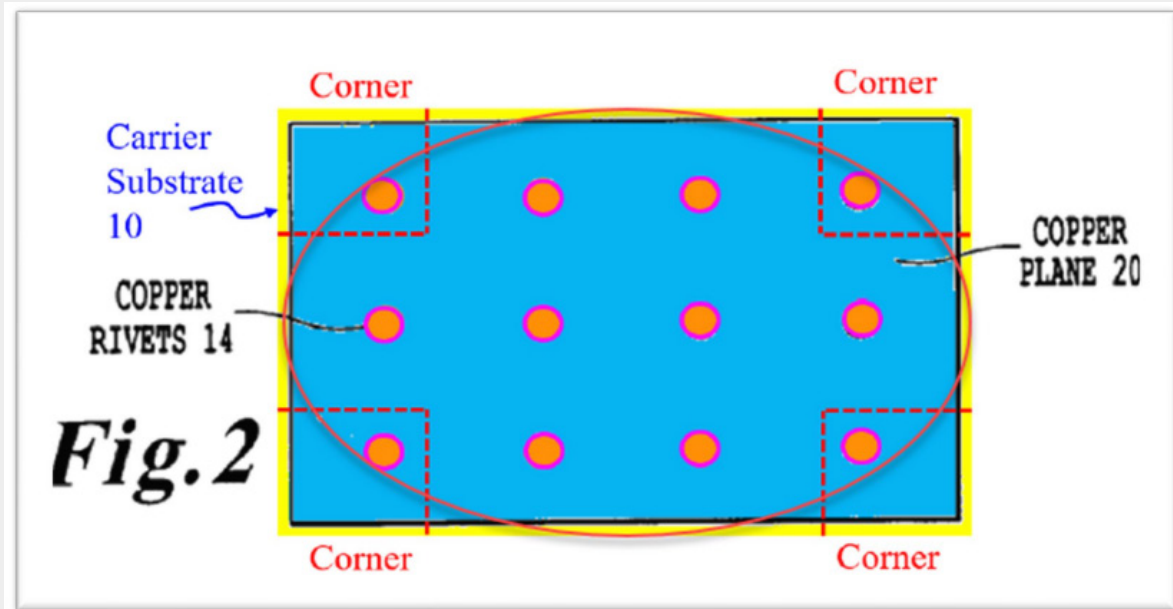


Conn, Fig. 2 (modified).

(Petition 39; Pet. Reply 19.)

Conn Discloses “Disposed in ... [a] Corner” Under HID’s Construction

HID



(POR 37.)

Samsung’s Expert

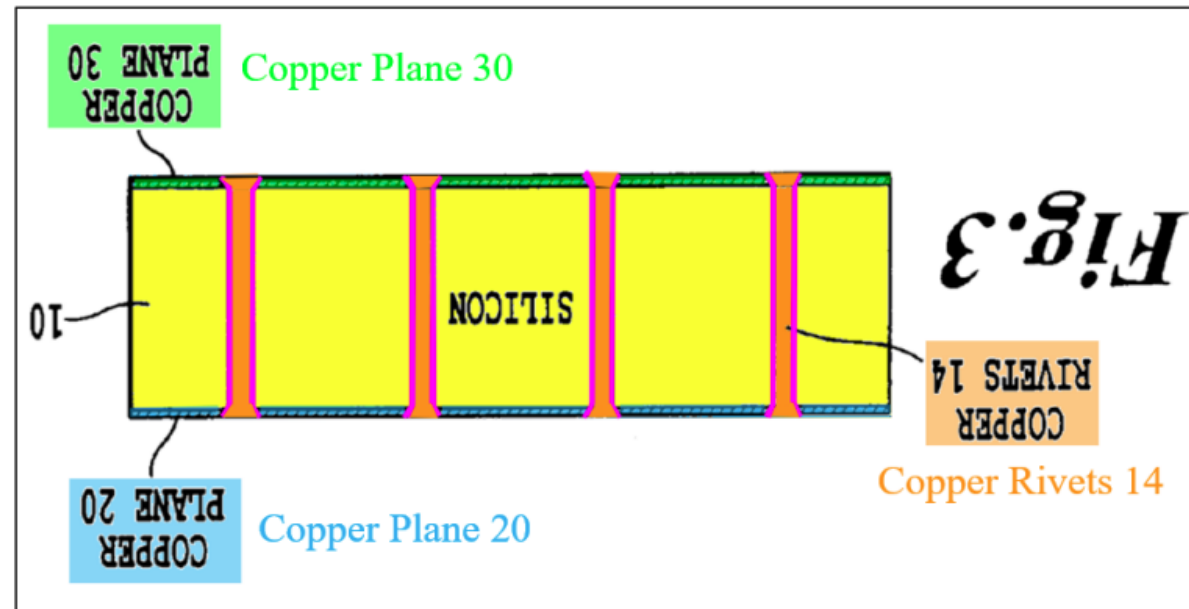
94. As discussed in §XIB.2, *Conn* discloses at least one **anchor via** disposed in a **corner** of a semiconductor substrate by disclosing a pattern of **anchor vias** that spreads across the substrate and extends to its **corners**. *Conn*, [0031], [0035], Fig. 2. This means the **anchor vias** are repeated in the substrate, including the **corners**, according to the pattern, and having certain densities as disclosed in *Conn*, e.g., 400 vias per mm². *Conn*, [0035]-[0036]. Thus, as illustrated below, a POSA would understand that each **corner** has a pattern of repeating **anchor vias**, i.e., “a cluster of **anchor vias**.” For example, semiconductor dies (i.e., chips)

(Thompson Open (Ex. 1003), ¶94.)

Conn Anticipates Claims 9 and 19

G. Claim 9

The structure of claim 1, wherein said **metal filler** within said at least one **anchor via** is bonded to a **metal layer** overlying said semiconductor substrate.



Conn, Fig. 3 (rotated by 180°).

(Petition 43.)

No Dispute: *Conn* Discloses “At Least One Anchor Via Does Not Provide Ground Connection to One or More Active Devices” (Claims 1, 11)

1. A structure comprising:
at least one anchor via disposed in at least one corner of a semiconductor substrate;
a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via:

wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

9. The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer overlying said semiconductor substrate.

(’826 patent, 7:58-8:3, 8:27-29.)

Conn Discloses a Mechanical Connection – Not a Ground Connection

plural vias 12. The vias can be through-vias or can be vias that extend from the first main surface but do not reach the opposing second main surface of the carrier substrate 10. As shown in FIG. 1, the via conductor 14 is formed to enter at least partially in the via 12 but the via conductor 14 does not necessarily have to go all the way through the via 12.

(*Conn*, [0028].)

[0038] In the embodiment shown in FIG. 3, the conducting layers 20 and 30 are mechanically connected by at least one via conductor 14, which acts as a rivet to hold the conducting layers 20 and 30 mechanically connected to the substrate. The

(*Conn*, [0038].)

POSITA: *Conn*'s Anchor Vias Do Not Provide Electrical Connection

1. *Conn* discloses that the anchor vias (or the via conductor) extend from the first main surface of the carrier substrate but do not need to reach the opposing second main surface. Thompson Open, ¶93 (citing *Conn* at [0028]). Thus, a POSITA would understand that *Conn*'s anchor vias are not used for providing electrical connection to active devices because otherwise it would be impossible to vary the length of the anchor vias or via conductor. Figure 3 of *Conn* shows the extreme case of such variation, with both anchor vias and via conductor extending to the opposing second main surface. *Conn*, [0038], [0040]-[0041]. But it does not mean they provide electrical connection to active devices. This is because the elements in

Thompson Suppl. (Ex. 1034), ¶19.

Dr. Thompson's Testimony Is Supported by Other Prior Art

Wang

dielectric substrate. Through-substrate vias (TSVs) 64 are formed in substrate 62, and electrically connect features on opposite sides of substrate 62. TSVs 64 may be formed of copper or other metals, such as tungsten, or alloys thereof. Bond pads 66 (including 66A, 66B, and 66C) are formed on one side of carrier wafer 60 and connect to TSVs 64.

TSVs 64 are dummy TSVs since they are not used to conduct currents, although voltages may be applied thereon. Throughout the description, dummy TSVs 64 are also referred to as thermal TSVs since they have the function of dissipating heat. Similarly, the bond pads 66 that have current

(*Wang* (Ex. 1019), 3:17-24.)

Nishio

[0096] To prevent this, in the via group shown in FIG. 7A according to the present example embodiment, a plurality of through vias (true through vias) 60 used for electrical connections are disposed at the center portion of the via group, while dummy through vias 61 not electrically connected to the wires in the semiconductor device are disposed at a peripheral portion of the via group. In other words, the

(*Nishio* (Ex. 1028), [0096].)

Conn's Disclosure Is the Same as that of the '826 Patent

Some TSVs Provide a Ground Connection

example. As shown in FIG. 1A, group 120 of TSVs is formed in a core region of semiconductor substrate 110, while each of anchor vias 132 and 133 are formed in a peripheral region of semiconductor substrate 110. Metal filler within group 120 of TSVs provide low resistance, low inductance ground connections to one or more active devices fabricated in and/or on semiconductor substrate 110 and may be electrically connected to an overlying metal layer, such as a metal 1 layer for example, for grounding active devices such as the emitters of bipolar transistors.

Some TSVs Provide Mechanical Connection

By contrast, a metal filler within anchor vias 132 and 133 does not provide ground connection to any active devices and instead provides physical anchor points between semiconductor substrate 110 and the underlying backside metal stack 150, which may be formed on bottom side 112 of semiconductor substrate 110 as shown in more detail in FIG. 1B. Each

than this value, according to the particular application. In addition, the metal filler within anchor vias 132 and 133 may either not contact a front side metal layer, or if contacting a front side metal layer such as metal 1 layer, the contacted portion of metal 1 layer may be patterned such that the metal filler within anchor vias 132 and 133 essentially has a floating voltage potential during operation. Where the metal filler

(’826 patent, 3:12-27.)

POSITA: *Conn*'s Anchor Vias in Figures 1-3 Do Not Provide Ground Connection

layer to form a circuit. As I explain above, the anchor vias in *Conn*'s Figures 1-3 do not serve the purpose of providing electrical connection. Figure 3 does not dictate otherwise. A POSITA would understand that the anchor vias in the embodiment in Figure 3 would only be capable of providing ground connection to active devices if the metal layers were patterned to do so, and *Conn* does not disclose such patterning or otherwise suggest the anchor vias provide electrical connection in Figure 3. Thus, a POSITA would understand that the anchor vias in Figure 3, just like those in Figure 1, do not provide ground connection to any active devices.

(Thompson Suppl. (Ex. 1034), ¶21.)



AC Techs. S.A. v. Amazon.com, Inc., 912 F.3d 1358, 1367 (Fed. Cir. 2019) (“a reference need not state a feature’s absence in order to disclose a negative limitation”) (citation omitted).

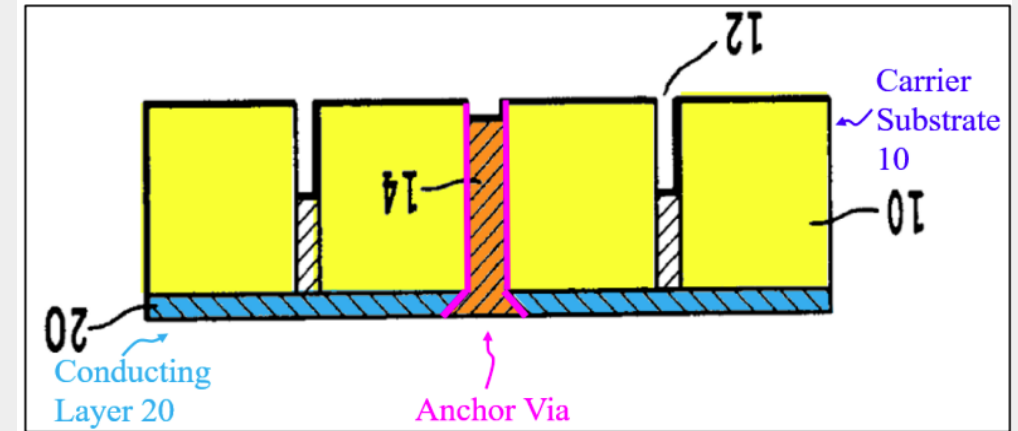
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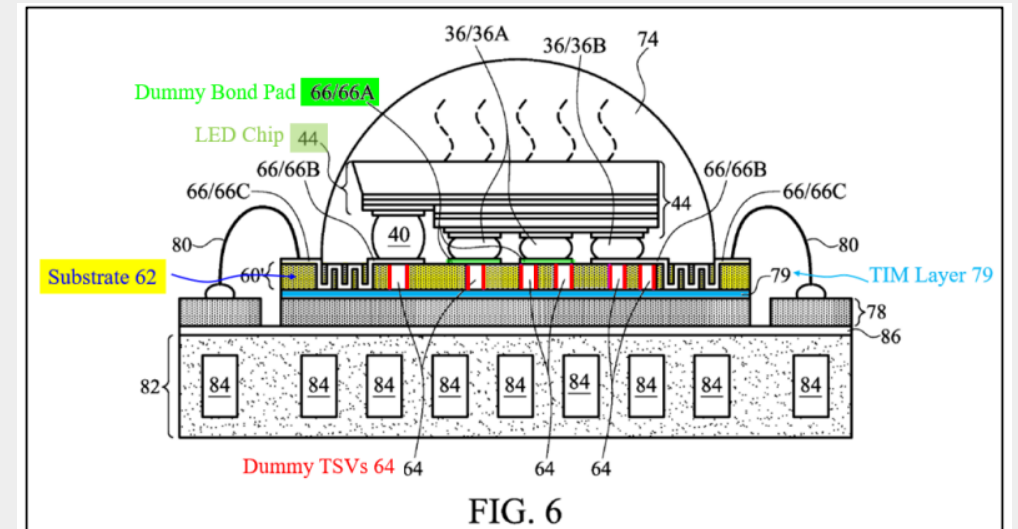
Conn Renders Obvious “Not Provide Ground Connection” Limitation

Specifically, *Conn* discloses that its carrier substrate is used “for mounting of semiconductor chip devices and components.” *Conn*, [0003]; *id.*, [0030], [0035]. *Conn* does not show how the chips are mounted, but a POSA would have known this. Thompson, ¶111. For example, *Wang* (*supra*, §II.D.2) provides a use case for *Conn*’s carrier substrate. As discussed in §II.D.2, *Wang* discloses a carrier chip 60’

(Petition 45-46.)



Conn, Fig. 1 (rotated by 180°).



Wang, Fig. 6.

Conn Renders Obvious “Not Provide Ground Connection” Limitation

113. In my opinion, a POSA would have been motivated to use *Conn*’s electronic package structure for packing *Wang*’s LED chip. As shown below, the

Therefore, a POSA would have appreciated that *Conn*’s electronic package structure is suitable for use in *Wang* to mount the LED chip 44. Namely, *Conn*’s 62 and TIM layer 79, respectively. And *Conn*’s anchor vias substitute *Wang*’s dummy TSVs 64 to achieve the dual purpose of improving *Wang*’s heat dissipation and metal layer adhesion (i.e., securing one or both of TIM layer 79 and dummy bond pads 66A).

(Thompson Open (Ex. 1003), ¶113.)

114. In the *Conn-Wang* use case, *Conn*’s conducting layer is disposed on a side of the carrier substrate opposite to the LED chip—active device, thereby constituting a backside metal layer. *Supra*, §VI.B. And, the via conductors in *Conn*’s anchor vias do not provide ground connection to the LED chip, because they are dummy vias designed for dissipating heat and securing backside metal, but not for providing electrical connection. *Conn*, [0011]; *Wang*, 3:23-27; *supra*, §XI.B.5.

(Thompson Open (Ex. 1003), ¶114.)

HID Incorrectly Argues that Ground 2 Does Not Address “Not Provide Ground Connection” Limitation

HID

Patent Owner’s arguments under Ground 1 are not related to any lack of disclosure relating to “backside” or “active devices,” nor to any ordering of steps in Claim 11. *See supra*. Accordingly, Petitioner’s Ground 2A arguments do not remedy the deficiencies of Ground 1.

(POR 44.)

the limited scope of Ground 2A,⁸ Petitioner now contends that Ground 2 renders Claims 9 and 19 obvious because a POSITA would modify *Conn* to use *Wang*’s structure where dummy TSVs do not provide a ground connection. Reply, 23. Substituting *Wang*’s dummy TSVs—extending fully through the substrate to another metal layer—for *Conn*’s vias is a new argument and modification not disclosed in the Petition. Pet., 47-48.

(PO Sur-Reply 17-18.)

Samsung’s Petition

Accordingly, considering the actual use cases of *Conn*’s electronic package, *Conn* renders obvious the “backside metal layer” and “not provide ground connection” limitations. Thompson, ¶115. A POSA would have had a reasonable

(Petition 48.)

[0037], with *Wang*, Fig. 6 (“dummy bond pads 66A”), 3:21-22, 3:27-33. Therefore, a POSA would have appreciated that *Conn*’s electronic package structure is suitable for use in *Wang* to mount LED chip 44. Thompson, ¶113. Namely, *Conn*’s carrier substrate 10 and conducting layer 20 can serve as *Wang*’s carrier substrate 62 and TIM layer 79, respectively. *Id.* *Conn*’s anchor vias can substitute *Wang*’s dummy TSVs 64 to achieve the dual purpose of improving *Wang*’s heat dissipation and metal layer adhesion. *Id.*

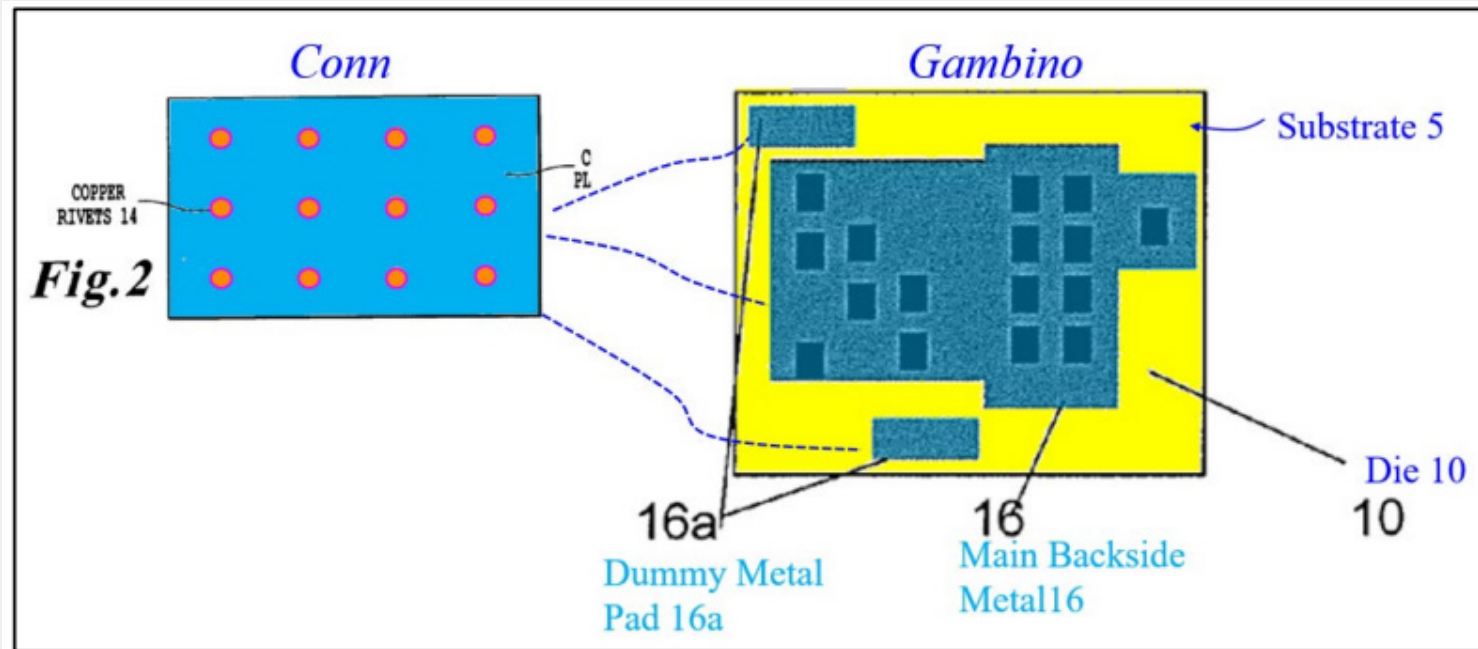
(Petition 47.)

Topics

- Instituted Grounds
- Technology Overview
- Ground 1: *Conn* Anticipation
- Ground 2: *Conn* Obviousness
- **Ground 3: *Gambino* Obviousness**
- Ground 4: *Torii* Anticipation
- Ground 5: *Ide* Anticipation

Proposed Combination

As shown below, a POSA would have found it obvious to apply *Conn*'s teachings to create **anchor vias** in *Gambino*'s **dummy metal pads 16a** and/or **main backside metal 16**, to secure **them** to the substrate and prevent delamination during singulation. Thompson, ¶135.



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

(Petition 60-61.)

Rationales to Combine *Gambino* and *Conn*

Samsung's Expert

139. Moreover, *Gambino* is ready for improvement because it already uses electrical TSVs and employs a TSV manufacturing process. *Gambino*, [0020]. The anchor vias could be made using the same process.

(Thompson Open (Ex. 1003), ¶139.)

electrical functions of the chip. Second, both *Gambino* and *Conn* teach using Bosch deep reactive ion etching (DRIE) to form the vias. *Gambino*, [0020]; *Conn*, [0049], [0055]. Thus, a POSA would have reasonably expected that the same process used for creating *Gambino*'s TSVs can also be used to create the anchor vias, with the patterns, linear densities, and total areas specified by *Conn*. Third,

(Thompson Open (Ex. 1003), ¶158.)

Conn

[0049] The vias 12 can be formed in the carrier substrate 10 by well know techniques, as for example Reactive Ions Etching (RIE) using the Bosch process. The Bosch process con-
(*Conn*, [0049].)

Gambino

[0019] In embodiments, the through silicon vias (TSV)12 can be formed using conventional processes, such as, for example, lithography, etching and deposition processes, with a backside polishing and grinding process, all of which are
(*Gambino*, [0019].)

[0020] As one example, Bosch deep reactive ion etching (DRIE) can be used to fabricate the TSVs with almost any diameter, from the submicrometer level to hundreds of micrometers. In more specific embodiments, a via can be
(*Gambino*, [0020].)

HID Alleges Two Wrong Outcomes of the Combination

HID

The proposed use of Gambino's [0020] process is a key element of

Petitioner's obviousness arguments because it is the sole offered reason that making the vias would lead to a predictable result and would not require undue experimentation. Pet., 64.

(POR 47.)

Utilizing Gambino's method to create *Conn* anchor vias would result in one

of two outcomes, neither of which meet the claims. Either the anchor vias would be

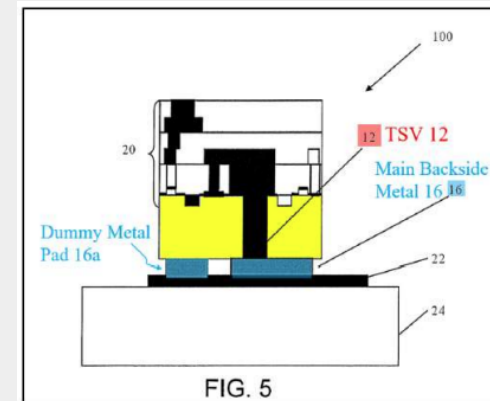
filled entirely, like Gambino's TSVs, or the anchor vias would not reach the backside

metal layer. Ex. 2004, ¶¶ 122-123. This is because Gambino creates holes in the

(POR 48.)

Gambino

micrometers. In more specific embodiments, a via can be formed in a front side of the die 10 using conventional lithography and etching processes. The via would typically extend only partially through the die 10 (or substrate 5). After formation of the via, metal can be deposited therein using conventional deposition processes such as, for example, electroplating or chemical vapor deposition techniques. In embodiments, the metal can be any appropriate metal used in semiconductor manufacturing processes for TSVs such as, for example, copper. The backside of the substrate 5 then undergoes a thinning process, e.g., a polishing and grinding process, in order to expose the TSVs 12.



Gambino, Fig. 5.

(Gambino, [0020], Fig. 5.)

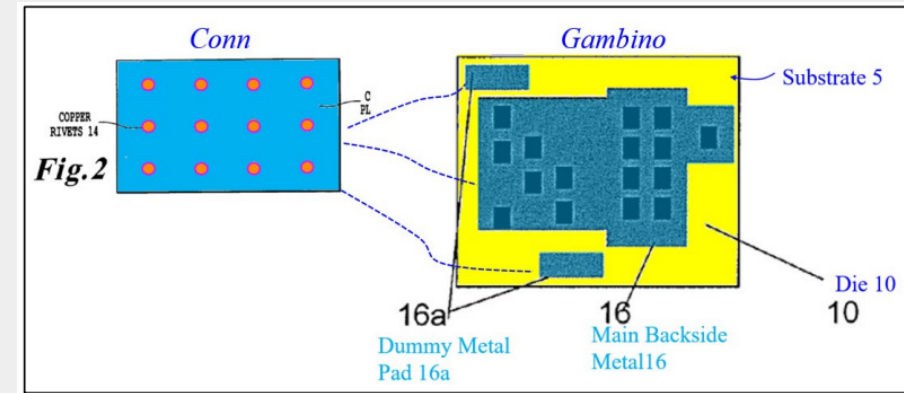
(1.A) POSITA Would Not Connect Anchor Vias to Active Devices

structure. Particularly, since the **anchor vias** are only formed at the backside of the substrate, they do not require redistribution of the active devices and wiring layers on the front side of the substrate. Moreover, *Gambino's* dummy metal pads 16a are located at the corners and peripheries of the substrate, which are less crowded areas that are not usually for planting active/passive devices, so adding the **anchor vias** here would not affect other elements in the devices.

(Thompson Open (Ex. 1003), ¶141.)

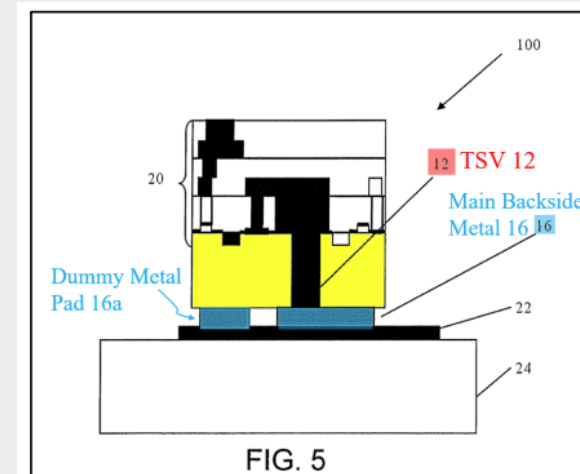
143. Third, the function of the resulting combination is predictable because the introduction of *Conn's* **anchor vias** to *Gambino* will not affect the packaged module's electrical functions. The **anchor vias** themselves do not need to be connected to active or passive devices. *Supra*, §XI.B.5. *Gambino's* dummy metal pads 16a also do not serve electrical functions. Thus, the **anchor vias'** presence will not change these devices' functioning.

(Thompson Open (Ex. 1003), ¶143.)



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

(Thompson Open (Ex. 1003), ¶135.)



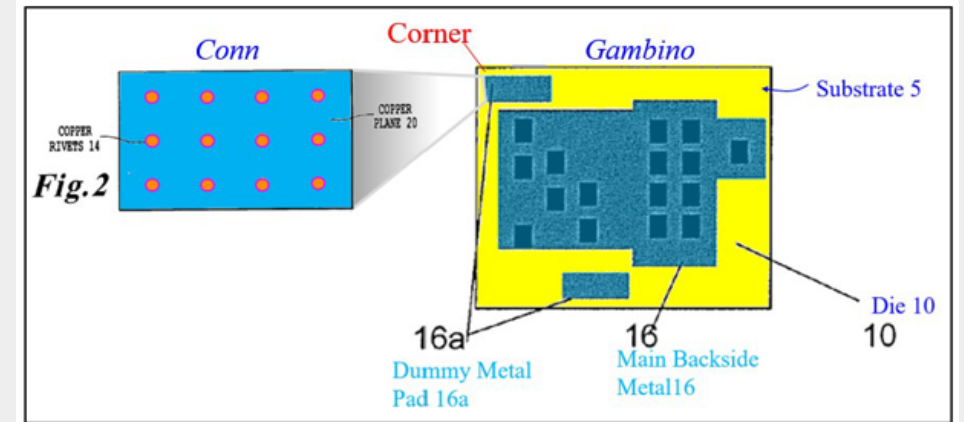
Gambino, Fig. 5.

(Thompson Open (Ex. 1003), ¶134.)

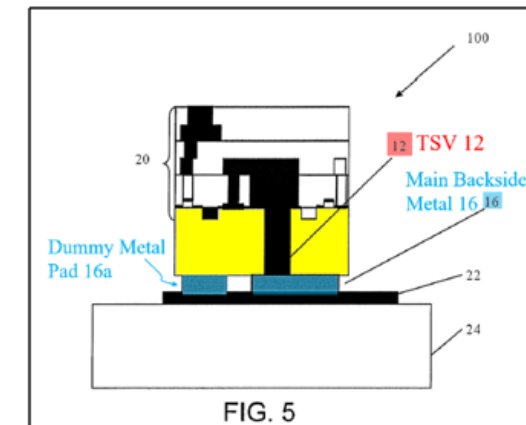
(1.A) POSITA Would Not Connect Anchor Vias to Active Devices

corners and peripheries of a die are close to the dicing channels. *Gambino* teaches locating the active TSVs and their connected backside metal in an area of the die so that they “do[] not interfere with dicing operations performed within the dicing channel” *Gambino*, Abstract; see also *Gambino*, [0004]-[0006], [0015]-[0017], [0021], [0029]. Motivated by the same principle, a POSITA would also have located the wiring layers in areas away from the corners and peripheries, to prevent the wiring layers from interfering with the dicing. Thus, on the front side of the substrate, a POSITA would not have placed wiring layers directly above the corner-located dummy metal pads 16a. *Gambino*, [0030], Fig. 5. As such, the metal filler of the anchor vias planted at the dummy metal pads 16a would not contact any wiring layers.

(Thompson Suppl. (Ex. 1034), ¶22.)



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

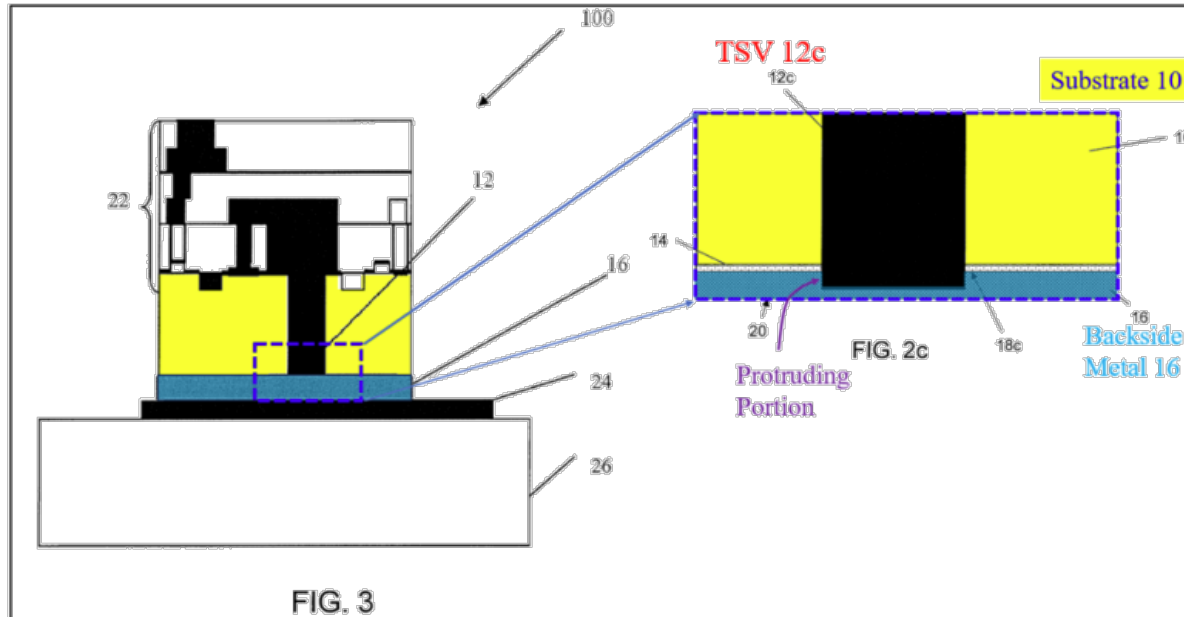


Gambino, Fig. 5.

(Thompson Suppl. (Ex. 1034), ¶22.)

(1.B) The Resulting Anchor Vias Would Form Protruding Portions

145. Fifth, the proposed combination was well-known. For example, *Burnham* had already used via structures with protrusion portions to improve backside layer adhesion. *Supra*, §VLE. A POSA would have appreciated that the proposed combination is simply replicating prior art and would have succeeded.



Burnham, Figs. 2c and 3.

(Thompson Open (Ex. 1003), ¶145.)

Pet. Reply 24-26; Thompson Open (Ex. 1003), ¶¶54, 145;
Thompson Depo. (Ex. 2009), 55:6-17.

6 Q. Have you ever seen an
7 implementation of Gambino that also used
8 anchor vias?

9 MR. ZANG: Objection; form.

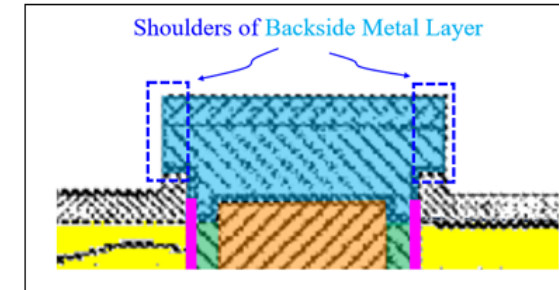
10 A. So I have. If you look at
11 Burnham on page 120 in my report, this is
12 from the same group. This is from IBM.
13 They also have a via that protrudes and
14 secures the backside metal. And so it
15 would be common to do multiple process
16 changes to secure the backside metal when
17 delaminating.

(Thompson Depo. (Ex. 2009), 55:6-17.)

(1.B) The Resulting Anchor Vias Would Form Protruding Portions

24. Mr. Berg further asserts that *Gambino*'s backside polishing or grinding method process would not yield a "protruding portion extending from a backside of said semiconductor substrate" as claimed. Berg, ¶128. I disagree. *Gambino* discloses using "a thinning process, e.g., a polishing and grinding process" to expose the metal filler of the anchor vias at the backside of the substrate. *Gambino*, [0020]. The backside polishing employs a chemical mechanical planarization (CMP) process to flatten and smooth the backside surface. It was well-known that the CMP process can selectively polish the substrate at a higher rate than the metal filler, thereby resulting in a metal protrusion. Ex. 1035 ("Yu"), 4:40-46 ("The second step involved a CMP process (Thompson Suppl. (Ex. 1034), ¶24.)

Moreover, I previously showed that the backside grinding process can form a protruding portion.



Torii, Fig. 46 (excerpted, zoomed).

(Thompson Suppl. (Ex. 1034), ¶24.)

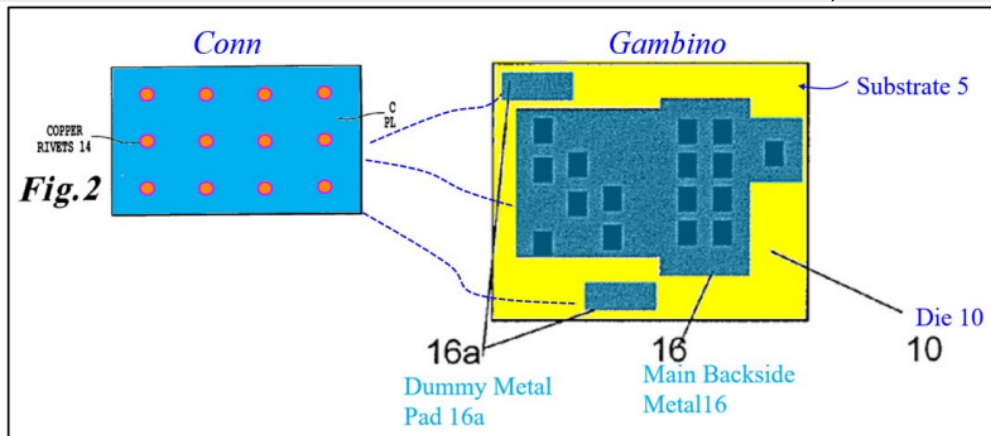
grinding. This substrate is backside-ground by mechanical grinding until the last minute whether to expose the bottom of insulating film **81**. FIG. 38 shows a state that the backside-grinding was stopped at the point of just exposing the bottom of insulating film **81**. Then, the substrate is etched by silicon etch-back up to a region in which the bottom of conductive film **82** slightly protrudes from the rear surface of the substrate, as illustrated in FIG. 39.

(*Torii*, [0099].)

(2) *Conn* and *Gambino*: Teach Mechanically Connecting the Anchor Vias to Backside Metal

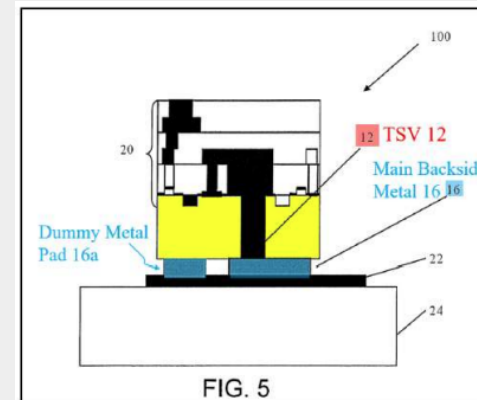
An electronic package and methods by which the package reduces thermal fatigue failure of conductors in the electronic package. The electronic package includes a carrier substrate having first and second surfaces and a plurality of anchor vias having a via material extending from the first surface toward the second surface. The electronic package includes a first conducting layer having a length and a width extending laterally in two dimensions across a major part of the first surface of the carrier substrate. The anchor vias have plural attachments along the length and the width of the first conducting layer to secure the first conducting layer to the carrier substrate.

(*Conn*, Abstract.)



Gambino, Fig. 3 (excerpted); *Conn*, Fig. 2.

[0030] FIG. 5 shows a packaged module with a backside metal ground plane attached to a substrate in accordance with aspects of the present invention. More specifically, FIG. 5 shows a device 100, comprising a plurality of metal wiring layers 20, one of which is at least in electrical communication with the TSV 12. The wiring layers 20 can include vias, wires, and a host of different active or passive devices, any combination of which is contemplated by the present invention. The TSV 12 is, in turn, in mechanical and electrical communication with the backside metal 16. In embodiments, the backside metal 16 has a planar surface, which connects to a substrate ground plane 22. The substrate ground plane 22 is bonded to the substrate 24. In embodiments, the construction of the device 100 does not require wirebonding techniques.



Gambino, Fig. 5.

(*Gambino*, [0030], Fig. 5.)

Topics

- Instituted Grounds
- Technology Overview
- Ground 1: *Conn* Anticipation
- Ground 2: *Conn* Obviousness
- Ground 3: *Gambino* Obviousness
- **Ground 4: *Torii* Anticipation**
- Ground 5: *Ide* Anticipation

Disputed Issues

- Claims 1, 11: “at least one anchor via does not provide ground connection to one or more active devices”
- Claims 1, 11: “a backside metal layer on a bottom surface of said semiconductor substrate”
 - Construction of “on”
 - *Torii* discloses “on a bottom surface” under its plain and ordinary meaning

Torii Discloses an Embodiment Where Sub-TSV Is Not Used as Current Pathway

Torii

[0048] Note that in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

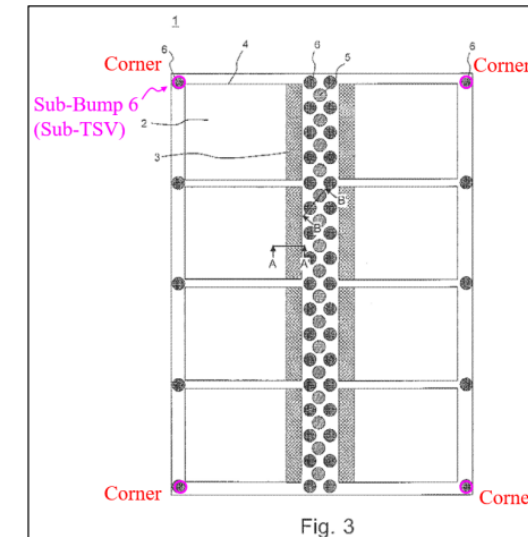
(Torii, [0048].)

Samsung's Petition

2. [1a]

.....

Thompson, ¶177. Torii discloses the sub-TSVs are used for joining adjacent semiconductor chips, so they serve as anchor points. Torii, [0083], [0090];



Torii, Fig. 3.

5. [1d]

Torii meets it because “[t]he sub-TSV is a dummy ... normally not used as a current pathway.” *Id.*, [0048]; Thompson, ¶181.

(Petition 80-81, 86.)

Torii Discloses an Embodiment Where Sub-TSV Is Not Used as Current Pathway

Torii

[0048] Note that in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.

(*Torii*, [0048].)

Samsung's Expert

28. Paragraph [0048] of *Torii* expressly teaches that the distinguishing point between the sub-TSVs and main TSVs is that the sub-TSVs are normally not used as a current pathway. Rather than using “and can,” the paragraph uses “but can” to indicate that the subsidiary current pathway is an exceptional case to the “normal” case. *Torii*'s “Summary” of the invention and claim 12 also state the

(Thompson Suppl. (Ex. 1034), ¶28.)

Torii Discloses an Embodiment Where Sub-TSV Is Not Used as Current Pathway

Torii

12. A semiconductor device comprising an electrode penetrating through a substrate, the electrode including:

a main electrode provided with a first main bump protruded from a first surface of the substrate, and a second main bump protruded from a second surface of the substrate to constitute a current pathway; and

a sub-electrode provided with a first sub-bump protruded from the first surface of the substrate and a second sub-bump protruded from the second surface of the substrate,

wherein the length of the sub-electrode, including the first sub-bump and the second sub-bump, in a substrate thickness direction is greater than the length of the main electrode, including the first main bump and the second main bump.

(*Torii*, Claim 12.)

Samsung's Expert

“normal” case. *Torii*’s “Summary” of the invention and claim 12 also state the

main TSVs are “to constitute a current pathway” but do not recite the same for the

sub TSVs. *Torii*, [0015]-[0016], claim 12. Thus, a POSITA reading *Torii*’s

disclosure as a whole would understand that the “subsidiary current pathway” is a

possible feature of the sub-TSV, but by no means mandatory. A POSITA therefore

(Thompson Suppl. (Ex. 1034), ¶28.)

Torii Discloses an Embodiment Where Sub-TSV Is Not Used as Current Pathway

HID's Expert

- A. **Torii Does Not Disclose** [1d] “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate”

136. Petitioner relies on *Torii*’s “sub-bump (sub-TSVs)” as the anchor vias. Pet., 80-81. However, *Torii* states that “The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity or the like.” Ex. 1009, [0048].

137. I understand that the Board has already found that *Torii* does not

138. A POSITA would understand that “releasing static electricity” is providing a ground connection, as static electricity would necessarily be released to ground.

139. A POSITA would therefore recognize that *Torii* provides ground connection to one or more active devices in the substrate, and, accordingly, does not anticipate any Challenged Claims.

(Berg Decl. (Ex. 2004), ¶¶136-139.)

Pet. Reply 27-29; Berg Decl. (Ex. 2004), ¶¶136-139;
Thompson Suppl. (Ex. 1034) ¶28.

Samsung's Expert

possible feature of the sub-TSV, but by no means mandatory. A POSITA therefore would understand the sub-TSV is used as a dummy (no electrical connection), or a subsidiary current pathway. That is, “not used as a current pathway” and “subsidiary current pathway” are alternative embodiments for the sub-TSVs. It is my opinion that the “not used as a current pathway” embodiment anticipates “wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate,” as claimed.

(Thompson Suppl. (Ex. 1034), ¶28.)

Torii Discloses an Embodiment Where Sub-TSV Is Not Used as Current Pathway



FMC Corp. v. Sharda USA, LLC, 145 F.4th 1326, 1334 (Fed. Cir. 2025) (“an anticipating embodiment in a prior art reference need not be the preferred embodiment”) (citation omitted).

Vicor Corp. v. SynQor, Inc., 603 F. App’x 969, 974–75 (Fed. Cir. 2015) (holding an alternative embodiment disclosed by a reference anticipates the patent claim at issue).

Construction of “on”

Claim Term	Samsung	HID
a backside metal layer “on” a bottom surface of said semiconductor substrate (all claims)	Plain and ordinary meaning — does not require direct contact	a backside metal layer “in [direct] contact with” a bottom surface of said semiconductor substrate

P&O Meaning of “on” Does Not Require Direct Contact

’826 Patent

1. A structure comprising:
at least one anchor via disposed in at least one corner of a semiconductor substrate;
a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;
a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;
wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

(’826 patent, 7:58-8:3.)



AFG Indus., Inc. v. Cardinal IG Co., 239 F.3d 1239, 1243, 1251 (Fed. Cir. 2001).

1. A transparent laminated product comprising a transparent substrate and a 5-layered transparent coating composed of a first ZnO layer formed on the substrate, a second Ag layer formed on the first layer, a third ZnO layer formed on the second layer, a fourth Ag layer formed on the third layer and a fifth ZnO layer formed on the fourth layer, and having a visible ray transmission of at least 60%, wherein the thickness of each Ag layer is from 60 to 250.

(*AFG*, 239 F.3d at 1243.)

b. “formed on”

[12] The parties dispute whether the claim language requires that each successive layer be “formed on” the prior layer in such a way that nothing is interposed between each layer. As described above, however, the court has determined that the claim language and the specification permit the presence of interlayers between layers. Notably, the claim does not state that each layer is “formed directly on” the preceding layer. Accordingly, we determine that “formed on” does not mean “directly in contact with.”

(*AFG*, 239 F.3d at 1251.)

P&O Meaning of “on” Does Not Require Direct Contact

’826 Patent - Background

increased, and continues to increase. Further miniaturization and increased density in semiconductor substrates has typically relied on a backside metal layer **attached to** the substrate to provide a common ground for the increasing number of active components on the semiconductor substrate. However, to ensure high fabrication yields the backside metal layer must remain **securely attached to** the substrate throughout the entire fabrication process and then for years during operation.

(’826 patent, 1:16-23.)

One conventional method of adhering a backside metal layer to a substrate relies on forming a backside metal stack having several layers, the first of which must form an adhesive bond with the substrate. For example, an interface layer may be **deposited on** a bottom side of the substrate followed by a thicker current carrying layer, and finally an outer packaging contact layer. However, fabrication procedures such as semi-

(’826 patent, 1:24-30.)

P&O Meaning of “on” Does Not Require Direct Contact

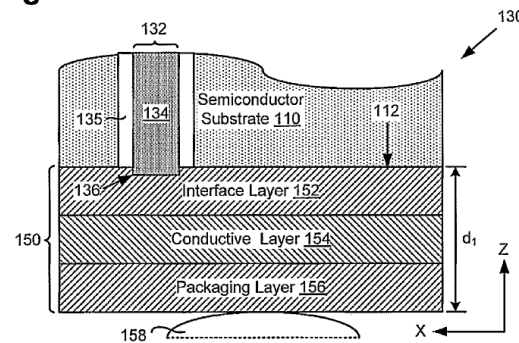
'826 Patent – Disclosed Embodiments

example. As shown in FIG. 1B, metal filler 134 may protrude from bottom side 112 to form protruding portion 136 such that when interface layer 152 is deposited on bottom side 112 of semiconductor substrate 110 the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond. Metal filler 134 may be tungsten, titanium, or any other suitable metal filler. Interface layer 152 may be formed from metals such as titanium or chrome-vanadium. Conduction layer 154 may then be formed on interface layer 152 using metals such as nickel or copper. Packaging layer 156 may then be formed on conduction layer 154 using metals such as gold or silver to provide a very low resistance contact surface. Packaging layer 156 may subse-

those concepts. Moreover, while the concepts have been described with specific reference to certain implementations, a person of ordinary skill in the art would recognize that changes can be made in form and detail without departing from the scope of those concepts. As such, the described implementations are to be considered in all respects as illustrative and not restrictive. It should also be understood that the present application is not limited to the particular implementations described above, but many rearrangements, modifications, and substitutions are possible without departing from the scope of the present disclosure.

(’826 patent, 7:45-49, 7:51-55.)

Fig. 1B



(’826 patent, 3:43-55, Fig. 1B.)

A POSITA Would Not Have Inserted HID's Unclaimed Limitations

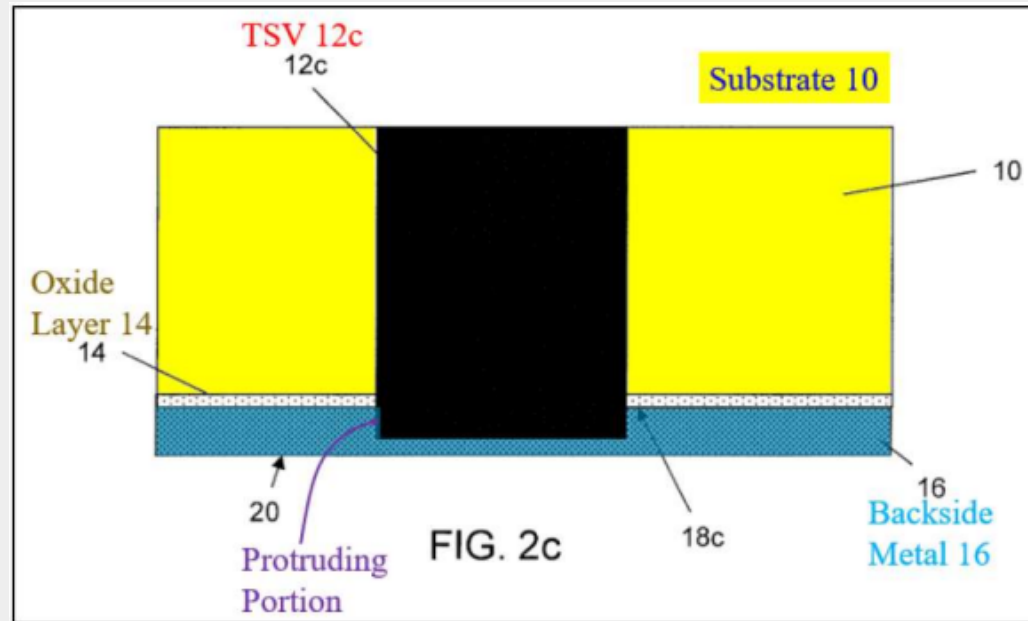
Samsung's Expert

contain an intervening oxide layer between the metal and substrate. Similarly, without additional words expressly signaling direct contact, a POSITA would understand the metal formed on a substrate allows intervening layers. The '826 specification does not use these additional words. Nor does it suggest any intent to redefine “on” from its plain and ordinary meaning. So there is no reason for a POSITA to read it as requiring direct contact. In addition, the '826 specification repeatedly cautions against using any particular embodiment to limit the claimed invention. '826 patent, 7:45-49 (“a person of ordinary skill in the art would

(Thompson Suppl. (Ex. 1034), ¶15.)

P&O Meaning of “on” Allows Both Direct and Indirect Contacts

Burnham



(*Burnham*, Fig. 2c.)

improved metal adhesion and methods of manufacture. More specifically, the present invention relates to structures and methods of forming backside metal on a Si substrate (Si wafer). In more specific embodiments, the backside metal is formed on an oxide material, e.g., SiO_x, preferably formed from a thinning process performed on the Si wafer. For example, the oxide material can be formed on a backside of a Si wafer by a grinding and polishing process, when forming a through silicon via (TSV).

(*Burnham*, 2:28-36.)

Still referring to FIG. 2c, the backside metal 16 is deposited directly on the oxide layer 14 and exposed portion of the TSV 12c. The backside metal 16 can be, for example, Ti or other

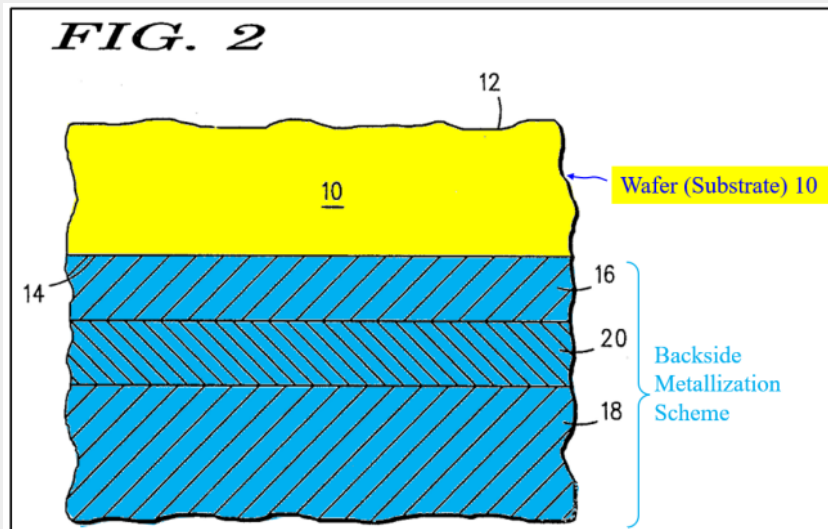
(*Burnham*, 5:1-3.)

present invention, e.g., chemical vapor deposition, etc. In embodiments, the oxide layer 14, which acts as an interface, will provide improved metal adhesion of the backside metal 16 on the oxide layer 14 (compared to conventional devices in which the backside metal 16 is formed directly on the backside of the Si wafer, after a cleaning process).

(*Burnham*, 5:8-13.)

P&O Meaning of “on” Allows Both Direct and Indirect Contacts

Sharma



(*Sharma*, Fig. 2.)

The foregoing and other objects and advantages are achieved in the present invention by one embodiment in which, as a part thereof, includes a vanadium layer disposed directly on the backside of a wafer, and a silver layer disposed on the vanadium layer. An optional intermediate layer comprised of either a mixture of vanadium and silver or of nickel may be disposed between the vanadium layer and the silver layer. It had previ-

(*Sharma*, 1:62-2:1.)

HID's Attorney Argument Contradicts the Objective Evidence

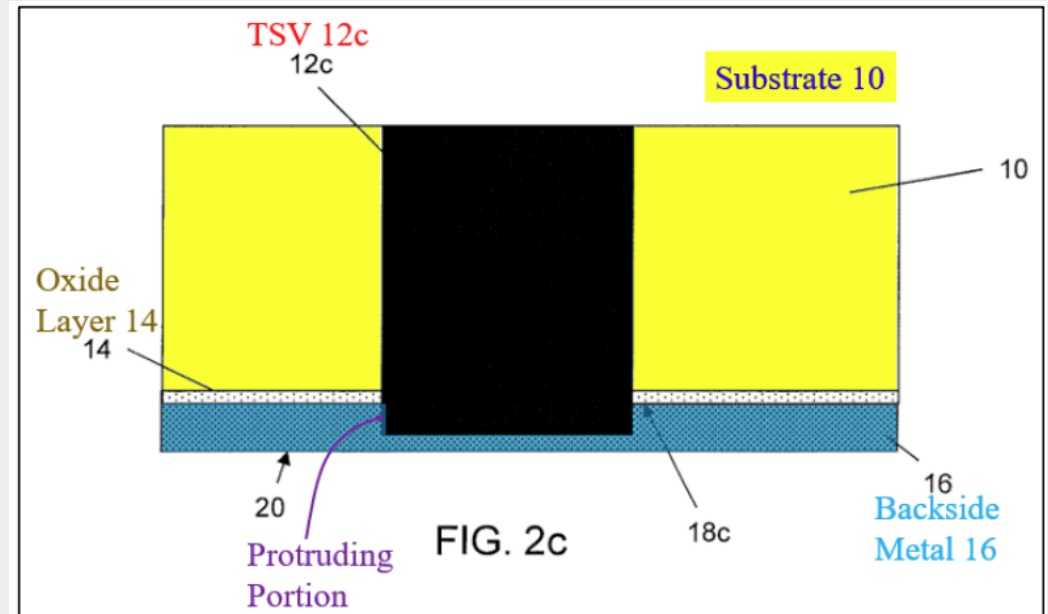
HID

The invention of the '826 Patent is thus designed to overcome insufficient adhesive qualities between the substrate and the interface layer (i.e., the backside metal layer) in these sorts of devices. *Id.*, 1:24-26, 2:44-53. It is beyond dispute that an adhesive bond between metal and substrate (*id.*, 1:24-26) requires direct contact. Otherwise, the patent would discuss the adhesive properties of some intermediate layer. The claimed anchor vias thus supplement that “adhesive bond.”

(PO Sur-Reply 4.)

Burnham

Notably, the structure in Figure 2c uses both the oxide layer (as an intermediate adhesion layer) and the TSV to improve the adhesion of the backside metal to the substrate, indicating that those skilled in the art had been combining different methods to solve the backside metal adhesion problem.



Burnham, Figs. 2c.

(Thompson Open (Ex. 1003), ¶54.)

HID's Attorney Argument Is Unsupported

Cronin). Whether a surface is a “bottom surface” is context specific. Thompson Open, ¶42. In the context of the ’826 patent claims, a POSITA would understand that the “bottom surface” refers to the surface of the substrate’s backside.

(Thompson Suppl. (Ex. 1034), ¶12.)

contact. For example, a POSITA would understand that “a first ZnO layer formed on the substrate” allows the first ZnO layer to be formed on any surface of the substrate, while “a first ZnO layer formed on a bottom surface of the substrate” specifically requires the first ZnO layer be formed on the bottom surface of the substrate (as opposed to other surfaces). A POSITA would not have read the

(Thompson Suppl. (Ex. 1034), ¶12.)

use of ‘surface’ would be irrelevant.” Berg, ¶57. I disagree. A POSITA would have understood that a metal layer can be formed on a surface of a semiconductor substrate by indirectly contacting it through an intervening layer, e.g., an oxidation layer. *See supra* (discussion of *Burnham*). This is similar to a tea cup resting on a table surface via a tea coaster, or an apple being placed on a table surface covered by table cloth. Thus, a POSITA would not have considered the use of “surface” to require direct contact.

(Thompson Suppl. (Ex. 1034), ¶11.)

HID's Attorney Argument Is Unsupported

'826 Patent

9. The structure of claim 1, wherein said metal filler within said at least one anchor via is bonded to a metal layer **overlying** said semiconductor substrate.

19. The method of claim 11, further comprising bonding said metal filler within said at least one anchor via to a metal layer **overlying** said semiconductor substrate.

(’826 patent, 8:27-29, 9:7-9.)

By contrast, a metal filler within anchor vias **132** and **133** does not provide ground connection to any active devices and instead provides physical anchor points between semiconductor substrate **110** and the **underlying** backside metal stack **150**, which may be **formed on bottom side 112** of semiconductor substrate **110** as shown in more detail in FIG. 1B. Each

(’826 patent, 3:12-17.)

Samsung's Expert

patent, 3:12-17 (emphases added). Here, the '826 patent uses “underlying” and

“on” a bottom side interchangeably. In view of that, a POSITA would understand

that “overlying” and “on” a front side are also interchangeable. Thus, a POSITA

would understand the difference between “overlying” and “on” is that overlying

specifies “on the front” without having to use the word “front,” and would not have

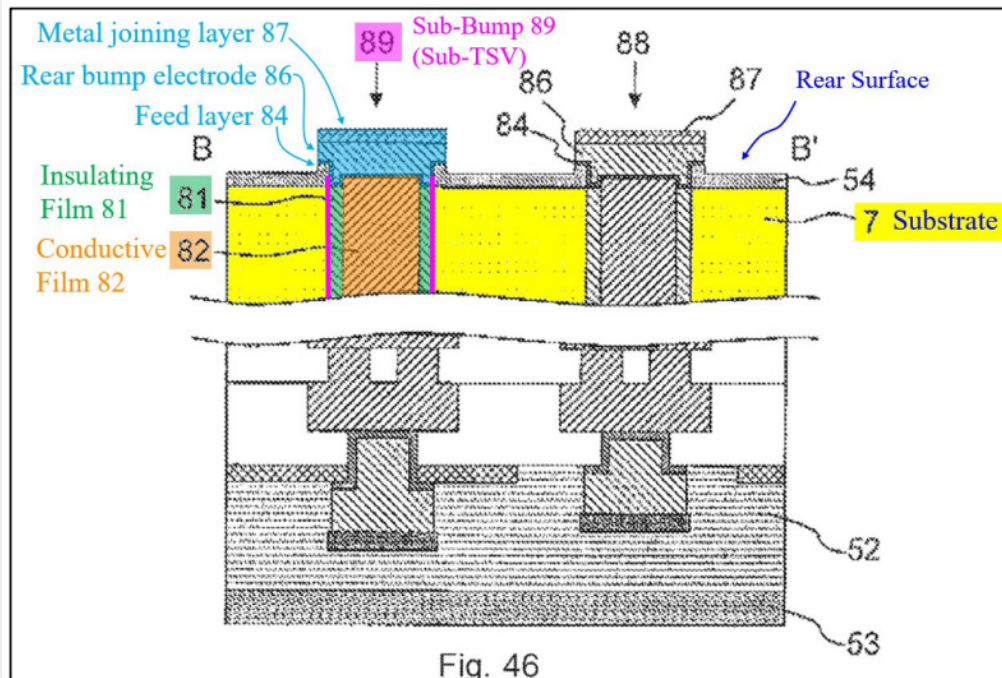
read this difference to suggest “on” is limited to direct contact.

(Thompson Suppl. (Ex. 1034), ¶13.)

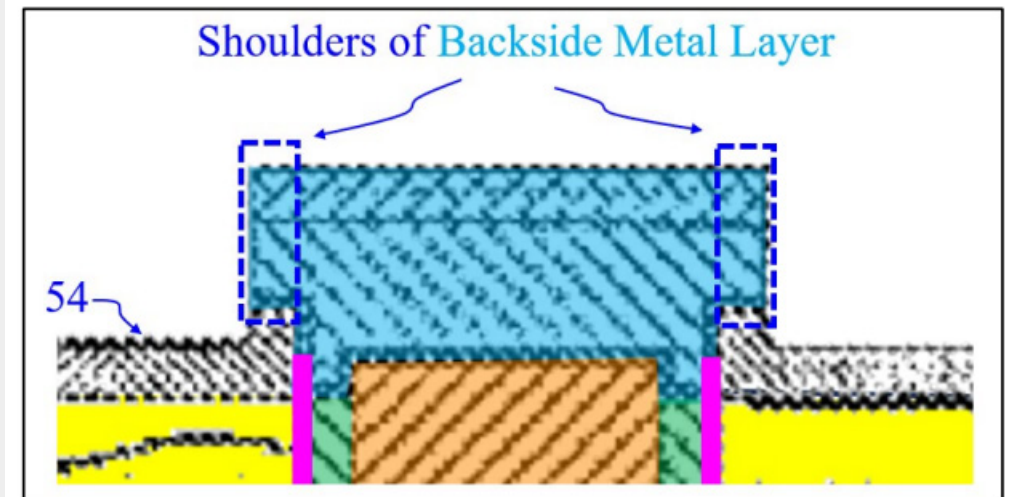
No Dispute: *Torii* Discloses “on a Bottom Surface” Under P&O Meaning

4. [1c]

Torii's Figure 46 discloses a “[s]econd feed layer 84 is formed on the rear surface” of the substrate and the protruding position of conductive film 82. *Id.*, [0100], Figs. 40-46. Notably, Figure 46 shows feed layer 84 forms a shoulder region on the substrate surface.¹² *Id.* This is a result of the fabrication process



¹² Rear-surface protective film 54 is between the shoulder region and the substrate surface. *Torii*, [0100]. But, the plain and ordinary meaning of “on” does not require direct contact, so the shoulder region is “on” the substrate surface, as claimed. *AFG Indus., Inc. v. Cardinal IG Co.*, 239 F.3d 1239, 1251 (Fed. Cir. 2001).



Torii, Fig. 46 (excerpted, zoomed).

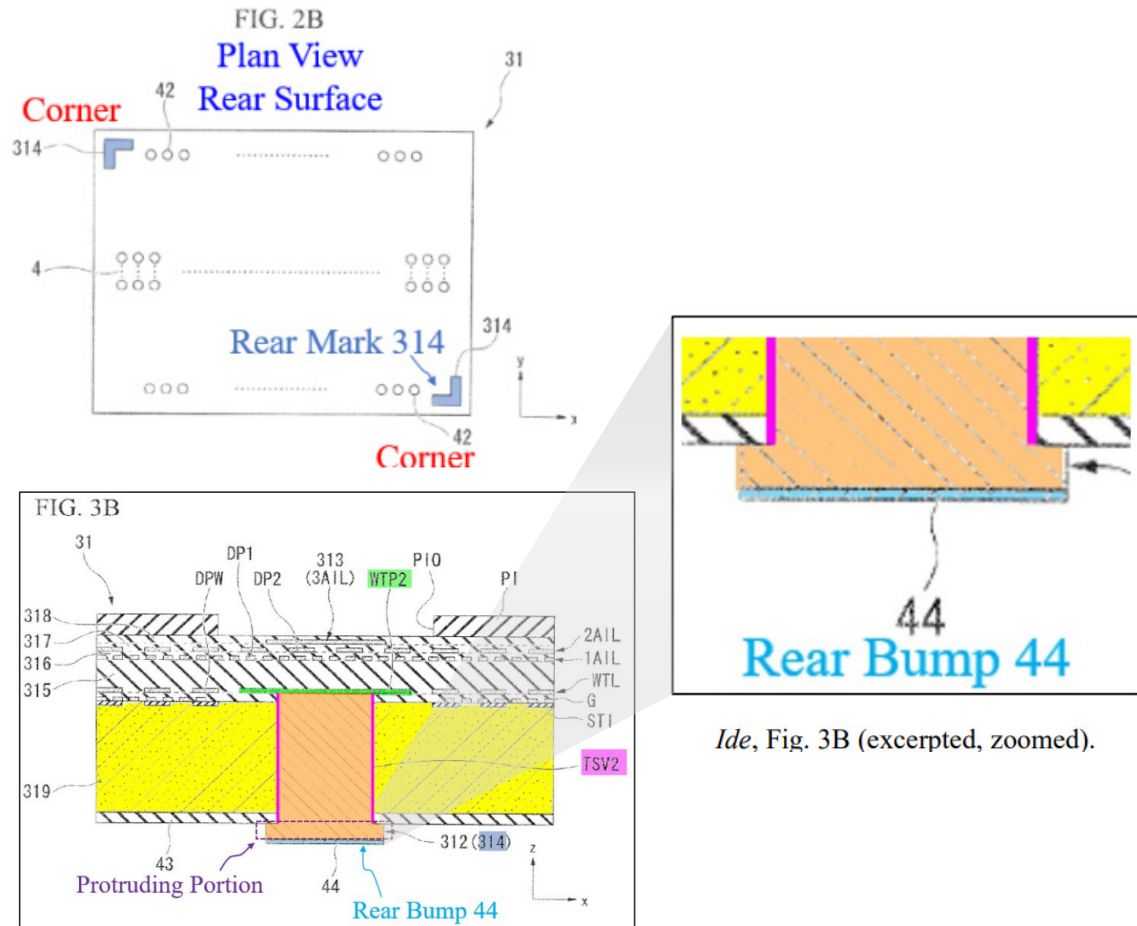
(Petition 84-85.)

Topics

- Instituted Grounds
- Technology Overview
- Ground 1: *Conn* Anticipation
- Ground 2: *Conn* Obviousness
- Ground 3: *Gambino* Obviousness
- Ground 4: *Torii* Anticipation
- Ground 5: *Ide* Anticipation

No Dispute: *Ide* Discloses “on a Bottom Surface” Under P&O Meaning

Samsung's Petition



Ide, Fig. 3B (excerpted, zoomed).

(Petition 92, 94-96.)

Samsung's Reply

VIII. Ground 5: Anticipation by *Ide*

Like Ground 4, HID argues that *Ide* does not anticipate the claimed “backside metal layer on a bottom surface of said semiconductor substrate” under its proposed construction of “on.” POR, 60-62.

For the same reasons discussed above, HID’s construction is unwarranted and *Ide* discloses this limitation under its plain and ordinary meaning. *See Pet.*, 94-96; *supra*, §VII.B.

(Pet. Reply 30.)