

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner

IPR2024-01403 (Patent 7,772,673 B1)
IPR2024-01405 (Patent 9,245,826 B2)

Record of Oral Hearing
Held: January 6, 2026

BEFORE: HYUN J. JUNG, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, Administrative Patent Judges.

IPR2024-01403 (Patent 7,772,673 B1)

IPR2024-01405 (Patent 9,245,826 B2)

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P R O C E E D I N G S

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JUDGE PESLAK: Okay, good afternoon again. We're now on the record. This is a consolidated hearing for IPR2024-1403 and 2024-1405, Samsung Electronics v. Harbor Island Dynamic. I'm Judge Peslak. I'm joined in the hearing room here in Alexandria by Judge Jung, and Judge Anderson is joining us today by video.

I'd like to start with appearances of Counsel. Counsel for Petitioner, please state your name, firm affiliation for the record, and identify anyone else who is present with you.

MR. HARDING: Good afternoon, Your Honors. This is Alex Harding on behalf of Petitioners, and I'm joined by our lead Counsel, Josh Goldberg, and my colleague, Maram Al-Shaer.

JUDGE PESLAK: Okay, thank you. Have there been any changes in Petitioners' real parties-in-interest since the last time you filed updated mandatory notices?

MR. HARDING: No, Your Honor.

JUDGE PESLAK: Okay. Patent Owner, would you please state your name, firm affiliation for the record, and identify anyone else who is present with you?

MR. COWELL: Thank you. Good afternoon, Your Honor. Richard Cowell, Fabricant LLP for Patent Owner Harbor Island Dynamic. With me is lead Counsel, Joseph Mercadante.

JUDGE PESLAK: Okay, thank you. And I'll ask you the same question. Have there been any changes in Patent Owner's real parties-in-

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1 interest since the last time you filed updated mandatory notices?

2 MR. COWELL: No, Your Honor.

3 JUDGE PESLAK: Okay, thank you. The court reporter today is
4 transcribing the hearing, please speak clearly so we can have an accurate
5 transcript. The transcript constitutes the official record of these proceedings,
6 and recording of any PTAB hearing is strictly prohibited.

7 We have the entire record, including the parties' demonstrative
8 exhibits. When you're referring to a demonstrative paper or other exhibit,
9 please do so clearly and explicitly by slide or page number. Also, pause
10 briefly after you identify it to provide us time to find it. We'll be keeping
11 track of the time for the hearing today on the clock behind me. There's a
12 public line open today, and members of the public may be listening in by
13 telephone. I'll note that neither party informed us that any confidential
14 information will be discussed today.

15 As set forth in the hearing order, this hearing will be conducted in
16 two parts. We'll first hear the parties' arguments for IPR2024-1403, then
17 we'll take a short break, then we'll hear the parties' arguments for IPR2024-
18 1405. Each side will receive 60 minutes of argument time total, including
19 any rebuttal time for each case. If there's any unused time from IPR2024-
20 1403, the time will not be carried over to the hearing for the 1405 case.
21 Either side have any questions about the procedure today?

22 MR. HARDING: None from Petitioner.

23 MR. COWELL: None from Patent Owner.

24 JUDGE PESLAK: Okay, thank you. So we'll start now with
25 IPR2024-1403. Petitioner, how much time would you like to reserve for
26 rebuttal?

1 MR. HARDING: Fifteen minutes, Your Honor.

2 JUDGE PESLAK: Fifteen minutes, okay. So you have 45
3 minutes, and you can start when you're ready.

4 MR. HARDING: Good afternoon, Your Honors. This is Alex
5 Harding on behalf of Petitioners Samsung Electronics Co., Limited, and
6 Samsung Electronics America. With me, I'm joined by our lead Counsel,
7 Josh Goldberg, and my colleague, Maram Al-Shaer. This is IPR2024-
8 01403, challenging U.S. Patent 7,772,673. At bottom, this case asks a very
9 simple question. Is it inventive to add a chamfer to a prior art isolation
10 trench when chamfered isolation trenches were already standard tools in the
11 art?

12 Moving to Slide 2. I'd like to start with a quick refresher on the
13 scope of our petition. The Board instituted on all three grounds in our
14 petition. The first was directed to all claims as obvious under the
15 combination of Yin and Koshimizu. The second was directed to Claims 1,
16 3, 5, 7 to 8, 10, 12, and 14 to 16 based on anticipation by Norstrom, and the
17 third was directed to Claims 7 and 15 based on obvious over Norstrom.

18 Today, almost everything boils down to two legal issues. For
19 Ground 1, HID's only argument is that Koshimizu is not analogous art. And
20 for Grounds 2 and 3, HID's only argument is that Norstrom's deep isolation
21 trench either does not have a plurality of chamfered trench corners or is not
22 situated in the substrate. I'd like to quickly begin with an overview of the
23 '673 Patent. Moving to Slide number 3. On the left is Figure 1 of the '673
24 Patent, what the patent admits to be a prior art semiconductor device with a
25 rectangular deep isolation trench having squared corners.

26 The patent tells us that its alleged improvement is the use of trench

1 chamfered corners on a trench surrounding a bipolar device, and that's
2 shown on the right in Figure 2. In particular, it tells us that, quote, for a
3 rectangular-shaped trench, a thick layer of polysilicon can be required to
4 adequately fill the trench with polysilicon, end quote. And so, it proposes
5 chamfering them. And states that, quote, by forming trench chamfered
6 corners to reduce trench corner width, the invention significantly increases
7 fill throughput.

8 Moving to Slide 4. The problem is that long before the March 16th
9 priority date of the '673 Patent, the art already used chamfered trench
10 corners for a variety of reasons, including for the very reason the '673 Patent
11 states, to improve trench refilling and prevent overfilling. We've presented
12 here on this slide, again, Slide 4, four examples, Norstrom IIs, Moens, and
13 Koshimizu. Norstrom and Koshimizu, of course, are presented in our
14 grounds. The others are presented as state-of-the-art.

15 Petitioner's expert, Dr. Thompson, explained that chamfered
16 corners on isolation trenches like those in these figures that we've presented
17 were standard tools to improve trench filling, among other things, exactly
18 what the '673 Patent is doing.

19 Moving to Slide 5. As I mentioned before, the '673 Patent
20 describes the problem of square corners causing inefficient filling of deep
21 isolation trenches. But Dr. Wolf, in his 1990 textbook on silicon processing,
22 said the same thing 17 years earlier. Quote, if trenches of widely varying
23 widths are used -- are filled, sorry, the narrow ones must be well overfilled
24 in order for the wider ones to be filled completely. Thus, the thickness of
25 the top surface deposited film will vary, making planarization very difficult.

26 JUDGE PESLAK: Counsel, does Wolf have an exhibit number?

1 MR. HARDING: Yes, Your Honor. One second. That's Exhibit
2 1007.

3 JUDGE PESLAK: Thank you.

4 MR. HARDING: Moving to Slide number 6. As you can see in
5 this slide, if you chamfer the square corner, you can get a width at the corner
6 that is approximately uniform across the trench. We've drawn in blue dashes
7 here on the right side where the corner used to be. This is how the '673
8 Patent proposes to address overfilling. But the problem is that this was
9 literally textbook knowledge by 2007. And, to be clear, the reason that this
10 occurs, as Dr. Thompson explains in his declaration and as Wolf explains, is
11 because the filling of the trench happens by chemical vapor deposition,
12 CVD.

13 So the filling comes in from the sides gradually and then fills up
14 over the top. So the further the sides are apart, the longer it will take to fill
15 the trenches. And if one area is wider, it will take more time and more fill
16 there while everything else overfills.

17 Moving to Slide number 7. Norstrom itself explains the same
18 thing. It explains, quote, the exterior corners of the isolating trench 257
19 have been made oblique by an angle of about 45 degrees in order to improve
20 the refilling of the trench. It appears advantageous to always form a deep
21 groove, which is to be filled with some material such as isolating or
22 conducting material to have walls which do not form corners having angles
23 about 90 degrees, but these angles should be instead as large as possible, for
24 example, 135 degrees.

25 I'd now like to move on, this is Slide 8, for Judge Anderson, to a
26 quick overview of the independent claim and then we'll get into the disputed

1 grounds, if that's okay with Your Honors.

2 Independent Claim 1 starts with a basic semiconductor die, the die
3 being, per the '673 Patent, the wafer that the device and trench are printed
4 on. HID does not dispute that any of the prior art meets this limitation.
5 Slide 9. Claim 1 then recites a deep isolation trench on that die. The patent
6 itself tells us that deep isolation trench 442 corresponds to the overhead
7 -- sorry, in the overhead view of Figure 4E corresponds to the deep trench
8 isolation 208 in the cutaway view of Figure 2.

9 HID does not dispute that any of the prior art teaches a trench,
10 although they do dispute the characteristics of the trench for Grounds 2 and
11 3. Claim 1 also recites an electronic device that is surrounded by that trench,
12 and this is Slide 10. Per the patent, the claimed electronic device may be a
13 bipolar transistor, and in fact, that is the only device that the '673 Patent
14 enumerates. The prior we rely on all involves bipolar transistors surrounded
15 by deep isolation trenches, and HID does not dispute that they meet this
16 limitation.

17 Slide 11. The only limitation that HID focuses on for its
18 arguments for Ground 2 and 3 is the at least one trench chamfered corner
19 limitation, which we've highlighted here in blue. For those grounds,
20 however, HID does not dispute that Norstrom, that's the art in Grounds 2 and
21 3, discloses a trench, but they do dispute whether the trench has both the
22 trench chamfered corners and is situated in the substrate.

23 Slide 12. Putting it all together, Claim 1 recites a semiconductor
24 die with a deep isolation trench around a bipolar device where at least one
25 corner of that trench is chamfered.

26 Slide 13. There is one other independent claim, that is Claim 10.

1 Slide 14. The only difference between Claims 1 and 10 is that Claim 10
2 recites the use of four sides to the trench. Specifically, HID does not dispute
3 that all of our prior art uses four-sided trenches. Slide 15 --

4 JUDGE PESLAK: The claims are argued together, right? Claims
5 1 and 10?

6 MR. HARDING: Correct, Your Honor. So we've previewed this a
7 little bit, but the Board only needs to resolve a few issues today. HID does
8 not dispute that chamfered isolation trenches for bipolar devices were known
9 in the art. For Ground 1, they don't dispute that our combination of Yin and
10 Koshimizu teaches every element of every challenged claim. They don't
11 dispute that a POSITA would be motivated to combine them or that they
12 would have had a reasonable chance of success in doing so. And they also
13 don't dispute that other than Claim 1's isolation trench, Norstrom meets
14 every element of every challenged claim for those grounds.

15 Slide 16. That leaves two issues. For Ground 1, the question is
16 whether Koshimizu qualifies as analogous art to the '673 Patent. Second, in
17 Grounds 2 and 3, the issue is whether Norstrom discloses a trench situated in
18 the substrate with at least one trench chamfered corner.

19 Slide 17, moving to Ground number 1. Skipping through Slide 18
20 and going to Slide 19. Koshimizu is analogous art. Under *In re Oetiker*, the
21 test from the Federal Circuit, prior art can be analogous in one of two ways.
22 Either, one, if it is from the same field of endeavor as the challenged patent,
23 and the second is if it is reasonably pertinent to a problem the inventor was
24 solving. Koshimizu, in this case, checks both boxes. It's in the field of
25 semiconductor devices and fabrication thereof. That alone would be
26 enough, but it also addresses, as part of its teachings, one of the very

1 problems the inventors of the '673 Patent said that they were facing.

2 I'd like to start with the -- or, sorry, with the field of endeavor test.

3 First, on Slide 20, the Board already correctly recited the *In re Oetiker*
4 standard and noted that the Federal Circuit has directed that the scope of
5 analogous art is to be construed broadly. Slide 22. The '673 Patent defines
6 its field broadly as, quote, the present invention is generally in the field of
7 semiconductor fabrication.

8 Slide 23. Koshimizu opens almost the exact same way, quote,
9 saying, quote, the present invention relates to a semiconductor device and a
10 manufacturing technique therefore, end quote. And it shows a deep trench
11 isolation in that device as it is being manufactured. That alone would be
12 enough.

13 The Federal Circuit explained in *Netflix* that it has affirmed this
14 Board when it has found prior art is directed to the same general field as the
15 patent being challenged. That's at 1359 on *Netflix*.

16 JUDGE PESLAK: How do you address Patent Owner's argument
17 that you've taken an inconsistent position on the field of the '664 Patent for
18 each of the different prior art references?

19 MR. HARDING: Of course, Your Honor. So there's three main
20 points. First -- and I believe you're referring to the *Gesture* case.

21 JUDGE PESLAK: Yes.

22 MR. HARDING: So *Gesture* is distinguishable, because in
23 *Gesture*, there the Petitioner had advanced, they had three pieces of prior art.
24 And for all three of them they did advance different fields, but those fields
25 were different in scope and they were different in a scope that the Patent
26 Owner was able to explain both to the Board and to the Federal Circuit as

1 excluding one of the Petitioner's prior art references. That's not the case
2 here. And if I can skip ahead just to Slide 28, those three grounds that were
3 advanced in the petition all would cover Koshimizu. So that's reason
4 number one.

5 It's distinguishable in that even if the Board were to adopt one of
6 these grounds, Koshimizu would fall into them, and HID hasn't argued that
7 they didn't. In fact, when we pointed this out in our reply, HID dropped this
8 argument entirely. *Gesture* doesn't show up in their surreply at all.

9 Reason number two, *Sanofi-Aventis* tells us that a Petitioner isn't
10 required to raise analogous art arguments until the Patent Owner puts them
11 at issue. And so, we, in effect, went above and beyond in our petition by
12 laying these out. But in our reply, we've explained that the Board's
13 institution decision field of endeavor is supported by substantial evidence
14 and it covers Koshimizu. Does that answer Your Honor's question?

15 JUDGE PESLAK: Yes.

16 MR. HARDING: Thank you. So I might just jump back. We can
17 go through these a little more quickly, because I think we've covered some
18 of these. I'm on Slide 24. Again, in its preliminary decision, the Board
19 already found that Koshimizu qualifies as analogous art under the field of
20 endeavor test, given that both it and the '673 Patent relate to, quote,
21 semiconductor devices, open parentheses, and methods of manufacturing
22 semiconductor devices, close parentheses, with a deep trench for isolating a
23 bipolar device. And HID never truly engages with the Board's reasoning.

24 So if I can go ahead to Slide 26. The Federal Circuit's explained
25 that our precedent doesn't require --

26 JUDGE PESLAK: Counsel, let me ask you -- before I forget to

1 ask this question, and this may be more related to the Norstrom ground. But
2 if you didn't have a four-sided trench, would the trench then be able to
3 perform its isolation function?

4 MR. HARDING: I think that is a -- you're asking whether, Your
5 Honor, whether a trench that had, for example, ten sides would be able to
6 electrically isolate?

7 JUDGE PESLAK: Or two sides.

8 MR. HARDING: Or two sides. It is hard to imagine for myself,
9 Your Honor, what a two-sided trench would look like in 3D space, but that's
10 certainly not something that anybody has opined on in this case. All of the
11 prior art we've relied on has been four-sided, some with chamfers, most of
12 them with chamfers. But I think the record is pretty limited to that.

13 JUDGE PESLAK: Okay.

14 MR. HARDING: Okay. Moving on to Slide 27. We can go
15 through this again quickly, because I think we addressed it a little bit earlier.
16 HID cites the recent case *Apple v. Gesture* and says this case is on all fours
17 with it, because the wording for Petitioner's field of endeavor were slightly
18 different in the petition. And it argues that because of that, as a de facto
19 matter, Koshimizu can't be analogous art. We think that that is wrong for
20 the reasons I explained earlier. I'd be happy to answer more questions if
21 Your Honors have them on *Gesture*, but recognizing that we've talked about
22 it, I can also move on. Okay.

23 JUDGE PESLAK: I don't think so.

24 MR. HARDING: Okay, I will move on, then. Moving to Slide 29.
25 We also believe that Koshimizu is analogous art given under HID's own
26 articulated field of endeavor. Specifically, it asserted that the field of

1 endeavor should be, quote, the formation of deep trench isolation regions. It
2 stated that in a few places, including on page 13 of its Patent Owner
3 response. The Koshimizu, its teachings fall within this field of endeavor as
4 well, because it discloses how to manufacture deep trench isolation 2B.

5 Specifically, at paragraph 52, moving to Slide 30, it states that in
6 an isolation region of the main surface, device-forming surface of the
7 semiconductor layer -- excuse me, 1E, a shallow isolation 2A and a deep
8 trench isolation 2B are formed. Moving to Slide 31. Koshimizu states that,
9 quote, by this isolation 2A, a plane range of an active region is defined. In
10 addition, the deep trench isolation 2B is formed by embedding, for example,
11 a silicon oxide film in a deep trench dug so as to reach the insulation layer
12 1B through isolation -- through the isolation 2A and the semiconductor layer
13 1E from the upper surface of the isolation 2A.

14 Moving to Slide 32. Koshimizu wraps up by explaining that by
15 this deep trench isolation 2B, each device in the semiconductor layer 1C is
16 completely separated electrically. So again, Your Honors, the Board's field
17 of endeavor remains unrebutted and is supported by substantial evidence.
18 But even if the Board were to adopt HID's field, the '67 -- Koshimizu would
19 still fit within that field of endeavor.

20 Koshimizu, moving to Slide 33, is also reasonably pertinent to at
21 least one problem faced by the '673 Patent, namely how to reduce overfilling
22 in a semiconductor substrate so that planarization is acceptable. The '673
23 Patent, we talked about this before, and Patent Owner described it as the
24 problem of prior art trenches requiring a thick layer of polysilicon to
25 adequately fill them. The '673 Patent states something very similar.

26 But a POSITA facing that problem would naturally look at

1 references like Koshimizu that teach forming deep trench isolation and
2 which don't use the widely varying trenches that textbooks taught made
3 overfilling problems worse, making it reasonably pertinent under *In re*
4 *Oetiker*. In particular, Petitioner's expert Dr. Thompson explained this very
5 problem, noting that chamfered corners were known to reduce the need for
6 overfilling. He cited specifically to pages 55 to 57 of Wolf. This was on
7 Slide 35.

8 Moving to Slide 36, HID's position is that Koshimizu's trench has a
9 different fill. Specifically, it is filled with silicon oxide, which has different
10 stress and electrical characteristics. But there are a couple of problems with
11 that argument, Your Honors.

12 First, HID does not dispute that overfilling was a problem the
13 inventors faced. And second, HID never ties either of these characteristics
14 to the problem of overfilling, and they never explain why either of these
15 characteristics would lead to silicon oxide being deposited in a different way
16 that would require it to have different kinds of trenches. They simply point
17 out things about silicon oxide that are different than polycrystalline.

18 In addition, Dr. Thompson had testified in his opening declaration
19 that polysilicon or silicon oxide could be used -- sorry, Your Honor, this is
20 Slide 37. And Wolf teaches that overfilling occurs without specifying what
21 kind of material. This is on page 56. Moving to Slide 38. Even more, on
22 the same page that Wolf explains that overfilling can be avoided by avoiding
23 widely varying trenches, it lists several different fill types. It lists
24 atmospheric-CVD polysilicon, again, that's chemical vapor deposited
25 polysilicon LPCVD polysilicon, and CVD silicon dioxide.

26 And it notes, again on page 56, although this isn't on our slide, that

1 with the exception of SEG, all of those materials are deposited in the same
2 way, and it shows that on page 57. So, Your Honor, there is no connection
3 between any difference in stress or electrical characteristics that HID has
4 tied to this problem, and Koshimizu's chamfered corners would be relevant
5 for the same reason that they're relevant in Koshimizu. That's all I have for
6 Ground 1. I'd be happy to move to Grounds 2 and 3, unless Your Honors
7 have any questions on this ground.

8 JUDGE PESLAK: I don't.

9 JUDGE JUNG: I have no questions.

10 MR. HARDING: Okay. So, for Grounds 2 and 3, the question is
11 whether Norstrom discloses a trench that is both situated in a substrate and
12 has at least one trench chamfered corner, and we respectfully submit that it
13 does.

14 Moving through Slide 40 and Slide 41 to Slide 42. Norstrom
15 explains that its Figures 13A and 13C show, respectively, the cutaway view
16 and the bird's-eye view of the same semiconductor device surrounded by an
17 isolation trench. In these images, Norstrom clearly --

18 JUDGE PESLAK: Counsel, before you go too far, I just want to
19 ask a couple of questions. On the right-hand side of this demonstrative, the
20 aligning of Figures 13A and 13C, this wasn't in the petition or the reply,
21 right? This is something you did for demonstrative purposes?

22 MR. HARDING: So, Figure 13C, with its highlighting in 13A, I
23 believe, are in the petition --

24 JUDGE PESLAK: No, I'm talking about stacking them up like
25 this with these lines.

26 MR. HARDING: I agree, Your Honor, that the blue crosshatches

1 were added for this demonstrative.

2 JUDGE PESLAK: Okay. So the thing I'm struggling with here,
3 maybe you can explain this, is, I realize these are patent drawings, but, for
4 mechanical -- someone who is familiar with mechanical drawing, right, if
5 they looked at 13C, where it identifies on the left edge the base contact 151,
6 it looks like from 13C that the left edge of the base contact would align with
7 the left edge of the trench, okay? And that's not what's shown in Figure
8 13A. So, that appears to be an inconsistency between these two drawings.

9 And this is something, that wasn't pointed out by Patent Owner
10 when we did the DI. But can you reconcile these two drawings? I mean,
11 obviously, Patent Owner is arguing that there's two separate trenches, one is
12 123 and one is 119. But these two figures don't appear to represent the same
13 thing. Can you address that, please?

14 MR. HARDING: Of course, Your Honor. So, I have a few points,
15 three points specifically. First, you had mentioned that you have a
16 background in mechanical. Norstrom notes that these are schematic
17 drawings in the same sense that a circuit diagram may be schematic. You
18 may remember your resistors and capacitors. It isn't necessarily to scale
19 when it's schematic, and this is not something that's specific to Norstrom.
20 It's also something that you see in other exhibits that we included in our
21 petition.

22 So, if I might skip ahead, Your Honor, I'll jump to one slide. I
23 believe it's Exhibit 1011 uses a similar setup for its cutaway versus its bird's-
24 eye view. So, I'll just jump ahead a couple of slides. And, Judge Anderson,
25 I am on Slide 53. So, if you look here, this is the '816 Patent. Again, this is
26 Exhibit 1011. It describes in its specification that the figures it shows from

1 about Figure 9 onwards are sequential steps in a manufacturing process for a
2 semiconductor device.

3 And it, too, goes from a drawing that has a particularly wide-
4 looking deep trench and a particularly narrow-looking deep trench. But it
5 does this because if you follow all the figures after 16, there's about to be a
6 bunch of stuff in the middle, and it is making room to show you all of that
7 stuff. So, it is true that --

8 JUDGE PESLAK: Can you just pause for one second?

9 MR. HARDING: Of course, Your Honor.

10 JUDGE PESLAK: Judge Anderson's having trouble hearing. Can
11 you hear me now, Judge Anderson? Okay, sorry.

12 MR. HARDING: Of course.

13 JUDGE ANDERSON: Yes, I can. I was muted, so I was a little
14 delayed there. Go ahead, Counsel. Sorry.

15 MR. HARDING: Thank you, Your Honor. I was just pointing out
16 that there are other examples of schematic drawings with respect to the
17 semiconductor die because there are so many parts. The figure has to be
18 able to show them all clearly with text, both from the bird's-eye view and
19 from the side view.

20 The next point I'd raise in response to Your Honor's question is
21 that the only time that Norstrom ever refers to element 123, it's referring to it
22 as the filling of the trench 119. It describes trench 119 as early as Figure 9
23 as being the empty deep-isolation trench that is then filled with 123. So the
24 only place, the only intrinsic disclosure in Norstrom about where 123 is, is
25 that it is filling trench 119 and that it is coextensive with it, and there's no
26 other place that is described there. Does that --

1 JUDGE PESLAK: So since both 13A and 13C are described in
2 Norstrom as schematic views, your position is that one of ordinary skill in
3 the art would understand that what's shown in those drawings wouldn't
4 necessarily align as they would, say, in a mechanical drawing?

5 MR. HARDING: It wouldn't necessarily be one-to-one in terms of
6 scale, Your Honor, but things like electrical connections would still be there.
7 So, for example, 157 and its connection between 155 --

8 JUDGE PESLAK: Well, let me make sure you understood my
9 question, though, because it's not necessarily scale. It's the fact that the left
10 edge of the base doesn't align with the left edge of the trench shown on the
11 left side of Figure 13A in 13C. So that was really my question. I understand
12 they're not to scale, and schematically maybe some resistors and electrical
13 parts shown without any kind of scale, but that was a thing that sort of
14 appeared inconsistent to me.

15 MR. HARDING: I agree with Your Honor that the alignments are
16 not necessarily one-to-one in a schematic drawing, absolutely. We believe
17 that, taken as a whole, with all of Norstrom's disclosures, a POSITA would
18 understand, as you had postulated, that because trench 123, first of all, is
19 shown both as having chamfered corners in 13C and as being in the substrate
20 in 13A without any reference to 119 at all, would understand that to be one
21 continuous trench shown in both places, even if the drawings may have
22 different alignments at a small scale, Your Honor.

23 Certainly, it's not the case that Norstrom discloses any separation
24 of any trenches. And again, it doesn't disclose that 123 goes anywhere
25 except in 119.

26 JUDGE PESLAK: Well, this also comes back to my earlier

1 question, if these are -- what Patent Owner seems to be postulating is that
2 what's shown on the left side of 13A and what's shown on the right side of
3 13A are separate trenches. Could you have isolation with two separate
4 trenches that weren't connected?

5 MR. HARDING: It does seem, Your Honor, that if there were
6 absolutely no isolating trench on the north or south side of the device, that
7 you would not have isolation. There's certainly no example of anything like
8 that anywhere in the record here. Every isolating trench must necessarily
9 surround the bipolar device. Does that answer your question?

10 JUDGE PESLAK: Yes, yes.

11 MR. HARDING: Thank you, Your Honor. And HID hasn't
12 pointed to any example of something like that. I'm going to move back a
13 few slides and just make sure I go through all of these. I am on Slide 43.
14 We've already talked a little bit about the figures. On the right-hand side, I'll
15 just note all of the disclosures that I was mentioning earlier and refer to them
16 specifically. These are presented in the same order that Norstrom presents
17 them. It notes, quote, the trenches are filled with an isolating material, 123,
18 for example, silicon oxide or polycrystalline silicon.

19 It notes the trenches, not a trench or some subset of the trenches. It
20 also notes in the second box that, quote, the trenches, the trenches 119 are
21 filled with an isolating material 123. Third, it notes that the opening of the
22 trench 119 at this side, referring to the left-hand side, is thus free from these
23 layers 129 and 131, again implying that there is another side, specifically the
24 right side.

25 And finally, it notes that the outer sidewalls of trench 123 shown in
26 Figure 13C have no right angles. That is the trench anchor corner limitation,

1 and its corners can be beveled by 45 degrees to become 135 degrees.

2 Dr. Thompson was deposed on his expert declaration supporting
3 our petition. He was asked by HID's Counsel if Figure 13A shows isolating
4 trenches. He explained that it does not. And this is Slide 44 for Your
5 Honor, Judge Anderson, I apologize. And he noted instead that Figure 13A
6 was showing a cutaway where you could see the left and the right sides of
7 the deep isolation trench around the bipolar device.

8 Moving to Slide 45, Norstrom isn't the only device that shows this
9 kind of overhead versus cutaway view. It is consistent with Koshimizu. It is
10 consistent with the '816 Patent. It's even consistent with the way the '673
11 Patent shows it. Although, as we noted, Your Honors, the '816 Patent is
12 probably the most comparable in using somewhat varying sizes for elements
13 when it's going through different steps to show them more clearly.

14 The Board recognized at institution, this is Slide 46. The Board
15 recognized at institution that Norstrom discloses the accused trench with a
16 deep isolation trench in the substrate having chamfered corners. In order to
17 rebut that preliminary finding and find for the Board, the Board would need
18 to ignore element 123 here that is both shown as being in the substrate and
19 shown as being the trench. It would need to ignore a few other things,
20 including the cutaway view being tied to the overhead view, and it would
21 need to ignore the disclosures that always tie 123 to the filling of 119.

22 It also noted in the institution decision at page 31 that Figure 13C
23 schematically shows the outlines of some of the layers. And HID has not
24 addressed that, nor have they addressed the disclosure of schematic -- or,
25 sorry, of Norstrom that explains that his drawings are schematic drawings.

26 For those reasons, we believe that Norstrom discloses every

1 element of Claim 1 as well as all of the other challenged claims that HID
2 does not dispute. And so, with that, Your Honors, I'll leave it up to you for
3 questions. If you don't have any, I'd be happy to save our time for rebuttal.

4 JUDGE PESLAK: I don't have any.

5 JUDGE JUNG: I have no questions.

6 JUDGE PESLAK: Judge Anderson, do you have any questions?

7 JUDGE ANDERSON: I have no questions.

8 JUDGE PESLAK: Okay. Thank you.

9 MR. HARDING: Thank you, Your Honors.

10 JUDGE PESLAK: So, let's see. Okay. Patent Owner, how much
11 time would you like to reserve for rebuttal?

12 MR. COWELL: I would like to reserve 15 minutes.

13 JUDGE PESLAK: Fifteen?

14 MR. COWELL: Yes.

15 JUDGE PESLAK: Okay. You have 45 minutes. You can begin
16 when you're ready.

17 MR. COWELL: Good afternoon, Your Honors. Richard Cowell
18 for Patent Owner, Harbor Island. I want to start off with something
19 Petitioner's Counsel said right at the beginning. He framed this question
20 with a question the Board is considering incorrectly. The question isn't
21 whether in some abstract, entirely universal way the claims are inventive.
22 The question is whether, before this Board, is whether Petitioner has shown
23 that the claims of the '673 Patent are obvious over the art of record and
24 should be asserted against the patents.

25 And Mr. Harding spent a lot of time on Wolf, saying, well, Wolf
26 shows this. Wolf shows that. But Wolf's not asserted prior art. Wolf's not

1 part of any grounds. Wolf is just simply not relevant to the Board's
2 consideration.

3 Now, moving to Koshimizu, and I'm on Slide number 3 of the
4 Patent Owner's slides. The '673 Patent tells us what its field of invention is.
5 And Mr. Harding showed us what I have right in the center here, the field of
6 the invention. And he read the first sentence and he did not read the second
7 sentence. And the second sentence, which says clearly, more particularly,
8 the invention is in the field of isolation region formation in semiconductor
9 substrates.

10 And immediately, the title of the patent, deep trench isolation and
11 method for forming same. All throughout the patent, the present invention is
12 directed to deep trench isolation and method for forming the same. That's
13 what this patent is about, it's about manufacturing a deep trench isolation
14 region. It's not about building a transistor. It doesn't even begin to tell you
15 how to build a transistor. It wants you to know how to build this isolation
16 region and how to fill it in a way that the polysilicon will not be overfilling it
17 in the corners.

18 Moving up to Slide 4, as the Board noted during Petitioner's
19 presentation, Petitioner never sets out a field of endeavor for the '673 Patent.
20 But it does tell us why it thinks various references are analogous art, and
21 they're different each time.

22 So Yin, it's because it's directed to a semiconductor die with a deep
23 trench isolation region that electrically isolates an electronic device, such as
24 a bipolar transistor. Koshimizu is directed to the manufacture of a silicon-
25 based bipolar transistor, employing a deep isolation region to isolate the
26 transistor from neighboring transistors. Following Norstrom, directed to the

1 manufacture of bipolar semiconductor devices, in particular bipolar
2 transistors and semiconductor diodes, which are electrically isolated or
3 confined by trenches.

4 And in each case -- give me one second. In each case, Petitioner
5 cites the exact paragraph from the '673 Patent that is set to support that
6 analogous art, which is the closest thing, as I said, to what they say is the
7 field of the endeavor. And, you know, the Federal Circuit has noted that it's
8 odd and probably not right if you're citing to the exact same passage in a
9 patent and changing the field of endeavor each time. Koshimizu --

10 JUDGE PESLAK: Counsel, to me, they kind of all sound like
11 different words for the same thing, no?

12 MR. COWELL: Well, the salient one is Koshimizu.

13 JUDGE PESLAK: Yes, let's talk about -- why don't you tell me
14 why that's different than the '673 Patent?

15 MR. COWELL: Right. So Koshimizu is directed to the
16 manufacture of a silicon-based bipolar transistor. And if we go to Slide 5,
17 that's essentially what Koshimizu tells you itself. It says the technical field
18 of the invention is applied to a semiconductor device having a hetero-
19 junction bipolar transistor and to manufacturing that semiconductor device.
20 And as I mentioned a few moments ago, the '673 Patent doesn't say anything
21 about manufacturing a transistor. It's completely agnostic as to what device
22 is being electrically isolated.

23 As we see here on Slide 5, this is an excerpt. The highlighted
24 sections are parts of Koshimizu discussing how to make a bipolar transistor.
25 It's columns upon columns, words upon words of how to do that. And if we
26 go to Slide 6 --

1 JUDGE PESLAK: Doesn't it also tell you, though, how to make
2 the isolation trench?

3 MR. COWELL: If we go to Slide 6, we see exactly what
4 Koshimizu says on the isolation trench. It is roughly two sentences, and it
5 just says put a silicon oxide, fill them in deep trench stuff, so as to reach the
6 insulation layer. It doesn't tell you anything about how to fill the isolation
7 trench. It doesn't say a word about polysilicon, and it does not -- it's just
8 something you do. It's not the focus of Koshimizu. It's not what Koshimizu
9 is directed to, and it's not Koshimizu's field of endeavor.

10 And we can see the -- Slide 7, we see the difference between the
11 two, just looking at the field of the invention paragraph. As I said, '673,
12 field of isolation region formation, Koshimizu manufacturing a bipolar
13 transistor. And the '673 Patent goes on, and this is Slide 8. And it tells you,
14 yes, I use the bipolar transistor as an example, but that's not the focus of this
15 invention. That's not the focus of this thing. It's just an exemplary device.
16 Any device could be isolated using the '673 Patent's technology.

17 Now, there's no dispute that polysilicon has different properties
18 than silicon dioxide. We put that in our Patent Owner response, and
19 Petitioner declined to cross-examine Mr. Berg on that. And therefore,
20 Petitioner simply hasn't shown why a person of skill in the art, trying to
21 solve the problem of the '673 Patent, which is how to avoid overfilling with
22 polysilicon by trenching polysilicon in the corners. Why would they turn to
23 a reference Koshimizu that just tells you how to build a transistor? It doesn't
24 make any sense, and therefore, Koshimizu is not analogous art. Unless the
25 Board has any questions, I'll move to Norstrom.

26 JUDGE PESLAK: Well, if you have -- Koshimizu is also -- I

1 understand the end result of Koshimizu is a semiconductor with a trench and
2 a bipolar transistor in it, right? And it seems like that's also the end result of
3 what's in the challenged patent. So why would it be at least reasonably
4 pertinent? Why would Koshimizu not be reasonably pertinent?

5 MR. COWELL: Because Koshimizu is not solving the same
6 problem. It has to be reasonably pertinent to the problem faced by the '673
7 Patent inventor, which is how to avoid overfilling a trench with polysilicon.
8 And it's about manufacturing that particular trench. Koshimizu is about
9 manufacturing a transistor. It doesn't tell you how to avoid overfilling the
10 trench. It doesn't tell you anything about polysilicon.

11 And the *Gesture* case, which Mr. Harding mentioned, which was
12 decided after the institution decision here, the field of -- excuse me. The
13 field of invention there, there were three different fields of invention, just
14 like there were here, and they're all related to portable camera systems. But
15 it was the details that mattered. One camera system was gesture-controlled,
16 and the other ones were captured image-controlled. And so, you still ended
17 up with a portable camera system, but there were not analogous art. Can I
18 answer any further questions on Norstrom -- on Koshimizu, Your Honor?

19 JUDGE PESLAK: I don't have any more. Do you?

20 JUDGE JUNG: Just one question. So, Mr. Harding put up a quote
21 from the Federal Circuit saying the analogous art is supposed to be applied
22 broadly, correct? So if we are persuaded by your argument, is that still
23 applying the analogous art test broadly? It seems like we're kind of
24 narrowing it down a little bit.

25 MR. COWELL: I mean, that's a tough question to answer,
26 broadly, by itself, doesn't really tell us what that means. And you could say

1 any two things are the same, and then you're applying it broadly, even if you
2 have a notepad and, I don't know, a pencil or a computer.

3 JUDGE JUNG: Okay. Let's say that that word broadly, you
4 know, it can be applied to the reasonably part of reasonably pertinent. So if
5 we construe reasonably pertinent to be the broad application of the art in
6 front of us, it seems like Koshimizu would fall within that reasonably
7 pertinent prong of the test. What's the one thing or what's your argument
8 that would take it out of a broad reading of reasonably pertinent?

9 MR. COWELL: I think it's the argument I made a few minutes
10 ago. It's that Koshimizu, yes, they're both about semiconductor devices, and
11 I believe that's Petitioner's main argument there is that everything's about
12 semiconductor devices. So that's all we have to look. We don't have to look
13 further. But they're not about the same problem.

14 JUDGE JUNG: Okay.

15 MR. COWELL: The problem is about electrical isolation and
16 building an electrically isolating deep trench with polysilicon. That's the
17 specific problem. It's what the '673 Patent inventor calls out as the problem.
18 And that's not the problem faced by Koshimizu.

19 JUDGE JUNG: Okay. Let me just put it a different way. Since
20 both the patent and Koshimizu end up in the same place, the same
21 semiconductor device, wouldn't it be -- doesn't it seem it would be at least
22 pertinent, even if it doesn't address the exact problem you're looking for? It
23 does get you to the same place, so you might consider it as a reference.

24 MR. COWELL: I mean, obviously, I disagree that it would get
25 you there. You can't just look at the end result and decide, okay, they look
26 kind of the same, so it's reasonably pertinent. And that just basically moves

1 the analogous art test completely away from any moorings. You have to
2 look at what tries to be solved, and you have to look at the steps you would
3 take to solve the problem. Koshimizu doesn't have any of the steps you
4 would take to solve the problem. And because it doesn't have those steps, it
5 can't be reasonably pertinent in my view.

6 JUDGE JUNG: Okay. Thank you.

7 MR. COWELL: Moving on to Norstrom. Mr. Harding put up a
8 slide, and I want to put up my response to that slide, which is Slide 16 of
9 Patent Owner's demonstratives. Norstrom describes in detail where trenches
10 119 are placed. And through column 10:32-56 is where he specifically sets
11 out exactly where they're placed. And I can show it here in the picture, and
12 then we'll go back and I'll look at the column itself.

13 The trenches are under -- the trench on the right side basically lines
14 up with the recess for the contact collector, at least on the right-hand side of
15 it. It's not, as Petitioner is saying, this huge swimming pool that fills the
16 entire chip. It's this one narrow region that fits under there. And it's not
17 -- this isn't a scaling issue. This isn't, oh, it's 2 millimeters here, a
18 micrometer there. This is where it tells you where it puts it. And 13A and
19 13C are just incompatible for that. They have to be talking about different
20 structures.

21 JUDGE PESLAK: Let me ask you the same question I'd asked
22 Petitioner's Counsel, which is if there's two trenches like that, how could
23 they perform their function of isolating the bipolar transistor?

24 MR. COWELL: It's depending on what you're isolating it from.
25 Something on the other side of that trench would be isolated. There's a
26 blockage between them and there's no electrical contacts around them.

1 JUDGE PESLAK: Is there anything in Norstrom that tells us
2 specifically what those two -- what you are claiming are two trenches,
3 specifically what those two trenches would isolate?

4 MR. COWELL: I don't believe Norstrom explains what's being
5 isolated. It certainly doesn't -- I don't believe there's anything in the record
6 about whether the trenches shown, 119, would or would not be isolating.
7 Because Norstrom says they are, I believe they would be, and they probably
8 should be presumed to be isolating.

9 So if we look at Slide 12, now we're looking at column 10 of
10 Norstrom. And it talks about the collector hole 157. And it tells us the
11 collector hole has one of its sidewalls in direct contact with the endoped
12 epitaxial layer 107, which we can see right here on the slide. It's highlighted
13 in blue. And the bottom diffusion layer. It has its opposite sidewall located
14 against the inner material in the trench. It's located against the trench. It's
15 not located all the way off to the edge as it shows in 13C.

16 It goes further to tell us that the other two sidewalls, i.e., the north
17 and south sidewalls, or up and down, however you want to put them, are
18 lined against the inner material of the trench themselves. So the trench has
19 to match with the collector hole. The collector hole's north and south
20 sidewalls and what are called the opposite sidewall all have to be lined up
21 with the trench. And that's not shown.

22 We go to Slide 13. You can see, what does that come up with?
23 That comes up with what's layered here in pink and purple. You can see the
24 north sidewall, that's the edge of the collector hole. The south sidewall,
25 that's the other sidewall of the collector hole. And, of course, the opposite
26 sidewall is under the collector contact. It's not all the way over to the end.

1 The only portion of Norstrom that even calls 123 the trench is this single line
2 at 16, 39, 42. The outer sidewalls of the trench shown in Figure 13C. That's
3 the trench 123. That's not trench 119. It's just the trench shown in Figure
4 13C.

5 It cannot match the geometry of the trenches shown in 13A. It's
6 not a matter of scaling. It's not a matter of anything else. It's just not
7 possible for the trenches in 119 to match up with the collector hole as they're
8 described as doing so in detail, and also what Petitioner calls trench 123.

9 JUDGE PESLAK: You do agree that Norstrom also describes 123
10 as the material that fills the trench 119, correct?

11 MR. COWELL: Yes, Norstrom uses 123 as the filling material for
12 the trenches 119. It doesn't explain why it suddenly changes 123 to trench
13 as opposed to filling material. It doesn't say 123 as part of 13C is the filling
14 material of trench 119. It's just calling 123 a different trench. And I think
15 Petitioner made the same point in its briefing. The numbers don't have to be
16 consistent between figures, and I think there were some errors in numbers
17 between figures. And so the fact that they reused 123 for this separate
18 trench is not dispositive of any issue.

19 JUDGE PESLAK: So your argument here is what I was
20 discussing with Petitioner's Counsel that if you look at these drawings as
21 mechanical drawings, the parts don't line up.

22 MR. COWELL: Correct.

23 JUDGE PESLAK: And Petitioner's Counsel was saying, well, one
24 of ordinary skill in the art would be, I guess, an electrical engineer, not a
25 mechanical engineer, and they would see schematic and from that they
26 noticed the elements wouldn't necessarily line up between those two

1 drawings. So what's your response to that?

2 MR. COWELL: My response to that is, I don't believe they made
3 that argument in their briefing, but it also doesn't make a lot of sense. It's
4 not something's blown up and they're slightly different scales. These are
5 completely incompatible arguments. People have worked as engineers and
6 I've worked as an engineer. You expect the drawings to make sense
7 consistently between the two of them. And looking at that, looking at
8 Norstrom's disclosure of trenches 119 used always in the plural.

9 And the specific description of how they are aligned with the
10 contactor holes and the other holes, you take all those things on one side and
11 then you look at the picture 123, 13C, trench 123, there's no way a person of
12 skill in the art would conclude that they were the same trench.

13 JUDGE PESLAK: But if you look at the right side at Figure 13A,
14 what's shown there in pink, I guess, is labeled both 119 and 123. So
15 shouldn't that be the same thing then, 123 and 119, for what's shown in
16 Figure 13C?

17 MR. COWELL: Figure 13A, 123 is described as the filling
18 material, not the trench itself. Figure 13C, to the extent it says anything, it
19 says it's a trench. It doesn't say it's the filling material of the trench. It
20 seems clear -- it's the clearest conclusion I think one would come to, is that
21 they were just talking about two different things at that point.

22 JUDGE PESLAK: So is the -- what's clearly labeled as the 123
23 trench in 13C, where is that shown in Figure 13A?

24 MR. COWELL: It's not shown in 13A. But there's numerous
25 features of 13A that aren't shown in 13C, and there's features of 13C that
26 aren't shown in 13A.

1 JUDGE PESLAK: So --

2 MR. COWELL: For example, 156, the collector contact, is not
3 shown in 13A.

4 JUDGE PESLAK: So, do you agree that what's shown in 13C as
5 trench 123 has chamfered corners, correct?

6 MR. COWELL: Yes, what's shown in 13C does have chamfered
7 corners.

8 JUDGE PESLAK: Okay. So why doesn't that trench that's shown
9 in 13C meet the claim limitation?

10 MR. COWELL: Because the other claim limitation that's at issue
11 is the trench that is, and I don't have the language directly in front of me, is
12 situated in the substrate. It has to be a deep trench, which means it goes all
13 the way down to the substrate. 13C doesn't show a trench going down to the
14 substrate. 13A trenches may go down to the substrate, but the 13C trench
15 does not. It probably, it seems to be a shallower trench.

16 JUDGE PESLAK: How can you determine that from 13C it's a
17 shallow trench?

18 MR. COWELL: You can't determine one way or the other, I think.
19 It doesn't tell you how deep it is, and there's no reason to think it goes down
20 to the substrate because it never says a word about it going down to the
21 substrate. I think the parties agree that Ground 3 rises and falls with Ground
22 2. So unless the Board has any further questions, I'll reserve my time.

23 JUDGE PESLAK: I don't have any questions.

24 JUDGE JUNG: No questions.

25 JUDGE PESLAK: Okay. Judge Anderson, do you have any
26 questions?

1 JUDGE ANDERSON: I do not.

2 JUDGE PESLAK: Okay.

3 MR. COWELL: Thank you, Your Honors.

4 JUDGE PESLAK: Okay. So, Petitioner, you have 15 minutes for
5 rebuttal. You can start when you're ready.

6 MR. HARDING: Thank you, Your Honor. I would just like to
7 address a couple of points in Grounds 2 and 3, unless Your Honors have any
8 questions about Koshimizu or Ground 1 first before I do that.

9 JUDGE PESLAK: I do not.

10 JUDGE JUNG: No questions.

11 MR. HARDING: Okay. I'd like to just address a few points that
12 Counsel for HID raised, specifically in your last line of questioning, Judge
13 Peslak. You noted, as we believe as well, there is no dispute, and HID's
14 Counsel admitted this, that Figure 13C shows a trench, and that trench is
15 chamfered. So then the only question left for whether or not that trench is in
16 the substrate is whether -- sorry, the only question remaining is whether that
17 trench is in the substrate.

18 And on Slide 46 in 13A, Norstrom shows in 13A that 123 is indeed
19 penetrating all the way down to the very bottom of the silicon, which is the
20 substrate. So in order to find for HID, the Board would have to adopt HID's
21 argument that Norstrom is simply wrong. It's wrong when it shows 123 is
22 there, and it's wrong when it states that Figure 13A is the cutaway view of
23 13C. Their argument is that there must be some mistake, there must be
24 some typo, because that's how it's shown.

25 And their argument goes even further than that because they argue
26 a POSITA looking at these figures would immediately determine that there

1 is a typo and draw figures, draw trenches in the same way that they drew it,
2 even though those aren't shown in the figure, and even though, as Your
3 Honor pointed out, that would leave the north and south side completely
4 exposed and isolated.

5 And finally, Counsel stated that Norstrom, quote, never says a
6 word about 123 going into the substrate. That's wrong for a few reasons.
7 One, figures can be considered for everything that they disclose. The
8 Federal Circuit has instructed that repeatedly. But also, again, the only time
9 that Norstrom describes 123, it describes it as being the filling for trench
10 119, and trench 119 is explicitly described, even in the text, as going into the
11 substrate. So we do believe that it says quite a bit about 123 going into the
12 substrate.

13 Finally, if you accepted HID's argument, you would have to
14 believe that 13A doesn't show anything about this 123 trench in 13C. My
15 Counsel on the other side couldn't answer Your Honor's question about 123
16 being narrow or being shallow or deep. If it were shallow or deep, it should
17 still show up in 13A and yet, according to opposing Counsel, it does not.
18 We submit that it does show up in 13A. It shows up right where it's shown
19 here. 123 is pointing to the filling of that trench and it is the same trench.
20 That is all I have, Your Honors, unless you have any questions.

21 JUDGE PESLAK: I don't.

22 JUDGE JUNG: No questions.

23 JUDGE ANDERSON: Judge Anderson, any questions?

24 JUDGE ANDERSON: No questions.

25 MR. HARDING: Thank you, Your Honors.

26 JUDGE PESLAK: Thank you. Patent Owner, you have 15

1 minutes. You can start when ready.

2 MR. COWELL: So I have up Slide 42 from Petitioner's slides.

3 And what Mr. Harding just said is, to believe Harbor Island, you'd have to
4 believe that Norstrom is wrong. But Norstrom is wrong. He's saying
5 Norstrom is wrong in his argument right here where he shows the alignment
6 of the trench in 13A aligning with the outside of the trench in 13C. And as I
7 showed this board just a few minutes ago, they can't do that. They do not do
8 that.

9 They match with the collector hole, which is a different structure
10 that is shown in 13C. And if there's an inconsistency or an error in this art, it
11 has to be held against Petitioner. It's Petitioner's burden to show these
12 claims are obvious. They can't show that these claims are obvious with art
13 that doesn't make any sense.

14 And finally, Petitioner says, Norstrom does tell us that 123 is into
15 the substrate. It tells us the filling material of trenches 119 is into the
16 substrate. If you assume that filling material 123 and trench 123 have to
17 mean the same thing, which is against all evidence within Norstrom,
18 including column 10, where it describes exactly where trenches are placed
19 and where the filling material is entered, that simply is inconsistent with the
20 evidence and cannot support any finding of obviousness. And with that, I'm
21 done, unless you have any questions for me.

22 JUDGE PESLAK: I don't have any further questions.

23 JUDGE JUNG: No questions.

24 JUDGE PESLAK: Judge Anderson?

25 JUDGE ANDERSON: No questions.

26 JUDGE PESLAK: Okay.

1 JUDGE ANDERSON: So let me just ask you something.

2 JUDGE PESLAK: Sure.

3 JUDGE ANDERSON: What's your best argument, Counsel, that
4 13C and 13A are different in some way? For the grounds --

5 MR. COWELL: Yes, I'm just putting up my slides again. So just
6 give me one moment, if you would. My best argument, if I could sum it up,
7 is Norstrom requires -- excuse me, not Norstrom -- is the '673 Patent
8 requires a trench situated in a substrate that has a trench chamfered corner.
9 And the disclosure of Norstrom, specifically column 10, round 48 to 56,
10 which describes where trenches 119 are as opposed to Figure 13C which
11 describes where trench 123 might be, are so fundamentally inconsistent that
12 you cannot apply any description of how trenches 119 going into the
13 substrate could apply to trench 123. And without that, it cannot anticipate
14 the claims, because you do not have one trench that meets both those
15 limitations.

16 JUDGE PESLAK: Let me ask one further question while we're on
17 this slide, just so I understand. So what we see here is that your expert, I
18 assume it's your expert who did this drawing, or Patent Owner, colored in a
19 box here on Figure 13C. And if I look at the original, it appears that he or
20 she, I guess it's a he, used the left side of what's shown as trench 123 in
21 Figure 13C, and then the right side of this recess of 157, which is the broken
22 line.

23 What's the basis for picking out that stripe? Because it's not -- that
24 doesn't show something that's shown in Figure 13C. You've sort of picked
25 out two different things there. So explain to me why the left side would be
26 the right side of what's the square that's labeled 123 trench, and the right side

1 would be the right side of this broken box that's the recess for collector
2 connection.

3 MR. COWELL: Sure. So I went to Slide 15 because I think it
4 shows it a little better. And if we see in 13A, the recess for collector
5 connection 157, which is described consistently between those two figures,
6 we see that the trench on the right-hand side lines up almost precisely with
7 that sidewall, with the sidewall of that recess, as it's described in column 10.
8 The left-hand side matches up with a portion under there, which is, it's not as
9 clear, I agree. But the right-hand side is very clear where it lines up. And
10 that's how the expert picked it.

11 JUDGE PESLAK: Right. Because what you've shown in Figure
12 13A is the left side of either 119 or 123 doesn't line up with 157 on that side.
13 Do you agree with me?

14 MR. COWELL: That's correct.

15 JUDGE PESLAK: All right. I don't have anything else.

16 MR. COWELL: Thank you.

17 JUDGE PESLAK: So we're done with the 1403 case. Why don't
18 we take -- it's 2:05 Eastern Time. 12:05 Mountain Time for Judge
19 Anderson. So why don't we take a ten-minute break and come back at 2:15
20 and we'll do the 1405 case.

21 (Whereupon, the above-entitled matter went off the record at 2:06
22 p.m. and resumed at 2:14 p.m.)

23 JUDGE PESLAK: Okay. Please be seated. Okay. So we're back
24 on the record. We're now going to hear argument for IPR2024-01405.
25 Petitioner, how much time would you like to reserve for rebuttal?

26 MR. SAIDMAN: Your Honor, if I may just clarify the procedure

1 for reserving the time.

2 JUDGE PESLAK: Yes.

3 MR. SAIDMAN: I saw in the first hearing --

4 JUDGE PESLAK: Yeah, I know. I made a mistake.

5 MR. SAIDMAN: Okay. Your Honor, we'll reserve 15 minutes.

6 Thank you.

7 JUDGE PESLAK: Sorry about that. If you needed more time, I
8 would have given it to you. And we have new people at the Counsel table
9 here. Were you introduced before?

10 MR. SAIDMAN: Yes, Your Honor, Ben Saidman on behalf of
11 Petitioner Samsung. I'm joined by my Co-Counsel, Mr. Chen Zang, who
12 will be sharing an argument with me today. And lead Counsel, Joshua
13 Goldberg, is here as well.

14 JUDGE PESLAK: Okay. We did hearings virtually and I was
15 keeping track on my phone. It was easier than using this thing. So anyway,
16 Petitioner, you have 45 minutes and you can start when ready.

17 MR. SAIDMAN: Thank you, Your Honors. Good afternoon. If
18 you would turn to Slide 6, just as a matter of housekeeping, go over the
19 instituted grounds. So I'm going to handle Grounds 1 and 2 today, and my
20 Co-Counsel, Mr. Zang, will handle Grounds 3-5.

21 If you turn to Slide 13, there are two disputed issues for Ground 1.
22 There's one issue for Independent Claims 1 and 11, that is whether the prior
23 art Conn reference discloses at least one anchor via disposed in at least one
24 corner. This is nominally presented as a claim construction issue. But as we
25 discussed in our briefing and we can discuss here today, ultimately whether
26 the Board adopts Petitioner's plain and ordinary meaning or HID's narrower

1 construction, Conn still discloses at least one anchor via disposed in at least
2 one corner.

3 The second dispute is for Dependent Claims 9 and 19. So the
4 claim language is said metal filler within said at least one anchor via is
5 bonded to a metal layer overlying said substrate. But the issue seems to
6 come down to if you have a via conductor or an anchor via that extends
7 between two conducting layers, does it necessarily provide ground
8 connection to an active device? And our position is no, it does not, and
9 that's supported by more than substantial evidence.

10 If you turn to Slide 14, you can see the parties' claim construction
11 positions for what it means to be disposed in a corner. So Samsung's
12 position is that the term should be afforded its plain and ordinary meaning in
13 that it -- excuse me. Disposed in a corner means disposed in a distance
14 proximate to a corner of a semiconductor substrate, and we believe this is
15 supported by the intrinsic evidence. And as you can see, HID's construction,
16 much narrower construction, located outside around or ovoid geometrical
17 shape inscribed within the edges of the semiconductor die.

18 So if you turn to Slide 15, you can see here a portion of the
19 evidence from the specification discussing how the anchor vias are located
20 in a corner. On the left-hand side, you can see how the patent talks about
21 anchor vias may be fabricated proximate to a corner of the substrate, and
22 you can see here in Figures 3A, 3C, 3D, and 3E, you have anchor vias that
23 are in a corner. There's no disclosure of a precise distance. It just says
24 proximate to a corner. And notably here, there are no ovoid or other circular
25 inscriptions separating out the corner from not the corner.

26 Now, the patent also discusses how the anchor vias may be formed

1 at a predetermined distance from the corner, and that distance may vary
2 depending on a particular application.

3 So if you go to Slide 17, there's more than substantial evidence that
4 Conn discloses disposed in a corner under its plain and ordinary meaning.
5 So the focus of our evidence here is Figure 2. So what does Figure 2
6 disclose? Figure 2 shows a copper plane 20. And what we understand from
7 Conn is that this copper plane is approximately coextensive with the carrier
8 substrate. There doesn't appear to be an argument to the contrary on the
9 record on this.

10 And you can see in orange these anchor vias in a grid like pattern
11 over the substrate. And what Conn says, this is in the abstract and also in
12 paragraph 11, that these anchor vias are along the length and along the width
13 of the majority of the substrate. But what's important here for Figure 2 is
14 you see 12 anchor vias in this figure, but that's just exemplary, right?

15 So if you turn to Slide 18, this is Conn at paragraphs 35 and 36. So
16 what it says is other patterns are permissible. You can have a distance
17 between the via conductors at 60 or to 1,000 micrometers. The density can
18 be uniform across the entire conducting layer, and the number of via
19 conductors can be 5,000, 100,000, 200,000, depending on the size of the
20 carrier substrate in the conducting layer. All that is to say that because Conn
21 discloses this high-density grid pattern, it necessarily discloses an anchor via
22 disposed in at least one corner.

23 Now, if you turn to Slide 20, you can see here on the left-hand side
24 of the screen, it's a graphical depiction of HID's construction. But there's no
25 indication of the intrinsic or the extrinsic evidence.

26 JUDGE PESLAK: Counsel, can you go back to Slide 19 for a

1 minute? This blow-up or enlargement that you have in the corner, this isn't
2 something that's specifically in Conn, right?

3 MR. SAIDMAN: That's correct. That was generated by our
4 expert, Your Honor.

5 JUDGE PESLAK: Okay. Just wanted to make sure.

6 MR. SAIDMAN: So if we go to Slide 20, there's no indication that
7 the inventors intended to act as their own lexicographers and provide a
8 unique definition for what it means to be disposed in a corner. Again, on the
9 right-hand side of Slide 20, you can see other examples of anchor vias in the
10 patent. And in each of these, you have anchor vias disposed in a corner, but
11 there's no circular or other ovoid shape.

12 Now, the Patent Owner relies heavily on extrinsic evidence,
13 Exhibit 2007 and Exhibit 2008. Those are the subjects of our motion to
14 exclude. But irrespective of how the Board rules on that motion, those
15 exhibits simply do not support this narrower construction. There's nothing
16 in those exhibits that indicates a unique definition to what it means to be
17 disposed in a corner. Instead, those exhibits show exemplary delamination
18 patterns.

19 But even if you look at exhibit -- excuse me, Slide 23, this is
20 Exhibit 2008, and you can see in the upper left-hand corner that this red
21 circular shape has been added by Patent Owner. But even there, the
22 delamination pattern goes into and inside of that circle.

23 JUDGE PESLAK: Is this where you're talking, in the upper left
24 corner?

25 MR. SAIDMAN: I'm sorry?

26 JUDGE PESLAK: When you say the delamination pattern goes

1 into the circle, so you're referring to the upper left corner?

2 MR. SAIDMAN: Yes. Correct, Your Honor.

3 JUDGE PESLAK: Okay.

4 MR. SAIDMAN: And Patent Owner's response has been, well,
5 yes, the delamination goes into the circle, but that would be corrected by
6 anchor vias located outside the circle. But there's no basis for that in the
7 record. There's no basis for that in Exhibit 2008 or Exhibit 2007 or the
8 patent itself.

9 Now, if you go to Slide 24, as I mentioned earlier, even if the
10 Board were to adopt Patent Owner's narrower construction because Conn
11 discloses this high-density grid, there would still be at least one anchor via,
12 if not more, disposed in a corner under even Patent Owner's own
13 construction. So, unless there are further questions on Claims 1 and 11, I'm
14 happy to turn to Claims 9 and 19.

15 JUDGE PESLAK: I don't have any questions.

16 JUDGE JUNG: I don't have any.

17 JUDGE PESLAK: Judge Anderson?

18 JUDGE ANDERSON: No, I don't have any. Thank you.

19 MR. SAIDMAN: Thank you. So, if you turn to Slide 26, Claim 9
20 depends from Claim 1, and it adds a limitation of this metal filler that's
21 bonded to a metal layer overlying the substrate. And so what we show here
22 on the slide is how we mapped Conn to this claim in the petition. So you
23 can see a copper plane 30 connected to a copper plane 20 by what's called
24 here as copper rivets 14, also called via conductors or anchor vias.

25 Now, Patent Owner's argument appears to be that if you have a via
26 conductor that extends between these two planes, it necessarily provides a

1 ground connection to active devices. But that's not supported by the record.
2 So if you go to Slide 28, this is Conn disclosure.

3 So at the bottom in paragraph 38, Conn repeatedly says, this is one
4 example, layers 20 and 30 are mechanically connected by at least one via
5 conductor. There's no disclosure of an electrical connection. Instead you
6 just have repeated disclosures of a mechanical connection. And then above
7 on the slide, you have Conn from paragraph 28, and it says the via conductor
8 does not necessarily have to go all the way through the via.

9 And as Samsung's expert Dr. Thompson explained, that if the via
10 conductor does not need to go all the way through the via, then it wouldn't
11 be designed to provide an electrical connection to any active devices. But
12 what's notable here, if you go to Slide 30, Conn is not unique in disclosing a
13 via conductor that extends entirely through the substrate that doesn't provide
14 a ground connection to any active devices. We have multiple examples in
15 the petition of pages 10 to 13 and two of them are here on the slide. We
16 have the Wang reference on the left and the Nishio reference on the right.

17 JUDGE PESLAK: But this is an anticipation ground, right?

18 MR. SAIDMAN: That's correct. Because it's to show Your Honor
19 that this understanding and reading of Conn is not far-fetched or
20 unreasonable, right? It's that how one of ordinary skill in the art would have
21 understood Conn's disclosure is reasonable and consistent with other art
22 known to one of ordinary skill in the art, not that Conn should be read any
23 differently because of what Wang and Nishio disclose.

24 JUDGE PESLAK: Okay, I understand.

25 MR. SAIDMAN: But if there are no further questions on Claims 9
26 and 19, I'm happy to turn briefly to Ground 2.

1 JUDGE PESLAK: I don't have any questions.

2 MR. SAIDMAN: Okay. So I'll just touch on Ground 2 relatively
3 briefly and otherwise rely on our briefing. So just to kind of set the context,
4 under Ground 1 we argue that Conn anticipates Claim 9. In the event the
5 Board disagrees, we have an alternative argument in Ground 2 that Conn, in
6 view of the knowledge of one of ordinary skill in the art, as exemplified by
7 the Wang reference, would have rendered Claims 9 and 19 obvious.

8 Now, Patent Owner's main argument to this has been, well, Ground
9 2 doesn't actually address the ground connection limitation. We argue that's
10 incorrect. If you go to Slide 36, on the upper right-hand side of the screen,
11 you can see an excerpt from the petition. The petition says, under Ground 2,
12 considering the actual use cases of Conn's electronic package, Conn renders
13 obvious the not-provided ground connection limitation. And that's
14 consistent with the exact same heading at the beginning of Ground 2. So, if
15 there are no further questions --

16 JUDGE PESLAK: Ground 2 doesn't rely on Wang then,
17 knowledge of a POSITA.

18 MR. SAIDMAN: So you're correct, Your Honor, that the way that
19 the ground is described is Conn in view of the knowledge of one of ordinary
20 skill in the art. But in the description of the knowledge of one of ordinary
21 skill in the art, it relies repeatedly on Wang as exemplifying that knowledge.
22 So it's not just Dr. Thompson talking alone. It's Dr. Thompson talking with
23 an example from the Wang reference.

24 JUDGE PESLAK: And there's no argument for motivation to
25 combine Wang and --

26 MR. SAIDMAN: No, Your Honor.

1 JUDGE PESLAK: Okay.

2 MR. SAIDMAN: So if there are no further questions on Ground 2,
3 I'll hand it over to my colleague, Mr. Zang, for the remainder.

4 MR. ZANG: Your Honor, my name is Chen Zang. It's my
5 pleasure to continue discussing Petitioner's positions regarding Ground 3
6 through Ground 5. As shown on Slide 38, the proposed combination of
7 Gambino and Conn is to incorporate Conn's anchor via into Gambino's
8 dummy metal pad 16 located in the corners of the semiconductor substrate to
9 improve the adhesion of the dummy metal pad 16A to the semiconductor
10 substrate.

11 As shown on Slide 39, among the numerous obviousness rationale
12 articulated by Petitioner, one of them refers to Conn's and Gambino's
13 teaching of the same conventional via forming method. And according to
14 the petition, it would have been obvious that applying the Gambino's via
15 forming method can result in the same anchor via as described in Conn.

16 And turning to Slide 40, however, HID disputes this rationale and
17 they point to the paragraph 20 of Gambino, which disclosed via forming
18 method that includes first, forming a via on the front side of the
19 semiconductor substrate, and then deposit a metal filler into the via, and then
20 using a backside polishing or grounding method to expose the metal filler in
21 the anchor via, in the TSVs.

22 JUDGE PESLAK: Just so I'm clear and the record is clear, when
23 you refer to -- did you say top side?

24 MR. ZANG: The top side, yes.

25 JUDGE PESLAK: So that's --

26 MR. ZANG: Sorry, Your Honor.

1 JUDGE PESLAK: -- the top of the yellow in Figure 8 of Gambino
2 -- Figure 5 of Gambino?

3 MR. ZANG: Yes, the top side of the Figure 5 of Gambino. That's
4 the front side.

5 JUDGE PESLAK: The backside is the opposite side?

6 MR. ZANG: The backside is the bottom side.

7 JUDGE PESLAK: Okay, thank you.

8 MR. ZANG: You're welcome. So if there's no other questions, I
9 will continue to discuss this Slide 40. So according to HID, utilizing
10 Gambino's method to create Conn's anchor via would result in one of the
11 two outcomes. First, it will create an anchor via fully extended from the
12 bottom side to the front side of the semiconductor substrate. And the second
13 outcome is that the anchor via will not reach the backside metal layer.

14 Well, before I get into the details of these two outcomes, I want to
15 mention that the second alleged outcome is really a red herring because it
16 directly contradicts with the teaching of Gambino and Conn. Both of them
17 describe that the via or TSVs have their metal filler exposed to the backside
18 of the semiconductor substrate. So therefore, if there's no other questions
19 regarding the second alleged outcome, I will focus my discussion on the first
20 alleged outcome.

21 As shown on Slide 41, regarding the first alleged outcome, HID
22 first argues that the fully extended anchor via from the bottom side to the top
23 side will provide ground connection to active devices located on the front
24 side of the semiconductor substrate. That's not correct, because as explained
25 by Petitioner's expert, Dr. Thompson, a POSITA would understand that the
26 corners of the substrate are usually the less crowded area, not for planting

1 the active devices. Therefore, a POSITA would understand that there's no
2 chance for the anchor via to meet any of these active devices on the front
3 side of the semiconductor substrate.

4 Move to Slide 42. In addition, Gambino teaches that the TSVs and
5 their connected backside metal are in the area of the dye to prevent from
6 interfering with dicing operation in a dicing street. So, motivated by the
7 same principle, a POSITA would have patterned wiring layer on the front
8 side of the semiconductor substrate to avoid interfering with corner area of
9 the semiconductor substrate. So therefore, there's also no reason to --

10 JUDGE PESLAK: I have a question. Can you just back up to
11 what's in red?

12 MR. ZANG: Yes.

13 JUDGE PESLAK: What is the dicing channel in Gambino?

14 MR. ZANG: Yeah, the dicing channel is not directly showing on
15 the figure of Gambino. However, to provide an example, I will go back to
16 Slide 20. So as shown on the Figure 2A and Figure 3A of the '826 Patent, so
17 the dicing street is located in the outer boundary of the semiconductor
18 substrate. So during the dicing operation, a POSITA would use diamond fall
19 to cut along the dicing street, so during the dicing operation, and the
20 resulting will be the single die.

21 JUDGE PESLAK: So dicing is cutting away the material on the
22 outer perimeter, is that what you're saying?

23 MR. ZANG: Yes. So the Figure 2A and the Figure 3A only
24 shows one die of the semiconductor device. However, if you imagine there's
25 a wafer that's constituting a lot of dies. So during the dicing operation, it
26 will cut along the dicing street, so the whole wafer will become multiple

1 smaller dies.

2 JUDGE PESLAK: Okay, I understand.

3 MR. ZANG: Thank you, Your Honor. So I will go back to slide
4 -- where I am before. Yeah, so I will go back to Slide 42. So refer back to
5 what I discussed earlier. Gambino teaches locating the TSV and the wiring
6 layer away from the corner because they don't want to interfere with the
7 dicing operation close to the corner area.

8 So, therefore, motivated by the same principle, a POSITA would
9 have also patterned the wiring layer on the front side of the semiconductor
10 substrate to avoid the corner area. Therefore, there's no chance for the
11 anchor via located in the corner area to meet with any of these wiring layers
12 on the front side. Therefore, there's no reason for the anchor via in the
13 proposed combination to provide any ground connection to the active
14 devices.

15 And next, I'm moving to Slide 43. So, in addition, HID argues that
16 the fully extended anchor via will not have a protruding portion on the back
17 side of the semiconductor substrate. This is also incorrect because, as shown
18 by the petition, Burnham teaches almost identical die structure as Gambino.

19 And Figure 2C of Burnham shows via with protruding portion
20 extending from the back side of the semiconductor substrate. And also, as
21 explained by Dr. Thompson, the Burnham and Gambino are from the same
22 IBM group. In fact, all the inventors of Gambino are also listed as the
23 inventor of the Burnham. So, therefore, a POSITA would understand that
24 utilizing the same method taught by Gambino will also result in a via with a
25 protruding portion.

26 And this is further explained by Dr. Thompson on Slide 44. So, in

1 order to arrive at that protruding portion, one can just polish the substrate at
2 a higher rate than the metal filler. So, therefore, that will result in a metal
3 protrusion.

4 JUDGE PESLAK: Counsel, I'm just trying to understand how this
5 fits into the whole picture here.

6 MR. ZANG: Yes.

7 JUDGE PESLAK: So, you're responding to Patent Owner's
8 argument that because Gambino polishes the back side --

9 MR. ZANG: Correct.

10 JUDGE PESLAK: -- you don't have the protruding portion? So,
11 and what you're showing in Burnham is a different view of the
12 semiconductor stack that's not shown in Gambino?

13 MR. ZANG: Yeah, the Gambino does not have this exact figure as
14 shown in the Figure 2C on the Slide 43. So, Your Honor, so to rephrase the
15 story. So, first of all, the HID argues that -- they point to the paragraph 20
16 of Gambino. And as shown on the Slide 40, they point to the last sentence
17 of the paragraph 20 of Gambino, which says that Gambino will employ a
18 thinning process, e.g., a polishing and a grinding process in order to expose
19 the TSV. So, according to HID, that will only expose a flat surface of the
20 metal filler of the TSV. It will not generate a protruding portion.

21 JUDGE PESLAK: Well, what does polishing and grinding mean
22 if it doesn't come out flush?

23 MR. ZANG: Yeah, so because according to Gambino, the via was
24 initially made from the front side of the semiconductor substrate --

25 JUDGE PESLAK: So it's filled from the top?

26 MR. ZANG: Filled from the top. And then after the metal filler

1 was filled in, the one of ordinary skill in the art are using a grinding process
2 on the bottom to ground extra excessive semiconductor substrate to expose
3 the metal filler of the vias.

4 JUDGE PESLAK: But wouldn't -- I mean, if it was flat, it would
5 still connect to the metal pad though, right?

6 MR. ZANG: Yeah, that's the flat --

7 JUDGE PESLAK: That's what's shown here. That's what I'm
8 puzzled with. If you're polishing and grinding, how do you get a protruding
9 portion?

10 MR. ZANG: So because the POSITA is not an automaton, so they
11 wouldn't know how to fill in the details into the Gambino's high-level
12 description of the backside grinding method. So, like, what I would --

13 JUDGE PESLAK: I understand that, but I'm not an automaton.

14 MR. ZANG: Yes.

15 JUDGE PESLAK: How does this process work where you would
16 have -- you would polish the backside and you would have something
17 protruding that -- you know, I'm having trouble picturing how that would
18 work. Is this like an etching thing that they do? It's not an etching thing,
19 right?

20 MR. ZANG: Yeah, Your Honor, you're right.

21 JUDGE PESLAK: I can see if it was etched, but I don't get how
22 you would grind and have a protruding portion on the back.

23 MR. ZANG: Your Honor, you're right. So certainly etching is one
24 of the methods. Another way of doing so, as explained by Dr. Thompson on
25 Slide 44, is that suppose this is an anchor via, and you have the
26 semiconductor substrate surrounding the anchor via, right? So if you apply

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1 the backside grinding method, and you can use a higher rate of grinding in
2 the surrounding silicon by using a lower grinding rate on the metal filler of
3 the anchor via. In that case, you will create a difference between the
4 grinding speed.

5 JUDGE PESLAK: So this is explained in Dr. Thompson's
6 supplemental declaration at paragraph 24?

7 MR. ZANG: Yes, this is also explained by Dr. Thompson in
8 paragraph 24 of his supplemental declaration.

9 JUDGE PESLAK: Okay. So I just want to know what I should
10 read in your papers to understand this process.

11 MR. ZANG: Yes. Thank you, Your Honor. And Your Honor, I
12 also want to refer you to column 4, line 53 through 56 of Burnham. That
13 discloses the same method as described by Dr. Thompson in his
14 supplemental declaration here. So basically, it's about applying a different
15 grinding speed on the silicon substrate and also on the metal filler of the
16 anchor vias.

17 JUDGE PESLAK: Okay.

18 MR. ZANG: Yes, so I will continue to talk about Slide 44. So on
19 the right-hand side of this slide, Your Honor, as you just asked, there is also
20 an additional method as described by Torii, which is after the backside
21 grinding process, one can etch the silicon substrate to slightly protrude the
22 real surface of the metal filler of the anchor vias. And if there's no other
23 questions, I will skip Slide 45 and move to Ground 4, anticipation by Torii.

24 As shown on Slide 47, there are two disputed issues between the
25 parties about Torii ground. First of all, HID argues that Torii does not
26 disclose --

1 JUDGE PESLAK: Could you back up to Gambino-Conn for a
2 second?

3 MR. ZANG: Yes, Your Honor.

4 JUDGE PESLAK: Is there any dispute that Gambino doesn't show
5 the vias disposed in a corner?

6 MR. ZANG: There's no dispute about Gambino's teaching of
7 disposing in a corner.

8 JUDGE PESLAK: Okay.

9 MR. ZANG: Yes. We'll go back to Slide 47. So a bit earlier, I
10 was discussing there are two disputed issues regarding Torii. So first of all,
11 HID argues that Torii does not disclose not providing ground connection to
12 one or more active devices. And the second disputed issue is that HID
13 argues that Torii does not disclose a backside metal layer on a bottom
14 surface of the semiconductor substrate.

15 So first, as shown on the Slide 48, in the petition, Petitioner relies
16 upon paragraph 48 of Torii to disclose not providing ground connection to
17 active devices. As you can see here, the paragraph 48 of Torii discloses that
18 the sub-TSV, i.e., the anchor via, is a dummy which is normally not used as
19 a current pathway. So this disclosure alone is sufficient to disclose not
20 providing ground connections to active devices.

21 Well, the second half of the sentence also says the dummy, but can
22 be used as a subsidiary current pathway. However, that's only a permissive
23 option, not a mandatory option featured for the sub-TSV. So therefore, it
24 does not exist in every embodiment of Torii.

25 As further explained on Slide 49, if you look at the phrase used in
26 the beginning of the second half of the sentence, it says but can. So that

1 means the subsidiary current pathway is only an exceptional case to the
2 normal case. In particular, the but suggests a contrast, an exception, right?
3 And also the can be suggests a permission or ability. It does not require
4 every sub-TSV to serve as a subsidiary current pathway.

5 JUDGE PESLAK: So is there a -- other than paragraph 48, is there
6 an embodiment described in Torii that would support your reading, i.e., the
7 one where it's normally not used and the one where it is used as a subsidiary
8 current pathway?

9 MR. ZANG: Yes, Your Honor. So I will answer your question
10 from three different angles. So the first angle is that, if we go back to Slide
11 30, as discussed by my colleague, so it is commonly understood in art that
12 the dummy is not used for contact currents. So if you're reading the whole
13 sentence of paragraph 48 of Torii, it does say that the dummy is normally
14 not used as a current pathway. So it is consistent with the ordinary
15 understanding of the art.

16 And my second response is that if you look at this whole invention
17 as a whole of Torii, and it describes using a sub-TSV to provide mechanical
18 support during the process of adjoining the stacks of semiconductor chips.
19 So if you look at the invention as a whole, Torii does not use sub-TSV as a
20 current pathway.

21 And also, in addition, third, as shown on Slide 49, the summary of
22 the invention and also the claims of -- so actually on slide, as shown on Slide
23 50, the summary of the invention and the claims of Torii also confirm this
24 understanding. For example, the Claim 12 of Torii recites that a main
25 electrode connected to a main TSV is to constitute a current pathway.
26 However, the claim does not require the sub-electrode connected to the sub-

1 TSV to serve as a current pathway.

2 So therefore, a POSITA reading the Torii's disclosure as a whole
3 would understand that the subsidiary current pathway is only a possible -- a
4 permissive feature of the sub-TSV, but they are not required for every
5 embodiment.

6 JUDGE PESLAK: So you're saying that what's in Claim 12 of
7 Torii, the first clause there that's highlighted in blue?

8 MR. ZANG: Yes.

9 JUDGE PESLAK: That that's a TSV that's not used as a current
10 -- that is used as a current pathway?

11 MR. ZANG: Correct.

12 JUDGE PESLAK: And the second clause is a TSV that is not used
13 as a current pathway?

14 MR. ZANG: Your Honor, you're right. So to give you more
15 context, if we look at the Slide 48, it shows Figure 3 of Torii from the top
16 view. So, basically, we label that the sub-TSV. And also the figure does not
17 label the main TSV, but the main TSV is located in the center of this top
18 view on the semiconductor substrate. So clearly, the sub-TSV is different
19 from the main TSVs.

20 JUDGE PESLAK: Okay. You can go ahead.

21 MR. ZANG: Thank you, Your Honor. As shown on the -- I will
22 move to Slide 51. HID has no rebuttal to the evidence from Torii. All they
23 submitted is their expert declaration, which says releasing static electricity is
24 providing a ground connection. However, this does not answer the question
25 whether the subsidiary current pathway is a permissive or mandatory feature
26 of the sub-TSV.

1 So according to the petition, because the subsidiary current
2 pathway is not required for every embodiment of Torii, so at least in some of
3 the embodiment the sub-TSV is not used for a current pathway at all, that is
4 insufficient to anticipate the claim limitation of not providing ground
5 connection to one or more active devices.

6 JUDGE PESLAK: Okay. So Patent Owner's position -- you're not
7 disputing that releasing static electricity would be providing a ground
8 connection?

9 MR. ZANG: Yeah, that's not disputed on the record.

10 JUDGE PESLAK: Okay. But you're disputing that that's a
11 requirement of Torii?

12 MR. ZANG: Yes.

13 JUDGE PESLAK: Okay.

14 MR. ZANG: So if there's no other questions, I will move to the
15 next issue. As shown on the Slide 53, the second dispute is regarding the
16 construction of on. In the petition, Petitioner showed that the plain and
17 ordinary meaning of on should apply, so it does not require direct contact.
18 However, HID proposed to constitute on to require direct contact between
19 the bottom surface of the semiconductor substrate and the backside metal
20 layer. HID's construction is not supported by the intrinsic or extrinsic
21 evidence.

22 As shown on 54, the petition cited the *AFG Industries* case from
23 the Federal Circuit. So in that case, it also involved a very similar claim
24 language as the '826 Patent claim. So in that case, the Federal Circuit held
25 that the claim at the issue does not state that each layer is formed directly on
26 the preceding layer, so therefore the Court refused to read it on to require

1 direct contact.

2 JUDGE PESLAK: I read this case a little differently.

3 MR. ZANG: Yes, Your Honor.

4 JUDGE PESLAK: The claim starts sort of this open-ended
5 comprising.

6 MR. ZANG: Yes.

7 JUDGE PESLAK: And then it says that this five-layer coating is
8 composed of. And was that -- I read what the Federal Circuit said there is
9 that composed of means you could have interstitial layers as long as you
10 didn't change the function. So, I don't know that this case is on all fours. I
11 mean, I don't know if the *AFG* case is on all fours with this case.

12 MR. ZANG: Your Honor, your points are well-taken. So
13 grantedly, we agree that no two cases are identical, right? So, the point for
14 Petitioner to cite to the *AFG* case is to illustrate that the plain and ordinary
15 meaning of on does not require direct contact. So, back to the '826 Patent,
16 there is no language of disclaimer or lexicographer to redefine the plain and
17 ordinary meaning of on for this patent. So, therefore, we believe that the on
18 in the '826 Patent also does not require direct contact.

19 JUDGE PESLAK: Well, what's the intrinsic evidence in support
20 of your position? I mean, that's more important for this case.

21 MR. ZANG: Your Honor, you're right. So, next I will go to
22 intrinsic evidence. So, as shown on the Slide 54, the HID cites to the
23 background section of '826 Patent. But as you can see here, the background
24 section only says the backside metal layer is attached to the substrate or
25 deposited on the bottom side of the substrate. It does not say directly deposit
26 or directly attached to. And also this language made it clear that this is just

1 one conventional method. So it shouldn't be used to limit the claim that you
2 mentioned of '826 Patent.

3 And next on Slide 56, HID also cite to the embodiment as showing
4 the Figure 1B of '826 Patent. But as you can see here, the accompanying
5 text of Figure 1B also describe that the backside metal layer is deposited on
6 the bottom side of the semiconductor substrate or formed on. It does not
7 require directly formed on. And also, the rest of the disclosure of '826
8 Patent also warn against reading any particular embodiment into the claim
9 that you mentioned. So, there's no reason to interpret the intrinsic evidence
10 to support HID's narrow construction.

11 If there's no questions, I will move to Slide 58. So HID's
12 construction is also contradicted by the extrinsic evidence. For example, as
13 shown on Slide 58, that Burnham says forming a backside metal on a silicon
14 substrate, as shown on the text in red. And Burnham further explains that
15 this means the backside metal is first formed on an oxide material, and then
16 the oxide material can be formed on the backside of a silicon wafer. In other
17 words, there's actually an oxide layer serving as an intermediate layer in
18 between the backside metal and the silicon substrate.

19 Therefore, if you read the text in red as a whole, it actually says the
20 forming backside metal means indirect contact. And also, if you look at the
21 text in green, Burnham says forming backside metal on the oxide layer
22 means the backside metal 16 is deposited directly on oxide layer 14. In
23 other words, Burnham also used formed on to mean directly on. In
24 summary, in the art, a POSITA would use formed on or deposited on to
25 mean both directly on and indirectly on. If there's no questions, I will skip
26 Slide 59 and I will go to Slide 60.

1 JUDGE PESLAK: Let's go back a second.

2 MR. ZANG: Yes.

3 JUDGE PESLAK: So, the claim language isn't formed on or
4 deposited on.

5 MR. ZANG: The --

6 JUDGE PESLAK: It says a backside metal layer on a bottom
7 surface of a semiconductor. So, I think Patent Owner's argument is --

8 MR ZANG: Yes.

9 JUDGE PESLAK: -- that it's on a bottom surface means it has to
10 be in direct contact because it says it's on a bottom surface.

11 MR. ZANG: Yes, Your Honor.

12 JUDGE PESLAK: Why isn't that correct?

13 MR. ZANG: Your Honor, I will go to -- that's an excellent point.
14 I will go to that in the next slide. Yes, so shown on Slide 61, HID argued
15 that the surface in the claim requires direct contact. That's not true. Because
16 as explained by Dr. Thompson, Petitioner's expert, the semiconductor
17 substrate has many different surfaces, right? So, each surface has their own
18 context and significance.

19 So, if I use the water bottle to resemble a semiconductor substrate,
20 the bottom surface is here. And if the claim does not use surface, you can
21 put the backside metal against the sidewall of the bottom portion of the
22 semiconductor substrate. So, clearly, the bottom surface in the claim is used
23 to indicate that the backside metal layer should be put against the bottom
24 surface of the semiconductor substrate rather than the sidewall of the bottom
25 portion of the semiconductor substrate.

26 So, the surface here does not signal direct contact. Rather, it just

1 indicates which surface that the semiconductor -- the backside metal layer
2 should be placed against on.

3 JUDGE PESLAK: Okay, forget about the bottom for a second.
4 That didn't really help, okay? Forget about the state of the art. So, if -- I
5 mean, looking at -- if the backside metal layer is on a bottom surface of the
6 semiconductor substrate --

7 MR. ZANG: Yes.

8 JUDGE PESLAK: -- how can that be on the side or someplace
9 else but not in direct contact? I'm not sure I understand your argument.

10 MR. ZANG: Your Honor, your points are well taken. So, if we
11 look at the claim language here, the HID's argument is that if you take away
12 the surface from this claim language, it will not require direct contact.
13 That's not true. Because if you just take away the surface, the claim will
14 read like, the backside metal layer on a bottom of the semiconductor
15 substrate.

16 So, that could mean the backside metal layer is placed against a
17 side surface of the semiconductor substrate, the lower portion -- the bottom
18 portion of the semiconductor substrate. So actually, the insert of this surface
19 into the claim language suggests that the backside metal layer is placed
20 against the bottom surface of the semiconductor substrate.

21 JUDGE PESLAK: But I think that's what Patent Owner is saying.

22 MR. ZANG: So, yeah, the Petitioner's argument is that the bottom
23 surface suggests which surface that the backside metal layer should be
24 placed against rather than direct contact or indirect contact.

25 JUDGE PESLAK: So, you're saying that because the claim doesn't
26 define which bottom surface?

1 MR. ZANG: The claim, as it recited, it defines the bottom surface
2 in view of the specification. But if you take out the surface, it does not
3 specify which surface of the bottom.

4 JUDGE PESLAK: Okay, we'll hear what Patent Owner has to say
5 about this.

6 MR. ZANG: Yes, Your Honor. Your Honor, so if there are no
7 questions, I will move to slide --

8 JUDGE ANDERSON: I have one question.

9 MR. ZANG: Yes, Your Honor.

10 JUDGE ANDERSON: Should we agree with Patent Owner and
11 their view of how we would understand and interpret on, do you have any
12 basis to succeed in your claim of unpatentability if we do that?

13 MR. ZANG: Your Honor, so that is not -- that point is not
14 disputed on the record. So during the briefing, the Petitioner's argument is
15 that the Torii should disclose on a bottom surface under the plain and
16 ordinary meaning rather than Patent Owner's claim construction.

17 JUDGE PESLAK: So, what's the plain and ordinary meaning?

18 MR. ZANG: The plain and ordinary meaning is that on does not
19 require direct contact, it should be -- including the case of direct contact or
20 indirect contact. So, as shown here in Torii, the Torii disclosed that the
21 backside of the metal layer is placed on the semiconductor substrate, which
22 is shown in the yellow, the intervening layer between them. So according to
23 Petitioner, the Torii disclosed on a bottom surface under the plain and
24 ordinary meaning of on because on does not require direct contact, and
25 indirect contact should also suffice to disclose on a bottom surface.

26 JUDGE PESLAK: But I think back -- okay. So, back to Judge

1 Anderson's question.

2 MR. ZANG: Yes.

3 JUDGE PESLAK: If we were to adopt Patent Owner's
4 construction, then there is no direct contact in Torii?

5 MR. ZANG: So, yes. So, under the Patent Owner's construction,
6 there's no direct contact in this example shown in Torii.

7 JUDGE PESLAK: Okay.

8 MR. ZANG: Your Honor, if there's no question, I'll move to the
9 Ground 5, Ide anticipation. So, the only issue involved in Ide ground is
10 same as Torii, which is whether Ide disclosed on the bottom surface on the
11 plain and ordinary meaning. So, if the Board agrees with Petitioner that on
12 does not require direct contact, the Ide should also disclose on the bottom
13 surface under the plain and ordinary meaning of on. And Patent Owner does
14 not dispute that. Therefore, the Board should find that Ide anticipates the
15 challenge of the claims.

16 JUDGE PESLAK: Okay. So, this is the same issue in Ide as in
17 Torii?

18 MR. ZANG: Yeah, this is the same issue as the claim construction
19 in Torii.

20 JUDGE PESLAK: And is there any dispute that Ide does not
21 disclose the corner limitation?

22 MR. ZANG: There's no dispute as to whether Ide discloses the
23 corner limitation.

24 JUDGE PESLAK: Okay.

25 MR. ZANG: And, Your Honor, if there's no question, I will stop
26 here for the Petitioner.

1 JUDGE JUNG: I have no questions.

2 MR. ZANG: Thank you, Your Honor.

3 JUDGE PESLAK: Judge Anderson, any more questions?

4 JUDGE ANDERSON: No more questions.

5 MR. ZANG: Thank you, Your Honor.

6 JUDGE PESLAK: Okay. So, you went to 47 minutes. So, you'll

7 have 13 minutes for rebuttal.

8 MR. ZANG: Understood.

9 JUDGE PESLAK: Patent Owner, how much time would you like
10 to reserve for rebuttal?

11 MR. COWELL: Fifteen minutes, please.

12 JUDGE PESLAK: You can start when you're ready.

13 MR. COWELL: So, if the Board will indulge me, I'd like to start
14 where Counsel just left off with the on the back side. So, I'm on Slide 9 of
15 Patent Owner's slides. And this entire invention is about improving the
16 adhesion of the backside metal layer to the semiconductor substrate. And it
17 uses the word adhesion and adhesive repeatedly. And Mr. Zang, Counsel
18 didn't really mention these parts. But if you look on our slide here, column 1
19 relies on forming a backside metal stack having several layers, the first of
20 which must form an adhesive bond with the substrate.

21 That can't mean anything other than direct contact. Relying on the
22 adhesive properties, or the adhesive qualities, and if we look down at the
23 bottom there, between the substrate and the interface layer, which is
24 indisputably the top layer of the backside metal. I think that right there --

25 JUDGE PESLAK: But the claim doesn't require that the backside
26 metal be bonded to the semiconductor substrate. It says that it should be

1 bonded to the protruding portion of the filament, right?

2 MR. COWELL: Correct, because the protruding portion goes
3 through and into the metal layer.

4 JUDGE PESLAK: So, I don't know how the adhesive part helps
5 you with this claim. We have to deal with the claim here, not the spec. And
6 there's no bonding required between the metal layer and the semiconductor
7 substrate as I read the claim, unless you can point to someplace where there
8 is adhesion required.

9 MR. COWELL: The explicitly claimed bonding, yes, is between
10 the protruding portion and the backside metal layer. So, let's look at the
11 claim. Now I'm on Slide 8. The backside metal layer on the bottom surface
12 of said semiconductor substrate. And we can contrast that with Claim 9,
13 where there's another layer, a metal layer, overlying the semiconductor
14 substrate. And the use of two different words means something. It's not on
15 the metal filler -- excuse me. The metal layer in Claim 9 isn't on the
16 semiconductor substrate. It's overlying it, which means it could be directly
17 on it, but it could, also, have layers in between.

18 Well, we have Claim 1, backside metal layer, on the bottom
19 surface of the semiconductor substrate. That implies, especially when you
20 read the intrinsic evidence, that it's in direct contact. Because again, it's all
21 about improving the adhesion of that backside metal layer to the bottom
22 surface.

23 JUDGE PESLAK: Okay. Just so I understand what Claim 9 is
24 really about, is there some embodiment in your figures that will explain?
25 Because this looks like a different metal layer than Claim 1. Claim 1 is a
26 backside metal layer and this is bonded to a metal layer overlying. Is there

1 some figure in the patent that would show a backside metal layer plus
2 another metal layer that the B is bonded to? Just so I -- I'm trying to get my
3 head around what this means in Claim 9.

4 MR. COWELL: Yeah, I'm not sure. So give me a moment, I don't
5 have the patent in my slides. I don't believe there's a specific figure. If you
6 want, we can talk for a moment about Claim 9 in regards to Conn. Because
7 they have a figure in Conn that Petitioner says shows both metal layers.

8 JUDGE PESLAK: Okay.

9 MR. COWELL: There's one on the backside, there's one on the
10 front side.

11 JUDGE PESLAK: Okay. Why don't we look at that when we get
12 to Conn?

13 MR. COWELL: Okay. But essentially, there's supposed to be
14 another layer on the other side from this backside metal layer, somewhere
15 over there, overlying it if you will.

16 JUDGE PESLAK: I don't mean to interrupt you, but this claim
17 construction argument only applies to Grounds 4 and 5, correct?

18 MR. COWELL: That's correct.

19 JUDGE PESLAK: Okay. Thank you.

20 MR. COWELL: And as I think Counsel would agree, there's no
21 dispute. If the Board adopts our construction, that it is correct. Now, the
22 embodiment in the claim -- excuse me, the embodiment in the patent uses
23 the word on repeatedly to show direct contact. The interface layer is
24 deposited on the bottom side of the semiconductor substrate, and we show in
25 the figure it's directly on there. The conduction layer, which is the next one,
26 is formed on the interface layer 152, and again, there's direct contact

1 between those two.

2 Finally, the packaging layer is formed on the conduction layer.

3 And we look at the figure, and again, it's directly in contact with. So, the
4 patent is telling us when it's using on, it means in direct contact with. It
5 doesn't provide any examples when there's no direct contact, nor does it ever
6 suggest that other than direct contact is acceptable. I'm just going to skip
7 ahead.

8 Now, what Petitioner relies on, Petitioner's main, and I'll put this in
9 quotes, evidence that they rely on are some court cases, the *AFG* case and
10 the other one, a couple of District Court cases. And they have absolutely no
11 bearing on this decision.

12 JUDGE PESLAK: Can we go back to the claim language for a
13 second. This is what I've got to look at. So if I look at Claim 1, right, it's a
14 comprising claim, it's open-ended. So, when we see a backside metal layer
15 on a bottom surface, it's an open-ended claim. Why couldn't it be construed
16 as, you know, another layer between the backside metal layer and the bottom
17 surface?

18 MR. COWELL: Because then the backside metal layer wouldn't
19 be on the bottom surface. Now, if the bottom surface were patterned, you
20 could have the backside metal layer in Quadrant A. Nobody discussed this
21 in the briefing, but I'm trying to answer your question. So, Quadrant A of
22 the substrate, and then at a different part, Quadrant B, there could be some
23 other material there. But the backside layer has to be in contact with the
24 bottom layer of the substrate, the bottom surface of the substrate.

25 JUDGE PESLAK: But that *AFG* case does seem to indicate that.
26 The *AFG* case is not really applicable here because it's got that composed-of

1 language. But I think the Federal Circuit started with the fact that that was
2 an open-ended claim comprising, and that's one of the reasons they seemed
3 to come to the conclusion you could have interstitial layers.

4 MR. COWELL: As I recall correctly, there were also descriptions
5 of interstitial layers.

6 JUDGE PESLAK: There were, there were.

7 MR. COWELL: Which there's not here.

8 JUDGE PESLAK: Okay.

9 MR. COWELL: And that's really important because the *AFG* case
10 is a completely different patent on a different technology, different vendors,
11 not even related in any way with different claim language and different
12 embodiments. That's not evident of what this patent means. We have to
13 look at the intrinsic evidence, which is what this patent means, when it talks
14 about adhesion, when it talks about putting the layers on each other, and it
15 uses them in direct contact with them in every example.

16 So those cases are completely, I think, irrelevant to this. And if we
17 look at this from first principles, we interpret a claim the way a person of
18 ordinary skill in the art interprets that claim reading it at the time of the
19 invention. Well, they didn't have these cases. They wouldn't have these
20 cases. So that's completely, I think, beside the point. So, I think, yeah,
21 Grounds 4 and 5, I think, are disposed of by this issue. I think there's no
22 further discussion required on those unless anybody has any questions on
23 those. Otherwise, I'm going to turn to Ground 1.

24 JUDGE PESLAK: But if we didn't adopt your construction then
25 Petitioner wins then, correct? There's no other argument on those grounds?
26 I mean, Torii is the, I understand, is the ground connection. But for Ide, this

1 is your only argument?

2 MR. COWELL: Yes, for Ide, the argument is that the backside
3 metal layer is not on the bottom surface.

4 JUDGE PESLAK: Okay. And Torii is the same, but you have the
5 ground connection issue on Torii.

6 MR. COWELL: Yes. Unless you want to discuss that further, we
7 can move on.

8 JUDGE PESLAK: We can get that. I'm just trying to understand
9 what all these arguments apply to, that's all.

10 MR. COWELL: Yeah. So just going to Torii, back to Torii then,
11 discussing the ground connection part. I believe the Petitioner's entire
12 argument hangs on using the word but. And the word but means it's
13 completely optional and it's another embodiment, even though there's no
14 embodiment within the claims -- excuse me, no embodiment within the
15 specification showing it sub-TSVs that don't carry current. It's completely
16 silent on that issue.

17 And they also rely on Claim 12, which, again, is just silent on this
18 issue. It says, okay, well, you have a -- I don't have the language directly in
19 front of me, you have a TSV that carries current and you have a sub-TSV. It
20 doesn't say sub-TSV doesn't carry current. It doesn't say anything about it.

21 And the legal framework for a negative limitation like this is
22 whether a person of ordinary skill in the art would understand that limitation
23 to be disclosed in the prior art. Not silent. Silence isn't good enough. There
24 needs to be analysis showing that they would understand that it was not
25 there. And so, there's no discussion within Torii. There's no examples
26 within Torii.

1 JUDGE PESLAK: So, do you have any evidence in the record that
2 would rebut this testimony by Dr. Thompson that one of ordinary skill in the
3 art would understand that that sentence in light of these other, you cited
4 some other documents there, would interpret that as an embodiment?

5 MR. COWELL: There's no evidence. Frankly, I don't think there's
6 any evidence going either way. That's not a technical opinion. That's a
7 grammar opinion. Dr. Thompson's not a grammar expert, he doesn't claim
8 to be. And he cites no support for his opinion. It's merely a conclusory
9 ipsedixitism.

10 JUDGE PESLAK: Okay.

11 MR. COWELL: Turn to Ground 1. And it starts with the disposed
12 in at least one corner of a semiconductor substrate claim construction issue.
13 And something Petitioner didn't mention is that, while they have no trouble
14 understanding where the corner of the substrate is for the Board, in District
15 Court they said it was hopelessly indefinite and no one would know the
16 boundaries of this. And that is a fundamental inconsistency that the Board
17 has been clear lately and the director has been clear lately, should disqualify
18 that argument.

19 And it is -- of course, their response was, well, the outside
20 boundaries of it are not at issue here. But as our arguments in Conn show,
21 the outside boundaries are at issue. We don't know whether any of the so-
22 called Conn anchor vias are within the corner or not. And they provide a no
23 reasoned explanation as to why it's indefinite -- it's a narrow indefiniteness
24 argument in front of the District Court and yet a broad reading here in front
25 of this Board.

26 JUDGE PESLAK: Well, let me ask you. Are they really arguing

1 the outer bounds? I mean, is it your argument on Conn that there's no
2 disclosure in Conn as to what's in a corner?

3 MR. COWELL: That is one of the main arguments, yes.

4 JUDGE PESLAK: Okay. Leaving aside your ovoids, that's your
5 argument that there's no disclosure in Conn of what's in the corner, that, you
6 know, that pattern they show in Figure 2 is illustrative of what may be there,
7 but that doesn't show the corners. That's really your argument, correct?

8 MR. COWELL: Yes, that's --

9 JUDGE PESLAK: I mean, the corners aren't there, so.

10 MR. COWELL: Right, they drew the corners on.

11 JUDGE PESLAK: And that's not the same issue as where does the
12 corner end? You're just saying -- I mean, I think your argument is there's no
13 corner shown there, so we don't know. As opposed to the corners are shown
14 and there's some views there, but they would argue in District Court, I
15 assume, for infringement. We don't know where the corner is, right? So, I
16 don't -- is that really inconsistent with what they're doing in District Court,
17 though?

18 MR. COWELL: I think it is. Because if we go to Slide 11 of
19 Patent Owner's slides, this is their figure. They drew the line on the corner
20 and they said, a-ha, we have rivets in the corner. It discloses anchor vias in
21 the corner. End of story, that's it. Now, if those anchor vias are not in the
22 corner. And again, I'm just using their exact figure. We had to respond to
23 their figure. We had to explain why it's wrong. Then, they're not in the
24 corner. They're within that ovoid shape inscribed in the substrate.

25 JUDGE PESLAK: Maybe I'm wrong. I was interpreting your
26 argument as this -- I mean, regardless of these rectangles they drew in, that's

1 not a corner anyway.

2 MR. COWELL: That is the primary argument, Your Honor.

3 JUDGE PESLAK: Okay. I want to make sure I understand.

4 MR. COWELL: Yes, there's two arguments. The primary
5 argument, I think you've already said it, but I'll restate it. Conn doesn't say
6 anything about corners. It doesn't say anything about which vias are in any
7 corners, if the ones in the corners are anchor vias or if they're not anchor
8 vias. It doesn't say anything about that. It just gives us one rectangle. It
9 says, here's a pattern maybe. And that's it, end of story. It uses the word
10 corner once in completely unrelated fashion. That's the main argument. The
11 main argument is Conn simply doesn't disclose it.

12 The responsive argument to the petition is that they put this figure
13 on us and they tell us these are where the corners are. We had to explain
14 why even if the Board does accept their figure as illustrative, then they're
15 still not in the corner. Those are the two arguments. So, I think to Your
16 Honor's questions, I think we kind of discussed those main arguments on the
17 corner. If you move to Claim 9, unless there's questions on Claim 1.

18 JUDGE PESLAK: I -- no.

19 MR. COWELL: Okay. So Claim 9. We brought about this
20 earlier. It's where the metal layers overlying the front side, essentially.
21 Overlying said semiconductor substrate. So, it has to be on the opposite side
22 from the backside. And it's not necessarily, but can be in direct contact.
23 And this is, on Slide 13 here, we see the figure that they use to say that this
24 is anticipated by Conn. But the anchor vias have to be both bonded to both
25 the backside and the front side layers, as well as not perform providing a
26 ground connection.

1 And Petitioner makes no real effort to show this as terms of the
2 Claim 9 analysis where they rely on this Figure 3 embodiment. For Claim 1,
3 they say, oh, we know that these can be anchored vias that don't provide
4 ground connection because Conn says they don't have to go all the way
5 through the substrate. Fair enough.

6 But for Claim 9, they just rely on what they said in Claim 1, that's
7 no longer true. They are going all the way through the substrate. They're
8 fully filled, and what they're filled with is explicitly described over and over
9 and over again as a conductor. It's tungsten, it's copper. It's a conductor, it
10 conducts electricity. It conducts, that's the word. And they don't have
11 anything to say that it doesn't – won't provide a ground connection at that
12 point.

13 There's no dispute that the active devices are on the front side.
14 There's no dispute that what they call the copper plane 30 on the front side
15 would be conductive and would carry current. All they can say is, well,
16 maybe they pattern it. Maybe somebody would pattern it. So, you know,
17 they're not connected somehow. There's no discussion of that in Conn.
18 They never point to a single embodiment like that where it's even
19 mentioned. And so, they don't have any evidence that a person of skill in the
20 art would say, oh, okay. There's no way these conduct -- these don't conduct
21 ground -- don't conduct electricity. Of course they do, they're conductors.

22 Now, moving to Ground 2A and Ground 2B. Counsel stood up
23 here and he said, well, of course, we said it could be obvious to add, to make
24 -- to modify Conn so there's no ground connection. Well, let's take a look at
25 what they said in the petition. Nevertheless, to the extent that HID may
26 erroneously argue that Conn does not expressly disclose backside or active

1 devices, they would have been obvious based on Conn and a POSA's
2 knowledge.

3 They're not talking about the ground connection. They're saying,
4 okay, Conn doesn't tell you where the active devices are, but everybody
5 knows. It would be obvious to put the active devices on that front side. And
6 Dr. Thompson agreed with me when I asked him at his deposition. I wanted
7 to make sure I understood what his argument was. And he says, I don't think
8 -- I think Conn doesn't have these gaps. But to the extent someone would
9 argue a backside metal is missing or active device is missing, a POSITA
10 would know based on their knowledge of integrated circuits that they would
11 not be missing.

12 What is that other than a clear setting forth of what this argument
13 is? And I asked him again, with respect to Claim 1, that's your use of a
14 knowledge of a POSITA. Just make sure I understand it. For Claim 1, I'm
15 using knowledge of a POSITA with support from Wang to show that
16 backside metal and active devices would be obvious elements to modify the
17 claim width. There's nothing about the ground connection.

18 They don't discuss the ground connection within the Grounds 2B
19 sections. And they certainly don't provide any motivation to change
20 anything. That is my discussion of Grounds 2A and 2B. And I'll move on to
21 Ground 3 unless there's any questions on that.

22 JUDGE PESLAK: So what were you -- I mean, I'm a little
23 confused. What -- you were asking Dr. Thompson if he's filling in gaps in
24 Conn relating to backside or active devices. So, that would be backside or
25 active devices that are connected to the via? Is that what the question was?

26 MR. COWELL: The question was, and I think it's clear on the

1 right hand side where it says that's your use of a knowledge of a POSITA.
2 The question was asking, you're modifying Conn to address the gaps which
3 he doesn't think are there, as to whether there's a backside or active devices.
4 And he was very clear in his answer that that's what he was using it for.

5 JUDGE PESLAK: Okay. All right.

6 MR. COWELL: And that's worn out by the petition which as I
7 said doesn't change anything about how the ground connection is or is not
8 there. Now, for Ground 3. Ground 3 is very clear. We're going to take
9 Gambino's process for making through silicon vias and we're going to use
10 them to manufacture the anchor vias. To be clear, they don't ever say they're
11 going to modify it. And in fact that's their evidence, that it's a -- that it
12 would be a successful response.

13 Gambino's method, and I think you discussed this already with
14 Counsel, but you essentially drill a via from the front side of the chip into
15 the chip partially through the substrate, and you stop. It's not all the way
16 through the substrate at this point, and then you fill it with metal. And it's all
17 right here on Slide 20. Fill with metal and then you grind and polish the
18 backside until you're flush with the -- until it exposes the TSV so it's flush
19 with the bottom, with the back of the chip.

20 What that means is you can't have a partially filled via, because the
21 vias are filled completely before they're polished. You can't have a Conn
22 style via where you fill it halfway or anything like that. That's not within
23 Gambino's method.

24 JUDGE PESLAK: So there's still an electrical connection, but
25 there's nothing protruding?

26 MR. COWELL: Right. There is nothing protruding, yes. There's

1 two points to this. One is there's nothing protruding because you polish the
2 backside to be flush because chips are always flush. And that's what
3 Gambino shows you anyway, a nice flat chip. But what Petitioner says is,
4 well, sure, but a person of skill in the art would know how to fill in the
5 details on this. But you can't just resort to filling in the details silently. The
6 petition says nothing about it. Silently, when you're talking about a claim
7 element.

8 And when the -- the evidence they support to, they said, well, you
9 do it the way Torii does it. Well, Torii adds an etching step. It's explicit
10 there. It's on Petitioner's Slide 44. And I'll bring that up if that's all right.
11 Then the substrate is etched by silicon etch back up to a region in which the
12 bottom of conductive film a bit too slightly protrudes from the rear surface
13 of the substrate.

14 So you're adding a step. That's how you get the protrusion. That's
15 nowhere in Gambino. Ground 3A doesn't say, isn't Gambino combined with
16 Torii? It's just Gambino with Conn. And nowhere in the petition does it
17 say, oh, we're throwing an etching step here. Same thing with Burnham.
18 They don't use -- Burnham's not an assertive prior art reference. So, they
19 don't use that either. So, I'll move back to our slides now.

20 And so, what we would have here is we have the same issue we
21 have Conn with respect to Claim 9, although Claim 9 is not challenged
22 under Ground 3, to be clear. You have a fully filled via going from the
23 dummy metal pad up to the wiring layer. The dummy metal pad
24 indisputably contacts the ground plane, which is 22. I'm on Slide 21 if I
25 didn't say that earlier. And so, you have an electrical connection from the
26 wiring layer down to the ground plane, providing a ground connection. And

1 the response is, again, well, you'd pattern the wiring layer to avoid this. But
2 there's no discussion of doing that. And --

3 JUDGE PESLAK: Let me ask you a question. You're not
4 disputing that Gambino shows these dummy metal pads in a corner?

5 MR. COWELL: No, Gambino shows dummy metal pads, I think,
6 within the corners under --

7 JUDGE PESLAK: Okay.

8 MR. COWELL: -- our construction, as well.

9 JUDGE PESLAK: Okay.

10 MR. COWELL: And I think Counsel said, well, you would avoid
11 putting active devices in the way of the dicing street, so therefore there's no
12 chance there would be something there. But the dicing street, as is shown in
13 the figures he put up from the patent, is outside of the die, outside of the
14 finished die. If you look at the '673 Patent's figures, it's -- you have the
15 anchor vias in the corners, and then the dicing street is actually a layer
16 outside, and that gets diced off later. That's not part of the finished
17 invention. It's not part of the claim.

18 JUDGE PESLAK: If you look at Figure 3 of Gambino, doesn't it
19 show the dummy metal pads outside the area where you would have active
20 devices? Am I misreading Figure 3?

21 MR. COWELL: What Figure 3 shows, it doesn't show where the
22 active devices are. It shows where Gambino's fully filled electrically
23 conducting vias are. Those are those dots. I think that's item 12, I believe.
24 Yeah, TSVs are 12. So Gambino, by the way, has no concept of a via that
25 doesn't provide an electrical connection. All the vias disclosed in Gambino
26 itself provide electrical connections. And what we see there --

1 JUDGE PESLAK: Is there any figure in Gambino that shows one
2 way or the other whether if you put an anchor via into the dummy metal pad
3 that there would be active devices over that on the substrate?

4 MR. COWELL: No. As I said, Gambino, first of all, doesn't have
5 any concept of anchor via. Gambino doesn't tell you where the active
6 devices are on the front side of the chip. It says you put these pads, the
7 dummy pad 16A, you put them in edges, essentially. But it doesn't avoid
8 -- there's no indication that that would avoid any wiring or active device
9 layers. And again, you know, Petitioner relies on, well, they'd do it this way,
10 because that would meet the claim. And I believe with that -- so that's
11 essentially my discussion of these grounds. If there's any questions, I'm
12 happy to answer them further.

13 There's one thing I do want to point out. The Petitioner has been
14 saying a lot today, well, there's substantial evidence of this, there's
15 substantial evidence of that. That's not the standard before this court. That's
16 the standard in the Federal Circuit. This court needs to find a preponderance
17 of the evidence. They have to show, it's their burden, a preponderance of the
18 evidence showing that these claims are anticipated or obvious. And I think
19 for the reasons I've explained, they fail to do so.

20 JUDGE PESLAK: I don't have any further questions.

21 JUDGE JUNG: I have no further questions.

22 JUDGE PESLAK: Judge Anderson, do you have any questions?

23 JUDGE ANDERSON: No, I'm good. Thank you.

24 JUDGE PESLAK: You used about 17 minutes left. So, you'll
25 have 32 minutes for rebuttal. I did the math right this time. Petitioner, you
26 have 13 minutes and you can start when you're ready.

1 MR. SAIDMAN: Okay. Your Honor, I'll start with Ground 1,
2 Independent Claims 1 and 11. I just want to make clear our position on the
3 inconsistency point. I'm going to turn to Slide 24. So, as we talked about in
4 the opening, Conn discloses an anchor via pattern that's high density, that's
5 along the length, along the width, and it's uniform across the substrate. And
6 so the question is, where is -- are we talking about the outer bounds of the
7 claim or are we not?

8 And I think if you look at the left-hand side of Slide 24, you can
9 see that there's a space in between where both parties agree that an anchor
10 via, if it's located in that location, it is disposed in the corner. So, we are not
11 here to talk about what are the outer limits of that claim and what are the
12 outer limits of what it means to be a corner, perhaps where the parties
13 disagree. But the parties are clear that where there's an anchor via disposed
14 in the corner and it's outside that ovoid shape within the limits of the hash
15 lines, it's in the corner.

16 JUDGE PESLAK: Which one are you referring to?

17 MR. SAIDMAN: On the -- Slide 24, the left-hand side. So you
18 can see --

19 JUDGE PESLAK: You're saying the upper left is --

20 MR. SAIDMAN: I'm sorry. I was looking at the upper left, but it
21 could be upper left, upper right. But any one of the corners, there is a space
22 that overlaps between what Samsung has identified, what we've identified as
23 in the corner, and the space that Patent Owner has identified.

24 JUDGE PESLAK: Oh, you're talking about -- okay. So, the two
25 lines -- you're talking about the lines on the left side, they both -- the line,
26 the outer perimeter of the via intersects that ovoid, whatever that shape is.

1 MR. SAIDMAN: That's right.

2 JUDGE PESLAK: Football shape.

3 MR. SAIDMAN: That's right. So, if there are no further questions
4 on Claims 1 and 11, I'm happy to turn to Claim 9. And I'll turn to Slide 18.
5 Excuse me, not Side 18. No, correct. Excuse me, Slide 28. So as we talked
6 about, Conn does have an express disclosure that it's a mechanical
7 connection. Now their argument is, look, it says it's a conductor. But just
8 because it's a conductor and it's an electrical conduit, that's not enough. The
9 claim is, does it provide a ground connection to an active device? And it
10 doesn't. It's a mechanical connection. There's no indication that these via
11 conductors provide any sort of ground connection to active devices.

12 And then finally on Ground 2, and I want to focus on, this is Slide
13 27. So, there's a discussion of, well, does Ground 2 cover a ground
14 connection or does it cover active devices? And I think the argument is
15 parsing the claims a little too thin. So as we showed in the opening, there
16 are multiple recitations about how Claims 9 and 19 and the ground
17 connection is rendered obvious.

18 I appreciate opposing Counsel points to active devices, but the
19 claims themselves, you can see here on the bottom left, an anchor via does
20 not provide a ground connection to one or more active devices. They're part
21 and parcel of the same claim limitation. So, if there are no further questions
22 on Ground 2, I'll hand it over to Mr. Zang for the remaining grounds.

23 JUDGE PESLAK: Thank you.

24 MR. ZANG: Your Honor, I will first direct your attention to Slide
25 40. So, this is about the Gambino ground. So earlier, Patent Owner's
26 Counsel argues that the paragraph 20 of Gambino only disclosed the

1 backside grounding method to flushing the surface of the metal filler.
2 However, nowhere in Gambino disclosed this method cannot result in a
3 protruding portion. So, HID's argument is incorrect. And in fact, as shown
4 on Slide 43 and 44, Dr. Thompson opined in his opening and supplemental
5 declarations that the backside grounding method can result in a protruding
6 portion.

7 And next, I will want to direct your attention to Slide 42. That is
8 about Gambino's teaching of not providing ground connection to one or
9 more active devices. So, I just want to point out that Patent Owner did not
10 show you the top view of this Gambino's semiconductor substrate. So, if
11 you actually look at the Figure 3 of Gambino, it shows that the dummy metal
12 pad is located in the corner area of the semiconductor substrate. However,
13 the main backside metal 16 is located in the center portion of the
14 semiconductor substrate.

15 So, if you just place the pounds anchor via in the dummy metal
16 pad, and extend it to the front side, which is not shown in this figure, but you
17 can imagine in the front side there will be active devices. So similarly, the
18 active devices should be also located directly above the main backside
19 metal, not above the corner dummy metal pad. So, that is Petitioner's
20 position that Gambino teaches not providing ground connections to active
21 devices, even if the anchor via extends fully from the bottom side of the
22 semiconductor substrate to the front side of the substrate.

23 If there's no questions, I will go to Slide 49, which is about the
24 Torii ground. So earlier, I heard Patent Owner's Counsel say that Torii does
25 not disclose the negative limitation of not providing ground connections to
26 one or more active devices. That's not correct. I mean, if you look at this

1 disclosure in paragraph 48 of Torii, it does say that the dummy of sub-TSV
2 is normally not used as a current pathway. That yes, here suggests this is a
3 mandatory feature of sub-TSV.

4 As a comparison, if you look at the second half of the sentence, it
5 says can be. So, can be signal a permission or ability. It does not require the
6 sub-TSV to serve as a current pathway. So this is a positive disclosure of a
7 negative limitation.

8 And next, I want to -- this is my last rebuttal, which is Slide 60.
9 So, I just want to point out, Patent Owner's Counsel is incorrect when he is
10 referring to it is undisputed that the adhesive bond between metal and
11 substrate requires direct contact. That's not correct. First of all, as you
12 pointed out, Your Honor, the claim does not recite an adhesive bond.

13 And second, as shown on the right-hand side of the Slide 60,
14 Burnham teaches that an oxide layer placed in between the backside metal
15 layer and a semiconductor substrate can improve the adhesion of the
16 backside metal adhesion to the substrate.

17 So, the Patent Owner's statement -- attorney argument is directly
18 contrast with the objective evidence. This is just like you are using a glue to
19 stick two objects together, right? The glue will serve as an intermediate
20 layer in between as a bonding material to bind these two objects. So, there's
21 no requirement for the adhesive bond to suggest any direct contact. So with
22 that, I will stop here. Does Your Honor have any questions?

23 JUDGE PESLAK: I don't. Judge Jung?

24 JUDGE JUNG: I have no questions.

25 JUDGE PESLAK: Any questions, Judge Anderson?

26 JUDGE ANDERSON: No, I don't have any. Thank you.

1 MR. ZANG: Thank you, Your Honor.

2 JUDGE PESLAK: Patent Owner, you have 32 minutes if you
3 want to use it. As rebuttal to what they said.

4 MR. COWELL: I never make promises, but I don't think I'm
5 going to use 32 minutes. So, I'm going to start right where Counsel left off
6 again. I'm on Slide 60 of Petitioner's slides. And he said, a-ha Burnham
7 uses an oxide layer to improve adhesion. There's a couple of points there.
8 One, Burnham's not talking about the adhesive bond. Bond in this context
9 means molecules of one layer interacting with the other to bond it. The glue
10 bonds it. The molecules of the glue bond to the substrate.

11 But more importantly, whenever, and this is true of all the extrinsic
12 evidence they cite and all the cases they cite, whenever there's an
13 intervening layer, it is explicitly described. Burnham uses an oxide layer as
14 an intermediate adhesion layer. Counsel didn't show us this slide earlier.
15 Sharma, an optional intermediate layer composed of a mixture of vanadium
16 and silver, et cetera. It's explicitly addressed, it's explicitly included, and it's
17 explicitly described. I think our briefing addresses every single example
18 they put up there.

19 Now, we talked about -- I'm just going to move backwards, and we
20 talked about Gambino. And he agreed, Gambino doesn't discuss protrusion.
21 And there's no evidence in petition as to the protrusion. He didn't agree with
22 that, but that's true. That's why they had to put in a supplemental
23 declaration. That's why they start reaching out to Torii and to Burnham and
24 to other references that are not part of the combination. Burnham is silent on
25 it. There's no reason to infer it.

26 He also asked about the figure, and he said, let's look at Figure 5,

1 and we have the main metal plane here. And so, of course, the devices are
2 right across the main metal plane. There's no disclosure of that. He's asking
3 us to guess where Gambino puts its devices based on no evidence. That
4 can't meet his burden of showing by preponderance that the claim is
5 obvious. And unless the Board has any questions, I think that's it from me.

6 JUDGE PESLAK: Judge Anderson, any questions?

7 JUDGE ANDERSON: Sorry about the delay. No, I don't have
8 any questions.

9 MR. COWELL: Thank you very much, Your Honors.

10 JUDGE PESLAK: So, before we go off the record, there's another
11 issue we'd like to address with the parties. There hasn't been any discussion
12 today of Ground 2B, which is in view of knowledge of POSITA and
13 Applicant-admitted prior art. And the office issued new guidance on AAPA
14 this summer, which revoked the prior guidance and only applies to cases
15 filed after September 1st, 2025. But that was in light of the Federal Circuit's
16 case decision in the second *Qualcomm v. Apple* case 134 F.4th 1355, which
17 tells us when we can consider Applicant-admitted prior art in an IPR.

18 So, we would like supplemental briefing from the parties as to the
19 application of *Qualcomm v. Apple* to Ground 2B. We'd like Petitioner to go
20 first and provide a five-page brief by January 14th. Can you do that in that
21 timeframe?

22 MR. SAIDMAN: Yes, Your Honor.

23 JUDGE PESLAK: And then Patent Owner can respond with a
24 five-page brief on January 21st. Is the timeframe okay for you?

25 MR. COWELL: Just because I'm not sure I heard correctly, you
26 said January 21st?

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IPR2024-01405 (Patent 9,245,826 B2)

1 JUDGE PESLAK: January 21st.

2 MR. COWELL: Yes, we can do that.

3 JUDGE PESLAK: Okay. And both sides understand what we're
4 asking here? I just want to make sure it's clear.

5 MR. SAIDMAN: Yes, we understand, Your Honor.

6 JUDGE PESLAK: Okay. And Patent Owner?

7 MR. COWELL: Yes, we understand.

8 JUDGE PESLAK: Okay. With that, the hearing is closed. We'll
9 take the case under advisement. I want to thank both sides today. It was a
10 very informative presentation.

11 (Whereupon, the above-entitled matter went off the record at 3:47
12 p.m.)

IPR2024-01403 (Patent 7,772,673 B1)

IPR2024-01405 (Patent 9,245,826 B2)

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