

571-272-7822

Entered: March 13, 2026

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,
Patent Owner.

IPR2024-01405
Patent 9,245,826 B2

Before HYUN J. JUNG, GREGG I. ANDERSON, and
ARTHUR M. PESLAK, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

JUDGMENT

Final Written Decision

Determining All Challenged Claims Unpatentable
Denying Petitioner's Motion to Exclude Evidence - Paper 27
35 U.S.C. § 318(a)

I. INTRODUCTION

Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively “Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1–20 (“the Challenged Claims”) of U.S. Patent No. 9,245,826 B2 (“the ’826 patent,” Ex. 1001). Paper 1 (“Pet.”). Petitioner filed a Declaration of Dr. Scott E. Thompson, Ph.D., in support of the Petition. Ex. 1003. Harbor Island Dynamic, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7. On March 24, 2025, we instituted this *inter partes* review. Paper 9 (“Dec.”).

On June 16, 2025, Patent Owner filed a Patent Owner’s Response (“PO Resp.”). Paper 17. In support of the Patent Owner’s Response, Patent Owner filed a Declaration of John Berg. Ex. 2004. On September 8, 2025, Petitioner filed a Reply to the Patent Owner’s Response (“Pet. Reply”). Paper 20. In support of the Reply, Petitioner filed a Supplemental Declaration of Dr. Scott E. Thompson, Ph.D. Ex. 1034. Patent Owner filed a Sur-reply (“Sur-reply”). Paper 23. Oral argument was held on January 6, 2026, and a transcript is entered in the record. Paper 41 (“Tr.”).

Petitioner filed a Motion to Exclude Evidence. Paper 27 (“MTE”). Patent Owner filed an Opposition to the Motion to Exclude. Paper 30 (“MTE Opp.”). Petitioner filed a Reply. Paper 35 (“MTE Rep.”).

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the Challenged Claims. For the reasons discussed below, we determine that Petitioner establishes by a preponderance of the evidence that all Challenged Claims are unpatentable. We also deny Petitioner’s Motion to Exclude as moot.

A. Related Matters

The parties identify the following proceeding as a related matter: *Harbor Island Dynamic, LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, No. 2:24-cv-00140-JRG-RSP (E.D. Tex.) (“District Court Litigation”). Pet. 104; Paper 6 (Patent Owner’s Mandatory Notices), 2.

B. Real Parties in Interest

Petitioner identifies “Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.” as the real parties-in-interest. Pet. 104. Patent Owner identifies “Harbor Island Dynamic, LLC” as the real party-in-interest. Paper 6, 2.

C. The ’826 patent (Ex. 1001)

The ’826 patent relates “to anchor vias for improved backside metal adhesion to a semiconductor substrate.” Ex. 1001, 1:42–44. The disclosure states “miniaturization and increased density in semiconductor substrates has typically relied on a backside metal layer attached to the substrate.” *Id.* at 1:15–17. A conventional method of adhering a backside metal layer to a substrate includes bonding via adhesive which can result in reduction of fabrication yields due to the backside metal layer peeling away from the semiconductor substrate. *Id.* at 1:24–27, 1:36–38.

Figure 1A is reproduced below:

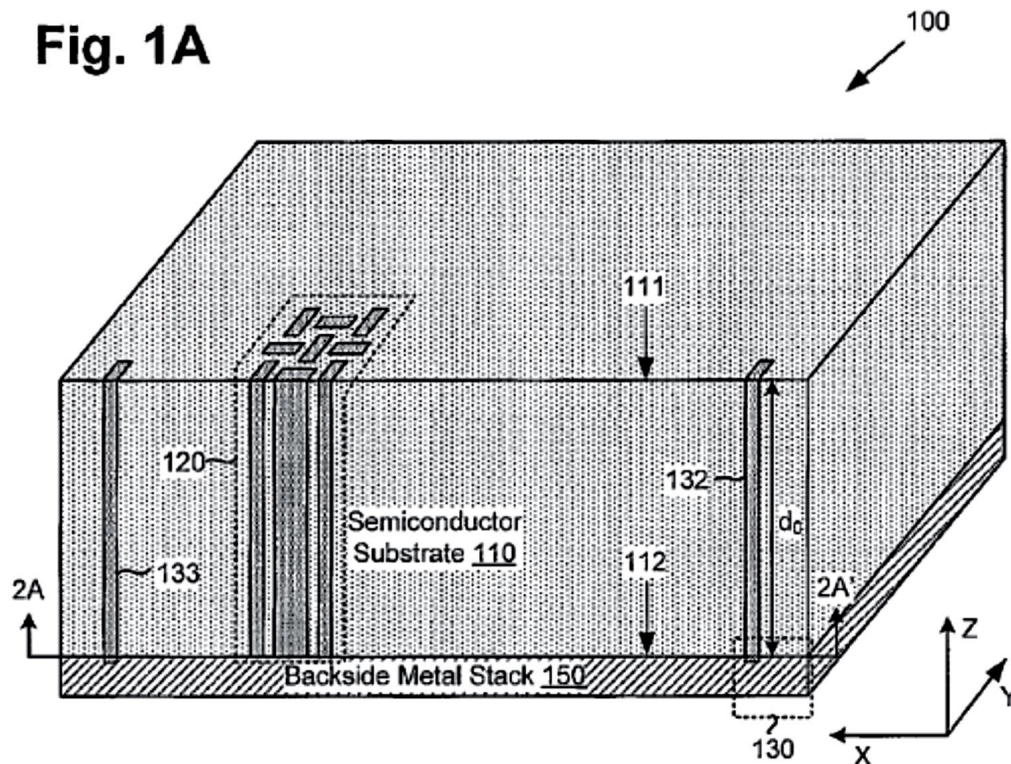


Figure 1A is a “cross-section of a semiconductor structure having anchor vias for improved backside metal adhesion.” Ex. 1001, 1:50–52. The semiconductor structure 100 includes a semiconductor substrate 110 having a top surface 111 (“front side”), polished bottom surface 112 (“backside”), backside metal stack 150, a group 120 of through silicon vias (TSVs) formed in a core region, and anchor vias 132, 133 formed in a peripheral region. *Id.* at 2:57–66, 3:2–5. Metal filler of the TSV group 120 provides ground connection to devices in the core region. *Id.* at 3:5–7. By contrast, metal filler within the anchor vias 132, 133 does not provide ground connections but rather physical anchor points between semiconductor substrate 110 and the backside metal stack 150. *Id.* at 3:12–17.

Figure 1B is reproduced below:

Fig. 1B

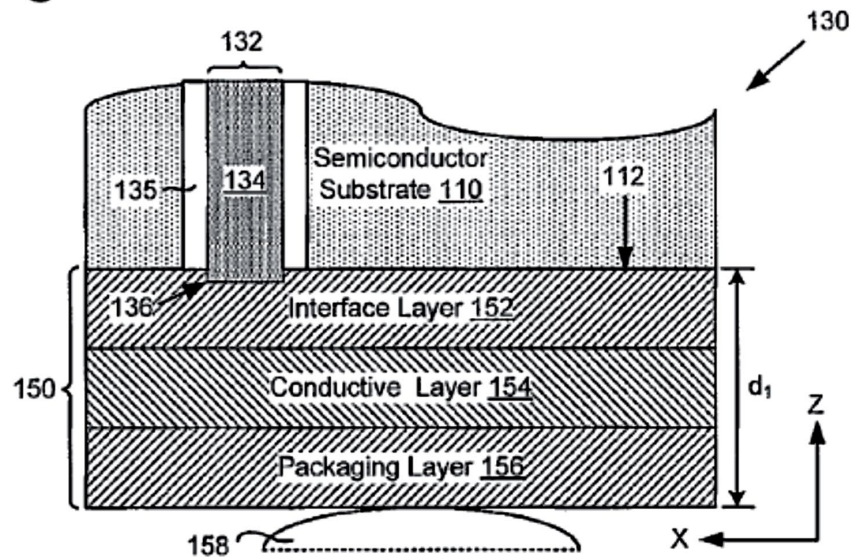


Figure 1B is “a magnified cross-section of a portion of an anchor via for improved backside metal adhesion.” Ex. 1001, 1:54–56. The magnified view 130 shows anchor via 132, backside metal stack 150 formed on bottom side 112 of semiconductor substrate 110, insulating silicon dioxide layer 135 on the sidewalls of anchor via 132, and metal filler 134 in anchor via 132. *Id.* at 3:36–43. The metal stack 150 includes an interface titanium layer 152, a nickel conduction layer 154, and a gold packaging layer 156 adjoining a printed computer board (PCB) contact 158 of another device. *Id.* at 3:49–59. A portion 136 of metal filler 134 protrudes past bottom side 112 of semiconductor substrate 110 to provide additional contact and, thereby, a stronger physical, metal-on-metal bond between the metal filler 134 and interface layer 152. *Id.* at 3:43–48.

D. Illustrative Claim

Claims 1 and 11 are independent claims. Claim 1 is reproduced, below, with Petitioner’s limitation identifiers in brackets (Pet. 1):

1. [1pre]¹ A structure comprising:

[1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;

[1b] a metal filler within said at least one anchor via, said metal filler having a protruding portion extending from a backside of said semiconductor substrate;

[1c] a backside metal layer on a bottom surface of said semiconductor substrate, said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via;

[1d] wherein said metal filler within said at least one anchor via does not provide ground connection to one or more active devices in said semiconductor substrate.

Ex. 1001, 7:58–6:3.

¹ Petitioner identifies claim limitations by claim number followed by letter designations. *See, e.g.*, Pet. 28–36 (claim 1).

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–20 would have been unpatentable on the following grounds (Pet. 23):

Ground	Claim(s) Challenged	35 U.S.C. §²	References/Basis
1	1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	102	Conn ³
2A	1, 2, 4–7, 9, 11, 12, 14–17, 19	103(a)	Conn
2B	8, 18	103(a)	Conn, AAPA
3A	1, 2, 4–7, 11, 12, 14–17	103(a)	Gambino ⁴ , Conn
3B	10, 20	103(a)	Gambino, Conn, Ding ⁵
4	1, 8–11, 18–20	102	Torii
5	1–3, 9, 11–13, 19	102	Ide

II. ANALYSIS

A. Overview

Petitioner bears the burden of establishing the unpatentability of the Challenged Claims by a preponderance of the evidence. 35 U.S.C. § 316(e);

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102, 103. Because the ’826 patent claims priority to an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA version of §§ 102 and 103 applies.

³ U.S. Patent Application Publication No. 2009/0079056 A1, pub. Mar. 26, 2009 to Conn (Ex. 1004).

⁴ U.S. Patent Application Publication No. 2014/0138844 A1, pub. May 22, 2014 to Gambino et al. (Ex. 1005).

⁵ U.S. Patent Application Publication No. 2012/0104546 A1 pub. May 3, 2012 to Ding et al. (Ex. 1008).

37 C.F.R. § 42.1(d). This burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

To establish anticipation under 35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyConn, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable under § 103(a) as obvious if the differences between the subject matter of the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious invention was made to a person having ordinary skill in the art to which the claimed invention pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying

factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).⁶ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained in *KSR International Co. v. Teleflex Inc.* that:

[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original)).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted). “[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61

⁶ No evidence of secondary considerations has been presented by the parties.

(Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art “would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems” and “[a]dditional relevant work experience can compensate for less education, and *vice versa*.” Pet. 23 (citing Ex. 1003 ¶¶ 73–74).

Patent Owner’s declarant, Mr. Berg testified that “engineers working in this field, and implementing designs such as that described in the ’826 Patent, typically have bachelor’s degrees.” See PO Resp. 17 (citing Ex. 2004 ¶ 26). According to Patent Owner, “[s]uch engineers are the target audience for the ’826 Patent, and thus, a [person of ordinary skill in the art] need not have a master’s degree.” *Id.*

Patent Owner contends that a person of ordinary skill in the art “would have (1) a Bachelor of Science degree or equivalent degree in electrical engineering, physics, materials science, or a similar field” along with “(2) at least two years of industry experience in semiconductor design and/or fabrication.” Patent Owner also submits that “[a]dditional formal education (such as Master of Science degrees) would compensate for less technical experience and *vice versa*.” PO Resp. 17 (citing Ex. 2004 ¶¶ 23–26).

Petitioner, in turn, argues that Patent Owner’s attempt to draw a distinction based on a bachelor’s degree as opposed to a master’s degree “is immaterial.” Pet. Reply 3. Petitioner further argues that “[b]oth parties

agree that a [person of ordinary skill in the art] would have at least two years of experience in semiconductor design and fabrication, and nothing in [the Patent Owner Response] identifies any analysis that would turn on whether a [person of ordinary skill in the art] held a bachelor’s or master’s degree.” *Id.*

We agree with Petitioner that the differences between the parties’ proposed levels of skill in the art are immaterial for the purposes of this Decision. We apply Petitioner’s proposed level of skill in the art because it appears consistent with the problems addressed in the ’826 patent and the prior art. Further, our determination in this case would not be affected if we were to adopt Patent Owner’s proposed level of skill in the art.

C. Claim Construction

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b) (2023). Accordingly, we construe each challenged claim of the ’826 patent to generally be “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

If the specification “reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is “when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Uship Intellectual Props., LLC v. United States*, 714 F.3d

1311, 1313 (Fed. Cir. 2013) (quoting *Thorner v. Sony Comput. Ent. Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Petitioner argues that “[i]ndependent method claim 11 does not require the steps therein to be performed in their recited order.” Pet. 20. In particular, Petitioner contends that limitations [11b] (“depositing a metal filler within said at least one anchor via, said metal layer having a protruding portion”) and [11c] (“forming a backside metal layer . . . said backside metal layer being bonded to said protruding portion of said metal filler of said at least one anchor via”) need not be performed in their recited order. *Id.* at 20–21.

Petitioner contends that the “grammar does not suggest an order because the claimed ‘forming a backside metal layer on a bottom surface of said semiconductor substrate’ does not mention anything about the ‘metal filler’ and that “[l]ogic also does not suggest an order because the backside metal layer is formed ‘on a bottom surface of said semiconductor substrate,’ not the ‘metal filler.’” Pet. 21. Petitioner further contends that “claim 11 does not recite that the bonding is an affirmative step that happens at any particular time or depends on the order of [11b] and [11c].” *Id.* Petitioner also argues that “the specification does not describe any specific method for making the structures.” *Id.* at 22.

Patent Owner does not dispute Petitioner’s proposal. PO Resp. 29.

We have reviewed Petitioner’s contentions and evidence and determine that claim 11 does not require that steps [11b] and [11c] be performed in the recited sequence.

Patent Owner offers two proposed claim constructions. First, Patent Owner contends that the limitation in claim 1 “disposed in at least one

corner of a semiconductor substrate” should be construed as “located outside a round or ovoid geometric shape inscribed within the edges of the semiconductor die.” PO Resp. 18. Second, Patent Owner contends that the limitation in claim 1 “a backside metal layer *on* a bottom surface of said semiconductor substrate” should be construed as “a backside metal layer *in contact with* a bottom surface of said semiconductor substrate.” *Id.* at 25 (emphasis added).

1. “*disposed in at least one corner of a semiconductor substrate*”

Patent Owner argues this proposed claim construction issue only with respect to an alternate argument in connection with the anticipation and Conn grounds. *See* PO Resp. 32–38. For its primary argument in the Conn grounds and the remaining grounds, Patent Owner does not dispute that the prior art discloses “at least one anchor via disposed in at least one corner of a semiconductor substrate.” *See id.* at 45–62. Because we are persuaded by Patent Owner’s primary argument that Petitioner’s cited evidence does not show that Conn discloses this limitation, we need not address Patent Owner’s construction which only relates to its alternate argument for Conn.⁷

⁷ Patent Owner also argued that Petitioner’s position in district court that this claim term is “indefinite” is inconsistent with its position here that no construction is necessary. PO Resp. 18. In light of the Office’s recent change in policy set forth in *Revvo Techs, Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20 (Director Squires, Nov.3, 2025) (precedential), we asked the parties to brief the effect of this policy change on this proceeding. Paper 28, 34. Because we need not address the construction of this term to resolve any ground in this proceeding, we do not address whether Petitioner has provided a sufficient explanation for its inconsistent claim construction positions. Further, we note that *Revvo* dealt with the question of whether the petitioner in that case provided a sufficient

2. “*backside metal layer on a bottom surface*”

Patent Owner contends that this term should be construed as “a backside metal layer in contact with a bottom surface of said semiconductor substrate.” PO Resp. 25. According to Patent Owner, “[t]his is the plain meaning of ‘on’ as recited in the claims, and a [person of ordinary skill in the art] reading the claims in view of the specification, would understand that the claims require such contact.” *Id.* (citing Ex. 2004 ¶ 57). In support of this construction, Patent Owner argues the claim recites “on a bottom surface” and “if the metal layer could be on the substrate but not in direct contact, then the use of ‘surface’ would be irrelevant.” *Id.* at 26 (case citation omitted).

Patent Owner next contends dependent “[c]laims 9 and 19 draw a distinction between a layer ‘on’ the bottom surface of the substrate and a layer ‘overlying’ the substrate.” PO Resp. 26. According to Patent Owner, “[a]s a layer can overlie (or underlie) a substrate while not being in contact with its surface, a [person of ordinary skill in the art] would understand that the use of ‘on the bottom surface’ in claims 1 and 11 denotes direct contact.” *Id.* (citing Ex. 2004 ¶ 59).

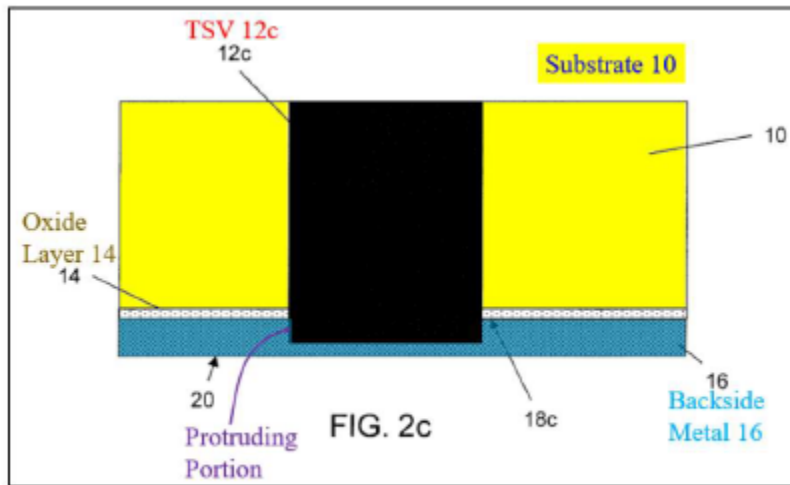
Patent Owner next contends that the Specification supports its construction. PO Resp. 27–28. In connection with Figure 1B, Patent Owner argues that the interface layer 152 “is ‘deposited on bottom side 112 of semiconductor substrate,’” “the conduction layer [154] is ‘then formed *on*

explanation to justify institution not whether a claim construction issue that need not be reached in an instituted proceeding would justify termination of an ongoing *inter partes* review with other grounds where construction of this claim term is not at issue.

interface layer 152” and “the packaging layer is then ‘formed *on conduction layer* 154.” *Id.* at 28 (citing Ex. 1001, 3:43–48, 3:51–55). According to Patent Owner, “[e]ach layer is in direct contact with the layer which it is ‘formed on’” and the cited portions of the Specification “confirm[] that the use of ‘on the bottom surface’ requires direct contact.” *Id.* (citing Ex. 2004 ¶¶ 62–63).

Petitioner reiterates its position from the Petition that “the plain and ordinary meaning of ‘on’ does not require direct contact.” Pet. Reply 9 (citing Pet. 84 n.12 (citing *AFG Indus., Inc. v. Cardinal IG Co.*, 239 F. 3d 1239, 1251 (Fed. Cir. 2001))). Petitioner further cites to several district court cases that it contends support its argument that “‘formed on’ does not require direct contact.” *See id.* at 10.

Relying on Dr. Thompson’s testimony, Petitioner contends that an ordinarily skilled artisan “would understand the terms ‘on’ or ‘formed on’ to mean ‘formed against with or without intervening layers.’” Pet. Reply 10 (citing Ex. 1034 ¶¶ 7–9). Petitioner supports this contention with reference to Exhibit 1022 (“Burnham”). Petitioner reproduces and annotates Burnham’s Figure 2C:



Burnham, Figs. 2c.

Pet. Reply 11. Figure 2C of Burnham “show[s] various structures and respective processing steps for manufacturing backside metal on a Si wafer.” Ex. 1022, 2:14–16. Petitioner annotates Figure 2C with yellow highlighting for substrate 10, blue highlighting for back side metal layer 16, black highlighting for TSV 12c, and identifying oxide layer 14 with brown type. Pet. Reply 11.

Petitioner contends that Burnham “discloses that it ‘relates to structures and methods of **forming** backside metal **on** a Si substrate (Si wafer),’ and ‘the oxide material can be **formed on** a backside of a Si wafer.’” Pet. Reply 11 (citing Ex. 1022, 2:28–36). Petitioner argues that the “oxide material is an intervening layer between the backside metal and Si substrate.” *Id.* Petitioner further argues that Exhibit 1021 similarly describes “a silver layer [is] **disposed on** the vanadium layer” and “[a]n optional **intermediate layer** . . . may be **disposed between** the vanadium layer and the silver layer.” *Id.* at 11–12 (citing Ex. 1021, 1:6–2:1).

For the following reasons, we do not adopt Patent Owner’s construction.

The crux of the dispute between the parties is whether the limitation “on a bottom surface” limits the backside metal layer to direct contact with the bottom surface of the semiconductor substrate or whether the claim language is broad enough to cover an intervening layer between the backside metal layer and the bottom surface of the semiconductor substrate.

We start by analyzing the claim language. Claim 1 recites, *inter alia*,

A structure comprising;
at least one anchor via disposed in at least one corner of a
semiconductor substrate;
...
a backside metal layer *on a bottom surface* of said semiconductor
substrate.

Ex. 1001, 7:58–65 (emphasis added).

Claim 1 uses the term “comprising” which is open-ended and normally does not exclude additional, unrecited elements. *See Mars Inc. v. H.J. Heinz Co.*, 377 F.3d 1369, 1376 (Fed. Cir. 2004). This is in contrast to the phrase “consisting of.” *See Multilayer Stretch Cling Film Holdings, Inc. v. Berry Plastics Corp.*, 831 F.3d 1350, 1358 (Fed. Cir. 2016) (there is an “exceptionally strong presumption that a claim term set off with ‘consisting of’ is closed to unrecited elements.”). The use of comprising in claim 1, thus, weighs against a construction limiting claim 1 to direct contact between the backside metal layer and the bottom surface of the semiconductor substrate. Additionally, we note that claim 1 does not recite that the backside metal layer is “directly on” or “formed on” the bottom surface or similar language that would suggest “direct contact” may be required. For these reasons, we determine that the language of claim 1 does not support Patent Owner’s proposed construction.

Patent Owner also attempts to draw a distinction between the language used in claim 9 of “a metal layer *overlying* said semiconductor substrate.” Ex. 1001, 8:28–30 (emphasis added). The “metal layer” recited in claim 9 is an additional layer not recited in claim 1. Consequently, the use of *overlying* with respect to this additional layer in claim 9 has little relevance to the construction of “on” in claim 1.

We now turn to the Specification.

Patent Owner does not argue that any part of the Specification meets the requirements of a lexicographic definition of “on” or a disavowal of the full scope of “on.” PO Resp. 25–29; Sur-reply 3–9.

The Specification describes that “backside metal layer stack 150 . . . *may be formed on* bottom side 112 of semiconductor substrate 110 as shown in more detail in FIG. 1B.” Ex. 1001, 3:15–17 (emphasis added). In connection with Figure 1B, the Specification further describes that “when interface layer 152 is deposited on bottom side 113 of semiconductor substrate 110, the additional contact between metal filler 134 and interface layer 152 form a very strong physical, metal-on-metal bond.” *Id.* at 3:45–48.

We agree with Patent Owner that Figure 1B shows direct contact between the backside metal layer and the bottom of the semiconductor substrate. However, the other language, quoted above, that the backside metal layer “*may be formed on*” suggests that direct contact is optional. This reading of the Specification aligns with the open-ended language of claim 1 that, as discussed above, does not necessarily require direct contact. Further, Patent Owner’s argument that Figure 1B supports its construction is

an improper attempt to import a limitation from that embodiment into claim 1.

Patent Owner does not direct us to any part of the prosecution history of the '826 patent in support of its construction. PO Resp. 25–28. Our review of the prosecution history does not reveal any portions relevant to this issue.

After considering all of the relevant intrinsic evidence, we determine that the scope of claim 1 includes direct contact between the backside metal layer and the bottom of the semiconductor substrate but does not require the backside metal layer be in direct contact with the bottom surface of the substrate.⁸

We determine that no express construction of any other claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

*D. Ground 1: Alleged Anticipation of
Claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 by Conn*

Petitioner contends that claims 1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, and 19 are anticipated by Conn. Pet. 24–45. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003.

⁸ Patent Owner also relies on testimony from Mr. Berg which substantially parrots the arguments in the Patent Owner Response and is, thus, entitled to little, if any, weight. *See* Ex. 2004 ¶¶ 56–63.

We begin with a brief summary of Conn. We then address the parties' respective contentions.

1. Conn (Ex. 1004)

Conn is titled “Large Substrate Structural Vias.” Ex. 1004, code (54). Conn “relates to a carrier substrate for mounting of semiconductor chip devices and components where the carrier substrate is resistant to thermal fatigue problems.” *Id.* ¶ 3.

Addressing the background of the invention, Conn states computing devices can require a large amount of power that largely increases the temperature of the devices. Ex. 1004 ¶ 5. These temperature changes cause fatigue of the electronic “package” structure, e.g., between the layers of a package laminate or between a packaged part and a PCB. *Id.*

In the invention, an electronic package includes a carrier substrate having first and second surfaces and a plurality of anchor vias having a via material extending from the first surface toward the second surface. Ex. 1004 ¶ 11.

Figure 1 is reproduced below:

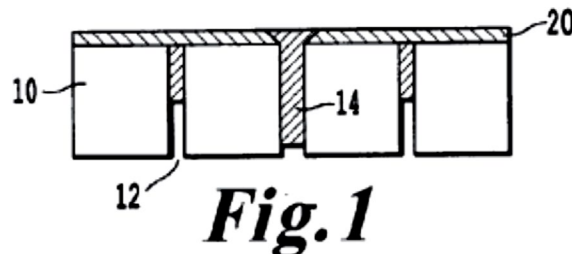


Figure 1 is a diagram depicting a side view of an electronic package. Ex. 1004 ¶ 17. The package includes a carrier substrate 10, a conducting layer 20 formed on a first main surface of the carrier substrate 10, and passive components (e.g., capacitors, resistors, and inductors) within the carrier substrate 10. *Id.* ¶ 26. The conducting layer 20 is connected to a via

conductor 14 formed in a via 12 and thereby providing an “anchor via” into the carrier substrate. *Id.* ¶ 28. The anchor via acts as a “rivet” whereby the conducting layer 20 maintains its structure under thermal stress. *Id.* The plural vias 12 can be “through-vias” or not span to the opposite surface of the carrier substrate 10. *Id.* The via conductor 14 enters at least partially into the via 12, but not necessarily all the way through the via 12, to form an array pattern of rivets securing the conducting layer 20 to the carrier substrate 10. *Id.* ¶¶ 29, 35; Fig. 2.

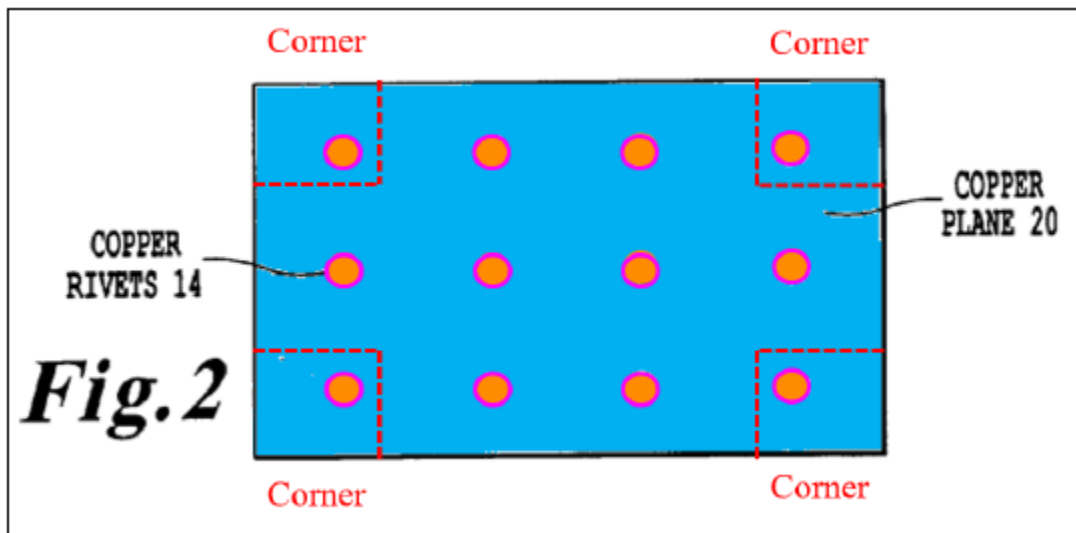
2. *Claim 1*

Petitioner provides a limitation--by--limitation analysis of claim 1, mapping each claim limitation to Conn. Pet. 28–38. Patent Owner argues Petitioner fails to show Conn teaches an anchor via disposed in the corner of the carrier substrate 10 as required by limitation [1a]. PO Resp. 32–37.

We agree with Patent Owner and focus our analysis on limitation [1a] which is dispositive.

“[1a] at least one anchor via disposed in at least one corner of a semiconductor substrate;”

Petitioner provides the following annotated version of Figure 2 of Conn:



Pet. 29. Figure 2 “depict[s] a top view of [an] electronic package according to an embodiment of the invention.” Ex. 1004 ¶ 18. Petitioner annotates Figure 2 by highlighting copper plane 20 blue, copper rivets 14 orange with a red circular border, and adding four dashed red-rectangles, with red text reading “Corner” outside each corner of rectangular copper plane 20. Pet. 29.

Petitioner contends Conn discloses carrier substrate 10 comprising “a plurality of anchor vias (e.g., via conductor 14).” Pet. 28 (citing Ex. 1004 ¶ 29). Petitioner further contends that Conn’s “Figure 2 shows the plurality of anchor vias . . . are ‘distributed relative to the conducting layer 20 in a pattern . . . cover[ing] the entire surface of conducting layer 20, such that [] anchor vias are disposed at the corners of conducting layer 20.” *Id.* at 28–29 (citing Ex. 1003 ¶ 83; Ex. 1004 ¶ 35, Fig. 2). Petitioner concedes that Figure 2 “does not show carrier substrate 10, but Conn discloses that conducting layer 20 can cover more than ‘90% of an entirety of the surface area of the carrier substrate,’ even approaching ‘100%.’” *Id.* at 29 (citing Ex. 1003 ¶ 84; Ex. 1004 ¶ 31). According to Petitioner, because of this disclosed

coverage of the conducting layer, “the corners of conducting layer 20 are also the corners of carrier substrate 10” and “the anchor vias located at the corners of conducting layer 20 are also located at the corners of carrier substrate 10.” *Id.* at 29–30 (citing Ex. 1003 ¶ 84).

Patent Owner, responds that Petitioner’s annotation of Figure 2 “delineating the ‘corner’ of the copper plane and orienting them in such a way to enclose one copper rivet in each corner” is “artificial.” PO Resp. 33. According to Patent Owner “*Conn* does not suggest that Fig. 2 represents any portion of the corner of a die” but “merely states that ‘[t]he via conductors can be distributed relative to the conducting layer 20 in a pattern as shown for example in FIG. 2.” *Id.* (citing Ex. 1004 ¶ 54; Ex. 2004 ¶ 81); *id.* at 34 (“describing that the anchor vias are distributed in ‘a pattern’ does not disclose that the anchor vias are disposed in the corners.”)

Patent Owner next contends that *Conn* is entirely silent as to the corners and edges of its semiconductor. For example, while *Conn* provides examples of distances between each via, it does not describe the distance between the vias and edges of the substrate.” PO Resp. 34 (citing Ex. 1003 ¶ 35; Ex. 2004 ¶ 83). Patent Owner argues that *Conn* does not teach that each via shown in Figure 2 is an anchor via. *Id.* at 34–35. According to Patent Owner, *Conn* only teaches that its conducting layers are connected by “at least one via conductor.” *Id.* at 35 (citing Ex. 1004 ¶ 38; Ex. 2004 ¶ 84).

Based on these arguments, Patent Owner contends that an ordinarily skilled artisan “reading *Conn* would understand that it is silent, and therefore does not disclose, anchor vias in the corners.” PO Resp. 36 (citing Ex. 2004 ¶ 87).

Petitioner, in turn, contends that Conn’s “pattern ‘spreads across the substrate and extends to its corners.’” Pet. Reply 16 (citing Pet. 38; Ex. 1004 ¶¶ 31, 35, Fig. 2). Petitioner next argues that “Conn discloses the anchor vias in this pattern have a spacing as small as 60 micrometers.” *Id.* at 16–17 (citing Ex. 1004 ¶ 35; Ex. 2009, 35:14–36:9, 39:25–40:14, 40:24–41:12). According to Petitioner, an ordinarily skilled artisan “would understand that this distance is ‘the width of a human hair,’ and ‘under any reasonable definition, that would be near the corner of the die.’” *Id.* at 17 (citing Ex. 2009, 35:14–36–9).

In response to Petitioner’s argument that Conn discloses anchors vias 60 micrometers from the corner, Patent Owner argues that Conn “actually states that its vias are spaced 60 micrometers apart.” Sur-reply 10 (citing Pet. Reply 16–17; Ex. 1004 ¶ 35).

Patent Owner next argues that if Conn’s Figure 2 “show[s] the entirety of a die”, as Dr. Thompson assumed, and “one applies the 60 micrometer distance between vias to the Figure, it would result in a wafer roughly 300 micrometers wide and 240 micrometers high.” Sur-reply 10–11. According to Patent Owner, such a wafer would be “far smaller than any existing semiconductor wafer, and orders of magnitude smaller than 140 mm by 80 mm size in Conn’s embodiment.” *Id.* at 11 (citing Ex. 1004 ¶ 36).

For the following reasons, Petitioner does not persuade us that Conn discloses this limitation.

Conn’s Figure 1 is reproduced below:

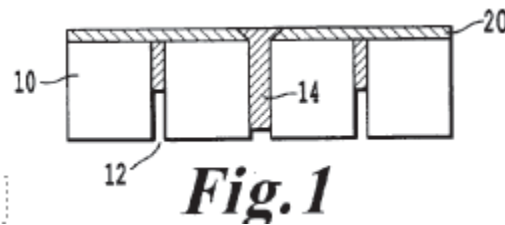


Figure 1 “is a side view through a carrier substrate 10.” Ex. 1004 ¶ 26. Conn discloses that conducting layer 20 is connected to at least a via conductor 14 formed in a via 12 thereby providing an anchor via.” *Id.* ¶ 28. In this side view, anchor via 14 is located between two other vias that Petitioner does not contend constitute anchor vias. Pet. 29. Consequently, in this side view, the non-anchor vias to the right and left of anchor via 14 are arguably located in the corners of the substrate not anchor via 14.

Petitioner also relies on an annotated version of Conn’s Figure 2 for this limitation. Pet. 29. We reproduce Conn’s Figure 2 without Petitioner’s annotations:

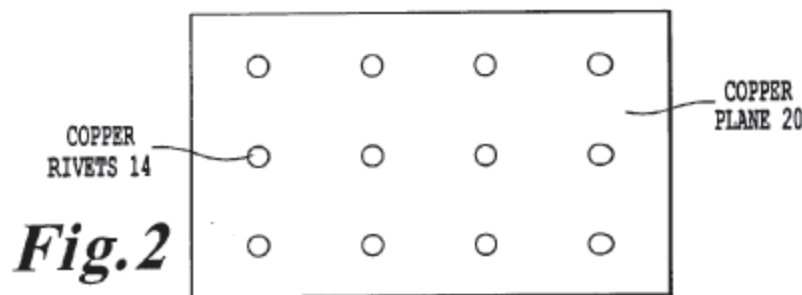
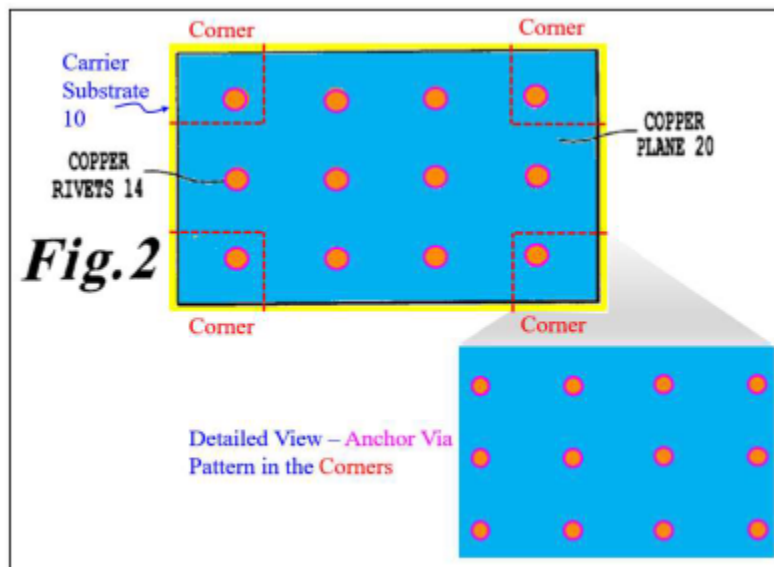


Figure 2 “is a diagram depicting a top view of [Conn’s] electronic package.” Ex. 1004 ¶ 18. Figure 2 is further described as showing a distribution pattern of via conductors relative to the conducting layer 20. *Id.* at ¶ 35. We have reviewed the text of Conn and do not locate any explicit disclosure that anchor vias 14 are located in a “corner” of the substrate in Figure 2.

Figure 2 includes text “Copper Rivets⁹ 14” with a line pointing to the middle horizontal row of circles. This placement of copper rivets 14 corresponds with Figure 1 which shows anchor vias 14 between two other vias that are not anchor vias. The disclosure of Figures 1 and 2 taken together supports Patent Owner’s position that Petitioner has not shown that Conn discloses anchor vias located in a corner of the semiconductor substrate.

Petitioner relies on paragraphs 31 and 35 of Conn for disclosure that the pattern of Figure 2 extends to the corners of the substrate. *See* Pet. Reply 16. However, those paragraphs do not describe that anchor vias 14 are located in or extend to the corner of the substrate. *See* Ex. 1004 ¶¶ 31, 35.

In the Petitioner’s Reply, Petitioner provides an additional annotated version of Conn’s Figure 2:



Conn, Fig. 2 (modified).

⁹ Conn alternately describes anchor vias 14 as “rivets.” Ex. 1004 ¶ 29.

Pet. Reply 16. In this annotated version of Figure 2, Petitioner adds an additional blue drop box from one of the rectangles it labels with “Corner.” *Id.* Inside the blue drop box is what Petitioner’s contends is an alleged pattern of anchor vias inside the red rectangle it added to Figure 2 labelled “Corner.” *Id.*

The source of both of Petitioner’s annotated versions of Figure 2 is Dr. Thompson. Ex. 1003 ¶ 83; Ex. 2009, 45:2–46:9. The blue drop box shown above does not appear in Conn and reflects Dr. Thompson’s interpretation of Conn. Ex. 2009, 45:2–46:9.

Petitioner fails to address the disclosure in Conn’s Figure 1 which supports a finding that anchor vias 14 are not located in the corner of the substrate. Pet. 28–30; Pet. Reply 15–17. As explained above, Conn’s Figure 2, with the middle row of vias labelled as “Copper Rivets,” is consistent with the disclosure of Figure 1.

Petitioner’s contention that Conn discloses anchor vias in the corners of the substrate is based on Dr. Thompson’s testimony. In his first declaration, Dr. Thompson relies on Conn’s paragraphs 31 and 35 to support the annotated version of Figure 2 in the Petition. Ex. 1003 ¶¶ 83–84. As discussed above, paragraphs 31 and 35 do not disclose that the anchor vias 14 are located in the corner of the substrate.

The second annotated Figure 2 shown in Petitioner’s Reply does not appear in either of Dr. Thompson’s declarations (*See* Ex. 1003, Ex. 1034). It appears to be mere attorney argument not evidence. Dr. Thompson testified in his deposition that the second annotated version is based on his interpretation of Conn. Ex. 2009, 45:2–46:9. Because Dr. Thompson’s testimony is not adequately supported by the disclosure of Conn, we find

that his testimony on the point of whether Conn discloses anchor vias located in the corner of the substrate is entitled to little, if any, weight. 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”). Therefore, because Petitioner has the burden of proof, we find that Petitioner has not shown that Conn discloses this limitation.

For these reasons, Petitioner has not shown by a preponderance of the evidence that claim 1 or claims 2, 4, 5, 7, and 9 which depend from claim 1 are anticipated by Conn.

For independent claim 11, Petitioner argues that claim 11 “is substantially similar to claim 1, except it recites a method for making the structure in claim 1” and “recites the same structural features of the anchor vias as those in claim 1.” Pet. 44. Consequently, Petitioner has not shown by a preponderance of the evidence that claim 11 or claims 12, 14, 15, 17, and 19 which depend from claim 11 are anticipated by Conn.

E. Grounds 2A and 2B: Alleged Obviousness of Claims 1, 2, 4–7, 8, 9, 11, 12, 14–17, 18, and 19 over Conn

Petitioner presents Grounds 2A and 2B as alternatives to Ground 1. Pet. 45–56.

For Ground 2A, Petitioner does not further address limitation 1[a] but focuses on the “backside metal layer.” Pet. 45–51; PO Resp. 43–44. Consequently, Petitioner does not cure the deficiency discussed above for Ground 1.

For these reasons, we find that Petitioner does not show by a preponderance of the evidence that claims 1, 2, 4–7, 8, 9, 11, 12, 14–17, 18,

and 19 would have been obvious over Conn and the knowledge of a person of ordinary skill in the art.

For Ground 2B, Petitioner addresses claims 8 and 18 not claim 1. Pet. 54–56. Consequently, Petitioner does not cure the deficiency discussed above for Ground 1.

For these reasons, we find that Petitioner does not show by a preponderance of the evidence that claims 8 and 18 would have been obvious over Conn and the knowledge of a person of ordinary skill in the art.

F. Ground 3A: Alleged Obviousness of Claims 1, 2, 4–7, 11, 12, and 14–17 over Gambino in view of Conn

Petitioner contends claims 1, 2, 4–7, 11, 12, and 14–17 would have been obvious over Gambino in view of Conn. Pet. 56–79.

We begin with a brief summary of Gambino. We then address the parties’ contentions.

1. Gambino (Ex. 1005)

Gambino “relates to semiconductor structures and, more particularly, to patterned backside metal ground planes for improved metal adhesion and methods of manufacture.” Ex. 1005 ¶ 1. Gambino states “[p]ackaging lead inductance is a major design issue,” e.g., whereby the emitter ground leads of some HBT designs contact the package via wire bonds or flip-chip solder bumps. *Id.* ¶ 2. Wire bond package ground leads have an undesirably high inductance. *Id.* Flip chips have undesirably high packaging complexity and cost. *Id.*

Gambino discloses patterning metal on a backside surface of a substrate and these limited regions “contact through-silicon vias.” Ex. 1005 ¶ 15; *see also id.* ¶¶ 23–26 (patterning process). The backside metal is

formed only on the die (e.g., not in any dicing channel) and “patterned differently than wiring” to form patches of metal coupled to the same potential (e.g., ground). *Id.* Because the patterned backside metal ground plane is not deposited in the dicing channel, the invention solves a prior problem that dicing of a substrate having blanketed metal can stress the metal-silicon interface in the dicing channel and thereby cause peeling of the metal from the corners and edges of the die. *Id.* ¶¶ 16–17.

Figure 3 is reproduced below:

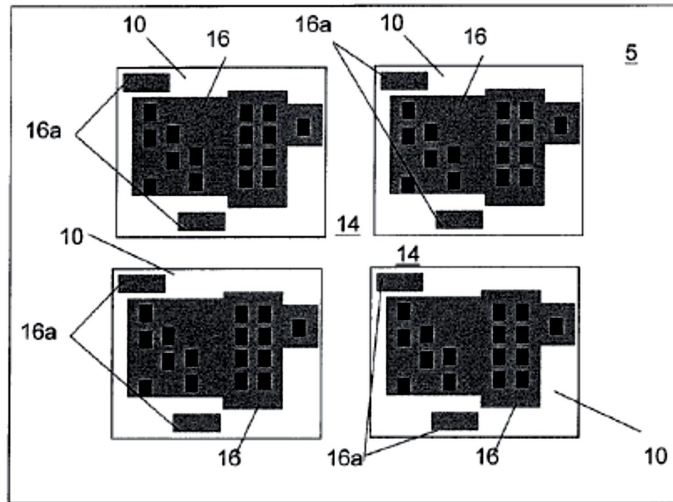


Figure 3 “shows a patterned backside metal with metal pads and methods of manufacture in accordance with additional aspects of the present invention.”

Ex. 1005 ¶ 11. Backside metal 16 is patterned into metal pads 16a over TSVs¹⁰ 12. Ex. 1005 ¶¶ 27–28. The metal pads 16a are configured (e.g., located and shaped) such that the dies 10 sit flatly on the package substrate and add mechanical support to the dies 10. *Id.* ¶ 28.

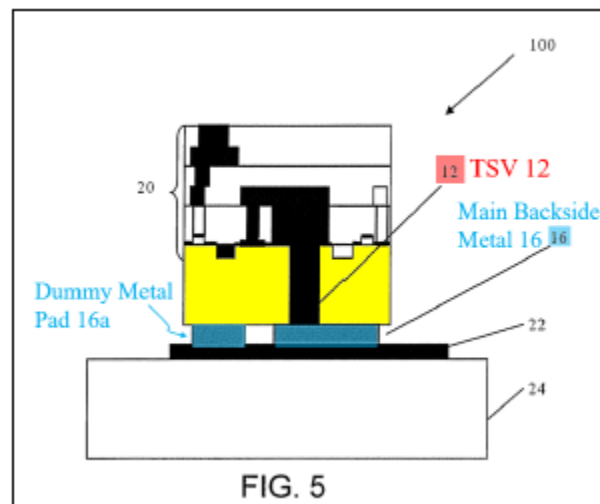
¹⁰ “TSV” is an acronym for “through silicon vias.” Ex. 1005 ¶ 4.

2. Claim 1

Petitioner provides a limitation-by-limitation analysis of claim 1, mapping each claim limitation to the combination of Conn and Gambino and setting forth reasons why an ordinarily skilled artisan would have been motivated to combine the teachings of Conn and Gambino with a reasonable expectation of success. Pet. 59–70. We start with motivation to combine/reasonable expectation of success.

a. Motivation to Combine and Reasonable Expectation of Success

Petitioner provides the following annotated version of Gambino's Figure 5:



Pet. 60. Figure 5 is “a packaged module with a backside metal ground plane attached to a substrate.” Ex. 1005 ¶ 13. Petitioner adds blue text to the left side of Figure 5, “Dummy Metal Pad 16a” with a blue arrow pointing to element 16a, blue text to the lower right, “Main Backside Metal 16,” and red text to the upper right of Figure 5, “TSV 12.” Pet. 60.

Petitioner contends that Gambino discloses a packaged module comprising metal wiring layers 20 in communication with TSV 12, back side metal 16 connected to substrate ground plane 22 which is bonded to

substrate 24, and dummy metal pads 16a located at the corners and peripheries of the substrate “to provide mechanical support.” Pet. 59 (citing Ex. 1005 ¶¶ 13, 27, 28, 30, Figs. 3, 5). Petitioner further contends that back side metal 16 covers the electrical TSV’s. *Id.* Petitioner next contends that an ordinarily skilled artisan “would have found it obvious to apply *Conn*’s teachings to create anchor vias in *Gambino*’s dummy metal pads 16a and/or main backside 16, to secure them to the substrate and prevent delamination during singulation.” *Id.* at 60 (citing Ex. 1003 ¶ 135).

Petitioner argues *Gambino* and *Conn* are both directed to improving structural integrity of packaged devices (Pet. 61 (citing Ex. 1003 ¶ 136; Ex. 1004 ¶ 11; Ex. 1005 ¶ 1)), “there would have been a desire to improve *Gambino* by adding *Conn*’s anchor vias at dummy metal pads 16a and main backside metal 16, to ensure they remain secured to the substrate” (*id.* at 62 (citing Ex. 1003 ¶ 137)), and an ordinarily skilled artisan would have been interested in combining the techniques of *Gambino* (backside dummy metal pads) and *Conn* (anchor vias) “to maximize backside metal adhesion” (*id.* at 63 (citing Ex. 1003 ¶ 140)).

Petitioner next argues that “the process of making the proposed combination is predictable because the same process used for manufacturing *Gambino*’s electrical TSVs can be used to manufacture the anchor vias.” Pet. 64 (citing Ex. 1003 ¶ 142). Petitioner further argues that Dr. Thompson illustrates that “*Gambino*’s method can yield the same rivet-like anchor via structure contemplated by *Conn*—the resulting via conductors will form protruding portions bonded to the backside metal.” *Id.* (citing Ex. 1003 ¶ 142).

Petitioner next contends that “the function of the resulting combination is predictable because the introduction of *Conn*’s anchor vias to *Gambino* will not affect the packaged module’s electrical functions.” Pet. 64 (citing Ex. 1003 ¶ 142). According to Petitioner, the anchor vias do not need to be connected to active or passive devices, “*Gambino*’s dummy metal pads 16a also do not serve electrical functions,” and “the anchor via’s presence will not change these devices’ functioning.” *Id.* (citing Ex. 1003 ¶ 143).

Petitioner next contends that there would have been a reasonable expectation of success for the combination. Pet. 64. In support of reasonable expectation of success, Petitioner contends that “*Conn* discloses the anchor vias can secure conducting layers with sizes ranging from 10% to 100% of the substrate’s total surface area” and *Gambino*’s “dummy metal pads 16a and main backside metal 16 have sizes in this range, and thus can be securely held by the anchor vias.” *Id.* at 64–65 (citing Ex. 1003 ¶ 144; Ex. 1005 ¶¶ 30–31).

Patent Owner does not dispute Petitioner’s motivation to combine and reasonable expectation of success contentions. PO Resp. 45–55.

We have reviewed Petitioner’s contentions and evidence, which we adopt, and, find that Petitioner establishes that an ordinarily skilled artisan would have been motivated to combine the teachings of *Gambino* and *Conn* and would have had a reasonable expectation of success in doing so. Ex. 1003 ¶¶ 134–145.

b. Claim 1

Petitioner relies on the combination of *Conn*’s anchor vias and *Gambino*’s “dummy metal pad 16a . . . located in at least one corner of the

substrate ‘to provide mechanical support’ as corresponding to limitation 1[a]. Pet. 66–67 (citing Ex. 1003 ¶ 147; Ex. 1005 ¶¶ 19, 27, 28, 30, Fig. 3). For limitation 1[b], Petitioner relies on Conn’s disclosure that “the via conductors in the anchor vias form protruding portions that are connected to a conducting layer.” *Id.* at 67–68 (citing Ex. 1003 ¶¶ 148–149; Ex. 1004, Fig. 1; Ex. 1005 ¶ Fig. 3). For limitation [1.c], Petitioner contends that the combination of Gambino and Conn teaches this limitation “because corner-located dummy metal pad(s) 16a is the claimed ‘backside metal layer’” and “applying Conn’s teachings regarding the anchor vias, a [person of ordinary skill in the art] would understand the protruding portions are ‘bonded to’ corner located dummy metal pad(s) 16a.” *Id.* at 69–70 (citing Ex. 1003 ¶ 150; Ex. 1004, Fig. 2; Ex. 1005, Figs. 3, 5). For limitation [1d], Petitioner contends that the combination of Gambino and Conn teaches this limitation “because corner-located dummy metal pad(s) 16a is only used for mechanical support—not used for electrical connection, which means the anchor vias therein do not provide ground connection to active devices.” Pet. 70 (citing Ex. 1003 ¶ 151; Ex. 1004 ¶¶ 28–30).

Patent Owner offers two arguments for this ground. The first relates to the requirement in limitation 1[b] that the metal filler in the anchor via have “a protruding portion extending from a backside of said semiconductor substrate.” The second relates to the requirement in limitation 1[d] that the “metal filler . . . does not provide ground connection to one or more active devices.” PO Resp. 45–53.

Patent Owner argues the Petition “use[s] Gambino’s via process described at Gambino [0020] to create its proposed anchor vias.” PO Resp. 46 (citing Pet. 64). Patent Owner contends that “Gambino creates its TSVs

by etching holes from the *front side* of the substrate.” *Id.* at 47 (citing Ex. 1005 ¶ 20). Patent Owner further contends that Gambino’s “TSVs extend partially through the unfinished die or substrate,” are “then filled with metal from the front side,” and “the backside is polished (or otherwise removed) to expose the filled via.” *Id.* (citing Ex. 1005 ¶ 20; Ex. 2004 ¶ 121).

Patent Owner contends that creating Conn’s anchor vias using Gambino’s method “would result in one of two outcomes, neither of which meets the claims.” PO Resp. 48. According to Patent Owner, “the anchor vias would be filled entirely, like Gambino’s TSVs, or the anchor vias would not reach the backside metal layer” because “Gambino creates holes in the front side and fills them” and “any anchor vias created using Gambino’s process would be filled from its maximum depth to the surface of the front side.” *Id.* (citing Ex. 1005 ¶ 20; Ex. 2004 ¶¶ 121–124). Patent Owner contends that “[a]dding a filled anchor via to Gambino Figure 5 shows that the anchor via conductor would reach the wiring level and connect it to ground plane 22” resulting in “a ground connection, either directly or indirectly, to an active device.” *Id.* at 48–49 (citing Ex. 1005 ¶ 30; Ex. 2004 ¶¶ 124, 125).

Patent Owner next contends that “Gambino’s process would not result in the filled vias including a ‘protruding portion extending from a backside of said semiconductor substrate.’” PO Resp. 50. Patent Owner argues that because Gambino polishes the backside of the substrate, “the conductors in the via are flush with the surface of the substrate” and “no portion of the conductor would protrude.” *Id.* (citing Ex. 1005 ¶ 20; Ex. 2004 ¶ 128).

Petitioner replies that Gambino’s dummy metal pads are located at the corners and peripheries of the substrate which are less crowded areas not

usually used for planting active/passive devices. Pet. Reply 24 (citing Pet. 56, 64). According to Petitioner, “[t]here would be no reason to place the wiring layers at the corners and peripheries, because the wiring layers are local to active devices” and an ordinarily skilled artisan “would not have placed wiring layers in corner/peripheral areas directly above the dummy metal pads 16a.” *Id.* (citing Ex. 1005, Fig. 5; Ex. 1034 ¶ 22).

Petitioner next argues that even if the wiring layers were located directly above a dummy metal pad, “the ground connection could be avoided by patterning the wiring layer . . . or recess etching the metal filler from the front side to prevent it from electrically contacting the wiring layers.” Pet. Reply 25–26 (citing Ex. 1034 ¶ 23). Further, because Gambino teaches both methods, Petitioner contends that an ordinarily skilled artisan

would have found it desirable to prevent the metal filler from providing ground connection to active devices because neither *Gambino*’s dummy metal pads nor *Conn*’s anchor vias are used for providing electrical connection, and providing the ground connection would unfavorably disturb and require redesign of *Gambino*’s existing active device circuitry.

Id. at 26 (citing Ex. 1034 ¶ 23).

Petitioner next disputes Patent Owner’s assertion that the anchor vias in the proposed combination would “not reach[] the backside metal.” Pet. Reply 26. Petitioner argues that the “proposed combination uses the metal filler in *Conn*’s anchor vias to secure *Gambino*’s proposed backside metal.” *Id.* Referring to *Conn*’s Figure 2 and *Gambino*’s Figure 3, Petitioner argues that both *Conn* and *Gambino* “form[] mechanical connections with the backside metal” and “applying *Gambino*’s process would create anchor vias anchoring the backside metal.” *Id.* at 27 (citing Ex. 1004, Abstract; Ex. 1005 ¶ 30).

Petitioner also disputes Patent Owner’s assertion that Gambino’s backside polishing and grinding would prevent the metal filler of the anchor vias from forming a protruding portion extending from the backside of the substrate. Pet Reply 26. According to Petitioner, the Petition showed that backside grinding can yield protruding portions in connection with the Torii ground and that Dr. Thompson confirms that an ordinarily skilled artisan “would understand *Gambino*’s process could too.” *Id.* (citing Ex. 1003 ¶¶ 54, 145; Ex. 1034 ¶ 24; Ex. 2009 55:6–17).

Patent Owner, in turn, cites to Figure 5 of Gambino and argues that Gambino “shows both devices and wiring layers directly above the dummy metal pads.” Sur-reply 20 (citing Ex. 1005 ¶30, Fig. 5). Patent Owner further argues that “Gambino does not disclose manipulating the wiring layers to avoid contact with an ‘anchor via.’” *Id.*

For the following reasons, we are not persuaded by Patent Owner’s arguments.

We first turn to whether the proposed combination of Gambino and Conn teaches “a metal filler within said a least one anchor via . . . having a protruding portion extending from a backside of said semiconductor substrate” as recited in limitation 1[b].

Patent Owner argues that Gambino polishes the back side of the substrate resulting in a via that is “flush with the surface of the substrate.” PO Resp. 50. Mr. Berg repeats this contention essentially verbatim. Ex. 2004 ¶ 128.

Dr. Thompson disagrees with Mr. Berg and replies that

Gambino discloses using “a thinning process, e.g., a polishing and grinding process” to expose metal filler of the anchor vias at the backside of the substrate. *Gambino*, [0020]. The backside polishing

employs a chemical mechanical planarization (CMP) process to flatten and smooth the backside surface. It was well-known that the CMP process can selectively polish the substrate at a higher rate than the metal filler, thereby resulting in a metal protrusion. Ex. 1035 (“*Yu*”), 4:40–46 (“The second step involved a CMP process which was selective to the material of the insulation layer Although it may be desirable to remove a small amount of the tungsten as well to either to polish the tungsten or to provide a convex protruding plug. If tungsten is removed at this step, it is done at a much slower rate than the removal of the insulation material.”).

Ex. 1034 ¶ 24. Patent Owner does not dispute Dr. Thompson’s testimony that protruding portions can be formed using the process cited in paragraph 20 of Gambino. *See* Sur-reply 22–23. Dr. Thompson’s testimony is supported by the disclosure of Yu and is entitled to weight. Consequently, we are not persuaded by Patent Owner’s argument that the process disclosed in Gambino would not result in the “protruding portions” recited in limitation 1[b].

After considering Petitioner’s arguments and evidence in light of Patent Owner’s arguments and evidence, we find that the combination of Gambino and Conn teaches limitation 1[b].

We now turn to Patent Owner’s ground connection argument.

Figure 3 of Gambino is reproduced below:

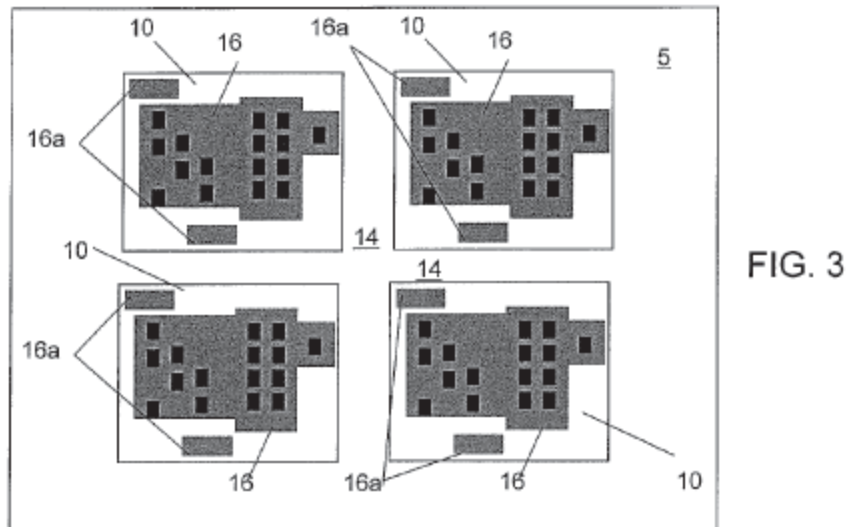


Figure 3 “shows a patterned backside metal with metal pads.” Ex. 1005

¶ 13. Figure 3 shows that “backside metal layer 16 does not entirely cover the dies 10; instead the backside metal layer 16 covers TSVs 12.” *Id.* ¶ 27. Further, metal pads 16a “are provided at strategic locations on the dies 10 to provide mechanical support.” *Id.* ¶ 28. As can be seen from Figure 3, metal pads 16a are not connected to backside metal 16 or TSVs 12.

Dr. Thompson testifies that the combination:

merely requires a simple incorporation of *Conn*’s anchor vias to *Gambino*’s substrate, and does not require any modification to *Gambino*’s overall structure. Particularly, since the anchor vias are only formed at the backside of the substrate, they do not require redistribution of the active devices and wiring layers on the front side of the substrate. Moreover, *Gambino*’s dummy metal pads 16a are located at the corners and peripheries of the substrate, which are less crowded areas that are not usually for planting active/passive devices, so adding the anchor vias here would not affect other elements in the devices.

Ex. 1003 ¶ 141.

Patent Owner provides the following annotated version of Gambino's Figure 5 (PO Resp. 49):

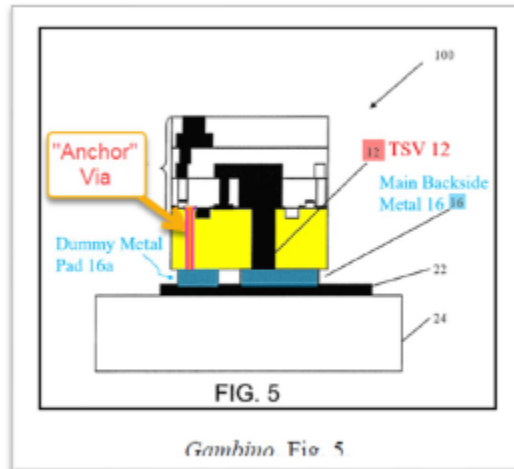


Figure 5 shows a side view of “a packaged module with a backside metal ground plane attached to a substrate.” Ex. 1005 ¶ 13. Patent Owner annotates Figure 5 by highlighting substrate 5 in yellow, ground plane 22 and TSV 12 in black, backside metal 16 blue and dummy metal pad 16a in blue. Sur-reply 20. Patent Owner also adds a red rectangle through substrate 5 between dummy metal pad 16a and the top of the substrate with an annotation “Anchor Via.” *Id.* (citing Ex. 2004 ¶ 124).

Mr. Berg testifies that he added an anchor via to Figure 5 “where [the] Petition suggests.” Ex. 2004 ¶ 124. He further testifies that “the anchor via conductor would reach the wiring level and connect it to the ground plane 22” and this “would result in another of *Gambino*’s grounded TSVs” that “would provide a ground connection, either directly or indirectly, to an active device.” *Id.* ¶¶ 124, 125.

Based on its annotated Figure 5, Patent Owner argues that Gambino’s wiring layers and devices are directly above the dummy metal pads and

“does not disclose manipulating the wiring layers to avoid contact with an ‘anchor via.’” Sur-reply 20.

Dr. Thompson responds that Mr. Berg’s annotated Figure 5 is misleading. Ex. 1034 ¶ 22. Dr. Thompson reiterates the position from his first declaration reproduced above and further explains that “no wiring layers would be placed at the corners and peripheries, because the wiring layers are local to the active devices.” *Id.* (citing Ex. 1005 ¶ 30). We also note that Figure 5 is a side view not a top view and, thus, is not determinative of whether or not active devices or wiring layers are located directly above dummy metal pads 16a.

Mr. Berg does not dispute Dr. Thompson’s testimony that no wiring layers normally would be placed at the corners and peripheries of the substrate. *See* Ex. 2004 ¶¶ 124–125. Dr. Thompson’s testimony appears consistent with the layout of the TSV’s and dummy metal pads in Gambino’s Figure 3 in that there is no connection on the backside of the dummy metal pads 16a to the TSV’s or backside metal layer 16. Ex. 1005, Fig. 3. For these reasons, we find that Dr. Thompson’s testimony that wiring is not normally placed in the corners is reasonable and entitled to weight.

Patent Owner’s argument that Gambino does not disclose manipulating wiring to avoid anchor vias is an attack on Gambino in isolation because Gambino does not disclose anchor vias. Further, the Petition does not propose that when Conn’s anchor vias are applied to Gambino’s metal pads 16a that the anchor vias would extend through to the front side of the substrate but, rather the anchor vias “form[] protruding

portions connected to corner-located dummy metal pad(s) 16a” on the backside. Pet. 68 (citing Ex. 1003 ¶ 149).

Based on the foregoing, we find that the combination of Gambino and Conn teaches limitation 1[d] because it “does not provide a ground connection to one or more active devices in said semiconductor substrate.”

Patent Owner does not dispute any other claim limitations or the motivation to combine Gambino and Conn. Consequently, we find that the combination of Gambino and Conn teaches every limitation of claim 1.

For all the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claim 1 would have been obvious over Gambino and Conn.

3. *Claims 2 and 4–7*

For these dependent claims, Petitioner contends that an ordinarily skilled artisan “would have been motivated to apply *Conn*’s teachings regarding patterns, linear densities, and total areas of anchor vias because they are suitable for achieving *Conn*’s stated purpose of securing backside metal and preventing delamination.” Pet. 73 (citing Ex. 1005 ¶ 157; Ex. 1004 ¶¶ 11, 30, 35, 36).

Petitioner also contends that an ordinarily skilled artisan would have had a reasonable expectation of success. Pet. 73. Petitioner argues that “since *Gambino*’s corner-located dummy metal pad(s) 16a does not provide electrical connection, applying *Conn*’s teachings would have no effect on the electrical functions of the chip,” “both *Gambino* and *Conn* teach using Bosch deep reactive ion etching (DRIE) to form the vias,” and an ordinarily skilled artisan “would have reasonably expected that the same process used for creating *Gambino*’s TSVs can also be used to create the anchor vias,

with the patterns, linear densities, and total areas specified by *Conn*.” *Id.* (citing Ex. 1003 ¶ 158; Ex. 1004 ¶¶ 49, 55; Ex. 1005 ¶ 20). Petitioner further argues that “*Conn*’s anchor vias and *Gambino*’s TSVs share similar parameters” and “sizes of *Conn*’s anchor vias fit for *Gambino*’s packaged module.” *Id.* at 73–74 (citing Ex. 1003 ¶ 158; Ex. 1004 ¶ 35; Ex. 1005 ¶ 20).

Patent Owner does not address Petitioner’s additional motivation to combine and reasonable expectation of success arguments for these claims. *See* PO Resp. 45–54.

To the extent that any additional evidence or arguments are required for motivation to combine and reasonable expectation of success for these claims, we find that Petitioner’s additional reasons are persuasive. Ex. 1003 ¶¶ 157–158.

Claim 2 depends from claim 1 and recites “at least one anchor via comprises a cluster of anchor vias.” Ex. 1001, 8:4–5.

Petitioner contends that *Gambino*’s dummy metal pads modified with *Conn*’s anchor via would render claim 2 obvious. Pet. 70–71 (citing Ex. 1003 ¶ 152; Ex. 1004 ¶¶ 35–36; Ex. 1005, Fig. 5).

Patent Owner does not address claim 2. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of *Gambino* and *Conn* teaches the limitations of claim 2 because *Gambino* discloses dummy metal pads located at the corners of the substrate and *Conn* discloses “distribution patterns and irregular distribution patterns . . . to accommodate chip attachment.” Ex. 1004 ¶ 35. Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 2 would have been obvious over *Gambino* and *Conn*.

Claim 4 depends from claim 1 and recites the “at least one anchor via comprises a plurality of anchor vias disposed in a straight line along a periphery of said semiconductor substrate.” Ex. 1001, 8:10–12.

Petitioner contends that the combination of Gambino and Conn teaches the limitations of claim 4 “because *Gambino*’s corner-located dummy metal pad(s) 16a is located at a **periphery** of the substrate and *Conn* discloses anchor vias therein can have a regular pattern . . . in which each row of the anchor vias is disposed in a straight line along a periphery.” Pet. 71–72 (citing Ex. 1003 ¶ 153; Ex. 1004 ¶¶ 35–36, Fig. 2; Ex. 1005, Fig. 5).

Patent Owner does not address claim 4. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of Gambino and Conn teaches the limitation of claim 4. Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over Gambino and Conn.

Claim 5 depends from claim 4 and recites “wherein a linear density of said plurality of anchor vias is less than approximately 10% of the total linear distance of said straight line along said periphery of said semiconductor substrate.” Ex. 1001, 8:13–16.

Petitioner contends that the combination of Gambino and Conn teaches the limitations of claim 5 “because *Conn* discloses the anchor via pattern at the periphery corner-located dummy metal pad(s) 16a has linear density meeting this requirement.” Pet. 72 (citing Ex. 1003 ¶ 154).

Patent Owner does not address claim 5. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of Gambino and Conn teaches the limitation of claim 5.

Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 5 would have been obvious over Gambino and Conn.

Claim 6 depends from claim 1 and recites “wherein said at least one anchor via comprises a plurality of anchor vias disposed in a staggered configuration along a periphery of said semiconductor substrate.” Ex. 1001, 8:17–20.

Petitioner contends that the combination of Gambino and Conn teaches the limitations of claim 6 “because *Gambino*’s corner-located dummy metal pad(s) 16a is located at a periphery of the substrate and *Conn* renders obvious the anchor vias therein being staggered.” Pet. 72 (citing Ex. 1003 ¶ 154; Ex. 1004 ¶ 35).

Patent Owner does not address claim 6. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of Gambino and Conn teaches the limitation of claim 6. Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 6 would have been obvious over Gambino and Conn.

Claim 7 depends from claim 1 and recites “wherein a total area of said at least one anchor via is less than approximately 0.5% of a total area of said semiconductor substrate.” Ex. 1001, 8:21–23.

Petitioner contends that the combination of Gambino and Conn teaches the limitations of claim 7. Pet. 73 (citing Ex. 1003 ¶ 156).

Patent Owner does not address claim 7. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of Gambino and Conn teaches the limitation of claim 7. Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 7 would have been obvious over Gambino and Conn.

4. *Claim 11*

Petitioner contends that the combination of Gambino and Conn teaches claim limitations “[11a] ‘forming at least one anchor vias,’ [11b] ‘depositing a metal filler,’ and [11c] ‘forming a backside metal layer.’” Pet. 74 (citing Ex. 1003 ¶ 159; Ex. 1005 ¶¶ 20, 21). According to Petitioner, “[a]lthough *Gambino* describes the above method as being used to make electrical TSVs, a [person of ordinary skill in the art] would have been motivated to use it to also manufacture the anchor vias” and “[d]oing so would form the electrical TSVs and anchor vias using the same process, thereby simplifying the manufacturing and minimizing the cost.” *Id.* at 74–75 (citing Ex. 1003 ¶ 160). Petitioner also contends that an ordinarily skilled artisan would have had a reasonable expectation of success. *Id.* at 75. For the remaining limitations of claim 11, Petitioner relies on its contentions for substantially similar limitations of claim 1. *Id.* (citing Ex. 1003 ¶ 101).

Patent Owner does not address claim 11 apart from its contentions for claim 1 discussed above. *See* PO Resp. 45–54.

We have reviewed Petitioner’s contentions and evidence and find that the combination of Gambino and Conn teaches the limitation of claim 11. Therefore, we determine that Petitioner has shown by a preponderance of the evidence that claim 11 would have been obvious over Gambino and Conn.

5. *Claims 12 and 14–17*

For these claims, Petitioner relies on its contentions for claims 11, 2, and 4–7.

For the same reasons discussed above for claims 11, 2, and 4–7, we determine that Petitioner has shown by a preponderance of the evidence that claims 12 and 14–17 would have been obvious over Gambino and Conn.

G. Ground 3B: Alleged Obviousness of Claims 10 and 20 over the combination of Gambino and Conn in view of Ding

Petitioner contends claims 10 and 20 would have been obvious over the combination of Gambino and Conn in view of Ding. Pet. 58. 75–79.

Patent Owner does not provide separate contentions for this ground but relies on its contentions for Ground 3A. PO Resp. 55.

We start with a brief overview of Ding and then address Petitioner’s contentions.

1. Ding (Ex. 1008)

Ding is directed to “integrated circuits, and more particularly, to structures with high-Q value inductors.” Ex. 1008 ¶ 15. Ding discloses depositing “a dielectric film 20 such as, for example, SiO₂ . . . in the openings 16 and 18 and surface of the resist 14.” *Id.* ¶ 21, Figs. 3, 4.

2. Petitioner’s Contentions

For its proposed combination, Petitioner argues that the combination of Gambino and Conn “discloses that its packaged module can be used as ‘RF analog chips,’ and contains ‘a host of different active or passive devices’” and that the inductors disclosed in Ding “are typical passive devices used in RF analog chips.” Pet. 75 (citing Ex. 1003 ¶ 137; Ex. 1005 ¶¶ 2, 30; Ex. 1008 ¶ 15). Petitioner argues that Ding “use[s] [a] TSV-forming process to make inductors in RF chips” which would have prompted an ordinarily skilled artisan “to modify *Gambino/Conn*’s method of forming electrical TSVs and anchor vias, to add a step of forming a dielectric film on

the TSVs/anchor vias, such that the modified method can be used to simultaneously make *Ding*'s high-quality inductor.” *Id.* at 76 (citing Ex. 1003 ¶ 167; Ex. 1004, Fig. 2; Ex. 1005, Fig. 3; Ex. 1008, Fig. 8).

For motivation to combine, Petitioner contends that “both *Gambino* and *Ding* aim to improve RF chip function/manufacturing in an inexpensive way” which, according to Petitioner would have motivated an ordinarily skilled artisan “to combine their teachings to maximize the benefits.” Pet. 77 (citing Ex. 1003 ¶¶ 168; Ex. 1005 ¶¶ 16, 17; Ex. 1008 ¶ 3).

Petitioner further contends that “*Gambino* discloses its packaged module includes ‘passive devices’ and can be ‘RF analog chips’ that use passive devices like inductors . . . [a]nd *Conn* discloses its carrier substrate may be formed with ‘[p]assive components (as capacitors, resistors, and inductors,)” which “suggest[s] its electronic package is suitable for RF applications.” Pet. 77 (citing Ex. 1004 ¶ 26; Ex. 1005 ¶¶ 2, 30). According to Petitioner the combination of *Gambino* and *Conn* “would have prompted a POSA to adopt *Ding*'s teaching about making high-quality inductors.” *Id.* (citing Ex. 1003 ¶ 169).

Petitioner next contends that the combination of *Gambino* and *Conn* “includes electrical TSVs and anchor vias” prompting an ordinarily skilled artisan to utilize “*Ding*'s proposal of using the TSV/anchor-via processing to manufacture the high-quality inductors” and thereby simplify the manufacturing process for RF chips. Pet. 78 (citing Ex. 1003 ¶ 170; Ex. 1008 ¶ 15). Petitioner further contends that “using *Ding*'s dielectric film would reduce signal interference between electrical TSVs . . . and the inductors . . . so making the combination would result in better RF chips.” *Id.* (citing Ex. 1003 ¶ 170).

Petitioner further contends that an ordinarily skilled artisan would have had a reasonable expectation of success. Pet. 78. Petitioner argues that “the proposed combination does not require any change to *Gambino/Conn*’s existing way of forming the TSVs/anchor-vias and back side metal” but “only requires . . . an additional step of depositing the dielectric film, before the metal filler is deposited into the vias.” *Id.* According to Petitioner “[t]his is a simple modification, and a POSA would have had a reasonable expectation of success in it.” *Id.* (citing Ex. 1003 ¶ 171). Further, Petitioner contends that the proposed modification to the via forming method taught by the combination of Gambino and Conn “would yield a predictable result—a dielectric film would be formed on the sidewall of the electrical TSVs and anchor vias” which “would reduce signal interference and yield better-functioning RF chips.” *Id.* at 78–79 (citing Ex. 1003 ¶ 172).

Patent Owner does not address Petitioner’s contentions for motivation to combine and reasonable expectation of success. PO Resp. 55.

We have reviewed Petitioner’s evidence and contentions and find that Petitioner has shown that an ordinarily skilled artisan would have been motivated to combine Ding with Gambino and Conn with a reasonable expectation of success. Ex. 1003 ¶¶ 168–172. This combination would have been the application of the known technique of applying a dielectric film as disclosed in Ding to the combination of Gambino and Conn with the result of “reduc[ing] signal interference between electrical TSVs . . . and the inductors . . . [and] making the combination would result in better RF chips.” Ex. 1003 ¶ 170. *KSR*, 550 U.S. at 417 (“if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is

obvious unless its actual application is beyond his or her skill.”); *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023).

Claim 10 depends from claim 1 and recites “further comprising an insulating layer disposed between said semiconductor substrate and said metal filler in said at least one anchor via.” Ex. 1001, 8:30–32. Claim 20 depends from claim 11 and recites the same limitation as claim 10. *Id.* at 9:10–12.

Petitioner contends that the combination of Gambino, Conn, and Ding teaches the limitation recited in claims 10 and 20 because “*Gambino/Conn*’s via-forming method, as modified by *Ding*, would result in a dielectric film formed in the electrical TSVs and anchor vias.” Pet. 79.

Patent Owner does not address Petitioner’s mapping of the combination of Gambino, Conn, and Ding to claims 10 and 20. PO Resp. 55.

After reviewing Petitioner’s evidence and contentions for claims 10 and 20, we find that the combination of Gambino, Conn, and Ding teaches the limitations of claims 10 and 20.

For the all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that claims 10 and 20 would have been obvious over Gambino, Conn, and Ding.

*H. Ground 4: Alleged Anticipation of
Claims 1, 8–11, and 18–20 by Torii*

Petitioner contends that claims 1, 8–11, and 18–20 are anticipated by Torii. Pet. 79–89. Petitioner supports its contentions with the Declaration of Dr. Thompson. Ex. 1003. Patent Owner argues that Torii does not disclose a metal filler that does not provide a ground connection as required by

limitation 1[d] and does not disclose a backside metal layer on the bottom of a semiconductor substrate as required by limitation 1[c]. PO Resp. 55–59

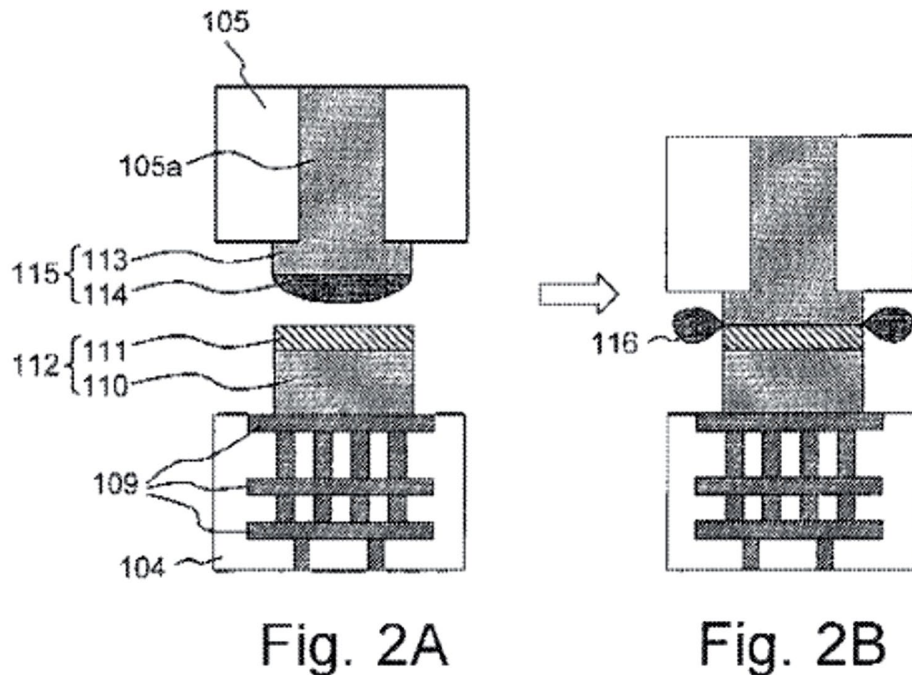
We begin with a brief summary of Torii. We then address the parties’ respective contentions.

1. Torii (Ex. 1009)

Torii is titled “Semiconductor Device.” Ex. 1009, code (54). Torii “relates to a semiconductor device, and more particularly, to a semiconductor device provided with an electrode penetrating through a substrate.” *Id.* ¶ 2.

Torii discloses that a vertical stacking of semiconductor chips may include TSV electrodes penetrating through the substrate of each semiconductor chip and thus providing electrical conduction between respective semiconductor chips. Ex. 1009 ¶ 4.

Figures 2A and 2B are reproduced below:



Figures 2A and 2b illustrate a “method of joining TSVs” of stacked semiconductor chips, “wherein FIG. 2A illustrates a state before joint and FIG. 2B illustrates a state after joint.” Ex. 1009 ¶ 30; *see also id.* ¶¶ 6–7 (describing Figure 1’s illustration of stacked semiconductor chips and Figure 2’s view after joining).

As shown in Figure 2A, a first chip 104 includes a front bump 112 and an interconnect layer 109 of a TSV (element 104a in Figure 1) and between the front bump 112 and TSV. Ex. 1009 ¶ 7. The front bump 112 includes a metal joining layer 111 and a first metal bump 110 between the interconnect layer 109 and metal joining layer 111. *Id.* A second chip 105 includes a rear bump 115. *Id.* The rear bump 115 includes a second metal joining layer 114 and a second metal bump 113 of a TSV 105a and between the second metal joining layer 114 and TSV 105a. *Id.*

As shown in Figure 2A, the front bump 112 of the first chip 104 and rear bump 115 of the second chip 105 are heated to solder-flow the second metal joining layer 114 and thereby join the first metal joining layer 111 and second metal joining layer 114. Ex. 1009, Fig. 2A. The second metal joining layer 114 transforms into a thin film and is consequently susceptible to damage from thermal stresses. *Id.*

The invention provides structure whereby the above “thin-filming of layers, such as a solder layer . . . fluidized by heating[,] is suppressed by providing sub-bumps . . . [that] come into contact with one another . . . [to] secur[e] margins of joint between the main bumps [110, 113].” Ex. 1009 ¶ 8.

Figure 3A is reproduced below:

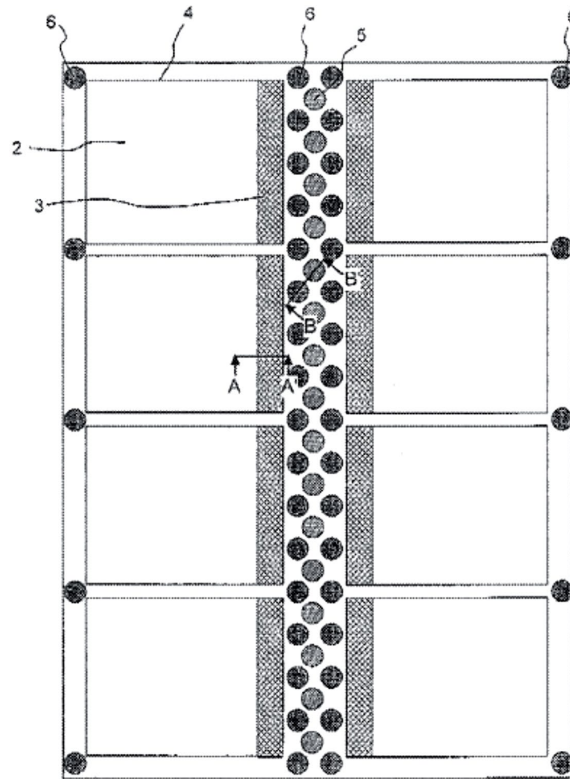


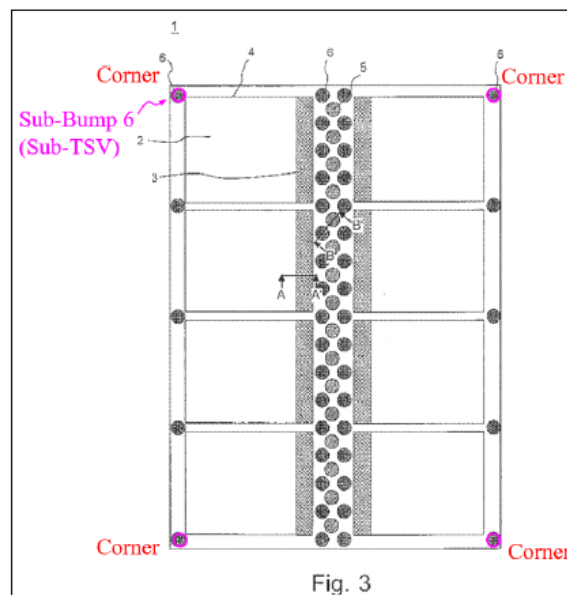
Figure 3A “is a layout plan view illustrating one example of a semiconductor chip according to one exemplary embodiment of the present invention.” Ex. 1009 ¶ 31. A memory mat 4 includes a memory cell region 2 and peripheral circuit region 3. *Id.* ¶ 45. Main bumps 5 of TSVs are disposed between two rows of the memory mats 4. *Id.* Sub-bumps 6 are disposed in proximity to main bumps 5 and along the outer circumference of semiconductor chip 1. *Id.*

A “main TSV” has main bumps and “is used mainly as a current pathway.” Ex. 1009 ¶ 48. A “sub-TSV” is a “dummy which is normally not used as a current pathway[] but can be used as a subsidiary current pathway, [e.g.,] . . . for releasing static electricity.” *Id.*

2. Claim 1

For the preamble, Petitioner relies on Torii's disclosure of a vertical stack of semiconductor chips forming "a semiconductor device 100 (e.g. a memory)." Pet. 79 (citing Ex. 1003 ¶¶ 174–176; Ex. 1009 ¶¶ 2, 4, 6–8, 31, 40, 45, Figs. 1, 3, 46).

For limitation 1[a], Petitioner provides the following annotated version of Torii's Figure 3 (Pet. 81):



Torii, Fig. 3.

Figure 3 "is a layout plan view illustrating one example of a semiconductor chip." Ex. 1009 ¶ 31. Petitioner annotates Figure 3 by adding red circles around element 6 with red text "Corner" and a purple arrow pointing to the upper left corner of the semiconductor chip with purple text "Sub-Bump 6 (Sub-TSV)." Pet. 81.

Petitioner contends that Figure 3 of Torii shows "that '[s]ub-bumps 6 are [] arranged in the outer circumference of semiconductor chip 1,' including corners of the chip." Pet. 80 (citing Ex. 1009 ¶ 45). Petitioner next contends that Torii "discloses 'a sub-bump is formed as part of a sub-

TSV’ and uses these two terms interchangeably” and that “the sub-TSVs are used for joining adjacent semiconductor chips, so they serve as anchor points.” *Id.* (citing Ex. 1003 ¶ 177; Ex. 1009 ¶¶ 45, 48, 83, 90). Petitioner further contends that Torii “discloses that elements of the chip are formed on a semiconductor substrate” and that Torii’s “Figure 46 provides a cross-sectional view of the chip, showing a sub-bump 89 (sub-TSV) is disposed in a substrate 7.” *Id.* at 80–81 (citing Ex. 1009 ¶¶ 43, 94, 100, 101).

For limitation 1[b], Petitioner provides the following annotated version of Torii’s Figure 46 (Pet. 83):

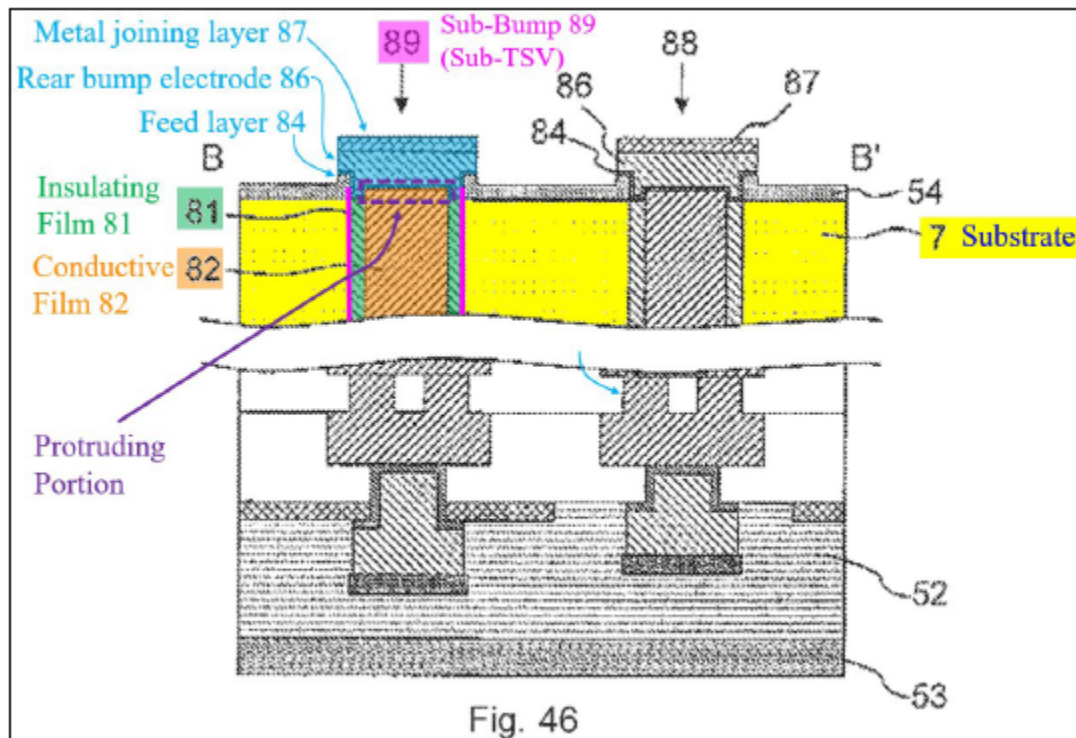


Figure 46 is a cross-sectional view of a semiconductor device. Ex. 1009 ¶ 40. Petitioner annotates Figure 7 by highlighting substrate 7 yellow, insulating film 81 green, conductive film 82 orange, feed layer 84 blue, rear bump electrode 86 blue, metal joining layer 87 blue, and sub-bump 89 purple. Pet. 83.

Petitioner contends that “conductive film 82, e.g., copper is within sub-bump 89 (sub-TSV)” and that “the bottom of conductive film 82 slightly protrudes from the rear surface of the substrate.” Pet. 82 (citing Ex. 1009 ¶¶ 96, 97, 99, 100, Figs. 39, 46).

We have reviewed Petitioner’s contentions and evidence for the preamble and limitations 1[a] and 1[b], which are not disputed by Patent Owner (PO Resp. 55–59), and find that Torii discloses the preamble and limitations 1[a] and 1[b].

We now turn to disputed limitations 1[c] and 1[d].

Petitioner contends that Torii discloses “a ‘[s]econd feed layer 84 is formed on the rear surface’ of the substrate and the protruding portion of conductive film 82.” Pet. 84 (citing Ex. 1009 ¶ 100, Figs. 40–46). Petitioner further contends that “Figure 46 shows feed layer 84 forms a shoulder region on the substrate surface” and the rear surface “is facing up to facilitate a ‘back-side grinding’ process.” *Id.* (citing Ex. 1003 ¶ 180; Ex. 1009 ¶¶ 40, 99, 100). According to Petitioner, Torii’s backside or “rear surface” corresponds to the recited “bottom surface.” *Id.* (citing Ex. 1003 ¶ 180).

Petitioner next contends that Torii’s “second feed layer 84 is made of metal, e.g., copper and/or titanium, and is disposed on the protruding portion by a sputtering or electrolytic plating method resulting in a metallic bonding between second feed layer 84 and conductive film 82.” Pet. 84 (citing Ex. 1003 ¶ 180; Ex. 1009 ¶¶ 37, 81). Petitioner also contends that Torii’s “‘rear bump electrode 86 and second metal joining layer 87 are formed by electrolytic plating’ and are disposed on second feed layer 84.” *Id.* (citing Ex. 1009 ¶ 10, Figs. 45, 46). According to Petitioner, “second feed layer 84

alone, or together with rear bump electrode 86 and second metal joining layer 87, constitutes the claimed backside metal layer.” *Id.* at 84–85 (citing Ex. 1003 ¶ 180).

Patent Owner relying on its construction of “on a bottom surface of the semiconductor substrate,” argues that Torii does not disclose this limitation because it discloses “a rear-surface protective film between the substrate and all portions of the alleged backside metal layer.” PO Resp. 57 (citing Pet. 84 n.12; Ex. 1009 ¶ 100; Ex. 2004 ¶¶ 142–143). As discussed above in connection with Patent Owner’s proposed claim construction, we determine that claim 1 is not limited to direct contact between the backside metal layer and the bottom of the semiconductor substrate. Consequently, Patent Owner’s argument for limitation 1[c] is unavailing.

We have reviewed Petitioner’s contentions and evidence in light of Patent Owner’s argument and find that Petitioner has shown that Torii discloses limitation 1[c].

For limitation 1[d], Petitioner contends that Torii discloses that “[t]he sub-TSV is a dummy . . . normally not used as a current pathway.” Pet. 86 (citing Ex. 1003 ¶ 181; Ex. 1009 ¶ 48).

Patent Owner contends that Petitioner’s quote from Torii “disingenuously removed the second half of the sentence which explicitly states that the sub-TSV can be used to conduct current, including static electricity, which of course is discharged to ground.” PO Resp. 55–56. (citing Ex. 1009 ¶ 48).¹¹ Patent Owner provides the full unedited quote and

¹¹ We preliminarily agreed with Petitioner in our Decision on Institution. Dec. 32.

argues that an ordinarily skilled artisan would “recognize that sub-TSVs provide ground connections.” *Id.* at 56 (citing Ex. 2004 ¶ 138).

Petitioner, in turn, argues that paragraph 48 of Torii “expressly teaches that the distinguishing point between the sub-TSVs and main TSVs is that the sub-TSVs are normally not used as a current pathway.” Pet. Reply 28. Petitioner further argues that “[r]ather than using ‘and can,’ the paragraph uses ‘but can’ to indicate that the subsidiary current pathway is an exceptional case to the ‘normal’ case.” *Id.* Petitioner next argues that “Torii’s ‘Summary’ of the invention and claim 12 also state the main TSVs are ‘to constitute a current pathway’ but do not recite the same for sub TSV’s.” *Id.* (citing Ex. 1009 ¶¶ 15, 16, claim 12). According to Petitioner, when Torii is read as a whole, an ordinarily skilled artisan “would understand that the ‘subsidiary current pathway’ is a possible feature of the sub-TSV, but by no means mandatory, so the sub-TSV is used as a dummy (no electrical connection) *or* a subsidiary pathway.” *Id.* (citing Ex. 1034 ¶ 28).

In the Sur-reply, Patent Owner argues that “Torri discloses multiple embodiments and clearly describes them as such.” Sur-reply 25 (citing Ex. 1009 ¶¶ 50–72, 73–78, 79–81, 82–92, 93–101). Patent Owner further argues that “the relevant subsection on sub-TSVs is not limited to any embodiment.” *Id.* (citing Ex. 1009 ¶ 48). According to Patent Owner, “Petitioner does not point to any Figure or description showing a sub-TSV that does not carry current” and Torii’s “Figures show sub-TSVs wired similarly to main TSVs.” *Id.*

For the following reasons, we are not persuaded by Patent Owner’s arguments.

Paragraph 48 of Torii reads in its entirety:

Note in the present invention, a TSV provided with main bumps is referred to as a main TSV for the reason that the TSV is used mainly as a current pathway, and a TSV provided with sub-bumps is referred to as a sub-TSV. The sub-TSV is a dummy which is normally not used as a current pathway, but can be used as a subsidiary current pathway, such as a current pathway for releasing static electricity.

Ex. 1009 ¶ 48. Torii also discloses that “a sub-bump is formed as part of a sub-TSV, in order to ensure the mechanical strength of the sub-TSV” and that “first and second sub-bumps may be formed on both surfaces of a substrate without being electrically connected to each other.” *Id.* ¶ 90.

Patent Owner cites to the various embodiments disclosed in Torii but does not direct us to any portion of Torii where a sub-TSV is used as a current pathway for releasing static electricity.¹² Sur-reply 25. Torii’s paragraph 90 is part of its “Exemplary Embodiment” 4. *See* Ex. 1009 ¶ 90. Yet the description of the sub-TSVs in this embodiment is that the sub-TSVs ensure mechanical strength and are not “electrically connected.” *Id.* Consequently, at least this embodiment of Torii does not disclose that the sub-TSV’s release static electricity or otherwise provide a ground connection.

For these reasons, we find that Petitioner has shown that Torii discloses limitation [1d].

In summary, for all the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 1 is anticipated by Torii.

¹² Petitioner does not dispute that releasing static electricity would be providing a ground connection. Tr. 54:6–9.

3. *Claim 8*

For claim 8, Petitioner contends that “*Torii*’s second feed layer 84, rear bump electrode 86, and second metal joining layer 87 respectively correspond to the claimed ‘interface layer,’ ‘conduction layer,’ and ‘packaging layer.’” Pet. 86 (citing Ex. 1003 ¶ 182).

Patent Owner does not address claim 8. PO Resp. 55–59.

We have reviewed Petitioner’s evidence and arguments for claim 8 and find that Petitioner shows that *Torii* discloses the limitations of claim 8.

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 8 is anticipated by *Torii*.

4. *Claim 9*

Petitioner contends that the semiconductor device in *Torii*’s “Figure 46 is placed upside down to show a backside-grinding process” while in Figure 36B the semiconductor “is flipped from Figure 46 and shows a front side process to create the TSVs.” Pet. 86 (citing Ex. 1009 ¶¶ 93, 98). According to Petitioner, “in Figure 36B, the semiconductor device is in its normal orientation with the front surface facing up,” “shows conductive film 82 in sub-bump 89 (sub-TSV) is bonded to a third interconnect pad 32a overlying the semiconductor substrate,” and “third interconnect pad 32a is ‘composed of a conductive material such as metal.’” *Id.* (citing Ex. 1003 ¶ 183; Ex. 1009 ¶ 55, Figs. 36B, 46).

Patent Owner does not address claim 9. PO Resp. 55–59.

We have reviewed Petitioner’s evidence and arguments for claim 9 and find that Petitioner shows that *Torii* discloses the limitations of claim 9.

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 9 is anticipated by *Torii*.

5. *Claim 10*

Petitioner contends that Figure 46 of Torii “discloses claim 10 by disclosing an insulating film 81 is formed on the sidewall of the sub-bump 89 (sub-TSV), and between conductive film 82 and the substrate.” Pet. 87 (citing Ex. 1003 ¶ 184; Ex. 1009, 95, 97, 99, 100).

Patent Owner does not address claim 10. PO Resp. 55–59.

We have reviewed Petitioner’s evidence and arguments for claim 10 and find that Petitioner shows that Torii discloses the limitations of claim 10.

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 10 is anticipated by Torii.

6. *Claim 11*

Petitioner contends that Torii “discloses each of the claimed [11a] ‘forming at least one anchor via,’ [11b] ‘depositing a metal filler,’ and [11c] ‘forming a backside metal layer.’” Pet. 88 (citing Ex. 1003 ¶ 185; Ex. 1009, ¶¶ 93, 95, 96, 100). Petitioner further contends that Figures 33B and 34B of Torii “show a front side process to form sub-bump 89 (sub-TSV) and deposit conductive film 82 in sub-bump 89 (sub-TSV)” and “Figure 46 shows a backside-grounding process in which the stack of second feed layer 84, rear bump electrode 86, and second metal joining layer 87 is formed on and bonded to the rear surface of conductive film 82.” *Id.* at 88–89 (citing Ex. 1003 ¶ 185). For the remaining limitations of claim 11, Petitioner relies on its contentions for substantially similar limitations of claim 1 discussed above. *Id.* at 89 (citing Ex. 1003 ¶ 186).

Patent Owner does not address claim 11 apart from its contentions for claim 1. PO Resp. 55–59.

We have reviewed Petitioner’s evidence and arguments for claim 11 and find that Petitioner shows that Torii discloses the limitations of claim 11.

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claim 11 is anticipated by Torii.

7. Claims 18–20

Petitioner relies on its contentions for claims 11 and 8–10. Pet. 89 (citing Ex. 1003 ¶¶ 187–189).

Patent Owner does not address claims 18–20. PO Resp. 55–59.

We have reviewed Petitioner’s evidence and arguments for claims 18–20 and find that Petitioner shows that Torii discloses the limitations of claims 18–20.

For the foregoing reasons, Petitioner has shown by a preponderance of the evidence that claims 18–20 is anticipated by Torii.

*I. Ground 5: Alleged Anticipation of
Claims 1, 2, 3, 9, 11, 12, 13, and 19 by Ide*

Petitioner contends that claims 1, 2, 3, 9, 11, 12, 13, and 19 are anticipated by Ide. Pet. 90–102.

Similar to the argument raised in Ground 4, Patent Owner contends that Ide does not disclose a backside metal layer on the bottom surface of the semiconductor substrate as required by limitation 1[c]. PO Resp. 60–62.

We begin with a brief summary of Ide and the address the parties’ respective contentions.

1. Ide (Ex. 1010)

Ide is titled “Semiconductor Device.” *Id.* at code (54). Ide relates to a “stack-type semiconductor device.” Ex. 1010 ¶¶ 5, 20, 22.

Addressing the background of the invention, Ide describes a chip stacked body including a plurality of memory chips stacked on an interface chip. Ex. 1010 ¶ 6, Fig. 20. Each of the memory chips includes a surface bump electrode on the chip's top surface, a corresponding rear bump pad on the chip's bottom surface, and a through electrode passing through the chip and connecting the bump electrode and bump pad. *Id.* When the memory chips are stacked, each bump electrode of a chip abuts the bump pad of the above chip and the stacked chips are thus electrically connected. *Id.* For assembly of the stack, a surface mark is formed on the top surface of each chip. *Id.* ¶ 15. Ide describes a problem during assembly that once a chip is embedded in the stack, contrast of the surface mark 313 is degraded and throughput is accordingly reduced. *Id.* ¶¶ 20–22.

Figure 1, reproduced below, “is a fragmentary cross sectional elevation view of a schematic configuration of a semiconductor device in accordance with one or more embodiments of the present invention.” Ex. 1010 ¶ 32.

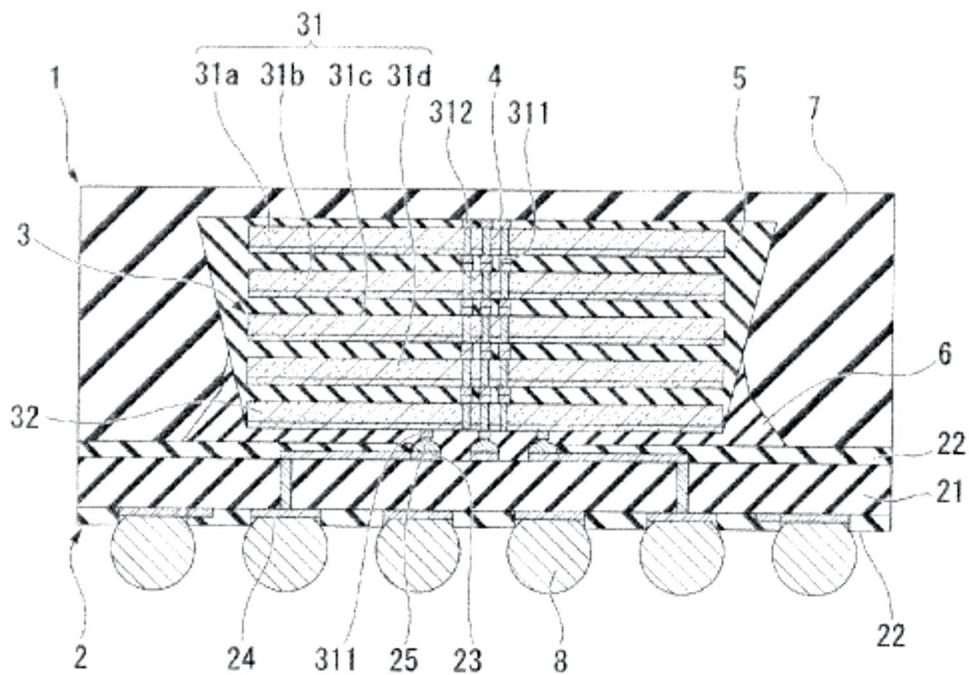
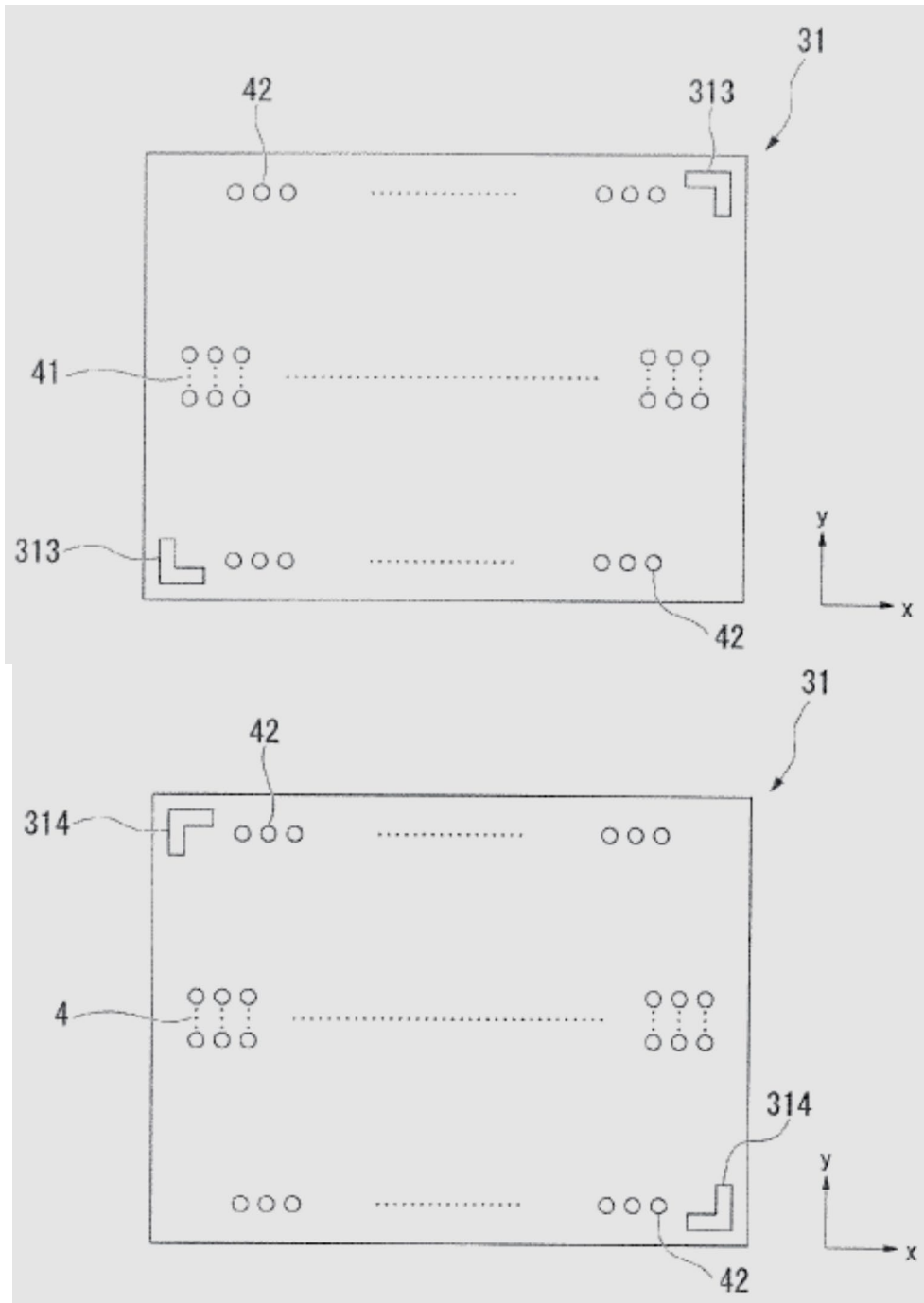


Figure 1 shows elements include a wiring board 2, insulating base 21, insulating layer 22, connection pads 23, lands 24, chip-stacked body 3, memory chips 31a–31d, interface chip 32, surface bump electrodes 311, rear bump electrodes 312, through electrodes 4, encapsulating resin unit 5, wire bump 25, non-conductive paste (NCP) 6, and solder balls 8. *Id.* ¶¶ 106–111.

Figures 2A and 2B, reproduced below (respectively top and bottom) are plan views “of a circuit formation surface of a memory chip of the semiconductor device of FIG. 1” (Fig. 2A) and “an opposite surface to the circuit formation surface of a memory chip of the semiconductor device of FIG. 1” (Fig. 2B). Ex. 1010 ¶¶ 33–34.



Figures 2A and 2B show through electrodes 41, memory chip 31, dummy bump through electrodes 42, surface marks 313, and rear marks 314.

Id. ¶¶ 113–116.

Figure 3B, reproduced below, “is a fragmentary cross-sectional elevation view of the memory chip.” Ex. 1010 ¶ 36.

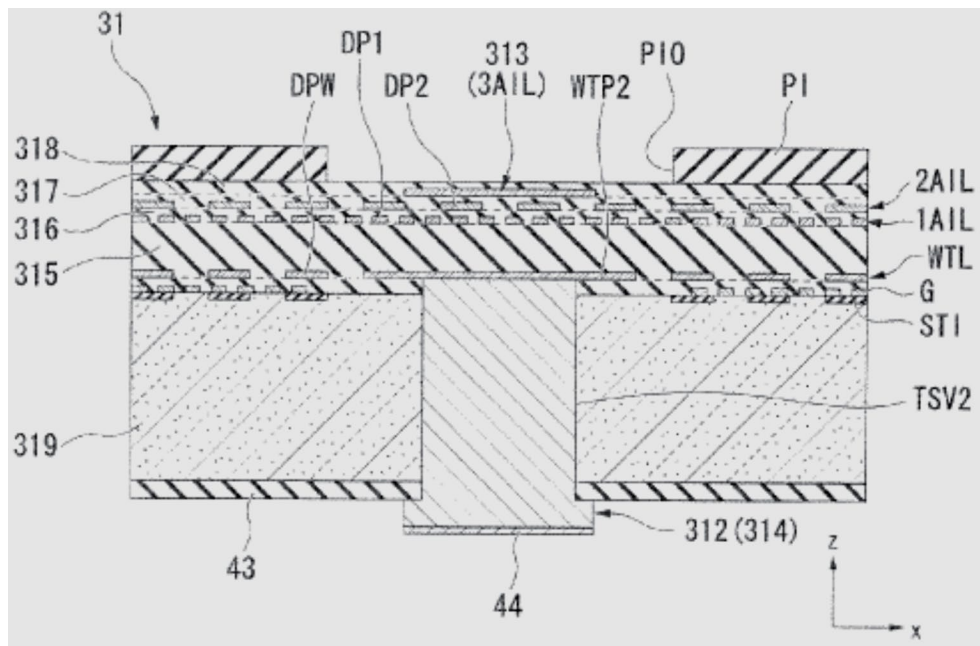


Figure 3B shows a chip that includes, in a surface of the mark portion, a surface mark 313 formed as a third aluminum wiring layer 3AIL located below an opening PIO formed in polyimide film PI. *Id.* ¶ 125. The chip also includes a wiring tungsten pad WTP2 formed as a wiring tungsten layer WTL below the opening PIO and connected to the through electrode TSV2, a rear bump 44, and a through electrode TSV2. *Id.*

2. Claim 1

Patent Owner does not dispute Petitioner’s contentions for the preamble of claim 1 and limitations [1a], [1b], and [1d]. We first summarize Petitioner’s contentions for the preamble and the undisputed limitations and then analyze the parties’ respective contentions for limitation [1c].

For the preamble of claim 1, Petitioner contends that Ide discloses a semiconductor chip. Pet. 90 (citing Ex. 1003 ¶¶ 190–193; Ex. 1010 ¶¶ 33–36, 112–127, Figs. 2A, 2B, 3A, 3B). Petitioner further contends that Ide

discloses that “[m]ultiple of such chips . . . can be vertically stacked to form a memory device.” *Id.* (citing Ex. 1010 ¶¶ 5, 6, 10, Fig. 1). Petitioner further contends that in order to facilitate alignment of the stacked chips, “each chip has surface marks 313 arranged in a pair of corners of its front surface . . . and rear marks 314 arranged in corresponding corners of its rear surface.” *Id.* at 90–91 (citing Ex. 1010 ¶¶ 33, 34, 112–114, Fig. 2A, 2B).

For limitation [1a], Petitioner contends that Ide’s Figure 2B “show[s] ‘rear marks 314 are arranged in a pair of corners which are located diagonally to each other[.]’” and Figure 3B shows “a corresponding cross-sectional view showing each rear mark 314 is formed below a through electrode TSV2, so the TSV2s are also located at the corners of the chip in plain view.” Pet. 91 (citing Ex. 1003 ¶ 194; Ex. 1010 ¶¶ 114, 125). Petitioner further contends that the TSV2s correspond to the recited anchor vias because “[t]he through electrode TSV2 for a mark penetrates the semiconductor substrate 319” and “connects to a rear bump 44 and a wiring tungsten pad WTP2 on the two opposite sides of the substrate, thereby providing an anchor point for affixing and aligning rear bump 44 and wiring tungsten pad WTP2.” *Id.* at 91–92 (citing Ex. 1003 ¶ 194; Ex. 1010 ¶¶ 125, 130, Figs. 2B, 3B).

For limitation [1b], Petitioner contends that Ide’s Figures 12A and 12B show that “during fabrication, ‘a Cu plating 324 is grown using a seed layer 323 as an electrode to fill a via of the through electrode TSV2.’” Pet. 92 (citing Ex. 1003 ¶ 195; Ex. 1010 ¶ 156). Petitioner further contends that Ide’s Figure 3B shows that “in the finished device, Cu plating 324 forms a rear bump electrode 312 (i.e., the claimed ‘protruding portion’) extending

from the rear surface (i.e., backside) of semiconductor substrate 319.” *Id.* at 93 (citing Ex. 1003 ¶ 196; Ex. 1010 ¶¶ 130, 155–157).

For limitation [1d], Petitioner contends that Ide’s “rear marks 314 are arranged within an area in which the plurality of dummy bump through electrodes 42 are arranged” and the “associated TSV2s, are located in a dummy region of the chip and not intended for electrical connections.” Pet. 96 (citing Ex. 1003 ¶ 199; Ex. 1010 ¶ 115). Petitioner further contends that Ide’s “Cu plating 324 in the TSV2 is connected to wiring tungsten pad WTP2 on the front side of the substrate” and the “WTP2 is below ‘a lower dummy pattern’ . . . and ‘an upper dummy pattern’ . . . both of which are not for electrical connections.” *Id.* at 97 (citing Ex. 1003 ¶ 200; Ex. 1010 ¶¶ 125, 126). Petitioner argues that Ide “discloses that ‘**the functional wirings are not** arranged in the first and second aluminum wiring layers 1AIL and 2AIL of an area on wiring tungsten pad WTP2.” *Id.* (citing Ex. 1010 ¶ 127). According to Petitioner, “[t]his means wiring tungsten pad WTP2 cannot function as a path to electrically connect Cu plating 324 in TSV2 to any active devices.” *Id.* at 97–98 (citing Ex. 1003 ¶ 200).

We have reviewed Petitioner’s evidence and arguments for these undisputed limitations and find that Petitioner shows that Ide discloses the preamble of claim 1 and limitations [1a], [1b] and [1d].

Petitioner contends that Ide’s Figure 3B shows that “rear bump 44 is ‘formed in a surface (a rear surface) of the semiconductor substrate’ and ‘below the through electrode TSV2’” and “that at least part of rear bump 44 is on the rear surface.” Pet. 94 (citing Ex. 1003 ¶ 137; Ex. 1010 ¶¶ 120, 125, Figs. 3B, 4C, 13A). Petitioner acknowledges that Ide discloses an intervening insulating layer between rear bump 44 and the bottom surface of

the semiconductor substrate. *Id.*, n.15. Petitioner further contends that “[r]ear bump 44 is made of ‘SnAg’ (tin-silver alloy), i.e., a metal, and formed on Cu plating 324 ‘by plating.’” *Id.* at 94–95 (citing Ex. 1003 ¶ 198; Ex. 1010 ¶ 157, Fig. 13A). According to Petitioner, a person of ordinary skill in the art “would understand that plating the tin-silver alloy on copper will cause them to form a metallic bond” resulting in “rear bump 44 . . . bonded to the protruding portion of Cu plating 324 in TSV2.” *Id.* at 95 (citing Ex. 1003 ¶ 198).

Patent Owner, again relying on its proposed claim construction, argues that “the plain meaning of ‘on the bottom surface’ requires direct contact between the substrate 319 and the rear bump 44 that Petitioner claims is the ‘backside metal layer.’” PO Resp. 61 (citing Ex. 2004 ¶¶ 147–148). Based on this proposed construction, Patent Owner argues that “Ide’s backside metal layer is not ‘on a bottom surface of said semiconductor substrate’ and therefore, *Ide* does not anticipate Claim 1 or 11.” *Id.* at 61–62. Because we do not adopt Patent Owner’s claim construction this argument is unavailing.

We have reviewed Petitioner’s evidence and arguments for limitation [1c] in light of Patent Owner’s argument and find that *Ide* discloses limitation [1c].

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that *Ide* anticipates claim 1.

3. Claim 2

Petitioner contends that *Ide*’s Figure 4C “shows that each ‘rear mark 314 ha[s] an L shape’ including a cluster of two perpendicularly arranged TSV2s.” Pet. 98 (citing Ex. 1003 ¶ 201; Ex. 1010 ¶¶ 59–60, 152–153).

Patent Owner does not address claim 2. PO Resp. 60–62.

We have reviewed Petitioner’s evidence and arguments and find that Ide discloses the limitations of claim 2.

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that Ide anticipates claim 2.

4. Claim 3

Petitioner relies on its contentions for claim 2. Pet. 99 (citing Ex. 1003 ¶ 202).

Patent Owner does not address claim 3. PO Resp. 60–62.

We have reviewed Petitioner’s evidence and arguments and find that Ide discloses the limitations of claim 3

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that Ide anticipates claim 3.

5. Claim 9

Petitioner contends that Ide’s “wiring Tungsten pad WTP2 overlying semiconductor substrate 319 and bonded to Cu plating 324 in the TSV2” discloses the limitations of claim 9. Pet. 99 (citing Ex. 1003 ¶ 203; Ex. 1010 ¶¶ 125, 130, 154–156, Figs. 3B, 12B).

Patent Owner does not address claim 9. PO Resp. 60–62.

We have reviewed Petitioner’s evidence and arguments and find that Ide discloses the limitations of claim 9.

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that Ide anticipates claim 9.

6. Claim 11

Petitioner contends that “*Ide* discloses each of the claimed [11a] ‘forming at least one anchor via,’ [11b] ‘depositing a metal filler,’ and [11c]

“forming a backside metal layer.” Pet. 100 (citing Ex. 1003 ¶ 204; Ex. 1010 ¶¶ 152–159, Figs. 11A–13C). According to Petitioner, Ide uses a dry etching process to form the photoresist PR as a mask to form an opening 331 of the through electrode TSV2, “a Cu plating 324 is grown using a seed layer 323 as an electrode to fill a via of the through electrode TSV2” and “SnAg is formed as rear bump electrode 312 including rear bump 44 by plating.” *Id.* at 100–101 (citing Ex. 1003 ¶ 204; Ex. 1010 ¶¶ 152, 156–157, Figs. 12A, 12B, 13A). For the remaining limitations of claim 11, Petitioner relies on its contentions for substantially similar limitations of claim 1. *Id.* at 101 (citing Ex. 1003 ¶ 205).

Patent Owner does not address claim 11 apart from its contentions for claim 1. PO Resp. 60–62.

We have reviewed Petitioner’s evidence and arguments and find that Ide discloses the limitations of claim 11.

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that Ide anticipates claim 11.

7. Claims 12, 13, 19

For claims 12, 13, and 19, Petitioner relies on its contentions for claims 11, 2, 3, and 9. Pet. 102 (citing Ex. 1003 ¶¶ 206–208).

Patent Owner does not address claims 12, 13, and 19. PO Resp. 60–62.

We have reviewed Petitioner’s evidence and arguments and find that Ide discloses the limitations of claims 12, 13, and 19.

For all the foregoing reasons, we determine that Petitioner shows by a preponderance of the evidence that Ide anticipates claims 12, 13, and 19.

J. Petitioner's Motion to Exclude

Petitioner moves to exclude Exhibits 2007 and 2008. MTE, 1. Petitioner argues that the Exhibits are in violation of FRE 401, 402, 403, and 901. *Id.*

We do not rely on either Exhibit 2007 or 2008 in this Decision. Consequently, we deny Petitioner's MTE as moot.

CONCLUSION¹³

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/ Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19	102	Conn		1, 2, 4, 5, 7, 9, 11, 12, 14, 15, 17, 19
1, 2, 4–7, 9, 11, 12, 14–17, 19	103(a)	Conn		1, 2, 4–7, 9, 11, 12, 14–17, 19
8, 18	103(a)	Conn, AAPA		8, 18
1, 2, 4–7, 11, 12, 14–17	103(a)	Gambino, Conn	1, 2, 4–7, 11, 12, 14–17	
10, 20	103(a)	Gambino, Conn, Ding	10, 20	
1, 8–11, 18–20	102	Torii	1, 8–11, 18– 20	
1–3, 9, 11– 13, 19	102	Ide	1–3, 9, 11–13, 19	
Overall Outcome			1–20	

¹³ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

III. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1–20 of the '826 patent have been shown by a preponderance of the evidence to be unpatentable;

FURTHER ORDERED that Petitioner's Motions to Exclude Evidence, Paper 27, is denied as moot; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2024-01405
Patent 9,245,826 B2

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