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IEEE Std 802.3ae™-2002
(Amendment to IEEE Std 802.3-2002)

IEEE Standards

802.3ae™

IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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IEEE Standard for Information technology—
Telecommunications and information exchange between systems—
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Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation

Sponsor
LAN/MAN Standards Committee
of the
IEEE Computer Society

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Abstract: Support to extend the IEEE 802.3 protocol and MAC specification to an operating speed of 10 Gb/s. Several Physical Coding Sublayers known as 10GBASE-X, 10GBASE-R, and 10GBASE-W are specified, as well as significant additional supporting material for a 10 Gigabit Media Independent Interface (XGMII), a 10 Gigabit Attachment Unit Interface (XAUI), a 10 Gigabit Sixteen-Bit Interface (XSBI) and management.
Keywords: 10 Gigabit Ethernet, fiber, LAN PHY, WAN PHY, XAUI, XGMII, XSBI

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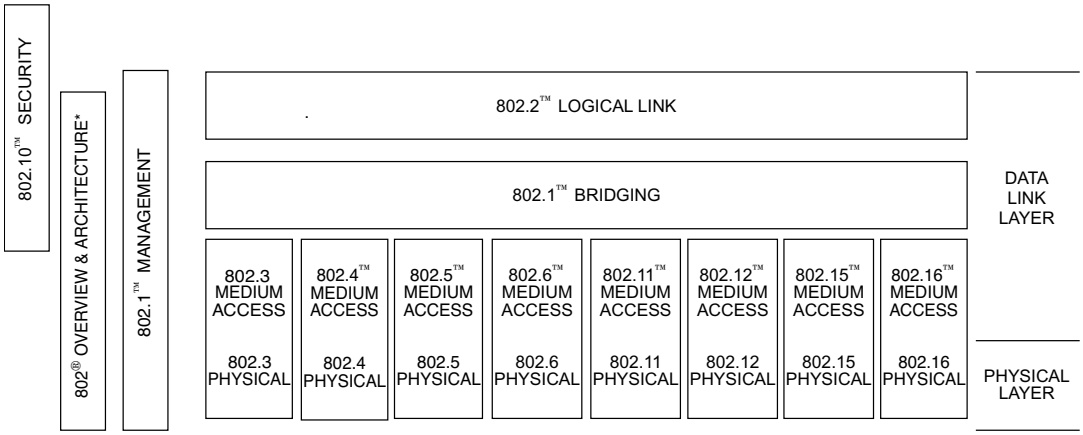
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Introduction to IEEE Std 802.3ae-2002

This standard is part of a family of standards for local and metropolitan area networks. The relationship between the standard and other members of the family is shown below. (The numbers in the figure refer to IEEE standard numbers.[1])



* Formerly IEEE Std 802.1A™

This family of standards deals with the Physical and Data Link layers as defined by the International Organization for Standardization (ISO) Open Systems Interconnection (OSI) Basic Reference Model (ISO/IEC 7498-1: 1994). The access standards define seven types of medium access technologies and associated physical media, each appropriate for particular applications or system objectives. Other types are under investigation.

The standards defining the technologies noted above are as follows:

- IEEE Std 802 — *Overview and Architecture*. This standard provides an overview to the family of IEEE 802 Standards.
- IEEE Std 802.1B™ and 802.1k™ [ISO/IEC 15802-2] — *LAN/MAN Management*. Defines an OSI management-compatible architecture, and services and protocol elements for use in a LAN/MAN environment for performing remote management.
- IEEE Std 802.1D™ — *Media Access Control (MAC) Bridges*. Specifies an architecture and protocol for the interconnection of IEEE 802 LANs below the MAC service boundary.
- IEEE Std 802.1E™ [ISO/IEC 15802-4] — *System Load Protocol*. Specifies a set of services and protocol for those aspects of management concerned with the loading of systems on IEEE 802 LANs.
- IEEE Std 802.1F™ — *Common Definitions and Procedures for IEEE 802 Management Information*.
- IEEE Std 802.1G™ [ISO/IEC 15802-5] — *Remote Media Access Control (MAC) Bridging*. Specifies extensions for the interconnection, using non-LAN communication technologies, of geographically separated IEEE 802 LANs below the level of the logical link control protocol.
- IEEE Std 802.1H™ [ISO/IEC TR 11802-5] — *Media Access Control (MAC) Bridging of Ethernet V2.0 in Local Area Networks*.

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- IEEE Std 802.2 [ISO/IEC 8802-2] — *Logical Link Control*.
- IEEE Std 802.3 — *CSMA/CD Access Method and Physical Layer Specifications*.
- IEEE Std 802.4 [ISO/IEC 8802-4] — *Token Passing Bus Access Method and Physical Layer Specifications*.
- IEEE Std 802.5 [ISO/IEC 8802-5] — *Token Ring Access Method and Physical Layer Specifications*.
- IEEE Std 802.6 [ISO/IEC 8802-6] — *Distributed Queue Dual Bus Access Method and Physical Layer Specifications*.
- IEEE Std 802.10 — *Interoperable LAN/MAN Security.*
- IEEE Std 802.11 [ISO/IEC DIS 8802-11] — *Wireless LAN Medium Access Control (MAC) and Physical Layer Specifications*.
- IEEE Std 802.12 [ISO/IEC 8802-12] — *Demand Priority Access Method, Physical Layer and Repeater Specifications*.
- IEEE Std 802.15 — *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for: Wireless Personal Area Networks*.
- IEEE Std 802.16 — *Standard Air Interface for Fixed Broadband Wireless Access Systems*.

In addition to the family of standards, the following is a recommended practice for a common Physical Layer technology:

- IEEE Std 802.7™ — *IEEE Recommended Practice for Broadband Local Area Networks*.

Conformance test methodology

An additional standard, IEEE Std 1802.3™ provides conformance test information for 10BASE-T.

IEEE Std 802.3ae-2002

This standard contains state-of-the-art material. The area covered by this standard is undergoing evolution. Revisions are anticipated to this standard within the next few years to clarify existing material, to correct possible errors, and to incorporate new related material. Details on the contents of this standard are provided on the following pages.

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IEEE Standard for Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements—

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Changes to IEEE Std 802.3™-2002

[These changes are part of IEEE Std 802.3-2002.]

EDITORIAL NOTE—This amendment is based on the current edition of IEEE Std 802.3-2002. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of IEEE Std 802.3ae-2002.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions. ***Replace*** is used to make large changes in existing text, subclauses, tables, or figures by removing existing material and replacing it with new material. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

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1. Introduction

1.1 Overview

Change 1.1 to read as follows:

This is a comprehensive International Standard for Local and Metropolitan Area Networks (LANs and MANs), employing CSMA/CD as the shared media access method and the IEEE 802.3 (Ethernet) protocol and frame format for data communication. This International Standard is intended to encompass several media types and techniques for a variety of signal rates. ~~from 1Mb/s to 1000Mb/s. This edition of the standard provides the necessary specifications for the following families of systems: a 1Mb/s baseband system, 10Mb/s baseband and broadband systems, a 100Mb/s baseband system, and a 1000Mb/s baseband system.~~ The families of systems supported by this standard are shown in Figure 1–1 and listed in 4.4.2. In addition, it specifies a method for linearly incrementing a system's data rate by aggregating multiple physical links of the same speed into one logical link.

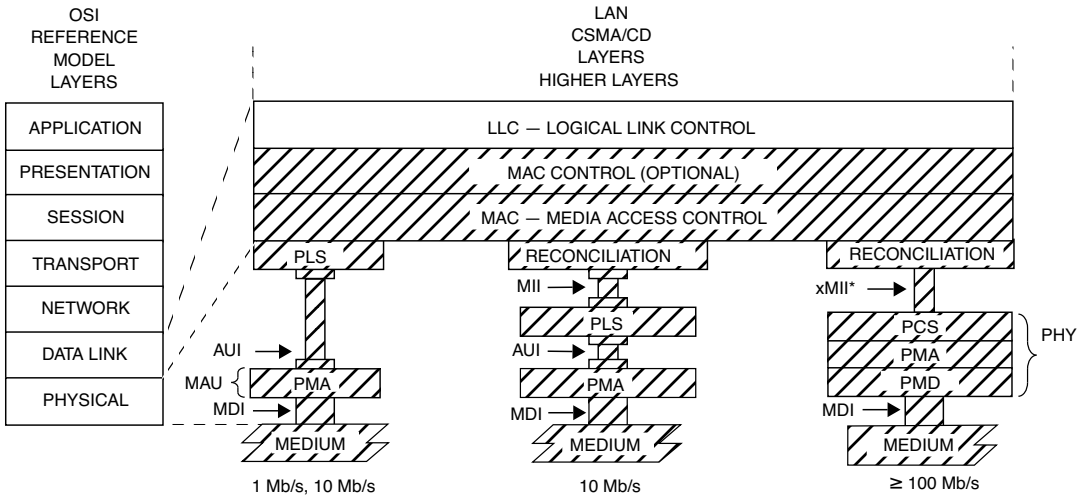
1.1.1.1 Half duplex operation

Change the second paragraph in 1.1.1.1 to read as follows:

Half duplex operation can be used with ~~all~~ certain media types and configurations ~~allowed~~ as defined by this standard. For allowable configurations, see 4.4.2.

1.1.2 Architectural perspectives

Replace Figure 1–1 with the following:



NOTE—In this figure, the xMII is used as a generic term for the Media Independent Interfaces for implementations of 100 Mb/s and above. For example: for 100 Mb/s implementations this interface is called MII; for 1 Gb/s implementations it is called GMII; for 10 Gb/s implementations it is called XGMII; etc.

Figure 1–1—IEEE 802.3 standard relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

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Change the first sentence in 1.1.2 to read as follows:

There are two important ways to view ~~local area~~ network ~~(LAN)~~ design, corresponding to the following:

1.1.2.2 Compatibility interfaces

Change the first sentence in 1.1.2.2 to read as follows:

~~Five~~The following important compatibility interfaces are defined within what is architecturally the Physical Layer.

Change item d) in 1.1.2.2 to read as follows:

d) *Gigabit Media Independent Interface (GMII)*. The GMII is designed to connect a 1 Gb/s capable ~~gigabit-capable~~ MAC or repeater unit to a 1 Gb/s ~~gigabit~~ PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 1 Gb/s ~~gigabit~~ speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.

Insert the following lettered items at the end of subclause 1.1.2.2:

f) *10 Gigabit Media Independent Interface (XGMII)*. The XGMII is designed to connect a 10 Gb/s capable MAC to a 10 Gb/s PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 10 Gb/s speeds. The XGMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XGMII. The XGMII is optional.

g) *10 Gigabit Attachment Unit Interface (XAUI)*. The XAUI is designed to extend the connection between a 10 Gb/s capable MAC and a 10 Gb/s PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 10 Gb/s speeds. The XAUI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XAUI. The XAUI is optional.

h) *10 Gigabit Sixteen-Bit Interface (XSBI)*. The XSBI is provided as a physical instantiation of the PMA service interface for 10GBASE-R and 10GBASE-W PHYs. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it provides a convenient partition between the high-frequency circuitry associated with the PMA sublayer and the logic functions associated with the PCS and MAC sublayers. The XSBI is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XSBI. The XSBI is optional.

1.1.4 Application areas

Change 1.1.4 to read as follows:

~~The applications environment for the LAN is intended to be commercial and light industrial. Use of CSMA/CD LANs in home or heavy industrial environments, while not precluded, is not considered within the scope of this standard.~~

Use of this standard is not restricted to any specific environments or applications.

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In the context of this standard, the term "LAN" is used to indicate all networks that utilize the 802.3 (Ethernet) protocol for communication. These may include (but are not limited to) LANs and MANs.

1.2.1 State diagram conventions

Change the fifth paragraph in 1.2.1 to read as follows:

Some devices described in this standard (e.g., repeaters) are allowed to have two or more ports. State diagrams that are capable of describing the operation of devices with an unspecified number of ports~~,~~ require a qualifier notation that allows testing for conditions at multiple ports. The notation used is a term that includes a description in parentheses of which ports must meet the term for the qualifier to be satisfied (e.g., ANY and ALL). It is also necessary to provide for term-assignment statements that assign a name to a port that satisfies a qualifier. The following convention is used to describe a term-assignment statement that is associated with a transition:

Add the following subclause after 1.2.4:

1.2.5 Hexadecimal notation

Numerical values designated by the 0x prefix indicate a hexadecimal interpretation of the corresponding number. For example: 0x0F represents an 8-bit hexadecimal value of the decimal number 15; 0x00000000 represents a 32-bit hexadecimal value of the decimal number 0; etc.

1.3 Normative references

Insert the following references in alphabetic order into the reference list in 1.3:

ANSI T1.105-1995, Telecommunications—Synchronous Optical Network (SONET)—Basic Description including Multiplex Structure, Rates and Formats.

ANSI T1.269-2000, Information Interchange—Structure and Representation of Trace Message formats for the North American Telecommunications System.

ANSI T1.416-1999, Telecommunications—Network to Customer Installation Interfaces—Synchronous Optical Network (SONET) Physical Layer Specification: Common Criteria.

ANSI X3.230-1994 (FC-PH), Information Technology—Fibre Channel—Physical and Signaling Interface.

ANSI/TIA/EIA-455-175A-92; Chromatic Dispersion Measurement of Single-Mode Optical Fibers by the Differential Phase-Shift Method.

ANSI/TIA/EIA-455-203-2001; Launched Power Distribution Measurement Procedure for Graded-Index Multimode Transmitters.

ANSI/TIA/EIA-455-204-2000; Measurement of Bandwidth on Multimode Fiber.

ANSI/TIA/EIA-526-4A-1997 (OFSTP-4A), Optical Eye Pattern Measurement Procedure.

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ANSI/TIA/EIA-568-B.3-2000; Optical Fiber Cabling Components Standard.

EIA/JEDEC Standard EIA/JESD8-6, High Speed Transceiver Logic (HSTL), August 1995.[1]

IEC 60793-1-41: 2001, Optical fibres—Part 1-41: Measurement methods and test procedures—Bandwidth.

IEC 60825-1: 2001, Edition 1.2, Consolidated Edition; Safety of Laser Products—Part 1: Equipment classification, requirements and user's guide.

IEC 61753-1-1: 2000, Fibre optic interconnecting devices and passive components performance standard - Part 1-1: General and guidance—Interconnecting devices (connectors).

IEC 61753-021-2 (2002-07), Fibre optic passive component performance standard—Part 021-2: Fibre optic connectors terminated on single-mode fibre to category C Controlled environment.

IEC 61753-022-2, Performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for Category C—Controlled environment.[2]

INCITS-TR-25:1999—Fibre Channel Methodologies for Jitter Specification.[3]

ITU-T Recommendation G.652, 2000—Characteristics of a single-mode optical fibre cable.

ITU-T Recommendation G.691, 2000—Optical interfaces for single-channel STM-64, STM-256 and other SDH systems with optical amplifiers.

ITU-T Recommendation G.957, 1999—Optical interfaces for equipments and systems relating to the synchronous digital hierarchy (SDH).

ITU-T Recommendation O.150, 1996—General requirements for instrumentation for performance measurements on digital transmission equipment.

ITU-T Recommendation O.172, 1999—Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH).

TIA-492AAAC-2002; Detail Specification for 850-nm Laser-Optimized, 50-um core diameter/125-um cladding diameter class Ia graded-index multimode optical fibers.

1.4 Definitions

Delete definition 1.4.250. Renumber the definitions that follow.

1.4.250 ~~side stream scrambling~~: ~~A data scrambling technique, used by 100BASE-T2 to randomize the sequence of transmitted symbols and avoid the presence of spectral lines in the signal spectrum. Synchronization of the scrambler and descrambler of connected PHYs is required prior to operation.~~

[1]EIA publications are available from Global Engineering Documents, 15 Inverness Way East, Englewood, Colorado 80112, USA (http://global.ihs.com/). JEDEC publications are available from JEDEC, 2001 I Street NW, Washington, DC 20006, USA.

[2]IEC 61753-022-2 is under development and not available at this time. Its anticipated publication date is April 2003. Until the IEC standard is available, users are encouraged to reference ANSI/TIA/EIA-568-B.3-2000 in its place.

[3]INCITS publications are available from http://www.incits.org.

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Change definition 1.4.89 to read as follows:

1.4.89 compatibility interfaces: ~~The Medium Dependent Interface (MDI) cable, the Attachment Unit Interface (AUI) branch cable, and the Media Independent Interface (MII); the three points at which hardware compatibility is defined to allow connection of independently designed and manufactured components to a baseband transmission medium. (See IEEE 802.3 Clause 8.)~~ Several hardware points of attachment have been defined by this standard to allow connection of independently designed and manufactured components to the transmission medium. See 1.1.2.2.

Insert the following definitions at the end of 1.4. These definitions will be renumbered in alphabetic order in a future edition of this standard, placed in the proper sequence with other definitions.

1.4.xxx 10 Gigabit Attachment Unit Interface (XAUI): The interface between two 10 Gigabit Extender Sublayers (XGXS) to extend the reach of the XGMII for 10 Gb/s operation. (See IEEE 802.3 Clause 47.)

1.4.xxx 10 Gigabit Media Independent Interface (XGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 10 Gb/s operation. (See IEEE 802.3 Clause 46.)

1.4.xxx 10 Gigabit Sixteen-Bit Interface (XSBI): The interface between the Physical Coding Sublayer (PCS) in 10GBASE-R or the WAN Interface Sublayer (WIS) in 10GBASE-W and the Physical Medium Attachment (PMA) sublayer for 10 Gb/s operation. (See IEEE 802.3 Clause 51.)

1.4.xxx anomaly: A discrepancy between the actual and desired characteristics of an item. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx bit interleaved parity N (BIP-N): A method of error monitoring using even (or odd) parity, such that an N-bit codeword is generated over a specified portion of an input data stream in such a manner that the i-th bit of the codeword provides even (or odd) parity over the i-th bit of all N-bit sequences in the covered portion of the data stream. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx container: An SDH term that is equivalent to the payload capacity of a synchronous payload envelope. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx defect: A limited interruption in the ability of an item to perform a required function. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx fixed stuff: Null or padding octets inserted to compensate for the bandwidth differences between the byte interleaving and the concatenation rules of SONET/SDH. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx jitter: The deviation from the ideal timing of an event at the mean amplitude of the signal population. Low-frequency deviations are tracked by the clock recovery circuit, and do not directly affect the timing allocations within a bit cell. Jitter that is not tracked by the clock recovery circuit directly affects the timing allocations in a bit cell. Total Jitter (TJ) is composed of Deterministic Jitter (DJ) and Random Jitter (RJ). Deterministic Jitter is characterized by its bounded peak-to-peak value and a non-Gaussian probability density function. Four kinds of Deterministic Jitter are identified by their specific causes: duty cycle distortion, data dependent, sinusoidal, and uncorrelated (to the data). Random Jitter is characterized by a Gaussian distribution. For example, Random Jitter is the peak-to-peak value at approximately 14 times the standard deviation of the Gaussian distribution for a BER of 10E-12, if the jitter population consists of only Gaussian components.

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1.4.xxx lane: A bundle of signals that constitutes a logical subset of a point-to-point interconnect. A lane contains enough signals to communicate a quantum of data and/or control information between the two end-points.

1.4.xxx Optical Modulation Amplitude (OMA): The absolute difference between the optical power of a logic one level and the optical power of a logic zero level.

1.4.xxx pointer: See Payload pointer.

1.4.xxx payload pointer: An indicator of the location of the beginning of the synchronous payload envelope. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx RIN_xOMA: Relative Intensity Noise. Laser noise in dB/Hz with XdB optical return loss, with respect to the optical modulation amplitude.

1.4.xxx rising edge: A rising edge for a differential signal pair, e.g. signal(P,N) is when, signal(P) transitions from logic low to high and signal(N) transitions from logic high to low.

1.4.xxx scrambler: A randomizing mechanism that is used to eliminate long strings of consecutive identical transmitted symbols and avoid the presence of spectral lines in the signal spectrum without changing the data rate. A self-synchronous scrambler is one in which the current state of the scrambler is the prior n bits of the scrambled output. Therefore, the descrambler can acquire the correct state directly from the received stream. A side-stream scrambler is one in which the current state of the scrambler is dependent only on the prior state of the scrambler and not on the transmitted data. Therefore, the descrambler must acquire state either by searching for a state that decodes a known pattern or by agreement to start at a known state in synchronization with the scrambler. A frame-synchronous scrambler is a side-stream scrambler that begins each frame in a known state. This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx Synchronous Payload Envelope (SPE): A 125-microsecond frame structure composed of STS Path Overhead and bandwidth for payload (payload capacity). The equivalent SDH term is Virtual Container (VC). This definition is derived from ANSI T1.416-1999 and ANSI T1.105-1995, which take precedence.

1.4.xxx WAN Interface Sublayer (WIS): Within 10GBASE-W, a sublayer used to couple the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer. The WIS contains functions to perform SONET STS-192c/SDH VC-4-64c framing and scrambling. (See IEEE 802.3 Clause 50.)

1.5 Abbreviations

Insert the following abbreviations in alphabetic order into the abbreviations list in 1.5:

AIS	Alarm Indication Signal
BERT	Bit Error Ratio Tester
BIP	Bit Interleaved Parity
CDR	Clock And Data Recovery Circuit
CID	Consecutive Identical Digit
CJPAT	Continuous Jitter Test Pattern
CRPAT	Continuous Random Test Pattern
DCD	Duty Cycle Distortion
DDJ	Data Dependent Jitter
DJ	Deterministic Jitter
ERDI	Enhanced Remote Defect Indication
LCD	Loss Of Code-Group Delineation

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LOF	Loss Of Framing
LOP	Loss Of Pointer
LOS	Loss Of Signal
LVDS	Low-Voltage Differential Signals
MAN	Metropolitan Area Network
MMD	MDIO Manageable Device
OIF	Optical Internetworking Forum
OMA	Optical Modulation Amplitude
PCB	Printed Circuit Board
PIPO	Parallel In Parallel Out
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PLM	Path Label Mismatch
PRBS	Pseudo Random Bit Sequence
REI	Remote Error Indication
RJ	Random Jitter
SDH	Synchronous Digital Hierarchy
SEF	Severely Errored Frame
SERDES	Serializer And Deserializer Circuit
SES	Severely Errored Second
SIPO	Serial In Parallel Out
SMSR	Side Mode Suppression Ratio
SNR	Signal To Noise Ratio
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope
STS	Synchronous Transport Signal
TSS	Test Signal Structure
UI	Unit Interval
VC	Virtual Container
WAN	Wide Area Network
WIS	WAN Interface Sublayer
WWDM	Wide Wavelength Division Multiplexing
XAUI	10 Gigabit Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extender Sublayer
XS	Extender Sublayer
XSBI	10 Gigabit Sixteen-Bit Interface

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2. Media Access Control (MAC) service specification

2.1 Scope and field of application

Change 2.1 to read as follows:

This clause specifies the services provided by the Media Access Control (MAC) sublayer and the optional MAC Control sublayer to the client of the MAC ~~(MAC client)~~ (~~see Figure 2–1~~see Figure 1–1). MAC clients may include the Logical Link Control (LLC) sublayer, Bridge Relay Entity, or other users of ISO/IEC LAN International Standard MAC services (see Figure ~~2–2~~2–1). The services are described in an abstract way and do not imply any particular implementation~~,~~ or any exposed interface. There is not necessarily a one-to-one correspondence between the primitives and the formal procedures and interfaces described in Clause 4 and Clause 31.

Delete Figure 2–1.

Renumber the remaining figures (i.e., "Figure 2–2" becomes "Figure 2–1").

2.3.1.2 Semantics of the service primitive

Change 2.3.1.2 to read as follows:

The semantics of the primitive are as follows:

```
MA_DATA.request     (
                    destination_address,
                    source_address,
                    ~~m_sdu,~~
                    mac_service_data_unit,
                    frame_check_sequence
                    ~~service_class~~
                    )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It must contain sufficient information to create the DA field that is prepended to the frame by the local MAC sublayer entity and any physical information. The source_address parameter, if present, must specify an individual MAC address. If the source_address parameter is omitted, the local MAC sublayer entity will insert a value associated with that entity. The ~~m_sdu~~ mac_service_data_unit parameter specifies the MAC service data unit to be transmitted by the MAC sublayer entity. There is sufficient information associated with ~~m_sdu~~ the mac_service_data_unit for the MAC sublayer entity to determine the length of the data unit. The frame_check_sequence parameter, if present, must specify the frame check sequence field for the frame (see 3.2.8). If the frame_check_sequence parameter is omitted, the local MAC sublayer entity will compute this field and append it to the end of the frame. ~~The service_class parameter indicates a quality of service requested by the MAC client (see 2.3.1.5).~~

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2.3.1.5 Additional comments

Change 2.3.1.5 to read as follows:

If this primitive contains the frame_check_sequence parameter, the MAC client entity must take into account this parameter's special bit-transmission order requirements, as specified in 3.3.

The mapping between the MA_UNITDATA.request primitive specified in ISO/IEC 15802-1 (for end stations) and the MA_DATA.request primitive specified here is as follows:

a) The user_priority parameter specified for MA_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
b) The access_priority parameter specified for MA_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
c) The frame_check_sequence parameter is not present for MA_UNITDATA.request.

The mapping between the M_UNITDATA.request primitive specified in ISO/IEC 15802-3 (for MAC Bridges) and the MA_DATA.request primitive specified here is as follows:

a) The frame_type parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
b) The mac_action parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
c) The user_priority parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.
d) The access_priority parameter specified for M_UNITDATA.request is not relevant for IEEE 802.3 operation and is ignored by MA_DATA.request.

~~The CSMA/CD MAC protocol provides a single quality of service regardless of the service_class requested.~~

2.3.2.2 Semantics of the service primitive

Change 2.3.2.2 to read as follows:

The semantics of the primitive are as follows:

```
MA_DATA.indication      (
                        destination_address,
                        source_address,
                        ~~m_sdu,~~
                        mac_service_data_unit,
                        frame_check_sequence,
                        reception_status
                        )
```

The destination_address parameter may be either an individual or a group address as specified by the DA field of the incoming frame. The source_address parameter is an individual address as specified by the SA field of the incoming frame. The ~~m_sdu~~ mac_service_data_unit parameter specifies the MAC service data unit as received by the local MAC entity. The frame_check_sequence parameter is the cyclic redundancy check value (see 3.2.8) as specified by the FCS field of the incoming frame. This parameter may be either omitted or (optionally) passed by the MAC sublayer entity to the MAC client. The reception_status parameter is used to pass status information to the MAC client entity.

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2.3.2.5 Additional comments

Change 2.3.2.5 to read as follows:

If the local MAC sublayer entity is designated by the destination_address parameter of an MA_DATA.request, the indication primitive will also be invoked by the MAC entity to the MAC client entity. This characteristic of the MAC sublayer may be due to unique functionality within the MAC sublayer or characteristics of the lower layers (for example, all frames transmitted to the broadcast address will invoke MA_DATA.indication at all stations in the network including the station that generated the request).

If this primitive contains the frame_check_sequence parameter, the MAC client entity must take into account this parameter's special bit-transmission order requirements, as specified in 3.3.

The mapping between the MA_DATA.indication primitive specified here and the MA_UNITDATA.indication primitive specified in ISO/IEC 15802-1 (for end stations) is as follows:

a) The user_priority parameter specified for MA_UNITDATA.indication is not relevant for IEEE 802.3 operation.
b) The frame_check_sequence parameter is not present for MA_UNITDATA.indication.
c) The reception_status parameter is not mapped to any parameter and is ignored by MA_UNITDATA.indication.

The mapping between the MA_DATA.indication primitive and the M_UNITDATA.indication primitive specified in ISO/IEC 15802-3 (for MAC Bridges) is as follows:

a) The frame_type parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation and is always assigned the value of user_data_frame.
b) The mac_action parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation and is always assigned the value of request_with_no_response.
c) The user_priority parameter specified for M_UNITDATA.indication is not relevant for IEEE 802.3 operation.
d) The reception_status parameter is not mapped to any parameter and is ignored by M_UNITDATA.indication.

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4. Media Access Control

4.1.2 CSMA/CD operation

Change the first paragraph in 4.1.2 to read as follows:

This subclause provides an overview of frame transmission and reception in terms of the functional model of the architecture. This overview is descriptive~~,~~ rather than definitional; the formal specifications of the operations described here are given in 4.2 and 4.3. Specific implementations for CSMA/CD mechanisms that meet this standard are given in 4.4. ~~Figure 4–1~~Figure 1–1 provides the architectural model described functionally in the subclauses that follow.

Delete Figure 4–1.

Renumber the remaining figures (i.e., "Figure 4–2" becomes "Figure 4–1").

4.1.2.1.1 Transmission without contention

Change 4.1.2.1.1 to read as follows:

When a MAC client requests the transmission of a frame, the Transmit Data Encapsulation component of the CSMA/CD MAC sublayer constructs the frame from the client-supplied data. It prepends a preamble and a Start Frame Delimiter to the beginning of the frame. Using information provided by the client, the CSMA/CD MAC sublayer also appends a PAD at the end of the MAC information field of sufficient length to ensure that the transmitted frame length satisfies a minimum frame-size requirement (see 4.2.3.3). It also prepends destination and source addresses, the length/type field, and appends a frame check sequence to provide for error detection. If the MAC supports the use of client-supplied frame check sequence values, then it shall use the client-supplied value, when present. If the use of client-supplied frame check sequence values is not supported, or if the client-supplied frame check sequence value is not present, then the MAC shall compute this value. The frame is then handed to the Transmit Media Access Management component in the MAC sublayer for transmission.

In half duplex mode, Transmit Media Access Management attempts to avoid contention with other traffic on the medium by monitoring the carrier sense signal provided by the Physical Layer Signaling (PLS) component and deferring to passing traffic. When the medium is clear, frame transmission is initiated (after a brief interframe delay to provide recovery time for other CSMA/CD MAC sublayers and for the physical medium). The MAC sublayer then provides a serial stream of bits to the Physical Layer for transmission.

In half duplex mode~~, at operating speeds above 100 Mb/s~~ at an operating speed of 1000 Mb/s, the minimum frame size is insufficient to ensure the proper operation of the CSMA/CD protocol for the desired network topologies. To circumvent this problem, the MAC sublayer will append a sequence of extension bits to frames which are less than slotTime bits in length so that the duration of the resulting transmission is sufficient to ensure proper operation of the CSMA/CD protocol.

In half duplex mode~~, at operating speeds above 100 Mb/s~~ at an operating speed of 1000 Mb/s, the CSMA/CD MAC may optionally transmit additional frames without relinquishing control of the transmission medium, up to a specified limit.

In full duplex mode, there is no need for Transmit Media Access Management to avoid contention with other traffic on the medium. Frame transmission may be initiated after the interframe delay, regardless of the presence of receive activity. In full duplex mode, the MAC sublayer does not perform either carrier extension or frame bursting.

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The Physical Layer performs the task of generating the signals on the medium that represent the bits of the frame. Simultaneously, it monitors the medium and generates the collision detect signal, which in the contention-free case under discussion, remains off for the duration of the frame. A functional description of the Physical Layer is given in Clause 7 and beyond.

When transmission has completed without contention, the CSMA/CD MAC sublayer so informs the MAC client and awaits the next request for frame transmission.

4.1.2.1.2 Reception without contention

Change 4.1.2.1.2 to read as follows:

At each receiving station, the arrival of a frame is first detected by the Physical Layer, which responds by synchronizing with the incoming preamble, and by turning on the receiveDataValid signal. As the encoded bits arrive from the medium, they are decoded and translated back into binary data. The Physical Layer passes subsequent bits up to the MAC sublayer, where the leading bits are discarded, up to and including the end of the preamble and Start Frame Delimiter.

Meanwhile, the Receive Media Access Management component of the MAC sublayer, having observed receiveDataValid, has been waiting for the incoming bits to be delivered. Receive Media Access Management collects bits from the Physical Layer entity as long as the receiveDataValid signal remains on. When the receiveDataValid signal is removed, the frame is truncated to an octet boundary, if necessary, and passed to Receive Data Decapsulation for processing.

Receive Data Decapsulation checks the frame's Destination Address field to decide whether the frame should be received by this station. If so, it passes the Destination Address (DA), the Source Address (SA), the Length/Type ~~Type/Length field~~, ~~and~~ the ~~d~~Data and (optionally) the Frame Check Sequence (FCS) fields to the MAC client, along with an appropriate status code, as defined in 4.3.2. ~~indicating reception_complete or reception_too_long.~~ It also checks for invalid MAC frames by inspecting the frame check sequence to detect any damage to the frame enroute, and by checking for proper octet-boundary alignment of the end of the frame. Frames with a valid FCS may also be checked for proper octet-boundary alignment.

In half duplex mode, ~~at operating speeds above 100 Mb/s~~ at an operating speed of 1000 Mb/s, frames may be extended by the transmitting station under the conditions described in 4.2.3.4. The extension is discarded by the MAC sublayer of the receiving station, as defined in the procedural model in 4.2.9.

4.1.4 CSMA/CD access method functional capabilities

Change the first sentence in the first paragraph in 4.1.1 to read as follows:

The following summary of the functional capabilities of the CSMA/CD MAC sublayer is intended as a quick reference guide to the capabilities of the standard, as shown in ~~Figure 4–2~~ Figure 4–1:

Change the following list items at the end of 4.1.4:

m) Appends extension bits to the first (or only) frame of a burst if it is less than slotTime bits in length when in half duplex mode ~~at speeds above 100 Mb/s~~ at an operating speed of 1000 Mb/s.
n) Strips extension bits from received frames when in half duplex mode ~~at speeds above 100 Mb/s~~ at an operating speed of 1000 Mb/s.

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4.2.2.3 Organization of the procedural model

Change 4.2.2.3 to read as follows:

The procedural model used here is based on seven cooperating concurrent processes. The Frame Transmitter process and the Frame Receiver process are provided by the clients of the MAC sublayer (which may include the LLC sublayer) and make use of the interface operations provided by the MAC sublayer. The other five processes are defined to reside in the MAC sublayer. The seven processes are as follows:

a) Frame Transmitter process
b) Frame Receiver process
c) Bit Transmitter process
d) Bit Receiver process
e) Deference process
f) BurstTime process
g) SetExtending process

This organization of the model is illustrated in ~~Figure 4–3~~ Figure 4–2 and reflects the fact that the communication of entire frames is initiated by the client of the MAC sublayer, while the timing of collision backoff and of individual bit transfers is based on interactions between the MAC sublayer and the Physical-Layer-dependent bit time.

~~Figure 4–3~~Figure 4–2 depicts the static structure of the procedural model, showing how the various processes and procedures interact by invoking each other. ~~Figures 4–4a), 4–4b), and 4–5~~ Figures 4–3a, 4–3b, 4-4a and 4–4b summarize the dynamic behavior of the model during transmission and reception, focusing on the steps that shall be performed, rather than the procedural structure that performs them. The usage of the shared-state variables is not depicted in the figures, but is described in the comments and prose in the following subclauses.

Change Figure 4–4a as follows:

- ***Change the figure number from "Figure 4–4" to "Figure 4–3."***
- ***Change the second note to read as follows:***

  * Applicable only to half duplex operation at ~~> 100~~ 1000 Mb/s.

Change Figure 4–4b as follows:

- ***Change the figure number from "Figure 4–4" to "Figure 4–3."***

Change Figure 4–5a as follows:

- ***Change the figure number from "Figure 4–5" to "Figure 4–4."***
- ***Change the second note to read as follows:***

  * Applicable only to half duplex operation at ~~> 100~~ 1000 Mb/s.

Change Figure 4–5b as follows:

- ***Change the figure number from "Figure 4–5" to "Figure 4–4."***
- ***Change the note to read as follows:***

  * Applicable only to half duplex operation at ~~> 100~~ 1000 Mb/s.

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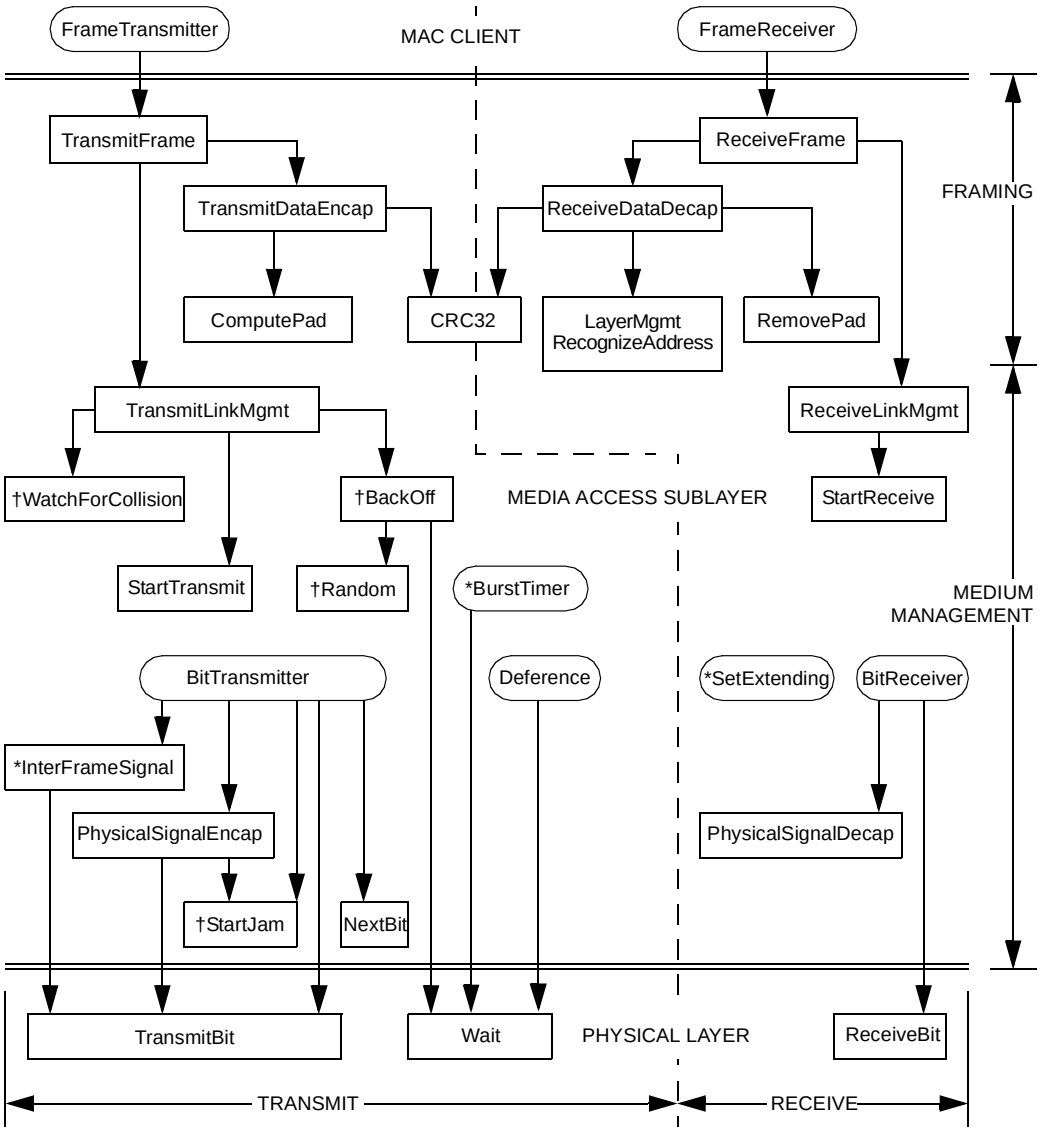
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Change Figure 4–3 as follows:

- ***Change the figure number from "Figure 4–3" to "Figure 4–2."***
- ***Replace "RecognizeAddress" with "LayerMgmtRecognizeAddress."***
- ***Add an arrow between Deference and Wait.***
- ***Delete function RealTimeDelay.***
- ***Change the second note to read as follows:***

* Applicable only to half duplex operation at ~~> 100~~ 1000 Mb/s.



† Not applicable to full duplex operation.
* Applicable only to half duplex operation at ~~> 100~~ 1000 Mb/s.

Figure 4–2—Relationship among CSMA/CD procedures

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4.2.2.4 Layer management extensions to procedural model

Change 4.2.2.4 to read as follows:

In order to incorporate network management functions, this Procedural Model has been expanded beyond that provided in ISO/IEC 8802-3: 1990. Network management functions have been incorporated in two ways. First, 4.2.7 through 4.2.10, 4.3.2, and ~~Figure 4–4~~ Figures 4–3a and 4-3b, have been modified and expanded to provide management services. Second, Layer Management procedures have been added as 5.2.4. Note that Pascal variables are shared between Clause 4 and Clause 5. Within the Pascal descriptions provided in Clause 4, a "‡" in the left margin indicates a line that has been added to support management services. These lines are only required if Layer Management is being implemented. These changes do not affect any aspect of the MAC behavior as observed at the LLC-MAC and MAC-PLS interfaces of ISO/IEC 8802-3: 1990.

The Pascal procedural specification shall be consulted for the definitive statement when there is any apparent ambiguity concerning the definition of some aspect of the CSMA/CD MAC access method.

The Layer Management facilities provided by the CSMA/CD MAC and Physical Layer management definitions provide the ability to manipulate management counters and initiate actions within the layers. The managed objects within this standard are defined as sets of attributes, actions, notifications, and behaviors in accordance with IEEE Std 802.1F-1993, and ISO/IEC International Standards for network management.

4.2.3 Frame transmission model

Change 4.2.3 to read as follows:

Frame transmission includes the following data encapsulation and Media Access management aspects:

a) Transmit Data Encapsulation includes the assembly of the outgoing frame (from the values provided by the MAC client) and frame check sequence generation (if not provided by the MAC client).
b) Transmit Media Access Management includes carrier deference, interframe spacing, collision detection and enforcement, collision backoff and retransmission, carrier extension and frame bursting.

4.2.3.1 Transmit data encapsulation

Change 4.2.3.1 to read as follows:

~~**4.2.3.1.1 Frame assembly**~~

~~The fields of the CSMA/CD MAC frame are set to the values provided by the MAC client as arguments to the TransmitFrame operation (see 4.3) with the following exceptions: the padding field, the extension field, and the frame check sequence. The padding field is necessary to enforce the minimum frame size. The extension field is necessary to enforce the minimum carrier event duration on the medium in the half duplex mode at operating speeds above 100 Mb/s. The frame check sequence is set to the CRC value generated by the MAC sublayer.~~

~~**4.2.3.1.2 Frame check sequence generation**~~

~~The CRC value defined in 3.8 is generated and inserted in the frame check sequence field, following the fields supplied by the MAC client.~~

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The fields of the CSMA/CD MAC frame are set to the values provided by the MAC client as arguments to the TransmitFrame operation (see 4.3) with the following possible exceptions: the padding field, the extension field, and the frame check sequence. The padding field is necessary to enforce the minimum frame size. The extension field is necessary to enforce the minimum carrier event duration on the medium in half duplex mode at an operating speed of 1000 Mb/s. The frame check sequence field may be (optionally) provided as an argument to the MAC sublayer. It is optional for a MAC to support the provision of the frame check sequence in such an argument. If this field is provided by the MAC client, the padding field shall also be provided by the MAC client, if necessary. If this field is not provided by the MAC client, or if the MAC does not support the provision of the frame check sequence as an external argument, it is set to the CRC value generated by the MAC sublayer, after appending the padding field, if necessary.

4.2.3.2.2 Interframe spacing

Change 4.2.3.2.2 to read as follows:

As defined in ~~4.2.3.1.1~~ 4.2.3.2.1, the rules for deferring to passing frames ensure a minimum interframe spacing of interFrameSpacing ~~seconds~~ bit times. This is intended to provide interframe recovery time for other CSMA/CD sublayers and for the physical medium.

Note that interFrameSpacing is the minimum value of the interframe spacing. If necessary for implementation reasons, a transmitting sublayer may use a larger value with a resulting decrease in its throughput. The larger value is determined by the parameters of the implementation, see 4.4.

A larger value for interframe spacing is used for dynamically adapting the nominal data rate of the MAC sublayer to SONET/SDH data rates (with packet granularity) for WAN-compatible applications of this standard. While in this optional mode of operation, the MAC sublayer counts the number of bits sent during a frame's transmission. After the frame's transmission has been completed, the MAC sublayer extends the minimum interframe spacing by a number of bits that is proportional to the length of the previously transmitted frame. For more details, see 4.2.7 and 4.2.8.

4.2.3.2.7 Frame bursting (half duplex mode only)

Change 4.2.3.2.7 to read as follows:

At ~~operating speeds above 100 Mb/s~~ an operating speed of 1000 Mb/s, an implementation may optionally transmit a series of frames without relinquishing control of the transmission medium. This mode of operation is referred to as *burst mode*. Once a frame has been successfully transmitted, the transmitting station can begin transmission of another frame without contending for the medium, because all of the other stations on the network will continue to defer to its transmission, provided that it does not allow the medium to assume an idle condition between frames. The transmitting station fills the interframe spacing interval with extension bits, which are readily distinguished from data bits at the receiving stations, and which maintain the detection of carrier in the receiving stations. The transmitting station is allowed to initiate frame transmission until a specified limit, referred to as burstLimit, is reached. The value of burstLimit is specified in ~~4.4.2.4~~ 4.4.2. ~~Figure 4–6~~ Figure 4–5 shows an example of transmission with frame bursting.

The first frame of a burst will be extended, if necessary, as described in 4.2.3.4. Subsequent frames within a burst do not require extension. In a properly configured network, and in the absence of errors, collisions cannot occur during a burst at any time after the first frame of a burst (including any extension) has been transmitted. Therefore, the MAC will treat any collision that occurs after the first frame of a burst, or that occurs after the slotTime has been reached in the first frame of a burst, as a late collision.

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Renumber "Figure 4–6" as "Figure 4–5."

4.2.3.3 Minimum frame size

Change 4.2.3.3 to read as follows:

The CSMA/CD Media Access mechanism requires that a minimum frame length of minFrameSize bits be transmitted. If frameSize is less than minFrameSize, then the CSMA/CD MAC sublayer shall append extra bits in units of octets (pad), after the end of the MAC client data field but prior to calculating, and appending, the FCS (if not provided by the MAC client). The number of extra bits shall be sufficient to ensure that the frame, from the DA field through the FCS field inclusive, is at least minFrameSize bits. If the FCS is (optionally) provided by the MAC client, the pad shall also be provided by the MAC client. The content of the pad is unspecified.

4.2.3.4 Carrier extension (half duplex mode only)

Change 4.2.3.4 to read as follows:

At ~~operating speeds above 100 Mb/s~~ an operating speed of 1000 Mb/s, the slotTime employed at slower speeds is inadequate to accommodate network topologies of the desired physical extent. Carrier Extension provides a means by which the slotTime can be increased to a sufficient value for the desired topologies, without increasing the minFrameSize parameter, as this would have deleterious effects. Non-data bits, referred to as extension bits, are appended to frames that are less than slotTime bits in length, so that the resulting transmission is at least one slotTime in duration. Carrier Extension can be performed only if the underlying physical layer is capable of sending and receiving symbols that are readily distinguished from data symbols, as is the case in most physical layers that use a block encoding/decoding scheme. The maximum length of the extension is equal to the quantity (slotTime – minFrameSize). ~~Figure 4–7~~ Figure 4–6 depicts a frame with carrier extension.

The MAC continues to monitor the medium for collisions while it is transmitting extension bits, and it will treat any collision that occurs after the threshold (slotTime) as a late collision.

Renumber "Figure 4–7" as "Figure 4–6."

4.2.4.1.1 Address recognition

Add the following paragraph to the end of 4.2.4.1.1 to read as follows:

The MAC sublayer may also provide the capability of operating in the promiscuous receive mode. In this mode of operation, the MAC sublayer recognizes and accepts all valid frames, regardless of their Destination Address field values.

4.2.4.2.1 Framing

Change the last paragraph in 4.2.4.2.1 to read as follows:

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When a burst of frames is received while operating in half duplex mode at ~~speeds above 100 Mb/s~~ an operating speed of 1000 Mb/s, the individual frames within the burst are delimited by sequences of interframe fill symbols, which are conveyed to the receiving MAC sublayer as extension bits. Once the collision filtering requirements for a given frame, as described in 4.2.4.2.2, have been satisfied, the receipt of an extension bit can be used as an indication that all of the data bits of the frame have been received.

4.2.7 Global declarations

Change 4.2.7 and its related subclauses to read as follows:

This subclause provides detailed formal specifications for the CSMA/CD MAC sublayer. It is a specification of generic features and parameters to be used in systems implementing this media access method. Subclause 4.4 provides values for these sets of parameters for recommended implementations of this media access mechanism.

4.2.7.1 Common constants, types, and variables

The following declarations of constants, types and variables are used by the frame transmission and reception sections of each CSMA/CD sublayer:

const
~~addressSize = ... ; {48 bits in compliance with 3.2.3}~~
addressSize = 48; {In bits, in compliance with 3.2.3}
lengthOrTypeSize = 16; {~~i~~In bits}
~~clientDataSize = ...; {in bits, MAC client Data, see 4.2.2.2, (1)(c)}~~
clientDataSize = ...; {In bits, size of MAC client data; see 4.2.2.2, a) 3)}
padSize = ...; {~~i~~In bits, = max (0, minFrameSize ─ (2 x addressSize + lengthOrTypeSize + clientDataSize + crcSize))}
dataSize = ...; {~~i~~In bits, = clientDataSize + padSize}
crcSize = 32; {In bits, 32-bit CRC~~ = 4 octets~~}
~~frameSize = ...; {in bits, = 2 x addressSize + lengthOrTypeSize + dataSize + crcSize, see 4.2.2.2, (1)}~~
frameSize = ...; {In bits, = 2 x addressSize + lengthOrTypeSize + dataSize + crcSize; see 4.2.2.2, a)}
minFrameSize = ...-; {~~i~~In bits, implementation-dependent, see 4.4}
maxUntaggedFrameSize = ...-; {~~i~~In octets, implementation-dependent, see 4.4}
qTagPrefixSize = 4; {~~i~~In octets, length of QTag Prefix, see 3.5}
extend = ...; {Boolean, true if (slotTime ─ minFrameSize) > 0, false otherwise}
extensionBit = ...; {~~a~~A nondata value which is used for carrier extension and interframe during bursts}
extensionErrorBit = ...; {~~a~~A nondata value which is used to jam during carrier extension}
minTypeValue = 1536; {~~m~~Minimum value of the Length/Type field for Type interpretation}
maxValidFrame = maxUntaggedFrameSize ─ (2 x addressSize + lengthOrTypeSize + crcSize) / 8; {~~i~~In octets, the maximum length of the MAC client data field. This constant is defined for editorial convenience, as a function of other constants}
slotTime = ...-; {In bit times, unit of time for collision handling, implementation-dependent, see 4.4}
~~preambleSize = ...; {56 bits, see 4.2.5}~~
preambleSize = 56; {In bits, see 4.2.5}
sfdSize = 8; {~~8 bit~~In bits, start frame delimiter}
~~headerSize = ...; {64 bits, sum of preambleSize and sfdSize}~~
headerSize = 64; {In bits, sum of preambleSize and sfdSize}
type
Bit = ~~0..1~~(0, 1);
PhysicalBit = ~~0,1, extensionBit, extensionErrorBit~~(0, 1, extensionBit, extensionErrorBit);

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{~~b~~Bits transmitted to the Physical Layer can be either 0, 1, extensionBit or extensionErrorBit. Bits received from the Physical Layer can be either 0, 1 or extensionBit~~.~~}

AddressValue = *array* [1..addressSize] *of* Bit;
LengthOrTypeValue = *array* [1..lengthOrTypeSize] *of* Bit;
DataValue = *array* [1..dataSize] *of* Bit; {Contains the portion of the frame that starts with the first bit following the Length/Type field and ends with the last bit prior to the FCS field. For VLAN Tagged frames, this value includes the Tag Control Information field and the original MAC client Length/Type field. See 3.5}
CRCValue = *array* [1..crcSize] *of* Bit;
PreambleValue = *array* [1..preambleSize] *of* Bit;
SfdValue = *array* [1..sfdSize] *of* Bit;
ViewPoint = (fields, bits); {Two ways to view the contents of a frame}
HeaderViewPoint = (headerFields, headerBits);
Frame = *record* {Format of Media Access frame}
case view: ViewPoint *of*
fields: (
destinationField: AddressValue;
sourceField: AddressValue;
lengthOrTypeField: LengthOrTypeValue;
dataField: DataValue;
fcsField: CRCValue);
bits: (contents: *array* [1..frameSize] *of* Bit)
end; {Frame}

Header = *record* {Format of preamble and start frame delimiter}
case headerView~~-~~: HeaderViewPoint *of*
headerFields~~-~~: (
preamble~~-~~: PreambleValue;
sfd~~-~~: SfdValue);
~~headerBits : (~~
~~headerContents : *array* [1..headerSize] *of* Bit)~~
headerBits: (headerContents: *array* [1..headerSize] *of* Bit)
end; {~~d~~Defines header for MAC frame}
var
halfDuplex: Boolean; {Indicates the desired mode of operation. halfDuplex is a static variable; its value shall only be changed by the invocation of the Initialize procedure}
~~its value does not change between invocations of the Initialize procedure}~~

4.2.7.2 Transmit state variables

The following items are specific to frame transmission. (See also 4.4.)

const
interFrameSpacing = ...~~-~~; {In bit times, minimum ~~time~~ gap between frames. Equal to interFrameGap, see 4.4}
interFrameSpacingPart1 = ...~~-~~; {In bit times, duration of the first portion of interFrameSpacing. In the range of 0 ~~up~~ to 2/3 of interFrameSpacing}
interFrameSpacingPart2 = ...~~-~~; {In bit times, duration of the remainder of interFrameSpacing. Equal to interFrameSpacing – interFrameSpacingPart1}
~~interFrameSize = ... ; {in bits, length of interframe fill during a burst. Equal to interFrameGap divided by the bit period}~~

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ifsStretchRatio = ...; {In bits, determines the number of bits in a frame that require one octet of interFrameSpacing extension, when ifsStretchMode is enabled; implementation dependent, see 4.4}
attemptLimit = ...-; {Max number of times to attempt transmission}
backOffLimit = ...-; {Limit on number of times to back off}
burstLimit= ...-; {~~in bits: Limit~~In bits, limit for initiation of frame transmission in Burst Mode, implementation dependent, see 4.4}
jamSize = ...-; {~~in bits:~~In bits, the value depends upon medium and collision detect implementation}
var
outgoingFrame: Frame; {The frame to be transmitted}
outgoingHeader: Header;
currentTransmitBit, lastTransmitBit: 1..frameSize; {Positions of current and last outgoing bits in outgoingFrame}
lastHeaderBit: 1..headerSize;
deferring: Boolean; {Implies any pending transmission must wait for the medium to clear}
frameWaiting: Boolean; {Indicates that outgoingFrame is deferring}
attempts: 0..attemptLimit; {Number of transmission attempts on outgoingFrame}
newCollision: Boolean; {Indicates that a collision has occurred but has not yet been jammed}
transmitSucceeding: Boolean; {Running indicator of whether transmission is succeeding}
burstMode: Boolean~~.~~; {Indicates the desired mode of operation, and enables the transmission of multiple frames in a single carrier event. burstMode is a static variable; its ~~value does not change between invocations of the Initialize procedure.)~~ value shall only be changed by the invocation of the Initialize procedure}
bursting: Boolean; {In burstMode, the given station has acquired the medium and the burst timer has not yet expired}
burstStart: Boolean; {In burstMode, indicates that the first frame transmission is in progress}
extendError: Boolean; {Indicates a collision occurred while sending extension bits}
ifsStretchMode: Boolean; {Indicates the desired mode of operation, and enables the lowering of the average data rate of the MAC sublayer (with frame granularity), using extension of the minimum interFrameSpacing. ifsStretchMode is a static variable; its value shall only be changed by the invocation of the Initialize procedure}
ifsStretchCount: 0..ifsStretchRatio; {In bits, a running counter that counts the number of bits during a frame's transmission that are to be considered for the minimum interFrameSpacing extension, while operating in ifsStretchMode}
ifsStretchSize: 0..(((maxUntaggedFrameSize + qTagPrefixSize) x 8 + headerSize + interFrameSpacing + ifsStretchRatio – 1) *div* ifsStretchRatio);
{In octets, a running counter that counts the integer number of octets that are to be added to the minimum interFrameSpacing, while operating in ifsStretchMode}

4.2.7.3 Receive state variables

The following items are specific to frame reception. (See also 4.4.)

var
incomingFrame: Frame; {The frame being received}
receiving: Boolean; {Indicates that a frame reception is in progress}
excessBits: 0..7; {Count of excess trailing bits beyond octet boundary}
receiveSucceeding: Boolean; {Running indicator of whether reception is succeeding}
validLength: Boolean; {Indicator of whether received frame has a length error}
exceedsMaxLength: Boolean; {Indicator of whether received frame has a length longer than the maximum permitted length}
extending: Boolean; {Indicates whether the current frame is subject to carrier extension}
extensionOK: Boolean; {Indicates whether any bit errors were found in the extension part of a frame,

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which is not checked by the CRC}
passReceiveFCSMode: Boolean; {Indicates the desired mode of operation, and enables passing of the frame check sequence field of all received frames from the MAC sublayer to the MAC client. passReceiveFCSMode is a static variable}

4.2.7.4 Summary of interlayer interfaces

a) The interface to the MAC client, defined in 4.3.2, is summarized below:

type
TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError, lateCollisionErrorStatus);
{Result of TransmitFrame operation, reporting of lateCollisionErrorStatus is optional for MACs operating at speeds at or below 100Mb/s}
ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError, lengthError, alignmentError); {Result of ReceiveFrame operation}
function TransmitFrame (
destinationParam: AddressValue;
sourceParam: AddressValue;
lengthOrTypeParam: LengthOrTypeValue;
~~dataParam: DataValue): TransmitStatus; {Transmits one frame}~~
dataParam: DataValue;
fcsParamValue: CRCValue;
fcsParamPresent: Bit): TransmitStatus; {Transmits one frame}
function ReceiveFrame (
var destinationParam: AddressValue;
var sourceParam: AddressValue;
var lengthOrTypeParam: LengthOrTypeValue;
~~*var* dataParam: DataValue): ReceiveStatus; {Receives one frame}~~
var dataParam: DataValue;
var fcsParamValue: CRCValue;
var fcsParamPresent: Bit): ReceiveStatus; {Receives one frame}

b) The interface to the Physical Layer, defined in 4.3.3, is summarized in the following:

var
receiveDataValid: Boolean; {Indicates incoming bits}
carrierSense: Boolean; {In half duplex mode, indicates that transmission should defer}
transmitting: Boolean; {Indicates outgoing bits}
collisionDetect: Boolean; {Indicates medium contention}
procedure TransmitBit (bitParam: PhysicalBit); {Transmits one bit}
function ReceiveBit: PhysicalBit; {Receives one bit}
procedure Wait (bitTimes: integer); {Waits for indicated number of bit times}

4.2.7.5 State variable initialization

The procedure Initialize must be run when the MAC sublayer begins operation, before any of the processes begin execution. Initialize sets certain crucial shared state variables to their initial values. (All other global variables are appropriately reinitialized before each use.) Initialize then waits for the medium to be idle, and starts operation of the various processes.

NOTE—Care should be taken to ensure that the time from the completion of the Initialize process to when the first packet transmission begins is at least an interFrameGap.

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If Layer Management is implemented, the Initialize procedure shall only be called as the result of the initializeMAC action (30.3.1.2.1).

```
procedure Initialize;
~~begin~~begin
    frameWaiting := false;
    deferring := false;
    newCollision := false;
    transmitting := false; {~~I~~An interface to Physical Layer; see below}
    receiving := false;
    halfDuplex := ...; {~~t~~True for half duplex operation, false for full duplex operation. For operation at
                        speeds above 1000 Mb/s, halfDuplex shall always be false}~~halfDuplex is a static
                        variable; its value does not change between invocations of the Initialize~~
    bursting := false;
    burstMode := ...; {~~t~~True for half duplex operation at~~ speeds above 100 Mb/s~~ an operating speed of 1000
                        Mb/s, when multiple frames' transmission in a single carrier event is desired and
                        supported, false otherwise}~~. burstMode is a static variable; its value does not change
                        between invocations of the Initialize procedure}~~
    extending := extend ~~and~~and halfDuplex;
    ifsStretchMode := ...; {True for operating speeds above 1000 Mb/s when lowering the average data rate
                            of the MAC sublayer (with frame granularity) is desired and supported, false
                            otherwise}
    ifsStretchCount := 0;
    ifsStretchSize := 0;
    passReceiveFCSMode := ...; {True when enabling the passing of the frame check sequence of all
                                received frames from the MAC sublayer to the MAC client is desired and
                                supported, false otherwise}
    ~~while carrierSense or receiveDataValid do nothing~~
    if halfDuplex then while carrierSense or receiveDataValid do nothing
    else while receiveDataValid do nothing
    {Start execution of all processes}
end; {Initialize}
```

4.2.8 Frame transmission

Change subclause 4.2.8 to read as follows:

The algorithms in this subclause define MAC sublayer frame transmission. The function TransmitFrame implements the frame transmission operation provided to the MAC client:

```
function TransmitFrame (
    destinationParam: AddressValue;
    sourceParam: AddressValue;
    lengthOrTypeParam: LengthOrTypeValue;
    ~~dataParam: DataValue): TransmitStatus;~~
    dataParam: DataValue;
    fcsParamValue: CRCValue;
    fcsParamPresent: Bit): TransmitStatus;
procedure TransmitDataEncap; ~~... {n~~{Nested procedure; see body below}
begin
    if transmitEnabled then
        begin
            TransmitDataEncap;
```


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```
            TransmitFrame := TransmitLinkMgmt
        end
    else TransmitFrame := transmitDisabled
end; {TransmitFrame}
```

If transmission is enabled, TransmitFrame calls the internal procedure TransmitDataEncap to construct the frame. Next, TransmitLinkMgmt is called to perform the actual transmission. The TransmitStatus returned indicates the success or failure of the transmission attempt.

TransmitDataEncap builds the frame and places the 32-bit CRC in the frame check sequence field:

```
procedure TransmitDataEncap;
begin
    with outgoingFrame do
        begin {~~a~~Assemble frame}
            view := fields;
            destinationField := destinationParam;
            sourceField := sourceParam;
            lengthOrTypeField := lengthOrTypeParam;
            ~~dataField := ComputePad (dataParam);~~
            ~~fcsField := CRC32(outgoingFrame);~~
            if fcsParamPresent then
                begin
                    dataField := dataParam; {No need to generate pad if the FCS is passed from MAC client}
                    fcsField := fcsParamValue {Use the FCS passed from MAC client}
                end
            else
                begin
                    dataField := ComputePad(dataParam);
                    fcsField := CRC32(outgoingFrame)
                end;
            view := bits
        end {~~a~~Assemble frame}
    with outgoingHeader do
        begin
            headerView := headerFields;
            preamble := ...; {* '1010...10,' LSB to MSB*}
            sfd := ...; {* '10101011,' LSB to MSB*}
            headerView := headerBits
        end
end; {TransmitDataEncap}
```

If the MAC client chooses to generate the frame check sequence field for the frame, it passes this field to the MAC sublayer via the fcsParamValue parameter. If the fcsParamPresent parameter is true, TransmitDataEncap uses the fcsParamValue parameter as the frame check sequence field for the frame. Such a frame shall not require any padding, since it is the responsibility of the MAC client to ensure that the frame meets the minFrameSize constraint. If the fcsParamPresent parameter is false, the fcsParamValue parameter is unspecified.TransmitDataEncap first calls the ComputePad function, followed by a call to the CRC32 function to generate the padding (if necessary) and the frame check sequence field for the frame internally to the MAC sublayer.

ComputePad appends an array of arbitrary bits to the MAC client data to pad the frame to the minimum frame size~~.~~:

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```
~~function ComputePad(~~
      ~~var dataParam: DataValue): DataValue;~~
~~begin~~
   ~~ComputePad := {Append an array of size padSize of arbitrary bits to the MAC client dataField}~~
~~end; {ComputePadParam}~~

function ComputePad(var dataParam: DataValue): DataValue;
begin
   ComputePad := {Append an array of size padSize of arbitrary bits to the MAC client dataField}
end; {ComputePad}
```

TransmitLinkMgmt attempts to transmit the frame. In half duplex mode, it first defers to any passing traffic. In half duplex mode, if a collision occurs, transmission is terminated properly and retransmission is scheduled following a suitable backoff interval:

```
function TransmitLinkMgmt: TransmitStatus;
begin
   attempts := 0;
   transmitSucceeding := false;
   lateCollisionCount := 0;
   deferred := false; {~~i~~Initialize}
   excessDefer := false;
   while  (attempts < attemptLimit) and (not transmitSucceeding)
                                          and (not extend or lateCollisionCount = 0) do
                                    {~~n~~No retransmission after late collision if operating at~~> 100~~ 1000 Mb/s}
      begin {~~l~~Loop}
         if bursting then {~~t~~This is a burst continuation}
            frameWaiting := true {~~s~~Start transmission without checking deference}
         else {~~n~~Non bursting case, or first frame of a burst}
            begin
               if attempts > 0 then BackOff;
               ~~if halfDuplex then frameWaiting := true;~~
               frameWaiting := true;
               while deferring do {~~d~~Defer to passing frame, if any[3]}
                  if halfDuplex then deferred := true;
                  ~~begin~~
                     ~~nothing;~~
~~‡~~                  ~~if halfDuplex then deferred := true~~
                  ~~end;~~
               burstStart := true;
               if burstMode then bursting := true
            end;
         lateCollisionError := false;
         StartTransmit;
         frameWaiting := false;
         if halfDuplex then
         begin
            ~~frameWaiting := false;~~
            while transmitting do WatchForCollision;
            if lateCollisionError then lateCollisionCount := lateCollisionCount + 1;
               ~~lateCollisionCount := lateCollisionCount + 1;~~
```

[3] The Deference process ensures that the reception of traffic does not cause deferring to be true when in full duplex mode. Deferring is used in full duplex mode to enforce the minimum interpacket gap spacing.

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```
            attempts := attempts + 1
         end {~~h~~Half duplex mode}
         else while transmitting do nothing {~~f~~Full duplex mode}
      end; {~~l~~Loop}
   LayerMgmtTransmitCounters; {~~u~~Update transmit and transmit error counters in 5.2.4.2}
   if transmitSucceeding then
      begin
         if burstMode then burstStart := false; {Can't be the first frame anymore}
         TransmitLinkMgmt := transmitOK
      end
   else if (extend and lateCollisionCount > 0) then TransmitLinkMgmt := lateCollisionErrorStatus;
      ~~TransmitLinkMgmt := lateCollisionErrorStatus;~~
   else  TransmitLinkMgmt := excessiveCollisionError
end; {TransmitLinkMgmt}
```

Each time a frame transmission attempt is initiated, StartTransmit is called to alert the BitTransmitter process that bit transmission should begin:

```
procedure StartTransmit;
begin
   currentTransmitBit := 1;
   lastTransmitBit := frameSize;
   transmitSucceeding := true;
   transmitting := true;
   lastHeaderBit~~:~~ := headerSize
end; {StartTransmit}
```

In half duplex mode, TransmitLinkMgmt monitors the medium for contention by repeatedly calling WatchForCollision, once frame transmission has been initiated:

```
procedure WatchForCollision;
begin
   if transmitSucceeding and collisionDetect then
      begin
         if currentTransmitBit > (slotTime – headerSize) then lateCollisionError := true;
            ~~lateCollisionError := true;~~
         newCollision := true;
         transmitSucceeding := false;
         if burstMode then
         begin
            bursting := false;
            if not burstStart then
               lateCollisionError := true {Every collision is late, unless it hits the first frame in a burst}
         end
      end
end; {WatchForCollision}
```

WatchForCollision, upon detecting a collision, updates newCollision to ensure proper jamming by the BitTransmitter process. The current transmit bit number is checked to see if this is a late collision. If the collision occurs later than a collision window of slotTime bits into the packet, it is considered as evidence of a late collision. The point at which the collision is received is determined by the network media propagation

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time and the delay time through a station and, as such, is implementation-dependent (see 4.1.2.2). While operating at speeds of 100 Mb/s or lower, an implementation may optionally elect to end retransmission attempts after a late collision is detected. While operating at ~~speeds above 100 Mb/s~~ the speed of 1000 Mb/s, an implementation shall end retransmission attempts after a late collision is detected.

After transmission of the jam has been completed, if TransmitLinkMgmt determines that another attempt should be made, BackOff is called to schedule the next attempt to retransmit the frame.

```
function Random (low, high: integer): integer;
begin
   Random := ...{tUniformly distributed random integer r, such that low ≤ r < high}
end; {Random}
```

BackOff performs the truncated binary exponential backoff computation and then waits for the selected multiple of the slot time~~.~~:

```
var maxBackOff: 2..1024; {Working variable of BackOff}
procedure BackOff;
begin
   if attempts = 1 then maxBackOff := 2
   else if attempts ≤ backOffLimit then maxBackOff := maxBackOff x 2;
   Wait(slotTime x Random(0, maxBackOff))
end; {BackOff}
```

BurstTimer is a process that does nothing unless the bursting variable is true. When bursting is true, BurstTimer increments burstCounter until the burstLimit limit is reached, whereupon BurstTimer assigns the value false to bursting~~.~~:

```
process BurstTimer;
   var burstCounter: integer;
begin
   cycle
      while not bursting do nothing; {wait for a burst}
      burstCounter := 0;
      while bursting and (burstCounter < burstLimit) do
         begin
            Wait(1);
            burstCounter := burstCounter + 1
         end;
      bursting := false
   end {burstMode cycle}
end; {BurstTimer}
```

```
process BurstTimer;
begin
   cycle
      while not bursting do nothing; {Wait for a burst}
      Wait(burstLimit);
      bursting := false
   end {burstMode cycle}
end; {BurstTimer}
```

The Deference process runs asynchronously to continuously compute the proper value for the variable deferring. In the case of half duplex burst mode, deferring remains true throughout the entire burst. Interframe

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spacing may be used to lower the average data rate of a MAC at operating speeds above 1000 Mb/s in the full duplex mode, when it is necessary to adapt it to the data rate of a WAN-based physical layer. When interframe stretching is enabled, deferring remains true throughout the entire extended interframe gap, which includes the sum of interFrameSpacing and the interframe extension as determined by the BitTransmitter:

```
process Deference;
   var realTimeCounter: integer; wasTransmitting: Boolean;
begin
   if halfDuplex then cycle{hHalf duplex loop}
      while not carrierSense do nothing; {wWatch for carrier to appear}
      deferring := true;  {dDelay start of new transmissions}
      wasTransmitting := transmitting;
      while carrierSense or transmitting do wasTransmitting := wasTransmitting or transmitting;
         wasTransmitting: = wasTransmitting or transmitting;
      if wasTransmitting then Wait(interFrameSpacingPart1) {Time out first part of interframe gap}
         begin
            StartRealTimeDelay; {time out first part interframe gap}
            while RealTimeDelay(interFrameSpacingPart1) do nothing
         end
      else
         begin
            StartRealTimeDelay;
            repeat
            while carrierSense do StartRealTimeDelay
            until not RealTimeDelay(interFrameSpacingPart1)
            realTimeCounter := interFrameSpacingPart1;
            repeat
               while carrierSense do realTimeCounter := interFrameSpacingPart1;
               Wait(1);
               realTimeCounter := realTimeCounter – 1
            until (realTimeCounter = 0)
         end;
      StartRealTimeDelay; {time out second part interframe gap}
      while RealTimeDelay(interFrameSpacingPart2) do nothing;
      Wait(interFrameSpacingPart2); {Time out second part of interframe gap}
      deferring: = := false; {aAllow new transmissions to proceed}
      while frameWaiting do nothing {aAllow waiting transmission, if any}
   end {hHalf duplex loop}
   else cycle {fFull duplex loop}
      while not transmitting do nothing; {wWait for the start of a transmission}
      deferring := true; {iInhibit future transmissions}
      while transmitting do nothing; {wWait for the end of the current transmission}
      StartRealTimeDelay; {time out an interframe gap}
      while RealTimeDelay(interFrameSpacing) do nothing;
      Wait(interFrameSpacing + ifsStretchSize x 8); {Time out entire interframe gap and IFS extension}
      if not frameWaiting then {Don't roll over the remainder into the next frame}
         begin
            Wait(8);
            ifsStretchCount := 0
         end
      deferring := false {dDon't inhibit transmission}
   end {fFull duplex loop}
end; {Deference}
```

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If the ifsStretchMode is enabled, the Deference process continues to enforce interframe spacing for an additional number of bit times, after the completion of timing the interFrameSpacing. The additional number of bit times is reflected by the variable ifsStretchSize. If the variable ifsStretchCount is less than ifsStretchRatio and the next frame is ready for transmission (variable frameWaiting is true), the Deference process enforces interframe spacing only for the integer number of octets, as indicated by ifsStretchSize, and saves ifsStretchCount for the next frame's transmission. If the next frame is not ready for transmission (variable frameWaiting is false), then the Deference process initializes the ifsStretchCount variable to zero.

```
procedure StartRealTimeDelay
   begin
      {reset the realtime timer and start it timing}
   end; {StartRealTimeDelay}

function RealTimeDelay (µsec:real): Boolean;
   begin
      {return the value true if the specified number of microseconds have
      not elapsed since the most recent invocation of StartRealTimeDelay,
      otherwise return the value false}
   end; {RealTimeDelay}
```

The BitTransmitter process runs asynchronously, transmitting bits at a rate determined by the Physical Layer's TransmitBit operation:

```
process BitTransmitter;
begin
   cycle {oOuter loop}
      if transmitting then
         begin {iInner loop}
            extendError := false;
            if ifsStretchMode then {Calculate the counter values}
               begin
                  ifsStretchSize := (ifsStretchCount + headerSize + frameSize + interFrameSpacing) div
                                                      ifsStretchRatio; {Extension of the interframe spacing}
                  ifsStretchCount := (ifsStretchCount + headerSize + frameSize + interFrameSpacing)
                        mod ifsStretchRatio {Remainder to carry over into the next frame's transmission}
               end;
            PhysicalSignalEncap;  {Send preamble and start of frame delimiter}
            while transmitting do
               begin
                  if (currentTransmitBit > lastTransmitBit) then TransmitBit(extensionBit)
                  else if extendError then TransmitBit(extensionErrorBit) {Jam in extension}
                     if extendError then
                        TransmitBit(extensionErrorBit) {jam in extension}
                  else TransmitBit(outgoingFrame[currentTransmitBit]);
                        TransmitBit(outgoingFrame[currentTransmitBit]);
                  if newCollision then StartJam else NextBit
               end;
            if bursting then
               begin
                  InterFrameSignal;
                  if extendError then
                     if transmitting then transmitting := false {TransmitFrame may have been
                                                      called during InterFrameSignal}
                                    {TransmitFrame may have been called during InterFrameSignal}
```


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```
                    else IncLargeCounter(lateCollision);
                                {Count late collisions which were missed by TransmitLinkMgmt}
                        IncLargeCounter(lateCollision); {count late collisions which
                                were missed by TransmitLinkMgmt}
                    bursting := bursting and (frameWaiting or transmitting)
                end
            end {iInner loop}
        end {oOuter loop}
    end; {BitTransmitter}
```

The bits transmitted to the physical layer can take one of four values: data zero (0), data one (1), extensionBit (EXTEND), or extensionErrorBit (EXTEND_ERROR). The values extensionBit and extensionErrorBit are not transmitted between the first preamble bit of a frame and the last data bit of a frame under any circumstances. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionBit only when it is necessary to perform carrier extension on a frame after all of the data bits of a frame have been transmitted. The BitTransmitter calls the procedure TransmitBit with bitParam = extensionErrorBit only when it is necessary to jam during carrier extension.

```
    procedure PhysicalSignalEncap;
    begin
        while currentTransmitBit ≤ lastHeaderBit do
            begin
                TransmitBit(outgoingHeader[currentTransmitBit]); {tTransmit header one bit at a time}
                currentTransmitBit := currentTransmitBit + 1
            end;
        if newCollision then StartJam else currentTransmitBit := 1
        currentTransmitBit := 1
    end; {PhysicalSignalEncap}
```

The procedure InterFrameSignal fills the interframe interval between the frames of a burst with extensionBits. InterFrameSignal also monitors the variable collisionDetect during the interframe interval between the frames of a burst, and will end a burst if a collision occurs during the interframe interval. The procedural model is defined such that a MAC operating in the burstMode will emit an extraneous sequence of interFrameSize extensionBits in the event that there are no additional frames ready for transmission after InterFrameSignal returns. Implementations may be able to avoid sending this extraneous sequence of extensionBits if they have access to information (such as the occupancy of a transmit queue) that is not assumed to be available to the procedural model.

```
    procedure InterFrameSignal;
        var interFrameCount, interFrameTotal-: integer;
    begin
        interFrameCount := 0;
        interFrameTotal := interFrameSize;
        interFrameTotal := interFrameSpacing;
        while interFrameCount < interFrameTotal do
            begin
                if not extendError then TransmitBit(extensionBit)
                    TransmitBit(extensionBit)
                else TransmitBit(extensionErrorBit);
                    TransmitBit(extensionErrorBit);
                interFrameCount := interFrameCount + 1;
                if collisionDetect and not extendError then
                begin
                    bursting := false;
```

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```
                extendError := true;
                interFrameCount := 0;
                interFrameTotal := jamSize
            end
        end
    end; {InterFrameSignal}

    procedure NextBit;
    begin
        currentTransmitBit := currentTransmitBit + 1;
        if halfDuplex and burstStart and transmitSucceeding then {eCarrier extension may be required}
            transmitting := (currentTransmitBit ≤ max(lastTransmitBit, slotTime))
        else transmitting := (currentTransmitBit ≤ lastTransmitBit)
            transmitting := (currentTransmitBit ≤ lastTransmitBit)
    end; {NextBit}

    procedure StartJam;
    begin
        extendError := currentTransmitBit > lastTransmitBit;
        currentTransmitBit := 1;
        lastTransmitBit := jamSize;
        newCollision := false
    end; {StartJam}
```

BitTransmitter, upon detecting a new collision, immediately enforces it by calling StartJam to initiate the transmission of the jam. The jam should contain a sufficient number of bits of arbitrary data so that it is assured that both communicating stations detect the collision. (StartJam uses the first set of bits of the frame up to jamSize, merely to simplify this program.)

4.2.9 Frame reception

Change subclause 4.2.9 to read as follows:

The algorithms in this subclause define CSMA/CD Media Access sublayer frame reception.

The function ReceiveFrame implements the frame reception operation provided to the MAC client:

```
    function ReceiveFrame (
        var destinationParam: AddressValue;
        var sourceParam: AddressValue;
        var lengthOrTypeParam: LengthOrTypeValue;
        var dataParam: DataValue): ReceiveStatus;
        var dataParam: DataValue;
        var fcsParamValue: CRCValue;
        var fcsParamPresent: Bit): ReceiveStatus;
    function ReceiveDataDecap: ReceiveStatus; ... {n{Nested function; see body below}
    begin
        if receiveEnabled then
            repeat
                ReceiveLinkMgmt;
                ReceiveFrame := ReceiveDataDecap;
            until receiveSucceeding
        else ReceiveFrame := receiveDisabled
            ReceiveFrame := receiveDisabled
    end; {ReceiveFrame}
```


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If enabled, ReceiveFrame calls ReceiveLinkMgmt to receive the next valid frame, and then calls the internal function ReceiveDataDecap to return the frame's fields to the MAC client if the frame's address indicates that it should do so. The returned ReceiveStatus indicates the presence or absence of detected transmission errors in the frame.

```
    function ReceiveDataDecap: ReceiveStatus;
‡       var status-: ReceiveStatus; {hHolds receive status information}
    begin
‡       with incomingFrame do
‡           begin
‡               view := fields;
                receiveSucceeding := RecognizeAddress (incomingFrame, destinationField);
‡               receiveSucceeding := LayerMgmtRecognizeAddress-(destinationField);
                if receiveSucceeding then
                    begin {dDisassemble frame}
                        destinationParam := destinationField;
                        sourceParam := sourceField;
                        lengthOrTypeParam:= := lengthOrTypeField;
                        dataParam := RemovePad-(lengthOrTypeField, dataField);
                        fcsParamValue := fcsField;
                        fcsParamPresent := passReceiveFCSMode;
                        exceedsMaxLength := ...; {{Check to determine if receive frame size exceeds the maximum
                                                   permitted frame size. MAC implementations may use either
                                                   maxUntaggedFrameSize or (maxUntaggedFrameSize +
                                                   qTagPrefixSize) for the maximum permitted frame size,
                                                   either as a constant or as a function of whether the frame being
                                                   received is a basic or tagged frame (see 3.2, 3.5). In
                                                   implementations that treat this as a constant, it is recommended
                                                   that the larger value be used. The use of the smaller value
                                                   in this case may result in valid tagged frames exceeding the
                                                   maximum permitted frame size.-}
                        if exceedsMaxLength then status := frameTooLong
                        else if fcsField = CRC32(incomingFrame) and extensionOK then
‡                           if validLength then status := receiveOK else status := lengthError
‡                       else if excessBits = 0 or not extensionOK then status := frameCheckError
‡                       else status := alignmentError;
                            if fcsField = CRC32(incomingFrame) and extensionOK then
                                begin
‡                                   if validLength then status: = receiveOK
‡                                   else status: = lengthError
                                end
                            else
                                begin
‡                                   if excessBits = 0 or not extensionOK then status:= frameCheckError
‡                                   else status := alignmentError
                                end;
‡                       LayerMgmtReceiveCounters(status); {Update receive counters in 5.2.4.3}
                            {update receive and receive error counters in 5.2.4.3}
                        view:= := bits
                    end {dDisassemble frame}
‡           end; {wWith incomingFrame}
‡       ReceiveDataDecap := status
    end; {ReceiveDataDecap}
```

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```
function RecognizeAddress (address: AddressValue): Boolean;
begin
   RecognizeAddress := ...; {Returns true for the set of physical, broadcast,
                            and multicast-group addresses corresponding
                            to this station}
end; {RecognizeAddress}

function LayerMgmtRecognizeAddress(address: AddressValue): Boolean;
begin
   if {promiscuous receive enabled} then LayerMgmtRecognizeAddress := true;
   if address = ... {MAC station address} then LayerMgmtRecognizeAddress := true;
   if address = ... {Broadcast address} then LayerMgmtRecognizeAddress := true;
   if address = ... {One of the addresses on the multicast list and multicast reception is enabled} then
                                                        LayerMgmtRecognizeAddress := true;
   LayerMgmtRecognizeAddress := false
end; {LayerMgmtRecognizeAddress}
```

The function RemovePad strips any padding that was generated to meet the minFrameSize constraint, if possible. When the MAC sublayer operates in the mode that enables passing of the frame check sequence field of all received frames to the MAC client (passReceiveFCSMode variable is true), it shall not strip the padding and it shall leave the data field of the frame intact. Length checking is provided for Length interpretations of the Length/Type field. For Length/Type field values in the range between maxValidFrame and minTypeValue, the behavior of the RemovePad function is unspecified.:

```
function RemovePad(var lengthOrTypeParam: LengthOrTypeValue; dataParam: DataValue): DataValue;
   var lengthOrTypeParam:LengthOrTypeValue; dataParam:DataValue):DataValue;
begin
   if lengthOrTypeParam ≥ minTypeValue then
      begin
         validLength := true; {Don't perform length checking for Type field interpretations}
         RemovePad := dataParam
      end
   else if lengthOrTypeParam ≤ maxValidFrame then
      begin
         if lengthOrTypeParam ≤ maxValidFrame then
         begin
         validLength := {For length interpretations of the Length/Type field, check to determine if value
                          represented by Length/Type field matches the received clientDataSize};
         if validLength and not passReceiveFCSMode then
            RemovePad := {tTruncate the dataParam (when present) to the value represented by the
                          lengthOrTypeParam (in octets) and return the result}
         else RemovePad := dataParam
         end
      end
end; {RemovePad}
```

ReceiveLinkMgmt attempts repeatedly to receive the bits of a frame, discarding any fragments from collisions by comparing them to the minimum valid frame size:

```
procedure ReceiveLinkMgmt;
begin
   repeat
      StartReceive;
      while receiving do nothing; {wWait for frame to finish arriving}
```


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```
            excessBits := frameSize mod 8;
            frameSize := frameSize – excessBits; {tTruncate to octet boundary}
            receiveSucceeding := receiveSucceeding and (frameSize ≥ minFrameSize)
                                                                {rReject collision fragments}
        until receiveSucceeding
    end; {ReceiveLinkMgmt}

    procedure StartReceive;
    begin
        receiveSucceeding := true;
        receiving := true
    end; {StartReceive}
```

The BitReceiver process runs asynchronously, receiving bits from the medium at the rate determined by the Physical Layer's ReceiveBit operation, partitioning them into frames, and optionally receiving them:

```
    process BitReceiver;
        var    b-: PhysicalBit;
               incomingFrameSize: integer; {cCount of all bits received in frame including extension}
               frameFinished: Boolean;
               enableBitReceiver: Boolean;
               currentReceiveBit: 1..frameSize; {Position of current bit in incomingFrame}
    begin
        cycle {oOuter loop}
            if receiveEnabled then
                begin {rReceive next frame from physical layer}
                    currentReceiveBit := 1;
                    incomingFrameSize := 0;
                    frameFinished := false;
                    enableBitReceiver := receiving;
                    PhysicalSignalDecap; {Skip idle and extension, strip off preamble and sfd}
                    if enableBitReceiver then extensionOK := true;
                    while receiveDataValid and not frameFinished do
                                                {inner loop to receive the rest of an incoming frame}
                        begin {Inner loop to receive the rest of an incoming frame}
                            b := ReceiveBit; {nNext bit from physical medium}
                            incomingFrameSize := incomingFrameSize + 1;
                            if b = 0 or b = 1 then {nNormal case}
                                if enableBitReceiver then {aAppend to frame}
                                begin
                                    if incomingFrameSize > currentReceiveBit then extensionOK := false;
                                                {Errors in the extension get mapped to data bits on input}
                                    incomingFrame[currentReceiveBit] := b;
                                    currentReceiveBit := currentReceiveBit + 1
                                end
                            else if not extending then frameFinished := true; {b must be an extensionBit}
                                if not extending then frameFinished := true;
                            if incomingFrameSize ≥ slotTime then extending := false
                        end; {iInner loop}
                    if enableBitReceiver then
                        begin
                            frameSize := currentReceiveBit – 1;
                            receiveSucceeding := not extending;
                            receiving := false
```

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```
                end
            end {eEnabled}
        end {oOuter loop}
    end; {BitReceiver}
```

The bits received from the physical layer can take one of three values: data zero (0), data one (1), or extensionBit (EXTEND). The value extensionBit will not occur between the first preamble bit of a frame and the last data bit of a frame in normal circumstances. Extension bits are counted by the BitReceiver but are not appended to the incoming frame. The BitReceiver checks whether the bit received from the physical layer is a data bit or an extensionBit before appending it to the incoming frame. Thus, the array of bits in incomingFrame will only contain data bits. The underlying Reconciliation Sublayer (RS) maps incoming EXTEND_ERROR bits to normal data bits. Thus, the reception of additional data bits after the frame extension has started is an indication that the frame should be discarded.

```
    procedure PhysicalSignalDecap;
    begin
        {Receive one bit at a time from physical medium until a valid sfd is detected, discard bits and return.}
    end; {PhysicalSignalDecap}
```

The process SetExtending controls the extending variable, which determines whether a received frame must be at least slotTime bits in length or merely minFrameSize bits in length to be considered valid by the BitReceiver. SetExtending sets the extending variable to true whenever receiveDataValid is de-asserted, while in half duplex mode at ~~operating speeds above 100 Mb/s.~~ an operating speed of 1000 Mb/s:

```
    process SetExtending;
    begin
        ~~cycle~~cycle {~~l~~Loop forever}
            while receiveDataValid do nothing;
            extending := extend and halfDuplex
        end {~~l~~Loop}
    end; {SetExtending}
```

4.2.10 Common procedures

Change 4.2.10 to read as follows:

The function CRC32 is used by both the transmit and receive algorithms to generate a 32-bit CRC value:

```
    function CRC32(f: Frame): CRCValue;
    begin
        CRC32 := {The 32-bit CRC for the entire frame, excluding the FCS field (if present)}
    end; {CRC32}
```

Purely to enhance readability, the following procedure is also defined:

```
    procedure nothing; begin end;
```

The idle state of a process (that is, while waiting for some event) is cast as repeated calls on this procedure.

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4.3.2 Services provided by the MAC sublayer

Change 4.3.2 to read as follows:

The services provided to the MAC client by the MAC sublayer are transmission and reception of frames. The interface through which the MAC client uses the facilities of the MAC sublayer therefore consists of a pair of functions.

Functions:

TransmitFrame

ReceiveFrame

Each of these functions has the components of a frame as its parameters (input or output), and returns a status code as its result. ~~Note that the service_class defined in 2.3.1 is ignored by the CSMA/CD MAC.~~

NOTE 1—The frame_check_sequence parameter defined in 2.3.1 and 2.3.2 is mapped here into two variables: fcsParamValue and fcsParamPresent. This mapping has been defined for editorial convenience. The fcsParamPresent variable indicates the presence or absence of the fcsParamValue variable in the two function calls. If the fcsParamPresent variable is true, the fcsParamValue variable contains the frame check sequence for the corresponding frame. If the fcsParamPresent variable is false, the fcsParamValue variable is unspecified. If the MAC sublayer does not support client-supplied frame check sequence values, then the fcsParamPresent variable in TransmitFrame shall always be false.

NOTE 2—The mac_service_data_unit parameter defined in 2.3.1 and 2.3.2 is mapped here into two variables: lengthOrTypeParam and dataParam. This mapping has been defined for editorial convenience. The first two octets of the mac_service_data_unit parameter contain the lengthOrTypeParam variable. The remaining octets of the mac_service_data_unit parameter form the dataParam variable.

The MAC client transmits a frame by invoking TransmitFrame:

~~function *TransmitFrame (*~~

function TransmitFrame (
destinationParam: AddressValue;
sourceParam: AddressValue;
lengthOrTypeParam: LengthOrTypeValue;
~~dataParam: DataValue): TransmitStatus;~~
dataParam: DataValue;
fcsParamValue: CRCValue;
fcsParamPresent: Bit): TransmitStatus;

The TransmitFrame operation is synchronous. Its duration is the entire attempt to transmit the frame; when the operation completes, transmission has either succeeded or failed, as indicated by the resulting status code:

type TransmitStatus = (transmitOK, excessiveCollisionError, lateCollisionErrorStatus);

‡ *type* TransmitStatus = (transmitDisabled, transmitOK, excessiveCollisionError,
lateCollisionErrorStatus);

The transmitDisabled status code indicates that the transmitter is not enabled. Successful transmission is indicated by the status code transmitOK~~;~~. ~~t~~The code excessiveCollisionError indicates that the transmission attempt was aborted due to excessive collisions, because of heavy traffic or a network failure. MACs operating in the half duplex mode ~~at speeds above 100~~ at the speed of 1000 Mb/s are required to report lateCollisionErrorStatus in response to a late collision; MACs operating in the half duplex mode at speeds of 100 Mb/s and below are not required to do so. TransmitStatus is not used by the service interface defined in 2.3.1. TransmitStatus may be used in an implementation dependent manner.

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The MAC client accepts incoming frames by invoking ReceiveFrame:

~~function *ReceiveFrame (*~~
function ReceiveFrame (
var destinationParam: AddressValue;
var sourceParam: AddressValue;
var lengthOrTypeParam: LengthOrTypeValue;
~~*var* dataParam: DataValue): ReceiveStatus;~~
var dataParam: DataValue;
var fcsParamValue: CRCValue;
var fcsParamPresent: Bit): ReceiveStatus;

The ReceiveFrame operation is synchronous. The operation does not complete until a frame has been received. The fields of the frame are delivered via the output parameters with a status code:

type ReceiveStatus = (receiveOK, lengthError, frameCheckError, alignmentError);
‡ *type* ReceiveStatus = (receiveDisabled, receiveOK, frameTooLong, frameCheckError, lengthError, alignmentError);

The receiveDisabled status indicates that the receiver is not enabled. Successful reception is indicated by the status code receiveOK. The frameTooLong error indicates that a frame was received whose frameSize was beyond the maximum allowable frame size. The code frameCheckError indicates that the frame received was damaged by a transmission error. The lengthError indicates that the lengthOrTypeParam value was both consistent with a length interpretation of this field (i.e., its value was less than or equal to maxValidFrame), and inconsistent with the frameSize of the received frame. The code alignmentError indicates that the frame received was damaged, and that in addition, its length was not an integer number of octets. ReceiveStatus is not mapped to any MAC client parameter by the service interface defined in 2.3.2. ReceiveStatus may be used in an implementation dependent manner.

Note that maxValidFrame represents the maximum number of octets that can be carried in the MAC client data field of a frame and is a constant, regardless of whether the frame is a basic or tagged frame (see 3.2 and 3.5). The maximum length of a frame (including all fields from the Destination address through the FCS, inclusive) is either maxUntaggedFrameSize (for basic frames) or maxUntaggedFrameSize + qTagPrefixSize, for tagged frames.

4.3.3 Services required from the physical layer

Change the second note in 4.3.3 to read as follows:

NOTE—When a burst of frames is received in half duplex mode at ~~operating speeds above 100~~ an operating speed of 1000 Mb/s, the variable receiveDataValid will remain true throughout the burst. Furthermore, the variable receiveDataValid remains true throughout the extension field. In these respects, the behavior of the variable receiveDataValid is different from the underlying GMII signal RX_DV, from which it may be derived. See 35.2.1.7.

4.4.2 Allowable implementations

Insert the following into 4.4.2:

The following parameter values shall be used for their corresponding implementations:

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Parameters	Values		
	10 Mb/s 1BASE-5 100 Mb/s	**1 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable
interFrameGap	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable
backoffLimit	10	10	not applicable
jamSize	32 bits	32 bits	not applicable
maxUntaggedFrameSize	1518 octets	1518 octets	1518 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable
ifsStretchRatio	not applicable	not applicable	104 bits

NOTE 1—For 10 Mb/s implementations, the spacing between two successive non-colliding packets, from start of idle at the end of the first packet to start of preamble of the subsequent packet, can have a minimum value of 47 BT (bit times), at the AUI receive line of the DTE. This interFrameGap shrinkage is caused by variable network delays, added preamble bits, and clock skew.

NOTE 2—For 1BASE-5 implementations, see also DTE Deference Delay in 12.9.2.

NOTE 3—For 1 Gb/s implementations, the spacing between two non-colliding packets, from the last bit of the FCS field of the first packet to the first bit of the preamble of the second packet, can have a minimum value of 64 BT (bit times), as measured at the GMII receive signals at the DTE. This interFrameGap shrinkage may be caused by variable network delays, added preamble bits, and clock tolerances.

NOTE 4—For 10 Gb/s implementations, the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the preamble of the second packet, can have a minimum value of 40 BT (bit times), as measured at the XGMII receive signals at the DTE. This interFrameGap shrinkage may be caused by variable network delays and clock tolerances.

NOTE 5—For 10 Gb/s implementations, the value of ifsStretchRatio of 104 bits adapts the average data rate of the MAC sublayer to SONET/SDH STS-192 data rate (with frame granularity), for WAN-compatible applications of this standard.

WARNING

Any deviation from the above specified values may affect proper operation of the network.

4.4.2.1 Parameterized values

Replace the contents of 4.4.2.1 with the following:

See 4.4.2.

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4.4.2.2 Parameterized values

Replace the contents of 4.4.2.2 with the following:

See 4.4.2.

4.4.2.3 Parameterized values

Replace the contents of 4.4.2.3 with the following:

See 4.4.2.

4.4.2.4 Parameterized values

Replace the contents of 4.4.2.4 with the following:

See 4.4.2.

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6. Physical Signaling (PLS) service specifications

6.1 Scope and field of application

Change 6.1 to read as follows:

This clause specifies the services provided by the PLS sublayer to the MAC sublayer ~~for the CSMA/CD clause of this LAN standard, Figure 6–1.~~for 1 Mb/s and 10 Mb/s implementations of this standard (see Figure 6–1). The services are described in an abstract way and do not imply any particular implementation.

Replace Figure 6–1 with the following:

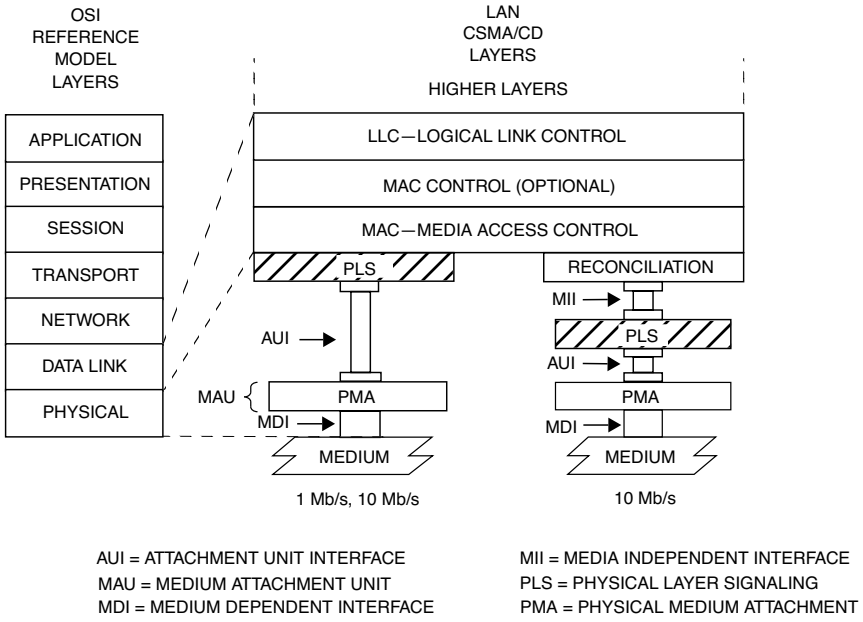


Figure 6–1—PLS service specification relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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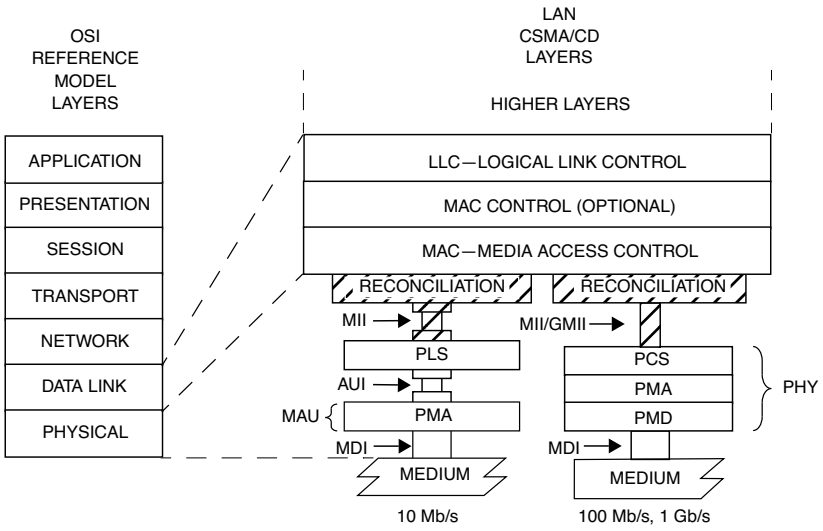
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22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

Replace Figure 22–1 with the following:



AUI = ATTACHMENT UNIT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
MAU = MEDIUM ATTACHMENT UNIT
MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PLS = PHYSICAL LAYER SIGNALING
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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30. 10 Mb/s, 100 Mb/s, 1000 Mb/s, MAC Control, and Link Aggregation Management

Change the title of this clause as follows:

30. 10 Mb/s, 100 Mb/s, 1000 Mb/s~~,~~ and 10 Gb/s ~~MAC Control, and Link Aggregation~~ Management

30.1 Overview

Change the first paragraph of this subclause as follows:

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviors to support 100 Mb/s, ~~and~~ 1000 Mb/s and 10 Gb/s ~~CSMA/CD~~, full duplex operation, MAC Control, and Link Aggregation.

Change the eighth paragraph of this subclause as follows:

Implementation of part or all of ~~10 Mb/s, 100 Mb/s and 1000 Mb/s~~ Layer Management is not a requirement for conformance to any other clause of this standard~~Clauses 4, 7, 9, 22, 23, 24, 25, 26, 27, 28, 31,32, 35, 36, 37, 38, 39, 40, and 41~~.

Insert the following new paragraph at the end of this subclause:

The device that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayer combination as a group. Therefore, in this clause, the term MAU will include PMA and PMD sublayers as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

30.1.1 Scope

Change the first and second paragraph of this subclause as follows:

This clause includes selections from Clauses 5, 19, and 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It also includes the additions for management of MAC Control, DTEs, and repeaters at speeds greater than 10 Mb/s, embedded MAUs, and PHYs.~~full duplex operation, MAC Control, 100 Mb/s and 1000 Mb/s DTEs and repeater units, embedded MAUs, and external PHYs connected with the MII, or GMII.~~ Implementations of management for ~~10 Mb/s~~ DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 or 1000 Mb/s operation, a half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

~~This clause defines a set of mechanisms that enable management of ISO/IEC 8802-3 10 Mb/s, 100 Mb/s, and 1000 Mb/s DTEs, baseband repeater units, and integrated Medium Attachment Units (MAUs). In addition, f~~For 10Mb/s ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of AUI MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard.

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The managed objects within this standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO standards for network management. Managed objects are grouped into mandatory and optional packages.

30.1.4 Management model

Change the fourth paragraph of this subclause as follows:

The above items are defined in 30.3, 30.4, 30.5, ~~and~~ 30.6, 30.7, and 30.8 of this clause in terms of the template requirements of ISO/IEC 10165-4: 1991.

30.2.1 Introduction

Change the second paragraph of this subclause as follows:

All counters defined in this specification are assumed to be wrap-around counters. Wrap-around counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wrap-around counters should be read frequently enough to avoid loss of information. ~~Counters in 30.3, 30.4, 30.5 and 30.6 that have maximum increment rates specified for 10 Mb/s operation, and are appropriate to 100 Mb/s operation, have ten times the stated maximum increment rate for 100 Mb/s operation unless otherwise indicated. Counters that are appropriate to 1000 Mb/s operation have one hundred times the stated maximum increment rate for 1000 Mb/s operation unless otherwise indicated.~~ When a counter has a maximum increment rate specified at one speed of operation, and that counter is appropriate to a higher speed of operation, then the maximum increment rate at that higher speed of operation is

$$\text{maximum increment rate specified} \times \left(\frac{\text{higher speed of operation in Mb/s}}{\text{specified speed of operation in Mb/s}}\right) \quad (30\text{–}1)$$

unless otherwise indicated.

30.2.2.1 Text description of managed objects

Insert the following text immediately after the description of oAutoNegotiation:

oWIS	The managed object of that portion of the containment tree shown in Figure 30-3. The attributes defined in this subclause are contained within the oMAU managed object.

30.2.2.2 Functions to support management

Change the first paragraph of this subclause as follows:

Functions are defined in other clauses that facilitate ~~Clauses 5, 7, 22, 23, 24, 25, 26, 27, 28, 31, 32, 35, 36, 37, 38, 39, 40 and 41 both to facilitate unmanaged operation and~~ managed operation. The functions in other ~~these~~ clauses that facilitate managed operation are referenced from the text of this management clause.

Change the Figure 30–3 as follows:

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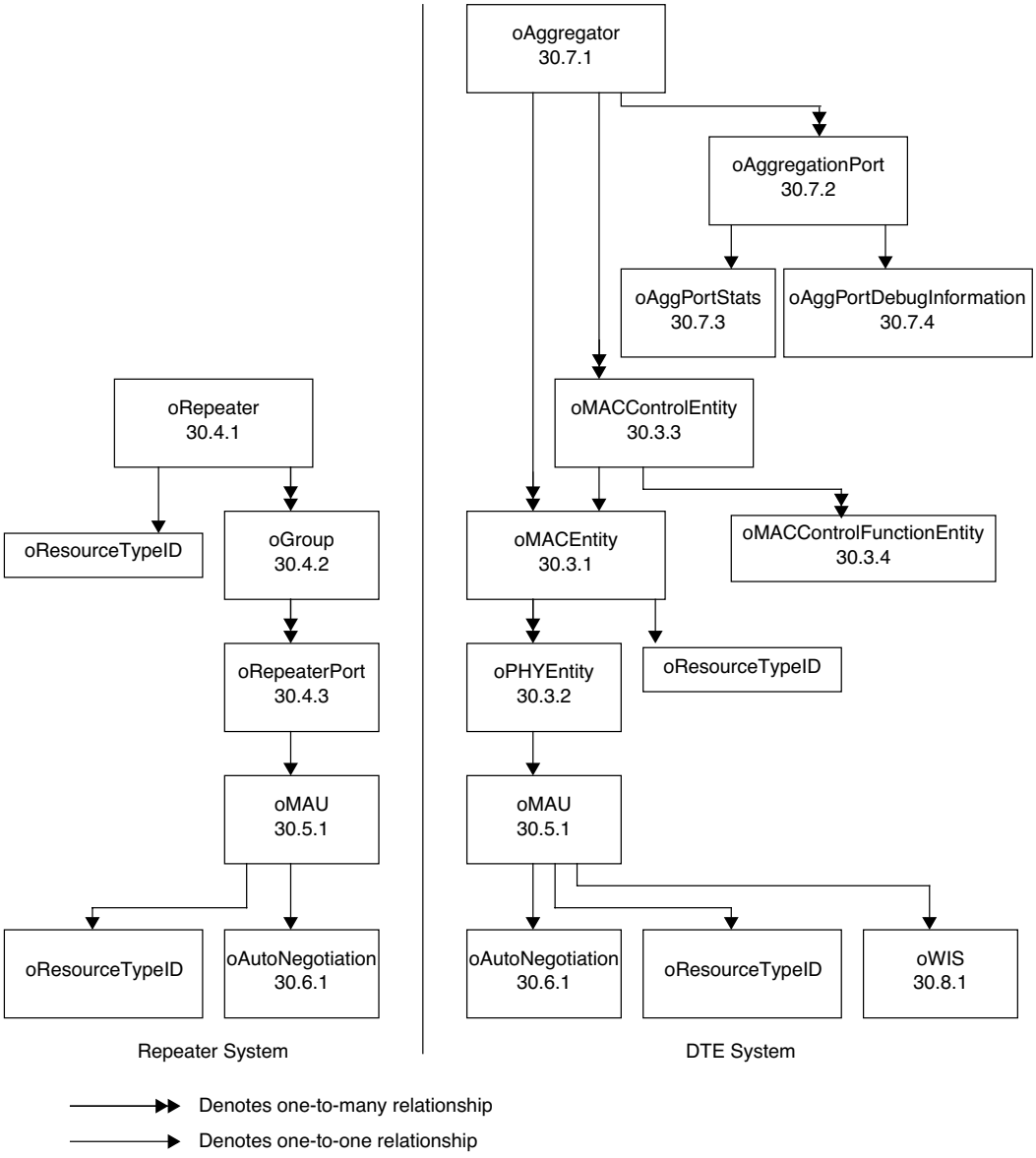


Figure 30–3—~~10/100/1000 Mb/s MAC, Control, and Link Aggregation e~~Entity relationship diagram

30.2.5 Capabilities

Change the first paragraph of this subclause as follows:

This standard makes use of the concept of *packages* as defined in ISO/IEC 10165-4: 1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this

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standard *capabilities* are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate basic and mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 ~~10 Mb/s, 100 Mb/s, 1000 Mb/s, MAC Control, and Link Aggregation~~ Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 ~~10 Mb/s, 100 Mb/s, and 1000 Mb/s~~ Management are specified in Tables 30–1, 30–2 and 30–3~~.a, 30–1b, 30–1c, 30–1d, and 30–1e. The capabilities and packages for Link Aggregation Management are specified in Table 30–2.~~

In Tables 30–1a, 30–1b, 30–1c, 30–1d, and 30–1e, change the DTE and MAU column heading "100/1000 Mb/s Monitor Capability (Optional)" ***to read*** "PHY Error Monitor Capability (Optional)."

Insert the following entries to Table 30–1b after "aDuplexStatus."

				DTE								Repeater				MAU						
				Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	100/1000 Mb/s Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	PHY Error Monitor Capability (Optional)	Auto-Negotiation Package (Mandatory)
	aRateControlAbility	ATTRIBUTE	GET		X																		
	aRateControlStatus	ATTRIBUTE	GET-SET		X																		

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Insert the following new table after Table 30–2

Table 30–3—WIS Capabilities

				WIS Basic Package (Mandatory)	WIS Recommended Package (Optional)
oWIS managed object class (30.8.1)					
	aWISID	ATTRIBUTE	GET	X	
	aSectionStatus	ATTRIBUTE	GET	X	
	aSectionSESThreshold	ATTRIBUTE	GET-SET		X
	aSectionSESs	ATTRIBUTE	GET		X
	aSectionESs	ATTRIBUTE	GET		X
	aSectionSEFSs	ATTRIBUTE	GET		X
	aSectionCVs	ATTRIBUTE	GET		X
	aJ0ValueTX	ATTRIBUTE	GET-SET		X
	aJ0ValueRX	ATTRIBUTE	GET		X
	aLineStatus	ATTRIBUTE	GET	X	
	aLineSESThreshold	ATTRIBUTE	GET-SET		X
	aLineSESs	ATTRIBUTE	GET		X
	aLineESs	ATTRIBUTE	GET		X
	aLineCVs	ATTRIBUTE	GET		X
	aFarEndLineSESs	ATTRIBUTE	GET		X
	aFarEndLineESs	ATTRIBUTE	GET		X
	aFarEndLineCVs	ATTRIBUTE	GET		X
	aPathStatus	ATTRIBUTE	GET	X	
	aPathSESThreshold	ATTRIBUTE	GET-SET		X
	aPathSESs	ATTRIBUTE	GET		X
	aPathESs	ATTRIBUTE	GET		X
	aPathCVs	ATTRIBUTE	GET		X
	aJ1ValueTX	ATTRIBUTE	GET-SET		X
	aJ1ValueRX	ATTRIBUTE	GET		X
	aFarEndPathStatus	ATTRIBUTE	GET	X	
	aFarEndPathSESs	ATTRIBUTE	GET		X
	aFarEndPathESs	ATTRIBUTE	GET		X
	aFarEndPathCVs	ATTRIBUTE	GET		X
Common Attributes Template					
	aCMCounter	ATTRIBUTE	GET		X

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30.3.1.1.7 aAlignmentErrors

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3). This counter will not increment for group encoding schemes encoding greater than 4 bits per group ~~8 bit wide group encoding schemes~~.;

30.3.1.1.31 aMACCapabilities

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

half duplex	Capable of operating in half duplex mode
full duplex	Capable of operating in full duplex mode

BEHAVIOUR DEFINED AS:

This indicates the duplex capabilities of the MAC.;

Insert the following text immediately following aDuplexStatus

30.3.1.1.33 aRateControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

“True” for operating speeds above 1000 Mb/s where Rate Control through lowering the average data rate of the MAC sublayer, with frame granularity, is supported (see 4.2.3.2.2), and “false” otherwise.;

30.3.1.1.34 aRateControlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

rate control off	Rate control mode disabled
rate control on	Rate control mode enabled
unknown	Rate control mode unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current Rate Control mode of operation of the MAC sublayer.

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A SET operation changes the mode of operation of the MAC sublayer to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.

This attribute maps to the variable ifsStretchMode (see 4.2.7.2).;

30.3.1.2.4 acExecuteSelfTest

Change this subclause as follows:

ACTION

APPROPRIATE SYNTAX:
None required

BEHAVIOUR DEFINED AS:
Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard. If PHY loopback is accessible through a Clause 22 MII, Clause 35 GMII, or Clause 45 MDIO interface, ~~a Clause 22 MII or Clause 35 GMII is present~~ then this action shall also invoke a data integrity test using ~~MII or GMII~~ PHY loopback, returning to normal operation on completion of the test. In the case of a Clause 45 MDIO Interface where multiple loopbacks are available, the loopback in the MMD closest to the MDI should be used.;

30.3.2.1.2 aPhyType

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
10 Mb/s	Clause 7 10 Mb/s Manchester
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS

BEHAVIOUR DEFINED AS:
A read-only value that identifies the PHY type. The enumeration of the type is such that the value matches the clause number of this International Standard that specifies the particular PHY. The value of this attribute maps to the value of aMAUType. The enumeration “none” can only occur in a standard implementation where an MII exists and there is nothing connected. However, the attribute aMIIDetect should be used to determine whether an MII exists or not.;

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30.3.2.1.3 aPhyTypeList

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
10 Mb/s	Clause 7 10 Mb/s Manchester
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS

BEHAVIOUR DEFINED AS:

A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28 or Clause 37, Auto-Negotiation, is present, then this attribute will map to the local technology ability or advertised ability of the local device.

NOTE—At 10 Gb/s the ability of the PMD must be taken into account when reporting the possible types that the PHY could be.;

30.3.2.1.5 aSymbolErrorDuringCarrier

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations.

BEHAVIOUR DEFINED AS:

For 100 Mb/s operation, it is a count of the number of times when valid carrier was present and there was at least one occurrence of an invalid data symbol (see 23.2.1.4, 24.2.2.1.6, and 32.3.4.1).

For half duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than slotTime (see 4.2.4), and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–2).

For full duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” on the GMII (see Table 35–2).

For operation at 10 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the XGMII (see Table 46-3).

At all speeds this counter shall be incremented only once per valid CarrierEvent and if a collision is present this counter shall not increment.;

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30.3.2.1.7 aPhyAdminState

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

A disabled PHY neither transmits nor receives. The PHY shall be explicitly enabled to restore operation. The acPhyAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across DTE reset including loss of power. Only one PHY per MAC can be enabled at any one time. Setting a PHY to the enabled state using the action acPhyAdminControl will result in all other instances of PHY (indicated by PhyID) instantiated within the same MAC to be disabled. If a Clause 22 MII or Clause 35 GMII is present then setting this attribute to "disabled" will result in electrical isolation as defined in 22.2.4.1.6, Isolate; and setting this attribute to "enabled" will result in normal operation as defined in 22.2.4.1.5, Power down; and 22.2.4.1.6, Isolate. For all MMDs that provide a Clause 45 MDIO Interface within the PHY, setting this attribute to "enabled" will result in the MMD Low-power bit being set for normal operation. MMDs that support Low Power are the PMA/PMD MMD (see 45.2.1.1.2 and 45.2.1.2.3), the WIS MMD (see 45.2.2.1.3 and 45.2.2.2.3), the PCS MMD (see 45.2.3.1.3 and 45.2.3.2.3), the PHY XS MMD (see 45.2.4.1.3 and 45.2.4.2.3) and the DTE XS MMD (see 45.2.5.1.3 and 45.2.5.2.3).;

30.5 Layer management for 10, 100, and 1000 Mb/s medium attachment units (MAUs)

Change the title of this clause as follows:

30.5 Layer management for 10 Mb/s, 100 Mb/s, ~~and~~ 1000 Mb/s and 10 Gb/s medium attachment units (MAUs)

30.5.1 MAU managed object class

Add the following additional paragraph at the end of this subclause:

The sublayer that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayers as a group. Therefore in this clause, the term MAU will include PMA and PMD sublayers, as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

30.5.1.1.2 aMAUType

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A GET-SET ENUMERATION that meets the requirements of the following description ~~below~~:
global undefined

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other	See 30.2.5.
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
10BASE5	Thick coax MAU as specified in Clause 8
FOIRL	FOIRL MAU as specified in 9.9
10BASE2	Thin coax MAU as specified in Clause 10
10BROAD36	Broadband DTE MAU as specified in Clause 11
10BASE-T	UTP MAU as specified in Clause 14, duplex mode unknown
10BASE-THD	UTP MAU as specified in Clause 14, half duplex mode
10BASE-TFD	UTP MAU as specified in Clause 14, full duplex mode
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-FB	Synchronous fiber MAU as specified in Clause 17
10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
100BASE-T4	Four-pair Category 3 UTP as specified in Clause 23
100BASE-TX	Two-pair Category 5 UTP as specified in Clause 25, duplex mode unknown
100BASE-TXHD	Two-pair Category 5 UTP as specified in Clause 25, half duplex mode
100BASE-TXFD	Two-pair Category 5 UTP as specified in Clause 25, full duplex mode
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-T2	Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown
100BASE-T2HD	Two-pair Category 3 UTP as specified in Clause 32, half duplex mode
100BASE-T2FD	Two-pair Category 3 UTP as specified in Clause 32, full duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD, half duplex mode
1000BASE-XFD	X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-LX	X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD	X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFD	X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SX	X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD	X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD	X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode
1000BASE-CXFD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-T	Four-pair Category 5 UTP PHY to be specified in Clause 40, duplex mode unknown
1000BASE-THD	Four-pair Category 5 UTP PHY to be specified in Clause 40, half duplex mode
1000BASE-TFD	Four-pair Category 5 UTP PHY to be specified in Clause 40, full duplex mode
10GBASE-X	X PCS/PMA as specified in Clause 48 over undefined PMD
10GBASE-LX4	X fibre over 4 lane 1310nm optics as specified in Clause 53
10GBASE-R	R PCS/PMA as specified in Clause 49 over undefined PMD

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10GBASE-ER	R fibre over 1550nm optics as specified in Clause 52
10GBASE-LR	R fibre over 1310nm optics as specified in Clause 52
10GBASE-SR	R fibre over 850nm optics as specified in Clause 52
10GBASE-W	W PCS/PMA as specified in Clauses 49 and 50 over undefined PMD
10GBASE-EW	W fibre over 1550nm optics as specified in Clause 52
10GBASE-LW	W fibre over 1310nm optics as specified in Clause 52
10GBASE-SW	W fibre over 850nm optics as specified in Clause 52
802.9a	Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T

BEHAVIOUR DEFINED AS:

Returns a value that identifies the ~~10 Mb/s, 100 Mb/s, or 1000 Mb/s~~ internal MAU type. If an AUI is to be identified to access an external MAU, the type "AUI" is returned. A SET operation to one of the possible enumerations indicated by aMAUTypeList will force the MAU into the new operating mode. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the mode force bits specified in 22.2.4.1. If a Clause 45 MDIO Interface is present, then this will map to the PCS type selection bit(s) in the 10G WIS Control 2 register specified in 45.2.2.6.6 and in the 10G PCS Control 2 register specified in 45.2.3.6.1 and to the PMA/PMD type selection bits in the 10G PMA/PMD Control 2 register specified in 45.2.1.6.1. If Clause 28 or Clause 37 Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

The enumerations 1000BASE-X, 1000BASE-XHD, ~~and~~ 1000BASE-XFD, 10GBASE-X, 10GBASE-R, and 10GBASE-W shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
available	link or light normal, loopback normal
not available	link loss or low light, no loopback
remote fault	remote fault with no detail
invalid signal	invalid signal, applies only to 10BASE-FB
remote jabber	remote fault, reason known to be jabber
remote link loss	remote fault, reason known to be far-end link loss
remote test	remote fault, reason known to be test
offline	offline, applies only to Clause 37 Auto-Negotiation
auto neg error	Auto-Negotiation Error, applies only to Clause 37 Auto-Negotiation
PMD link fault	PMD/PMA receive link fault
WIS frame loss	WIS loss of frame, applies only to 10GBASE-W
WIS signal loss	WIS loss of signal, applies only to 10GBASE-W
PCS link fault	PCS receive link fault
excessive BER	PCS Bit Error Rate monitor reporting excessive error rate
DXS link fault	DTE XGXS receive link fault, applies only to XAUI
PXS link fault	PHY XGXS transmit link fault, applies only to XAUI

BEHAVIOUR DEFINED AS:

If the MAU is a 10 Mb/s link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI, 10BASE2, 10BASE5, or 10BROAD36 MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

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At power-up or following a reset, the value of this attribute will be "unknown" for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, 10BASE2, 10BASE5, 10BROAD36, and 10BASE-FP MAUs.
For 100BASE-T2, 100BASE-T4, 100BASE-TX, and 100BASE-FX the enumerations match the states within the respective link integrity state diagrams, Figure 32–17, Figure 23–12, and Figure 24–15. Any MAU that implements management of Clause 28 Auto-Negotiation will map remote fault indication to MediaAvailable "remote fault." Any MAU that implements management of Clause 37 Auto-Negotiation will map the received RF1 and RF2 bits as specified in Table 37–2, as follows. Offline maps to the enumeration "offline," Link_Failure maps to the enumeration "remote fault" and Auto-Negotiation Error maps to the enumeration "auto neg error."
The enumeration "remote fault" applies to 10BASE-FB remote fault indication, the 100BASE-X far-end fault indication and nonspecified remote faults from a system running Clause 28 Auto-Negotiation. The enumerations "remote jabber," "remote link loss," or "remote test" should be used instead of "remote fault" where the reason for remote fault is identified in the remote signaling protocol.
Where a Clause 22 MII or Clause 35 GMII is present, a logic one in the remote fault bit (22.2.4.2.11) maps to the enumeration "remote fault," a logic zero in the link status bit (22.2.4.2.13) maps to the enumeration "not available." The enumeration "not available" takes precedence over "remote fault."
For 10 Gb/s, the enumerations map to the value of the link_fault variable within the Link Fault Signaling state diagram (Figure 46–9) as follows: the value OK maps to the enumeration "available," the value Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault." The enumeration "PMD link fault," "WIS frame loss," "WIS signal loss," "PCS link fault," "excessive BER," or "DXS link fault" should be used instead of the enumeration "not available" where the reason for the Local Fault state can be identified through the use of the Clause 45 MDIO Interface. Where multiple reasons for the Local Fault state can be identified only the highest precedence error should be reported. This precedence in descending order is as follows: "PXS link fault," "PMD link fault," "WIS frame loss," "WIS signal loss," "PCS link fault," "excessive BER," "DXS link fault."
Where a Clause 45 MDIO interface is present, a logic zero in the PMA/PMD Receive link status bit (45.2.1.2.2) maps to the enumeration "PMD link fault," a logic one in the LOF status bit (45.2.2.10.4) maps to the enumeration "WIS frame loss," a logic one in the LOS status bit (45.2.2.10.5) maps to the enumeration "WIS signal loss," a logic zero in the PCS Receive link status bit (45.2.3.2.2) maps to the enumeration "PCS link fault," a logic one in the 10GBASE-R PCS Latched high BER status bit (45.2.3.12.2) maps to the enumeration "excessive BER," a logic zero in the DTE XS receive link status bit (45.2.5.2.2) maps to the enumeration "DXS link fault," a logic zero in the PHY XS transmit link status bit (45.2.4.2.2) maps to the enumeration "PXS link fault."

30.5.1.1.6 aJabber

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two indications. The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
normal	state is true or normal

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fault state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresettable counter. This counter has a maximum increment rate of 40 counts per second.

BEHAVIOUR DEFINED AS:

If the MAU is in the JABBER state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI. Note that this counter will not increment for a 100 Mb/s, ~~or~~ 1000 Mb/s or 10 Gb/s PHY, as there is no defined JABBER state.;

Add the following subclauses after subclause 30.7.4.1.13:

30.8 Management for WAN Interface Sublayer (WIS)

30.8.1 WIS managed object class

This subclause formally defines the behaviours for the oWIS managed object class and attributes.

30.8.1.1 WIS attributes

The attributes in 30.8.1.1.1 through 30.8.1.1.28 may be used, possibly in conjunction with other attributes, to derive various system performance monitoring parameters and information.

30.8.1.1.1 aWISID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aWISID is assigned so as to uniquely identify a WIS among the subordinate managed objects of the containing object.;

30.8.1.1.2 aSectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A string of 2 bits corresponding to the Section Status (50.3.2.5). The first bit corresponds to the Loss of Signal flag and maps to the LOS bit in the WIS Status 3 register. The second bit corresponds to the Loss of Frame flag and maps to the LOF bit in the WIS Status 3 register. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10.;

30.8.1.1.3 aSectionSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value for *x* for Section SES definition (30.8.1.1.4). A SET operation

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changes the value for *x* for Section SES definition. After reset (or power-off, power-on cycle), *x* for Section SES returns to the default value 8554.

NOTE—8554 is selected to reflect the number of Section BIP-8 Errors that would occur with a random bit error rate of 1×10^{-6} (see Annex 50A).;

30.8.1.1.4 aSectionSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1, where *x* is the Section SES threshold defined by aSectionSESThreshold (30.8.1.1.3).;

30.8.1.1.5 aSectionESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1.;

30.8.1.1.6 aSectionSEFSs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Framing Second" (SEFS), i.e., a second containing one or more SEF events (50.3.2.5).;

30.8.1.1.7 aSectionCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 64 000 counts per second.

BEHAVIOUR DEFINED AS:

For every received B1 octet, increment counter by the number of detected Section BIP-8 Errors (50.3.2.5).;

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30.8.1.1.8 aJ0ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 15

BEHAVIOUR DEFINED AS:
An 16 octet value defining the transmitter's Section Trace message as defined in 50.3.2.3. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Section Trace message value. A GET operation returns the current Section Trace message value. The default transmitter's Section Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 transmit registers specified in 45.2.2.18.;

30.8.1.1.9 aJ0ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 15

BEHAVIOUR DEFINED AS:
An 16 octet value indicating the received Section Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 receive registers specified in 45.2.2.19.;

30.8.1.1.10 aLineStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A string of 2 bits reflecting the Line status (50.3.2.5). The first bit corresponds to the Line Alarm Indication Signal flag and maps to the AIS-L bit. The second bit corresponds to the Line Remote Defect Indication flag and maps to the RDI-L bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.11 aLineSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET operation returns the value for *x* for Line SES definition (30.8.1.1.12). A SET operation changes the value for x for Line SES definition. After WIS reset (or power-off, power-on cycle), *x* for Line SES returns to the default value 9835.;

NOTE—9835 is selected to reflect the number of Line BIP Errors that would occur with a random bit error rate of 1×10^{-6} (see Annex 50A).;

30.8.1.1.12 aLineSESs

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

30.8.1.1.13 aLineESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1.;

30.8.1.1.14 aLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 12 288 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:

For every received WIS frame (50.3.2), increment counter by the number of detected Line BIP Errors (50.3.2.5).;

30.8.1.1.15 aFarEndLineSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 count second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

30.8.1.1.16 aFarEndLineESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1.;

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30.8.1.1.17 aFarEndLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresetable counter. This counter has a maximum increment rate of 2 040 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:
For every received WIS frame (50.3.2), increment counter by the number of reported Far End Line BIP Errors (50.3.2.5).;

30.8.1.1.18 aPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (4)]

BEHAVIOUR DEFINED AS:
A string of 4 bits corresponding to the Path Status (50.3.2.5). The first bit corresponds to the Loss of Pointer flag and maps to the LOP-P bit, the second bit corresponds to the Alarm Indication Signal and maps to the AIS-P bit, the third bit corresponds to the Path Label Mismatch flag and maps to the PLM-P bit and the fourth bit corresponds to the Path Loss of Cell Delineation flag and maps to the LCD-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.19 aPathSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET operation returns the value for *x* for Path SES definition (30.8.1.1.20). A SET operation changes the value for *x* for Path SES definition. After reset (or power-off, power-on cycle), *x* for Path SES is set to the default value 2400.

NOTE—2400 is selected to reflect the point where 30% of all SPEs have a Path Block Error (see Annex 50A).;

30.8.1.1.20 aPathSESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a “Severely Errored Second” (SES), i.e., a second that had *x* or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1, where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

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30.8.1.1.21 aPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in an Errored Second (ES), i.e., a second that had one or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1.;

30.8.1.1.22 aPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:
Increment counter by one for every received B3 indicating a Path Block Error (Annex 50A).;

30.8.1.1.23 aJ1ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 15

BEHAVIOUR DEFINED AS:
An 16 octet value defining the transmitter's Path Trace message as defined in 50.3.2.1. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Path Trace message value. A GET operation returns the current Path Trace message value. The default transmitter's Path Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 transmit registers specified in 45.2.2.12.;

30.8.1.1.24 aJ1ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 15

BEHAVIOUR DEFINED AS:
An 16 octet value indicating the received Path Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 receive registers specified in 45.2.2.13.;

30.8.1.1.25 aFarEndPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

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BEHAVIOUR DEFINED AS:

A string of 2 bits corresponding to the Far End Path Status (50.3.2.5). The first bit corresponds to the Far End Path Label Mismatch/Path Loss of Cell Delineation flag and maps to the Far End PLM-P/LCD-P bit, and the second bit corresponds to the Far End Path Alarm Indication Signal/Path Loss of Pointer flag and maps to the Far End AIS-P/LOP-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.26 aFarEndPathSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a “Severely Errored Second” (SES), i.e., a second that had *x* or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/LCD-P, AIS-P, and LOP-P bits (50.3.2.5), where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

30.8.1.1.27 aFarEndPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an “Errored Second” (ES), i.e., a second that had one or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/LCD-P, AIS-P, and LOP-P bits (50.3.2.5).;

30.8.1.1.28 aFarEndPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for each received G1 octet indicating a Far End Path Block Error reported in REI-P (50.3.2.5).;

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31. MAC Control

31.3 Support by interlayer interfaces

Delete the note in 31.3 as follows:

~~NOTE—In the absence of the MAC Control sublayer, Clause 31 makes no attempt to reconcile the long-standing inconsistencies between the interface definitions in subclauses 4.3.2 and 2.3. These existing inconsistencies have not historically hampered the construction of interoperable networking equipments, and are not sufficiently important to merit further attention.~~

31.5.1 Frame parsing and data frame reception

Change 31.5.1 to read as follows:

Upon receipt, the MAC Control sublayer parses the incoming frame to determine whether it is destined for the MAC client (Data frame) or for a specific function within the MAC Control sublayer entity itself (MAC Control frame). MAC Control frames with a length of minFrameSize and a supported opcode field are interpreted and acted upon by the MAC Control sublayer.

A frame that does not contain the unique Length/Type field specified in 31.4.1.3 is a Data frame. The receipt of a Data frame results in the generation of an MA_DATA.indication primitive by the MAC Control sublayer, with the following parameters:

a) The destination_address parameter is set equal to the destinationParam from the ReceiveFrame function.
b) The source_address parameter is set equal to the sourceParam from the ReceiveFrame function.
c) The ~~m_sdu~~ mac_service_data_unit parameter is set equal to the concatenation of the lengthOrTypeParam and the dataParam from the ReceiveFrame function.
d) ~~The reception_status parameter is set equal to the ReceiveStatus from the ReceiveFrame function.~~ The frame_check_sequence parameter is equal to fcsParamValue from the ReceiveFrame function if fcsParamPresent from the ReceiveFrame function is true; otherwise, the frame_check_sequence parameter is not present.
e) The reception_status parameter is set equal to the ReceiveStatus from the ReceiveFrame function.

NOTE—For Length/Type field values in the range between maxValidLength and minTypeValue, the behavior of the RemovePad function in the underlying MAC sublayer is unspecified. Frames with Length/Type field values in this range may or may not be passed up by the MAC sublayer.

MAC Control frames with a length greater than minFrameSize and a supported opcode field may be either discarded, or truncated to minFrameSize, interpreted, and acted upon. Unsupported MAC Control frames are discarded. Discarded frames are neither ~~passed to the MAC client nor~~ interpreted nor acted upon by the MAC Control sublayer.

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35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

35.1 Overview

Replace Figure 35–1 with the following:

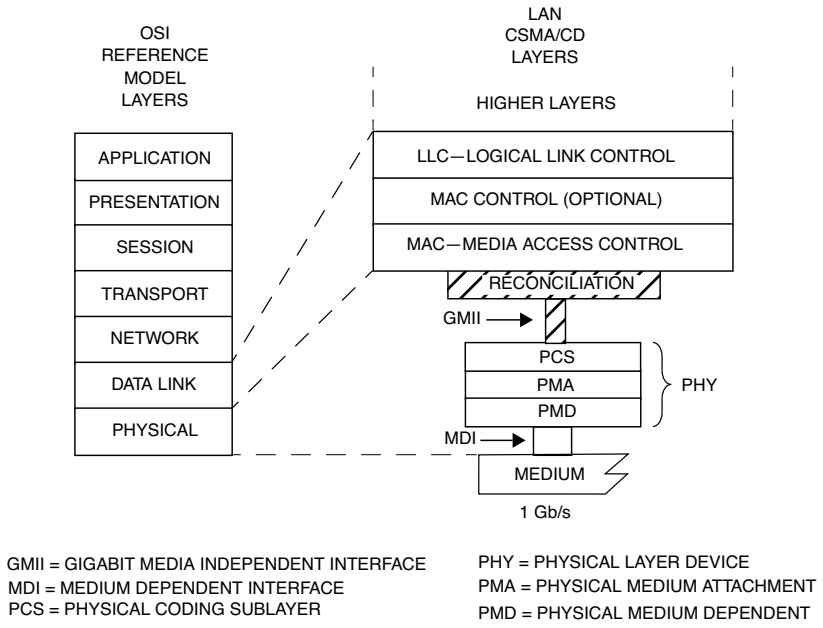


Figure 35–1—GMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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Annex 30A

(normative)

Change the entire Annex 30A and Annex 30B as follows:

GDMO specification for IEEE 802.3 managed object classes

This annex formally defines the protocol encodings for CMIP and ISO/IEC 15802-2: 1995 [ANSI/IEEE Std 802.1B and 802.1k, 1995 Edition] for the IEEE 802.3 Managed Objects using the templates specified in ISO/IEC 10165-4: 1992. The application of a GDMO template compiler against 30A.1 to ~~30A.8~~30A.15 will produce the proper protocol encodings.

NOTE 1—The arcs (that is, object identifier values) defined in Annex 30A deprecate the arcs previously defined in Annexes H.1 (Layer Management), H.2 (Repeater Management), and H.3 (MAU Management). See IEEE Std 802.1F-1993, Annex C.4.

NOTE 2—During the update for 1000 Mb/s operation differences between objects in the root of the registration arcs were harmonized. All instances of *{iso(1) std(0) iso8802(8802) csma(3)...* were changed to *{iso(1) member-body(2) us(840) ieee802dot3(10006)...* in order to harmonize with the rest of this GDMO specification. For maximum compatibility with previous implementations it is recommended that all implementations respond equally to requests for communication based on either registration arc.

Each attribute definition in this clause references directly by means of the WITH ATTRIBUTE SYNTAX construct or indirectly by means of the DERIVED FROM construct an ASN.1 type or subtype that defines the attribute's type and range. Those ASN.1 types and subtypes defined exclusively for CSMA/CD Management appear in a single ASN.1 module in 30B.1.

Counters for these protocol encodings are specified as either 32 or 64 bits wide. Thirty-two bit counters are used for the protocol encoding of counter attributes, providing the minimum rollover time is 58 min or more. Sixty-four bit counters are used for the protocol encoding of counter attributes that could roll over in less than 58 min with a 32-bit counter. Approximate counter rollover times are provided as notes below each counter BEHAVIOUR definition. 10 Gb/s counters are 10 times faster than 1000 Mb/s counters, 1000 Mb/s counters are 10 times faster than 100 Mb/s counters~~,~~ and 100 Mb/s counters are 10 times faster than 10 Mb/s counters. For formal definition of the counter, refer to the BEHAVIOUR bCMCounter in 30B.1.

30A.1 DTE MAC entity managed object class

30A.1.1 DTE MAC entity formal definition

oMACEntity	**MANAGED OBJECT CLASS**
DERIVED FROM	"CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY	
pBasic	PACKAGE
ATTRIBUTES	aMACID GET;
ACTIONS	acInitializeMAC;
;	
;	
CONDITIONAL PACKAGES	
pMandatory	PACKAGE

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	ATTRIBUTES	aFramesTransmittedOK	GET,
		aSingleCollisionFrames	GET,
		aMultipleCollisionFrames	GET,
		aFramesReceivedOK	GET,
		aFrameCheckSequenceErrors	GET,
		aAlignmentErrors	GET,
		aMACCapabilities	GET,
		aDuplexStatus	GET-~~SET~~REPLACE,
		aRateControlAbility	GET,
		aRateControlStatus	GET-REPLACE;
	REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) macMandatoryPkg(1)};	
	PRESENT IF	Conformance to DTE Management is desired. Attributes aMACCapabilities and aDuplexStatus are mandatory in systems that can operate in full duplex mode and are recommended in systems that can only operate in half duplex mode.~~;~~,	
pRecommended		PACKAGE	
	ATTRIBUTES	aOctetsTransmittedOK	GET,
		aFramesWithDeferredXmissions	GET,
		aLateCollisions	GET,
		aFramesAbortedDueToXSColls	GET,
		aFramesLostDueToIntMACXmitError	GET,
		aCarrierSenseErrors	GET,
		aOctetsReceivedOK	GET,
		aFramesLostDueToIntMACRcvError	GET,
		aPromiscuousStatus	GET-~~SET~~REPLACE,
		aReadMulticastAddressList	GET;
	ACTIONS	acAddGroupAddress, acDeleteGroupAddress;	
	REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) macRecommendedPkg(2)};	
	PRESENT IF	The Recommended Package is implemented.~~;~~,	
pOptional		PACKAGE	
	ATTRIBUTES	aMulticastFramesXmittedOK	GET,
		aBroadcastFramesXmittedOK	GET,
		aMulticastFramesReceivedOK	GET,
		aBroadcastFramesReceivedOK	GET,
		aInRangeLengthErrors	GET,
		aOutOfRangeLengthField	GET,
		aFrameTooLongErrors	GET,
		aMACEnableStatus	GET-~~SET~~REPLACE,
		aTransmitEnableStatus	GET-~~SET~~REPLACE,
		aMulticastReceiveStatus	GET-~~SET~~REPLACE,
		aReadWriteMACAddress	GET-~~SET~~REPLACE;
	ACTIONS	acExecuteSelfTest;	
	REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006)	

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csmacdmgt(30) package(4) optionalPkg(3)};
PRESENT IF The Optional Package and the Recommended Package are implemented.;,
pArray PACKAGE
ATTRIBUTES aCollisionFrames GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) arrayPkg(4)};
PRESENT IF The Array Package and the Recommended Package are implemented.;,
pExcessiveDeferral PACKAGE
ATTRIBUTES aFramesWithExcessiveDeferral GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) excessiveDeferralPkg(5)};
PRESENT IF The ExcessiveDeferral Package and the Recommended Package are implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) macObjectClass(1)};

nbMACName NAME BINDING

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) macName(1)};

nbMACMonitor NAME BINDING

SUBORDINATE OBJECT CLASS "IEEE802.1F":oEWMA~~ewma~~MetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE "IEEE802.1F":aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) macMonitor(2)};

nbMAC-MACControl NAME BINDING

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS oMACControlEntity;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMAC-MACControl(16)};

nbMAC-Aggregator NAME BINDING

SUBORDINATE OBJECT CLASS oMACEntity;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMAC-Aggregator(17)};

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30A.1.2 DTE MAC entity attributes

aMACID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMACID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) macID(1)};

bMACID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.1;

aFramesTransmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesTransmittedOK(2)};

bFramesTransmittedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.2;

NOTE 1—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

NOTE 2—This maps to framesSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aSingleCollisionFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSingleCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) singleCollisionFrames(3)};

bSingleCollisionFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.3;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 103 h.;

aMultipleCollisionFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bMultipleCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multipleCollisionFrames(4)};

bMultipleCollisionFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.4;

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NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 125 h.;

aFramesReceivedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesReceivedOK(5)};

bFramesReceivedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.5;

NOTE 1—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

NOTE 2—This maps to framesReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFrameCheckSequenceErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFrameCheckSequenceErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameCheckSequenceErrors(6)};

bFrameCheckSequenceErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.6;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aAlignmentErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) alignmentErrors(7)};

bAlignmentErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.7;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOctetsTransmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bOctetsTransmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) octetsTransmittedOK(8)};

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bOctetsTransmittedOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.8;

NOTE 1—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.

NOTE 2—This maps to octetsSent (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFramesWithDeferredXmissions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesWithDeferredXmissions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesWithDeferredXmissions(9)};

bFramesWithDeferredXmissions **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.9;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 103 h.;

aLateCollisions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bLateCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lateCollisions(10)};

bLateCollisions **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.10;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFramesAbortedDueToXSColls **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesAbortedDueToXSColls;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesAbortedDueToXSColls(11)};

bFramesAbortedDueToXSColls **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.11;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 53 days.;

aFramesLostDueToIntMACXmitError **ATTRIBUTE**

DERIVED FROM aCMCounter;

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SUPERSEDED

BEHAVIOUR bFramesLostDueToIntMACXmitError;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesLostDueToIntMACXmitError(12)};

bFramesLostDueToIntMACXmitError BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.12;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 16 h.;

aCarrierSenseErrors ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bCarrierSenseErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) carrierSenseErrors(13)};

bCarrierSenseErrors BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.13;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOctetsReceivedOK ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bOctetsReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) octetsReceivedOK(14)};

bOctetsReceivedOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.14;

NOTE 1—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.

NOTE 2—This maps to octetsReceived (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aFramesLostDueToIntMACRcvError ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesLostDueToIntMACRcvError;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesLostDueToIntMACRcvError(15)};

bFramesLostDueToIntMACRcvError BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.15;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

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aPromiscuousStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bPromiscuousStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) promiscuousStatus(16)};

bPromiscuousStatus **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.16;

aReadMulticastAddressList **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MulticastAddressList;
BEHAVIOUR bReadMulticastAddressList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readMulticastAddressList(17)};

bReadMulticastAddressList **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.17;

aMulticastFramesXmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bMulticastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastFramesXmittedOK(18)};

bMulticastFramesXmittedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.18;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aBroadcastFramesXmittedOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bBroadcastFramesXmittedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) broadcastFramesXmittedOK(19)};

bBroadcastFramesXmittedOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.19;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFramesWithExcessiveDeferral **ATTRIBUTE**

DERIVED FROM aCMCounter;

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BEHAVIOUR bFramesWithExcessiveDeferral;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesWithExcessiveDeferral(20)};

bFramesWithExcessiveDeferral BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.20;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 days.;

aMulticastFramesReceivedOK ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bMulticastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastFramesReceivedOK(21)};

bMulticastFramesReceivedOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.21;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aBroadcastFramesReceivedOK ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bBroadcastFramesReceivedOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) broadcastFramesReceivedOK(22)};

bBroadcastFramesReceivedOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.22;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aInRangeLengthErrors ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bInRangeLengthErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) inRangeLengthErrors(23)};

bInRangeLengthErrors BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.23;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aOutOfRangeLengthField ATTRIBUTE

DERIVED FROM aCMCounter;

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SUPERSEDED

BEHAVIOUR bOutOfRangeLengthField;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) outOfRangeLengthField(24)};

bOutOfRangeLengthField BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.24;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFrameTooLongErrors ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bFrameTooLongErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameTooLongErrors(25)};

bFrameTooLongErrors BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.25;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 61 days.;

aMACEnableStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMACEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mACEnableStatus(26)};

bMACEnableStatus BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.26;

aTransmitEnableStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bTransmitEnableStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) transmitEnableStatus(27)};

bTransmitEnableStatus BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.1.1.27;

aMulticastReceiveStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bMulticastReceiveStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) multicastReceiveStatus(28)};

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bMulticastReceiveStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.28;

aReadWriteMACAddress **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
BEHAVIOUR bReadWriteMACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) modifyMACAddress(29)};

bReadWriteMACAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.29;

NOTE—This maps to localMACAddress (of the mandatory macPackage) in ISO/IEC 10742: 1994.;

aCollisionFrames **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AttemptArray;
BEHAVIOUR bCollisionFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) collisionFrames(30)};

bCollisionFrames **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.30;

NOTE—The approximate minimum time for any single counter rollover for 10 Mb/s operation is 103 h.;

aMACCapabilities **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACCapabilitiesList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMACCapabilities;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACCapabilities(89)};

bMACCapabilities **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.31;

aDuplexStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DuplexValues;
MATCHES FOR EQUALITY;
BEHAVIOUR bDuplexStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aDuplexStatus(90)};

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bDuplexStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.32;

aRateControlAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TrueFalse;
BEHAVIOUR bRateControlAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) rateControlAbility(179)};

bRateControlAbility **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.33;

aRateControlStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RateValues;
MATCHES FOR EQUALITY;
BEHAVIOUR bRateControlStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) rateControlStatus(180)};

bRateControlStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.1.34;

30A.1.3 DTE MAC entity actions

acInitializeMAC **ACTION**

BEHAVIOUR bInitializeMAC;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) initializeMAC(1)};

bInitializeMAC **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.1;

acAddGroupAddress **ACTION**

BEHAVIOUR bAddGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) addGroupAddress(2)};

bAddGroupAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.2;

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SUPERSEDED

acDeleteGroupAddress **ACTION**

BEHAVIOUR bDeleteGroupAddress;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802CommonDefinitions.MACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) 802dot3(10006) csmacdmgt(30) action(9) deleteGroupAddress(3)};

bDeleteGroupAddress **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.3;

acExecuteSelfTest **ACTION**

BEHAVIOUR bExecuteSelfTestMAC;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) executeSelfTestMAC(4)};

bExecuteSelfTestMAC **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.1.2.4;

30A.2 DTE physical entity managed object class

30A.2.1 DTE physical entity formal definition

oPHYEntity MANAGED OBJECT CLASS

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;

CHARACTERIZED BY
pBasic PACKAGE
ATTRIBUTES aPHYID GET,
aPHYType GET,
aPHYTypeList GET,
aMIIDetect GET,
aPHYAdminState GET;
;
;
CONDITIONAL PACKAGES
pRecommended PACKAGE
ATTRIBUTES aSQETestErrors GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) phyRecommendedPkg(6)};
PRESENT IF The Recommended Package is implemented.;,
pMultiplePhy PACKAGE
ACTIONS acPHYAdminControl;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) phyMultiplePhyPkg(7)};

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SUPERSEDED

PRESENT IF There is more than one PHY per MAC.÷,
p100MbpsMonitor PACKAGE
ATTRIBUTES aSymbolErrorDuringCarrier GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) phy100MbpsMonitor(8)};
PRESENT IF The 100/1000 Mb/s Monitor capability is implemented.;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) phyObjectClass(2)};

nbPHYName NAME BINDING

SUBORDINATE OBJECT CLASS oPHYEntity;
NAMED BY SUPERIOR OBJECT CLASS oMACEntity;
WITH ATTRIBUTE aPHYID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) phyName(3)};

nbPHYMonitor NAME BINDING

SUBORDINATE OBJECT CLASS "IEEE802.1F":oEWMA~~ewma~~MetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE "IEEE802.1F":aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) phyMonitor(4)};

30A.2.2 DTE physical entity attributes

aPHYID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bPHYID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyID(31)};

bPHYID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.1;

aPHYType ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PhyTypeValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bPHYType;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyType(32)};

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SUPERSEDED

bPHYType **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.2;

aPHYTypeList **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PhyTypeList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPHYTypeList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyTypeList(33)};

bPHYTypeList **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.3;

aSQETestErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSQETestErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sqeTestErrors(34)};

bSQETestErrors **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.4~~;~~

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aSymbolErrorDuringCarrier **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSymbolErrorDuringCarrier;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) symbolErrorDuringCarrier(35)};

bSymbolErrorDuringCarrier **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.5~~;~~

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aMIIDetect ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MIIDetect;
MATCHES FOR EQUALITY;
BEHAVIOUR bMIIDetect;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mIIDetect(36)};

bMIIDetect **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.6;

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SUPERSEDED

aPHYAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPHYAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) phyAdminState(37)};

bPHYAdminState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.1.7;

30A.2.3 DTE physical entity actions

acPHYAdminControl **ACTION**

BEHAVIOUR bPHYAdminControl;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) phyAdminControl(5)};

bPHYAdminControl **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.2.2.1;

30A.3 DTE MAC control entity managed object class

30A.3.1 DTE MAC control entity formal definition

oMACControlEntity **MANAGED OBJECT CLASS**

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CHARACTERIZED BY
pMandatory PACKAGE
ATTRIBUTES aMACControlFunctionsSupported GET-~~SET~~REPLACE;
;
;
CONDITIONAL PACKAGES
pRecommended PACKAGE
ATTRIBUTES aMACControlFramesTransmitted GET,
aMACControlFramesReceived GET,
aUnsupportedOpcodesReceived GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
package(4) macControlRecommendedPkg(17)};
PRESENT IF The Recommended Package is implemented.;

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REGISTERED AS{iso(1) member-body(2) us(840) ieee802dot3(10006)
csmacdmgt(30)
managedObjectClass(3) macControlObjectClass(8)};

nbMACControl-System NAME BINDING

SUBORDINATE OBJECT CLASS oMACControlEntity;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMACControl-System(18)};

nbMACControl-Aggregator NAME BINDING

SUBORDINATE OBJECT CLASS oMACControlEntity;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbMACControl-Aggregator(19)};

nbMACControlMonitor NAME BINDING

SUBORDINATE OBJECT CLASS"IEEE802.1F":oEWMA~~ewma~~MetricMonitor;
NAMED BY SUPERIOR OBJECT CLASS
"ISO/IEC 10165-2":system;
WITH ATTRIBUTE "IEEE802.1F":aScannerId;
CREATE WITH-AUTOMATIC-INSTANCE-NAMING;
DELETE ONLY-IF-NO-CONTAINED-OBJECTS;
REGISTERED AS{iso(1) member-body(2) us(840) ieee802dot3(10006)
csmacdmgt(30) nameBinding(6) macControlMonitor(15)};

30A.3.2 DTE MAC Control entity attributes

aMACControlID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMACControlID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlID(92)};

bMACControlID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.3.1;

aMACControlFunctionsSupported ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
MACControlFunctionsList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMACControlFunctionsSupported;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFunctionsSupported(93)};

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bMACControlFunctionsSupported BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.3.2;

aMACControlFramesTransmitted ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~aCMCounter;
BEHAVIOUR bMACControlFramesTransmitted;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFramesTransmitted(94)};

bMACControlFramesTransmitted BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.3.3;

aMACControlFramesReceived ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~aCMCounter;
BEHAVIOUR bMACControlFramesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aMACControlFramesReceived(95)};

bMACControlFramesReceived BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.3.4;

aUnsupportedOpcodesReceived ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~aCMCounter;
BEHAVIOUR bUnsupportedOpcodesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aUnsupportedOpcodesReceived(96)};

bUnsupportedOpcodesReceived BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.3.3.5;

30A.4 DTE MAC Control function entity managed object class

30A.4.1 DTE MAC Control function entity formal definition

oMACControlFunctionEntityMANAGED OBJECT CLASS

DERIVED FROM“CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pMandatory PACKAGE
ATTRIBUTES aPAUSELinkDelayAllowance GET-~~SET~~REPLACE;
;
;
CONDITIONAL PACKAGES
pRecommended PACKAGE
ATTRIBUTES aPAUSEMACCtrlFramesTransmitted GET,
aPAUSEMACCtrlFramesReceived GET;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) macControlFunctionRecomendedPkg(2517)};
PRESENT IF The Recommended Package is implemented.;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3)macControlFunctionObjectClass(9)};

30A.4.2 DTE MAC Control function entity attributes

aPAUSELinkDelayAllowance ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.LinkDelayAllowance;
BEHAVIOUR bPAUSELinkDelayAllowance;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aPAUSELinkDelayAllowance(97)};

bPAUSELinkDelayAllowance BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.4.1;

aPAUSEMACCtrlFramesTransmitted ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~aCMCounter;
BEHAVIOUR bPAUSEMACCtrlFramesTransmitted;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aPAUSEMACCtrlFramesTransmitted(98)};

bPAUSEMACCtrlFramesTransmitted BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.4.2;

aPAUSEMACCtrlFramesReceived ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~aCMCounter;
BEHAVIOUR bPAUSEMACCtrlFramesReceived;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aPAUSEMACCtrlFramesReceived(99)};

bPAUSEMACCtrlFramesReceived BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.3.4.3;

30A.5 Repeater managed object class

30A.5.1 Repeater, formal definition

oRepeater MANAGED OBJECT CLASS

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 1992":top;

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SUPERSEDED


```
        pRepeaterBasicControl       PACKAGE
            ATTRIBUTES              aRepeaterID                 GET,
                                    aRepeaterType               GET,
                                    aRepeaterGroupCapacity      GET,
                                    aGroupMap                   GET,
                                    aRepeaterHealthState        GET,
                                    aRepeaterHealthText         GET,
                                    aRepeaterHealthData         GET;
            ACTIONS                 acResetRepeater,
                                    acExecuteNonDisruptiveSelfTest;
            NOTIFICATIONS           nRepeaterHealth,
                                    nRepeaterReset,
                                    nGroupMapChange;
        ;
    ;
    CONDITIONAL PACKAGES
        pRepeaterPerfMonitor        PACKAGE
            ATTRIBUTES              aTransmitCollisions         GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    repeaterPerfMonitorPkg(9)};
            PRESENT IF              The Performance Monitor Capability is implemented.;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        managedObjectClass(3) repeaterObjectClass(3)};

nbRepeaterName                      NAME BINDING

    SUBORDINATE OBJECT CLASS        oRepeater;
    NAMED BY SUPERIOR OBJECT CLASS
                                    "ISO/IEC 10165-2":system  AND SUBCLASSES;
    WITH ATTRIBUTE                  aRepeaterID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) repeaterName(5)};

nbRepeaterMonitor                   NAME BINDING

    SUBORDINATE OBJECT CLASS        "IEEE802.1F":oEWMAMetricMonitor;
    NAMED BY SUPERIOR OBJECT CLASS
                                    "ISO/IEC 10165-2":system  AND SUBCLASSES;
    WITH ATTRIBUTE                  "IEEE802.1F":aScannerId;
        CREATE                      WITH-AUTOMATIC-INSTANCE-NAMING;
        DELETE                      ONLY-IF-NO-CONTAINED-OBJECTS;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) repeaterMonitor(6)};
```

30A.5.2 Repeater attributes

```
aRepeaterID                         ATTRIBUTE

    WITH ATTRIBUTE SYNTAX           IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                     EQUALITY;
    BEHAVIOUR                       bRepeaterID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        attribute(7) repeaterID(38)};
```


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bRepeaterID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.1.;

aRepeaterType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterType;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterType;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterType (39)};

bRepeaterType **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.2.;

a**RepeaterGroupCapacity** **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bRepeaterGroupCapacity;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterGroupCapacity(40)};

bRepeaterGroupCapacity **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.3.;

aGroupMap **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bGroupMap;

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) groupMap(41)};

bGroupMap **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.4.;

aRepeaterHealthState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
RepeaterHealthState;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthState(42)};

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bRepeaterHealthState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.5.;

aRepeaterHealthText **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
RepeaterHealthText;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthText;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthText(43)};

bRepeaterHealthText **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.6.;

aRepeaterHealthData **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
RepeaterHealthData;
MATCHES FOR EQUALITY;
BEHAVIOUR bRepeaterHealthData;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) repeaterHealthData(44)};

bRepeaterHealthData **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.7.;

aTransmitCollisions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bTransmitCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) transmitCollisions (45)};

bTransmitCollisions **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.1.8.

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.;

30A.5.3 Repeater actions

acResetRepeater **ACTION**

BEHAVIOUR bResetRepeater;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) resetRepeater(6)};

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bResetRepeater **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.2.1.;

acExecuteNonDisruptiveSelfTest **ACTION**

BEHAVIOUR bExecuteNonDisruptiveSelfTest;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) executeNonDisruptiveSelfTestAction(7)};

bExecuteNonDisruptiveSelfTest **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.2.2.;

30A.5.4 Repeater notifications

nRepeaterHealth **NOTIFICATION**

BEHAVIOUR bRepeaterHealth;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthInfo
AND ATTRIBUTE IDS repeaterHealthState aRepeaterHealthState, repeaterHealthText aRepeaterHealthText, repeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) repeaterHealth(1)};

bRepeaterHealth **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.3.1.;

nRepeaterReset **NOTIFICATION**

BEHAVIOUR bRepeaterReset;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.RepeaterHealthInfo
AND ATTRIBUTE IDS repeaterHealthState aRepeaterHealthState, repeaterHealthText aRepeaterHealthText, repeaterHealthData aRepeaterHealthData
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) repeaterReset(2)};

bRepeaterReset **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.1.3.2.;

nGroupMapChange **NOTIFICATION**

BEHAVIOUR bGroupMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) groupMapChange(3)};

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bGroupMapChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.1.3.3.;

30A.6 Group managed object class

30A.6.1 Group, formal definition

```
oGroup                                  MANAGED OBJECT CLASS

    DERIVED FROM                        “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2
                                        1992”:top;
    CHARACTERIZED BY
        pGroupBasicControl              PACKAGE
            ATTRIBUTES                  aGroupID                GET,
                                        aGroupPortCapacity      GET,
                                        aPortMap                GET;
            NOTIFICATIONS               nPortMapChange;
        ;
    ;

    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        managedObjectClass(3) groupObjectClass(4)};

nbGroupName                             NAME BINDING

    SUBORDINATE OBJECT CLASS            oGroup;
    NAMED BY SUPERIOR OBJECT CLASS
                                        oRepeater  AND SUBCLASSES;
    WITH ATTRIBUTE                      aGroupID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) groupName(7)};
```

30A.6.2 Group attributes

aGroupID **ATTRIBUTE**

```
    WITH ATTRIBUTE SYNTAX               IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                         EQUALITY;
    BEHAVIOUR                           bGroupID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        attribute(7) groupID(46)};
```

bGroupID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.2.1.1;

aGroupPortCapacity **ATTRIBUTE**

```
    WITH ATTRIBUTE SYNTAX               IEEE802Dot3-MgmtAttributeModule.OneOfName;
    MATCHES FOR                         EQUALITY, ORDERING;
    BEHAVIOUR                           bGroupPortCapacity;
```


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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) groupPortCapacity(47)};

bGroupPortCapacity BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.2.1.2;

aPortMap ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
MATCHES FOR EQUALITY;
BEHAVIOUR bPortMap;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portMap(48)};

bPortMap BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.2.1.3;

30A.6.3 Group notifications

nPortMapChange NOTIFICATION

BEHAVIOUR bPortMapChange;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.BitString;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) portMapChange(4)};

bPortMapChange BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.2.2.1;

30A.7 Repeater port managed object class

30A.7.1 Port, formal definition

```
oRepeaterPort                    MANAGED OBJECT CLASS

    DERIVED FROM                 "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2
                                 1992":top;
    CHARACTERIZED BY
        pPortBasicControl        PACKAGE
            ATTRIBUTES           aPortID                 GET,
                                 aPortAdminState         GET,
                                 aAutoPartitionState     GET;
            ACTIONS              acPortAdminControl;
        ;
    ;
    CONDITIONAL PACKAGES
        pPortPerfMonitor         PACKAGE
            ATTRIBUTES           aReadableFrames         GET,
                                 aReadableOctets         GET,
```

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SUPERSEDED


```
                                    aFrameCheckSequenceErrors   GET,
                                    aAlignmentErrors            GET,
                                    aFramesTooLong              GET,
                                    aShortEvents                GET,
                                    aRunts                      GET,
                                    aCollisions                 GET,
                                    aLateEvents                 GET,
                                    aVeryLongEvents             GET,
                                    aDataRateMismatches         GET,
                                    aAutoPartitions             GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    portPerfMonitorPkg(10)};
            PRESENT IF              The Performance Monitor Capability is
                                    implemented.÷,
        pPortAddrTracking           PACKAGE
            ATTRIBUTES              aLastSourceAddress          GET,
                                    aSourceAddressChanges       GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4) portAddrTrackPkg(11)};
            PRESENT IF              The Address Tracking and Performance Monitor
                                    capabilities are implemented.÷,
        p100MbpsMonitor             PACKAGE
            ATTRIBUTES              aIsolates                   GET,
                                    aSymbolErrorDuringPacket    GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    port100MbpsMonitor(12)};
            PRESENT IF              The 100/1000 Mb/s Monitor capability is
                                    implemented;÷,
        pBurst                      PACKAGE
            ATTRIBUTES              aBursts                     GET;
            REGISTERED AS           {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                    csmacdmgt(30) package(4)
                                    portBurst(18)};
            PRESENT IF              The 1000 Mb/s Burst Monitor capability is
                                    implemented;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        managedObjectClass(3) repeaterPortObjectClass(5)};

nbPortName                          NAME BINDING

    SUBORDINATE OBJECT CLASS        oRepeaterPort;
    NAMED BY SUPERIOR OBJECT CLASS
                                    oGroup  AND SUBCLASSES;
    WITH ATTRIBUTE                  aPortID;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) portName(8)};
```

30A.7.2 Port attributes

```
aPortID                             ATTRIBUTE

    WITH ATTRIBUTE SYNTAX           IEEE802Dot3-MgmtAttributeModule.OneOfName;
```


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SUPERSEDED

BEHAVIOUR bPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portID(49)};

bPortID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.1;

aPortAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
MATCHES FOR EQUALITY;
BEHAVIOUR bPortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) portAdminState(50)};

bPortAdminState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.2;

aAutoPartitionState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoPartitionState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoPartition;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoPartitionState(51)};

bAutoPartition **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.3;

aReadableFrames **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bReadableFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readableFrames(52)};

bReadableFrames **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.4~~;~~

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aReadableOctets **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bReadableOctets;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) readableOctets(53)};

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bReadableOctets **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.5;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 58 min.;

aFrameCheckSequenceErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFCSErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) frameCheckSequenceErrors(54)};

bFCSErrors **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.6;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aAlignmentErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAlignmentErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) alignmentErrors(55)};

bAlignmentErrors **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.7;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 80 h.;

aFramesTooLong **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bFramesTooLong;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) framesTooLong(56)};

bFramesTooLong **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.4.3.1.8;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 61 days.;

aShortEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bShortEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) shortEvents(57)};

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bShortEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.9;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 16 hours;

aRunts **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bRunts;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) runts(58)};

bRunts **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.10;

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.;

aCollisions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bCollisions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) collisions(59)};

bCollisions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.11;

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 16 h.;

aLateEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bLateEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lateEvents(60)};

bLateEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.12;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 81 h.;

aVeryLongEvents **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bVeryLongEvents;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) veryLongEvents(61)};

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bVeryLongEvents **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.13;

NOTE—The approximate minimum time between counter rollovers for 10 Mb/s operation is 198 days.;

aDataRateMismatches **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bDataRateMismatches;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) dataRateMismatches(62)};

bDataRateMismatches **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.14;

aAutoPartitions **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bAutoPartitions;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoPartitions(63)};

bAutoPartitions **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.15;

aIsolates **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bIsolates;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) isolates(64)};

bIsolates **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.16;

aSymbolErrorDuringPacket **ATTRIBUTE**

DERIVED FROM aCMCounter;
BEHAVIOUR bSymbolErrorDuringPacket;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) symbolErrorDuringPacket(65)};

bSymbolErrorDuringPacket **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.17;

aLastSourceAddress **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802CommonDefinitions.MACAddress;
MATCHES FOR EQUALITY;

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BEHAVIOUR bLastSourceAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lastSourceAddress(66)};

bLastSourceAddress BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.18;

aSourceAddressChanges ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bSourceAddressChanges;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sourceAddressChanges(67)};

bSourceAddressChanges BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.19~~;~~

NOTE—The approximate minimum time for counter rollover for 10 Mb/s operation is 81 h.;

aBursts ATTRIBUTE

DERIVED FROM aCMCounter;
BEHAVIOUR bBursts;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bursts(100)};

bBursts BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.1.20;

30A.7.3 Port actions

acPortAdminControl ACTION

BEHAVIOUR bPortAdminControl;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.PortAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) portAdminControl(8)};

bPortAdminControl BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.4.3.2.1;

30A.8 MAU managed object class

30A.8.1 MAU, formal definition

oMAU MANAGED OBJECT CLASS

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```
        DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 :
                                        1992":top;
        CHARACTERIZED BY
                pMAUBasic               PACKAGE
                        ATTRIBUTES      aMAUID                  GET,
                                        aMAUType                GET-
                                        SETREPLACE,
                                        aMAUTypeList            GET,
                                        aMediaAvailable         GET,
                                        aJabber                 GET,
                                        aMAUAdminState          GET;
                        NOTIFICATIONS   nJabber;
                ;
        ;
        CONDITIONAL PACKAGES
                pMAUControl             PACKAGE
                        ACTIONS         acResetMAU,
                                        acMAUAdminControl;
                        REGISTERED AS   {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30)
                                        package(4) mauControlPkg(13)};
                        PRESENT IF      The pMAUControl package is implemented.;
                pMediaLossTracking      PACKAGE
                        ATTRIBUTES      aLoseMediaCounter       GET;
                        REGISTERED AS   {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30)
                                        package(4) mediaLossTrackingPkg(14)};
                        PRESENT IF      MAU TypeValue = AUI or if the
                                        pMediaLossTracking package is implemented.;
                pBroadbandDTEMAU        PACKAGE
                        ATTRIBUTES      aBbMAUXmitRcvSplitType  GET,
                                        aBroadbandFrequencies   GET;
                        REGISTERED AS   {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30)
                                        package(4) broadbandMAUPkg(15)};
                        PRESENT IF      The MAU is of type 10BROAD36.;
                p100MbpsMonitor         PACKAGE
                        ATTRIBUTES      aFalseCarriers          GET,
                                        aIdleErrorCount         GET;
                        REGISTERED AS   {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30)
                                        package(4) mau100MbpsMonitor(16)};
                        PRESENT IF      The MAU is capable of 100 Mb/s operation.;
        REGISTERED AS                   {iso(1) member-body(2) us(840) ieee802dot3(10006)
                                        csmacdmgt(30)
                                        managedObjectClass(3) mauObjectClass(6)};

nbMAU-repeaterName                      NAME BINDING

        SUBORDINATE OBJECT CLASS        oMAU;
        NAMED BY SUPERIOR OBJECT CLASS
                                                --(of oRepeaterPort)
                                        oRepeaterPort   AND SUBCLASSES;
                                                --{1.2.840.10006.30.3.5}
        WITH ATTRIBUTE                  aMAUID;
```


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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) mau-repeaterName(9)};

nbMAU-dteName NAME BINDING

SUBORDINATE OBJECT CLASS oMAU;
NAMED BY SUPERIOR OBJECT CLASS --(of oPHYEntity)
oPHYEntity AND SUBCLASSES;
--{1.2.840.10006.30.3.2};
WITH ATTRIBUTE aMAUID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) mau-dteName(10)};

30A.8.2 MAU attributes

aMAUID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bMAUID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauID(68)};

bMAUID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.1.1;

aMAUType ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TypeValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMAUType;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauType(69)};

bMAUType BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.1.2;

aMAUTypeList ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.TypeList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bMAUTypeList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauTypeList(70)};

bMAUTypeList BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.1.3;

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aMediaAvailable **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.MediaAvailState;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bMediaAvailable;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauMediaAvailable(71)};

bMediaAvailable **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.4;

aLoseMediaCounter **ATTRIBUTE**

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~	IEEE802Dot3-~~MgmtAttributeModule.~~aCMCounter;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bLoseMediaCounter;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauLoseMediaCounter(72)};

bLoseMediaCounter **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.5;

aJabber **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.Jabber;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bJabberAttribute;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) jabber(73)};

bJabberAttribute **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.6;

aMAUAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.AdminState;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bMAUAdminState;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) mauAdminState(74)};

bMAUAdminState **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.5.1.1.7;

aBbMAUXmitRcvSplitType **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.BbandXmitRcvSplitType;

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MATCHES FOR EQUALITY;
BEHAVIOUR bBbMAUXmitRcvSplitType;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bBandSplitType(75)};

bBbMAUXmitRcvSplitType BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.8;

aBroadbandFrequencies ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.BbandFrequency;
MATCHES FOR EQUALITY;
BEHAVIOUR bBroadbandFrequencies;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) bBandFrequencies(76)};

bBroadbandFrequencies BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.9;

aFalseCarriers ATTRIBUTE

DERIVED FROM~~WITH ATTRIBUTE SYNTAX~~IEEE802Dot3-~~MgmtAttributeModule.~~aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFalseCarriers;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) falseCarriers(77)};

bFalseCarriers BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.10;

aIdleErrorCount ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RegisterEight;
BEHAVIOUR bIdleErrorCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) idleErrorCount(91)};

bIdleErrorCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.5.1.1.11;

30A.8.3 MAU actions

acResetMAU ACTION

BEHAVIOUR bResetMAU;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) resetMAU(9)};

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bResetMAU **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.2.1;

acMAUAdminControl **ACTION**

BEHAVIOUR bMAUAdminControl;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AdminState;
~~MODE~~ ~~CONFIRMED;~~
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) mauAdminCtrl(10)};

bMAUAdminControl **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.2.2;

30A.8.4 MAU notifications

nJabber **NOTIFICATION**

BEHAVIOUR bJabberNotification;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.Jabber;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) jabber(5)};

bJabberNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.5.1.3.1;

30A.9 AutoNegotiation managed object class

30A.9.1 AutoNegotiation, formal definition

oAutoNegotiation MANAGED OBJECT CLASS

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pAutoNeg PACKAGE
ATTRIBUTES aAutoNegID GET,
aAutoNegAdminState GET,
aAutoNegRemoteSignaling GET,
aAutoNegAutoConfig GET-~~SET~~REPLACE,
aAutoNegLocalTechnologyAbility GET,
aAutoNegAdvertisedTechnologyAbility GET-~~SET~~REPLACE,
aAutoNegReceivedTechnologyAbility GET,
aAutoNegLocalSelectorAbility GET,
aAutoNegAdvertisedSelectorAbility GET-~~SET~~REPLACE,

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```
                                    aAutoNegReceivedSelectorAbility     GET;
                        ACTIONS
                                    acAutoNegRestartAutoConfig,
                                    acAutoNegAdminControl;
                ;
        ;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            managedObjectClass(3) autoNegObjectClass(7)};

nbAutoNeg-mauName                   NAME BINDING

        SUBORDINATE OBJECT CLASS    oAutoNegotiation~~oMAU~~;
        NAMED BY SUPERIOR OBJECT CLASS          --(of oMAU)
                                    oMAU   AND SUBCLASSES;
                                                --{1.2.840.10006.30.3.6}
        WITH ATTRIBUTE              aMAUID;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            nameBinding(6) autoNeg-mauName(11)};
```

30A.9.2 Auto-Negotiation attributes

```
aAutoNegID                          ATTRIBUTE

        WITH ATTRIBUTE SYNTAX       IEEE802Dot3-MgmtAttributeModule.OneOfName;
        MATCHES FOR                 EQUALITY;
        BEHAVIOUR                   bAutoNegID;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            attribute(7) autoNegID(78)};

bAutoNegID                          BEHAVIOUR

        DEFINED AS          See “BEHAVIOUR DEFINED AS” in 30.6.1.1.1;

aAutoNegAdminState                  ATTRIBUTE

        WITH ATTRIBUTE SYNTAX       IEEE802Dot3-MgmtAttributeModule.
                                    AutoNegAdminState;
        MATCHES FOR                 EQUALITY;
        BEHAVIOUR                   bAutoNegAdminState;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                            attribute(7) autoNegAdminState(79)};

bAutoNegAdminState                  BEHAVIOUR

        DEFINED AS          See “BEHAVIOUR DEFINED AS” in 30.6.1.1.2;

aAutoNegRemoteSignaling             ATTRIBUTE

        WITH ATTRIBUTE SYNTAX       IEEE802Dot3-MgmtAttributeModule.
                                    AutoNegRemoteSignalingDetect;
        MATCHES FOR                 EQUALITY;
        BEHAVIOUR                   bAutoNegRemoteSignaling;
        REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
```

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attribute(7) autoNegRemoteSignaling(80)};

bAutoNegRemoteSignaling **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.3;

aAutoNegAutoConfig **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegAutoConfig;
MATCHES FOR EQUALITY;
BEHAVIOUR bAutoNegAutoConfig;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
attribute(7) autoNegAutoConfig(81)};

bAutoNegAutoConfig **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.4;

aAutoNegLocalTechnologyAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegLocalTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
attribute(7) autoNegLocalTechnologyAbility(82)};

bAutoNegLocalTechnologyAbility **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.5;

aAutoNegAdvertisedTechnologyAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegAdvertisedTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
attribute(7) autoNegAdvertisedTechnologyAbility(83)};

bAutoNegAdvertisedTechnologyAbility **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.6;

aAutoNegReceivedTechnologyAbility **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.
AutoNegTechnologyList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegReceivedTechnologyAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
attribute(7) autoNegReceivedTechnologyAbility(84)};

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bAutoNegReceivedTechnologyAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.7;

aAutoNegLocalSelectorAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegLocalSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegLocalSelectorAbility(85)};

bAutoNegLocalSelectorAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.8;

aAutoNegAdvertisedSelectorAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegAdvertisedSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegAdvertisedSelectorAbility(86)};

bAutoNegAdvertisedSelectorAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.9;

aAutoNegReceivedSelectorAbility ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegSelectorList;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAutoNegReceivedSelectorAbility;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) autoNegReceivedSelectorAbility(87)};

bAutoNegReceivedSelectorAbility BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.1.10;

30A.9.3 AutoNegotiation actions

acAutoNegRestartAutoConfig ACTION

BEHAVIOUR bAutoNegRestartAutoConfig;
MODE CONFIRMED;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) autoNegRestartAutoConfig(11)};

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SUPERSEDED

bAutoNegRestartAutoConfig BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.2.1;

acAutoNegAdminControl ACTION

BEHAVIOUR bAutoNegAdminControl;
MODE CONFIRMED;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AutoNegAdminState;
~~MODE~~ ~~CONFIRMED;~~
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) action(9) autoNegAdminCtrl(12)};

bAutoNegAdminControl BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.6.1.2.2;

30A.10 ResourceTypeID managed object class

30A.10.1 ResourceTypeID, formal definition

— Implementation of this managed object in accordance with the definition contained in IEEE Std
— 802.1F-1993 is a conformance requirement of this standard.
— NOTE—A single instance of the Resource Type ID managed object exists within the oMACEntity
— managed object class, a single instance of the Resource Type ID managed object exists within
— the oRepeater managed object class, and a single instance of the Resource Type ID managed
— object exists within the oMAU managed object class conditional on the presence of an MII.
— The managed object itself is contained in IEEE Std 802.1F-1993, therefore only name bindings
— appear in this standard;

nbResourceTypeID-mac NAME BINDING

SUBORDINATE OBJECT CLASS “IEEE802.1F”:oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oMACEntity;
WITH ATTRIBUTE “IEEE802.1F”:aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-mac(12)};

nbResourceTypeID-repeater NAME BINDING

SUBORDINATE OBJECT CLASS “IEEE802.1F”:oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS
oRepeater AND SUBCLASSES;
WITH ATTRIBUTE “IEEE802.1F”:aResourceTypeIDName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) resourceTypeID-repeater(13)};

nbResourceTypeID-mau NAME BINDING

SUBORDINATE OBJECT CLASS “IEEE802.1F”:oResourceTypeID;
NAMED BY SUPERIOR OBJECT CLASS

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SUPERSEDED


```
                                    oMAU  AND SUBCLASSES;
    WITH ATTRIBUTE                  "IEEE802.1F":aResourceTypeIDName;
    REGISTERED AS       {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30)
                        nameBinding(6) resourceTypeID-mau(14)};
```

30A.11 Aggregator managed object class

30A.11.1 Aggregator, formal definition

```
oAggregator                         MANAGED OBJECT CLASS

    DERIVED FROM                    "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
    CHARACTERIZED BY
            pAggregatorBasic        PACKAGE
                    ATTRIBUTES      aAggID                              GET;
            ;
    ;
    CONDITIONAL PACKAGES
            pAggregatorMandatory    PACKAGE
                    ATTRIBUTES      aAggDescription                     GET,
                                    aAggName                            GET-REPLACE,
                                    aAggActorSystemID                   GET-REPLACE,
                                    aAggActorSystemPriority             GET-REPLACE,
                                    aAggAggregateOrIndividual           GET,
                                    aAggActorAdminKey                   GET-REPLACE,
                                    aAggActorOperKey                    GET,
                                    aAggMACAddress                      GET,
                                    aAggPartnerSystemID                 GET,
                                    aAggPartnerSystemPriority           GET,
                                    aAggPartnerOperKey                  GET,
                                    aAggAdminState                      GET-REPLACE,
                                    aAggOperState                       GET,
                                    aAggTimeOfLastOperChange            GET,
                                    aAggDataRate                        GET,
                                    aAggFramesTxOK                      GET,
                                    aAggFramesRxOK                      GET,
                                    aAggLinkUpDownNotificationEnable    GET-REPLACE,
                                    aAggCollectorMaxDelay               GET-REPLACE;
                    NOTIFICATIONS
                                    nAggLinkUpNotification,
                                    nAggLinkDownNotification;
                    REGISTERED AS
                                    {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacd-
                    mgt(30) package(4) pAggregatorMandatory(19)};
                    PRESENT IF      Conformance to Link Aggregation management is desired;,
            pAggregatorRecommendedPACKAGE
                    ATTRIBUTES      aAggOctetsTxOK                      GET,
                                    aAggOctetsRxOK                      GET,
                                    aAggFramesDiscardedOnTx             GET,
                                    aAggFramesDiscardedOnRx             GET,
                                    aAggFramesWithTxErrors              GET,
                                    aAggFramesWithRxErrors              GET,
```

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SUPERSEDED

aAggUnknownProtocolFrames GET,
aAggPortList GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacd-mgt(30) package(4) pAggregatorRecommended(20)};
PRESENT IF The recommended package is implemented;,
pAggregatorOptional PACKAGE
ATTRIBUTES aAggMulticastFramesTxOK GET,
aAggMulticastFramesRxOK GET,
aAggBroadcastFramesTxOK GET,
aAggBroadcastFramesRxOK GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacd-mgt(30) package(4) pAggregatorOptional(21)};
PRESENT IF The optional package is implemented;

;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) manage-dObjectClass(3) oAggregator(10)};

nbAggregatorName NAME BINDING

SUBORDINATE OBJECT CLASS oAggregator;
NAMED BY SUPERIOR OBJECT CLASS "ISO/IEC 10165-2":system;
WITH ATTRIBUTE aAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) name-Binding(6) nbAggregatorName(20)};

30A.11.2 Aggregator attributes

aAggID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggID(101)};

bAggID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.1;

aAggDescription ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggDescription;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggDescription(102)};

bAggDescription BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.2;

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SUPERSEDED

aAggName **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggName;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggName(103)};

bAggName **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.3;

aAggActorSystemID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggActorSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorSystemID(104)};

bAggActorSystemID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.4;

aAggActorSystemPriority **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggActorSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorSystemPriority(105)};

bAggActorSystemPriority **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.5;

aAggAggregateOrIndividual **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggOrInd;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggAggregateOrIndividual;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggAggregateOrIndividual(106)};

bAggAggregateOrIndividual **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.6;

aAggActorAdminKey **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggActorAdminKey;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorAdminKey(107)};

bAggActorAdminKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.7;

aAggActorOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggActorOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggActorOperKey(108)};

bAggActorOperKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.8;

aAggMACAddress ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMACAddress;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMACAddress(109)};

bAggMACAddress BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.9;

aAggPartnerSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPartnerSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerSystemID(110)};

bAggPartnerSystemID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.10;

aAggPartnerSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPartnerSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerSystemPriority(111)};

bAggPartnerSystemPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.11;

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SUPERSEDED

aAggPartnerOperKey **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPartnerOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPartnerOperKey(112)};

bAggPartnerOperKey **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.12;

aAggAdminState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggAdminState(113)};

bAggAdminState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.13;

aAggOperState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggOperState ;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOperState(114)};

bAggOperState **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.14;

aAggTimeOfLastOperChange **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.Integer32;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggTimeOfLastOperChange;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggTimeOfLastOperChange(115)};

bAggTimeOfLastOperChange **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.15;

aAggDataRate **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggDataRate;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggDataRate;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggDataRate(116)};

bAggDataRate **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.16;

aAggOctetsTxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggOctetsTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOctetsTxOK(117)};

bAggOctetsTxOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.17.

NOTE—This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s.;

aAggOctetsRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggOctetsRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggOctetsRxOK(118)};

bAggOctetsRxOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.18.

NOTE—This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s.;

aAggFramesTxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesTxOK(119)};

bAggFramesTxOK **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.19.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;

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SUPERSEDED

MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesRxOK(120)};

bAggFramesRxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.20.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggMulticastFramesTxOK ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMulticastFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMulticastFramesTxOK(121)};

bAggMulticastFramesTxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.21.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggMulticastFramesRxOK ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggMulticastFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggMulticastFramesRxOK(122)};

bAggMulticastFramesRxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.22.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggBroadcastFramesTxOK ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggBroadcastFramesTxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggBroadcastFramesTxOK(123)};

bAggBroadcastFramesTxOK BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.23.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

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SUPERSEDED

aAggBroadcastFramesRxOK **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggBroadcastFramesRxOK;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggBroadcastFramesRxOK(124)};

bAggBroadcastFramesRxOK **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.24.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesDiscardedOnTx **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesDiscardedOnTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesDiscardedOnTx(125)};

bAggFramesDiscardedOnTx **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.25.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesDiscardedOnRx **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesDiscardedOnRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesDiscardedOnRx(126)};

bAggFramesDiscardedOnRx **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.26.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesWithTxErrors **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesWithTxErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesWithTxErrors(127)};

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SUPERSEDED

bAggFramesWithTxErrors BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.27.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggFramesWithRxErrors ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggFramesWithRxErrors;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggFramesWithRxErrors(128)};

bAggFramesWithRxErrors BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.28.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggUnknownProtocolFrames ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggUnknownProtocolFrames;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggUnknownProtocolFrames(129)};

bAggUnknownProtocolFrames BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.29.

NOTE—This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s.;

aAggLinkUpDownNotificationEnable ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.NotificationEnable;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggLinkUpDownNotificationEnable;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggLinkUpDownNotificationEnable(130)};

bAggLinkUpDownNotificationEnable BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.1.1.31;

aAggPortList ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortList;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortList;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortList(131)};

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SUPERSEDED

bAggPortList **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.30;

aAggCollectorMaxDelay **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.CollectorMaxDelay;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggCollectorMaxDelay;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggCollectorMaxDelay(132)};

bAggCollectorMaxDelay **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.1.32;

30A.11.3 Aggregator notifications

nAggLinkUpNotification **NOTIFICATION**

BEHAVIOUR bAggLinkUpNotification;
WITH INFORMATION SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) nAggLinkUpNotification(6)};

bAggLinkUpNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.2.1;

nAggLinkDownNotification **NOTIFICATION**

BEHAVIOUR bAggLinkDownNotification;
WITH INFORMATION~~ATTRIBUTE~~ SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) notification(10) nAggLinkDownNotification(7)};

bAggLinkDownNotification **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.1.2.2;

30A.12 Aggregation Port managed object class

30A.12.1 Aggregation Port, formal definition

oAggregationPort **MANAGED OBJECT CLASS**

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CHARACTERIZED BY
pAggregationPortBasic PACKAGE
ATTRIBUTES aAggPortID GET;
;

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SUPERSEDED

;
CONDITIONAL PACKAGES
pAggregationPortMandatory PACKAGE

ATTRIBUTES	aAggPortActorSystemPriority	GET-REPLACE,
	aAggPortActorSystemID	GET,
	aAggPortActorAdminKey	GET-REPLACE,
	aAggPortActorOperKey	GET,
	aAggPortPartnerAdminSystemPriority	GET-REPLACE,
	aAggPortPartnerOperSystemPriority	GET,
	aAggPortPartnerAdminSystemID	GET-REPLACE,
	aAggPortPartnerOperSystemID	GET,
	aAggPortPartnerAdminKey	GET-REPLACE,
	aAggPortPartnerOperKey	GET,
	aAggPortSelectedAggID	GET,
	aAggPortAttachedAggID	GET,
	aAggPortActorPort	GET,
	aAggPortActorPortPriority	GET-REPLACE,
	aAggPortPartnerAdminPort	GET-REPLACE,
	aAggPortPartnerOperPort	GET,
	aAggPortPartnerAdminPortPriority	GET-REPLACE,
	aAggPortPartnerOperPortPriority	GET,
	aAggPortActorAdminState	GET-REPLACE,
	aAggPortActorOperState	GET,
	aAggPortPartnerAdminState	GET-REPLACE,
	aAggPortPartnerOperState	GET,
	aAggPortAggregateOrIndividual	GET;

REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggregationPortMandatory(22)};
PRESENT IF Conformance to Link Aggregation management is desired;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggregationPort(11)};

nbAggregationPort **NAME BINDING**

SUBORDINATE OBJECT CLASS oAggregationPort;
NAMED BY SUPERIOR OBJECT CLASS oAggregator;
WITH ATTRIBUTE aAggPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggregationPortName(21)};

30A.12.2 Aggregation Port attributes

aAggPortID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortID(133)};

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bAggPortID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.1;

aAggPortActorSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorSystemPriority(134)};

bAggPortActorSystemPriority BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.2;

aAggPortActorSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorSystemID(135)};

bAggPortActorSystemID BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.3;

aAggPortActorAdminKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorAdminKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorAdminKey(136)};

bAggPortActorAdminKey BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.4;

aAggPortActorOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorOperKey(137)};

bAggPortActorOperKey BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.5;

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SUPERSEDED

aAggPortPartnerAdminSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminSystemPriority(138)};

bAggPortPartnerAdminSystemPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.6;

aAggPortPartnerOperSystemPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperSystemPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperSystemPriority(139)};

bAggPortPartnerOperSystemPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.7;

aAggPortPartnerAdminSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminSystemID(140)};

bAggPortPartnerAdminSystemID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.8;

aAggPortPartnerOperSystemID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MACAddress;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR ~~b~~aAggPortPartnerOperSystemID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperSystemID(141)};

bAggPortPartnerOperSystemID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.9;

aAggPortPartnerAdminKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortPartnerAdminKey;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminKey(142)};

bAggPortPartnerAdminKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.10;

aAggPortPartnerOperKey ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.KeyValue;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortPartnerOperKey;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperKey(143)};

bAggPortPartnerOperKey BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.11;

aAggPortSelectedAggID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortSelectedAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortSelectedAggID(144)};

bAggPortSelectedAggID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.12;

aAggPortAttachedAggID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggID;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortAttachedAggID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortAttachedAggID(145)};

bAggPortAttachedAggID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.13;

aAggPortActorPort ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorPort;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorPort(146)};

bAggPortActorPort BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.14;

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SUPERSEDED

aAggPortActorPortPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortActorPortPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorPortPriority(147)};

bAggPortActorPortPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.15;

aAggPortPartnerAdminPort ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminPort;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminPort(148)};

bAggPortPartnerAdminPort BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.16;

aAggPortPartnerOperPort ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PortNumber;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperPort;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperPort(149)};

bAggPortPartnerOperPort BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.17;

aAggPortPartnerAdminPortPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminPortPriority;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminPortPriority(150)};

bAggPortPartnerAdminPortPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.18;

aAggPortPartnerOperPortPriority ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PriorityValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperPortPriority;

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REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperPortPriority(151)};

bAggPortPartnerOperPortPriority BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.19;

aAggPortActorAdminState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorAdminState(152)};

bAggPortActorAdminState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.20;

aAggPortActorOperState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortActorOperState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortActorOperState(153)};

bAggPortActorOperState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.21;

aAggPortPartnerAdminState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerAdminState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerAdminState(154)};

bAggPortPartnerAdminState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.22;

aAggPortPartnerOperState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortState;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortPartnerOperState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortPartnerOperState(155)};

bAggPortPartnerOperState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.2.1.23;

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aAggPortAggregateOrIndividual ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggOrInd;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortAggregateOrIndividual;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortAggregateOrIndividual(156)};

bAggPortAggregateOrIndividual BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.2.1.24;

30A.13 Aggregation Port Statistics managed object class

30A.13.1 Aggregation Port Statistics, formal definition

oAggPortStats MANAGED OBJECT CLASS

DERIVED FROM “CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;
CONDITIONAL PACKAGES
pAggPortStats PACKAGE
ATTRIBUTES aAggPortStatsID GET,
aAggPortStatsLACPDUsRx GET,
aAggPortStatsMarkerPDUsRx GET,
aAggPortStatsMarkerResponsePDUsRx GET,
aAggPortStatsUnknownRx GET,
aAggPortStatsIllegalRx GET,
aAggPortStatsLACPDUsTx GET,
aAggPortStatsMarkerPDUsTx GET,
aAggPortStatsMarkerResponsePDUsTx GET;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggPortStats(23)};
PRESENT IF The Aggregation Port Statistics package is supported;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggPortStats(12)};

nbAggPortStats NAME BINDING

SUBORDINATE OBJECT CLASS oAggPortStats;
NAMED BY SUPERIOR OBJECT CLASS oAggregationPort;
WITH ATTRIBUTE aAggPortStatsID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggPortStats(22)};

30A.13.2 Aggregation Port Statistics attributes

aAggPortStatsID ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;

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SUPERSEDED

MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortStatsID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsID(157)};

bAggPortStatsID BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.1;

aAggPortStatsLACPDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsLACPDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsLACPDUsRx(158)};

bAggPortStatsLACPDUsRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.2.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerPDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerPDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerPDUsRx(159)};

bAggPortStatsMarkerPDUsRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.3.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerResponsePDUsRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerResponsePDUsRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerResponsePDUsRx(160)};

bAggPortStatsMarkerResponsePDUsRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.4.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsUnknownRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsUnknownRx;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsUnknownRx(161)};

bAggPortStatsUnknownRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.5.

NOTE—This counter has a maximum increment rate of 50 counts per second at 10 Mb/s.;

aAggPortStatsIllegalRx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsIllegalRx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsIllegalRx(162)};

bAggPortStatsIllegalRx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.6.

NOTE—This counter has a maximum increment rate of 50 counts per second at 10 Mb/s.;

aAggPortStatsLACPDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsLACPDUsTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsLACPDUsTx(163)};

bAggPortStatsLACPDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.7.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerPDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerPDUsTx;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerPDUsTx(164)};

bAggPortStatsMarkerPDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.8.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

aAggPortStatsMarkerResponsePDUsTx ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortStatsMarkerResponsePDUsTx;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortStatsMarkerResponsePDUsTx(165)};

bAggPortStatsMarkerResponsePDUsTx BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.3.1.9.

NOTE—This counter has a maximum increment rate of 5 counts per second at 10 Mb/s.;

30A.14 Aggregation Port Debug Information managed object class

30A.14.1 Aggregation Port Debug Information, formal definition

oAggPortDebugInformation MANAGED OBJECT CLASS

DERIVED FROM "CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992":top;
CONDITIONAL PACKAGES
pLACPDebug PACKAGE
ATTRIBUTES
aAggPortDebugInformationID GET,
aAggPortDebugRxState GET,
aAggPortDebugLastRxTime GET,
aAggPortDebugMuxState GET,
aAggPortDebugMuxReason GET,
aAggPortDebugActorChurnState GET,
aAggPortDebugPartnerChurnState GET,
aAggPortDebugActorChurnCount GET,
aAggPortDebugPartnerChurnCount GET,
aAggPortDebugActorSyncTransitionCount GET,
aAggPortDebugPartnerSyncTransitionCount GET,
aAggPortDebugActorChangeCount GET,
aAggPortDebugPartnerChangeCount GET;
REGISTERED AS
{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) package(4) pAggPortDebugInformation(24)};
PRESENT IF The Aggregation Port Debug Information package is supported;
;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) managedObjectClass(3) oAggPortDebugInformation(13)};

nbAggPortDebugInformation NAME BINDING

SUBORDINATE OBJECT CLASS oAggPortDebugInformation;
NAMED BY SUPERIOR OBJECT CLASS oAggregationPort;
WITH ATTRIBUTE aAggPortDebugInformationID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) nameBinding(6) nbAggPortDebugInformation(23)};

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SUPERSEDED

30A.14.2 Aggregation Port Debug Information attributes

aAggPortDebugInformationID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.AggPortID;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugInformationID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugInformationID(166)};

bAggPortDebugInformationID **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.1;

aAggPortDebugRxState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.RxState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugRxState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugRxState(167)};

bAggPortDebugRxState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.2;

aAggPortDebugLastRxTime **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.Integer32;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugLastRxTime;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugLastRxTime(168)};

bAggPortDebugLastRxTime **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.3;

aAggPortDebugMuxState **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.MuxState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugMuxState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugMuxState(169)};

bAggPortDebugMuxState **BEHAVIOUR**

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.4;

aAggPortDebugMuxReason **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.DescriptionString;
MATCHES FOR EQUALITY;

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BEHAVIOUR bAggPortDebugMuxReason;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugMuxReason(170)};

bAggPortDebugMuxReason BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.5;

aAggPortDebugActorChurnState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.ChurnState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugActorChurnState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChurnState(171)};

bAggPortDebugActorChurnState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.6;

aAggPortDebugPartnerChurnState ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.ChurnState;
MATCHES FOR EQUALITY;
BEHAVIOUR bAggPortDebugPartnerChurnState;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChurnState(172)};

bAggPortDebugPartnerChurnState BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.7;

aAggPortDebugActorChurnCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorChurnCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChurnCount(173)};

bAggPortDebugActorChurnCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.8.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerChurnCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerChurnCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChurnCount(174)};

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bAggPortDebugPartnerChurnCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.9.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugActorSyncTransitionCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorSyncTransitionCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorSyncTransitionCount(175)};

bAggPortDebugActorSyncTransitionCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.10.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerSyncTransitionCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerSyncTransitionCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerSyncTransitionCount(176)};

bAggPortDebugPartnerSyncTransitionCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.11.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugActorChangeCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugActorChangeCount;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugActorChangeCount(177)};

bAggPortDebugActorChangeCount BEHAVIOUR

DEFINED AS See "BEHAVIOUR DEFINED AS" in 30.7.4.1.12.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

aAggPortDebugPartnerChangeCount ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bAggPortDebugPartnerChangeCount;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) aAggPortDebugPartnerChangeCount(178)};

bAggPortDebugPartnerChangeCount BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.7.4.1.13.

NOTE—This counter has a maximum increment rate of 5 counts per second.;

30A.15 WIS managed object class

30A.15.1 WIS, formal definition

oWIS		**MANAGED OBJECT CLASS**	
DERIVED FROM		“CCITT Rec. X.721 (1992) | ISO/IEC 10165-2 : 1992”:top;	
CHARACTERIZED BY			
	pWISBasic	PACKAGE	
	ATTRIBUTES	aWISID	GET,
		aSectionStatus	GET,
		aLineStatus	GET,
		aPathStatus	GET,
		aFarEndPathStatus	GET;
	;		
;			
CONDITIONAL PACKAGES			
	pWISOptional	PACKAGE	
	ATTRIBUTES	aSectionSESThreshold	GET-REPLACE,
		aSectionSESs	GET,
		aSectionESs	GET,
		aSectionSEFSs	GET,
		aSectionCVs	GET,
		aJ0ValueTX	GET-REPLACE,
		aJ0ValueRX	GET,
		aLineSESThreshold	GET-REPLACE,
		aLineSESs	GET,
		aLineESs	GET,
		aLineCVs	GET,
		aFarEndLineSESs	GET,
		aFarEndLineESs	GET,
		aFarEndLineCVs	GET,
		aPathSESThreshold	GET-REPLACE,
		aPathSESs	GET,
		aPathESs	GET,
		aPathCVs	GET,
		aJ1ValueTX	GET-REPLACE,
		aJ1ValueRX	GET,
		aFarEndPathSESs	GET,
		aFarEndPathESs	GET,
		aFarEndPathCVs	GET;
	REGISTERED AS		

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{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacd-mgt(30) package(4) wisOptionalPkg(26)};
PRESENT IF The optional package is implemented;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) manage-dObjectClass(3) wisObjectClass(14)};

nbWIS-mauName **NAME BINDING**

SUBORDINATE OBJECT CLASS oWIS;
NAMED BY SUPERIOR OBJECT CLASS oMAU AND SUBCLASSES;
WITH ATTRIBUTE aWISID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) name-Binding(6) wis-mauName(24)};

30A.15.2 WIS attributes

aWISID **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.OneOfName;
MATCHES FOR EQUALITY;
BEHAVIOUR bWISID;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) wisID(182)};

bWISID **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.1;

aSectionStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.SectionStatus;
MATCHES FOR EQUALITY;
BEHAVIOUR bSectionStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionStatus(182)};

bSectionStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.2;

aSectionSESThreshold **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.SESThreshold;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bSectionSESThreshold;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionSESThreshold(183)};

NOTE—This counter has a maximum increment rate of 1 count per second.;

bSectionSESThreshold **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.3;

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SUPERSEDED

aSectionSESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bSectionSESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionSESs(184)};

bSectionSESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.4

NOTE—This counter has a maximum increment rate of 1 count per second.;

aSectionESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bSectionESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionESs(185)};

bSectionESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.5;

aSectionSEFSs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bSectionSEFSs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionSEFSs(186)};

bSectionSEFSs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.6

NOTE—This counter has a maximum increment rate of 1 count per second.;

aSectionCVs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bSectionCVs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) sectionCVs(187)};

bSectionCVs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.7

NOTE—This counter has a maximum increment rate of 64 000 counts per second.;

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aJ0ValueTX **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.JValue;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bJ0ValueTX;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) j0ValueTX(188)};

bJ0ValueTX **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.8.1.1.8;

aJ0ValueRX **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.JValue;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bJ0ValueRX;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) j0ValueRX(189)};

bJ0ValueRX **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.8.1.1.9;

aLineStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.LineStatus;
MATCHES FOR	EQUALITY;
BEHAVIOUR	bLineStatus;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lineStatus(190)};

bLineStatus **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.8.1.1.10;

aLineSESThreshold **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX	IEEE802Dot3-MgmtAttributeModule.SESThreshold;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bLineSESThreshold;
REGISTERED AS	{iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lineSESThreshold(191)};

bLineSESThreshold **BEHAVIOUR**

DEFINED AS	See “BEHAVIOUR DEFINED AS” in 30.8.1.1.11;

aLineSESs **ATTRIBUTE**

DERIVED FROM	aCMCounter;
MATCHES FOR	EQUALITY, ORDERING;
BEHAVIOUR	bLineSESs;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lineSESs(192)};

bLineSESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.12

NOTE—This counter has a maximum increment rate of 1 count per second.;

aLineESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bLineESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lineESs(193)};

bLineESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.13

NOTE—This counter has a maximum increment rate of 1 count per second.;

aLineCVs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bLineCVs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) lineCVs(194)};

bLineCVs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.14

NOTE—This counter has a maximum increment rate of 12 288 000 counts per second.;

aFarEndLineSESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndLineSESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndLineSESs(195)};

bFarEndLineSESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.15

NOTE—This counter has a maximum increment rate of 1 count per second.;

aFarEndLineESs **ATTRIBUTE**

DERIVED FROM aCMCounter;

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SUPERSEDED

MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndLineESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndLineESs(196)};

bFarEndLineESs BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.16

NOTE—This counter has a maximum increment rate of 1 count per second.;

aFarEndLineCVs ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndLineCVs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndLineCVs(197)};

bFarEndLineCVs BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.17

NOTE—This counter has a maximum increment rate of 2 040 000 counts per second.;

aPathStatus ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.PathStatus;
MATCHES FOR EQUALITY;
BEHAVIOUR bPathStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pathStatus(198)};

bPathStatus BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.18;

aPathSESThreshold ATTRIBUTE

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.SESThreshold;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPathSESThreshold;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pathSESThreshold(199)};

bPathSESThreshold BEHAVIOUR

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.19;

aPathSESs ATTRIBUTE

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPathSESs;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pathSESs(200)};

bPathSESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.20

NOTE—This counter has a maximum increment rate of 1 count per second.;

aPathESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPathESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pathESs(201)};

NOTE—This counter has a maximum increment rate of 1 count per second.;

bPathESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.21;

aPathCVs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bPathCVs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) pathCVs(202)};

bPathCVs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.22

NOTE—This counter has a maximum increment rate of 8000 counts per second.;

aJ1ValueTX **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.JValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bJ1ValueTX;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) j1ValueTX(203)};

bJ1ValueTX **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.23;

aJ1ValueRX **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.JValue;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bJ1ValueRX;

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SUPERSEDED

REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) j1ValueRX(204)};

bJ1ValueRX **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.24;

aFarEndPathStatus **ATTRIBUTE**

WITH ATTRIBUTE SYNTAX IEEE802Dot3-MgmtAttributeModule.FarEndPathStatus;
MATCHES FOR EQUALITY;
BEHAVIOUR bFarEndPathStatus;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndPathStatus(205)};

bFarEndPathStatus **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.25;

aFarEndPathSESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndPathSESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndPathSESs(206)};

bFarEndPathSESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.26

NOTE—This counter has a maximum increment rate of 1 count per second.;

aFarEndPathESs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndPathESs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndPathESs(207)};

bFarEndPathESs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.27

NOTE—This counter has a maximum increment rate of 1 count per second.;

aFarEndPathCVs **ATTRIBUTE**

DERIVED FROM aCMCounter;
MATCHES FOR EQUALITY, ORDERING;
BEHAVIOUR bFarEndPathCVs;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) farEndPathCVs(208)};

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bFarEndPathCVs **BEHAVIOUR**

DEFINED AS See “BEHAVIOUR DEFINED AS” in 30.8.1.1.28

NOTE—This counter has a maximum increment rate of counts 8000 per second.;

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Annex 30B

(normative)

GDMO and ASN.1 definitions for management

30B.1 Common attributes template

This template defines generic facilities that are used in the standard.

aCMCounter ATTRIBUTE

DERIVED FROM "ISO/IEC 10165-5":genericWrappingCounter;
BEHAVIOUR bCMCounter;
REGISTERED AS {iso(1) member-body(2) us(840) ieee802dot3(10006) csmacdmgt(30) attribute(7) cmCounter(88)};

bCMCounter BEHAVIOUR

DEFINED AS Wraps at one of two sizes. Size is conditional.
Wraps at 32 bits, that is this counter reaches its maximum value at $2^{32}-1$ (i.e., approximately 4.294×10^{9}) and then rolls over to zero on the next increment, if maximum increment rate from zero causes a rollover in 58 min or more.
Wraps at 64 bits, that is this counter reaches its maximum value at $2^{64}-1$ (i.e., approximately $1.844\ldots \times 10^{19}$) and then rolls over to zero on the next increment, if maximum increment rate from zero would cause a 32 bit counter to roll over in less than 58 min.
The counter that this is derived from initializes to zero. Initialization to zero is not a requirement of this standard;

30B.2 ASN.1 module for CSMA/CD managed objects

This ASN.1 module defines the ASN.1 types and subtypes that are referred to immediately after the WITH ATTRIBUTE SYNTAX construct in this clause's uses of the attribute template defined in ISO/IEC 10165-4: 1992, Guidelines for the definition of managed objects (GDMO).

IEEE802Dot3-MgmtAttributeModule {iso(1) member-body(2) us(840) ieee802dot3(10006) global(1) asn1Module(2) commonDefinitions(0) version(2)} DEFINITIONS IMPLICIT TAGS::= BEGIN

EXPORTS--*everything*

IMPORTS--*implicitly imports ISO 8824: 1990*

```
MACAddress
    FROM IEEE802CommonDefinitions
    {iso(1) member-body(2) us(840) ieee802dot1partF(10011)
    asn1Module(2) commonDefinitions(0) version1(0)};
AdminState::= ENUMERATED {
    other                   (1),    --undefined
```

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```
        unknown         (2),    --initializing, true state not yet known
        operational     (3),    --powered and connected
        standby         (4),    --inactive but on
        shutdown        (5)     --similar to power down
        }
    AggDataRate ::= INTEGER (0..2^32-1)--The data rate of an Aggregation

    AggID ::= INTEGER (0..2^32-1)

    AggOrInd ::= BOOLEAN

    AggPortID ::= INTEGER (0..2^32-1)

    AggPortList ::= SEQUENCE OF AggPortID

    AggPortState ::= BIT STRING (SIZE (1..8))

    AggState ::= ENUMERATED {
        up              (0),    --operational
        down            (1)     --disabled
        }

    AttemptArray::= SEQUENCE OF aCMCounter--array [1..attempt limit - 1]

    AutoNegAdminState::= ENUMERATED {
        disabled        (1),
        enabled         (2)
        }

    AutoNegAutoConfig::= ENUMERATED {
        other           (1),
        configuring     (2),
        complete        (3),
        disabled        (4),
        parallel detect fail    (5)
        }

    AutoNegRemoteSignalingDetect::= ENUMERATED {
        detected        (1),
        notdetected     (2)
        }

    AutoNegSelector::= ENUMERATED {
        other           (1),    --undefined
        ethernet        (2),    --802.3
        isoethernet     (3)     --802.9
        }

    AutoNegSelectorList::= SEQUENCE OF AutoNegSelector

    AutoNegTechnology::= ENUMERATED {
```


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```
        global              (0),    --reserved for future use.
        other               (1),    --undefined
        unknown             (2),    --initializing, true ability not yet known.
        10BASE-T            (14),   --10BASE-T as defined in Clause 14
        10BASE-TFD          (142),  --Full duplex 10BASE-T as defined in Clauses 14 and 31
        100BASE-T4          (23),   --100BASE-T4 as defined in Clause 23
        100BASE-TX          (25),   --100BASE-TX as defined in Clause 25
        100BASE-TXFD        (252),  --Full duplex 100BASE-TX as defined in Clauses 25 and 31
        FDX PAUSE           (312),  --PAUSE operation for full duplex links as defined in
        Annex 31B
        FDX APAUSE          (313),  --Asymmetric PAUSE operation for full duplex links as defined
                                     in Clause 37 and Annex 31B
        FDX SPAUSE          (314),  --Symmetric PAUSE operation for full duplex links as defined
                                     in Clause 37 and Annex 31B
        FDX BPAUSE          (315),  --Asymmetric and Symmetric PAUSE operation for full duplex
                                     links as defined in Clause 37 and Annex 31B
        100BASE-T2          (32),   --100BASE-T2 as defined in Clause 32
        100BASE-T2FD        (322),  --Full duplex 100BASE-T2 as defined in Clauses 31 and 32
        1000BASE-X          (36),   --1000BASE-X as defined in Clause 36
        1000BASE-XFD        (362),  --Full duplex 1000BASE-X as defined in Clause 36
        1000BASE-T          (40),   --1000BASE-T UTP PHY as defined in Clause 40
        1000BASE-TFD        (402),  --Full duplex 1000BASE-T UTP PHY to be defined in
        Clause 40
        Rem Fault1          (37),   --Remote fault bit 1 (RF1) as specified in Clause 37
        Rem Fault2          (372),  --Remote fault bit 2 (RF1) as specified in Clause 37
        isoethernet         (8029)  --802.9 ISLAN-16T
        }

AutoNegTechnologyList::= SEQUENCE OF AutoNegTechnology

AutoPartitionState::= ENUMERATED {
        autoPartitioned     (1),
        notAutoPartitioned  (2)
        }


BbandFrequency::= SEQUENCE {
        xmitCarrierFrequency    [1]     INTEGER , --Frequency in MHz times 4 (250 kHz resolution)
        translationFrequency    [2]     INTEGER   --Frequency in MHz times 4 (250 kHz resolution)
        }


BbandXmitRcvSplitType::= ENUMERATED {
        other               (1),    --undefined
        single              (2),    --single-cable system
        dual                (3)     --dual-cable system, offset normally zero
        }


BitString::= BIT STRING (SIZE (1..1024))


ChurnState ::= ENUMERATED {
        noChurn              (0),   --NO_ACTOR/PARTNER_CHURN
                                    --or ACTOR/PARTNER_CHURN_MONITOR
        churn               (1)     --ACTOR/PARTNER_CHURN
                            }


CollectorMaxDelay ::= INTEGER       --16 bit value, tens of microseconds
                                    --(max = 0.65535 seconds)


DescriptionString ::= PrintableString (SIZE 0..255))
```

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```
DuplexValues::= ENUMERATED {
    half duplex         (1),    --capable of operating in half duplex mode
    full duplex         (2),    --capable of operating in full duplex mode
    unknown             (3)     --unknown duplex capability
    }

FarEndPathStatus ::= BIT STRING (SIZE (2))

Integer32 ::= INTEGER (0..2^32-1)    --32 bit value

Jabber::= SEQUENCE {
    jabberFlag          [1]     JabberFlag,
    jabberCounter       [2]     JabberCounter
    }

JabberFlag::= ENUMERATED {
    other               (1),    --undefined
    unknown             (2),    --initializing, true state not yet known
    normal              (3),    --state is true or normal
    fault               (4)     --state is false, fault or abnormal
    }

JabberCounter::= INTEGER (0..2^32 - 1)

JValue::= OCTET STRING (SIZE (16))

KeyValue ::= INTEGER (0..2^16-1)    --16 bit value; range 0-65535

LACPActivity ::= ENUMERATED {
    active              (0),    --Port is Active LACP
    passive             (1)     --Port is Passive LACP
    }

LACPTimeout ::= ENUMERATED {
    short               (0),    --Timeouts are Short
    long                (1)     --Timeouts are Long
    }

LineStatus ::= BIT STRING (SIZE (2))

LinkDelayAllowance::= INTEGER (0..2^32 - 1)

MACControlFunctions::= ENUMERATED {
    PAUSE               (312)   --PAUSE command implemented
    }

MACControlFunctionsList::= SEQUENCE OF MACControlFunctions

MACCapabilitiesList::= SEQUENCE OF DuplexValues
```


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```
MauTypeList::= SEQUENCE OF TypeValue


MediaAvailState::= ENUMERATED {
      other                 (1),      --undefined
      unknown               (2),      --initializing, true state not yet known
      available             (3),      --link or light normal, loopback normal
      not available         (4),      --link loss or low light, no loopback
      remote fault          (5),      --remote fault with no detail
      invalid signal        (6),      --invalid signal, applies only to 10BASE-FB
      remote jabber         (7),      --remote fault, reason known to be jabber
      remote link loss      (8),      --remote fault, reason known to be far-end link loss
      remote test           (9),      --remote fault, reason known to be test
      offline               (10),     --offline, applies only to Clause 37 Auto-Negotiation
      auto neg error        (11)      --Auto-Negotiation error, applies only to Clause 37 Auto-
                                      Negotiation
      PMD link fault        (12)      --PMD/PMD receive link fault
      WIS frame loss        (13)      --WIS loss of frame , applies only to 10GBASE-W
      WIS signal loss       (14)      --WIS loss of signal, applies only to 10GBASE-W
      PCS link fault        (15)      --PCS receive link fault
      excessive BER         (16)      --PCS Bit Error Rate monitor reporting excessive error rate
      DXS link fault        (17)      --DTE XS receive link fault, applies only to XAUI
      PXS link fault        (18)      --PHY XS transmit link fault, applies only to XAUI
      }


MIIDetect::= ENUMERATED {
      unknown               (1),
      presentNothingConnected(2),
      presentConnected      (3),
      absent                (4)
      }


MulticastAddressList::= SEQUENCE OF MACAddress


MuxState ::= ENUMERATED {
      detached              (0),      --DETACHED
      waiting               (1),      --WAITING
      attached              (2),      --ATTACHED
      collecting            (3),      --COLLECTING
      distributing          (4),      --DISTRIBUTING
      collecting_distributing (5)     --COLLECTING_DISTRIBUTING
      }


NotificationEnable ::= ENUMERATED {
      enabled               (0),      --Notifications enabled
      disabled              (1)       --Notifications disabled


OneOfName::= INTEGER (1..1024)


PathStatus ::= BIT STRING (SIZE (4))


PhyTypeList::= SEQUENCE OF PhyTypeValue


PhyTypeValue::= ENUMERATED {
      other                 (1),      --undefined
```

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```
        unknown             (2),    --initializing, true state or type not yet known
        none                (3),    --MII present and nothing connected
        10 Mb/s             (7),    --Clause 7 10 Mb/s Manchester
        100BASE-T4          (23),   --Clause 23 100 Mb/s 8B/6T
        100BASE-X           (24),   --Clause 24 100 Mb/s 4B/5B
        100BASE-T2          (32),   --Clause 32 100 Mb/s PAM5x5
        1000BASE-X          (36),   --Clause 36 1000 Mb/s 8B/10B
        1000BASE-T          (40)    --Clause 40 1000 Mb/s 4D-PAM5
        10GBASE-X           (48)    --Clause 48 10 Gb/s 4
        10GBASE-R           (49)    --Clause 49 10 Gb/s 64B/66B
        10GBASE-W           (50)    --Clause 49 10 Gb/s 64B/66B and Clause 50 WIS
        }

PortAdminState::= ENUMERATED {
        disabled            (1),
        enabled             (2)
        }

PortNumber ::= INTEGER (0..2^16-1)

PriorityValue ::= INTEGER (0..2^16-1) --16 bits

RateValues ::= ENUMERATED {
        rate control off    (1),    -- rate control enabled
        rate control on     (2),    -- rate control disabled
        unknown             (3)     -- rate control mode unknown
        }

RegisterEight::= INTEGER (0..255)

RepeaterHealthData::= OCTET STRING (SIZE (0..255))

RepeaterHealthInfo::= SEQUENCE {
        repeaterHealthState [1]     RepeaterHealthState,
        repeaterHealthText  [2]     RepeaterHealthText  OPTIONAL,
        repeaterHealthData  [3]     RepeaterHealthData  OPTIONAL
        }

RepeaterHealthState::= ENUMERATED {
        other               (1),    --undefined or unknown
        ok                  (2),    --no known failures
        repeaterFailure     (3),    --known to have a repeater-related failure
        groupFailure        (4),    --known to have a group-related failure
        portFailure         (5),    --known to have a port-related failure
        generalFailure      (6)     --has a failure condition, unspecified type
        }

RepeaterType::= ENUMERATED {
        other               (1),    --See 30.2.5:
        unknown             (2),    --initializing, true state or type not yet known
        10 Mb/s             (9),    --Clause 9 10 Mb/s Baseband repeater
        100 Mb/sClassI      (271),  --Clause 27 class I 100 Mb/s Baseband repeater
        100 Mb/sClassII     (272),  --Clause 27 class II 100 Mb/s Baseband repeater
        1000 Mb/s           (41),   --Clause 41 1000 Mb/s Baseband repeater
        802.9a              (99)    --Integrated services repeater
```


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```
        }

    RepeaterHealthText::= PrintableString (SIZE (0..255))

    RxState ::= ENUMERATED {
        current             (0),
        expired             (1),
        defaulted           (2),
        initialize          (3),
        lacpDisabled        (4),
        portDisabled        (5)
        }

    SectionStatus ::= BIT STRING (SIZE (2))

    SESThreshold ::= INTEGER (0..2^32-1)

    TrueFalse::= BOOLEAN

    TypeList::= SEQUENCE OF TypeValue

    TypeValue::= ENUMERATED {
        global              (0),    --undefined
        other               (1),    --undefined
        unknown             (2),    --initializing, true state not yet known
        AUI                 (7),    --no internal MAU, view from AUI
        10BASE5             (8),    --Thick coax MAU as specified in Clause 8
        FOIRL               (9),    --FOIRL MAU as specified in 9.9
        10BASE2             (10),   --Thin coax MAU as specified in Clause 10
        10BROAD36           (11),   --Broadband DTE MAU as specified in Clause 11
        10BASE-T            (14),   --UTP MAU as specified in Clause 14, duplex mode
                                      unknown
        10BASE-THD          (141),  --UTP MAU as specified in Clause 14, half duplex mode
        10BASE-TFD          (142),  --UTP MAU as specified in Clause 14, full duplex mode
        10BASE-FP           (16),   --Passive fiber MAU as specified in Clause 16
        10BASE-FB           (17),   --Synchronous fiber MAU as specified in Clause 17
        10BASE-FL           (18),   --Asynchronous fiber MAU as specified in Clause 18, duplex
                                      mode unknown
        10BASE-FLHD         (181),  --Asynchronous fiber MAU as specified in Clause 18, half
                                      duplex mode
        10BASE-FLFD         (182),  --Asynchronous fiber MAU as specified in Clause 18, full
                                      duplex mode
        100BASE-T4          (23),   --Four-pair Category 3 UTP as specified in Clause 23
        100BASE-TX          (25),   --Two-pair Category 5 UTP as specified in Clause 25, duplex
                                      mode unknown
        100BASE-TXHD        (251),  --Two-pair Category 5 UTP as specified in Clause 25, half
                                      duplex mode
        100BASE-TXFD        (252),  --Two-pair Category 5 UTP as specified in Clause 25, full
                                      duplex mode
        100BASE-FX          (26),   --X fiber over PMD as specified in Clause 26, duplex mode
                                      unknown
        100BASE-FXHD        (261),  --X fiber over PMD as specified in Clause 26, half duplex mode
        100BASE-FXFD        (262),  --X fiber over PMD as specified in Clause 26, full duplex mode
        100BASE-T2          (32),   --Two-pair Category 3 UTP as specified in Clause 32, duplex
                                      mode unknown
        100BASE-T2HD        (321),  --Two-pair Category 3 UTP as specified in Clause 32, half
                                      duplex mode
```

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```
        100BASE-T2FD        (322),   --Two-pair Category 3 UTP as specified in Clause 32, full
                                       duplex mode
        1000BASE-X          (36),    --X PCS/PMA as specified in Clause 36 over unknown PMD,
                                     duplex mode unknown
        1000BASE-XHD        (361),   --X  PCS/PMA as specified in Clause 36 over unknown PMD,
                                     half duplex mode
        1000BASE-XFD        (362),   --X PCS/PMA as specified in Clause 36 over unknown PMD,
                                      full duplex mode
        1000BASE-LX         (381),   --X fiber over long-wavelength laser PMD as specified in
                                     Clause 38, duplex mode unknown
        1000BASE-LXHD       (382),   --X fiber over long-wavelength laser PMD as specified in
                                     Clause 38, half duplex mode
        1000BASE-LXFD       (383),   --X fiber over long-wavelength laser PMD as specified in
                                     Clause 38, full duplex mode
        1000BASE-SX         (384),   --X fiber over short-wavelength laser PMD as specified in
                                     Clause 38, duplex mode unknown
        1000BASE-SXHD       (385),   --X fiber over short-wavelength laser PMD as specified in
                                     Clause 38, half duplex mode
        1000BASE-SXFD       (386),   --X fiber over short-wavelength laser PMD as specified in
                                     Clause 38, full duplex mode
        1000BASE-CX         (39),    --X copper over 150-Ohm balanced cable PMD as specified in
                                     Clause 39, duplex mode unknown
        1000BASE-CXHD       (391),   --X copper over 150-Ohm balanced cable PMD as specified in
                                     Clause 39, half duplex mode
        1000BASE-CXFD       (392),   --X copper over 150-Ohm balanced cable PMD as specified in
                                     Clause 39, full duplex mode
        1000BASE-T          (40),    --Four-pair Category 5 UTP PHY as specified in Clause 40,
                                     duplex mode unknown
        1000BASE-THD        (401),   --Four-pair Category 5 UTP PHY as specified in Clause 40,
                                     half duplex mode
        1000BASE-TFD        (402),   --Four-pair Category 5 UTP PHY as specified in Clause 40,
                                     full duplex mode
        10GBASE-X           (48)     --X PCS/PMA as specified in Clause 48 over undefined PMD
        10GBASE-LX4         (481)    --X fibre over WWDM optics as specified in Clause 53
        10GBASE-R           (49)     --R PCS/PMA as specified in Clause 49 over undefined PMD
        10GBASE-ER          (491)    --R fibre over 1550nm optics as specified in Clause 52
        10GBASE-LR          (492)    --R fibre over 1310nm optics as specified in Clause 52
        10GBASE-SR          (493)    --R fibre over 850nm optics as specified in Clause 52
        10GBASE-W           (50)     --W PCS/PMA as specified in Clauses 49 and 50 over
                                     undefined PMD
        10GBASE-EW          (501)    --W fibre over 1550nm optics as specified in Clause 52
        10GBASE-LW          (502)    --W fibre over 1310nm optics as specified in Clause 52
        10GBASE-SW          (503)    --W fibre over 850nm optics as specified in Clause 52
        802.9a              (99)     --Integrated services MAU as specified in IEEE Std 802.9
                                     ISLAN-16T

        }
END
```


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Annex 31B

(normative)

MAC Control PAUSE operation

31B.3.1 Transmit operation

Change 31B.3.1 to read as follows:

Upon receipt of an MA_CONTROL.request primitive containing the PAUSE opcode from a MAC Control client, the MAC Control sublayer calls the MAC sublayer TransmitFrame function with the following parameters:

a) The destinationParam is set equal to the destination_address parameter of the ~~MA_DATA.request~~ MA_CONTROL.request primitive. This parameter is currently restricted to the value specified in 31B.1.
b) The sourceParam is set equal to the 48-bit individual address of the station.
c) The lengthOrTypeParam is set to the reserved ~~802.3_MAC_Control~~ 802.3 MAC Control type value specified in 31.4.1.3.
d) The dataParam is set equal to the concatenation of the PAUSE opcode encoding (see Annex 31A), the pause_time request_operand specified in the MA_CONTROL.request primitive ~~(see 2.3.3.2)~~, and a field containing zeros of the length specified in 31.4.1.6.
e) The fcsParamPresent is set to false.

Upon receipt of a data transmission request from the MAC Control client through the MA_DATA.request primitive, if the transmission of data frames has not been inhibited due to reception of a valid MAC Control frame specifying the PAUSE operation and a non-zero pause_time, the MAC Control sublayer calls the MAC sublayer TransmitFrame function with the following parameters:

a) The destinationParam is set equal to the destination_address parameter of the MA_DATA.request ~~MA_CONTROL.request~~ primitive.
b) ~~The sourceParam is set equal to the 48-bit individual address of the station.~~
The sourceParam is set equal to the source_address parameter of the MA_DATA.request primitive.
c) ~~The lengthOrTypeParam and dataParam are set from the m_sdu field of the MA_DATA.request primitive.~~
The lengthOrTypeParam is set to the value of the first two octets of the mac_service_data_unit parameter and the dataParam is set to the value of the remaining octets of the mac_service_data_unit parameter.
d) If the frame_check_sequence parameter is present and the MAC sublayer supports client-supplied frame check sequence values, then the fcsParamValue is set to the value of the FCS for the frame and the fcsParamPresent is set to true. Otherwise, fcsParamPresent is set to false.

31B.3.2.6 Transmit state diagram for PAUSE operation

Replace Figure 31B-1 to read as follows:

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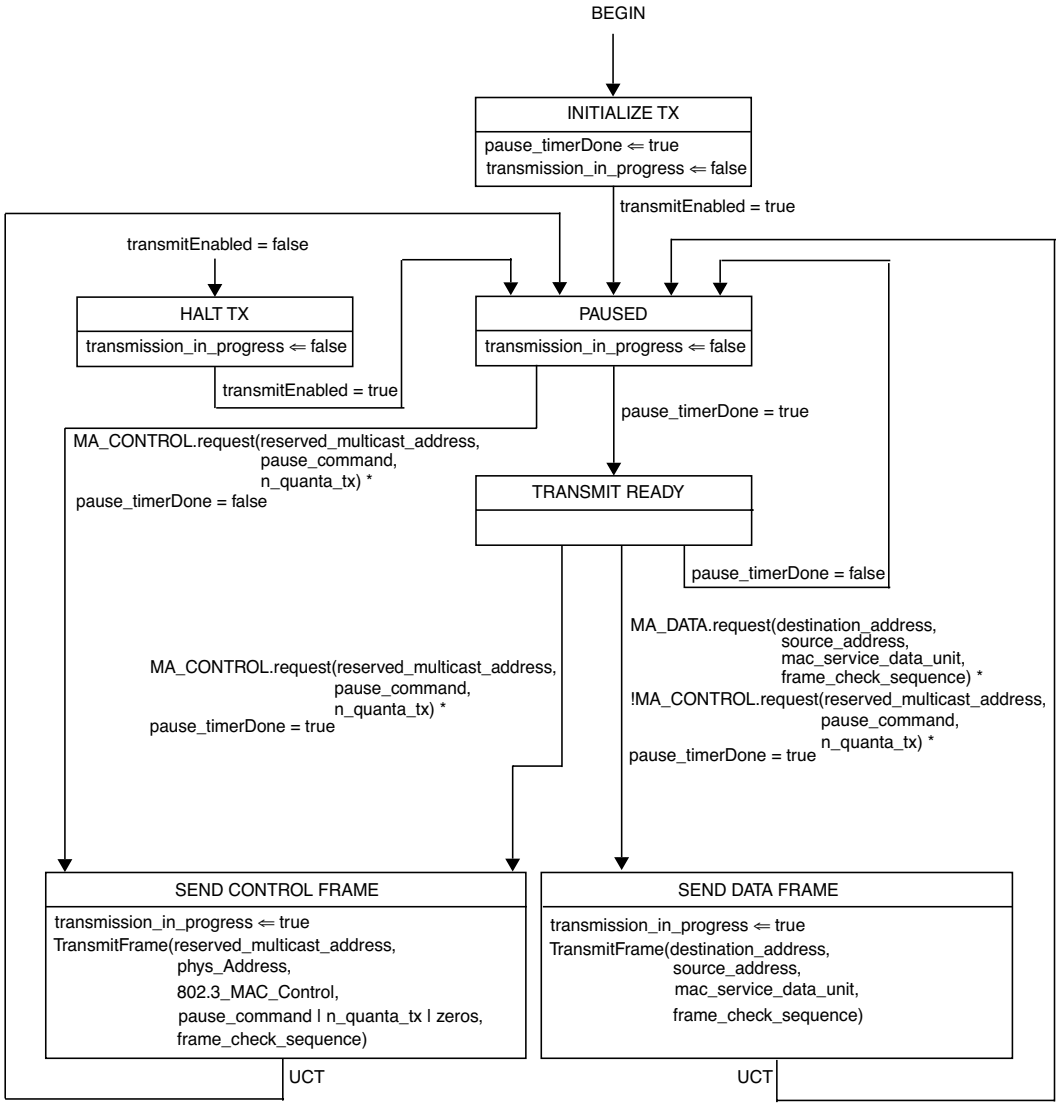


Figure 31B–1—PAUSE Operation Transmit state diagram

31B.3.4.4 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for PAUSE operation

Delete the "_" (underscore) in the header of 31B.3.4.4 between "INITIATE" and "MAC."

31B.3.7 Timing considerations for PAUSE operation

Change 31B.3.7 to read as follows:

In a full duplex mode DTE, it is possible to receive PAUSE frames asynchronously with respect to the transmission of Data frames. For effective flow control, it is necessary to place an upper bound on the length of time that a DTE can transmit Data frames after receiving a valid PAUSE frame with a non-zero pause_time request_operand.

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Reception of a PAUSE frame shall not affect the transmission of a frame that has been submitted by the MAC Control sublayer to the underlying MAC (i.e., the TransmitFrame function is synchronous, and is never interrupted).

At operating speeds of 100 Mb/s or less, a station that implements an exposed MII, shall not begin to transmit a (new) frame (assertion of TX_EN at the MII, see 22.2.2.3) more than pause_quantum bit times after the reception of a valid PAUSE frame (de-assertion of RX_DV at the MII, see 22.2.2.6) that contains a non-zero value of pause_time. Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to (pause_quantum + 64) bit times.

At an operating speeds above 100 Mb/s of 1000 Mb/s, a station shall not begin to transmit a (new) frame more than two pause_quantum bit times after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 10 Gb/s and above, a station shall not begin to transmit a (new) frame more than sixty pause_quantum bit times after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

In addition to DTE and MAC Control delays, system designers should take into account the delay of the link segment when designing devices that implement the PAUSE operation (see Clause 29).

31B.4.6 PAUSE command MAC timing considerations

Change the PICS table in 31B.4.6 to read as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Effect of PAUSE frame on a frame already submitted to underlying MAC	31B.3.7	Has no effect	M	Yes [ ]
	Delay from receiving valid PAUSE command, with non-zero value for pause_time, to cessation of transmission	31B.3.7	Measured as described		
TIM2	Measurement point for station with MII		Delay at MDI ≤ pause_quantum bits	MIIa: M	N/A [ ] M: Yes [ ]
TIM3	Measurement point for station without MII at 100 Mb/s or less		Delay at MDI ≤ (pause_quantum + 64) bits	MIIb: M	N/A [ ] M: Yes [ ]
TIM4	Measurement point for station at greater than 100 Mb/s at 1000 Mb/s		Delay at MDI ≤ (2 × pause_quantum) bits	MIIc: M	N/A [ ] M: Yes [ ]
TIM5	Measurement point for station at 10 Gb/s or greater		Delay at MDI ≤ (60 × pause_quantum) bits	MIId: M	N/A [ ] M: Yes [ ]

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IEEE Standard for Information technology—
Telecommunications and information exchange between systems—
Local and metropolitan area networks—
Specific requirements—

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation

44. Introduction to 10 Gb/s baseband network

44.1 Overview

44.1.1 Scope

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

10 Gigabit Ethernet extends the IEEE 802.3 MAC beyond 1000 Mb/s to 10 Gb/s. The bit rate is faster and the bit times are shorter—both in proportion to the change in bandwidth. The minimum packet transmission time has been reduced by a factor of ten. A rate control mode (see 4.2.3.2.2) is added to the MAC to adapt the average MAC data rate to the SONET/SDH data rate for WAN-compatible applications of this standard. Achievable topologies for 10 Gb/s operation are comparable to those found in 1000BASE-X full duplex mode and equivalent to those found in WAN applications.

10 Gigabit Ethernet is defined for full duplex mode of operation only.

44.1.2 Objectives

The following are the objectives of 10 Gigabit Ethernet:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s, and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using optical fiber compliant with ISO/IEC 11801: 1995.
e) Allow for a nominal network extent of up to 40 km.
f) Support a BER objective of 10^{-12}.

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44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

10 Gigabit Ethernet couples the IEEE 802.3 (CSMA/CD) MAC to a family of 10 Gb/s Physical Layers. The relationships among 10 Gigabit Ethernet, the IEEE 802.3 (CSMA/CD) MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 44–1.

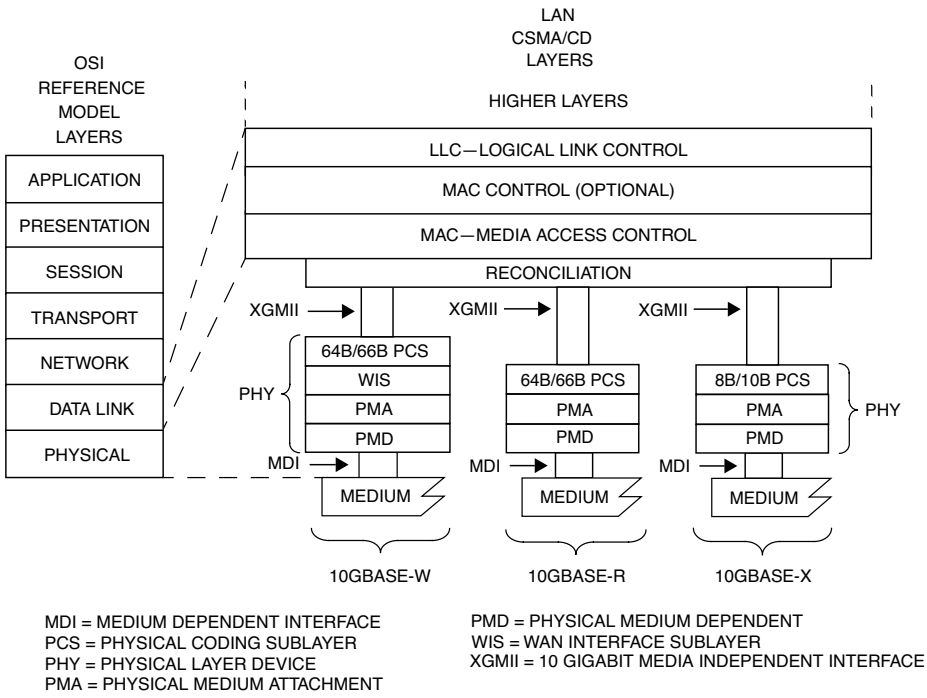


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The XGMII, which, when implemented at an observable interconnection port, uses a four octet-wide data path as specified in Clause 46.
b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.
c) The PMA Service Interface, which, when physically implemented as the XSBI (10 Gigabit Sixteen Bit Interface) at an observable interconnection port, uses a 16-bit-wide data path as specified in Clause 51.
d) The MDI as specified in Clause 53 for 10GBASE-LX4 and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

The 10 Gigabit Media Independent Interface (Clause 46) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY). This XGMII supports 10 Gb/s operation through its 32-bit-wide transmit and receive data paths. The Reconciliation Sublayer provides a mapping between the signals provided at the XGMII and the MAC/PLS service definition.

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While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clauses 47, 48, and 49.

44.1.4.2 XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

The 10 Gigabit Attachment Unit Interface (Clause 47) provides an interconnection between two XGMII Extender sublayers to increase the reach of the XGMII. This XAUI supports 10 Gb/s operation through its four-lane, differential-pair transmit and receive paths. The XGXS provides a mapping between the signals provided at the XGMII and the XAUI.

44.1.4.3 Management interface (MDIO/MDC)

The MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

44.1.4.4 Physical Layer signaling systems

This standard specifies a family of Physical Layer implementations. The generic term 10 Gigabit Ethernet refers to any use of the 10 Gb/s IEEE 802.3 MAC (the 10 Gigabit Ethernet MAC) coupled with any IEEE 802.3 10GBASE physical layer implementation. Table 44–1 specifies the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures shall meet the requirements of the corresponding clauses.

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause							
	48	49	50	51	52			53
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD
10GBASE-SR		M[a]		M	M			
10GBASE-SW		M	M	M	M			
10GBASE-LX4	M							M
10GBASE-LR		M		M		M		
10GBASE-LW		M	M	M		M		
10GBASE-ER		M		M			M	
10GBASE-EW		M	M	M			M	

[a]M = Mandatory

The term 10GBASE-X, specified in Clause 48 and Clause 53, refers to a specific family of physical layer implementations based upon 8B/10B data coding method. The 10GBASE-X family of physical layer implementations is composed of 10GBASE-LX4.

The term 10GBASE-R, specified in Clauses 49, 51, and 52, refers to a specific family of physical layer implementations based upon 64B/66B data coding method. The 10GBASE-R family of physical layer implementations is composed of 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER.

The term 10GBASE-W, specified in Clause 49 to Clause 52, refers to a specific family of physical layer implementations based upon STS-192c/SDH VC-4-64c encapsulation of 64B/66B encoded data. The

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10GBASE-W family of physical layer standards has been adapted from the ANSI T1.416-1999 (SONET STS-192c/SDH VC-4-64c) physical layer specifications. The 10GBASE-W family of physical layer implementations is composed of 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

All 10GBASE-R and 10GBASE-W PHY devices share a common PCS specification (see Clause 49). The 10GBASE-W PHY devices also require the use of the WAN Interface Sublayer, (WIS) (Clause 50).

Specifications of each physical layer device are contained in Clause 52 and Clause 53.

44.1.4.5 WAN Interface Sublayer (WIS), type 10GBASE-W

The WIS provides a 10GBASE-W device with the capability to transmit and receive IEEE 802.3 MAC frames within the payload envelope of a SONET STS-192c/SDH VC-4-64c frame.

44.1.5 Management

Managed objects, attributes, and actions are defined for all 10 Gigabit Ethernet components. Clause 30 consolidates all IEEE 802.3 management specifications so that 10/100/1000 Mb/s and 10 Gb/s agents can be managed by existing network management stations with little or no modification to the agent code.

44.2 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

44.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 44–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

Equation (44–1) specifies the calculation of bit time per meter of fiber based upon the parameter *n,* which represents the ratio of the speed of light in the fiber to the speed of light in a vacuum. The value of *n* should be available from the fiber manufacturer, but if no value is known then a conservative delay estimate can be calculated using a default value of $n = 0.66$. The speed of light in a vacuum is $c = 3 \times 10^8$ m/s. Table 44–3 can be used to convert fiber delay values specified relative to the speed of light or in nanoseconds per meter.

$$\text{cable delay} = \frac{10^{10}}{nc} \text{ BT/m} \qquad (44\text{–}1)$$

44.4 Protocol Implementation Conformance Statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 45 through Clause 53, demonstrates compliance by completing a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each

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Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5.
10GBASE-R PCS	3584	7	See 49.2.15.
WIS	14336	28	See 50.3.7.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.

Table 44–3—Conversion table for cable delays

Speed relative to c	ns/m	BT/m
0.40	8.33	83.3
0.50	6.67	66.7
0.51	6.54	65.4
0.52	6.41	64.1
0.53	6.29	62.9
0.54	6.17	61.7
0.55	6.06	60.6
0.56	5.95	59.5
0.57	5.85	58.5
0.58	5.75	57.5
0.5852	5.70	57.0
0.59	5.65	56.5
0.60	5.56	55.6
0.61	5.46	54.6
0.62	5.38	53.8
0.63	5.29	52.9

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Table 44–3—Conversion table for cable delays *(continued)*

Speed relative to c	ns/m	BT/m
0.64	5.21	52.1
0.65	5.13	51.3
0.654	5.10	51.0
0.66	5.05	50.5
0.666	5.01	50.1
0.67	4.98	49.8
0.68	4.90	49.0
0.69	4.83	48.3
0.7	4.76	47.6
0.8	4.17	41.7
0.9	3.70	37.0

clause as appropriate. Each of the 10 Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

44.5 Relation of 10 Gigabit Ethernet to other standards

Suitable entries for Table G1 of ISO/IEC 11801: 1995, Annex G, would be as follows:

a) Within the section Optical Link:
CSMA/CD 10GBASE-SR ISO/IEC 8802-3/ PDAM 26

b) Within the section Optical Link:
CSMA/CD 10GBASE-SW ISO/IEC 8802-3/PDAM 26

c) Within the section Optical Link:
CSMA/CD 10GBASE-LR ISO/IEC 8802-3/PDAM 26

d) Within the section Optical Link:
CSMA/CD 10GBASE-LW ISO/IEC 8802-3/PDAM 26

e) Within the section Optical Link:
CSMA/CD 10GBASE-ER ISO/IEC 8802-3/PDAM 26

f) Within the section Optical Link:
CSMA/CD 10GBASE-EW ISO/IEC 8802-3/PDAM 26

g) Within the section Optical Link:
CSMA/CD 10GBASE-LX4 ISO/IEC 8802-3/PDAM 26

A suitable entry for Table G5 of ISO/IEC 11801: 1995, Annex G, is exemplified in Table 44–4.

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Table 44–4—Table G5 of ISO/IEC 11801: 1995

	Fibre per Clauses 5, 7, and 8			Optical link per Clause 8								
				Horizontal			Building backbone			Campus backbone		
	62.5/125 μm MMF	50/125 μm MMF	10/125 μm SMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm SMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm SMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm SMF
8802-3: 10GBASE-SR	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-SW	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-LR	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-LW	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-ER			I			N			N			N
8802-3: 10GBASE-EW			I			N			N			N
8802-3: 10GBASE-LX4	I	I	I	N	N	N	N	N	N	N	N	N

NOTE—"N" denotes normative support of the media in the standard.
"I" denotes that there is information in the International Standard regarding operation on this media.

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45. Management Data Input/Output (MDIO) Interface

45.1 Overview

This clause defines the logical and electrical characteristics of an extension to the two signal Management Data Input/Output (MDIO) Interface specified in Clause 22.

The purpose of this extension is to provide the ability to access more device registers while still retaining logical compatibility with the MDIO interface defined in Clause 22. Clause 22 specifies the MDIO frame format and uses an ST code of 01 to access registers. In this clause, additional registers are added to the address space by defining MDIO frames that use an ST code of 00.

This extension to the MDIO interface is applicable to Ethernet implementations that operate at speeds of 10 Gb/s and above.

The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

Throughout this clause, an "a.b.c" format is used to identify register bits, where "a" is the device address, "b" is the register address, and "c" is the bit number within the register.

45.1.1 Summary of major concepts

The following are major concepts of the MDIO Interface:

a) Preserve the management frame structure defined in 22.2.4.5.
b) Define a mechanism to address more registers than specified in 22.2.4.5.
c) Define ST and OP codes to identify and control the extended access functions.
d) Provide an electrical interface specification that is compatible with common digital CMOS ASIC processes.

45.1.2 Application

This clause defines a management interface between Station Management (STA) and the sublayers that form a 10 Gb/s Physical Layer device (PHY) entity. Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an MDIO Manageable Device (MMD). This clause allows a single STA, through a single MDIO interface, to access up to 32 PHYs (defined as PRTAD in the frame format defined in 45.3) consisting of up to 32 MMDs as shown in Figure 45–1. The MDIO interface can support up to a maximum of 65 536 registers in each MMD.

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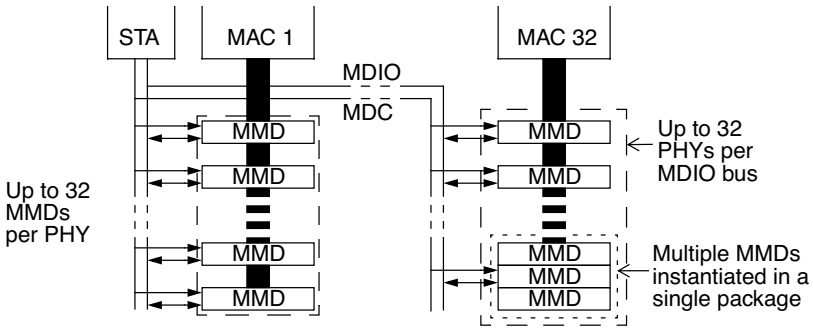


Figure 45–1—DTE and MMD devices

45.2 MDIO Interface Registers

The management interface specified in Clause 22 provides a simple, two signal, serial interface to connect a Station Management entity and a managed PHY for providing access to management parameters and services. The interface is referred to as the MII management interface.

The MDIO interface is based on the MII management interface, but differs from it in several ways. The MDIO interface uses indirect addressing to create an extended address space allowing a much larger number of registers to be accessed within each MMD. The MDIO address space is orthogonal to the MII management interface address space. The mechanism for the addressing is defined in 45.3. The MDIO electrical interface operates at lower voltages than those specified for the MII management interface. The electrical interface is specified in 45.4. For cases where a single entity combines Clause 45 MMDs with Clause 22 registers, then the Clause 22 registers may be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. The list of possible MMDs is shown in Table 45–1. The PHY XS and DTE XS devices are the two partner devices used to extend the interface that sits immediately below the Reconciliation Sublayer. For 10 Gigabit Ethernet, the interface extenders are defined as the XGXS devices.

If a device supports the MDIO interface it shall respond to all possible register addresses for the device and return a value of zero for undefined and unsupported registers. Writes to undefined registers and read-only registers shall have no effect. The operation of an MMD shall not be affected by writes to reserved and unsupported register bits, and such register bits shall return a value of zero when read.

To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

Some of the bits within MMD registers are defined as latching low (LL) or latching high (LH). When a bit is defined as latching low and the condition for the bit to be low has occurred, the bit shall remain low until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors. When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

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Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6 through 29	Reserved
30	Vendor specific 1
31	Vendor specific 2

For multi-bit fields, the lowest numbered bit of the field in the register corresponds to the least significant bit of the field.

Figure 45–2 describes the signal terminology used for the MMDs.

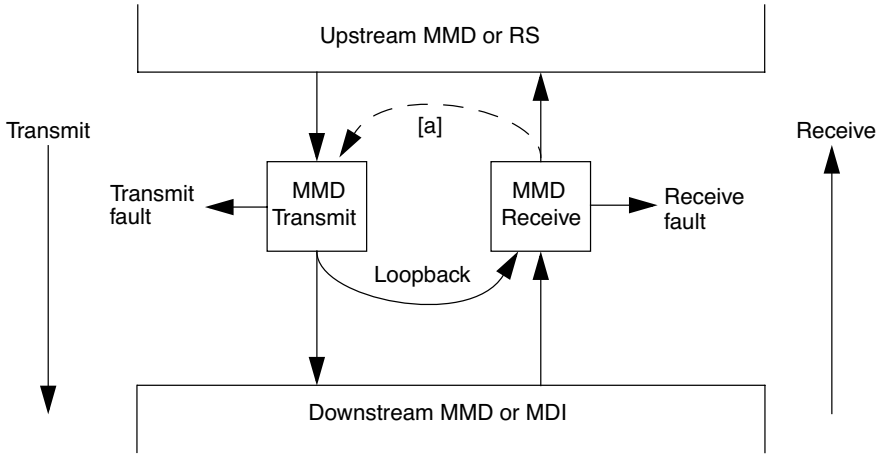


Figure 45–2—MMD signal terminology

[a] Direction of the optional PHY XS loopback

45.2.1 PMA/PMD registers

The assignment of registers in the PMA/PMD is shown in Table 45–2.

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Table 45–2—PMA/PMD registers

Register address	Register name
1.0	PMA/PMD control 1
1.1	PMA/PMD status 1
1.2, 1.3	PMA/PMD device identifier
1.4	PMA/PMD speed ability
1.5, 1.6	PMA/PMD devices in package
1.7	10G PMA/PMD control 2
1.8	10G PMA/PMD status 2
1.9	10G PMD transmit disable
1.10	10G PMD receive signal detect
1.11 through 1.13	Reserved
1.14, 1.15	PMA/PMD package identifier
1.16 through 1.32 767	Reserved
1.32 768 through 1.65 535	Vendor specific

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45.2.1.1 PMA/PMD control 1 register (Register 1.0)

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–3. The default value for each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–3—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0, writes ignored	R/W
1.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
1.0.12	Reserved	Value always 0, writes ignored	R/W
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0, writes ignored	R/W
1.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
1.0.1	Reserved	Value always 0, writes ignored	R/W
1.0.0	PMA loopback	1 = Enable PMA Loopback mode 0 = Disable PMA Loopback mode	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.1.1 Reset (1.0.15)

Resetting a PMA/PMD is accomplished by setting bit 1.0.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.0.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.0.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

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45.2.1.1.2 Low power (1.0.11)

A PMA/PMD may be placed into a low-power mode by setting bit 1.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.0.11 is zero.

NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

45.2.1.1.3 Speed selection (1.0.13,1.0.6, 1.0.5:2)

Speed selection bits 1.0.13 and 1.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PMA/PMD may be selected using bits 5 through 2. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD speed selection defaults to a supported ability.

45.2.1.1.4 PMA loopback (1.0.0)

The PMA shall be placed in a Loopback mode of operation when bit 1.0.0 is set to a one. When bit 1.0.0 is set to a one, the PMA shall accept data on the transmit path and return it on the receive path.

The loopback function is mandatory for the 10GBASE-X port type and optional for all other port types. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

The default value of bit 1.0.0 is zero.

NOTE—The signal path through the PMA that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PMA circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

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45.2.1.2 PMA/PMD status 1 register (Register 1.1)

The assignment of bits in the status 1 register is shown in Table 45–4. All the bits in the status 1 register are read only; therefore, a write to the status 1 register shall have no effect.

Table 45–4—PMA/PMD status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1.15:8	Reserved	Ignore when read	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Ignore when read	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

45.2.1.2.1 Fault (1.1.7)

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

45.2.1.2.2 Receive link status (1.1.2)

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

45.2.1.2.3 Low-power ability (1.1.1)

When read as a one, bit 1.1.1 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.1.1 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.0.11.

45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier.

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The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

The assignment of bits in the PMA/PMD speed ability register is shown in Table 45–5.

Table 45–5—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.1.4.1 10G capable (1.4.0)

When read as a one, bit 1.4.0 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 1.4.0 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s.

45.2.1.5 PMA/PMD devices in package (Registers 1.5 and 1.6)

The assignment of bits in the PMA/PMD devices in package registers is shown in Table 45–6.

When read as a one, a bit in the PMA/PMD devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PMA/PMD devices in package registers. Bit 1.5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.1.6 10G PMA/PMD control 2 register (Register 1.7)

The assignment of bits in the 10G PMA/PMD control 2 register is shown in Table 45–7.

45.2.1.6.1 PMA/PMD type selection (1.7.2:0)

The PMA/PMD type of the 10G PMA/PMD shall be selected using bits 2 through 0. The PMA/PMD type abilities of the 10G PMA/PMD are advertised in bits 7 through 0 of the 10G PMA/PMD status 2 register. A 10G PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

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Table 45–6— PMA/PMD devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
1.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
1.6.13:0	Reserved	Ignore on read	RO
1.5.15:6	Reserved	Ignore on read	RO
1.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
1.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
1.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
1.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
1.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
1.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

Table 45–7—10G PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:3	Reserved	Value always 0, writes ignored	R/W
1.7.2:0	PMA/PMD type selection	2 1 0 1 1 1 = 10GBASE-SR PMA/PMD type 1 1 0 = 10GBASE-LR PMA/PMD type 1 0 1 = 10GBASE-ER PMA/PMD type 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 1 1 = 10GBASE-SW PMA/PMD type 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 = Reserved	R/W

[a]R/W = Read/Write

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45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)

The assignment of bits in the 10G PMA/PMD status 2 register is shown in Table 45–8. All the bits in the 10G PMA/PMD status 2 register are read only; a write to the 10G PMA/PMD status 2 register shall have no effect.

Table 45–8—10G PMA/PMD status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
1.8.9	Reserved	Ignore on read	RO
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO

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Table 45–8—10G PMA/PMD status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO

[a]RO = Read Only, LH = Latching High

45.2.1.7.1 Device present (1.8.15:14)

When read as <10>, bits 1.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 1.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.1.7.2 Transmit fault ability (1.8.13)

When read as a one, bit 1.8.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.8.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.7.3 Receive fault ability (1.8.12)

When read as a one, bit 1.8.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.8.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.7.4 Transmit fault (1.8.11)

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for serial PMDs is given in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for serial PMDs is given in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.10 is zero.

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45.2.1.7.6 PMD transmit disable ability (1.8.8)

When read as a one, bit 1.8.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.8.8 indicates that the PMD is not able to perform the transmit disable function. If a PMD is able to perform the transmit disable function, then it is controlled using the PMD transmit disable register.

45.2.1.7.7 10GBASE-SR ability (1.8.7)

When read as a one, bit 1.8.7 indicates that the PMA/PMD is able to support a 10GBASE-SR PMA/PMD type. When read as a zero, bit 1.8.7 indicates that the PMA/PMD is not able to support a 10GBASE-SR PMA/PMD type.

45.2.1.7.8 10GBASE-LR ability (1.8.6)

When read as a one, bit 1.8.6 indicates that the PMA/PMD is able to support a 10GBASE-LR PMA/PMD type. When read as a zero, bit 1.8.6 indicates that the PMA/PMD is not able to support a 10GBASE-LR PMA/PMD type.

45.2.1.7.9 10GBASE-ER ability (1.8.5)

When read as a one, bit 1.8.5 indicates that the PMA/PMD is able to support a 10GBASE-ER PMA/PMD type. When read as a zero, bit 1.8.5 indicates that the PMA/PMD is not able to support a 10GBASE-ER PMA/PMD type.

45.2.1.7.10 10GBASE-LX4 ability (1.8.4)

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-LX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-LX4 PMA/PMD type.

45.2.1.7.11 10GBASE-SW ability (1.8.3)

When read as a one, bit 1.8.3 indicates that the PMA/PMD is able to support a 10GBASE-SW PMA/PMD type. When read as a zero, bit 1.8.3 indicates that the PMA/PMD is not able to support a 10GBASE-SW PMA/PMD type.

45.2.1.7.12 10GBASE-LW ability (1.8.2)

When read as a one, bit 1.8.2 indicates that the PMA/PMD is able to support a 10GBASE-LW PMA/PMD type. When read as a zero, bit 1.8.2 indicates that the PMA/PMD is not able to support a 10GBASE-LW PMA/PMD type.

45.2.1.7.13 10GBASE-EW ability (1.8.1)

When read as a one, bit 1.8.1 indicates that the PMA/PMD is able to support a 10GBASE-EW PMA/PMD type. When read as a zero, bit 1.8.1 indicates that the PMA/PMD is not able to support a 10GBASE-EW PMA/PMD type.

45.2.1.7.14 PMA loopback ability (1.8.0)

When read as a one, bit 1.8.0 indicates that the PMA is able to perform the loopback function. When read as a zero, bit 1.8.0 indicates that the PMA is not able to perform the loopback function. If a PMA is able to perform the loopback function, then it is controlled using the PMA loopback bit 1.0.0.

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45.2.1.8 10G PMD transmit disable register (Register 1.9)

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–9. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for serial PMDs is described in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7.

Table 45–9—10G PMD transmit disable register bit definitions

Bit(s)	Name	Description	R/W[a]
1.9.15:5	Reserved	Value always 0, writes ignored	R/W
1.9.4	PMD transmit disable 3	1 = Disable output on transmit lane 3 0 = Enable output on transmit lane 3	R/W
1.9.3	PMD transmit disable 2	1 = Disable output on transmit lane 2 0 = Enable output on transmit lane 2	R/W
1.9.2	PMD transmit disable 1	1 = Disable output on transmit lane 1 0 = Enable output on transmit lane 1	R/W
1.9.1	PMD transmit disable 0	1 = Disable output on transmit lane 0 0 = Enable output on transmit lane 0	R/W
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]R/W = Read/Write

45.2.1.8.1 PMD transmit disable 3 (1.9.4)

When bit 1.9.4 is set to a one, the PMD shall disable output on lane 3 of the transmit path. When bit 1.9.4 is set to a zero, the PMD shall enable output on lane 3 of the transmit path.

The default value for bit 1.9.4 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.2 PMD transmit disable 2 (1.9.3)

When bit 1.9.3 is set to a one, the PMD shall disable output on lane 2 of the transmit path. When bit 1.9.3 is set to a zero, the PMD shall enable output on lane 2 of the transmit path.

The default value for bit 1.9.3 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

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45.2.1.8.3 PMD transmit disable 1 (1.9.2)

When bit 1.9.2 is set to a one, the PMD shall disable output on lane 1 of the transmit path. When bit 1.9.2 is set to a zero, the PMD shall enable output on lane 1 of the transmit path.

The default value for bit 1.9.2 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.4 PMD transmit disable 0 (1.9.1)

When bit 1.9.1 is set to a one, the PMD shall disable output on lane 0 of the transmit path. When bit 1.9.1 is set to a zero, the PMD shall enable output on lane 0 of the transmit path.

The default value for bit 1.9.1 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

45.2.1.8.5 Global PMD transmit disable (1.9.0)

When bit 1.9.0 is set to a one, the PMD shall disable output on the transmit path. When bit 1.9.0 is set to a zero, the PMD shall enable output on the transmit path.

For single wavelength PMD types, transmission will be disabled when this bit is set to one. When this bit is set to zero, transmission is enabled.

For multiple wavelength PMD types, transmission will be disabled on all lanes when this bit is set to one. When this bit is set to zero, the lanes are individually controlled by their corresponding transmit disable bits 1.9.4:1.

The default value for bit 1.9.0 is zero.

45.2.1.9 10G PMD receive signal detect register (Register 1.10)

The assignment of bits in the 10G PMD receive signal detect register is shown in Table 45–10. The 10G PMD receive signal detect register is mandatory. PMD types that use only a single wavelength indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.4:1. PMD types that use multiple wavelengths indicate the status of each lane in bits 1.10.4:1 and the logical AND of those bits in bit 1.10.0.

45.2.1.9.1 PMD receive signal detect 3 (1.10.4)

When bit 1.10.4 is read as a one, a signal has been detected on lane 3 of the PMD receive path. When bit 1.10.4 is read as a zero, a signal has not been detected on lane 3 of the PMD receive path.

45.2.1.9.2 PMD receive signal detect 2 (1.10.3)

When bit 1.10.3 is read as a one, a signal has been detected on lane 2 of the PMD receive path. When bit 1.10.3 is read as a zero, a signal has not been detected on lane 2 of the PMD receive path.

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Table 45–10—10G PMD receive signal detect register bit definitions

Bit(s)	Name	Description	R/W[a]
1.10.15:5	Reserved	Value always 0, writes ignored	RO
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3	RO
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2	RO
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1	RO
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0	RO
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO

[a]RO = Read Only

45.2.1.9.3 PMD receive signal detect 1 (1.10.2)

When bit 1.10.2 is read as a one, a signal has been detected on lane 1 of the PMD receive path. When bit 1.10.2 is read as a zero, a signal has not been detected on lane 1 of the PMD receive path.

45.2.1.9.4 PMD receive signal detect 0 (1.10.1)

When bit 1.10.1 is read as a one, a signal has been detected on lane 0 of the PMD receive path. When bit 1.10.1 is read as a zero, a signal has not been detected on lane 0 of the PMD receive path.

45.2.1.9.5 Global PMD receive signal detect (1.10.0)

When bit 1.10.0 is read as a one, a signal has been detected on all the PMD receive paths. When bit 1.10.0 is read as a zero, a signal has not been detected on at least one of the PMD receive paths.

Single wavelength PMD types indicate the status of their receive path signal using this bit.

Multiple wavelength PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

45.2.1.10 PMA/PMD package identifier (Registers 1.14 and 1.15)

Registers 1.14 and 1.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

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The format of the package identifier is specified in 22.2.4.3.1.

45.2.2 WIS registers

The assignment of registers in the WIS is shown in Table 45–11. For the WIS octet fields, bit 8 of the corresponding field in the WIS frame maps to the lowest numbered bit of the field in the register.

Table 45–11—WIS registers

Register address	Register name
2.0	WIS control 1
2.1	WIS status 1
2.2, 2.3	WIS device identifier
2.4	WIS speed ability
2.5, 2.6	WIS devices in package
2.7	10G WIS control 2
2.8	10G WIS status 2
2.9	10G WIS test-pattern error counter
2.10 through 2.13	Reserved
2.14, 2.15	WIS package identifier
2.16 through 2.32	Reserved
2.33	10G WIS status 3
2.34 through 2.36	Reserved
2.37	10G WIS far end path block error count
2.38	Reserved
2.39 through 2.46	10G WIS J1 transmit
2.47 through 2.54	10G WIS J1 receive
2.55, 2.56	10G WIS far end line BIP errors
2.57, 2.58	10G WIS line BIP errors
2.59	10G WIS path block error count
2.60	10G WIS section BIP error count
2.61 through 2.63	Reserved
2.64 through 2.71	10G WIS J0 transmit

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Table 45–11—WIS registers *(continued)*

Register address	Register name
2.72 through 2.79	10G WIS J0 receive
2.80 through 2.32 767	Reserved
2.32 768 through 2.65 535	Vendor specific

45.2.2.1 WIS control 1 register (Register 2.0)

The assignment of bits in the WIS control 1 register is shown in Table 45–12. The default value for each bit of the WIS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–12— WIS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.0.15	Reset	1 = WIS reset 0 = Normal operation	R/W SC
2.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
2.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.12	Reserved	Value always 0, writes ignored	R/W
2.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
2.0.10:7	Reserved	Value always 0, writes ignored	R/W
2.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
2.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.2.1.1 Reset (2.0.15)

Resetting a WIS is accomplished by setting bit 2.0.15 to a one. This action shall set all WIS registers to their default states. As a consequence, this action may change the internal state of the WIS and the state of the

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physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a WIS shall return a value of one in bit 2.0.15 when a reset is in progress and a value of zero otherwise. A WIS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 2.0.15. During a reset, a WIS shall respond to reads from register bits 2.0.15 and 2.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.2.1.2 Loopback (2.0.14)

The WIS shall be placed in a Loopback mode of operation when bit 2.0.14 is set to a one. When bit 2.0.14 is set to a one, the WIS shall ignore all data presented to it by the PMA sublayer. When bit 2.0.14 is set to a one, the WIS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the detailed behavior of the WIS during loopback is specified in 50.3.9

The default value of bit 2.0.14 is zero.

NOTE—The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the WIS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.2.1.3 Low power (2.0.11)

A WIS may be placed into a low-power mode by setting bit 2.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the WIS. The behavior of the WIS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 2.0.11 is zero.

45.2.2.1.4 Speed selection (2.0.13, 2.0.6, and 2.0.5:2)

Speed selection bits 2.0.13 and 2.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the WIS may be selected using bits 5 through 2. The speed abilities of the WIS are advertised in the WIS speed ability register. A WIS may ignore writes to the WIS speed selection bits that select speeds it has not advertised in the WIS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The WIS speed selection defaults to a supported ability.

45.2.2.2 WIS status 1 register (Register 2.1)

The assignment of bits in the WIS status 1 register is shown in Table 45–13. All the bits in the WIS status 1 register are read only; a write to the WIS status 1 register shall have no effect.

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Table 45–13—WIS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.1.15:8	Reserved	Ignore when read	RO
2.1.7	Fault	1 = Fault condition 0 = No fault condition	RO/LH
2.1.6:3	Reserved	Ignore when read	RO
2.1.2	Link status	1 = WIS link up 0 = WIS link down	RO/LL
2.1.1	Low-power ability	1 = WIS supports low-power mode 0 = WIS does not support low-power mode	RO
2.1.1:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High, LL = Latching Low

45.2.2.2.1 Fault (2.1.7)

When read as a one, bit 2.1.7 indicates that the WIS has detected a fault condition. When read as a zero, bit 2.1.7 indicates that the WIS has not detected a fault condition. The fault bit shall be implemented with latching high behavior.

The default value of bit 2.1.7 is zero.

45.2.2.2.2 Link status (2.1.2)

When read as a one, bit 2.1.2 indicates that the WIS receive link is up. When read as a zero, bit 2.1.2 indicates that the WIS receive link is down. The link status bit shall be implemented with latching low behavior.

45.2.2.2.3 Low-power ability (2.1.1)

When read as a one, bit 2.1.1 indicates that the WIS supports the low-power feature. When read as a zero, bit 2.1.1 indicates that the WIS does not support the low-power feature. If a WIS supports the low-power feature, then it is controlled using the low-power bit in the WIS control register.

45.2.2.3 WIS device identifier (Registers 2.2 and 2.3)

Registers 2.2 and 2.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of WIS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS device identifier.

The format of the WIS device identifier is specified in 22.2.4.3.1.

45.2.2.4 WIS speed ability (Register 2.4)

The assignment of bits in the WIS speed ability register is shown in Table 45–14.

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Table 45–14— WIS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
2.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
2.4.0	10G capable	1 = WIS is capable of operating at 10 Gb/s 0 = WIS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.2.4.1 10G capable (2.4.0)

When read as a one, bit 2.4.0 indicates that the WIS is able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate). When read as a zero, bit 2.4.0 indicates that the WIS is not able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate).

45.2.2.5 WIS devices in package (Registers 2.5 and 2.6)

The assignment of bits in the WIS devices in package registers is shown in Table 45–15.

Table 45–15— WIS devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
2.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
2.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
2.6.13:0	Reserved	Ignore on read	RO
2.5.15:6	Reserved	Ignore on read	RO
2.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
2.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
2.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
2.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
2.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
2.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

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When read as a one, a bit in the WIS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the WIS devices in package registers. Bit 2.5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.2.6 10G WIS control 2 register (Register 2.7)

The assignment of bits in the 10G WIS control 2 register is shown in Table 45–16. The default value for each bit of the 10G WIS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–16—10G WIS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.7.15:6	Reserved	Value always 0, writes ignored	R/W
2.7.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
2.7.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
2.7.3	Test-pattern selection	1 = Select square wave test pattern 0 = Select mixed-frequency test pattern	R/W
2.7.2	Receive test-pattern enable	1 = Enable test-pattern mode on the receive path 0 = Disable test-pattern mode on the receive path	R/W
2.7.1	Transmit test-pattern enable	1 = Enable test-pattern mode on the transmit path 0 = Disable test-pattern mode on the transmit path	R/W
2.7.0	PCS type selection	1 = Select 10GBASE-W PCS type 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

45.2.2.6.1 PRBS31 receive test-pattern enable (2.7.5)

If the WIS supports the optional PRBS31 (see 49.2.8) pattern testing advertised in bit 2.8.1 and the mandatory receive test-pattern enable bit (2.7.2) is not one, setting bit 2.7.5 to a one shall set the receive path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2

45.2.2.6.2 PRBS31 transmit test-pattern enable (2.7.4)

If the WIS supports the optional PRBS31 pattern testing advertised in bit 2.8.1 and the mandatory transmit test-pattern enable bit (2.7.1) is not one, then setting bit 2.7.4 to a one shall set the transmit path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2

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45.2.2.6.3 Test-pattern selection (2.7.3)

Bit 2.7.3 controls the type of pattern sent by the transmitter when in test-pattern mode. Setting bit 2.7.3 to a one shall select the square wave test pattern. Setting bit 2.7.3 to a zero shall select the mixed-frequency test pattern. The details of the test patterns are specified in Clause 50.

45.2.2.6.4 Receive test-pattern enable (2.7.2)

Setting bit 2.7.2 to a one shall set the receive path of the WIS into the test-pattern mode. Setting bit 2.7.2 to a zero shall disable the test-pattern mode on the receive path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

45.2.2.6.5 Transmit test-pattern enable (2.7.1)

Setting bit 2.7.1 to a one shall set the transmit path of the WIS into the test-pattern mode. Setting bit 2.7.1 to a zero shall disable the test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in test-pattern mode is specified in Clause 50.

45.2.2.6.6 PCS type selection (2.7.0)

Setting bit 2.7.0 to a one shall enable the 10GBASE-W logic and set the speed of the WIS-PMA interface to 9.95328 Gb/s. Setting bit 2.7.0 to a zero shall disable the 10GBASE-W logic, set the speed of the PCS-PMA interface to 10.3125 Gb/s and bypass the data around the 10GBASE-W logic. A WIS that is only capable of supporting 10GBASE-W operation and is unable to support 10GBASE-R operation shall ignore values written to this bit and shall return a value of one when read. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

45.2.2.7 10G WIS status 2 register (Register 2.8)

The assignment of bits in the 10G WIS status 2 register is shown in Table 45–17. All the bits in the 10G WIS status 2 register are read only; a write to the 10G WIS status 2 register shall have no effect.

Table 45–17—10G WIS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
2.8.13:2	Reserved	Ignore when read	RO
2.8.1	PRBS31 pattern testing ability	1 = WIS is able to support PRBS31 pattern testing 0 = WIS is not able to support PRBS31 pattern testing	RO
2.8.0	10GBASE-R ability	1 = WIS is able to support 10GBASE-R port types 0 = WIS is not able to support 10GBASE-R port types	RO

[a]RO = Read Only

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45.2.2.7.1 Device present (2.8.15:14)

When read as <10>, bits 2.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 2.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.2.7.2 PRBS31 pattern testing ability (2.8.1)

When read as a one, bit 2.8.1 indicates that the WIS is able to support PRBS31 pattern testing. When read as a zero, bit 2.8.1 indicates that the WIS is not able to support PRBS31 pattern testing. If the WIS is able to support PRBS31 pattern testing, then the pattern generation and checking is controlled using bits 2.7.5:4.

45.2.2.7.3 10GBASE-R ability (2.8.0)

When read as a one, bit 2.8.0 indicates that the WIS is able to bypass the WIS logic and adjust the XSBI interface speed to support 10GBASE-R port types. When read as a zero, bit 2.8.0 indicates that the WIS is not able to bypass the WIS logic and cannot support 10GBASE-R port types.

45.2.2.8 10G WIS test-pattern error counter register (Register 2.9)

The assignment of bits in the 10G WIS test-pattern error counter register is shown in Table 45–18. This register is only required when the PRBS31 pattern generation capability is supported.

Table 45–18—10G WIS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
2.9.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the WIS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.8.

45.2.2.9 WIS package identifier (Registers 2.14 and 2.15)

Registers 2.14 and 2.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the WIS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the WIS package identifier is specified in 22.2.4.3.1.

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45.2.2.10 10G WIS status 3 register (Register 2.33)

The assignment of bits in the 10G WIS status 3 register is shown in Table 45–19. All the bits in the 10G WIS status 3 register are read only; a write to the 10G WIS status 3 register shall have no effect.

Table 45–19—10G WIS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.33.15:12	Reserved	Ignore when read	RO
2.33.11	SEF	Severely errored frame	RO/LH
2.33.10	Far end PLM-P/LCD-P	1 = Far end path label mismatch / Loss of code-group delineation 0 = No far end path label mismatch / Loss of code-group delineation	RO/LH
2.33.9	Far end AIS-P/LOP-P	1 = Far end path alarm indication signal / Path loss of pointer 0 = No far end path alarm indication signal / Path loss of pointer	RO/LH
2.33.8	Reserved	Ignore when read	RO
2.33.7	LOF	1 = Loss of frame flag raised 0 = Loss of frame flag lowered	RO/LH
2.33.6	LOS	1 = Loss of signal flag raised 0 = Loss of signal flag lowered	RO/LH
2.33.5	RDI-L	1 = Line remote defect flag raised 0 = Line remote defect flag lowered	RO/LH
2.33.4	AIS-L	1 = Line alarm indication flag raised 0 = Line alarm indication flag lowered	RO/LH
2.33.3	LCD-P	1 = Path loss of code-group delineation flag raised 0 = Path loss of code-group delineation flag lowered	RO/LH
2.33.2	PLM-P	1 = Path label mismatch flag raised 0 = Path label mismatch flag lowered	RO/LH
2.33.1	AIS-P	1 = Path alarm indication signal raised 0 = Path alarm indication signal lowered	RO/LH
2.33.0	LOP-P	1 = Loss of pointer flag raised 0 = Loss of pointer flag lowered	RO/LH

[a]RO = Read Only, LH = Latching High

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45.2.2.10.1 SEF (2.33.11)

When read as a one, bit 2.33.11 indicates that the SEF flag has been raised by the WIS. When read as a zero, bit 2.33.11 indicates that the SEF flag is lowered. The SEF bit shall be implemented with latching high behavior.

The SEF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.2 Far end PLM-P/LCD-P (2.33.10)

When read as a one, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag is lowered. The far end PLM-P/LCD-P bit shall be implemented with latching high behavior.

The far end path label mismatch/loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.3 Far end AIS-P/LOP-P (2.33.9)

When read as a one, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag has been raised by the WIS. When read as a zero, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag is lowered. The far end AIS-P/LOP-P bit shall be implemented with latching high behavior.

The far end path alarm indication signal/path loss of pointer functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.4 LOF (2.33.7)

When read as a one, bit 2.33.7 indicates that the loss of frame flag has been raised. When read as a zero, bit 2.33.7 indicates that the loss of frame flag is lowered. The LOF bit shall be implemented with latching high behavior.

The LOF functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.5 LOS (2.33.6)

When read as a one, bit 2.33.6 indicates that the loss of signal flag has been raised. When read as a zero, bit 2.33.6 indicates that the loss of signal flag is lowered. The LOS bit shall be implemented with latching high behavior.

The LOS functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.6 RDI-L (2.33.5)

When read as a one, bit 2.33.5 indicates that the line remote defect flag has been raised. When read as a zero, bit 2.33.5 indicates that the line remote defect flag is lowered. The RDI-L bit shall be implemented with latching high behavior.

The RDI-L functionality implemented by the WIS is described in 50.3.2.5.

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45.2.2.10.7 AIS-L (2.33.4)

When read as a one, bit 2.33.4 indicates that the line alarm indication flag has been raised. When read as a zero, bit 2.33.4 indicates that the line alarm indication flag is lowered. The AIS-L bit shall be implemented with latching high behavior.

The AIS-L functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.8 LCD-P (2.33.3)

When read as a one, bit 2.33.3 indicates that the loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.3 indicates that the loss of code-group delineation flag is lowered. The LCD-P bit shall be implemented with latching high behavior.

The loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.9 PLM-P (2.33.2)

When read as a one, bit 2.33.2 indicates that the path label mismatch flag has been raised. When read as a zero, bit 2.33.2 indicates that the path label mismatch flag is lowered. The PLM-P bit shall be implemented with latching high behavior.

The PLM-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.10 AIS-P (2.33.1)

When read as a one, bit 2.33.1 indicates that the path alarm indication signal has been raised. When read as a zero, bit 2.33.1 indicates that the path alarm indication signal is lowered. The AIS-P bit shall be implemented with latching high behavior.

The path alarm indication signal functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.10.11 LOP-P (2.33.0)

When read as a one, bit 2.33.0 indicates that the loss of pointer flag has been raised. When read as a zero, bit 2.33.0 indicates that the loss of pointer flag is lowered. The LOP-P bit shall be implemented with latching high behavior.

The LOP-P functionality implemented by the WIS is described in 50.3.2.5.

45.2.2.11 10G WIS far end path block error count (Register 2.37)

The assignment of bits in the 10G WIS far end path block error count register is shown in Table 45–20.

Table 45–20—10G WIS far end path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.37.15:0	Far end path block error count	Far end path block error count	RO

[a]RO = Read Only,

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The 10G WIS far end path block error count is incremented by one whenever a far end path block error, defined in Annex 50A, is detected as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.12 10G WIS J1 transmit (Registers 2.39 through 2.46)

The assignment of octets in the 10G WIS J1 transmit registers is shown in Table 45–21.

Table 45–21—10G WIS J1 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.46.15:8	J1 transmit 15	Transmitted path trace octet 15	R/W
2.46.7:0	J1 transmit 14	Transmitted path trace octet 14	R/W
2.45.15:8	J1 transmit 13	Transmitted path trace octet 13	R/W
2.45.7:0	J1 transmit 12	Transmitted path trace octet 12	R/W
2.44.15:8	J1 transmit 11	Transmitted path trace octet 11	R/W
2.44.7:0	J1 transmit 10	Transmitted path trace octet 10	R/W
2.43.15:8	J1 transmit 9	Transmitted path trace octet 9	R/W
2.43.7:0	J1 transmit 8	Transmitted path trace octet 8	R/W
2.42.15:8	J1 transmit 7	Transmitted path trace octet 7	R/W
2.42.7:0	J1 transmit 6	Transmitted path trace octet 6	R/W
2.41.15:8	J1 transmit 5	Transmitted path trace octet 5	R/W
2.41.7:0	J1 transmit 4	Transmitted path trace octet 4	R/W
2.40.15:8	J1 transmit 3	Transmitted path trace octet 3	R/W
2.40.7:0	J1 transmit 2	Transmitted path trace octet 2	R/W
2.39.15:8	J1 transmit 1	Transmitted path trace octet 1	R/W
2.39.7:0	J1 transmit 0	Transmitted path trace octet 0	R/W

[a]R/W = Read/Write

The first transmitted path trace octet is J1 transmit 15, which contains the delineation octet. The default value for the J1 transmit 15 octet is 137 (hexadecimal 89). The last transmitted path trace octet is J1 transmit 0. The default value for the J1 transmit 0 through 14 octets is 0. The transmitted path trace is described in 50.3.2.1.

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45.2.2.13 10G WIS J1 receive (Registers 2.47 through 2.54)

The assignment of octets in the 10G WIS J1 receive registers is shown in Table 45–22.

Table 45–22—10G WIS J1 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.54.15:8	J1 receive 15	Received path trace octet 15	RO
2.54.7:0	J1 receive 14	Received path trace octet 14	RO
2.53.15:8	J1 receive 13	Received path trace octet 13	RO
2.53.7:0	J1 receive 12	Received path trace octet 12	RO
2.52.15:8	J1 receive 11	Received path trace octet 11	RO
2.52.7:0	J1 receive 10	Received path trace octet 10	RO
2.51.15:8	J1 receive 9	Received path trace octet 9	RO
2.51.7:0	J1 receive 8	Received path trace octet 8	RO
2.50.15:8	J1 receive 7	Received path trace octet 7	RO
2.50.7:0	J1 receive 6	Received path trace octet 6	RO
2.49.15:8	J1 receive 5	Received path trace octet 5	RO
2.49.7:0	J1 receive 4	Received path trace octet 4	RO
2.48.15:8	J1 receive 3	Received path trace octet 3	RO
2.48.7:0	J1 receive 2	Received path trace octet 2	RO
2.47.15:8	J1 receive 1	Received path trace octet 1	RO
2.47.7:0	J1 receive 0	Received path trace octet 0	RO

[a]RO = Read Only

The first received path trace octet is J1 receive 15. The last received path trace octet is J1 receive 0. The received path trace is described in 50.3.2.4.

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45.2.2.14 10G WIS far end line BIP errors (Registers 2.55 and 2.56)

The assignment of octets in the 10G WIS far end line BIP errors registers is shown in Table 45–23.

Table 45–23—10G WIS far end line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.56.15:0	WIS far end line BIP errors 0	Least significant word of the WIS far end line BIP errors counter	RO
2.55.15:0	WIS far end line BIP errors 1	Most significant word of the WIS far end line BIP errors counter	RO

[a]RO = Read Only

The 10G WIS far end line BIP Errors register pair reflects the contents of the far end line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of far end line BIP errors reported by the far end, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.55) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.55 and the least significant 16 bits appearing in 2.56, the value being latched before the contents of 2.55 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.56 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

45.2.2.15 10G WIS line BIP errors (Registers 2.57 and 2.58)

The assignment of octets in the 10G WIS line BIP errors registers is shown in Table 45–24.

Table 45–24—10G WIS line BIP errors 0–1 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.58.15:0	WIS line BIP errors 0	Least significant word of the WIS line BIP errors counter	RO
2.57.15:0	WIS line BIP errors 1	Most significant word of the WIS line BIP errors counter	RO

[a]RO = Read Only

The 10G WIS line BIP errors register pair reflects the contents of the line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of line BIP errors detected on the incoming data stream, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.57) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.57 and the least significant 16 bits appearing in 2.58, the value being latched before the contents of 2.57 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.58 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

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45.2.2.16 10G WIS path block error count (Register 2.59)

The assignment of bits in the 10G WIS path block error count register is shown in Table 45–25.

Table 45–25—10G WIS path block error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.59.15:0	Path block error count	Path block error counter	RO

[a]RO = Read Only

45.2.2.16.1 Path block error count (2.59.15:0)

The path block error count is incremented by one whenever a B3 parity error (defined in Annex 50A) is detected, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.17 10G WIS section BIP error count (Register 2.60)

The assignment of bits in the 10G WIS section BIP error count register is shown in Table 45–26.

Table 45–26—10G WIS section BIP error count register bit definitions

Bit(s)	Name	Description	R/W[a]
2.60.15:0	Section BIP error count	Section BIP error count	RO

[a]RO = Read Only

45.2.2.17.1 Section BIP error count (2.60.15:0)

The section BIP error count is incremented by the number of section BIP errors detected within each WIS frame, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

45.2.2.18 10G WIS J0 transmit (Registers 2.64 through 2.71)

The assignment of octets in the 10G WIS J0 transmit registers is shown in Table 45–27.

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Table 45–27—10G WIS J0 transmit 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.71.15:8	J0 transmit 15	Transmitted section trace octet 15	R/W
2.71.7:0	J0 transmit 14	Transmitted section trace octet 14	R/W
2.70.15:8	J0 transmit 13	Transmitted section trace octet 13	R/W
2.70.7:0	J0 transmit 12	Transmitted section trace octet 12	R/W
2.69.15:8	J0 transmit 11	Transmitted section trace octet 11	R/W
2.69.7:0	J0 transmit 10	Transmitted section trace octet 10	R/W
2.68.15:8	J0 transmit 9	Transmitted section trace octet 9	R/W
2.68.7:0	J0 transmit 8	Transmitted section trace octet 8	R/W
2.67.15:8	J0 transmit 7	Transmitted section trace octet 7	R/W
2.67.7:0	J0 transmit 6	Transmitted section trace octet 6	R/W
2.66.15:8	J0 transmit 5	Transmitted section trace octet 5	R/W
2.66.7:0	J0 transmit 4	Transmitted section trace octet 4	R/W
2.65.15:8	J0 transmit 3	Transmitted section trace octet 3	R/W
2.65.7:0	J0 transmit 2	Transmitted section trace octet 2	R/W
2.64.15:8	J0 transmit 1	Transmitted section trace octet 1	R/W
2.64.7:0	J0 transmit 0	Transmitted section trace octet 0	R/W

[a]R/W = Read/Write

The J0 transmit octets allow a receiver to verify its continued connection to the WIS transmitter. The first transmitted section trace octet is J0 transmit 15, which contains the delineation octet. The default value for the J0 transmit 15 octet is 137 (hexadecimal 89). The last transmitted section trace octet is J0 transmit 0. The default value for the J0 transmit 0 through 14 octets is 0. The transmitted section trace is described in 50.3.2.3.

45.2.2.19 10G WIS J0 receive (Registers 2.72 through 2.79)

The assignment of octets in the 10G WIS J0 receive registers is shown in Table 45–28.

The first received section trace octet is J0 receive 15. The last received section trace octet is J0 receive 0. The J0 receive octets allow a WIS receiver to verify its continued connection to the intended transmitter. The received section trace is described in 50.3.2.4.

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Table 45–28— 10G WIS J0 receive 0–15 register bit definitions

Bit(s)	Name	Description	R/W[a]
2.79.15:8	J0 receive 15	Received section trace octet 15	RO
2.79.7:0	J0 receive 14	Received section trace octet 14	RO
2.78.15:8	J0 receive 13	Received section trace octet 13	RO
2.78.7:0	J0 receive 12	Received section trace octet 12	RO
2.77.15:8	J0 receive 11	Received section trace octet 11	RO
2.77.7:0	J0 receive 10	Received section trace octet 10	RO
2.76.15:8	J0 receive 9	Received section trace octet 9	RO
2.76.7:0	J0 receive 8	Received section trace octet 8	RO
2.75.15:8	J0 receive 7	Received section trace octet 7	RO
2.75.7:0	J0 receive 6	Received section trace octet 6	RO
2.74.15:8	J0 receive 5	Received section trace octet 5	RO
2.74.7:0	J0 receive 4	Received section trace octet 4	RO
2.73.15:8	J0 receive 3	Received section trace octet 3	RO
2.73.7:0	J0 receive 2	Received section trace octet 2	RO
2.72.15:8	J0 receive 1	Received section trace octet 1	RO
2.72.7:0	J0 receive 0	Received section trace octet 0	RO

[a]RO = Read Only

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45.2.3 PCS registers

The assignment of registers in the PCS is shown in Table 45–29.

Table 45–29—PCS registers

Register address	Register name
3.0	PCS control 1
3.1	PCS status 1
3.2, 3.3	PCS device identifier
3.4	PCS speed ability
3.5, 3.6	PCS devices in package
3.7	10G PCS control 2
3.8	10G PCS status 2
3.9 through 3.13	Reserved
3.14, 3.15	PCS package identifier
3.16 through 23	Reserved
3.24	10GBASE-X PCS status
3.25	10GBASE-X PCS test control
3.26 through 31	Reserved
3.32	10GBASE-R PCS status 1
3.33	10GBASE-R PCS status 2
3.34 through 37	10GBASE-R PCS test pattern seed A
3.38 through 41	10GBASE-R PCS test pattern seed B
3.42	10GBASE-R PCS test pattern control
3.43	10GBASE-R PCS test pattern error counter
3.44 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

45.2.3.1 PCS control 1 register (Register 3.0)

The assignment of bits in the PCS control 1 register is shown in Table 45–30. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–30—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
3.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
3.0.12	Reserved	Value always 0, writes ignored	R/W
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10:7	Reserved	Value always 0, writes ignored	R/W
3.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.3.1.1 Reset (3.0.15)

Resetting a PCS is accomplished by setting bit 3.0.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 3.0.15 when a reset is in progress and a value of zero otherwise. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 3.0.15. During a reset, a PCS shall respond to reads from register bits 3.0.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.3.1.2 Loopback (3.0.14)

The 10GBASE-R PCS shall be placed in a Loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. For all other port types when operating at 10 Gb/s, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

The default value of bit 3.0.14 is zero.

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NOTE—The signal path through the PCS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PCS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.3.1.3 Low power (3.0.11)

A PCS may be placed into a low-power mode by setting bit 3.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PCS. The behavior of the PCS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 3.0.11 is zero.

45.2.3.1.4 Speed selection (3.0.13, 3.0.6, 3.0.5:2)

Speed selection bits 3.0.13 and 3.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are advertised in the PCS speed ability register. A PCS may ignore writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PCS speed selection defaults to a supported ability.

45.2.3.2 PCS status 1 register (Register 3.1)

The assignment of bits in the PCS status 1 register is shown in Table 45–31. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

Table 45–31—PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.1.15:8	Reserved	Ignore when read	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6:3	Reserved	Ignore when read	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

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45.2.3.2.1 Fault (3.1.7)

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition. For 10 Gb/s operation, bit 3.1.7 is read as a one when either of the fault bits (3.8.11, 3.8.10) located in register 3.8 are read as a one.

45.2.3.2.2 PCS receive link status (3.1.2)

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10GBASE-R or 10GBASE-W mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

45.2.3.2.3 Low-power ability (3.1.1)

When read as a one, bit 3.1.1 indicates that the PCS supports the low-power feature. When read as a zero, bit 3.1.1 indicates that the PCS does not support the low-power feature. If a PCS supports the low-power feature then it is controlled using the low-power bit 3.0.11.

45.2.3.3 PCS device identifier (Registers 3.2 and 3.3)

Registers 3.2 and 3.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PCS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS device identifier.

The format of the PCS device identifier is specified in 22.2.4.3.1.

45.2.3.4 PCS speed ability (Register 3.4)

The assignment of bits in the PCS speed ability register is shown in Table 45–32.

Table 45–32—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
3.4.0	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.3.4.1 10G capable (3.4.0)

When read as a one, bit 3.4.0 indicates that the PCS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 3.4.0 indicates that the PCS is not able to operate at a data rate of 10 Gb/s.

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45.2.3.5 PCS devices in package (Registers 3.5 and 3.6)

The assignment of bits in the PCS devices in package registers is shown in Table 45–33.

Table 45–33—PCS devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
3.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
3.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
3.6.13:0	Reserved	Ignore on read	RO
3.5.15:6	Reserved	Ignore on read	RO
3.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
3.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
3.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
3.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
3.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
3.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

When read as a one, a bit in the PCS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PCS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.3.6 10G PCS control 2 register (Register 3.7)

The assignment of bits in the 10G PCS control 2 register is shown in Table 45–34. The default value for each bit of the 10G PCS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.3.6.1 PCS type selection (3.7.1:0)

The PCS type shall be selected using bits 1 through 0. The PCS type abilities of the 10G PCS are advertised in bits 3.8.2:0. A 10G PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable

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Table 45–34—10G PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:2	Reserved	Value always 0, writes ignored	R/W
3.7.1:0	PCS type selection	1 0 1 1 = Reserved 1 0 = Select 10GBASE-W PCS type 0 1 = Select 10GBASE-X PCS type 0 0 = Select 10GBASE-R PCS type	R/W

[a]R/W = Read/Write

MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

45.2.3.7 10G PCS status 2 register (Register 3.8)

The assignment of bits in the 10G PCS status 2 register is shown in Table 45–35. All the bits in the 10G PCS status 2 register are read only; a write to the 10G PCS status 2 register shall have no effect.

Table 45–35—10G PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
3.8.13:12	Reserved	Ignore when read	RO
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/LH
3.8.9:3	Reserved	Ignore when read	RO
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO

[a]RO = Read Only, LH = Latching High

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45.2.3.7.1 Device present (3.8.15:14)

When read as <10>, bits 3.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 3.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

45.2.3.7.2 Transmit fault (3.8.11)

When read as a one, bit 3.8.11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 3.8.11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.11 is zero.

45.2.3.7.3 Receive fault (3.8.10)

When read as a one, bit 3.8.10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 3.8.10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.10 is zero.

45.2.3.7.4 10GBASE-W capable (3.8.2)

When read as a one, bit 3.8.2 indicates that the 64B/66B PCS is able to support operation in a 10GBASE-W PHY (that is, supports operation with a WIS). When read as a zero, bit 3.8.2 indicates that the 64B/66B PCS is not able to support operation with a WIS in a 10GBASE-W PHY.

NOTE—This bit does not indicate that the PCS is performing the functionality contained in the WIS. This bit indicates whether the 64B/66B PCS would be able to support a WIS if it were to be attached.

45.2.3.7.5 10GBASE-X capable (3.8.1)

When read as a one, bit 3.8.1 indicates that the PCS is able to support the 10GBASE-X PCS type. When read as a zero, bit 3.8.1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

45.2.3.7.6 10GBASE-R capable (3.8.0)

When read as a one, bit 3.8.0 indicates that the PCS is able to support operation in a 10GBASE-R PHY. When read as a zero, bit 3.8.0 indicates that the PCS is not able to support operation in a 10GBASE-R PHY.

45.2.3.8 PCS package identifier (Registers 3.14 and 3.15)

Registers 3.14 and 3.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PCS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

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45.2.3.9 10GBASE-X PCS status register (Register 3.24)

The assignment of bits in the 10GBASE-X PCS status register is shown in Table 45–36. All the bits in the 10GBASE-X PCS status register are read only; a write to the 10GBASE-X PCS status register shall have no effect. A PCS device that does not implement 10GBASE-X shall return a zero for all bits in the 10GBASE-X PCS status register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

Table 45–36—10GBASE-X PCS status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.24.15:13	Reserved	Ignore when read	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
3.24.10:4	Reserved	Ignore when read	RO
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.3.9.1 10GBASE-X receive lane alignment status (3.24.12)

When read as a one, bit 3.24.12 indicates that the 10GBASE-X PCS has synchronized and aligned all four receive lanes. When read as a zero, bit 3.24.12 indicates that the 10GBASE-X PCS has not synchronized and aligned all four receive lanes.

45.2.3.9.2 Pattern testing ability (3.24.11)

When read as a one, bit 3.24.11 indicates that the 10GBASE-X PCS is able to generate test patterns. When read as a zero, bit 3.24.11 indicates that the 10GBASE-X PCS is not able to generate test patterns. If the 10GBASE-X PCS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 3.25.

45.2.3.9.3 Lane 3 sync (3.24.3)

When read as a one, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is synchronized. When read as a zero, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is not synchronized.

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45.2.3.9.4 Lane 2 sync (3.24.2)

When read as a one, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is synchronized. When read as a zero, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is not synchronized.

45.2.3.9.5 Lane 1 sync (3.24.1)

When read as a one, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is synchronized. When read as a zero, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is not synchronized.

45.2.3.9.6 Lane 0 sync (3.24.0)

When read as a one, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is synchronized. When read as a zero, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is not synchronized.

45.2.3.10 10GBASE-X PCS test control register (Register 3.25)

The assignment of bits in the 10GBASE-X PCS test control register is shown in Table 45–36. The default value for each bit of the 10GBASE-X PCS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–37—10GBASE-X PCS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.25.15:3	Reserved	Value always 0, writes ignored	R/W
3.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
3.25.1:0	Test pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.3.10.1 10GBASE-X test-pattern enable (3.25.2)

When bit 3.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 3.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10GBASE-X PCS to generate test patterns is advertised by the pattern testing ability bit in register 3.24. A 10GBASE-X PCS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 3.25.2 is zero.

45.2.3.10.2 10GBASE-X test-pattern select (3.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 3.25.2 is selected using bits 3.25.1:0. When bits 3.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

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45.2.3.11 10GBASE-R PCS status 1 register (Register 3.32)

The assignment of bits in the 10GBASE-R PCS status 1 register is shown in Table 45–38. All the bits in the 10GBASE-R PCS status 1 register are read only; a write to the 10GBASE-R PCS status 1 register shall have no effect. A PCS device that does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.32 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

Table 45–38—10GBASE-R PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.32.15:13	Reserved	Ignore when read	RO
3.32.12	10GBASE-R receive link status	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
3.32.11:3	Reserved	Ignore when read	RO
3.32.2	PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.32.1	10GBASE-R PCS high BER	1 = 10GBASE-R PCS reporting a high BER 0 = 10GBASE-R PCS not reporting a high BER	RO
3.32.0	10GBASE-R PCS block lock	1 = 10GBASE-R PCS locked to received blocks 0 = 10GBASE-R PCS not locked to received blocks	RO

[a]RO = Read Only

45.2.3.11.1 10GBASE-R receive link status (3.32.12)

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the state of the PCS_status variable defined in 49.2.14.1.

45.2.3.11.2 PRBS31 pattern testing ability (3.32.2)

When read as a one, bit 3.32.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.32.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits 3.42.5:4.

45.2.3.11.3 10GBASE-R PCS high BER (3.32.1)

When read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_ber variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

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45.2.3.11.4 10GBASE-R PCS block lock (3.32.0)

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver has not got block lock. This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

45.2.3.12 10GBASE-R PCS status 2 register (Register 3.33)

The assignment of bits in the 10GBASE-R PCS status 2 register is shown in Table 45–39. All the bits in the 10GBASE-R PCS status 2 register are read only; a write to the 10GBASE-R PCS status 2 register shall have no effect. A PCS device which does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

Table 45–39—10GBASE-R PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.33.15	Latched block lock	1 = 10GBASE-R PCS has block lock 0 = 10GBASE-R PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = 10GBASE-R PCS has reported a high BER 0 = 10GBASE-R PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read Only, LL = Latching Low, LH = Latching High, NR = Non Roll-over

45.2.3.12.1 Latched block lock (3.33.15)

When read as a one, bit 3.33.15 indicates that the 10GBASE-R PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 10GBASE-R PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10GBASE-R PCS block lock status bit (3.32.0).

45.2.3.12.2 Latched high BER (3.33.14)

When read as a one, bit 3.33.14 indicates that the 10GBASE-R PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 10GBASE-R PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-R PCS high BER status bit (3.32.1).

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45.2.3.12.3 BER(3.33.13:8)

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2. These bits shall be reset to all zeros when the BER count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.12.4 Errored blocks (3.33.7:0)

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.13 10GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)

The assignment of bits in the 10GBASE-R PCS test pattern seed A registers is shown in Table 45–40. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

Table 45–40—10GBASE-R PCS test pattern seed A 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.37.15:10	Reserved	Value always 0, writes ignored	R/W
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W

[a]R/W = Read/Write

The A seed for the pseudo random test pattern is held in registers 3.34 through 3.37. The test-pattern methodology is described in 49.2.8.

45.2.3.14 10GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)

The assignment of bits in the 10GBASE-R PCS test pattern seed B registers is shown in Table 45–41. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

The B seed for the pseudo random test pattern is held in registers 3.38 through 3.41. The test-pattern methodology is described in 49.2.8.

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Table 45–41—10GBASE-R PCS test pattern seed B 0-3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.41.15:10	Reserved	Value always 0, writes ignored	R/W
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W

[a]R/W = Read/Write

45.2.3.15 10GBASE-R PCS test-pattern control register (Register 3.42)

The assignment of bits in the 10GBASE-R PCS test-pattern control register is shown in Table 45–42. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. The test-pattern methodology is described in 49.2.8.

Table 45–42—10GBASE-R PCS test-pattern control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.42.15:6	Reserved	Value always 0, writes ignored	R/W
3.42.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.42.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W

[a]R/W = Read/Write

45.2.3.15.1 PRBS31 receive test-pattern enable (3.42.5)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.32.2 to a one shall set the receive path of the PCS into

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the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.43. Setting bit 3.32.2 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

45.2.3.15.2 PRBS31 transmit test-pattern enable (3.42.4)

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.42.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

45.2.3.15.3 Transmit test-pattern enable (3.42.3)

When bit 3.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 3.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 3.42.3 is zero.

45.2.3.15.4 Receive test-pattern enable (3.42.2)

When bit 3.42.2 is set to a one, pattern testing is enabled on the receive path. When bit 3.42.2 is set to a zero, pattern testing is disabled on the receive path.

The default value for bit 3.42.2 is zero.

45.2.3.15.5 Test-pattern select (3.42.1)

When bit 3.42.1 is set to a one, the square wave test pattern is used for pattern testing. When bit 3.42.1 is set to a zero, the pseudo random test pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

45.2.3.15.6 Data pattern select (3.42.0)

When bit 3.42.0 is set to a one, the zeros data pattern is used for pattern testing. When bit 3.42.0 is set to a zero, the LF data pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

45.2.3.16 10GBASE-R PCS test-pattern error counter register (Register 3.43)

The assignment of bits in the 10GBASE-R PCS test-pattern error counter register is shown in Table 45–43. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode, or may function as defined for 10GBASE-R.

Table 45–43—10GBASE-R PCS test-pattern error counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.43.15:0	Test-pattern error counter	Error counter	RO

[a]RO = Read Only

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The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.12. This counter will count either block errors or bit errors dependent on the test mode (see 49.2.12).

45.2.4 PHY XS registers

The assignment of registers in the PHY XS is shown in Table 45–44.

Table 45–44—PHY XS registers

Register address	Register name
4.0	PHY XS control 1
4.1	PHY XS status 1
4.2, 4.3	PHY XS device identifier
4.4	PHY XS speed ability
4.5, 4.6	PHY XS devices in package
4.7	Reserved
4.8	PHY XS status 2
4.9 through 4.13	Reserved
4.14, 4.15	PHY XS package identifier
4.16 through 4.23	Reserved
4.24	10G PHY XGXS lane status
4.25	10G PHY XGXS test control
4.26 through 4.32 767	Reserved
4.32 768 through 4.65 535	Vendor specific

45.2.4.1 PHY XS control 1 register (Register 4.0)

The assignment of bits in the PHY XS control 1 register is shown in Table 45–45. The default value for each bit of the PHY XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.4.1.1 Reset (4.0.15)

Resetting a PHY XS is accomplished by setting bit 4.0.15 to a one. This action shall set all PHY XS registers to their default states. As a consequence, this action may change the internal state of the PHY XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the

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Table 45–45—PHY XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.0.15	Reset	1 = PHY XS reset 0 = Normal operation	R/W SC
4.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
4.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.12	Reserved	Value always 0, writes ignored	R/W
4.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
4.0.10:7	Reserved	Value always 0, writes ignored	R/W
4.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
4.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

same package. This bit is self-clearing, and a PHY XS shall return a value of one in bit 4.0.15 when a reset is in progress and a value of zero otherwise. A PHY XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 4.0.15. During a reset, a PHY XS shall respond to reads from register bits 4.0.15 and 4.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.4.1.2 Loopback (4.0.14)

The PHY XS shall be placed in a Loopback mode of operation when bit 4.0.14 is set to a one. When bit 4.0.14 is set to a one, the PHY XS shall accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other MMD loopbacks.

The loopback function is optional. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PHY XS that is unable to perform the loopback function shall ignore writes to this bit and return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and the loopback ability bit is specified in the 10G PHY XGXS Lane status register.

The default value of bit 4.0.14 is zero.

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NOTE—The signal path through the PHY XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY XS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.4.1.3 Low power (4.0.11)

A PHY XS may be placed into a low-power mode by setting bit 4.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PHY XS. The behavior of the PHY XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 4.0.11 is zero.

45.2.4.1.4 Speed selection (4.0.13, 4.0.6, 4.0.5:2)

Speed selection bits 4.0.13 and 4.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PHY XS speed selection defaults to a supported ability.

45.2.4.2 PHY XS status 1 register (Register 4.1)

The assignment of bits in the PHY XS status 1 register is shown in Table 45–46. All the bits in the PHY XS status 1 register are read only; a write to the PHY XS status 1 register shall have no effect.

Table 45–46—PHY XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.1.15:8	Reserved	Ignore when read	RO
4.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
4.1.6:3	Reserved	Ignore when read	RO
4.1.2	PHY XS transmit link status	1 = The PHY XS transmit link is up 0 = The PHY XS transmit link is down	RO/LL
4.1.1	Low-power ability	1 = PHY XS supports low-power mode 0 = PHY XS does not support low-power mode	RO
4.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

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45.2.4.2.1 Fault (4.1.7)

When read as a one, bit 4.1.7 indicates that the PHY XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 4.1.7 indicates that the PHY XS has not detected a fault condition. Bit 4.1.7 is set to a one when either of the fault bits (4.8.11, 4.8.10) located in register 4.8 are set to a one.

45.2.4.2.2 PHY XS transmit link status (4.1.2)

When read as a one, bit 4.1.2 indicates that the PHY XS transmit link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS transmit link is not aligned. The transmit link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, bit 4.1.2 is a latching low version of bit 4.24.12.

45.2.4.2.3 Low-power ability (4.1.1)

When read as a one, bit 4.1.1 indicates that the PHY XS supports the low-power feature. When read as a zero, bit 4.1.1 indicates that the PHY XS does not support the low-power feature. If a PHY XS supports the low-power feature then it is controlled using the low-power bit in the PHY XS control register.

45.2.4.3 PHY XS device identifier (Registers 4.2 and 4.3)

Registers 4.2 and 4.3 provide a 32-bit value, which may constitute a unique identifier for a PHY XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS device identifier.

The format of the PHY XS device identifier is specified in 22.2.4.3.1.

45.2.4.4 PHY XS speed ability (Register 4.4)

The assignment of bits in the PHY XS speed ability register is shown in Table 45–47.

Table 45–47—PHY XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
4.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
4.4.0	10G capable	1 = PHY XS is capable of operating at 10 Gb/s 0 = PHY XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.4.4.1 10G capable (4.4.0)

When read as a one, bit 4.4.0 indicates that the PHY XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 4.4.0 indicates that the PHY-XS is not able to operate at a data rate of 10 Gb/s.

45.2.4.5 PHY XS devices in package (Registers 4.5 and 4.6)

The assignment of bits in the PHY XS devices in package registers is shown in Table 45–48.

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Table 45–48—PHY XS devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
4.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
4.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
4.6.13:0	Reserved	Ignore on read	RO
4.5.15:6	Reserved	Ignore on read	RO
4.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
4.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
4.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
4.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
4.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
4.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

When read as a one, a bit in the PHY XS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PHY XS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.4.6 PHY XS status 2 register (Register 4.8)

The assignment of bits in the PHY XS status 2 register is shown in Table 45–49. All the bits in the PHY XS status 2 register are read only; a write to the PHY XS status 2 register shall have no effect.

45.2.4.6.1 Device present (4.8.15:14)

When read as <10>, bits 4.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 4.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.4.6.2 Transmit fault (4.8.11)

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

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Table 45–49—PHY XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
4.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
4.8.13:12	Reserved	Ignore when read	RO
4.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
4.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

The default value for bit 4.8.11 is zero.

45.2.4.6.3 Receive fault (4.8.10)

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 4.8.10 is zero.

45.2.4.7 PHY XS package identifier (Registers 4.14 and 4.15)

Registers 4.14 and 4.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PHY XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the PHY XS package identifier is specified in 22.2.4.3.1.

45.2.4.8 10G PHY XGXS lane status register (Register 4.24)

The assignment of bits in the 10G PHY XGXS lane status register is shown in Table 45–50. All the bits in the 10G PHY XGXS lane status register are read only; a write to the 10G PHY XGXS lane status register shall have no effect.

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Table 45–50—10G PHY XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
4.24.15:13	Reserved	Ignore when read	RO
4.24.12	PHY XGXS lane alignment status	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO
4.24.10	PHY XGXS loopback ability	1 = PHY XGXS has the ability to perform a loopback function 0 = PHY XGXS does not have the ability to perform a loopback function	RO
4.24.9:4	Reserved	Ignore when read	RO
4.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.4.8.1 PHY XGXS transmit lane alignment status (4.24.12)

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four transmit lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four transmit lanes.

45.2.4.8.2 Pattern testing ability (4.24.11)

When read as a one, bit 4.24.11 indicates that the 10G PHY XGXS is able to generate test patterns. When read as a zero, bit 4.24.11 indicates that the 10G PHY XGXS is not able to generate test patterns. If the 10G PHY XGXS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 4.25.

45.2.4.8.3 PHY XS loopback ability (4.24.10)

When read as a one, bit 4.24.10 indicates that the PHY XGXS is able to perform the loopback function. When read as a zero, bit 4.24.10 indicates that the PHY XGXS is not able to perform the loopback function. If a 10G PHY XGXS is able to perform the loopback function, then it is controlled using the PHY XGXS loopback bit 4.0.14.

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45.2.4.8.4 Lane 3 sync (4.24.3)

When read as a one, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is synchronized. When read as a zero, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is not synchronized.

45.2.4.8.5 Lane 2 sync (4.24.2)

When read as a one, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is synchronized. When read as a zero, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is not synchronized.

45.2.4.8.6 Lane 1 sync (4.24.1)

When read as a one, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is synchronized. When read as a zero, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is not synchronized.

45.2.4.8.7 Lane 0 sync (4.24.0)

When read as a one, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is synchronized. When read as a zero, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is not synchronized.

45.2.4.9 10G PHY XGXS test control register (Register 4.25)

The assignment of bits in the 10G PHY XGXS test control register is shown in Table 45–51. The default value for each bit of the 10G PHY XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–51—10G PHY XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
4.25.15:3	Reserved	Value always 0, writes ignored	R/W
4.25.2	Receive test-pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern not enabled	R/W
4.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.4.9.1 10G PHY XGXS test-pattern enable (4.25.2)

When bit 4.25.2 is set to a one, pattern testing is enabled on the receive path. When bit 4.25.2 is set to a zero, pattern testing is disabled on the receive path. Pattern testing is optional, and the ability of the 10G PHY XGXS to generate test patterns is advertised by the pattern testing ability bit in register 4.24. A 10G PHY XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 4.25.2 is zero.

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45.2.4.9.2 10G PHY XGXS test-pattern select (4.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 4.25.2 is selected using bits 4.25.1:0. When bits 4.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

45.2.5 DTE XS registers

The assignment of registers in the DTE XS is shown in Table 45–52.

Table 45–52—DTE XS registers

Register address	Register name
5.0	DTE XS control 1
5.1	DTE XS status 1
5.2, 5.3	DTE XS device identifier
5.4	DTE XS speed ability
5.5, 5.6	DTE XS devices in package
5.7	Reserved
5.8	DTE XS status 2
5.9 through 5.13	Reserved
5.14, 5.15	DTE XS package identifier
5.16 through 5.23	Reserved
5.24	10G DTE XGXS lane status
5.25	10G DTE XGXS test control
5.26 through 5.32 767	Reserved
5.32 768 through 5.65 535	Vendor specific

45.2.5.1 DTE XS control 1 register (Register 5.0)

The assignment of bits in the DTE XS control 1 register is shown in Table 45–53. The default value for each bit of the DTE XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–53—DTE XS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.0.15	Reset	1 = DTE XS reset 0 = Normal operation	R/W SC
5.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
5.0.13	Speed selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	R/W
5.0.12	Reserved	Value always 0, writes ignored	R/W
5.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
5.0.10:7	Reserved	Value always 0, writes ignored	R/W
5.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
5.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
5.0.1:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.5.1.1 Reset (5.0.15)

Resetting a DTE XS is accomplished by setting bit 5.0.15 to a one. This action shall set all DTE XS registers to their default states. As a consequence, this action may change the internal state of the DTE XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a DTE XS shall return a value of one in bit 5.0.15 when a reset is in progress and a value of zero otherwise. A DTE XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 5.0.15. During a reset, a DTE XS shall respond to reads to register bits 5.0.15 and 5.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.5.1.2 Loopback (5.0.14)

The DTE XS shall be placed in a Loopback mode of operation when bit 5.0.14 is set to a one. When bit 5.0.14 is set to a one, the DTE XS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the specific behavior of a DTE XS during loopback is specified in 48.3.3.

The default value of bit 5.0.14 is zero.

NOTE—The signal path through the DTE XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the DTE XS circuitry as is practical. The

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intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

45.2.5.1.3 Low power (5.0.11)

A DTE XS may be placed into a low-power mode by setting bit 5.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the DTE XS. The behavior of the DTE XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 5.0.11 is zero.

45.2.5.1.4 Speed selection (5.0.13, 5.0.6, 5.0.5:2)

Speed selection bits 5.0.13 and 5.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the DTE XS may be selected using bits 5 through 2. The speed abilities of the DTE XS are advertised in the DTE XS speed ability register. A DTE XS may ignore writes to the DTE XS speed selection bits that select speeds it has not advertised in the DTE XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The DTE XS speed selection defaults to a supported ability.

45.2.5.2 DTE XS status 1 register (Register 5.1)

The assignment of bits in the DTE XS status 1 register is shown in Table 45–54. All the bits in the DTE XS status 1 register are read only; a write to the DTE XS status 1 register shall have no effect.

Table 45–54—DTE XS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.1.15:8	Reserved	Ignore when read	RO
5.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
5.1.6:3	Reserved	Ignore when read	RO
5.1.2	DTE XS receive link status	1 = The DTE XS receive link is up 0 = The DTE XS receive link is down	RO/LL
5.1.1	Low-power ability	1 = DTE XS supports low-power mode 0 = DTE XS does not support low-power mode	RO
5.1.0	Reserved	Ignore when read	RO

[a]RO = Read Only, LL = Latching Low

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45.2.5.2.1 Fault (5.1.7)

When read as a one, bit 5.1.7 indicates that the DTE XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 5.1.7 indicates that the DTE XS has not detected a fault condition. Bit 5.1.7 is set to a one when either of the fault bits (5.8.11, 5.8.10) located in register 5.8 are set to a one.

45.2.5.2.2 DTE XS receive link status (5.1.2)

When read as a one, bit 5.1.2 indicates that the DTE XS receive link is aligned. When read as a zero, bit 5.1.2 indicates that the DTE XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, this bit is a latching low version of bit 5.24.12.

45.2.5.2.3 Low-power ability (5.1.1)

When read as a one, bit 5.1.1 indicates that the DTE XS supports the low-power feature. When read as a zero, bit 5.1.1 indicates that the DTE XS does not support the low-power feature. If a DTE XS supports the low-power feature then it is controlled using the low-power bit in the DTE XS control register.

45.2.5.3 DTE XS device identifier (Registers 5.2 and 5.3)

Registers 5.2 and 5.3 provide a 32-bit value, which may constitute a unique identifier for a DTE XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS device identifier.

The format of the DTE XS device identifier is specified in 22.2.4.3.1

45.2.5.4 DTE XS speed ability (Register 5.4)

The assignment of bits in the DTE XS speed ability register is shown in Table 45–55.

Table 45–55— DTE XS speed ability register bit definitions

Bit(s)	Name	Description	R/W[a]
5.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
5.4.0	10G capable	1 = DTE XS is capable of operating at 10 Gb/s 0 = DTE XS is not capable of operating at 10 Gb/s	RO

[a]RO = Read Only

45.2.5.4.1 10G capable (5.4.0)

When read as a one, bit 5.4.0 indicates that the DTE XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 5.4.0 indicates that the DTE XS is not able to operate at a data rate of 10 Gb/s.

45.2.5.5 DTE XS devices in package (Registers 5.5 and 5.6)

The assignment of bits in the DTE XS devices in package registers is shown in Table 45–56.

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Table 45–56—DTE XS devices in package registers bit definitions

Bit(s)	Name	Description	R/W[a]
5.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
5.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
5.6.13:0	Reserved	Ignore on read	RO
5.5.15:6	Reserved	Ignore on read	RO
5.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
5.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
5.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
5.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
5.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
5.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

[a]RO = Read Only

When read as a one, a bit in the DTE XS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the DTE XS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

45.2.5.6 DTE XS status 2 register (Register 5.8)

The assignment of bits in the DTE XS status 2 register is shown in Table 45–57. All the bits in the DTE XS status 2 register are read only; a write to the DTE XS status 2 register shall have no effect.

45.2.5.6.1 Device present (5.8.15:14)

When read as <10>, bits 5.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 5.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.5.6.2 Transmit fault (5.8.11)

When read as a one, bit 5.8.11 indicates that the DTE XS has detected a fault condition on the transmit path. When read as a zero, bit 5.8.11 indicates that the DTE XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

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Table 45–57—DTE XS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
5.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
5.8.13:12	Reserved	Ignore when read	RO
5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
5.8.9:0	Reserved	Ignore when read	RO

[a]RO = Read Only, LH = Latching High

The default value of bit 5.8.11 is zero.

45.2.5.6.3 Receive fault (5.8.10)

When read as a one, bit 5.8.10 indicates that the DTE XS has detected a fault condition on the receive path. When read as a zero, bit 5.8.10 indicates that the DTE XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.10 is zero.

45.2.5.7 DTE XS package identifier (Registers 5.14 and 5.15)

Registers 5.14 and 5.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the DTE XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the DTE XS package identifier is specified in 22.2.4.3.1.

45.2.5.8 10G DTE XGXS lane status register (Register 5.24)

The assignment of bits in the 10G DTE XGXS lane status register is shown in Table 45–58. All the bits in the 10G DTE XGXS lane status register are read only; a write to the 10G DTE XGXS lane status register shall have no effect.

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Table 45–58—10G DTE XGXS lane status register bit definitions

Bit(s)	Name	Description	R/W[a]
5.24.15:13	Reserved	Ignore when read	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10:4	Reserved	Ignore when read	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

[a]RO = Read Only

45.2.5.8.1 DTE XGXS receive lane alignment status (5.24.12)

When read as a one, bit 5.24.12 indicates that the DTE XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 5.24.12 indicates that the DTE XGXS has not synchronized and aligned all four receive lanes.

45.2.5.8.2 Pattern testing ability (5.24.11)

When read as a one, bit 5.24.11 indicates that the 10G DTE XGXS is able to generate test patterns. When read as a zero, bit 5.24.11 indicates that the 10G DTE XGXS is not able to generate test patterns. If the 10G DTE XGXS is able to generate test patterns then the functionality is controlled using the transmit test-pattern enable bit in register 5.25.

45.2.5.8.3 Lane 3 sync (5.24.3)

When read as a one, bit 5.24.3 indicates that the XGXS receive lane 3 is synchronized. When read as a zero, bit 5.24.3 indicates that the XGXS receive lane 3 is not synchronized.

45.2.5.8.4 Lane 2 sync (5.24.2)

When read as a one, bit 5.24.2 indicates that the XGXS receive lane 2 is synchronized. When read as a zero, bit 5.24.2 indicates that the XGXS receive lane 2 is not synchronized.

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45.2.5.8.5 Lane 1 sync (5.24.1)

When read as a one, bit 5.24.1 indicates that the XGXS receive lane 1 is synchronized. When read as a zero, bit 5.24.1 indicates that the XGXS receive lane 1 is not synchronized.

45.2.5.8.6 Lane 0 sync (5.24.0)

When read as a one, bit 5.24.0 indicates that the XGXS receive lane 0 is synchronized. When read as a zero, bit 5.24.0 indicates that the XGXS receive lane 0 is not synchronized.

45.2.5.9 10G DTE XGXS test control register (Register 5.25)

The assignment of bits in the 10G DTE XGXS test control register is shown in Table 45–59. The default value for each bit of the 10G DTE XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–59—10G DTE XGXS test control register bit definitions

Bit(s)	Name	Description	R/W[a]
5.25.15:3	Reserved	Value always 0, writes ignored	R/W
5.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W
5.25.1:0	Test-pattern select	1 0 1 1 = Reserved 1 0 = Mixed-frequency test pattern 0 1 = Low-frequency test pattern 0 0 = High-frequency test pattern	R/W

[a]R/W = Read/Write

45.2.5.9.1 10G DTE XGXS test-pattern enable (5.25.2)

When bit 5.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 5.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10G DTE XGXS to generate test patterns is advertised by the pattern testing ability bit in register 5.24. A 10G DTE XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 5.25.2 is zero.

45.2.5.9.2 10G DTE XGXS test-pattern select (5.25.1:0)

The test pattern to be used when pattern testing is enabled using bit 5.25.2 is selected using bits 5.25.1:0. When bits 5.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

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45.2.6 Vendor specific MMD 1 registers

The assignment of registers in the vendor specific MMD 1 is shown in Table 45–60. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–60—Vendor specific MMD 1 registers

Register address	Register name
30.0, 30.1	Vendor specific
30.2, 30.3	Vendor specific MMD 1 device identifier
30.4 through 30.7	Vendor specific
30.8	Vendor specific MMD 1 status register
30.9 through 30.13	Vendor specific
30.14, 30.15	Vendor specific MMD 1 package identifier
30.16 through 30.65 535	Vendor specific

45.2.6.1 Vendor specific MMD 1 device identifier (Registers 30.2 and 30.3)

Registers 30.2 and 30.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 1 device identifier.

The format of the vendor specific MMD 1 device identifier is specified in 22.2.4.3.1.

45.2.6.2 Vendor specific MMD 1 status register (Register 30.8)

The assignment of bits in the vendor specific MMD 1 status register is shown in Table 45–61. All the bits in the vendor specific MMD 1 status register are read only; a write to the vendor specific MMD 1 status register shall have no effect.

45.2.6.2.1 Device present (30.8.15:14)

When read as <10>, bits 30.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 30.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.6.3 Vendor specific MMD 1 package identifier (Registers 30.14 and 30.15)

Registers 30.14 and 30.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD 1 is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package

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Table 45–61—Vendor specific MMD 1 status register bit definitions

Bit(s)	Name	Description	R/W[a]
30.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
30.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD 1 may return a value of zero in each of the 32 bits of the vendor specific MMD 1 package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 1 package identifier is specified in 22.2.4.3.1.

45.2.7 Vendor specific MMD 2 registers

The assignment of registers in the vendor specific MMD 2 is shown in Table 45–62. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

Table 45–62—Vendor specific MMD 2 registers

Register address	Register name
31.0, 31.1	Vendor specific
31.2, 31.3	Vendor specific MMD 2 device identifier
31.4 through 31.7	Vendor specific
31.8	Vendor specific MMD 2 status register
31.9 through 31.13	Vendor specific
31.14, 30.15	Vendor specific MMD 2 package identifier
31.16 through 31.65 535	Vendor specific

45.2.7.1 Vendor specific MMD 2 device identifier (Registers 31.2 and 31.3)

Registers 31.2 and 31.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number,

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plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 2 device identifier.

The format of the vendor specific MMD 2 device identifier is specified in 22.2.4.3.1.

45.2.7.2 Vendor specific MMD 2 status register (Register 31.8)

The assignment of bits in the vendor specific MMD 2 status register is shown in Table 45–63. All the bits in the vendor specific MMD 2 status register are read only; a write to the vendor specific MMD status register shall have no effect.

Table 45–63—Vendor specific MMD 2 status register bit definitions

Bit(s)	Name	Description	R/W[a]
31.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
31.8.13:0	Reserved	Ignore when read	RO

[a]RO = Read Only

45.2.7.2.1 Device present (31.8.15:14)

When read as <10>, bits 31.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 31.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

45.2.7.3 Vendor specific MMD 2 package identifier (Registers 31.14 and 31.15)

Registers 31.14 and 31.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 2 package identifier is specified in 22.2.4.3.1.

45.3 Management frame structure

The MDIO interface frame structure is compatible with the one defined in 22.2.4.5 such that the two systems can co-exist on the same MDIO bus. The electrical specification for the MDIO interface is incompatible to that defined in 22.2.4.5; therefore, if the two systems are to co-exist on the same bus, a voltage translation device is required (see Annex 45A). The extensions that are used for MDIO indirect register accesses are specified in Table 45–64.

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Table 45–64—Extensions to Management Frame Format for Indirect Access

	Management frame fields							
Frame	**PRE**	**ST**	**OP**	**PRTAD**	**DEVAD**	**TA**	**ADDRESS / DATA**	**IDLE**
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

Each MMD shall implement a sixteen bit address register that stores the address of the register to be accessed by data transaction frames. The address register shall be overwritten by address frames. At power up or device reset, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register.

Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. For the case where the MMD's address register contains 65 535, the MMD shall not increment the address register.

Implementations that incorporate several MMDs within a single component shall implement separate address registers so that the MMD's address registers operate independently of one another.

45.3.1 IDLE (idle condition)

The idle condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the MMD's pull-up resistor will pull the MDIO line to a one.

45.3.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC to provide the MMD with a pattern that it can use to establish synchronization. An MMD shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

45.3.3 ST (start of frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 shall be ignored by the devices specified in Clause 45.

45.3.4 OP (operation code)

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address

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frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read-increment-address operation.

45.3.5 PRTAD (port address)

The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity must have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.

45.3.6 DEVAD (device address)

The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.

45.3.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the device address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, both the STA and the MMD shall remain in a high-impedance state for the first bit time of the turnaround. The MMD shall drive a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read or post-read-increment-address transaction.

45.3.8 ADDRESS / DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read-increment-address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

45.4 Electrical interface

45.4.1 Electrical specification

The electrical characteristics of the MDIO interface are shown in Table 45–65. The MDIO uses signal levels that are compatible with devices operating at a nominal supply voltage of 1.2V.

NOTE—It is possible to implement the MDIO electrical interface using open drain buffers and a weak resistive pull up to a V_{DD} of 1.2V.

45.4.2 Timing specification

MDIO is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the MMD. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 45–3, measured at the MMD.

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

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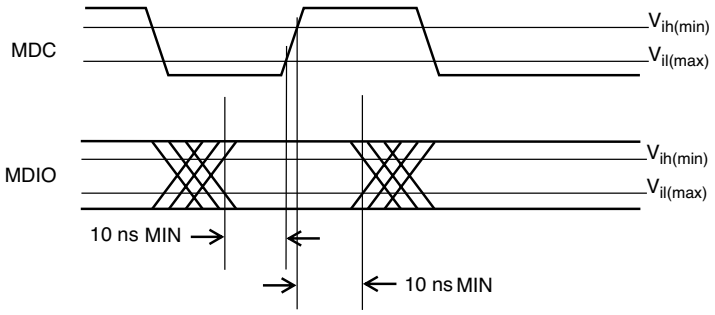


Figure 45–3—MDIO sourced by STA

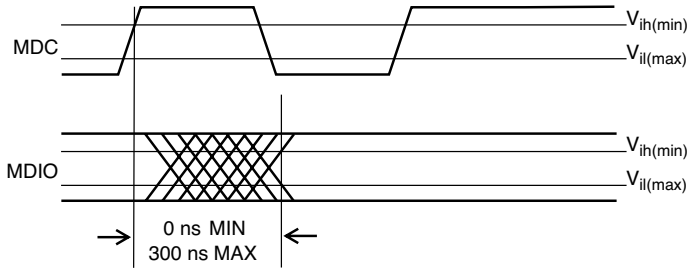


Figure 45–4—MDIO sourced by MMD

Table 45–65—MDIO electrical interface characteristics

Symbol	Parameter	Condition	Min.	Max.
V_{IH}	Input high voltage		0.84V	1.5V
V_{IL}	Input low voltage		–0.3V	0.36V
V_{OH}	Output high voltage	I_{OH} = -100uA	1.0V	1.5V
V_{OL}	Output low voltage	I_{OL} = 100uA	–0.3V	0.2V
I_{OH}[a]	Output high current	V_I = 1.0V		–4mA
I_{OL}	Output low current	V_I = 0.2V	+4mA	
C_i	Input capacitance			10pF
C_L	Bus loading			470pF

[a]I_{OH} parameter is not applicable to open drain drivers.

The timing specification for the MDC signal is given in 22.2.2.11.

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45.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 45, MDIO interface[4]

45.5.3 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.4 Identification

45.5.4.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.4.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose any may further publish the completed PICS.

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45.5.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Implementation of PMA/PMD MMD	45.2.1		O	Yes [ ] No [ ]
*WIS	Implementation of WIS MMD	45.2.2		O	Yes [ ] No [ ]
*PCS	Implementation of PCS MMD	45.2.3		O	Yes [ ] No [ ]
*PX	Implementation of PHY XS MMD	45.2.4		O	Yes [ ] No [ ]
*DX	Implementation of DTE XS MMD	45.2.5		O	Yes [ ] No [ ]
*VSA	Implementation of Vendor Specific MMD 1	45.2.6		O	Yes [ ] No [ ]
*VSB	Implementation of Vendor Specific MMD 2	45.2.7		O	Yes [ ] No [ ]

45.5.5 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.5.1 MDIO signal functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	MDC min high/low time	45.4.2	160 ns	M	Yes [ ] No [ ]
SF2	MDC min period	45.4.2	400 ns	M	Yes [ ] No [ ]
SF3	MDIO uses three-state drivers	45.4.1		M	Yes [ ] No [ ]

45.5.5.2 PMA/PMD MMD options

Item	Feature	Subclause	Value/Comment	Status	Support
*ALB	Implementation of PMA loop-back function	45.2.1.1.4		PMA:O	Yes [ ] No [ ] N/A [ ]
*PLF	Implementation of fault detection	45.2.1.7		PMA:O	Yes [ ] No [ ] N/A [ ]
*PTD	Implementation of transmit disable function	45.2.1.8		PMA:O	Yes [ ] No [ ] N/A [ ]

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45.5.5.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Speed selection bits 13 and 6 are written as one	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM16	PMA is set into Loopback mode when bit 0 is set to a one	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM17	PMA transmit data is returned on receive path when in loopback	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM18	PMA ignores writes to this bit if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA returns a value of zero when read if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM20	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM21	Receive link status implemented with latching low behavior	45.2.1.2.2		PMA:M	Yes [ ] N/A [ ]
MM22	Unique identifier is composed of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM23	10G PMA/PMD type is selected using bits 2:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM24	10G PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM25	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM27	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM28	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM29	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM30	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM31	Single wavelength device uses lane zero for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM32	Single wavelength device ignores writes to bits 1 – 4 and returns a value of zero for them	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM33	Setting bit 4 to a one disables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM34	Setting bit 4 to a zero enables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM35	Setting bit 3 to a one disables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM36	Setting bit 3 to a zero enables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Setting bit 2 to a one disables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 2 to a zero enables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 1 to a one disables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Setting bit 1 to a zero enables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM41	Setting bit 0 to a one disables transmission	45.2.1.8.5		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM42	Setting bit 0 to a zero enables transmission	45.2.1.8.5	Only is all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM43	Unique identifier is composed of OUI, model number and revision	45.2.1.10		PMA:M	Yes [ ] N/A [ ]

45.5.5.4 WIS options

Item	Feature	Subclause	Value/Comment	Status	Support
*WPT	Implementation of PRBS31 pattern testing	45.2.2		WIS:O	Yes [ ] No [ ] N/A [ ]

45.5.5.5 WIS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
WM1	Device responds to all register addresses for that device	45.2		WIS:M	Yes [ ] N/A [ ]
WM2	Writes to undefined and read-only registers have no effect	45.2		WIS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		WIS:M	Yes [ ] N/A [ ]
WM4	Reserved and unsupported bits return a value of zero	45.2		WIS:M	Yes [ ] N/A [ ]
WM5	Latching low bits remain low until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM7	Latching high bits remain high until after they have been read via the management interface	45.2		WIS:M	Yes [ ] N/A [ ]
WM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ ] N/A [ ]
WM9	Action on reset	45.2.2.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	WIS:M	Yes [ ] N/A [ ]
WM10	Return 1 until reset completed	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM11	Reset completes within 0.5 s	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM12	Responds to reads of bits 2.0.15 and 2.8.15:14 during reset	45.2.2.1.1		WIS:M	Yes [ ] N/A [ ]
WM13	Loopback mode	45.2.2.1.2	Whenever bit 2.0.14 is set to a one	WIS:M	Yes [ ] N/A [ ]
WM14	Data received from PMA ignored during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM15	Transmit data returned on receive path during loopback	45.2.2.1.2		WIS:M	Yes [ ] N/A [ ]
WM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.2.1.3		WIS:M	Yes [ ] N/A [ ]
WM17	Speed selection bits 13 and 6 are written as one	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM18	Invalid writes to speed selection bits are ignored	45.2.2.1.4		WIS:M	Yes [ ] N/A [ ]
WM19	Writes to status 1 register have no effect	45.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM20	Fault bit implemented using latching high behavior	45.2.2.2.1		WIS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM21	Link status bit implemented using latching low behavior	45.2.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM22	Unique identifier is composed of OUI, model number and revision	45.2.2.3		WIS:M	Yes [ ] N/A [ ]
WM23	Setting bit 2.7.5 to a one enables PRBS31 receive pattern testing if bit 2.8.1 is a one and bit 2.7.2 is not a one	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM24	Setting bit 2.7.5 to a zero disables PRBS31 receive pattern testing	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM25	Setting bit 2.7.4 to a one enables PRBS31 transmit pattern testing if bit 2.8.1 is a one and bit 2.7.1 is not a one	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM26	Setting bit 2.7.4 to a zero disables PRBS31 transmit pattern testing	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM27	Setting bit 3 to one selects the square wave test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM28	Setting bit 3 to zero selects the pseudo random test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM29	Setting bit 2 to one enables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM30	Setting bit 2 to zero disables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM31	Setting bit 1 to one enables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM32	Setting bit 1 to zero disables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM33	Setting bit 0 to a one enables 10GBASE-W logic and sets interface speed	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM34	Setting bit 0 to a zero disables 10GBASE-W logic, sets interface speed. and bypasses data	45.2.2.6.6		WIS:O	Yes [ ] N/A [ ]
WM35	Writes to bit are ignored by WIS not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM36	Bit returns one when read if WIS is not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM37	Writes to status 2 register have no effect	45.2.2.7		WIS:M	Yes [ ] N/A [ ]
WM38	Counter is reset to all zeros when read or reset	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM39	Counter is held at all ones at overflow	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM40	Unique identifier is composed of OUI, model number and revision	45.2.2.9		WIS:M	Yes [ ] N/A [ ]
WM41	Writes to Status 3 register have no effect	45.2.2.10		WIS:M	Yes [ ] N/A [ ]
WM42	SEF bit implemented using latching high behavior	45.2.2.10.1		WIS:M	Yes [ ] N/A [ ]
WM43	Far end PLM-P/LCD-P bit implemented using latching high behavior	45.2.2.10.2		WIS:M	Yes [ ] N/A [ ]
WM44	Far end AIS-P/LOP-P bit implemented using latching high behavior	45.2.2.10.3		WIS:M	Yes [ ] N/A [ ]
WM45	LOF bit implemented using latching high behavior	45.2.2.10.4		WIS:M	Yes [ ] N/A [ ]
WM46	LOS bit implemented using latching high behavior	45.2.2.10.5		WIS:M	Yes [ ] N/A [ ]
WM47	RDI-L bit implemented using latching high behavior	45.2.2.10.6		WIS:M	Yes [ ] N/A [ ]
WM48	AIS-L bit implemented using latching high behavior	45.2.2.10.7		WIS:M	Yes [ ] N/A [ ]
WM49	LCD-P bit implemented using latching high behavior	45.2.2.10.8		WIS:M	Yes [ ] N/A [ ]
WM50	PLM-P bit implemented using latching high behavior	45.2.2.10.9		WIS:M	Yes [ ] N/A [ ]
WM51	AIS-P bit implemented using latching high behavior	45.2.2.10.10		WIS:M	Yes [ ] N/A [ ]
WM52	LOP-P bit implemented using latching high behavior	45.2.2.10.11		WIS:M	Yes [ ] N/A [ ]

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45.5.5.6 PCS options

Item	Feature	Subclause	Value/Comment	Status	Support
*CR	Implementation of 10GBASE-R PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CX	Implementation of 10GBASE-X PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*XP	Implementation of 10GBASE-X pattern testing	45.2.3		PCS* CX:O	Yes [ ] No [ ] N/A [ ]
*PPT	Implementation of PRBS31 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]

45.5.5.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Device responds to all register addresses for that device	45.2		PCS:M	Yes [ ] N/A [ ]
RM2	Writes to undefined and read-only registers have no effect	45.2		PCS:M	Yes [ ] N/A [ ]
RM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PCS:M	Yes [ ] N/A [ ]
RM4	Reserved and unsupported bits return a value of zero	45.2		PCS:M	Yes [ ] N/A [ ]
RM5	Latching low bits remain low until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM7	Latching high bits remain high until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM9	Action on reset	45.2.3.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PCS:M	Yes [ ] N/A [ ]
RM10	Return 1 until reset completed	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM11	Reset completes within 0.5 s	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM12	Device responds to reads of register bits 3.0.15 and 3.5.15:14 during reset	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM13	Loopback mode	45.2.3.1.2	Whenever bit 3.0.14 is set to a one	PCS:M	Yes [ ] N/A [ ]
RM14	Transmit data is returned on the receive path during loopback	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM15	Writes to loopback bit are ignored when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM16	Loopback bit returns zero when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM17	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.3.1.3		PCS:M	Yes [ ] N/A [ ]
RM18	Speed selection bits 13 and 6 are written as one	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM19	Invalid writes to speed selection bits are ignored	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM20	Writes to PCS status 1 register have no effect	45.2.3.2		PCS:M	Yes [ ] N/A [ ]
RM21	Receive link status implemented using latching low behavior	45.2.3.2.2		PCS:M	Yes [ ] N/A [ ]
RM22	Unique identifier is composed of OUI, model number and revision	45.2.3.3		PCS:M	Yes [ ] N/A [ ]
RM23	PCS type is selected using bits 1 through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM24	Writes to the type selection bits that select types that have not been advertised are ignored	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM25	Writes to PCS status 2 register have no effect	45.2.3.7		PCS:M	Yes [ ] N/A [ ]
RM26	Transmit fault implemented with latching high behavior	45.2.3.7.3		PCS:M	Yes [ ] N/A [ ]
RM27	Receive fault implemented with latching high behavior	45.2.3.7.2		PCS:M	Yes [ ] N/A [ ]
RM28	Unique identifier is composed of OUI, model number and revision	45.2.3.8		PCS:M	Yes [ ] N/A [ ]
RM29	Writes to 10GBASE-X PCS status register have no effect	45.2.3.9		PCS* CX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM30	Register returns zero if the PCS does not implement the 10GBASE-X port type	45.2.3.9		PCS* !CX:M	Yes [ ] N/A [ ]
RM31	Writes to bit are ignored and reads return a value of zero	45.2.3.10.1		PCS* PX:M	Yes [ ] N/A [ ]
RM32	Setting the bits to <10> selects the mixed frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM33	Setting the bits to <01> selects the low-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM34	Setting the bits to <00> selects the high-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM35	Writes to 10GBASE-R PCS status 1 register have no effect	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM36	Reads from 10GBASE-R PCS status 1 register return zero for PCS that does not support 10GBASE-R	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM37	Writes to 10GBASE-R PCS status 2 register have no effect	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM38	Reads from 10GBASE-R PCS status 2 register return zero for PCS that does not support 10GBASE-R	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM39	Latched block lock implemented with latching low behavior	45.2.3.12.1		PCS* CR:M	Yes [ ] N/A [ ]
RM40	Latched high BER implemented with latching high behavior	45.2.3.12.2		PCS* CR:M	Yes [ ] N/A [ ]
RM41	BER counter clears to zero on read or reset	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM42	BER counter holds at all ones at overflow	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM43	Errored blocks counter implemented as a non roll over counter	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM44	Errored blocks counter clears to zero on read	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM45	Setting bit 3.42.5 to a one enables PRBS31 receive pattern testing if bit 3.32.2 is a one and bit 3.42.2 is not a one	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM46	Setting bit 3.42.5 to a zero disables PRBS31 receive pattern testing	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM47	Setting bit 3.42.4 to a one enables PRBS31 transmit pattern testing if bit 3.32.2 is a one and bit 3.42.3 is not a one	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM48	Setting bit 3.42.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM49	Test-pattern error counter clears to zero on read or reset	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM50	Test-pattern error counter holds at all ones at overflow	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]

45.5.5.8 PHY XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*PL	Implementation of loopback	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]
*PT	Implementation of pattern testing	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]

45.5.5.9 PHY XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Device responds to all register addresses for that device	45.2		PX:M	Yes [ ] N/A [ ]
PM2	Writes to undefined and read-only registers have no effect	45.2		PX:M	Yes [ ] N/A [ ]
PM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PX:M	Yes [ ] N/A [ ]
PM4	Reserved and unsupported bits return a value of zero	45.2		PX:M	Yes [ ] N/A [ ]
PM5	Latching low bits remain low until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM7	Latching high bits remain high until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PM9	Action on reset	45.2.4.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PX:M	Yes [ ] N/A [ ]
PM10	Return 1 until reset completed	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM11	Reset completes within 0.5 s	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM12	Device responds to reads of bits 4.0.15 and 4.8.15:14 during reset	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM13	Loopback mode	45.2.4.1.2	Whenever bit 4.0.14 is set to a one	PX*PL:M	Yes [ ] N/A [ ]
PM14	Receive data is returned on transmit path during loopback	45.2.4.1.2		PX*PL:M	Yes [ ] N/A [ ]
PM15	Writes to loopback bit are ignored and reads return zero	45.2.4.1.2		PX*!PL:M	Yes [ ] N/A [ ]
PM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.4.1.3		PX:M	Yes [ ] N/A [ ]
PM17	Speed selection bits 13 and 6 are written as one	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM18	Invalid writes to speed selection bits are ignored	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM19	Writes to status 1 register have no effect	45.2.4.2		PX:M	Yes [ ] N/A [ ]
PM20	Transmit link status implemented using latching low behavior	45.2.4.2.2		PX:M	Yes [ ] N/A [ ]
PM21	Unique identifier is composed of OUI, model number and revision	45.2.4.3		PX:M	Yes [ ] N/A [ ]
PM22	Writes to status 2 register have no effect	45.2.4.6		PX:M	Yes [ ] N/A [ ]
PM23	Transmit fault implemented with latching high behavior	45.2.4.6.2		PX:M	Yes [ ] N/A [ ]
PM24	Receive fault implemented with latching high behavior	45.2.4.6.3		PX:M	Yes [ ] N/A [ ]
PM25	Unique identifier is composed of OUI, model number and revision	45.2.4.7		PX:M	Yes [ ] N/A [ ]
PM26	Writes to 10G PHY XGXS Lane status register have no effect	45.2.4.8		PX:M	Yes [ ] N/A [ ]
PM27	Writes to bit are ignored and reads return a value of zero	45.2.4.9.1		PX*!PT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PM28	Setting the bits to <10> selects the mixed frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM29	Setting the bits to <01> selects the low-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM30	Setting the bits to <00> selects the high-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]

45.5.5.10 DTE XS options

Item	Feature	Subclause	Value/Comment	Status	Support
*DT	Implementation of pattern testing	45.2.5		DX:O	Yes [ ] No [ ] N/A [ ]

45.5.5.11 DTE XS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
DM1	Device responds to all register addresses for that device	45.2		DX:M	Yes [ ] N/A [ ]
DM2	Writes to undefined and read-only registers have no effect	45.2		DX:M	Yes [ ] N/A [ ]
DM3	Operation is not affected by writes to reserved and unsupported bits	45.2		DX:M	Yes [ ] N/A [ ]
DM4	Reserved and unsupported bits return a value of zero	45.2		DX:M	Yes [ ] N/A [ ]
DM5	Latching low bits remain low until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM7	Latching high bits remain high until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM9	Action on reset	45.2.5.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	DX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DM10	Return 1 until reset completed	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM11	Reset completes within 0.5 s	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM12	Device responds to reads of bits 5.0.15 and 5.8.15:14 during reset	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM13	Loopback mode	45.2.5.1.2	Whenever bit 5.0.14 is set to a one	DX:M	Yes [ ] N/A [ ]
DM14	Transmit data is returned on receive path during loopback	45.2.5.1.2		DX:M	Yes [ ] N/A [ ]
DM15	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.5.1.3		DX:M	Yes [ ] N/A [ ]
DM16	Speed selection bits 13 and 6 are written as one	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM17	Invalid writes to speed selection bits are ignored	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM18	Writes to status 1 register have no effect	45.2.5.2		DX:M	Yes [ ] N/A [ ]
DM19	Receive link status implemented using latching low behavior	45.2.5.2.2		DX:M	Yes [ ] N/A [ ]
DM20	Unique identifier is composed of OUI, model number and revision	45.2.5.3		DX:M	Yes [ ] N/A [ ]
DM21	Writes to status 2 register have no effect	45.2.5.6		DX:M	Yes [ ] N/A [ ]
DM22	Transmit fault implemented with latching high behavior	45.2.5.6.2		DX:M	Yes [ ] N/A [ ]
DM23	Receive fault implemented with latching high behavior	45.2.5.6.3		DX:M	Yes [ ] N/A [ ]
DM24	Unique identifier is composed of OUI, model number and revision	45.2.5.7		DX:M	Yes [ ] N/A [ ]
DM25	Writes to 10G DTE XGXS Lane status register have no effect	45.2.5.8		DX:M	Yes [ ] N/A [ ]
DM26	Writes to bit are ignored and reads return a value of zero	45.2.5.9.1		DX*!DT:M	Yes [ ] N/A [ ]
DM27	Setting the bits to <10> selects the mixed frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM28	Setting the bits to <01> selects the low-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM29	Setting the bits to <00> selects the high-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]

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45.5.5.12 Vendor specific MMD 1 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSA1	Device responds to all register addresses for that device	45.2		VSA:M	Yes [ ] N/A [ ]
VSA2	Writes to undefined and read-only registers have no effect	45.2		VSA:M	Yes [ ] N/A [ ]
VSA3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSA:M	Yes [ ] N/A [ ]
VSA4	Reserved and unsupported bits return a value of zero	45.2		VSA:M	Yes [ ] N/A [ ]
VSA5	Unique identifier is composed of OUI, model number and revision	45.2.6.1		VSA:M	Yes [ ] N/A [ ]
VSA6	Writes to status register have no effect	45.2.6.2		VSA:M	Yes [ ] N/A [ ]
VSA7	Unique identifier is composed of OUI, model number and revision	45.2.6.3		VSA:M	Yes [ ] N/A [ ]

45.5.5.13 Vendor specific MMD 2 management functions

Item	Feature	Subclause	Value/Comment	Status	Support
VSB1	Device responds to all register addresses for that device	45.2		VSB:M	Yes [ ] N/A [ ]
VSB2	Writes to undefined and read-only registers have no effect	45.2		VSB:M	Yes [ ] N/A [ ]
VSB3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSB:M	Yes [ ] N/A [ ]
VSB4	Reserved and unsupported bits return a value of zero	45.2		VSB:M	Yes [ ] N/A [ ]
VSB5	Unique identifier is composed of OUI, model number and revision	45.2.7.1		VSB:M	Yes [ ] N/A [ ]
VSB6	Writes to status register have no effect	45.2.7.2		VSB:M	Yes [ ] N/A [ ]
VSB7	Unique identifier is composed of OUI, model number and revision	45.2.7.3		VSB:M	Yes [ ] N/A [ ]

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45.5.5.14 Management frame structure

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Device has implemented sixteen bit address register	45.3		M	Yes [ ]
MF2	Address register is overwritten by address frames	45.3		M	Yes [ ]
MF3	Write, read, and post-read-increment-address frames access the register whose address is held in the address register	45.3		M	Yes [ ]
MF4	Write and read frames do not modify the address register	45.3		M	Yes [ ]
MF5	Post-read-increment-address frames increment the address register by one unless the address register contains 65 535	45.3		M	Yes [ ]
MF6	Components containing several MMDs implement separate address registers	45.3		M	Yes [ ]
MF7	Tri state drivers are disabled during idle	45.3.1		M	Yes [ ]
MF8	STA sources 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF9	MMD observes 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF10	Frames containing ST=<01> sequence are ignored	45.3.3		M	Yes [ ]
MF11	STA tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF12	MMD tri state driver is high impedence during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF13	MMD tri state driver drives a zero bit during second bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF14	STA tri state driver drives a one bit followed by a zero bit for the TA during write or address frames	45.3.7		M	Yes [ ]
MF15	First bit transmitted and received is bit 15	45.3.8		M	Yes [ ]

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45.5.5.15 Signal timing characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	MDIO setup and hold time	45.4.2	Setup min = 10 ns; Hold min = 10 ns per	M	Yes [ ]
ST2	MDIO clock to output delay	45.4.2	Min = 0 ns; Max = 300 ns per	M	Yes [ ]

45.5.5.16 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	V_{OH}	45.4.1	≥ 1.0V (I_{OH} = –100 uA) ≤ 1.5V (I_{OH} = –100 uA)	M	Yes [ ]
EC2	V_{OL}	45.4.1	≥ –0.3V (I_{OL} = 100 uA) ≤ 0.2 V (I_{OL} = 100 uA)	M	Yes [ ]
EC3	V_{IH}	45.4.1	0.84 V ≤ V_{IH} ≤ 1.5 V	M	Yes [ ]
EC4	V_{IL}	45.4.1	–0.3 ≤ V_{IL} ≤ 0.36 V	M	Yes [ ]
EC5	Input capacitance for MDIO	45.4.1	≤ 10pF	M	Yes [ ]
EC6	Bus loading	45.4.1	≤ 470pF	M	Yes [ ]
EC7	I_{OH}	45.4.1	≤ –4mA at V_I = 1.0V	M	Yes [ ]
EC8	I_{OL}	45.4.1	≥ +4mA at V_I = 0.2V	M	Yes [ ]

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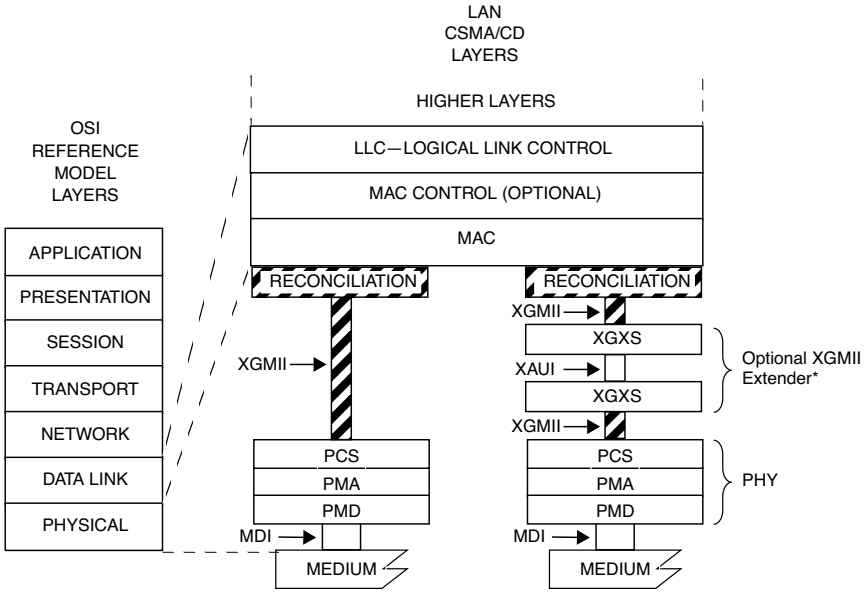
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46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

46.1 Overview

This clause defines the logical and electrical characteristics for the Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII) between CSMA/CD media access controllers and various PHYs. Figure 46–1 shows the relationship of the RS and XGMII to the ISO/IEC (IEEE) OSI reference model.



MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XAUI = 10 GIGABIT ATTACHMENT UNIT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
XGXS = XGMII EXTENDER SUBLAYER

*specified in Clause 47

Figure 46–1—XGMII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of the XGMII is to provide a simple, inexpensive, and easy-to-implement interconnection between the Media Access Control (MAC) sublayer and the Physical layer (PHY). The 10 Gigabit Attachment Unit Interface (XAUI) may optionally be used to extend the operational distance of the XGMII with reduced pin count (see Clause 47).

The RS adapts the bit serial protocols of the MAC to the parallel encodings of 10 Gb/s PHYs. Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 10 Gb/s Physical Coding Sublayer (PCS) is specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented.

The XGMII has the following characteristics:

a) It is capable of supporting 10 Gb/s operation.
b) Data and delimiters are synchronous to clock reference.

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c) It provides independent 32-bit-wide transmit and receive data paths.
d) It uses signal levels compatible with common digital ASIC processes.
e) It provides for full duplex operation only.

46.1.1 Summary of major concepts

The following are the major concepts of XGMII:

a) The XGMII is functionally similar to the MII defined in Clause 22 and GMII defined in Clause 35 as they all define an interface allowing independent development of MAC and PHY logic.
b) The RS converts between the MAC serial data stream and the parallel data paths of the XGMII.
c) The RS maps the signal set provided at the XGMII to the PLS service primitives provided at the MAC.
d) Each direction of data transfer is independent and serviced by data, control, and clock signals.
e) The RS generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.
f) The RS participates in link fault detection and reporting by monitoring the receive path for status reports that indicate an unreliable link, and generating status reports on the transmit path to report detected link faults to the DTE on the remote end of the connecting link.
g) When the XGMII is optionally extended with XAUI, two XGMII interfaces logically exist (see Figure 46–1). The transmit path signals are from the RS to the DTE (top) XGXS of the XAUI via one XGMII and from the PHY (bottom) XGXS to the PCS via the other XGMII. The receive path signals are from the PCS to the PHY XGXS of the XAUI via one XGMII and from the DTE XGXS to the RS via the other XGMII. The descriptions of the XGMII as between the RS and the PCS are, therefore, equally applicable between the RS and the DTE XGXS or the PHY XGXS and the PCS.

46.1.2 Application

This clause applies to the interface between the MAC and PHY. The physical implementation of the interface is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. The XGMII may also be used in other ways, for example, as a logical interface between ASIC logic modules within an integrated circuit.

This interface is used to provide media independence so that an identical media access controller may be used with all 10GBASE PHY types using either serial or wavelength division multiplexed optics.

46.1.3 Rate of operation

The XGMII supports only the 10 Gb/s MAC data rate as defined within this clause. Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35.

PHYs that provide an XGMII shall support the 10 Gb/s MAC data rate. 10GBASE-X and 10GBASE-R PHYs operate at a 10 Gb/s data rate. 10GBASE-W PHYs operate at the STS-192/VC-4-64c line rate of 9.95328 Gb/s, mapping the encoded data stream at a 9.58464 Gb/s payload rate. On transmit, this mapping is performed by discarding Idle control characters corresponding to the stretched interpacket gap created by the MAC in this mode of operation, and on receive, by adding interpacket gap Idle control characters as required to adapt to the XGMII RX_CLK rate.

46.1.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control

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sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The maximum cumulative MAC Control, MAC and RS round-trip (sum of transmit and receive) delay shall meet the values specified in Table 46–1. Bit time is specified in 1.4, and pause_quanta is specified in 31B.2.

Table 46–1—Round-trip delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)
MAC, RS, and MAC Control	8192	16

46.1.5 Allocation of functions

The allocation of functions at the XGMII balances the need for media independence with the need for a simple and cost-effective interface. The bus width and signaling rate are applicable to short distance chip-to-chip interconnect with printed circuit board trace lengths electrically limited to approximately 7 cm. The XGMII (like the MII and GMII) maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling between the PLS sublayer or PCS and the PMA sublayer.

46.1.6 XGMII structure

The XGMII is composed of independent transmit and receive paths. Each direction uses 32 data signals (TXD<31:0> and RXD<31:0>), four control signals (TXC<3:0> and RXC<3:0>), and a clock (TX_CLK and RX_CLK). Figure 46–2 depicts a schematic view of the RS inputs and outputs.

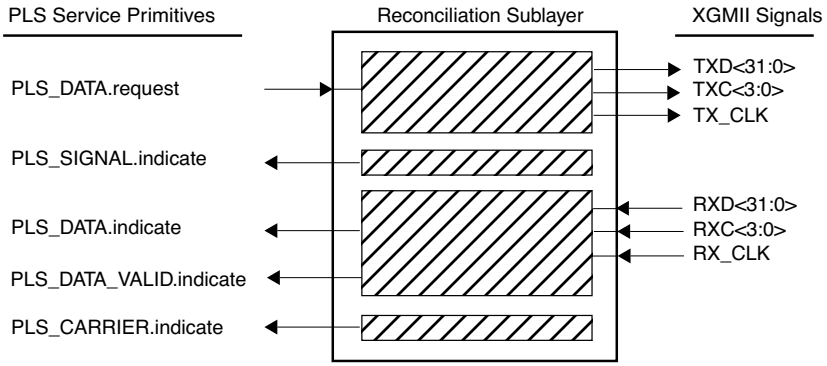


Figure 46–2—Reconciliation Sublayer (RS) inputs and outputs

The 32 TXD and four TXC signals shall be organized into four data lanes, as shall the 32 RXD and four RXC signals (see Table 46–2). The four lanes in each direction share a common clock—TX_CLK for transmit and RX_CLK for receive. The four lanes are used in round-robin sequence to carry an octet stream. On transmit, each eight PLS_DATA.request transactions represent an octet transmitted by the MAC. The first octet is aligned to lane 0, the second to lane 1, the third to lane 2 the fourth to lane 3, then repeating with the fifth to lane 0, etc. Delimiters and interframe idle characters are encoded on the TXD and RXD signals with the control code indicated by assertion of TXC and RXC, respectively.

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Table 46–2—Transmit and receive lane associations

TXD RXD	TXC RXC	Lane
<7:0>	<0>	0
<15:8>	<1>	1
<23:16>	<2>	2
<31:24>	<3>	3

46.1.7 Mapping of XGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 10 Gb/s; therefore, PLS service primitives supporting CSMA/CD operation are not mapped through the RS to the XGMII.

Mappings for the following primitives are defined for 10 Gb/s operation:

PLS_DATA.request
PLS_DATA.indicate
PLS_CARRIER.indicate
PLS_SIGNAL.indicate
PLS_DATA_VALID.indicate

46.1.7.1 Mapping of PLS_DATA.request

46.1.7.1.1 Function

Map the primitive PLS_DATA.request to the XGMII signals TXD<31:0>, TXC<3:0>, and TX_CLK.

46.1.7.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The DATA_COMPLETE value signifies that the Media Access Control sublayer has no more data to output.

46.1.7.1.3 When generated

This primitive is generated by the MAC sublayer to request the transmission of a single data bit on the physical medium or to stop transmission.

46.1.7.1.4 Effect of receipt

The OUTPUT_UNIT values are conveyed to the PHY by the signals TXD<31:0> and TXC<3:0> on each TX_CLK edge. Each PLS_DATA.request transaction shall be mapped to a TXD signal in sequence (TXD<0>, TXD<1>, ... TXD<31>, TXD<0>) as described in 46.2. After 32 PLS_DATA.request transactions from the MAC sublayer (four octets of eight PLS_DATA.request transactions each), the RS requests transmission of 32 data bits by the PHY. The first octet of preamble shall be converted to a Start control

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character and aligned to lane 0. The TXD<31:0> and TXC<3:0> shall be generated by the RS for each 32 bit-times of the MAC sublayer.

The DATA_COMPLETE value shall be mapped to a Terminate control character encoded on the next eight TXD signals in sequence after the last data octet; and is transferred to the PHY at the next TX_CLK edge. This may be on the same TX_CLK edge as the last data octet or the subsequent TX_CLK edge. When the Terminate control character is in lane 0, 1, or 2, the lanes following in sequence are encoded with an Idle control character.

46.1.7.2 Mapping of PLS_DATA.indicate

46.1.7.2.1 Function

Map the primitive PLS_DATA.indicate to the XGMII signals RXD<31:0>, RXC<3:0> and RX_CLK.

46.1.7.2.2 Semantics of the service primitive

PLS_DATA.indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit.

46.1.7.2.3 When generated

The INPUT_UNIT values are derived from the signals RXC<3:0> and RXD<31:0> received from the PHY on each edge of RX_CLK. Each primitive generated to the MAC sublayer entity corresponds to a PLS_DATA.request issued by the MAC at the remote end of the link connecting two DTEs. For each RXD<31:0> during frame reception, the RS shall generate 32 PLS_DATA.indicate transactions until the end of frame (Terminate control character), where 0, 8, 16, or 24 PLS_DATA.indicate transactions will be generated from the RXD<31:0> containing the Terminate. During frame reception, each RXD signal shall be mapped in sequence into a PLS_DATA.indicate transaction (RXD<0>, RXD<1>,... RXD<31>, RXD<0>) as described in 46.2.

The RS shall convert a valid Start control character to a preamble octet prior to generation of the associated PLS_DATA.indicate transactions. The RS shall not generate any PLS_DATA.indicate primitives for a Terminate control character. To assure robust operation, the value of the data transferred to the MAC may be changed by the RS as required by XGMII error indications (see 46.3.3). Sequence ordered_sets are not indicated to the MAC (see 46.3.4).

46.1.7.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

46.1.7.3 Mapping of PLS_CARRIER.indicate

10 Gb/s operation supports full duplex operation only. The RS never generates this primitive.

46.1.7.4 Mapping of PLS_SIGNAL.indicate

10 Gb/s operation supports full duplex operation only. The RS never generates this primitive.

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46.1.7.5 Mapping of PLS_DATA_VALID.indicate

46.1.7.5.1 Function

Map the primitive PLS_DATA_VALID.indicate to the XGMII signals RXC<3:0> and RXD<31:0>.

46.1.7.5.2 Semantics of the service primitive

PLS_DATA_VALID.indicate (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. The DATA_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indicate primitive contains a valid data of an incoming frame. The DATA_NOT_VALID value indicates that the INPUT_UNIT parameter of the PLS_DATA.indicate primitive does not contain valid data of an incoming frame.

46.1.7.5.3 When generated

The PLS_DATA_VALID.indicate service primitive shall be generated by the RS whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

DATA_VALID_STATUS shall assume the value DATA_VALID when a PLS_DATA.indicate transaction is generated in response to reception of a Start control character on lane 0 if the prior RXC<3:0> and RXD<31:0> contained four Idle characters or a Sequence ordered set. DATA_VALID_STATUS shall assume the value DATA_NOT_VALID when RXC of the current lane in sequence is asserted for anything except an Error control character. In the absence of errors, DATA_NOT_VALID is caused by a Terminate control character. When DATA_VALID_STATUS changes from DATA_VALID to DATA_NOT_VALID because of a control character other than Terminate, the RS shall ensure that the MAC will detect a FrameCheckError prior to indicating DATA_NOT_VALID to the MAC (see 46.3.3.1).

46.1.7.5.4 Effect of receipt

The effect of receipt of this primitive by the MAC sublayer is unspecified.

46.2 XGMII data stream

Data frames transmitted through the XGMII shall be transferred within the XGMII data stream. The data stream is a sequence of bytes, where each byte conveys either a data octet or control character. The parts of the data stream are shown in Figure 46–3.

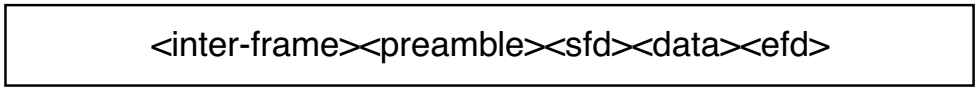


Figure 46–3—XGMII data stream

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For the XGMII, transmission and reception of each bit and mapping of data octets to lanes shall be as shown in Figure 46–4.

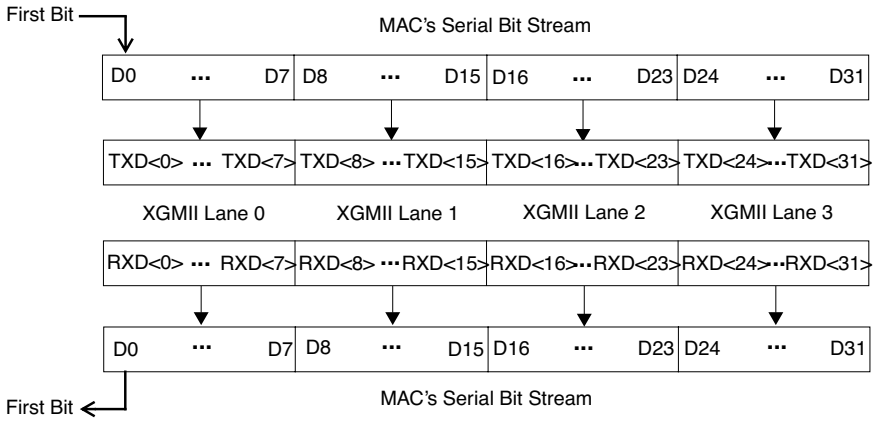


Figure 46–4—Relationship of data lanes to MAC serial bit stream

46.2.1 Inter-frame <inter-frame>

The inter-frame <inter-frame> period on an XGMII transmit or receive path is an interval during which no frame data activity occurs. The <inter-frame> corresponding to the MAC interpacket gap begins with the Terminate control character, continues with Idle control characters and ends with the Idle control character prior to a Start control character. The length of the interpacket gap may be changed between the transmitting MAC and receiving MAC by one or more functions (e.g., RS lane alignment, PHY clock rate compensation, or 10GBASE-W data rate adaptation functions). The minimum IPG at the XGMII of the receiving RS is five octets.

The signaling of link status information logically occurs in the <inter-frame> period (see 46.3.4). Subclause 46.3.3 describes frame processing when signaling of link status information is initiated or terminated.

46.2.2 Preamble <preamble> and start of frame delimiter <sfd>

The preamble <preamble> begins a frame transmission by a MAC as specified in 4.2.5 and when generated by a MAC consists of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The Start control character indicates the beginning of MAC data on the XGMII. On transmit, the RS converts the first data octet of preamble transferred from the MAC into a Start control character. On receive, the RS will convert the Start control character into a preamble data octet. The start control character is aligned to lane 0 of the XGMII by the RS on transmit and by the PHY on receive.

The start of frame delimiter <sfd> indicates the start of a frame and immediately follows the preamble. The bit value of <sfd> at the XGMII is unchanged from the Start Frame Delimiter (SFD) specified in 4.2.6 and is the bit sequence:

10101011

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The preamble and SFD are shown previously with their bits ordered for serial transmission from left to right. As shown, the left-most bit of each octet is the LSB of the octet and the right-most bit of each octet is the MSB of the octet.

The preamble and SFD are transmitted through the XGMII as octets sequentially ordered on the lanes of the XGMII. The first preamble octet is replaced with a Start control character and it is aligned to lane 0, the second octet on lane 1, the third on lane 2 and the fourth on lane 3, and the four octets are transferred on the next edge of TX_CLK. The fifth octet is assigned to lane 0 with subsequent octets sequentially assigned to the lanes with the SFD assigned to lane 3. The XGMII <preamble> and <sfd> are:

Lane 0	**Lane 1**	**Lane 2**	**Lane 3**
Start	10101010	10101010	10101010
10101010	10101010	10101010	10101011

46.2.3 Data <data>

The data <data> in a well-formed frame shall consist of a set of data octets.

46.2.4 End of frame delimiter <efd>

Assertion of TXC with the appropriate Terminate control character encoding of TXD on a lane constitutes an end of frame delimiter <efd> for the transmit data stream. Similarly, assertion of RXC with the appropriate Terminate control character encoding of RXD constitutes an end of frame delimiter for the receive data stream. The XGMII shall recognize the end of frame delimiter on any of the four lanes of the XGMII.

46.2.5 Definition of Start of Packet and End of Packet Delimiters

For the purposes of Clause 30, the Start of Packet delimiter is defined as the Start control character, and the End of Packet delimiter is defined as the end of the last sequential data octet preceding the Terminate control character or other control character causing a change from DATA_VALID to DATA_NOT_VALID. (See 46.1.7.5.2 and 30.3.2.1.5.)

46.3 XGMII functional specifications

The XGMII is designed to make the differences among the various media and transceiver combinations transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end.

NOTE—No XGMII loopback is defined, but XGMII signals are specified such that transmit signals may be connected to receive signals to create a loopback path. To do this, TXD<0> is connected to RXD<0> ... TXD<31> to RXD<31>, TXC<0> to RXC<0> ... TXC<3> to RXC<3>, and TXCLK to RXCLK. Such a loopback does not test the Link Fault Signaling state machine, nor any of the error handling functions of the receive RS.

46.3.1 Transmit

46.3.1.1 TX_CLK (10 Gb/s transmit clock)

TX_CLK is a continuous clock used for operation at 10 Gb/s. TX_CLK provides the timing reference for the transfer of the TXC<3:0> and TXD<31:0> signals from the RS to the PHY. The values of TXC<3:0> and TXD<31:0> shall be sampled by the PHY on both the rising edge and falling edge of TX_CLK. TX_CLK is sourced by the RS.

The TX_CLK frequency shall be 156.25 MHz ±0.01%, one-sixty-fourth of the MAC transmit data rate.

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46.3.1.2 TXC<3:0> (transmit control)

TXC<3:0> indicate that the RS is presenting either data or control characters on the XGMII for transmission. The TXC signal for a lane shall be de-asserted when a data octet is being sent on the corresponding lane and asserted when a control character is being sent. In the absence of errors, the TXC signals are de-asserted by the RS for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be transmitted are presented on the lanes of the XGMII. TXC<3:0> are driven by the RS and shall transition synchronously with respect to both the rising and falling edges of TX_CLK. Table 46–3 specifies the permissible encodings of TXD and TXC for a XGMII transmit lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Table 46–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	00 through 06	Reserved	—
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet)
1	FC	Reserved	—
1	FD	Terminate	DATA_COMPLETE
1	FE	Transmit error propagation	No applicable parameter
1	FF	Reserved	—
NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			

46.3.1.3 TXD<31:0> (transmit data)

TXD is a bundle of 32 data signals organized into four lanes of eight signals each (TXD<7:0>, TXD<15:8>, TXD<23:16>, and TXD<31:24>) that are driven by the RS. Each lane is associated with a TXC signal as shown in Table 46–2 and shall be encoded as shown in Table 46–3. TXD<31:0> shall transition synchronously with respect to both the rising and falling edges of TX_CLK. For each high or low TX_CLK transition, data and/or control are presented on TXD<31:0> to the PHY for transmission. TXD<0> is the least significant bit of lane 0, TXD<8> the least significant bit of lane 1, TXD<16> the least significant bit of lane 2, and TXD<24> the least significant bit of lane 3.

Assertion on a lane of appropriate TXD values when TXC is asserted will cause the PHY to generate code-groups associated with either Idle, Start, Terminate, Sequence, or Error control characters. While the TXC of a lane is de-asserted, TXD of the lane is used to request the PHY to generate code-groups corresponding to the data octet value of TXD. An example of normal frame transmission is illustrated in Figure 46–5.

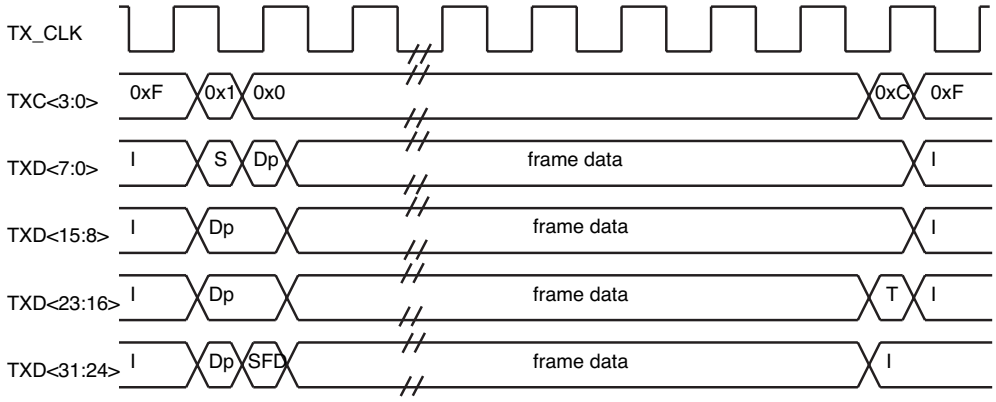
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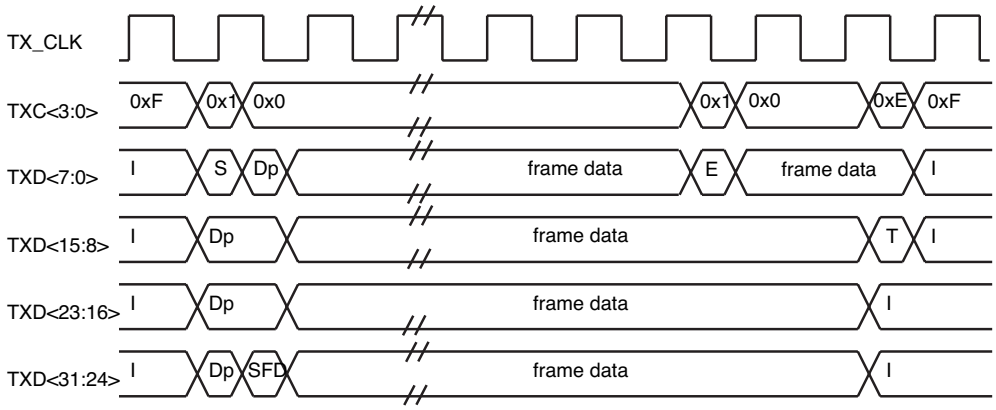
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Figure 46–6 shows the behavior of TXD and TXC during an example transmission of a frame propagating an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–5—Normal frame transmission



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character

Figure 46–6—Transmit Error Propagation

46.3.1.4 Start control character alignment

On transmit, it may be necessary for the RS to modify the length of the <inter-frame> in order to align the Start control character (first octet of preamble) on lane 0. This shall be accomplished in one of the following two ways:

1) A MAC implementation may incorporate this RS function into its design and always insert additional idle characters to align the start of preamble on a four byte boundary. Note that this will reduce the effective data rate for certain packet sizes separated with minimum inter-frame spacing.

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2) Alternatively, the RS may maintain the effective data rate by sometimes inserting and sometimes deleting idle characters to align the Start control character. When using this method the RS must maintain a Deficit Idle Count (DIC) that represents the cumulative count of idle characters deleted or inserted. The DIC is incremented for each idle character deleted, decremented for each idle character inserted, and the decision of whether to insert or delete idle characters is constrained by bounding the DIC to a minimum value of zero and maximum value of three. Note that this may result in inter-frame spacing observed on the transmit XGMII that is up to three octets shorter than the minimum transmitted inter-frame spacing specified in Clause 4; however, the frequency of shortened inter-frame spacing is constrained by the DIC rules. The DIC is only reset at initialization and is applied regardless of the size of the IPG transmitted by the MAC sublayer. An equivalent technique may be employed to control RS alignment of the Start control character provided that the result is the same as if the RS implemented DIC as described.

46.3.2 Receive

46.3.2.1 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RXC<3:0> and RXD<31:0> signals from the PHY to the RS. RXC<3:0> and RXD<31:0> shall be sampled by the RS on both the rising and falling edge of RX_CLK. RX_CLK is sourced by the PHY.

The frequency of RX_CLK may be derived from the received data or it may be that of a nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be 156.25 MHz ±0.01%, one-sixty-fourth of the MAC receive data rate.

There is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference. Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall not decrease the time between adjacent edges of RX_CLK.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals.

46.3.2.2 RXC<3:0> (receive control)

RXC<3:0> indicate that the PHY is presenting either recovered and decoded data or control characters on the XGMII. The RXC signal for a lane shall be de-asserted when a data octet is being received on the corresponding lane and asserted when a control character is being received. In the absence of errors, the RXC signals are de-asserted by the PHY for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be received are presented on the lanes of the XGMII. RXC<3:0> are driven by the PHY and shall transition synchronously with respect to both the rising and falling edges of RX_CLK. Table 46–4 specifies the permissible encodings of RXD and RXC for a XGMII receive lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Figure 46–7 shows the behavior of RXC<3:0> during an example frame reception with no errors.

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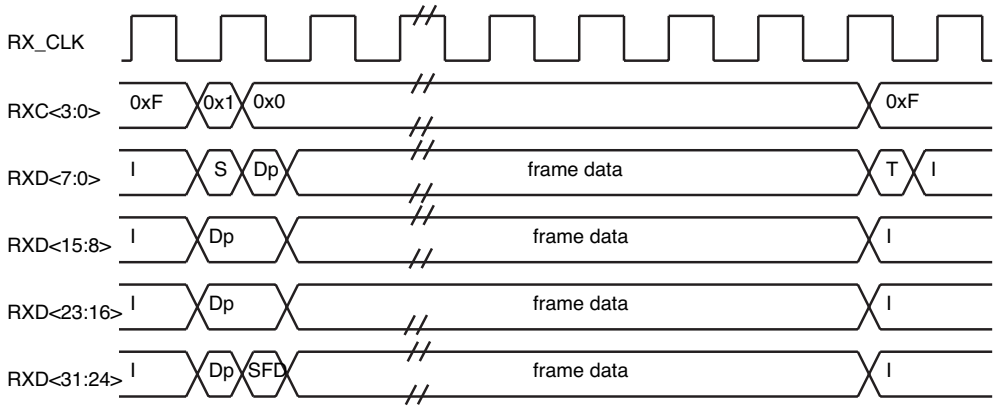
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Table 46–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indicate parameter
0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	00 through 06	Reserved	—
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, first eight ZERO, ONE of a frame (a preamble octet)
1	FC	Reserved	—
1	FD	Terminate	No applicable parameter (Start of inter-frame)
1	FE	Receive error	No applicable parameter
1	FF	Reserved	—

NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–7—Basic frame reception

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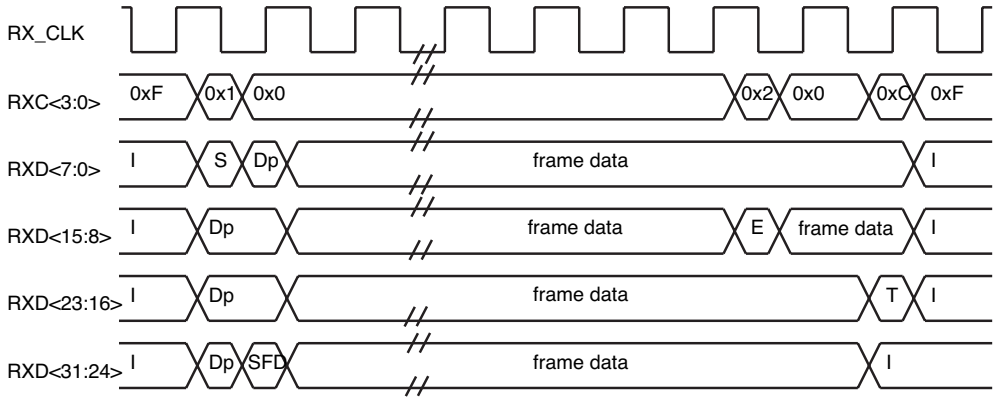
46.3.2.3 RXD (receive data)

RXD is a bundle of 32 data signals (RXD<31:0>) organized into four lanes of eight signals each (RXD<7:0>, RXD<15:8>, RXD<23:16>, and RXD<31:24>) that are driven by the PHY. Each lane is associated with a RXC signal as shown in Table 46–2 and shall be decoded by the RS as shown in Table 46–4. RXD<31:0> shall transition synchronously with respect to both the rising and falling edges of RX_CLK. For each high or low RX_CLK transition, received data and/or control are presented on RXD<31:0> for mapping by the RS. RXD<0> is the least significant bit of lane 0, RXD<8> the least significant bit of lane 1, RXD<16> the least significant bit of lane 2, and RXD<24> the least significant bit of lane 3. Figure 46–7 shows the behavior of RXD<31:0> during frame reception.

While the RXC of a lane is de-asserted, RXD of the lane is used by the RS to generate PLS_DATA.indicate transactions. Assertion on a lane of appropriate RXD values when RXC is asserted indicates to the RS the Start control character, Terminate control character, Sequence control character, or Error control character that drive its mapping functions.

RXC of a lane is asserted with the appropriate Error control character encoding on RXD of the lane to indicate an error was detected somewhere in the frame presently being transferred from the PHY to the RS (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer).

The effect of an Error control character on the RS is defined in 46.3.3.1. Figure 46–8 shows the behavior of RXC and RXD during the reception of an example frame with an error.



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character, E: Error control character

Figure 46–8—Reception with error

46.3.3 Error and fault handling

46.3.3.1 Response to error indications by the XGMII

If, during frame reception (i.e., when DATA_VALID_STATUS = DATA_VALID), a control character other than a Terminate control character is signaled on a received lane, the RS shall ensure that the MAC will detect a FrameCheckError in that frame. This requirement may be met by incorporating a function in the RS that produces a received frame data sequence delivered to the MAC sublayer that is guaranteed to not yield a

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valid CRC result, as specified by the frame check sequence algorithm (see 3.2.8). This data sequence may be produced by substituting data delivered to the MAC. The RS generates eight PLS_DATA.indicate primitives for each Error control character received within a frame, and may generate eight PLS_DATA.indicate primitives to ensure FrameCheckError when a control character other than Terminate causes the end of the frame.

Other techniques may be employed to respond to a received Error control character provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

46.3.3.2 Conditions for generation of transmit Error control characters

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then an Error control character may be asserted on a transmit lane by the appropriate encoding of the lane's TXD and TXC signals.

46.3.3.3 Response to received invalid frame sequences

The 10 Gb/s PCS is required to either preserve the column alignment of the transmitting RS, or align the Start control character to lane 0. The RS shall not indicate DATA_VALID to the MAC for a Start control character received on any other lane. Error free 10 Gb/s operation will not change the SFD alignment in lane 3. A 10 Gb/s MAC/RS implementation is not required to process a packet that has an SFD in a position other than lane 3 of the column following the column containing the Start control character.

46.3.4 Link fault signaling

Link fault signaling operates between the remote RS and the local RS. Faults detected between the remote RS and the local RS are received by the local RS as Local Fault. Only an RS originates Remote Fault signals.

Sublayers within the PHY are capable of detecting faults that render a link unreliable for communication. Upon recognition of a fault condition a PHY sublayer indicates Local Fault status on the data path. When this Local Fault status reaches an RS, the RS stops sending MAC data, and continuously generates a Remote Fault status on the transmit data path (possibly truncating a MAC frame being transmitted). When Remote Fault status is received by an RS, the RS stops sending MAC data, and continuously generates Idle control characters. When the RS no longer receives fault status messages, it returns to normal operation, sending MAC data.

Status is signaled in a four byte Sequence ordered_set as shown in Table 46–5. The PHY indicates Local Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x01 in lane 3. The RS indicates a Remote Fault with a Sequence control character in lane 0 and data characters of 0x00 in lanes 1 and 2 plus a data character of 0x02 in lane 3. Though most fault detection is on the receive data path of a PHY, in some specific sublayers, faults can be detected on the transmit side of the PHY. This is also indicated by the PHY with a Local Fault status.

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Table 46–5—Sequence ordered_sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	≥ 0x00	≥ 0x00	≥ 0x03	Reserved
NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state machine allows future standardization of reserved Sequence ordered sets for functions other than link fault indications				

The RS reports the fault status of the link. Local Fault indicates a fault detected on the receive data path between the remote RS and the local RS. Remote Fault indicates a fault on the transmit path between the local RS and the remote RS. The RS shall implement the link fault signaling state machine (see Figure 46–9).

46.3.4.1 Conventions

The notation used in the state diagram follows the conventions of 21.5. The notation ++ after a counter indicates it is to be incremented.

46.3.4.2 Variables and counters

The link fault signaling state machine uses the following variables and counters:

col_cnt
: A count of the number of columns received not containing a fault_sequence. This counter increments at RX_CLK rate (on both the rising and falling clock transitions) unless reset.

fault_sequence
: A new column received on RXC<3:0> and RXD<31:0> comprising a Sequence ordered_set of four bytes and consisting of a Sequence control character in lane 0 and a seq_type in lanes 1, 2, and 3 indicating either Local Fault or Remote Fault.

last_seq_type
: The seq_type of the previous Sequence ordered_set received
Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.

link_fault
: An indicator of the fault status.
Values: OK; No fault.
Local Fault; fault detected by the PHY.
Remote Fault; fault detection signaled by the remote RS.

reset
: Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
Values: FALSE: The device is completely powered and has not been reset (default).
TRUE: The device has not been completely powered or has been reset.

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seq_cnt
A count of the number of received Sequence ordered_sets of the same type.
seq_type
The value received in the current Sequence ordered_set
Values: Local Fault; 0x00 in lane 1, 0x00 in lane 2, 0x01 in lane 3.
Remote Fault; 0x00 in lane 1, 0x00 in lane 2, 0x02 in lane 3.

46.3.4.3 State Diagram

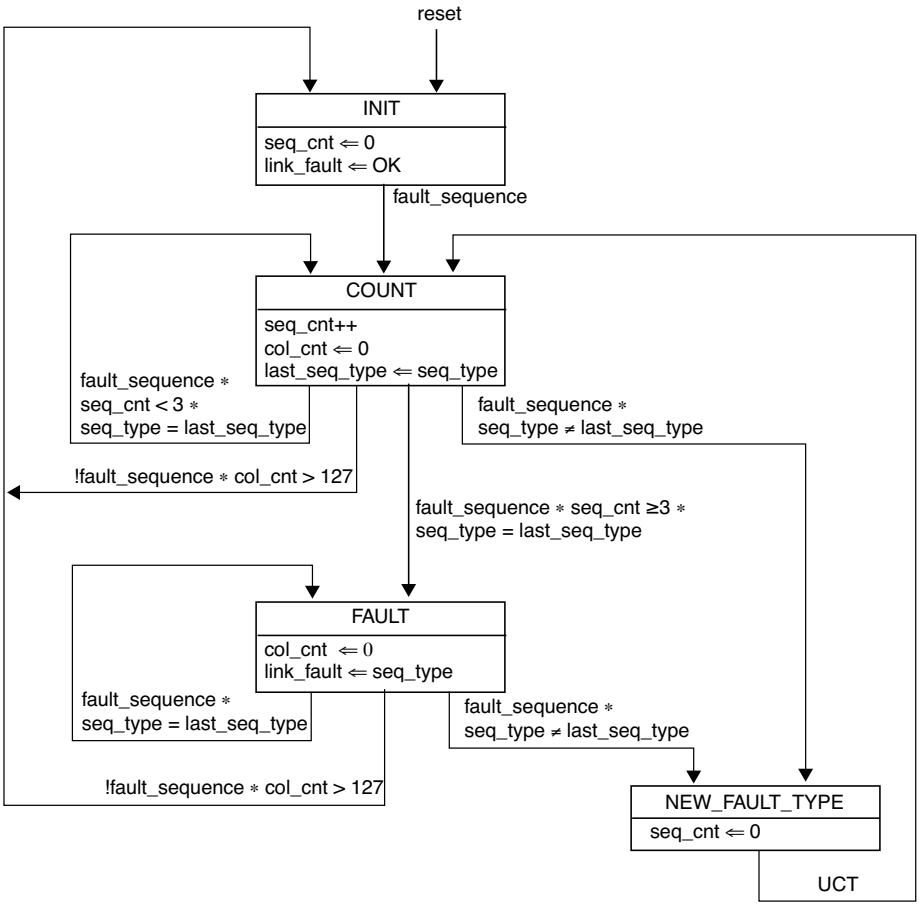


Figure 46–9—Link Fault Signaling State Diagram

The link fault signaling state machine specifies the RS monitoring of RXC<3:0> and RXD<31:0> for Sequence ordered_sets. The variable link_fault is set to indicate the value of a received Sequence ordered_set when four fault_sequences containing the same fault value have been received with each pair of fault sequences separated by less than 128 columns and no intervening fault_sequences of a different fault value.

The variable link_fault is set to OK following any interval of 128 columns not containing a Remote Fault or Local Fault Sequence ordered_set.

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The RS output onto TXC<3:0> and TXD<31:0> is controlled by the variable link_fault.

a) link_fault = OK
The RS shall send MAC frames as requested through the PLS service interface. In the absence of MAC frames, the RS shall generate Idle control characters.
b) link_fault = Local Fault
The RS shall continuously generate Remote Fault Sequence ordered_sets.
c) link_fault = Remote Fault
The RS shall continuously generate Idle control characters.

46.4 XGMII electrical characteristics

The electrical characteristics of the XGMII are specified such that the XGMII can be applied within a variety of 10 Gb/s equipment types. The electrical specifications are selected for an integrated circuit to integrated circuit application. The electrical characteristics specified in this clause apply to all XGMII signals.

When implemented as a chip-to-chip interface, the XGMII uses High Speed Transceiver Logic (HSTL), specified for a 1.5 volt output buffer supply voltage. XGMII chip-to-chip signals shall comply with EIA/JEDEC Standard EIA/JESD8-6 using Class I, output buffers. Output impedance shall be greater than 38Ω to assure acceptable overshoot and undershoot performance in an unterminated interconnection.

The thresholds and parametric values for HSTL XGMII signals are shown in the informative Figure 46–10 and informative Table 46–6.

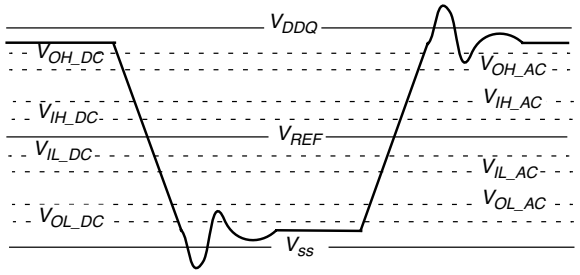


Figure 46–10—Electrical characteristics (informative)

Table 46–6—DC and AC specifications (informative)

Symbol	Parameter	Min	Nom	Max	Units
V_{DDQ}	Output supply voltage	1.4	1.5	1.6	V
V_{REF}	Input reference voltage	0.68	0.75	0.90	V
V_{IH_DC}	DC input logic high	V_{REF}+0.10	—	V_{DDQ}+0.3	V
V_{IL_DC}	DC input logic low	–0.30	—	V_{REF}–0.1	V
V_{IH_AC}	AC input logic high	V_{REF}+0.20	—	—	V
V_{IL_AC}	AC input logic low	—	—	V_{REF}–0.20	V

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The HSTL specification shows a number of termination options for different applications. Informative Figure 46–11 illustrates a possible XGMII circuit topology. Unterminated interconnection is recommended.

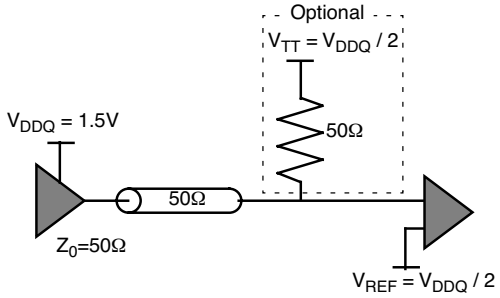
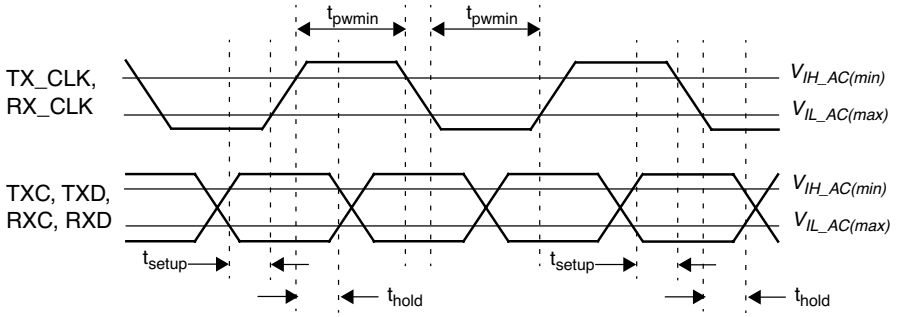


Figure 46–11—Circuit topology example (informative)

The XGMII chip-to-chip signals shall meet the timing requirements shown in Figure 46–12. All XGMII timing measurements shall be made at the XGMII driver output with the optional termination shown in Figure 46–11 and with a capacitive load from all sources of 10pF and are specified relative to the $V_{IL\_AC(max)}$ and $V_{IH\_AC(min)}$ thresholds.



Symbol	Driver	Receiver	Units
t_{setup}	960	480	ps
t_{hold}	960	480	ps
t_{pwmin}	2.5	—	ns

Figure 46–12—TX_CLK and RX_CLK timing parameters

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46.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[5]

46.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

46.5.2 Identification

46.5.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

46.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	

Date of Statement	

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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46.5.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY	PHY support of XGMII	46.2, 46.3		O	Yes [ ] No [ ]
*RS	Reconciliation Sublayer support of XGMII	46.2, 46.3		O	Yes [ ] No [ ]
*XGE	XGMII electrical interface	46.4		O	Yes [ ] No [ ]

46.5.3 PICS proforma Tables for Reconciliation Sublayer and 10 Gigabit Media Independent Interface

46.5.3.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of MAC data rate	46.1.3	Support MAC data rate of 10 Gb/s	PHY:M	Yes [ ] N/A [ ]
G2	Cumulative MAC Control, MAC and RS round-trip delay	46.1.4	Per Table 46–1	RS:M	Yes [ ] N/A [ ]
G3	Lane structure	46.1.6	Per Table 46–2	M	Yes [ ]

46.5.3.2 Mapping of PLS service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
PL1	Mapping to Clause 6	46.1.7	RS implements mapping to Clause 6 PLS service primitives	RS:M	Yes [ ] N/A [ ]
PL2	Mapping of PLS_DATA.requests	46.1.7.1.4	In sequence TXD<0> to TXD<31>	RS:M	Yes [ ] N/A [ ]
PL3	Start control character creation	46.1.7.1.4	First octet of preamble converted to Start control character	RS:M	Yes [ ] N/A [ ]
PL4	TXD and TXC generation	46.1.7.1.4	For each 32 PLS_DATA.requests	RS:M	Yes [ ] N/A [ ]
PL5	Terminate control character creation	46.1.7.1.4	DATA_COMPLETE causes creation of Terminate control character in next lane in sequence	RS:M	Yes [ ] N/A [ ]
PL6	Mapping RXD to PLS_DATA.incicates	46.1.7.2.3	Create PLS_DATA.increments in sequence from RXD<0> to RXD<31>	RS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PL7	PLS_DATA.indicate generation	46.1.7.2.3	Generate 32 PLS_DATA.indicates for each RXD<0:31> until Terminate then generating 0, 8, 16, or 24	RS:M	Yes [ ] N/A [ ]
PL8	Start control character conversion	46.1.7.2.3	Convert valid Start control character to preamble before generating PLS_DATA.indicates	RS:M	Yes [ ] N/A [ ]
PL9	Terminate control character	46.1.7.2.3	No PLS_DATA.indicates generated	RS:M	Yes [ ] N/A [ ]
PL10	PLS_DATA_VALID.indicate generation	46.1.7.5.3	On change of value of DATA_VALID_STATUS	RS:M	Yes [ ] N/A [ ]
PL11	DATA_VALID_STATUS	46.1.7.5.3	Value of DATA_VALID on a lane 0 Start control character preceeded by four idles or a Sequence ordered set	RS:M	Yes [ ] N/A [ ]
PL12	DATA_VALID_STATUS	46.1.7.5.3	Value of DATA_NOT_VALID on any control character but Error	RS:M	Yes [ ] N/A [ ]
PL13	Frame not ending with Terminate control character	46.1.7.5.3	Ensure MAC detects CRC error	RS:M	Yes [ ] N/A [ ]

46.5.3.3 Data stream structure

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Frame transfer	46.2	Within XGMII data stream	RS:M	Yes [ ] N/A [ ]
DS2	Bit mapping	46.2	Per Figure 46–4	RS:M	Yes [ ] N/A [ ]
DS3	Content of <data>	46.2.3	Consist of data octets	RS:M	Yes [ ] N/A [ ]
DS4	Recognition of <efd>	46.2.4	Terminate recognized in any lane	RS:M	Yes [ ] N/A [ ]

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46.5.3.4 XGMII signal functional specifications

NOTE—An XGXS adjacent to an RS exhibits the characteristics of a PHY for the items in this subclause, and an XGXS adjacent to a PCS exhibits the characteristics of an RS for the items in this subclause.

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	TX_CLK active edges	46.3.1.1	TXD and TXC sampled on both edges of TX_CLK	XGE:M	Yes [ ] N/A [ ]
FS2	TX_CLK frequency	46.3.1.1	156.25 MHz ± 0.01%	XGE:M	Yes [ ] N/A [ ]
FS3	TXC assertion and de-assertion	46.3.1.2	De-asserted for data, asserted for control character	RS:M	Yes [ ] N/A [ ]
FS4	TXC clock	46.3.1.2	Synchronous to TX_CLK	XGE:M	Yes [ ] N/A [ ]
FS5	TXD encoding	46.3.1.3	Per Table 46–3	RS:M	Yes [ ] N/A [ ]
FS6	TXD clock	46.3.1.3	Synchronous to TX_CLK	XGE:M	Yes [ ] N/A [ ]
FS7	Start alignment	46.3.1.4	Start control character aligned to lane 0	RS:M	Yes [ ] N/A [ ]
FS8	RX_CLK active edges	46.3.2.1	RXD and RXC sampled on both edges of RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS9	RX_CLK frequency	46.3.2.1	156.25 MHz ± 0.01% when received data rate is within tolerance	XGE:M	Yes [ ] N/A [ ]
FS10	Loss of receive signal	46.3.2.1	Source RX_CLK from nominal clock	PHY:M	Yes [ ] N/A [ ]
FS11	Transition between clock sources	46.3.2.1	No decrease of RX_CLK period when switching sources	PHY:M	Yes [ ] N/A [ ]
FS12	RXC assertion and de-assertion	46.3.2.2	De-asserted for data, asserted for control character	PHY:M	Yes [ ] N/A [ ]
FS13	RXC clock	46.3.2.2	Synchronous to RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS14	RXD decoding	46.3.2.3	Per Table 46–4	RS:M	Yes [ ] N/A [ ]
FS15	RXD clock	46.3.2.3	Synchronous to RX_CLK	XGE:M	Yes [ ] N/A [ ]
FS16	Received Error control character	46.3.3.1	RS cause MAC FrameCheck-Error	RS:M	Yes [ ] N/A [ ]
FS17	DATA_VALID assertion	46.3.3.3	RS not assert DATA_VALID unless Start control character in lane 0	RS:M	Yes [ ] N/A [ ]

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46.5.3.5 Link fault signaling state machine

Item	Feature	Subclause	Value/Comment	Status	Support
LF1	Link fault signaling state machine	46.3.4	Implement per Figure 46–9	RS:M	Yes [ ] N/A [ ]
LF2	link_fault = OK and MAC frames	46.3.4.3	RS services MAC frame transmission requests	RS:M	Yes [ ] N/A [ ]
LF3	link_fault = OK and no MAC frames	46.3.4.3	In absence of MAC frames, RS transmits Idle control characters	RS:M	Yes [ ] N/A [ ]
LF4	link_fault = Local Fault	46.3.4.3	RS transmits continuous Remote Fault Sequence ordered_sets	RS:M	Yes [ ] N/A [ ]
LF5	link_fault = Remote Fault	46.3.4.3	RS transmits continuous Idle control characters	RS:M	Yes [ ] N/A [ ]

46.5.3.6 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	Referenced standard for signals	46.4	Signals to be compliant with EIA/JESD8-6 using Class I, output buffers	XGE:M	Yes [ ] N/A [ ]
EC2	Output impedance	46.4	Signal output impedance of at least 38Ω	XGE:M	Yes [ ] N/A [ ]
EC3	Signal timing	46.4	Per Figure 46–12	XGE:M	Yes [ ] N/A [ ]
EC4	Signal measurement	46.4.2.3	At driver output with optional termination per Figure 46–11 and with a capacitive load from all sources of 10pF	XGE:M	Yes [ ] N/A [ ]

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47. XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)

47.1 Overview

This clause defines the functional and electrical characteristics for the optional XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI). Figure 47–1 shows the relationships of the XGMII, XGMII Extender, XGXS, and XAUI.

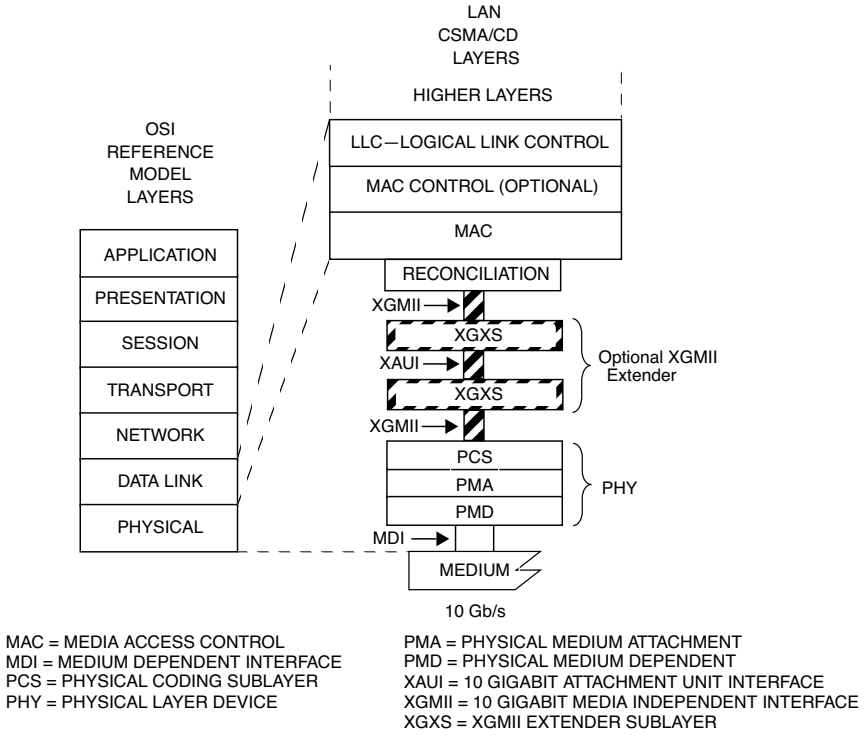


Figure 47–1—XAUI and XGXS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of the XGMII Extender, which is comprised of an XGXS at the RS end (DTE XGXS), an XGXS at the PHY end (PHY XGXS) and a XAUI between them, is to extend the operational distance of the XGMII and to reduce the number of interface signals. Applications include extending the physical separation possible between MAC and PHY components in a 10 Gigabit Ethernet system distributed across a circuit board.

The optional XGMII Extender has the following characteristics:

a) Simple signal mapping to the XGMII
b) Independent transmit and receive data paths
c) Four lanes conveying the XGMII 32-bit data and control
d) Differential signaling with low voltage swing
e) Self-timed interface allows jitter control to the PCS
f) Shared technology with other 10 Gb/s interfaces
g) Shared functionality with other 10 Gb/s Ethernet blocks
h) Utilization of 8B/10B coding

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47.1.1 Summary of major concepts

The following is a list of the major concepts of XGXS and XAUI:

a) The optional XGMII Extender can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the physical reach of the XGMII and reduce the interface pin count.
b) The XGMII is organized into four lanes with each lane conveying a data octet or control character on each edge of the associated clock. The source XGXS converts bytes on an XGMII lane into a self clocked, serial, 8B/10B encoded data stream. Each of the four XGMII lanes is transmitted across one of the four XAUI lanes.
c) The source XGXS converts XGMII Idle control characters (interframe) into an 8B/10B code sequence. The destination XGXS recovers clock and data from each XAUI lane and deskews the four XAUI lanes into the single-clock XGMII.
d) The destination XGXS adds to or deletes from the interframe as needed for clock rate disparity compensation prior to converting the interframe code sequence back into XGMII Idle control characters.
e) The XGXS uses the same code and coding rules as the 10GBASE-X PCS and PMA specified in Clause 48.

47.1.2 Application

This clause applies to the XGMII between the MAC and PHY. The implementation of the optional XGMII Extender is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board. Where the XGMII is electrically limited to distances of approximately 7 cm, the XGMII Extender allows distances up to approximately 50 cm.

47.1.3 Rate of operation

The XGMII Extender supports the 10 Gb/s data rate of the XGMII. The 10 Gb/s MAC data stream is converted into four lanes at the XGMII (by the Reconciliation Sublayer for transmit or the PHY for receive). The byte stream of each lane is 8B/10B encoded by the XGXS for transmission across the XAUI at a nominal rate of 3.125 GBaud. The XGXS at the PHY end of the XGMII Extender (PHY XGXS) and the XGXS at the RS end (DTE XGXS) may operate on independent clocks.

47.1.4 Allocation of functions

The XGMII Extender is transparent to the Reconciliation Sublayer and PHY device, and operates symmetrically with similar functions on the DTE transmit and receive data paths. The XGMII Extender is logically composed of two XGXSs interconnected with a XAUI data path in each direction. One XGXS acts as the source to the XAUI data path in the DTE transmit path and as the destination in the receive path. The other XGXS is the destination in the transmit path and source in the receive path. Each XAUI data path is composed of four serial lanes. All specifications for the XGMII Extender are written assuming conversion from XGMII to XAUI and back to XGMII, but other techniques may be employed provided that the result is that the XGMII Extender operates as if all specified conversions had been made. One example of this is the use of the optional XAUI with the 10GBASE-LX4 8B/10B PHY, where the XGXS interfacing to the Reconciliation Sublayer provides the PCS and PMA functionality required by the PHY. An XGXS layer is not required at the PHY end of the XAUI in this case. However, means may still be required to remove jitter introduced on the XAUI in order to meet PHY jitter requirements.

47.2 Functional specifications

At the source side of a XAUI, the XGXS takes XGMII data streams striped over four lanes as its input, maps XGMII data and control characters into XAUI code-groups, and encodes them for transmission. At the destination end of the XAUI, the XGXS decodes the code-groups, deskews the four lanes, compensates for

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clock rate disparity, and maps the XAUI code-groups back into XGMII data and control characters. Each XGXS is bidirectional, having both source and destination functionality. Figure 47–2 depicts a schematic representation of the XGXS inputs and outputs.

47.2.1 PCS and PMA functionality

The XGXS shall meet all mandatory portions of 48.2 and 48.3, and may meet any optional portions of 48.2 and 48.3. Since the PHY XGXS operates with the XGMII below the XAUI, the transmit requirements of 48.2 and 48.3 apply to the PHY XGXS receive requirements and the receive requirements apply to the PHY XGXS transmit functionality.

47.2.2 Delay constraints

The XGMII Extender shall meet the delay constraints in 48.5. The contribution of the XAUI interconnect is included in these delay constraints.

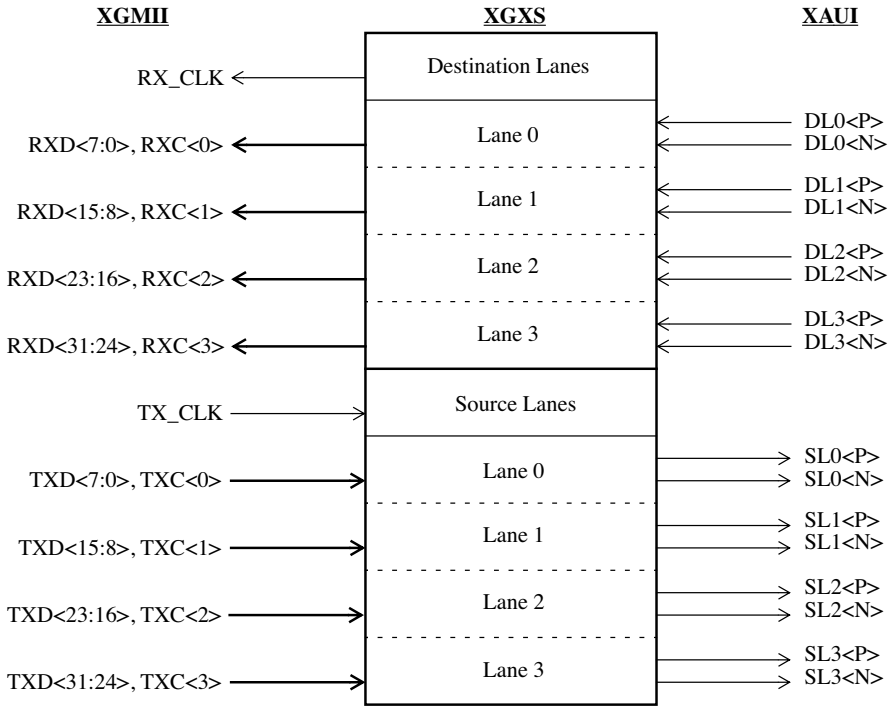


Figure 47–2—XGXS inputs and outputs

47.3 XAUI Electrical characteristics

The electrical characteristics of the XGMII Extender are specified such that it can be applied within a variety of 10 Gb/s Ethernet equipment types. There are two interface types associated with the XGMII Extender: the XGMII and XAUI. The electrical characteristics of both are selected for an integrated circuit to integrated circuit application. The electrical characteristics for the XGMII are specified in 46.4. The electrical characteristics for XAUI are specified in this section. Unless specified otherwise, the electrical characteristics defined in this subclause are applicable to all valid sequences of code-groups.

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47.3.1 Signal levels

The XAUI is a low swing AC coupled differential interface. AC coupling allows for interoperability between components operating from different supply voltages. Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI). Differential signal swings defined in 47.3 depend on several factors, such as transmitter pre-equalization and transmission line losses.

47.3.2 Signal paths

The XAUI signal paths are point-to-point connections. Each path corresponds to a XAUI lane and is comprised of two complementary signals making a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to approximately 50 cm over controlled impedance traces on standard FR4 printed circuit boards (PCBs).

47.3.3 Driver characteristics

The XAUI driver characteristics are summarized in Table 47–1. The XAUI Baud shall be 3.125 GBaud ±100 ppm. The corresponding Baud period is nominally 320 ps.

Table 47–1—Driver characteristics

Parameter	Value	Units
Baud rate tolerance	3.125 GBd ± 100 ppm	GBd ppm
Unit interval nominal	320	ps
Differential amplitude maximum	1600	mV_{p-p}
Absolute output voltage limits maximum minimum	 2.3 –0.4	 V V
Differential output return loss minimum	[See Equation (47-1)]	dB
Output jitter Near-end maximums Total jitter Deterministic jitter Far-end maximums Total jitter Deterministic jitter	 ± 0.175 peak from the mean ± 0.085 peak from the mean ± 0.275 peak from the mean ± 0.185 peak from the mean	 UI UI UI UI

47.3.3.1 Load

The load is 100 Ω ± 5% differential to 2.5 GHz for these measurements, unless otherwise noted.

47.3.3.2 Amplitude and swing

Driver differential output amplitude shall be less than 1600 mV_{p-p} including any transmit equalization. DC-referenced logic levels are not defined since the receiver is AC coupled. Absolute driver output voltage shall be between –0.4 V and 2.3 V with respect to ground. See Figure 47–3 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

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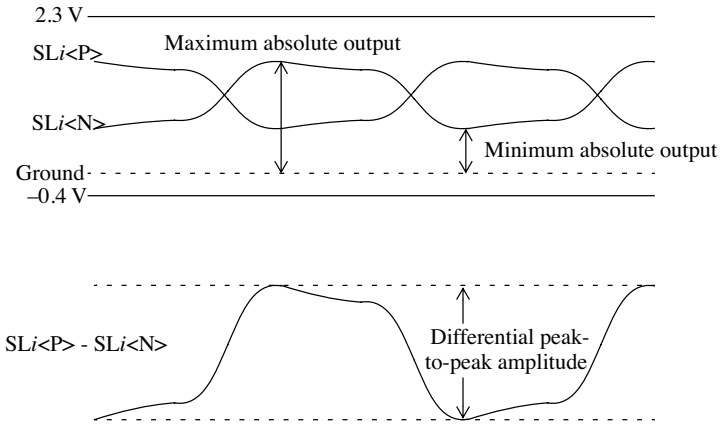


Figure 47–3—Driver output voltage limits and definitions
[L*i*<P> and L*i*<N> are the positive and negative sides of the differential signal pair for Lane *i* (*i* = 0, 1, 2, 3)]

47.3.3.3 Transition time

Differential transition times between 60 and 130 ps are recommended, as measured between the 20% and 80% levels. Shorter transitions may result in excessive high-frequency components and increase EMI and crosstalk. The upper recommended limit of 130 ps corresponds to a sine wave at the half Baud.

47.3.3.4 Output impedance

For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver shall exceed Equation (47-1). Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$s_{11} = -10 \text{ dB for } 312.5 \text{ MHz} < \text{Freq } (f) < 625 \text{ MHz, and} \quad (47\text{-}1)$$
$$-10 + 10\log(f/625) \text{ dB for } 625 \text{ MHz} <= \text{Freq } (f) = < 3.125 \text{ GHz}$$

47.3.3.5 Driver template and jitter

The driver shall satisfy either the near-end eye template and jitter requirements, or the far-end eye template and jitter requirements. The eye templates are given in Figure 47–4 and Table 47–2. The template measurement requirements are specified in 47.4.2. The jitter requirements at the near end are for a maximum total jitter of ± 0.175 UI peak from the mean and a maximum deterministic component of ± 0.085 UI peak from the mean. The far-end requirements are for a maximum total jitter of ± 0.275 UI peak from the mean and a maximum deterministic component of ± 0.185 UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak-to-peak total jitter value must be less than these total jitter values to claim compliance to the template requirements per the methods of 47.4.2. Jitter specifications include all but 10^{-12} of the jitter population. The maximum random jitter is equal to the maximum total jitter minus the actual deterministic jitter. Jitter measurement requirements are described in 47.4.3.

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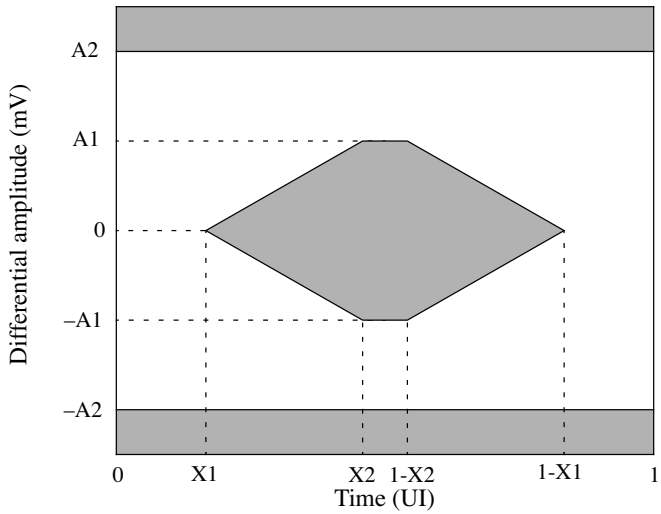


Figure 47–4—Driver template

Table 47–2—Driver template intervals

Symbol	Near-end value	Far-end value	Units
X1	0.175	0.275	UI
X2	0.390	0.400	UI
A1	400	100	mV
A2	800	800	mV

47.3.4 Receiver characteristics

Receiver characteristics are summarized in Table 47–3 and detailed in the following subclauses.

47.3.4.1 Bit error ratio

The receiver shall operate with a BER of better than 10^{-12} in the presence of a reference input signal as defined in 47.3.4.2.

47.3.4.2 Reference input signals

Reference input signals to a XAUI receiver have the characteristics determined by compliant XGXSs and XAUI drivers. Reference input signals satisfy the far-end template given in Figure 47–4 and Table 47–2 when the signal source impedance is 100 Ω ±5%. The template measurement requirements are specified in 47.4.2. Note that the input signal might not meet this template when this load is replaced by the actual receiver. Signal jitter does not exceed the jitter tolerance requirements specified in 47.3.4.6.

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Table 47–3—Receiver characteristics

Parameter	Value	Units
Baud rate tolerance	3.125 ±100	GBd ppm
Unit interval (UI) nominal	320	ps
Receiver coupling	AC	
Return loss[a] differential common mode	 10 6	 dB dB
Jitter amplitude tolerance[b]	0.65	UI_{p-p}

[a]Relative to 100 Ω differential and 25 Ω common mode. See 47.3.4.5 for input impedance details.
[b]See 47.3.4.6 for jitter tolerance details.

47.3.4.3 Input signal amplitude

XAUI receivers shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. Note that this may be larger than the 1600 mV_{p-p} maximum of 47.3.3.2 due to actual driver and receiver input impedances. The minimum input amplitude is defined by the far-end driver template and the actual receiver input impedance. Note that the far-end driver template is defined using a well controlled load impedance. The minimum signal amplitude into an actual receiver may vary from the minimum template height due to the actual receiver input impedance. Since the XAUI receiver is AC coupled to the XAUI, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

47.3.4.4 AC coupling

The XAUI receiver shall be AC coupled to the XAUI to allow for maximum interoperability between various 10 Gbps components. AC coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC coupling in actual implementations.

47.3.4.5 Input impedance

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to 2.5 GHz. This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode.

47.3.4.6 Jitter tolerance

The XAUI receiver shall have a peak-to-peak total jitter amplitude tolerance of at least 0.65 UI. This total jitter is composed of three components: deterministic jitter, random jitter, and an additional sinusoidal jitter. Deterministic jitter tolerance shall be at least 0.37 UI_{p-p}. Tolerance to the sum of deterministic and random jitter shall be at least 0.55 UI_{p-p}. The XAUI receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 47–5. This additional component is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects. Jitter specifications include all but 10^{-12} of the jitter population. Jitter tolerance test requirements are specified in 47.4.3.

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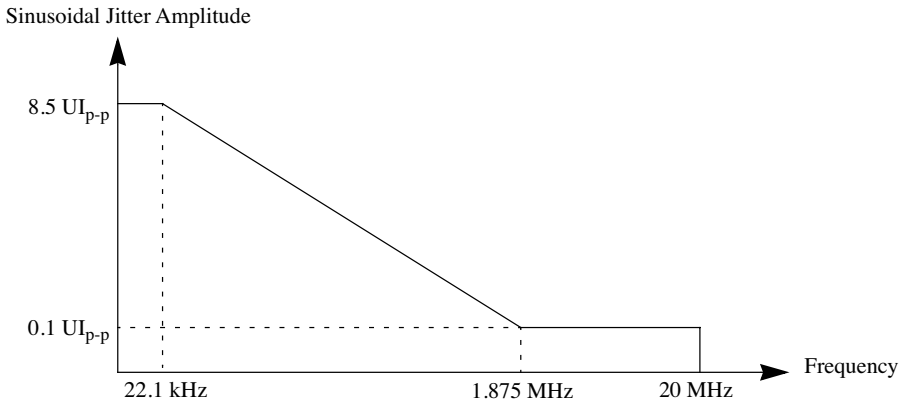


Figure 47–5—Single-tone sinusoidal jitter mask

47.3.5 Interconnect characteristics

The XAUI is primarily intended as a point-to-point interface of up to approximately 50 cm between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). Informative loss and jitter budgets are presented in Table 47–4 to demonstrate the feasibility of standard FR4 epoxy PCBs. The performance of an actual XAUI interconnect is highly dependent on the implementation. The compliance interconnect limit of 47.4.1 represents the median performance of a range of interconnect designs. The range included designs from 46 to 56 cm in total length, having trace widths of 0.125 to 0.300 mm, and using different grades and thicknesses of FR4. Interconnect configurations ranged from single-board designs to systems of two daughter cards mating to a backplane through high-speed electrical connectors.

Table 47–4—Informative XAUI loss, skew and jitter budget

	Loss (dB)[a]	Differential skew (ps_{p-p})	Total jitter (UI_{p-p})[c]	Deterministic jitter (UI_{p-p})[c]
Driver	0	15	0.35	0.17
Interconnect	7.5	60	0.20	0.20
Other[b]	4.5		0.10	0.10
Total	12.0	75	0.65	0.47

[a]Budgetary loss in height of eye opening.
[b]Includes such effects as crosstalk, noise, and interaction between jitter and eye height.
[c]Jitter specifications include all but 10^{-12} of the jitter population.

47.3.5.1 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10% from 100 MHz to 2.5 GHz.

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47.3.5.2 Connector impedance

The recommended impedance of any connectors, such as used between circuit board subsystems, is 100 Ω ± 30%.

47.4 Electrical measurement requirements

47.4.1 Compliance interconnect definition

The compliance interconnect is a 100 Ω differential system specified with respect to transmission magnitude response and intersymbol interference (ISI) loss. The compliance interconnect limits have been chosen to allow a realistic differential interconnect of about 50 cm length on FR4 epoxy PCB. See 47.3.5 for a more detailed description of the target XAUI interconnect. The transmission magnitude response, $|s_{21}|$, of the compliance interconnect in dB satisfies Equation (47-2).

$$s_{21}| \le |s_{21}|_{limit} = -20\log(e) \times [a_1\sqrt{f} + a_2 f + a_3 f^2 \quad (47\text{-}2)$$

where f is frequency in Hz, a_1=6.5 × 10^{-6}, a_2=2.0 × 10^{-10}, and a_3=3.3 × 10^{-20}. This limit applies from DC to 3.125 GHz. The magnitude response above 3.125 GHz does not exceed –11.4 dB. The ISI loss, defined as the difference in magnitude response between two frequencies, is greater than 4.0 dB between 312.5 MHz and 1.5625 GHz. The magnitude response and ISI loss limits are illustrated in Figure 47–6.

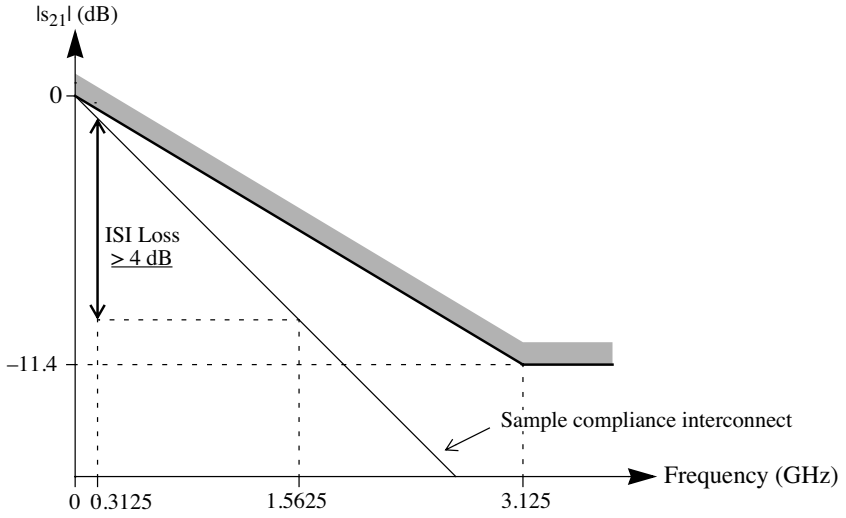


Figure 47–6—Compliance interconnect magnitude response and ISI loss

47.4.2 Eye template measurements

For the purpose of eye template measurements, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. See 48B.1.3 for an explanation of this technique. The data pattern for template measurements is the CJPAT pattern defined in Annex 48A. All XAUI lanes are active in both the transmit and receive directions, and opposite ends of the link use asynchronous clocks. The amount of data represented in the data eye must be adequate to ensure a bit error ratio of less than 10^{-12}. The eye template is measured with AC coupling and centered at 0 Volts differential. The left and right edges of the template are

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aligned with the mean zero crossing points of the measured data eye, as illustrated in Figure 47–7. The near-end load for this test is specified in 47.3.3.1. The far-end template is measured at the end of the compliance interconnect specified in 47.4.1. The far-end load for the compliance link is specified in 47.3.3.1.

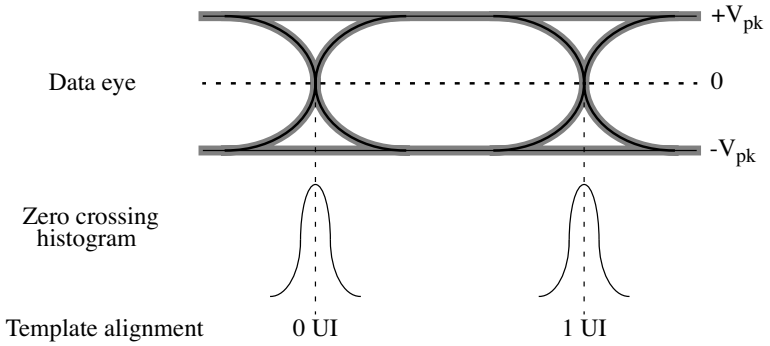


Figure 47–7—Eye template alignment

47.4.3 Jitter test requirements

For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements is the CJPAT pattern defined in Annex 48A. All four lanes of XAUI are active in both directions, and opposite ends of the link use asynchronous clocks. Jitter is measured with AC coupling and at 0 volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.

47.4.3.1 Transmit jitter

Transmit near-end jitter is measured at the driver output when terminated into the load specified in 47.3.3.1. Far-end jitter is measured at the end of a compliance interconnect specified in 47.4.1. The far-end load for the compliance link is specified in 47.3.3.1.

47.4.3.2 Jitter tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the required sum of deterministic and random jitter defined in 47.3.4.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the driver's template shown in Figure 47–4 and Table 47–2. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean of the zero crossing. If these symmetries are not achieved, then some portions of the test signal will encroach into the template and provide overstress of the receiver, and/or some points of the template may not be contacted, resulting in understress of the receiver. Eye template measurement requirements are given in 47.4.2. Random jitter is calibrated using a high pass filter with a low-frequency corner of 20 MHz and 20 dB/decade rolloff below this. The required sinusoidal jitter specified in 47.3.4.6 is then added to the signal and the far-end load is replaced by the receiver being tested.

47.5 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

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47.6 Protocol Implementation Conformance Statement (PICS) proforma for Clause 47, XGMII Extender (XGMII) and 10 Gigabit Attachment Unit Interface (XAUI)[6]

47.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Clause 47, XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

47.6.2 Identification

47.6.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

47.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 47, XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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47.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII compatibility interface	46, 47.1.4	Compatibility interface is supported	O	Yes [ ] No [ ]
MD	MDIO	47.2	Registers and interface supported	O	Yes [ ] No [ ]

47.6.4 PICS Proforma tables for XGXS and XAUI

47.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Environmental specifications	47.5		M	Yes [ ]

47.6.4.2 XGXS and XAUI functions

Item	Feature	Subclause	Value/Comment	Status	Support
F1	XGXS PCS and PMA requirements	47.2.1	Meet all mandatory requirements of 48.2 and 48.3	M	Yes [ ]
F2	XGXS PCS and PMA options	47.2.1	Meet optional clock rate compensation in unencoded data stream per 48.2.4.2.3	O	Yes [ ] No [ ]
F3	XGMII Extender delay	47.2.2	Meets delay constraints of 48.5	M	Yes [ ]

47.6.4.3 Electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
E1	XAUI Baud	47.3.3	3.125 GBd ± 100 ppm	M	Yes [ ]
E2	Driver output amplitude	47.3.3.2	Less than 1600 mV_{p-p}	M	Yes [ ]
E3	Driver output swing	47.3.3.2	Between –0.4 and +2.3 V	M	Yes [ ]
E4	Driver output impedance	47.3.3.4	s_{11} = –10 dB for 312.5 MHz < Freq (f) < 625 MHz, and –10 + 10log(f/625) dB for 625 MHz <= Freq (f) = < 3.125 GHz	M	Yes [ ]
E5	Driver near-end template and jitter	47.3.3.5	At driver output	O.1	Yes [ ] No [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
E6	Driver far-end template and jitter	47.3.3.5	At end of compliance interconnect	O.1	Yes [ ] No [ ]
E7	Receiver bit error ratio	47.3.4	Less than 10^{-12}	M	Yes [ ]
E8	Receive input amplitude tolerance	47.3.4.3	May be larger than 1600 mV_{p-p}	M	Yes [ ]
E9	Receiver coupling	47.3.4.4	AC-coupled	M	Yes [ ]
E10	Receiver input impedance	47.3.4.5	At least 10 dB differential and 6 dB common mode return loss	M	Yes [ ]
E11	Total jitter tolerance	47.3.4.6	At least 0.65 UI	M	Yes [ ]
E12	Deterministic jitter tolerance	47.3.4.6	At least 0.37 UI	M	Yes [ ]
E13	Tolerance to sum of deterministic and random jitter	47.3.4.6	At least 0.55 UI	M	Yes [ ]
E14	Additional sinusoidal jitter tolerance	47.3.4.6	Per Figure 47–5	M	Yes [ ]
E15	Jitter measurement	47.4.3	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]

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48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X

48.1 Overview

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 10 Gb/s Physical Layer implementations, collectively known as 10GBASE-X. The 10GBASE-LX4 PMD described in Clause 53 is a member of the 10GBASE-X PHY family. The term 10GBASE-X is used when referring to issues common to any of the variants within this family.

The 10GBASE-X PCS and PMA sublayers are also utilized by the XGXS specified in Clause 47.

10GBASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation Sublayer (RS) and the logical and electrical characteristics of the 10 Gigabit Media Independent Interface (XGMII). Although the XGMII is optional, it is used as the basis for the definition of the 10GBASE-X PCS and PMA sublayers.

10GBASE-X assumes the use of the MDIO interface and register set for communication between PHY and Station Management (STA) entities, see Clause 45.

10GBASE-X has the following characteristics:

a) The capability of supporting 10 Gb/s operation at the XGMII and RS
b) Clock references embedded in all data and control code-groups
c) Data paths consisting of independent serial links called lanes
d) Independent four-lane-wide transmit and receive data paths
e) Simple signal mapping to the XGMII and RS
f) Full duplex operation
g) Shared technology with other 10 Gb/s interfaces
h) Shared functionality with other 10 Gb/s Ethernet blocks

48.1.1 Objectives

The following are the objectives of 10GBASE-X:

a) Support the IEEE 802.3 MAC
b) Provide a data rate of 10 Gb/s at the XGMII
c) Support cable plants using optical fiber compliant with second edition of ISO/IEC 11801: 1995
d) Support a BER objective of 10^{-12}
e) Support the optional XAUI
f) Support link fault and error indications

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48.1.2 Relationship of 10GBASE-X to other standards

Figure 48–1 depicts the relationships among the 10GBASE-X sublayers (shown shaded), the IEEE 802.3 MAC and RS, and the IEEE 802.2 LLC.

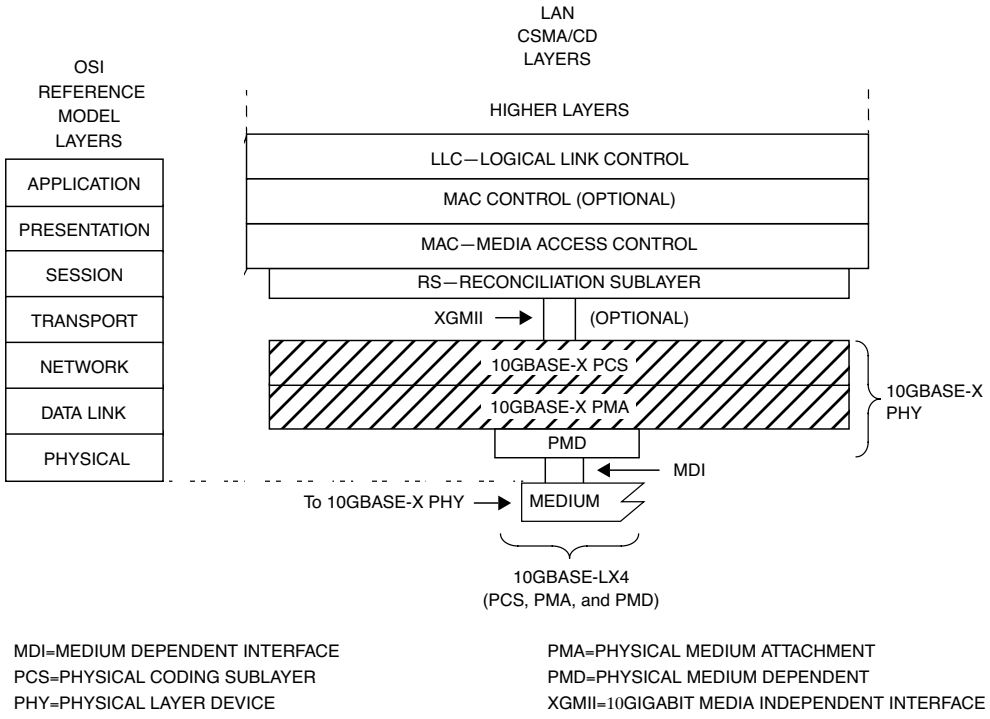


Figure 48–1—10GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE CSMA/CD LAN Model

48.1.3 Summary of 10GBASE-X sublayers

The following provides an overview of the 10GBASE-X sublayers.[7]

48.1.3.1 Physical Coding Sublayer (PCS)

The interface between the PCS and the RS is the XGMII as specified in Clause 46. The 10GBASE-X PCS provides services to the XGMII in a manner analogous to how the 1000BASE-X PCS provides services to the 1000 Mb/s GMII.

The 10GBASE-X PCS provides all services required by the XGMII and in support of the 10GBASE-X PMA, including:

a) Encoding of 32 XGMII data bits and 4 XGMII control bits to four parallel lanes conveying 10-bit code-groups each, for communication with the underlying PMA.
b) Decoding of four PMA parallel lanes, conveying 10-bit code-groups each, to 32 XGMII data bits and 4 XGMII control bits.
c) Synchronization of code-groups on each lane to determine code-group boundaries.

[7] The 10GBASE-X PHY consists of that portion of the Physical Layer between the MDI and XGMII consisting of the PCS, PMA, and PMD sublayers. The 10GBASE-X PHY is roughly analogous to the 1000BASE-X PHY.

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d) Deskew of received code-groups from all lanes to an alignment pattern.
e) Support of the MDIO interface and register set as specified in Clause 45 to report status and enable control of the PCS.
f) Conversion of XGMII Idle control characters to (from) a randomized sequence of code-groups to enable serial lane synchronization, clock rate compensation and lane-to-lane alignment.
g) Clock rate compensation protocol.
h) Link Initialization based on the transmission and reception of the Idle sequence.
i) Link status reporting for fault conditions.

48.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 10GBASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA service interface.
b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD.
c) Clock recovery from the code-groups supplied by the PMD.
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD service interface.
e) Direct passing of signal_detect from the PMD to the PCS through the PMA via the PMD and PMA service interfaces.

48.1.3.3 Physical Medium Dependent (PMD) sublayer

10GBASE-X supports the PMD sublayer and MDI specified in Clause 53. The 10GBASE-LX4 PMD performs the following functions:

a) Transmission of quad serial bit streams on the underlying medium.
b) Reception of quad serial bit streams on the underlying medium.

48.1.4 Rate of operation

The 10GBASE-X PCS and PMA support the 10 Gb/s MAC data rate. The line rate of each of four PMA lanes is 3.125 GBaud ± 100 ppm.

48.1.5 Allocation of functions

PCS and PMA functions directly map onto the 10GBASE-X PMD, MDI and medium which attach, in turn, to another 10GBASE-X PHY. In addition, 10GBASE-X PCS and PMA functions embodied in the XGXS described in Clause 47 may be used to attach to alternate 10 Gb/s PHYs such as 10GBASE-R or 10GBASE-W.

The longer interconnect distances afforded through the specification of a self-clocked serial architecture enable significant implementation flexibility while imposing a requirement on those implementations to ensure sufficient signal fidelity over the link. The implementer of this standard is expected to meet the required specifications in this and related clauses through implementation methods not specified by this standard.

48.1.6 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-X. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. Figure 48–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-X.

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Multiple optional physical instantiations of the PCS service interface have been defined. One is the XGMII described in Clause 46. The other is the interface to the XGXS described in Clause 47.

Physical instantiations of the 10GBASE-X PMA and PMD service interfaces are not defined in this standard.

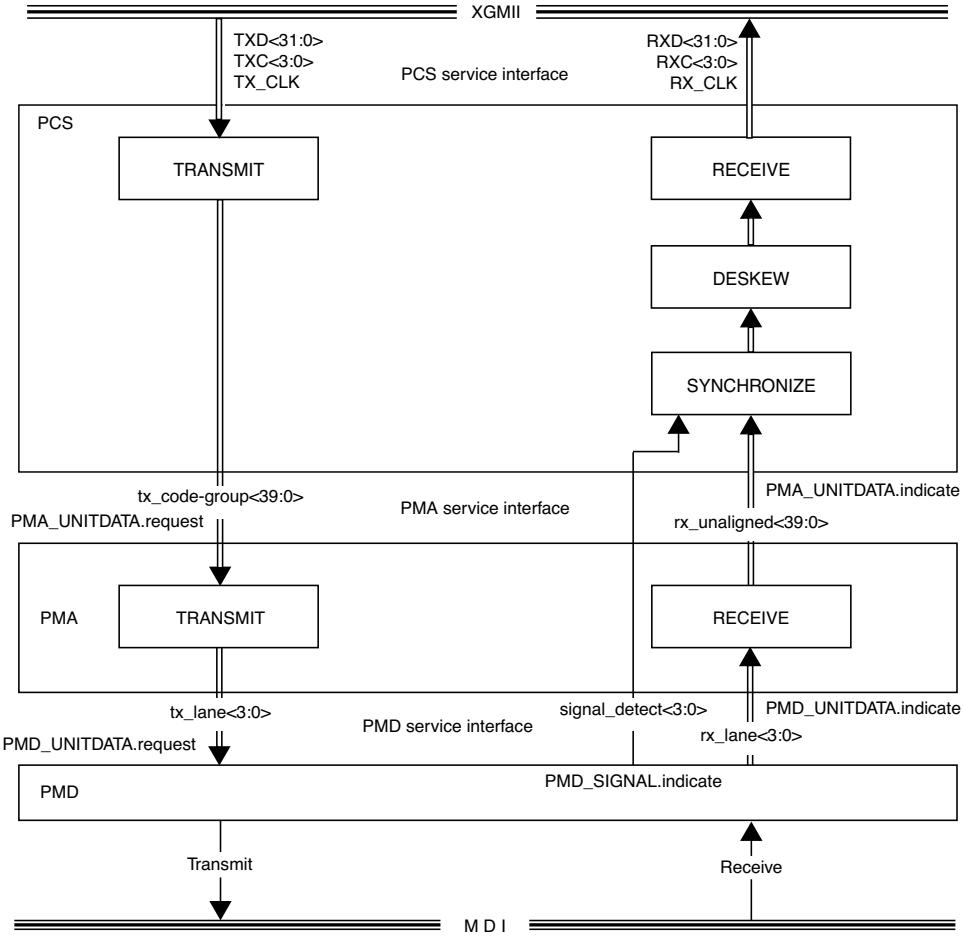


Figure 48–2—Functional block diagram

48.1.7 Functional block diagram

Figure 48–2 provides a functional block diagram of the 10GBASE-X PHY.

48.1.8 Special symbols

/x/ The code-group x is represented by preceding and following slash characters.

||y|| Four code-groups, one each in lanes 0 through 3 inclusive, synchronous to each other and arranged in a column identified by the value y, is represented by preceding and following double bar characters.

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48.2 Physical Coding Sublayer (PCS)

48.2.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-X PCS to transfer information to and from the PCS client. The PCS client is the RS defined in Clause 46, or the XGXS defined in Clause 47. An instantiation of the PCS service interface is the XGMII defined in Clause 46.

In the transmit direction, the 10GBASE-X PCS accepts packets from the PCS client on the XGMII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 10GBASE-X PCS maps XGMII data and control characters into a code-group stream. In the receive direction, the PCS decodes the code-group stream received from the PMA, maps the code-groups to XGMII data and control characters and forwards the character stream to the XGMII to the PCS client for further processing.

48.2.2 Functions within the PCS

The PCS includes the Transmit, Receive, Synchronization, and Deskew processes for 10GBASE-X. The PCS shields the RS (and MAC) from the specific nature of the underlying channel.

When communicating with the XGMII, the PCS uses, in each direction, 32 data signals (TXD <31:0> and RXD <31:0>), four control signals (TXC <3:0> and RXC <3:0>), and a clock (TX_CLK and RX_CLK).

When communicating with the PMA, the PCS uses the data signals tx_code-group <39:0> in the transmit direction and rx_unaligned <39:0> in the receive direction. Each set of data signals conveys four lanes of 10-bit code-groups. At the PMA service interface, code-group alignment, lane-to-lane deskew, and provision for PHY clock rate compensation are made possible by embedding special non-data code-groups in the idle stream. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

The tx_code-group and rx_unaligned signals are organized into four lanes in a manner similar to that of the XGMII. On transmit, the first PCS code-group is aligned to lane 0, the second to lane 1, the third to lane 2, the fourth to lane 3, then repeating with the fifth to lane 0, etc. This lane-oriented organization extends through the PMA to the PMD service interface. (See Table 48–1.)

Table 48–1—Transmit and receive lane associations

Lane	XGMII TXD RXD	XGMII TXC RXC	PMA tx_code-group rx_unaligned	PMD tx_lane rx_lane
0	<7:0>	<0>	<9:0>	<0>
1	<15:8>	<1>	<19:10>	<1>
2	<23:16>	<2>	<29:20>	<2>
3	<31:24>	<3>	<39:30>	<3>

The PCS Transmit process continuously generates code-groups based upon the TXD <31:0> and TXC <3:0> signals on the XGMII, sending them to the PMA service interface via the PMA_UNITDATA.request primitive.

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The PCS Synchronization process continuously accepts unaligned and unsynchronized code-groups via the PMA_UNITDATA.indicate primitive, obtains 10-bit code-group synchronization, and conveys synchronized 10-bit code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message. The PCS Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis).

The PCS Deskew process continuously accepts synchronized code-groups via the SYNC_UNITDATA.indicate message, aligns the code-groups to remove skew between the lanes that has been introduced by the link, and conveys aligned and synchronized code-groups to the PCS Receive process via the ALIGN_UNITDATA.indicate message. The PCS Deskew process asserts the align_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all PCS lanes. The PCS Deskew process attempts deskew and alignment whenever the align_status flag is de-asserted. The PCS Deskew process is otherwise idle.

The PCS Receive process continuously accepts code-groups from the PMA service interface via the ALIGN_UNITDATA.indicate message. The PCS Receive process monitors these code-groups and generates RXD and RXC on the XGMII. All code-groups received that represent idle are replaced with Idle characters prior to forwarding to the XGMII.

The PCS Transmit and Receive processes provide support for Link status reporting, which supports the transmit fault and receive fault conditions.

All PCS processes are described in detail in the state diagrams in 48.2.6.2.

48.2.3 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3.

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream.

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The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–4.

XGMII

T/RXD<7:0>	I	I	S	Dp	D	D	D	---	D	D	D	D	I	I	I	I	I	I
T/RXD<15:8>	I	I	Dp	Dp	D	D	D	---	D	D	D	T	I	I	I	I	I	I
T/RXD<23:16>	I	I	Dp	Dp	D	D	D	---	D	D	D	I	I	I	I	I	I	I
T/RXD<31:24>	I	I	Dp	Ds	D	D	D	---	D	D	D	I	I	I	I	I	I	I

PCS

LANE 0	K	R	S	Dp	D	D	D	---	D	D	D	D	A	R	R	K	K	R
LANE 1	K	R	Dp	Dp	D	D	D	---	D	D	D	T	A	R	R	K	K	R
LANE 2	K	R	Dp	Dp	D	D	D	---	D	D	D	K	A	R	R	K	K	R
LANE 3	K	R	Dp	Ds	D	D	D	---	D	D	D	K	A	R	R	K	K	R

Legend:
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

Figure 48–3—XGMII character stream to PCS code-group stream mapping example

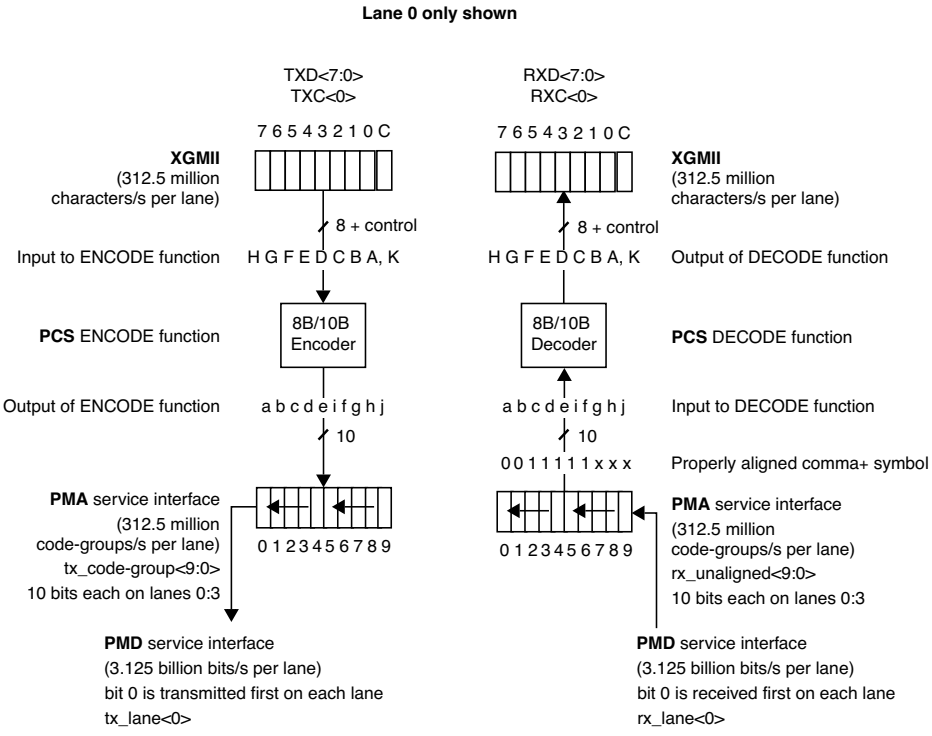


Figure 48–4—PCS reference diagram

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48.2.4 Ordered_sets and special code-groups

10GBASE-X PCS ordered_sets consist of combinations of special and data code-groups (defined as a column of code-groups). All ordered_sets are four code-groups in length and begin in lane 0. In addition to ordered_sets, the PCS defines several special code-groups for control purposes. Ordered_sets and special code-groups provide the following capabilities:

a) PCS Synchronization process ability to obtain bit and code-group synchronization
b) Packet delineation
c) Synchronization between the transmitter and receiver circuits at opposite ends of a link
d) Deskew of received code-groups from all serial lanes to an alignment pattern
e) Clock rate compensation protocol
f) Link status reporting protocol
g) Column fill
h) Error indication

Table 48–4 lists the defined ordered_sets and special code-groups.

Table 48–2—XGMII character to PCS code-group mapping

XGMII TXC	XGMII TXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	07	K28.0 or K28.3 or K28.5	Idle in ||I||
1	07	K28.5	Idle in ||T||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36-2	See Table 36-2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character
NOTE—Values in TXD column are in hexadecimal.			

48.2.4.1 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered_set, conveys one octet of data between the XGMII and the PCS. Any data code-group can be followed by any other data code-group. Data code-groups are encoded and decoded but not interpreted by the PCS.

48.2.4.2 Idle (/I/)

Idle ordered_sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD <31:0>=0x07070707 and TXC <3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

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Table 48–3—PCS code-group to XGMII character mapping

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data reception
1	07	K28.0 or K28.3 or K28.5	Idle in ‖I‖
1	07	K28.5	Idle in ‖T‖
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code-group	Received code-group
1	See Table 36-2	Other valid code-group	Received reserved code-group
NOTE—Values in RXD column are in hexadecimal.			

A sequence of ‖I‖ ordered_sets consists of one or more consecutively transmitted ‖K‖, ‖R‖ or ‖A‖ ordered_sets, as defined in Table 48–4. Rules for ‖I‖ ordered_set sequencing shall be as follows:

a) ‖I‖ sequencing starts with the first column following a ‖T‖.
b) The first ‖I‖ following ‖T‖ alternates between ‖A‖ or ‖K‖ except if an ‖A‖ is to be sent and less than r [see item d)] columns have been sent since the last ‖A‖, a ‖K‖ is sent instead.
c) ‖R‖ is chosen as the second ‖I‖ following ‖T‖.
d) Each ‖A‖ is sent after r non-‖A‖ columns where r is a uniform randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-‖A‖ columns between two ‖A‖ columns provides a theoretical 85-bit deskew capability.
e) When not sending an ‖A‖, either ‖K‖ or ‖R‖ is sent with a random uniform distribution between the two.
f) Whenever sync_status=OK, all ‖I‖ received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other !‖I‖ received during idle are mapped directly to XGMII data or control characters on a lane by lane basis.

The purpose of randomizing the ‖I‖ sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ‖I‖ sequence produces no discrete spectrum. Both ‖A‖ spacing as well as ‖K‖, ‖R‖, or ‖A‖ selection shall be based on the generation of a random integer r generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–5. ‖A‖ spacing is set to the next generated value of r. The rate of generation of r is once per column, 312.5 MHz ± 100 ppm. Once the ‖A‖ spacing count goes to zero (A_CNT=0), ‖A‖ is selected for transmission at the next opportunity during the Idle sequence. ‖K‖ and ‖R‖ selection follows the value of code_sel, which is continuously set according to the even or odd value of r. The method of generating the random integer r is left to the implementer. PCS Idle randomizer logic is illustrated in Figure 48–5

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Table 48–4—Defined ordered_sets and special code-groups

Code	Ordered_Set	Number of code-groups	Encoding
||I||	**Idle**		**Substitute for XGMII Idle**
||K||	Sync column	4	/K28.5/K28.5/K28.5/K28.5/
||R||	Skip column	4	/K28.0/K28.0/K28.0/K28.0/
||A||	Align column	4	/K28.3/K28.3/K28.3/K28.3/
	Encapsulation		
||S||	Start column	4	/K27.7/Dx.y/Dx.y/Dx.y/[a]
||T||	Terminate column	4	Terminate code-group in any lane
||T_0||	Terminate in Lane 0	4	/K29.7/K28.5/K28.5/K28.5/
||T_1||	Terminate in Lane 1	4	/Dx.y/K29.7/K28.5/K28.5/[a]
||T_2||	Terminate in Lane 2	4	/Dx.y/Dx.y/K29.7/K28.5/[a]
||T_3||	Terminate in Lane 3	4	/Dx.y/Dx.y/Dx.y/K29.7/[a]
	Control		
/E/	Error code-group	1	/K30.7/
	Link Status		
||Q||	Sequence ordered_set	4	/K28.4/Dx.y/Dx.y/Dx.y/[a]
||LF||	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
||RF||	Remote Fault signal	4	/K28.4/D0.0/D0.0/D2.0/
||Qrsvd||	Reserved	4	!||LF|| and !||RF||
	Reserved		
||Fsig||	Signal ordered_set	4	/K28.2/Dx.y/Dx.y/Dx.y/[a,b]

[a]/Dx.y/ indicates any data code-group.
[b]Reserved for INCITS T11.

.

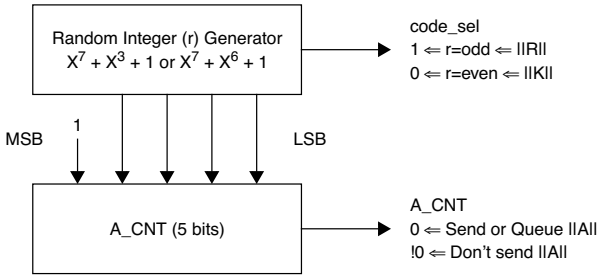


Figure 48–5—PCS idle randomizer

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48.2.4.2.1 Sync ||K||

Code-group synchronization is the process by which the receiver detects code-group boundaries in the incoming bit stream of each lane. The detection of the comma pattern in the incoming bit stream identifies a code-group boundary. The proper alignment of a comma used for code-group synchronization is depicted in Figure 48–4. The Sync or ||K|| ordered_set included in the PCS Idle sequence guarantees a sufficient frequency of commas in each lane. The comma pattern is defined in 36.2.4.9. The Sync ordered_set is defined in Table 48–4. /K/ code-groups are interpreted per lane by the PCS Synchronization process which is described in 48.2.6.2.2. Detection of both comma+ and comma- variants of /K/ shall be required.

48.2.4.2.2 Align ||A||

Skew is introduced between lanes by both active and passive elements of a 10GBASE-X link. The PCS deskew function compensates for all lane-to-lane skew observed at the receiver. The Align or ||A|| ordered_set consists of a unique special code-group, also known as Align or /A/ in each lane. /A/ is not used in any other ordered_set. The definition of a 10GBASE-X ordered_set guarantees that /A/ code-groups are simultaneously initiated on all lanes at the transmitter, resulting in minimal lane-to-lane skew at the transmitter. The Align ordered_set is defined in Table 48–4. Allowable skew for all link elements shall be as specified in Table 48–5.

Table 48–5—Skew budget

Skew Source	#	Skew	Total Skew
PMA Tx	1	1 UI[a]	1 UI
PCB	2	1 UI	2 UI
Medium	1	<18 UI	<18 UI
PMA Rx[b]	1	20 UI	20 UI
Total			<41 UI

[a]UI represents unit interval. For 10GBASE-X, 1 UI = 320 ps.
[b]Includes deserialization function, physical deserializer skew and clock boundary transition.

48.2.4.2.3 Skip ||R||

The 10GBASE-X PHY allows for multiple clock domains along a single link. The Skip or ||R|| ordered_set is included in the PCS Idle sequence to allow for clock rate compensation for the case of multiple clock domains. Clock rate compensation may be performed via insertion or removal of either Idle characters in the unencoded data stream or ||R|| in the encoded Idle stream. Any ||R|| may be removed. ||R|| may be inserted anywhere in the Idle stream with the exception of the first column following ||T||.

When clock compensation is done in the unencoded data stream, rules for idle insertion and deletion shall be as follows:

a) Idle insertion or deletion occurs in groups of four Idle characters.
b) Idle characters are added following idle or ordered_sets.
c) Idle characters are not added while data is being received.
d) When deleting idles, the minimum IPG of five characters is maintained.

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e) Sequence ordered_sets are deleted to adapt between clock rates.

f) Sequence ordered_set deletion occurs only when two consecutive sequence ordered_sets have been received and deletes only one of the two.

g) Only idles are inserted for clock compensation.

The disparity of the /R/ code-group is neutral, allowing its removal or insertion without affecting the current running disparity of the serial stream. The correct current running disparity version of /R/ must be inserted in each lane during Skip insertion (see Table 36-2). The Skip ordered_set is defined in Table 48–4.

48.2.4.3 Encapsulation

The Start and Terminate ordered_sets correspond to columns containing the XGMII Start and Terminate control characters, respectively.

48.2.4.3.1 Start ||S||

The Start or ||S|| ordered_set directly maps to the XGMII Start control character in lane 0 followed by any three data characters in XGMII lanes 1 through 3. Normally, the three data characters will be the preamble pattern, but the PCS neither checks nor alters their contents. ||S|| indicates to the PCS that a packet has been initiated. The Start ordered_set is defined in Table 48–4.

48.2.4.3.2 Terminate ||T||

The Terminate or ||T|| ordered_set directly maps to the XGMII Terminate control character located in any lane, preceded by data characters if Terminate is not in lane 0, and followed by Idle characters if Terminate is not in lane 3. ||T|| indicates to the PCS that a packet has been terminated. All XGMII control characters following ||T|| are translated by the PCS until the recognition of the next XGMII Start control character. The PCS considers the MAC interpacket gap (IPG) to have begun with the reception of ||T||. The Terminate ordered_set is defined in Table 48–4.

Unrecognized running disparity errors which propagate to any Idle code-groups in ||T|| or to the column following ||T|| are indicated as /E/ in the preceding column in the same lane in which the errors were recognized. All ||I|| ordered_sets are selected to ensure that propagated code violations are recognized and not propagated further.

The cvtx_terminate function is used to convert all XGMII Idle control characters in the same column as the XGMII Terminate control character to /K/ code-groups. The cvrx_terminate function is used to convert all /K/ code-groups in ||T|| to XGMII Idle control characters.

48.2.4.4 Error /E/

The Error code-group is directly mapped to the XGMII Error control character. /E/ may also be generated by the PCS client to indicate a transmission error to its peer entity or deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability. Error is signaled per lane since code-violations are detected on a per lane basis. The Error code-group is defined in Table 48–4.

The presence of /E/ or any invalid code-group on the medium denotes an error condition. 10GBASE-X elements that detect code-group violations shall replace the invalid code-group with /E/ prior to retransmission.

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48.2.4.5 Link status

Link status reporting uses the Sequence ordered-set to transport the transmit fault and receive fault link status conditions.

48.2.4.5.1 Sequence ||Q||

The Sequence or ||Q|| ordered_set directly maps to the XGMII Sequence control character on lane 0 followed by three data characters in XGMII lanes 1 through 3. ||Q|| indicates to the PCS that a link status message has been initiated. The PCS Receive process may also initiate Sequence ordered-sets upon detection of a link status condition. Sequence ordered-sets are always sent over the PMA service interface in the column that follows an ||A|| ordered-set. The Sequence ordered-sets do not otherwise interfere with the randomized ||I|| sequence. Sequence ordered-sets corresponding to Local Fault signal and Remote Fault signal are specified in Table 48–4.

48.2.5 Management function requirements

The 10GBASE-X PCS supports a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the 10GBASE-X sublayer is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.4 and 45.2.5. The details of the register bit allocations and general usage are given in Clause 45. Table 48–6, Table 48–8, and Table 48–8 describe how the PCS state diagram variables map to management register bits. If an MDIO interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

Table 48–6—State diagram variable to management register mapping for PCS

State diagram variable	Management Register Bit
reset	3.0.15 Reset
sync_status	3.24.12 10GBASE-X lane alignment status
lane_sync_status<3>	3.24.3 Lane 3 sync
lane_sync_status<2>	3.24.2 Lane 2 sync
lane_sync_status<1>	3.24.1 Lane 1 sync
lane_sync_status<0>	3.24.0 Lane 0 sync

Table 48–7—State diagram variable to management register mapping for PHY XS

State diagram variable	Management Register Bit
reset	4.0.15 Reset
align_status	4.8.10 Receive local fault
sync_status	4.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	4.24.3 Lane 3 sync
lane_sync_status<2>	4.24.2 Lane 2 sync
lane_sync_status<1>	4.24.1 Lane 1 sync
lane_sync_status<0>	4.24.0 Lane 0 sync

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Table 48–8—State diagram variable to management register mapping for DTE XS

State diagram variable	Management Register Bit
reset	5.0.15 Reset
align_status	5.8.10 Receive local fault
sync_status	5.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	5.24.3 Lane 3 sync
lane_sync_status<2>	5.24.2 Lane 2 sync
lane_sync_status<1>	5.24.1 Lane 1 sync
lane_sync_status<0>	5.24.0 Lane 0 sync

48.2.6 Detailed functions and state diagrams

The body of this clause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Timeless states are employed as an editorial convenience to facilitate the distribution of transition conditions from prior states. No actions are taken within these states. Exit conditions are evaluated for timeless states. There is one timeless state. It is PCS Receive state RECEIVE.

48.2.6.1 State variables

48.2.6.1.1 Notation conventions

/x/
: Denotes the constant code-group specified in 48.2.6.1.2 (valid code-groups must follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[/x/]
: Denotes the latched received value of the constant code-group (/x/) specified in 48.2.6.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 48.2.6.1.6.

||y||
: Denotes the column of constant code-groups in lanes 0 through 3, inclusively, specified in 48.2.6.1.2 (valid code-groups must follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

[||y||]
: Denotes the latched received value of the column of constant code-groups in lanes 0 through 3, inclusively (||y||), specified in 48.2.6.1.2 and conveyed by the SYNC_UNITDATA.indicate message described in 48.2.6.1.6 or the ALIGN_UNITDATA.indicate message described in 48.2.6.1.6.

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48.2.6.1.2 Constants

/A/
: The /K28.3/ code-group used in the Idle Align function specified in 48.2.4.2.2.

||A||
: The column of four identical Idle Align code-groups corresponding to the Idle Align function specified in 48.2.4.2.2.

/COMMA/
: The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36-2.

/D/
: The set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36-1.

||D||
: The column of four Data code-groups present during packet reception.

/Dx.y/
: One of the set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36-1.

/E/
: The /K30.7/ code-group corresponding to the Error function specified in 48.2.4.4.

||I||
: The column of four identical Idle code-groups corresponding to the Idle function specified in 48.2.4.2. Also used to represent the corresponding XGMII control characters.

||IDLE||
: Alias for ||I||.

/INVALID/
: The set of invalid data or special code-groups, as specified in 36.2.4.6.

/K/
: The /K28.5/ code-group used in the Idle Sync function specified in 48.2.4.2.1. Also used in the Terminate function specified in 48.2.4.3.2.

||K||
: The column of four identical Idle Sync code-groups corresponding to the Idle Sync function specified in 48.2.4.2.1.

/Kx.y/
: One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36-2.

LFAULT
: A vector of bits RXD<31:0> and RXC<3:0> containing a Local Fault sequence ordered_set. The Local Fault sequence ordered_set is defined in 46.3.4.

||Q||
: The column of four code-groups corresponding to the Sequence function specified in 48.2.4.5.1. Also used to represent the corresponding set of XGMII control and data characters.

/R/
: The /K28.0/ code-group used for the Idle Skip function specified in 48.2.4.2.3.

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||R||

The column of four identical Idle Skip code-groups corresponding to the Idle Skip function specified in 48.2.4.2.3.

||S||

The column of code-groups including the Start code-group as specified in 48.2.4.3.1. Also used to represent the corresponding set of XGMII control and data characters.

||T||

The column of code-groups including the Terminate code-group as specified in 48.2.4.3.2. Also used to represent the corresponding XGMII control and data characters.

48.2.6.1.3 Variables

align_column <39:0>

A vector of bits represented by the most recently received column of aligned 10-bit code-groups on all four lanes from the PCS Deskew process. For lane 0, the element align_column <0> corresponds to the least recently received (oldest) rx_bit of the code-group; align_column <9> corresponds to the most recently received (newest) rx_bit of the code-group. The same bit aging is applicable to the bits in align_column <39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

align_status

A parameter set by the PCS Deskew process to reflect the status of the lane-to-lane code-group alignment.

Values: FAIL; The deskew process is not complete.
OK; All lanes are synchronized and aligned.

code_sel

A boolean derived from a uniformly distributed random integer r generated by a PRBS based on a 7th order polynomial.

Values: 0; LSB of random number is zero.
1; LSB of random number is one.

deskew_error

A boolean used by the PCS Deskew process to indicate that a lane-to-lane alignment error has been detected.

Values: FALSE; /A/ not recognized in any lane or recognized in all lanes simultaneously.
TRUE; /A/ recognized in fewer than all lanes.

enable_cgalign

A boolean that indicates the enabling and disabling of code-group comma alignment. The code-group boundary may be changed whenever code-group comma alignment is enabled. This process is known as code-group alignment.

Values: FALSE; Code-group alignment is disabled.
TRUE; Code-group alignment is enabled.

enable_deskew

A boolean that indicates the enabling and disabling of the deskew process. Code-groups may be discarded whenever deskew is enabled. This process is known as code-group slipping.

Values: FALSE; Deskew is disabled.
TRUE; Deskew is enabled.

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IDLE

A vector of bits RXD<31:0> and RXC<3:0> containing Idle. Idle is defined in Table 46-4.

lane_sync_status <3:0>

A parameter set by the PCS Synchronization process to reflect the status of the link for each lane as viewed by the receiver. lane_sync_status <n> represents lane_sync_status on lane n where n=0:3.

Values: FAIL; The receiver is not synchronized to the code-group boundary.
OK; The receiver is synchronized to the code-group boundary.

next_ifg

Controls the ||IDLE|| pattern immediately following the next frame. It is used to ensure an equal and deterministic presence of both ||A|| and ||K||

Values: A; The first ||IDLE|| following the end of the next frame will be ||A||.
K; The first ||IDLE|| following the end of the next frame will be ||K||.

reset

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low-power mode set via Control register bit 4.0.11 or 5.0.11. The condition is also true when a reset request is detected via Control register bit 4.0.15 or 5.0.15.

Values: FALSE; The device is completely powered and has not been reset (default).
TRUE; The device has not been completely powered or has been reset.

NOTE—Reset evaluates to its default value in each state where it is not explicitly set.

RX

Alias for RXD <31:0> and RXC <3:0> representing the XGMII Receive Data and Control signals.

RXC <3:0>

Receive Control signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

RXD <31:0>

Receive Data signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

rx_lane <3:0>

A vector of bits representing the serial lanes used to convey data from the PMD to the PMA via the PMD_UNITDATA.indicate service primitive as specified in Clause 53.

Bit values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

rx_unaligned <39:0>

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PMA. For lane 0, the element rx_unaligned <0> is the least recently received (oldest) rx_bit from the PMD; rx_unaligned <9> is the most recently received (newest) rx_bit from the PMD. The same bit aging is applicable to the bits in rx_unaligned <39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

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signal_detect <3:0>

A parameter set continuously and directly from the PMD_SIGNAL.indicate(signal_detect <3:0>) primitive to reflect the status of the incoming link signal for each lane. Used by the PCS Synchronization process to validate the data received on rx_unaligned <39:0>. Signal_detect <n> represents signal_detect on lane n where n=0:3.

Values: FAIL; A signal is not present on the lane.
OK; A signal is present on the lane.

sync_code-group <39:0>

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PCS Synchronization process. For lane 0, the element sync_code-group <0> corresponds to the least recently received (oldest) rx_bit; sync_code-group <9> corresponds to the most recently received (newest) rx_bit. The same bit aging is applicable to the bits in sync_code-group<39:10> with respect to rx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

sync_status

A boolean that represents the following behavior: For all n in lane_sync_status<n>.

Values: FAIL; At least one lane is not in sync.
OK; All lanes are in sync.

TQMSG

A vector of bits representing the last link status message received over the XGMII once the link status message is recognized. Used by the PCS Transmit process to load tx_code-group <39:0>.

tx_code-group <39:0>

A vector of bits representing a column of four aligned 10-bit code-groups which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMA_UNITDATA.request(tx_lane <3:0>) service primitive. For lane 0, the element tx_code-group <0> is the first tx_bit transmitted; tx_code-group <9> is the last tx_bit transmitted. The same bit aging is applicable to the bits in tx_code-group <39:10> with respect to tx_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

TX

Alias for either TXD <31:0> and TXC <3:0> representing the XGMII Transmit Data and Control signals, or the Local Fault ordered_set as defined in 46.3.4 when a fault condition is detected on the transmit path.

TXC <3:0>

Transmit Control signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

TXD <31:0>

Transmit Data signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

tx_lane <3:0>

A vector of bits representing the serial lanes used to convey data from the PMA to the PMD via the PMD_UNITDATA.request service primitive as specified in Clause 53.

Bit values: ZERO; Data bit is a logical zero.
ONE; Data bit is a logical one.

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48.2.6.1.4 Functions

check_end

Prescient Terminate function used by the PCS Receive process to set the RXD<31:0> and RXC<3:0> signals to indicate Error if a running disparity error was propagated to any Idle code-groups in ||T||, or to the column following ||T||. The XGMII Error control character is returned in all lanes less than n in ||T||, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code-groups other than /A/ or /K/ are recognized in the column following ||T||. The XGMII Error control character is also returned in all lanes greater than n in the column prior to ||T||, where n identifies the specific Terminate ordered-set $||T_n||$, for which a running disparity error or any code group other than /K/ is recognized in the corresponding lane of ||T||. For all other lanes the value set previously is retained.

cvrx_terminate

Conversion function used by the PCS Receive process when Terminate is indicated to convert all /K/ code-groups to Idle control characters signaled via RX. Conversion is performed for all lanes.

cvtx_terminate

Conversion function used by the PCS Transmit process when Terminate is indicated to convert all Idle control characters signaled via TX to /K/ code-groups. Conversion is performed for all lanes.

DECODE ([||y||])

Consists of four independent synchronous processes, one each per lane. In the PCS Receive process, this function takes as its arguments the latched value of align_column ([||y||]) and the current running disparity, and returns XGMII RX as specified in 48.2.3 and 48.2.4. When decoding ||T||, the returned XGMII RX value is further modified by the cvrx_terminate and check_end functions, the result of the check_end function takes priority over the result of the cvrx_terminate function. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

ENCODE(TX)

Consists of four independent synchronous processes, one each per lane. In the PCS Transmit process, this function takes as its argument the XGMII TX signals and the current running disparity for each lane, and returns four corresponding 10-bit code-groups as specified in 48.2.3 and 48.2.4. When encoding ||T||, the XGMII TX values are modified by the result of the cvtx_terminate function. ENCODE also updates the current running disparity per Tables 36-1 or 36-2.

Q_det

Function to determine the need to transmit sequence ordered_sets. If TX=||Q|| then Q_det is set to true and TQMSG is set to the result of ENCODE(TX). Q_det remains true until set to false by the PCS transmit source state diagram. In the event that this function and the state diagram both attempt to modify Q_det, the setting of Q_det by this function to true will take priority.

signal_detectCHANGE <3:0>

In the PCS Synchronization process, this function monitors the signal_detect parameter on a per lane basis for a state change. The function is set upon state change detection, which is required to detect signal_detect changes which occur asynchronously to PUDI. signal_detectCHANGE <n> represents signal_detectCHANGE on lane n where n=0:3.

Values: TRUE; The output of this function changes to true when the function detects a change in signal_detect and stays true until the false condition is satisfied.
FALSE; The output of this function changes to false when the LOSS_OF_SYNC state of the PCS synchronization state diagram is entered.

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48.2.6.1.5 Counters

A_CNT
: A 5-bit down counter used to control Align code-group spacing. Loaded with a value between 16 and 31, inclusive, by a uniformly distributed random integer r generated by a PRBS based on a 7th order polynomial as described in 48.2.4.2. A_CNT is decremented once per PUDR. The count remains at zero until ||A|| is transmitted, at which time a new value is loaded.

good_cgs
: A 2-bit consecutive valid code-groups received counter.

48.2.6.1.6 Messages

AUDI([||y||])
: Alias for ALIGN_UNITDATA.indicate(parameters).

ALIGN_UNITDATA.indicate([align_column <39:0>])
: A signal sent by the PCS Deskew process to the PCS Receive process conveying the latched value of the indicated column of code-groups over each lane ([||y||]) (see 48.2.6.2.3).

PMA_UNITDATA.indicate(rx_unaligned <39:0>)
: A signal sent by the PMA Receive process to the PCS Synchronization process conveying the next code-group set received over each lane of the medium (see 48.3.2.2).

PMA_UNITDATA.request(tx_code-group <39:0>)
: A signal sent by the PCS Transmit process conveying the next code-group set for all lanes ready for transmission over the medium (see 48.3.2.1).

PMD_SIGNAL.indicate(signal_detect <3:0>)
: Indicates the status of the incoming link signal. A signal mapped to the PMD_SIGNAL.indicate(SIGNAL_DETECT) service primitive specified in Clause 53. signal_detect <n> is set to the same value for all lanes n where n=0:3.

  Values: FAIL; A signal is not present on the lane.
  OK; A signal is present on the lane.

PUDI
: Alias for PMA_UNITDATA.indicate(parameters).

PUDR
: Alias for PMA_UNITDATA.request(parameters).

SUDI
: Alias for SYNC_UNITDATA.indicate(parameters).

SYNC_UNITDATA.indicate(sync_code-group <39:0>)
: A signal sent by the PCS Synchronization process to the PCS Deskew process conveying code-groups over each lane (see 48.2.6.2.2).

48.2.6.2 State diagrams

48.2.6.2.1 Transmit

The PCS shall implement its Transmit process as depicted in Figure 48–6, including compliance with the associated state variables as specified in 48.2.6.1. This state machine makes exactly one transition for each transmitted ordered_set that is processed.

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The Transmit Source process determines whether XGMII data and control information should be passed through to the PMA for serialization or converted before passing to the PMA. In all cases, XGMII data and control information is encoded before it is passed to the PMA. Data and control information may be sourced either directly from the XGMII or generated by the PCS depending on whether packet or Idle is being sourced by the XGMII. The recognition of the XGMII Start, Terminate, Idle and Sequence control characters is used to determine whether packet, Idle, or link status is being sourced by the XGMII.

The detection of a link status condition including the receipt of link status messages over the XGMII causes the PCS Transmit process to generate link status messages interspersed in an Idle sequence.

The PCS Transmit process continuously sources tx_code-group<39:0> to the PMA. The Transmit process determines the proper code-group to source on each lane based on running disparity requirements.

48.2.6.2.2 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–7 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indicate primitive and conveys received code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message.

When in the LOSS_OF_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states. The Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane_sync_status <3:0>, the align_status flag is set to FAIL.

48.2.6.2.3 Deskew

The PCS shall implement the Deskew process as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the align_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the align_status flag is de-asserted. The Deskew process is otherwise idle. Whenever the align_status flag is set to FAIL the condition is indicated as a link_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

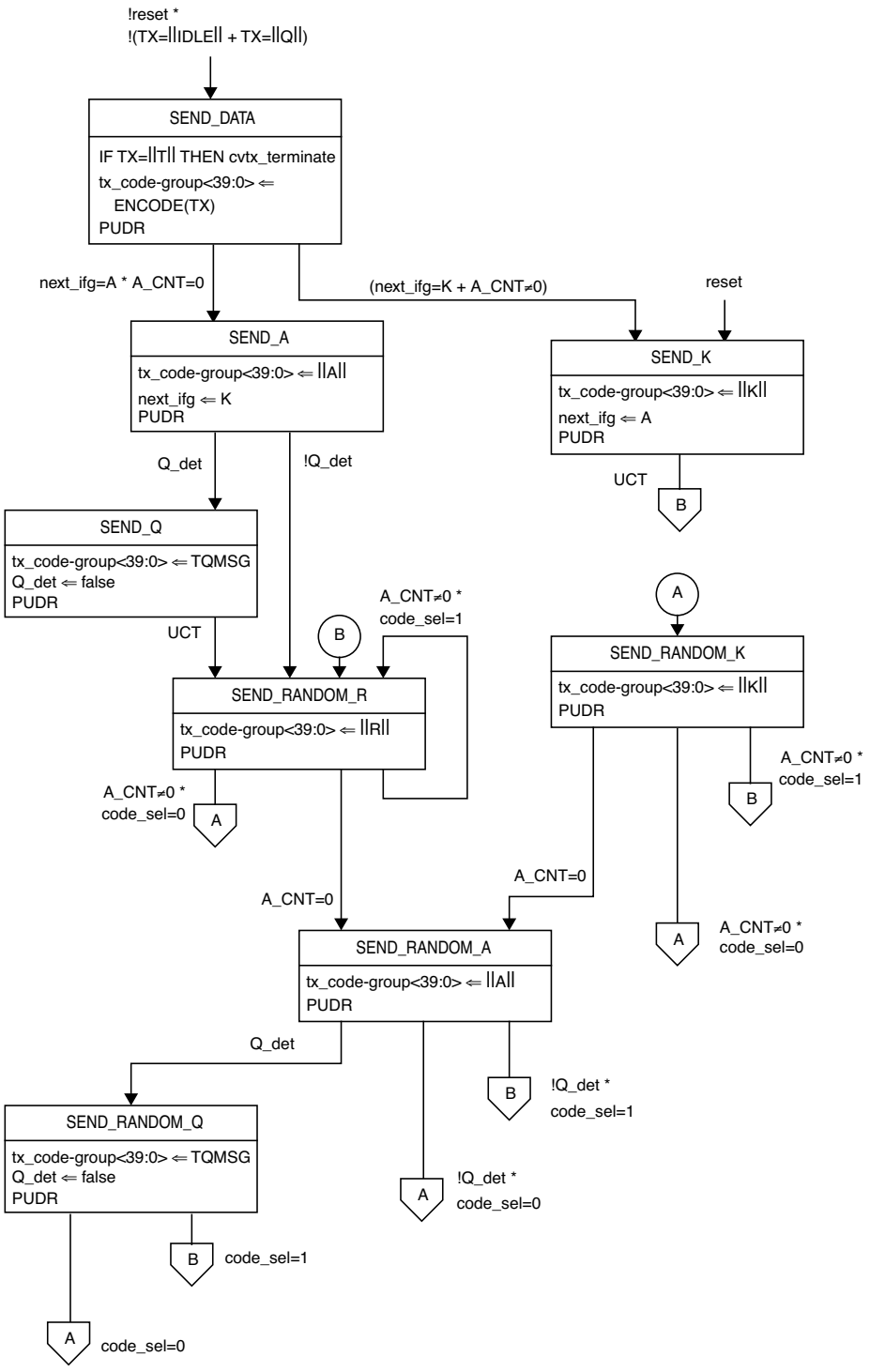
Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN_ACQUIRED_1 and LOSS_OF_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.

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NOTE—The state machine makes exactly one transition for each transmit code-group processed.

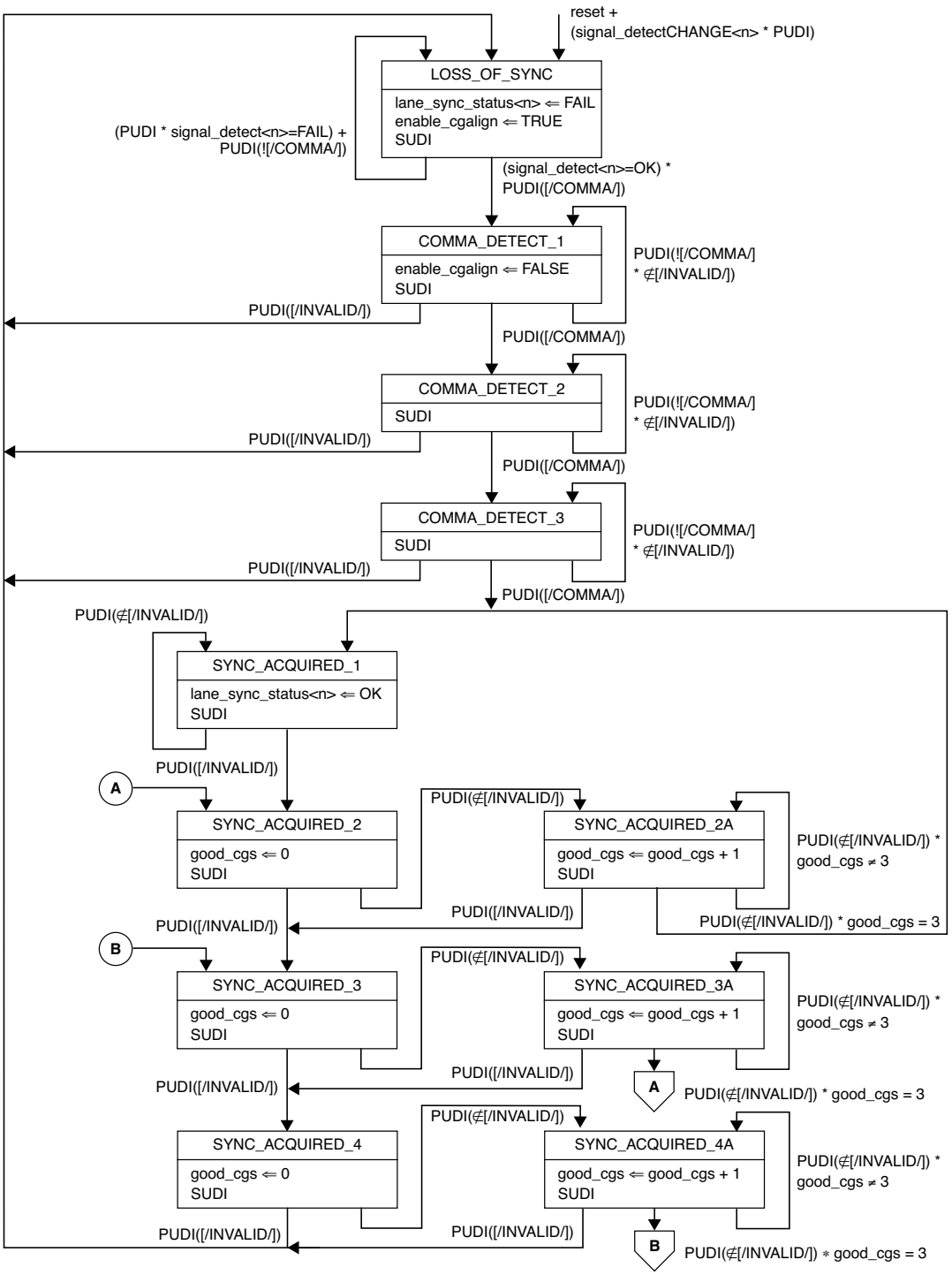
Figure 48–6—PCS transmit source state diagram

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NOTE— lane_sync_status<n>, signal_detect<n> and signal_detectCHANGE<n>, refer to the number of the received lane n where n=0:3

Figure 48–7—PCS synchronization state diagram

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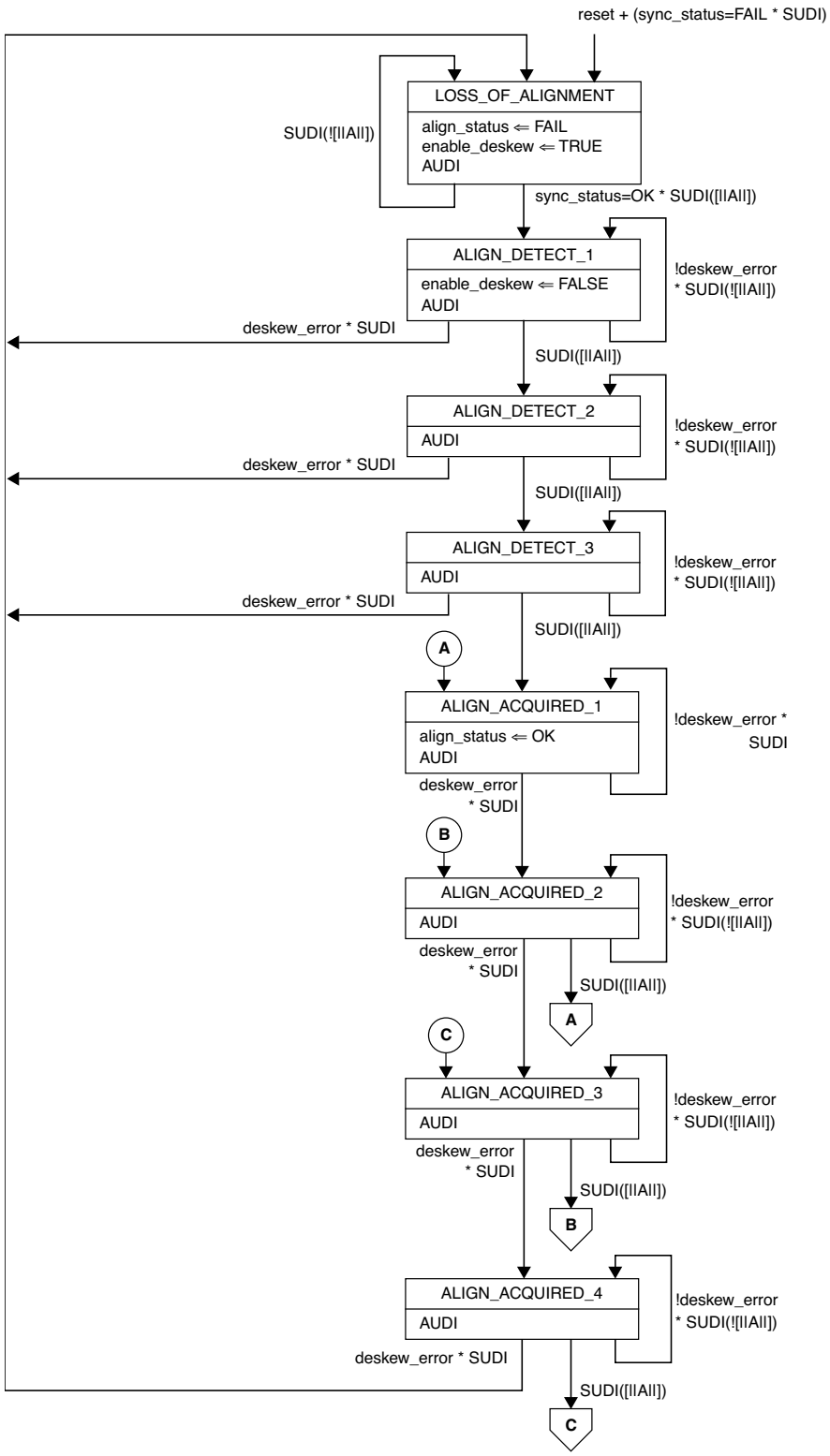


Figure 48–8—PCS deskew state diagram

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48.2.6.2.4 Receive

The PCS shall implement its Receive process as depicted in Figure 48–9, including compliance with the associated state variables as specified in 48.2.6.1.

The PCS Receive process continuously performs the DECODE function on the received code-groups from the PCS Deskew Process via the ALIGNED_UNITDATA.indicate message. The PCS Receive process generates the receive clock signal of the XGMII (RX_CLK) as specified in Clause 46. State transitions in the PCS Receive state diagram that generate the data and control characters (RXD<31:0> and RXC<3:0>) on the XGMII occur synchronous to RX_CLK. The Receive process operates in the following two modes:

a) Data mode during packet reception including Start and Terminate. Additionally, Data mode is active whenever !||I|| columns are received during the Idle sequence or !||I|| or !||Q|| columns are received during the Fault sequence signifying either an error or unusual or unsupported indication. Valid code-groups received while in Data mode are mapped to corresponding XGMII data or control characters regardless of whether or not the control characters are valid XGMII control characters. Invalid or Error code-groups are mapped directly to XGMII Error control characters. All code-groups are mapped on a lane by lane basis.

b) Idle mode during idle reception excluding Start and Terminate. Idle mode is active whenever ||I|| is received during idle reception. ||I|| is translated to XGMII Idle control characters.

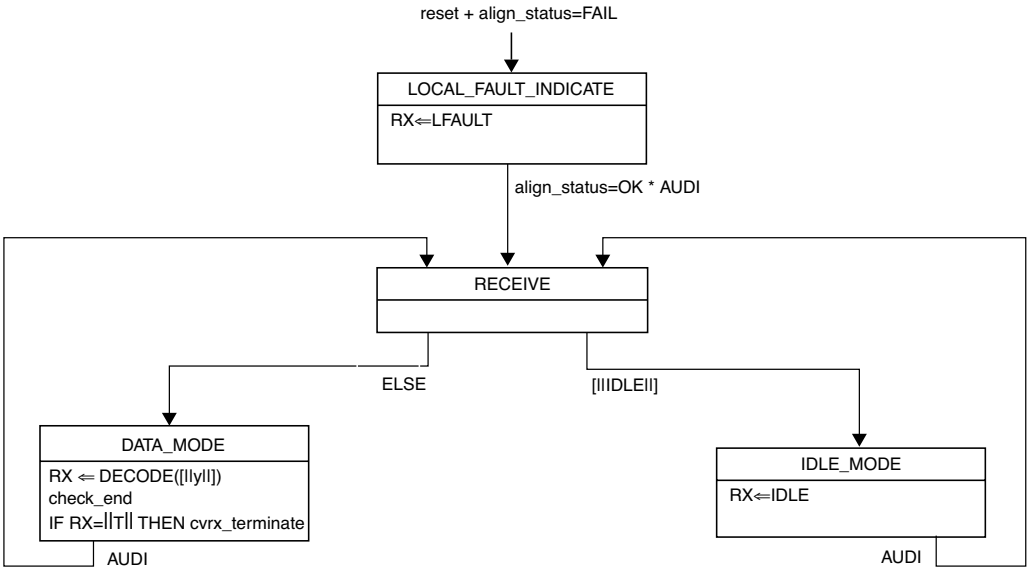


Figure 48–9—PCS receive state diagram

48.2.6.3 Initialization process

Link initialization involves the completion of the PCS Synchronization and Deskew processes and the ability to transmit and receive code-groups via the PCS Transmit and Receive processes, respectively. The status register link_status flag is set to OK whenever the align_status flag is set to OK and no errors preventing link operation are present in the PCS or PMA.

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48.2.6.4 Link status reporting

Link status reporting involves detection of link status conditions and the signaling of link fault status. The purpose of link status reporting is to quickly identify and convey link status conditions to the RS which can take the necessary action to activate (deactivate) the link via the setting of the RS link_fault 2-bit variable. Link status reporting and MAC packet transmission is mutually exclusive.

48.2.6.4.1 Link status detection

10GBASE-X link status conditions include signal and deskew status conditions. Link status conditions include Local Fault and Remote Fault signals. A receive fault is recognized by the PCS Receive process whenever align_status=FAIL. Other fault conditions are not detected by the PCS or PMA and are detected only by the RS. A fault condition may also be recognized by any 10GBASE-X process upon detection of an error condition, which prevents continued reliable operation, but this is beyond the scope of this standard.

48.2.6.4.2 Link status signaling

Link status signaling follows the detection or recognition of a link status condition and involves the generation of Sequence ordered-sets (||Q||) by the PCS Transmit process. Link status signaling involves the transmission of ||Q|| following ||A|| transmission in the Idle sequence as specified in 48.2.4.2.

48.2.6.4.3 Link status messages

A 10GBASE-X link status message is a Sequence ordered-set. Ordered-sets associated with link status messages are specified in Table 48–4. Link status messages detected by the PCS Receive process are forwarded to the XGMII.

48.3 Physical Medium Attachment (PMA) sublayer

The PMA is specified in the form of a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of code-group information between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa.

48.3.1 Functions within the PMA

The PMA comprises the PMA Transmit process and PMA Receive process. Figure 48–4 depicts the mapping of the 36-bit-wide data and control path of the XGMII to the forty-bit-wide code-groups of the PMA service interface, and on to the four lane serial PMD service interface.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clause 47 and Clause 53. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

48.3.1.1 PMA transmit process

The PMA Transmit process passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of the PMA_UNITDATA.request primitive, the PMA shall individually serialize the four aligned 10-bit code-groups, one from each of four lanes, and transmit them to the PMD in the form of forty PMD_UNITDATA.request primitives, 10 each on four lanes.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA_UNITDATA.indicate parameter corresponds to the first bit transmitted to the PMD and the highest numbered bit of the

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PMA_UNITDATA.indicate parameter corresponds to the last bit transmitted to the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–4.

PMA_UNITDATA.request primitives shall be generated with a frequency of 312.5 MHz ± 100 ppm. An internal clock multiplier unit multiplies the frequency of the 10-bit code-group based PMA_UNITDATA.request primitives by a factor of 10 to serialize the latched data out of the PMA and into the PMD.

48.3.1.2 PMA receive process

The PMA Receive process passes data unaltered (except for deserializing) from the PMD directly to the PCS. Upon receipt of forty PMD_UNITDATA.indicate primitives, 10 in succession from each of four lanes, the PMA shall assemble the bits received into a 40-bit vector representing four 10-bit unaligned code-groups and pass that vector to the PCS as the parameter of four PMA_UNITDATA.indicate primitives.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA_UNITDATA.indicate parameter corresponds to the first bit received from the PMD and the highest numbered bit of the PMA_UNITDATA.indicate parameter corresponds to the last bit received from the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. Receive code-group alignment is performed by the PCS and is not applicable to PMA. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–4.

PMA_UNITDATA.indicate primitives shall be generated with a frequency of 312.5 MHz ± 100 ppm. The line rate of each of four PMD lanes is 3.125 GBaud ± 100 ppm. The serial data stream of the PMD includes an embedded clock that nominally operates at a frequency 10 times higher than that of a single lane code-group stream. The PMA Receive process shall recover a clock from a valid 8B/10B received data stream if the stream is within tolerance.

48.3.2 Service interface

The following primitives are defined:

PMA_UNITDATA.request(tx_code-group <39:0>)

PMA_UNITDATA.indicate(rx_unaligned <39:0>)

48.3.2.1 PMA_UNITDATA.request

This primitive defines the transfer of data in the form of aligned code-groups from the PCS to the PMA. PMA_UNITDATA.request is generated by the PCS Transmit process.

48.3.2.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_code-group <39:0>)

The data conveyed by PMA_UNITDATA.request is the tx_code-group <39:0> parameter defined in 48.2.6.1.3.

48.3.2.1.2 When generated

The PCS continuously sends tx_code-group <39:0> to the PMA at a nominal rate of 312.5 MHz ± 100 ppm, as governed by frequency and tolerance of XGMII TX_CLK.

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48.3.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of forty PMD_UNITDATA.request primitives, 10 for each of the four PMD lanes, tx_lane <3:0>, requesting the four lane serial transmission of tx_code-group <39:0> to the PMD.

48.3.2.2 PMA_UNITDATA.indicate

This primitive defines the transfer of data in the form of code-groups from the PMA to the PCS. PMA_UNITDATA.indicate is used by the PCS Synchronization process.

48.3.2.2.1 Semantics of the service primitive

PMA_UNITDATA.indicate(rx_unaligned <39:0>)

The data conveyed by PMA_UNITDATA.indicate is the rx_unaligned <39:0> parameter defined in 48.2.6.1.3.

48.3.2.2.2 When generated

The PMA continuously sends rx_unaligned <39:0> to the PCS at a nominal rate of 312.5 MHz ± 100 ppm, as governed by frequency and tolerance of PMD_UNITDATA.indicate.

48.3.2.2.3 Effect of receipt

Upon receipt of this primitive, the PCS Sychronization process attempts to achieve code-group synchronization on each lane (see 48.2.6.2.2).

48.3.3 Loopback mode

Loopback mode shall be provided for the 10GBASE-X PMA and DTE XGXS, and optionally for the PHY XGXS, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). Loopback applies to all lanes as a group (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing Loopback mode is not defined by this standard.

Control of the Loopback function may be supported through the MDIO management interface of Clause 45 or equivalent.

NOTE—The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

48.3.3.1 Receiver considerations

Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

48.3.3.2 Transmitter considerations

While in Loopback mode, the transmitter output is not defined.

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48.3.4 Test functions

A limited set of test functions may be provided as an implementation option for testing of the transmitter function or for testing of an attached receiver.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. Random jitter test patterns for 10GBASE-X are specified in Annex 48A. Test-pattern capability and selection is optional and supported via MDIO register bits defined in Clause 45. Jitter Test methodology for 10GBASE-X is specified in Annex 48B.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See ANSI X3.230-1994, FC-PH subclause 5.4 for a more detailed discussion of receiver and transmitter behavior under various test conditions.

48.4 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of an XGMII shall comply with the requirements as specified in Clause 46.

48.5 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 10GBASE-X PCS shall be no more than 2048 BT.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference bit, as measured at the MDI.

48.6 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

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48.7 Protocol Implementation Conformance Statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[8]

48.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

48.7.2 Identification

48.7.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

48.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 48, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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48.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
MD	MDIO	45, 48.1.3.1	Registers and interface supported	O	Yes [ ] No [ ]
XGXS	Support of XAUI/XGXS	47, 48.1.5		O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 48.1.3.1	Compatibility interface is supported	O	Yes [ ] No [ ]
LX4	Support of 10GBASE-LX4 PMD	53, 48.1.3.3		O	Yes [ ] No [ ]

48.7.4 PICS proforma tables for the PCS and PMA sublayer, type 10GBASE-X

48.7.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Jitter test patterns	48.3.4	As per Annex 48A	M	Yes [ ]
CC2	Environmental specifications	48.6		M	Yes [ ]

48.7.4.2 PCS functions

Item	Feature	Subclause	Value/Comment	Status	Support
CG	Code-group usage	48.2.3	PCS support of 8B/10B code-groups	M	Yes [ ]
IOS	||I|| sequencing rules	48.2.4.2	All rules apply	M	Yes [ ]
PRBS	Random integer generator	48.2.4.2	$X^7 + X^3 + 1$ or $X^7 + X^6 + 1$. Used for ||A|| spacing. Optional and ancillary use for testing	M	Yes [ ]
CMA	Comma detection	48.2.4.2.1	comma+ and comma- for /K/	M	Yes [ ]
CKCU	Clock rate compensation in unencoded idle stream	48.2.4.2.3	Meets the requirements of 48.2.4.2.3	O	Yes [ ] No [ ]
ERR	Error indication	48.2.4.4	Replacement of invalid code-groups with /E/	M	Yes [ ]
TSD	Transmit state diagrams	48.2.6.2.1	Meets the requirements of Figures 48–6	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
SSD	Synchronization state diagram	48.2.6.2.2	Meets the requirements of Figure 48–7	M	Yes [ ]
DSD	Deskew state diagrams	48.2.6.2.3	Meets the requirements of Figure 48–8	M	Yes [ ]
RSD	Receive state diagrams	48.2.6.2.4	Meets the requirements of Figure 48–9	M	Yes [ ]

48.7.4.3 PMA Functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT	Transmit function	48.3.1.1	PMA_UNITDATA.request	M	Yes [ ]
TXRT	Transmit rate	48.3.1.1	3.125 GBaud ± 100 ppm	M	Yes [ ]
PMAR	Receive function	48.3.1.2	PMA_UNITDATA.indicate	M	Yes [ ]
RXRT	Receive rate	48.3.1.2	3.125 GBaud ± 100 ppm	M	Yes [ ]
CDR	Clock and data recovery	48.3.1.2	Required if line rate is within 3.125 GBaud ± 100 ppm	M	Yes [ ]

48.7.4.4 Interface functions

Item	Feature	Subclause	Value/Comment	Status	Support
SKEW	Allowable lane skew	48.2.4.2.2	Table 48–5	M	Yes [ ]
LBXPMA	10GBASE-X PMA Loopback mode	48.3.3		M	Yes [ ]
LBDTE	DTE XGXS Loopback mode	48.3.3		M	Yes [ ]
LBPHY	PHY XGXS Loopback mode	48.3.3		O	Yes [ ]
DLY	Delay constraints	48.5	2048 BT	M	Yes [ ]

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49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R

49.1 Overview

49.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) that is common to a family of 10 Gb/s Physical Layer implementations, known as 10GBASE-R. This PCS can connect directly to one of the 10GBASE-R Physical Layers: 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER. Alternatively, this PCS can connect to a Wan Interface Sublayer (WIS), which will produce the 10GBASE-W encoding (10GBASE-R encoded data stream encapsulated into frames compatible with SONET and SDH networks) for transport by the 10GBASE-W Physical Layers: 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW. The term 10GBASE-R is used when referring generally to physical layers using the PCS defined here.

The 10GBASE-R is based on a 64B/66B code. The 64B/66B code supports data and control characters, while maintaining robust error detection.

10GBASE-R PCS maps the interface characteristics of the WIS when present, and the PMA sublayer to the services expected by the Reconciliation and XGXS sublayers. 10GBASE-R can be extended to support any full duplex medium requiring only that the medium be compliant at the PMA level. 10GBASE-R PCS may be attached through the PMA sublayer to a LAN PMD sublayer supporting a data rate of 10 Gb/s or it may be attached to a WAN PMD through the WIS and PMA sublayers. When attached to a WAN sublayer, this PCS adapts the data stream to the WAN data rate.

49.1.2 Objectives

The following are the objectives of 10GBASE-R:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using optical fiber compliant with ISO/IEC 11801: 1995 as specified in Clause 52.
e) Allow for a nominal network extent of up to 40 km.
f) Support a BER objective of 10^{-12}.

49.1.3 Relationship of 10GBASE-R to other standards

Figure 49–1 depicts the relationships among the 10GBASE-R sublayers (shown shaded), the Ethernet MAC and reconciliation layers, and the higher layers.

49.1.4 Summary of 10GBASE-R and 10GBASE-W sublayers

The following subclauses provide an overview of the 10GBASE-R and 10GBASE-W sublayers.[9] Figure 49–1 depicts the relationship between the 10GBASE-R PCS and its associated sublayers.

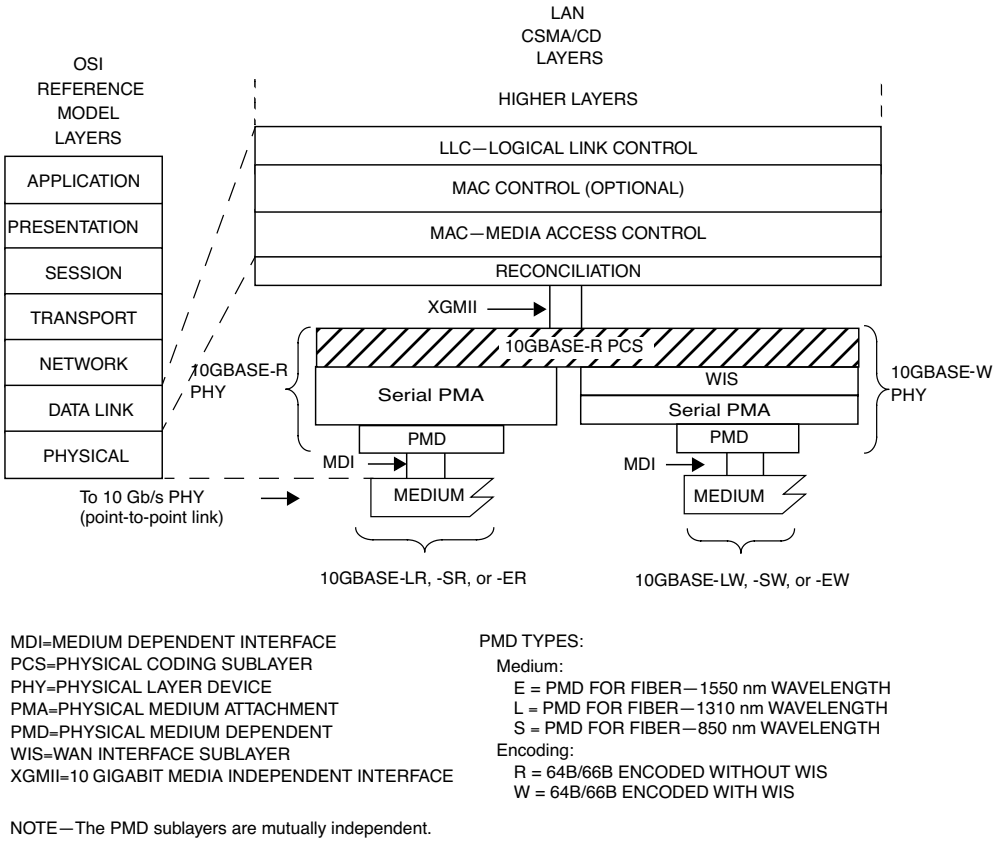
[9] The 10GBASE-R PHY consists of that portion of the Physical Layer between the MDI and XGMII consisting of the PCS, PMA, and PMD sublayers. The 10GBASE-R PHY is roughly analogous to the 100BASE-X PHY.

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MDI=MEDIUM DEPENDENT INTERFACE
PCS=PHYSICAL CODING SUBLAYER
PHY=PHYSICAL LAYER DEVICE
PMA=PHYSICAL MEDIUM ATTACHMENT
PMD=PHYSICAL MEDIUM DEPENDENT
WIS=WAN INTERFACE SUBLAYER
XGMII=10 GIGABIT MEDIA INDEPENDENT INTERFACE

PMD TYPES:
Medium:
E = PMD FOR FIBER—1550 nm WAVELENGTH
L = PMD FOR FIBER—1310 nm WAVELENGTH
S = PMD FOR FIBER—850 nm WAVELENGTH
Encoding:
R = 64B/66B ENCODED WITHOUT WIS
W = 64B/66B ENCODED WITH WIS

NOTE—The PMD sublayers are mutually independent.

Figure 49–1—10GBASE-R PCS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and IEEE 802.3 CSMA/CD LAN model

49.1.4.1 Physical Coding Sublayer (PCS)

The PCS service interface is the 10 Gigabit Media Independent Interface (XGMII), which is defined in Clause 46. The XGMII provides a uniform interface to the Reconciliation Sublayer for all 10 Gb/s PHY implementations (e.g., not only 10GBASE-R but also other types of 10 Gigabit PHY entities).

The 10GBASE-R PCS provides all services required by the XGMII, including the following:

a) Encoding (decoding) of eight XGMII data octets to (from) 66-bit blocks (64B/66B).
b) Transferring encoded data to (from) the PMA in 16 bit transfers.
c) When connected to a WAN PMD, deleting (inserting) idles to compensate for the rate difference between the MAC and PMD.
d) Determining when a functional link has been established and informing the management entity via the MDIO when the PHY is ready for use.

49.1.4.2 WAN Interface Sublayer (WIS)

The WIS provides a medium-independent means for the PCS to operate over WAN links. It creates a 10GBASE-W encoding by encapsulating the encoded data steam from the 10GBASE-R PCS in frames compatible with SONET and SDH transmission formats. The WIS is specified in Clause 50.

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49.1.4.3 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 10GBASE-R PMA performs the following functions:

a) Mapping of transmit and receive data streams between the PCS or WIS and PMA via the PMA service interface.
b) Serialization (deserialization) of bits for transmission (reception) on the underlying serial PMD.
c) Recovery of clock from the received data stream.
d) Mapping of transmit and receive bits between the PMA and PMD via the PMD service interface.
e) Optionally provides data loopback at the PMA service interface.

The PMA is specified in Clause 51.

49.1.4.4 Physical Medium Dependent (PMD) sublayer

The PMD and its media are specified in Clause 52.

The MDI, logically subsumed within each PMD subclause, is the actual medium attachment for the various supported media.

49.1.4.5 Bit ordering across 10GBASE-R and 10GBASE-W sublayers.

The ordering of bits and octets for the case when no WIS is present between the PCS and PMA is shown in Figure 49–2. The diagram depicts the bit mappings for the data path at the service interfaces.

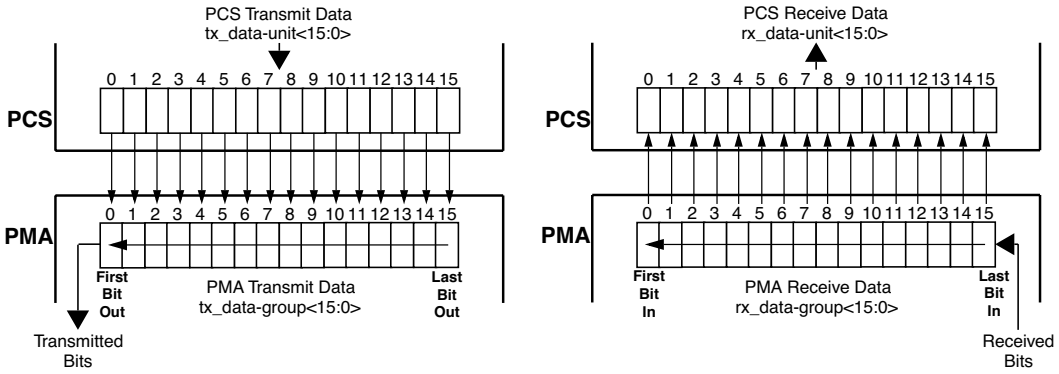


Figure 49–2—10GBASE-R PHY Transmission order

The bit/octet ordering when a WIS is interposed between the PCS and PMA is shown in Figure 49–3. The details of WIS frame generation, as well as internal interfaces, have been omitted. Note that since SONET convention is to send the most significant bit (MSB) of each octet first and Ethernet convention is to send the least significant bit (LSB) of each octet first, the LSBs from the PCS octets are mapped into the MSBs of the WIS octets. It should be clear from the diagram that the Ethernet order of transmission (i.e., least-significant bit first), and hence the error detecting properties of the Ethernet CRC, are preserved in spite of the different bit ordering conventions followed by the WIS. Also, the SONET/SDH bit labeling conventions are different from the usual IEEE 802.3 bit labeling. The bits of a SONET/SDH octet are labeled from 1 to 8 with bit 1 being the MSB. Ethernet conventions label bits of an n-bit field from 0 to n–1 with bit 0 being the LSB. Figure 49–3 shows the results of these conventions. For example, tx_data-unit<0> through tx_data-unit<7> map to bits 1 through 8 respectively of a WIS octet.

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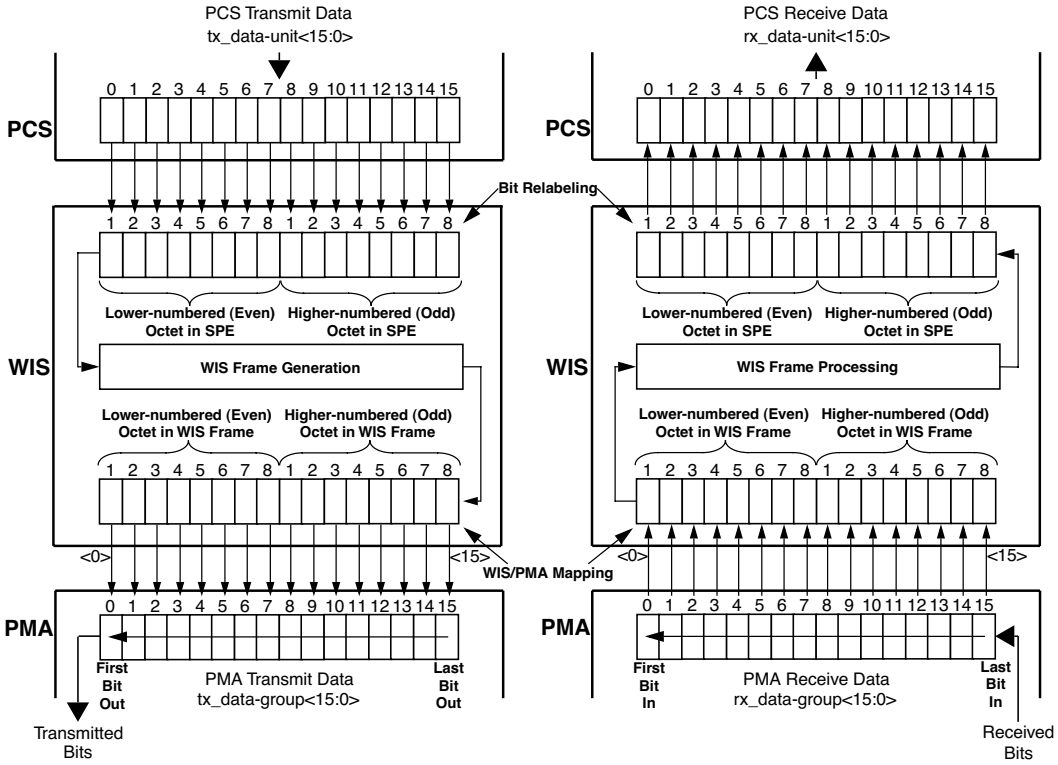


Figure 49–3—10GBASE-W PHY Transmission order

49.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-R. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. The PCS service interface is the XGMII that is defined in Clause 46. The XGMII has an optional physical instantiation. An optional physical instantiation of the PMA service interface has also been defined (see Clause 51). It is called XSBI (10 Gigabit Sixteen Bit Interface). Figure 49–4 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-R.

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XGMII or the PCS may connect to an XGXS sublayer. The XGXS and the Reconciliation Sublayer provide the same service interface to the PCS. The lower interface of the PCS may connect to the WIS to support a WAN PMD or to the PMA sublayer to support a 10GBASE-R LAN PMD. The WIS and PMA interfaces are functionally equivalent except for data rate. When the PCS is connected directly to a LAN PMA, the nominal rate of the PMA service interface is 644.53 Mtransfers/s which provides capacity for the MAC data rate of 10 Gb/s. When the PCS is connected to a WAN PMA, the nominal rate of the WIS service interface is 599.04 Mtransfers/s and the MAC uses IFS stretch mode to ensure that there will be enough idle time that the PCS can delete idles to adjust to the lower rate. Since the data rates are different, WIS and PMA interface connections pose somewhat different constraints. The PCS shall support connection to either a WIS or to a PMA and may optionally support both.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

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49.1.6 Functional block diagram

Figure 49–4 provides a functional block diagram of the 10GBASE-R PHY.

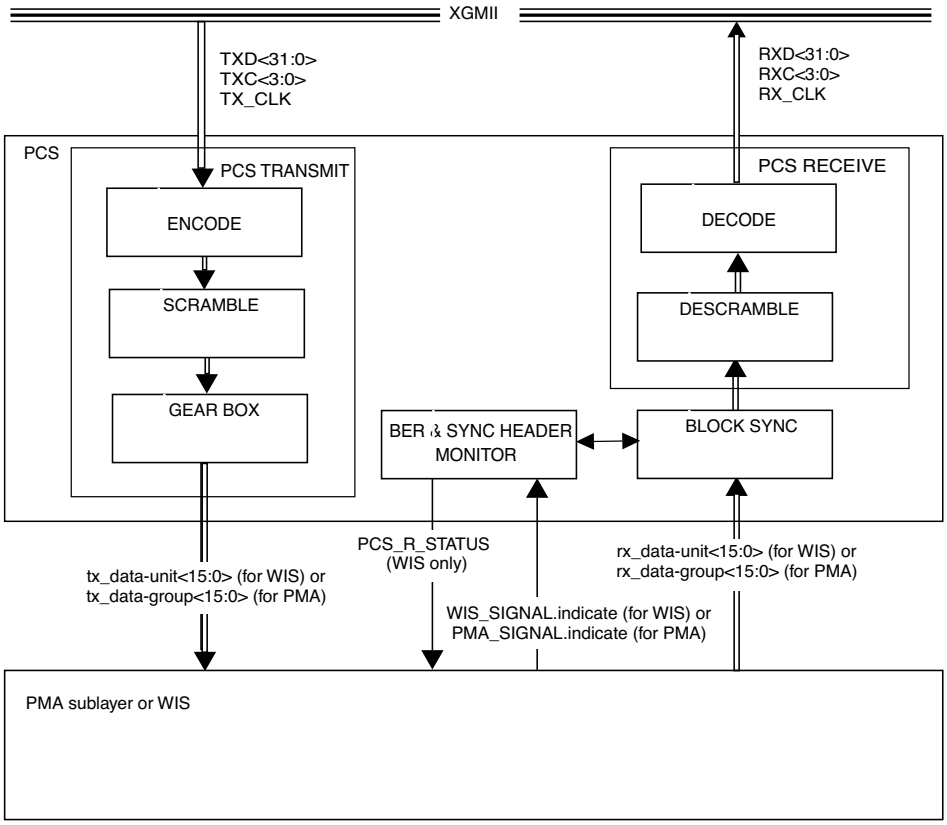


Figure 49–4—Functional block diagram

49.2 Physical Coding Sublayer (PCS)

49.2.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-R PCS to transfer information to and from a PCS client. A PCS client is generally the Reconciliation Sublayer or an XGXS sublayer. The PCS Interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

49.2.2 Functions within the PCS

The PCS comprises the PCS Transmit, Block Synchronization, PCS Receive, and BER monitor processes for 10GBASE-R. The PCS shields the Reconciliation Sublayer (and MAC) from the specific nature of the underlying channel. The PCS transmit channel and receive channel can each operate in normal mode or, when not attached to a WIS, test-pattern mode. When the PCS is attached to a WIS, the WIS provides the test-pattern functionality.

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When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals (TXCn = 1) and receive control signals (RXCn = 1). When communicating with the PMA or WIS, the PCS uses a 16-bit wide, synchronous data path that conveys 16 encoded bits. Alignment to 64B/66B block is performed in the PCS. The WIS and PMA sublayers operate independent of block and packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

When the transmit channel is in normal mode, the PCS Transmit process continuously generates blocks based upon the TXD <31:0> and TXC <3:0> signals on the XGMII. The Gearbox function of the PCS Transmit process then packs the resulting bits into 16-bit transmit data-units. Transmit data-units are sent to the PMA or WIS service interface via the PMA_UNITDATA.request or WIS_UNITDATA.request primitive, respectively. When the WIS is present, the PCS Transmit process also adapts between the XGMII and WIS data rates by deleting idle characters.

When the transmit channel is in test-pattern mode, a test pattern is packed into the transmit data-units that are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

When the receive channel is in normal mode, the PCS Synchronization process continuously monitors PMA_SIGNAL.indicate(SIGNAL_OK) or WIS_SIGNAL.indicate(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indicate primitive or the WIS_UNITDATA.indicate primitive. It attains block sychronization based on the 2-bit synchronization headers and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the sync_status flag to indicate whether the PCS has obtained synchronization.

When the PCS Synchronization process has obtained synchronization, the BER monitor process monitors the signal quality asserting hi_ber if excessive errors are detected. When sync_status is asserted and hi_ber is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII. When the WIS is present, the PCS Receive process also adapts between the WIS and XGMII data rates by inserting idle characters. The PCS Receive process also sends the WIS_SIGNAL.request(PCS_R_STATUS) primitive to the WIS to indicate its status. The primitive is sent when the value of PCS_R_STATUS changes. The value of PCS_R_STATUS shall be FAIL when the Receive state machine is in the RX_INIT state and OK otherwise.

When the receive channel is in test-pattern mode, the BER monitor process is disabled. The Receive process will be held in the RX_INIT state. The received bits will be compared to the test pattern and errors counted.

A PCS that supports direct connection to a PMA shall provide transmit test-pattern mode for the square wave and pseudo-random patterns, and shall provide receive test-pattern mode for the pseudo-random pattern. It may provide support for the PRBS31 test pattern. Support of the optional PRBS31 test pattern shall include both the transmit and the receive capability for that pattern. Test-pattern mode is activated separately for transmit and receive. A PCS that supports direct connection to a PMA shall support transmit test-pattern mode and receive test-pattern mode operating simultaneously so as to support loopback testing. Test-pattern mode is provided by the WIS when a WIS is present.

49.2.3 Use of blocks

The PCS maps XGMII signals into 66-bit blocks, and vice versa, using a 64B/66B coding scheme. The synchronization headers of the blocks allow establishment of block boundaries by the PCS Synchronization process. Blocks are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks as provided by the rules in 49.2.4.

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49.2.4 64B/66B transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encodings defined by the transmission code ensure that sufficient transitions are present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, the synchronization headers of the code enable the receiver to achieve block alignment on the incoming PHY bit stream. The 64B/66B transmission code specified for use in this standard has a high transition density and is a run-length-limited code.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 49–5 for transmit and Figure 49–6 for receive. These figures illustrate the processing of a block containing 8 data octets. See 49.2.4.3 for information on how blocks containing control characters are mapped. Note that the sync header is generated by the encoder and bypasses the scrambler.

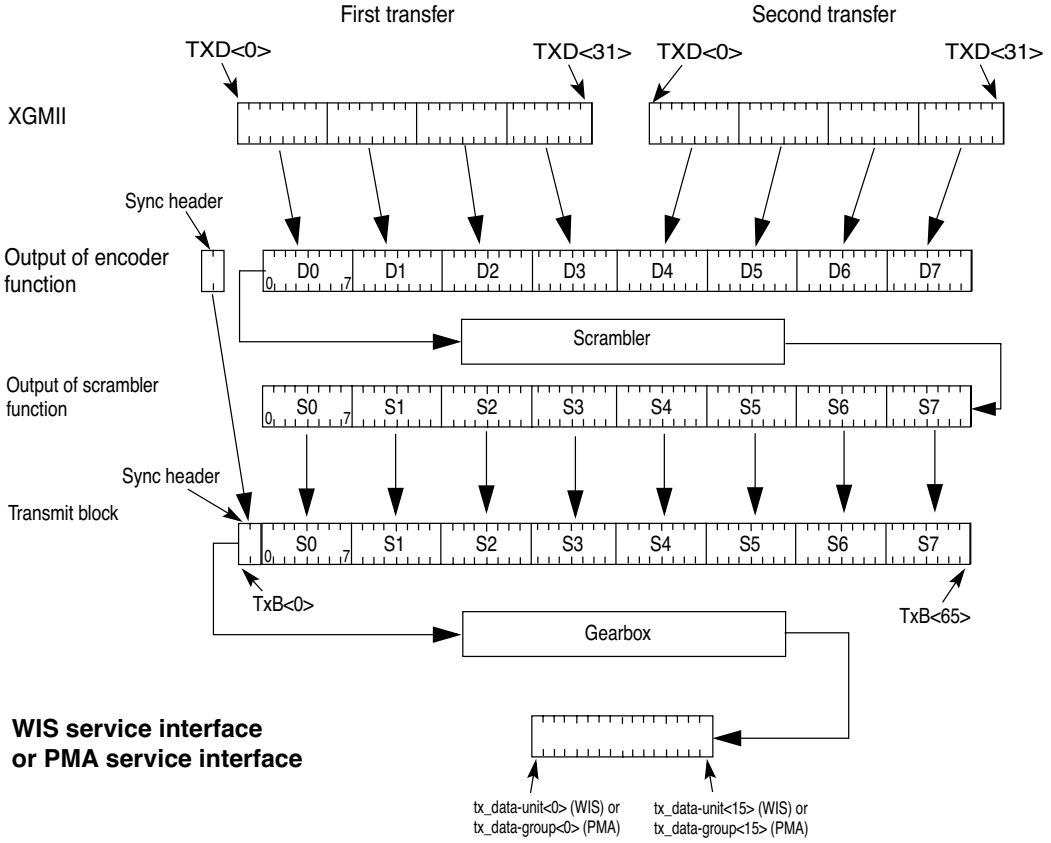


Figure 49–5—PCS Transmit Bit Ordering

49.2.4.1 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

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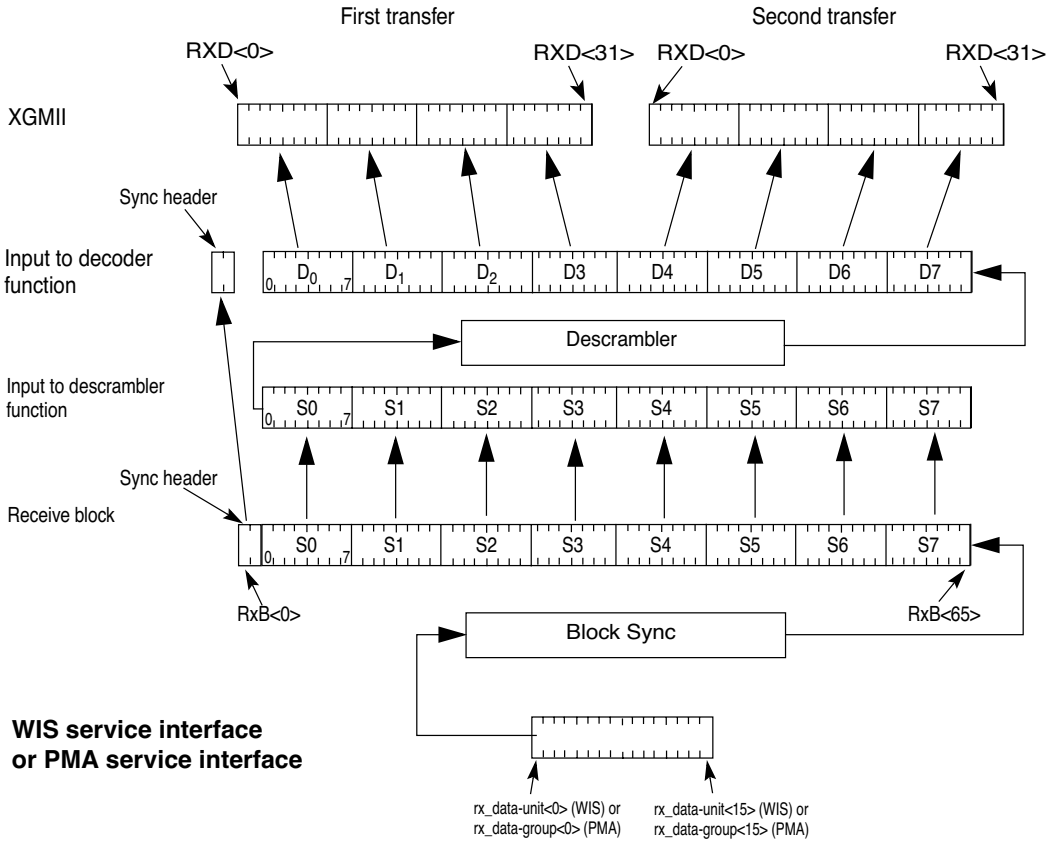


Figure 49–6—PCS Receive Bit Ordering

64B/66B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/ and /T/ are labeled C_0 to C_7. The control character for ordered_set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

Two consecutive XGMII transfers provide eight characters that are encoded into one 66-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfers.

Contents of block type fields, data octets and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1e is sent from left to right as 01111000. The bits of a transmitted or received block are labeled TxB<65:0> and RxB<65:0> respectively where TxB<0> and RxB<0> represent the first transmitted bit. The value of the sync header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

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49.2.4.2 Transmission order

Block bit transmission order is illustrated in Figure 49–5 and Figure 49–6. Note that these figures show the mapping from XGMII to 64B/66B block for a block containing eight data characters.

49.2.4.3 Block structure

Blocks consist of 66 bits. The first two bits of a block are the synchronization header (sync header). Blocks are either data blocks or control blocks. The sync header is 01 for data blocks and 10 for control blocks. Thus, there is always a transition between the first two bits of a block. The remainder of the block contains the payload. The payload is scrambled and the sync header bypasses the scrambler. Therefore, the sync header is the only position in the block that always contains a transition. This feature of the code is used to obtain block synchronization.

Data blocks contain eight data characters. Control blocks begin with an 8-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a 7-bit control code or a 4-bit O Code. Each control block contains eight characters.

The format of the blocks is as shown in Figure 49–7. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 66-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the Input Data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Bits and field positions are shown with the least significant bit on the left. Hexadecimal numbers are shown in normal hexadecimal. For example the block type field 0x1e is sent as 01111000 representing bits 2 through 9 of the 66 bit block. The least significant bit for each field is placed in the lowest numbered position of the field.

All unused values of block type field[10] are reserved.

49.2.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-R PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-R PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-R PCS encodes each of the other control characters into a 7-bit C code).

The control characters and their mappings to 10GBASE-R control codes and XGMII control codes are specified in Table 49–1. All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

[10]The block type field values have been chosen to have a 4-bit Hamming distance between them. The only unused value which maintains the Hamming distance is 0x00.

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Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block Type Field**							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 49–7—64B/66B Block Formats

49.2.4.5 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and local fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 10 Gigabit Ethernet uses one kind of ordered_set: the sequence ordered_set (see 46.3.4). The sequence ordered_set control character is denoted /Q/. An additional ordered_set, the signal ordered_set, has been reserved and it begins with another control code. The 4-bit O field encodes the control code. See Table 49–1 for the mappings.

49.2.4.6 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The sync field has a value of 00 or 11.
b) The block type field contains a reserved value.
c) Any control character contains a value not in Table 49–1.
d) Any O code contains a value not in Table 49–1.
e) The set of eight XGMII characters does not have a corresponding block format in Figure 49–7.

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49.2.4.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

Table 49–1—Control Codes

Control Character	Notation	XGMII Control Code	10GBASE-R Control Code	10GBASE-R O Code	8B/10B Code[a]
idle	/I/	0x07	0x00		K28.0 or K28.3 or K28.5
start	/S/	0xfb	Encoded by block type field		K27.7
terminate	/T/	0xfd	Encoded by block type field		K29.7
error	/E/	0xfe	0x1e		K30.7
Sequence ordered_set	/Q/	0x9c	Encoded by block type field plus O code	0x0	K28.4
reserved0	/R/[b]	0x1c	0x2d		K28.0
reserved1		0x3c	0x33		K28.1
reserved2	/A/	0x7c	0x4b		K28.3
reserved3	/K/	0xbc	0x55		K28.5
reserved4		0xdc	0x66		K28.6
reserved5		0xf7	0x78		K23.7
Signal ordered_set[c]	/Fsig/	0x5c	Encoded by block type field plus O code	0xF	K28.2

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.
[b]The codes for /A/, /K/, and /R/ are used on the XAUI interface to signal idle. They are not present on the XGMII when no errors have occurred, but certain bit errors cause the XGXS to send them on the XGMII.
[c]Reserved for INCITS T11 Fibre Channel use.

49.2.4.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<0:7> and RXD<0:7>). Receipt of an /S/ on any other octet of TxD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

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49.2.4.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

49.2.4.10 ordered_set (/O/)

The ordered_set control characters (/O/) indicate the start of an ordered_set. There are two kinds of ordered sets: the sequence ordered_set and the signal ordered_set (which is reserved). When it is necessary to designate the control character for the sequence ordered_set specifically, /Q/ will be used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered_set.

Sequence ordered_sets may be deleted by the PCS to adapt between clock rates. Such deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two. Only Idles may be inserted for clock compensation. Signal ordered_sets are not deleted for clock compensation.

49.2.4.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. It is also sent when invalid blocks are received. The /E/ allows physical sublayers such as the XGXS and PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 49.2.13.2.3 for further information.

49.2.5 Transmit process

The transmit process generates blocks based upon the TXD<31:0> and TXC<3:0> signals received from the XGMII. Two XGMII data transfers are encoded into each block. It takes 4.125 PMA_UNITDATA or WIS_UNITDATA transfers to send a block of data. Therefore, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 16:33, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process will need to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates. The WIS data rate is always slower than the XGMII data rate and a PCS connected to a WIS must delete idles or sequence ordered sets to adapt between rates.

The transmit process generates blocks as specified in the transmit process state machine. The contents of each block are contained in a vector tx_coded<65:0>, which is passed to the scrambler. tx_coded<1:0> contains the sync header and the remainder of the bits contain the block payload.

49.2.6 Scrambler.

The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 49–8. This implements the scrambler polynomial:[11]

$$G(x) = 1 + x^{39} + x^{58} \quad (49–1)$$

[11]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

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There is no requirement on the initial value for the scrambler. The scrambler is run continuously on all payload bits. The sync header bits bypass the scrambler.

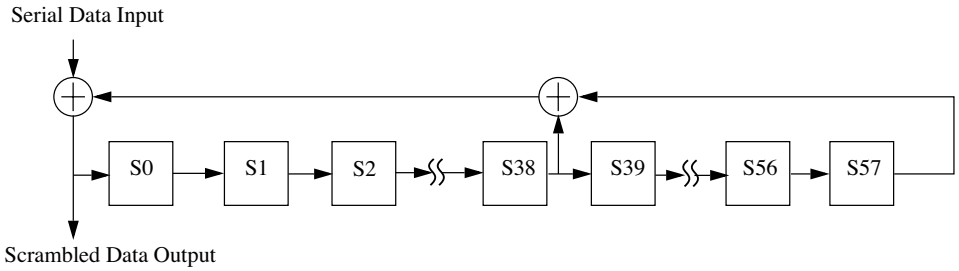


Figure 49–8—Scrambler

49.2.7 Gearbox

The gearbox adapts between the 66-bit width of the blocks and the 16-bit width of the PMA or WIS interface. It receives the 66-bit blocks. When the transmit channel is operating in normal mode, the gearbox sends 16 bits of transmit data at a time via WIS_UNITDATA.request or PMA_UNITDATA.request primitives. The UNITDATA.request primitives are fully packed with bits. For example, if one block happened to start with the sync header on bits 0 and 1 of a PMA_UNITDATA.request, then the last two bits of that block would be on bits 0 and 1 of a PMA_UNITDATA.request and the next block would begin with a sync header on bits 2 and 3 of that PMA_UNITDATA.request. When a PMA_UNITDATA.request or WIS_UNITDATA.request contains bits from two blocks, then the bits from the first block shall be placed in the lowest numbered bits of tx_data-group<15:0>. The bits shall be packed into the tx_data-group in sequence with the lowest numbered bit of the block going into the lowest numbered bit of the part of tx_data-group<15:0> bits containing bits from that block (see Figure 49-5).

The gearbox functionality is necessary when the optional PMA compatibility interface, XSBI, is implemented since that interface passes data over a 16-bit wide path. It is also necessary when connecting to a WIS since the WIS processes the data stream with 8-bit granularity. When neither the WIS nor the XSBI is implemented, the internal data-path width between the PCS and PMA is an implementation choice. Depending on the path width, the gearbox functionality may not be necessary.

49.2.8 Test-pattern generators

When the transmit channel is operating in test-pattern mode, it sends 16 bits of test pattern at a time via PMA_UNITDATA.request primitives. When the PCS allows direct connection to the PMA, the test-pattern generator shall be implemented. The test-pattern generator does not apply to a PCS, which only supports connection to the WIS. A PCS which supports both WIS and direct PMA attachment may reject or allow an attempt to activate a transmit test-pattern mode when a WIS is attached.

There are two types of required transmit test patterns: square wave and pseudo-random. The square wave pattern is intended to aid in conducting certain transmitter tests. It is not intended for receiver tests and the receiver is not expected to receive this test pattern. The pseudo-random test-pattern mode is suitable for receiver tests and for certain transmitter tests. There is also an optional PRBS31 test pattern, which may be used for some transmit and receiver tests. When this option is supported, both the PRBS31 test-pattern generator and the PRBS31 test-pattern checker shall be provided. See Clause 52.9 for recommendations on the appropriate pattern for tests.

When square wave pattern is selected, the PCS will send a repeating pattern of n ones followed by n zeros where n may be any number between 4 and 11 inclusive. The value of n is an implementation choice.

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When pseudo-random pattern is selected, the test pattern is generated by the scrambler using the seeds loaded through the MDIO registers and the selected data pattern. The scrambler is loaded with a seed or its inverse at the start of a block every 128 blocks. The seeds are loaded in the following pattern:

Seed A
Seed A Invert
Seed B
Seed B Invert

Invert indicates that the seed is inverted for that load. Either 64 zeros or the 64-bit encoding for two Local Fault ordered_sets can be selected as the data pattern. After loading Seed A or Seed B, the scrambler input shall be driven with the data pattern. After loading Seed A Invert or Seed B Invert, the scrambler input shall be driven with the inverse of the data pattern. While in pseudo-random test-pattern mode, the sync headers will be the control sync header, 10. Thus the pseudo-random test pattern is a series of blocks with the control sync header and a pseudo-random payload. The characteristics of the pseudo-random test pattern can be varied by varying the seed values and data input.

When the optional PRBS31 mode is selected, the PRBS31 pattern generator sends 16 bits of PRBS31 test pattern at a time via PMA_UNITDATA.request primitives. The PRBS31 test pattern is the output of a Pseudo-Random Bit Sequence of order 31 (PRBS31) generator. The PRBS31 pattern generator shall produce the same result as the implementation shown in Figure 49–9. This implements the inverted version of the bit stream produced by the polynomial:[12]

$$G(x) = 1 + x^{28} + x^{31} \tag{49–2}$$

The initial value of the PRBS31 pattern generator shall not be all zeros. It may be any other value.

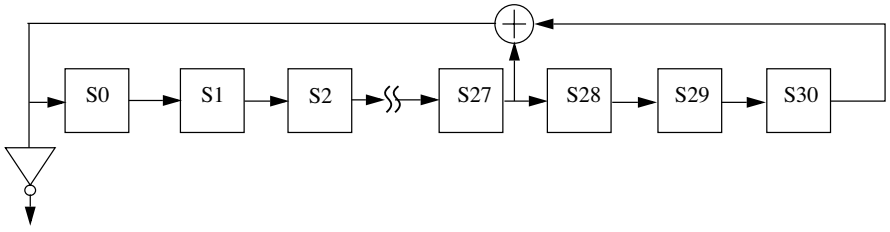


Figure 49–9—PRBS31 pattern generator

49.2.9 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 16-bit PMA_UNITDATA.request or WIS_UNITDATA.request primitives. It shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state machine shown in Figure 49–12.

[12]The convention here, which considers the most recent bit into the PRBS generator to be the lowest order term, is consistant with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the PRBS generator to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–2). In case of doubt, note that the conformance requirement is based on the representation in the figure rather than the polynomial equation.

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49.2.10 Descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It shall produce the same result as the implementation shown in Figure 49–10.

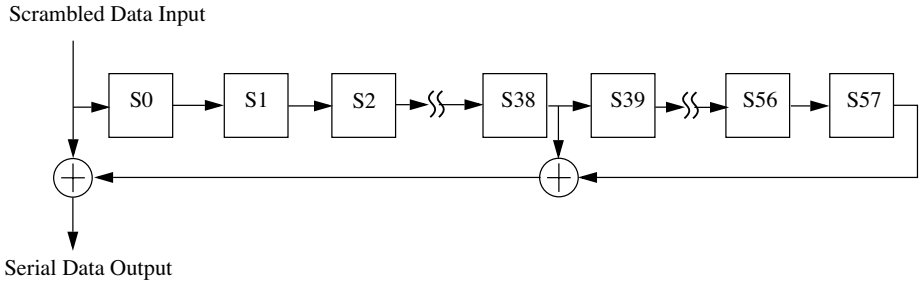


Figure 49–10—Descrambler

49.2.11 Receive process

The receive process decodes blocks to produce RXD<31:0> and RXC<3:0> for transmission to the XGMII. Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized to a 16:33 ratio, the receive process will insert idles, delete idles, or delete sequence ordered sets to adapt between rates. The WIS data rate is always slower than the XGMII data rate and a PCS connected to a WIS will insert idles to adapt between the rates.

The receive process decodes blocks as specified in the receive state machine shown in Figure 49–15.

49.2.12 Test-pattern checker

When the PCS allows direct connection to the PMA, the pseudo-random test-pattern checker shall be implemented. The pseudo-random test-pattern checker does not apply to a PCS, which only supports connection to the WIS. When the PRBS31 test-pattern option is supported, the PRBS31 receive test-pattern checker shall be implemented. A PCS that supports both WIS and direct PMA attachment may reject or allow an attempt to activate a receive test-pattern mode when a WIS is attached.

When the receive channel is operating in pseudo-random test-pattern mode, the pseudo-random test-pattern checker checks the bits received via PMA_UNITDATA.indicate primitives.

The pseudo-random test-pattern checker utilizes the lock state machine and the descrambler operating as they do during normal data reception. The hi_ber state machine is disabled during receive test-pattern mode. When block_lock is true and the pseudo-random receive test-pattern mode is active, the pseudo-random test-pattern checker observes the output from the descrambler. When the output of the descrambler is the data pattern or its inverse, a match is detected. Since the transmitter's scrambler is loaded with a seed value every 128 blocks and the receiver's descrambler is running normally, a mismatch will be detected once every 128 blocks in the absence of errors. The pseudo-random test-pattern checker will count 128-block windows. When operating in pseudo-random test pattern, the test-pattern error counter counts blocks with a mismatch corrected to remove the effect of loading a new seed. The first block with a mismatch in a window shall not increment the test-pattern error counter. Any subsequent block with a mismatch in a window indicates an error and shall increment the test-pattern error counter.

When the receive channel is operating in PRBS31 test mode, the PRBS31 pattern checker checks the bits received in PMA_UNITDATA.indicate primitives relative to the PRBS31 test pattern.

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The PRBS31 pattern error checker is self-synchronizing. It compares each bit received to the result of the PRBS31 generator based on the prior 31 bits received. It shall produce the same result as the implementation shown in Figure 49–11. When no errors occur, the PRBS31 pattern error signal will be zero. When an isolated bit error occurs, it will cause the PRBS31 pattern error signal to go high three times; once when it is received and once when it is at each tap. The test-pattern error counter shall increment once for each bit time that the PRBS31 pattern error signal is high.

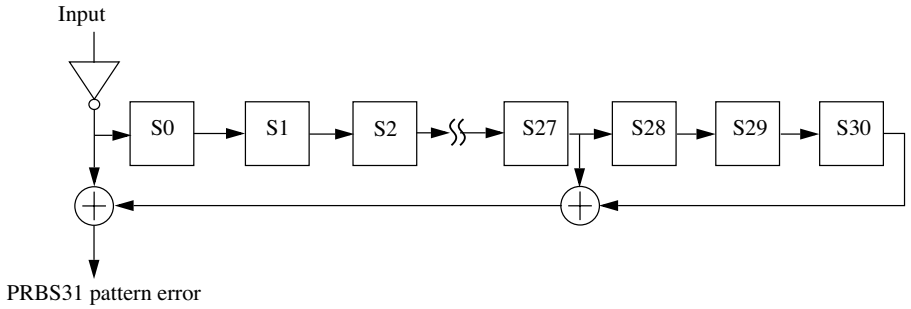


Figure 49–11—PRBS31 pattern checker

Note that the test-pattern error counter behavior is dependent on the test-pattern mode. In pseudo-random test mode, it is counting block errors. In PRBS31 test mode, it is counting bit errors at the PRBS31 pattern checker output.

49.2.13 Detailed functions and state diagrams

49.2.13.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

49.2.13.2 State variables

49.2.13.2.1 Constants

EBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72 bit vector to be sent to the XGMII interface containing two Local Fault ordered_sets. The Local Fault ordered_set is defined in 46.3.4.

LBLOCK_T<65:0>
: 66 bit vector to be sent to the PMA containing two Local Fault ordered sets.

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49.2.13.2.2 Variables

ber_test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when BER_TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA or the WIS to evaluate the header of the next block

block_lock
: Boolean variable that is set true when receiver acquires block delineation

hi_ber
: Boolean variable which is asserted true when the ber_cnt exceeds 16 indicating a bit error ratio $>10^{-4}$

reset
: Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

r_test_mode
: Boolean variable that is asserted true when the receiver is in test-pattern mode.

rx_coded<65:0>
: Vector containing the input to the 64B/66B decoder. The format for this vector is shown in Figure 49–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<65>.

rx_raw<71:0>
: Vector containing two successive XGMII transfers. RXC<0> through RXC<3> for the first transfer are placed in rx_raw<0> through rx_raw<3>, respectively. RXC<0> through RXC<3> for the second transfer are placed in rx_raw<4> through rx_raw<7>, respectively. RXD<0> through RXD<31> for the first transfer are placed in rx_raw<8> through rx_raw<39>, respectively. RXD<0> through RXD<31> for the second transfer are placed in rx_raw<40> through rx_raw<71>, respectively.

sh_valid
: Boolean indication that is set true if received block rx_coded has valid sync header bits. That is, sh_valid is asserted if rx_coded<0> ≠ rx_coded<1> and de-asserted otherwise.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indicate(SIGNAL_OK) or WIS_UNITDATA.indicate(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the Block Lock State Machine has been completed indicating that the next candidate block sync position can be tested.

test_sh
: Boolean variable that is set true when a new sync header is available for testing and false when TEST_SH state is entered. A new sync header is available for testing when the Block Sync process has accumulated enough bits from the PMA or the WIS to evaluate the header of the next block

tx_coded<65:0>
: Vector containing the output from the 64B/66B encoder. The format for this vector is shown in Figure 49–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<65>.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<0> through TXC<3> for the first transfer are placed in tx_raw<0> through tx_raw<3>, respectively. TXC<0> through TXC<3> for the second transfer are placed in tx_raw<4> through tx_raw<7>, respectively. TXD<0> through TXD<31> for the first transfer are placed in tx_raw<8> through tx_raw<39>, respectively. TXD<0> through TXD<31> for the second transfer are placed in tx_raw<40> through tx_raw<71>, respectively.

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49.2.13.2.3 Functions

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 49.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<63:0> is sent to the scrambler. The two high order sync bits bypass the scrambler. The ENCODE function shall encode the block as specified in 49.2.4.

R_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 66-bit rx_coded vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x1e and eight valid control characters other than /E/;
b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a sync header of 10 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.

D; The vector contains a sync header of 01.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-R control code specified in Table 49–1. A valid O code is one containing an O code specified in Table 49–1.

R_TYPE(rx_coded<65:0>)

Returns the R_BLOCK_TYPE of the rx_coded<65:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains one of the following:
a) eight valid control characters other than /O/, /S/, /T/ and /E/;
b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;
c) two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

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E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 49–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 49–1.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

49.2.13.2.4 Counters

ber_cnt
Count up to a maximum of 16 of the number of invalid sync headers within the current 125 μs period.

sh_cnt
Count of the number of sync headers checked within the current 64 block window.

sh_invalid_cnt
Count of the number of invalid sync headers within the current 64 block window.

49.2.13.2.5 Timers

State diagram timers follow the conventions of 14.2.3.2.

125us_timer
Timer that is triggered every 125 μs +1%, –25%.

49.2.13.3 State diagrams

The Lock state machine shown in Figure 49–12 determines when the PCS has obtained lock to the received data stream. The BER Monitor state machine shown in Figure 49–13 monitors the received signal for high bit error ratio.

The Transmit state machine shown in Figure 49–14 controls the encoding of transmitted blocks. It makes exactly one transition for each transmit block processed. Though the Transmit state machine sends Local Fault ordered sets when reset is asserted, the scrambler and gearbox may not be operational during reset. Thus, the Local Fault ordered sets may not appear on the WIS or PMA service interface.

The Receive state machine shown in Figure 49–15 controls the decoding of received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of Lock, BER Monitor, Transmit and Receive as specified in these state machines.

49.2.14 PCS Management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

49.2.14.1 Status

PCS_status:
Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_ber is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is

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reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:
Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_ber:
Indicates the state of the hi_ber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

49.2.14.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

ber_count:
6-bit counter that counts each time BER_BAD_SH state is entered. This counter is reflected in MDIO register bits 3.33.13:8. Note that this counter counts a maximum of 16 counts per 125 μs since the BER_BAD_SH can be entered a maximum of 16 times per 125 μs window.

errored_block_count:
8-bit counter. When the receiver is in normal mode, errored_block_count counts once for each time RX_E state is entered. This counter is reflected in MDIO register bits 3.33.7:0.

test_pattern_error_count:
16-bit counter. When the receiver is in test-pattern mode, the test_pattern_error_count counts errors as described in 49.2.12. This counter is reflected in MDIO register bits 3.43.14:0.

49.2.14.3 Test mode control

tx_test_mode:
Boolean variable controlling transmit channel operating mode. When false, the transmit channel operates in normal mode. When true, the transmit channel operates in test-pattern mode.

rx_test_mode:
Boolean variable controlling receive channel operating mode. When false, the receive channel operates in normal mode. When true, the receive channel operates in test-pattern mode.

49.2.14.4 Loopback

The PCS shall be placed in Loopback mode when the Loopback bit in MDIO register 3.0.14 is set to a logic one. In this mode, the PCS shall accept data on the transmit path from the XGMII and return it on the receive path to the XGMII. In addition, the PCS shall transmit a continuous stream of 0x00FF data words to the PMA or WIS sublayer, and shall ignore all data presented to it by the PMA or WIS sublayer.

49.2.15 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-R PCS shall be no more than 3584 BT.

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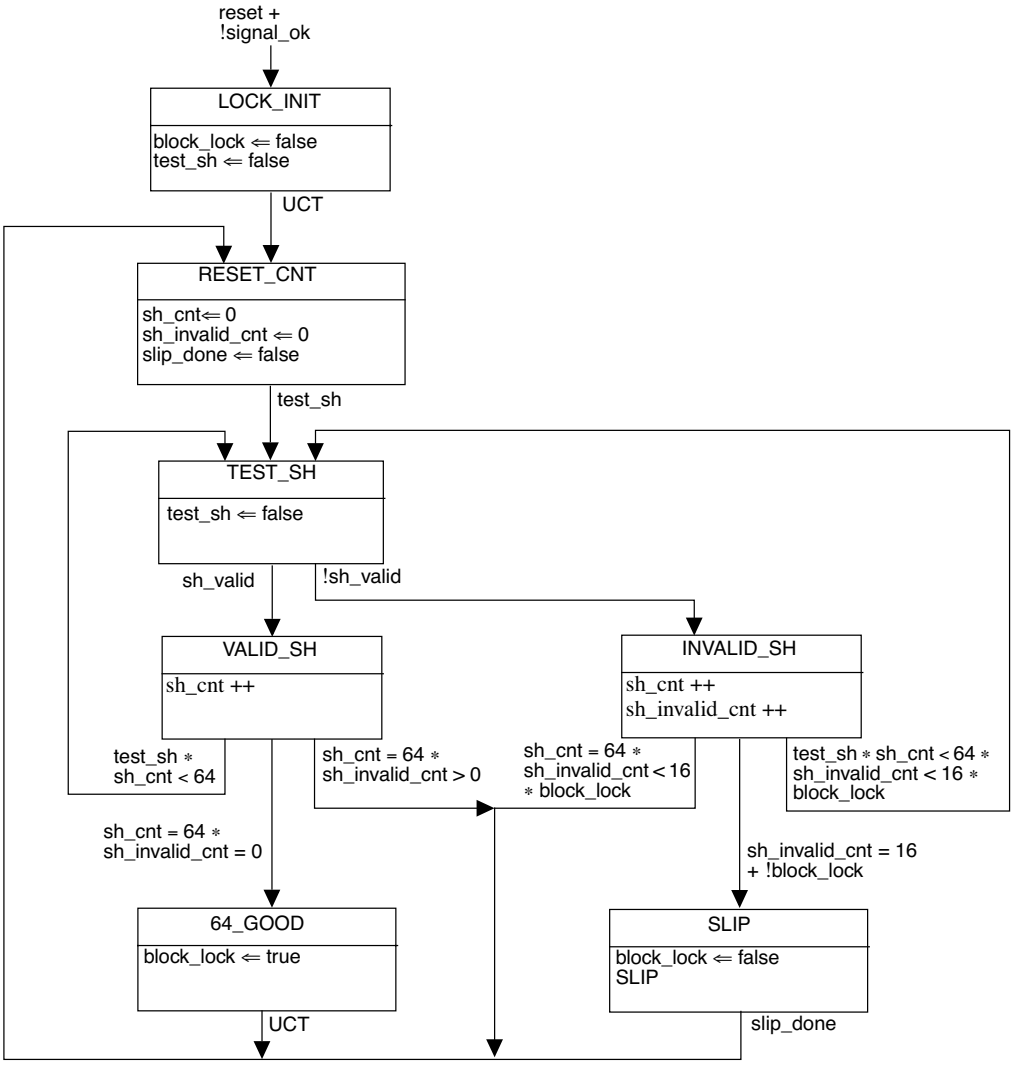


Figure 49–12—Lock state machine

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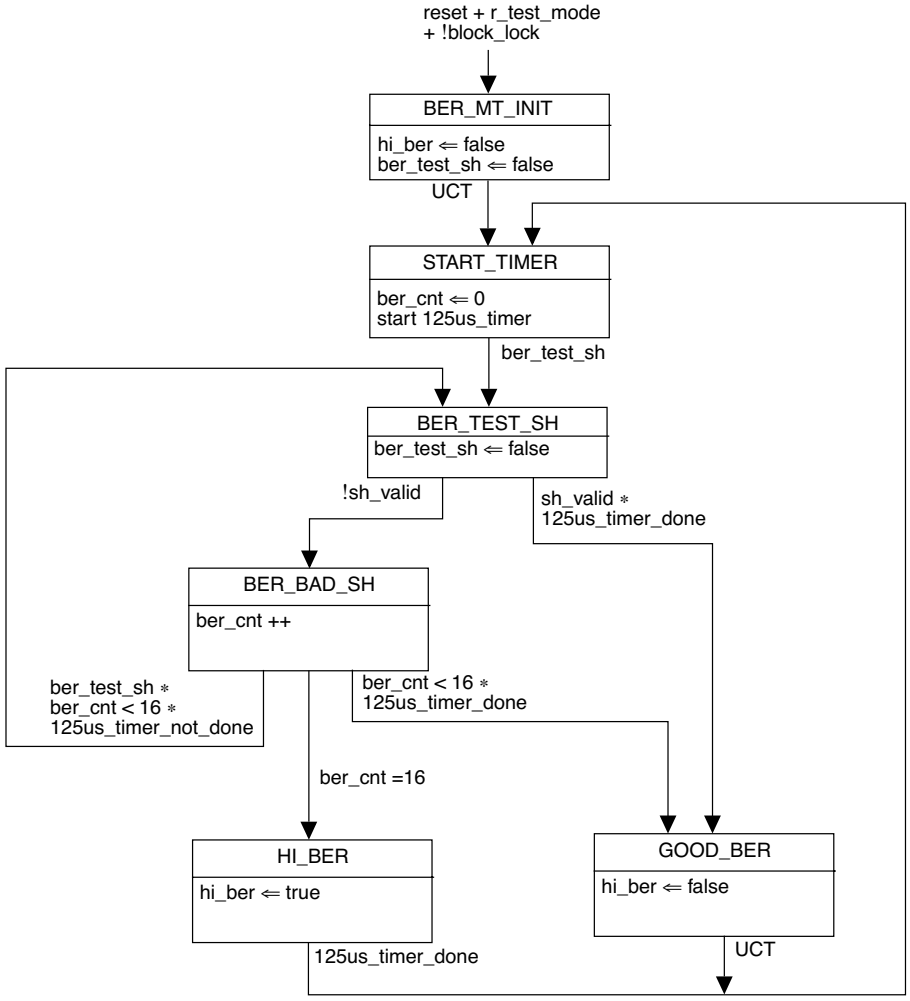


Figure 49–13—BER monitor state machine

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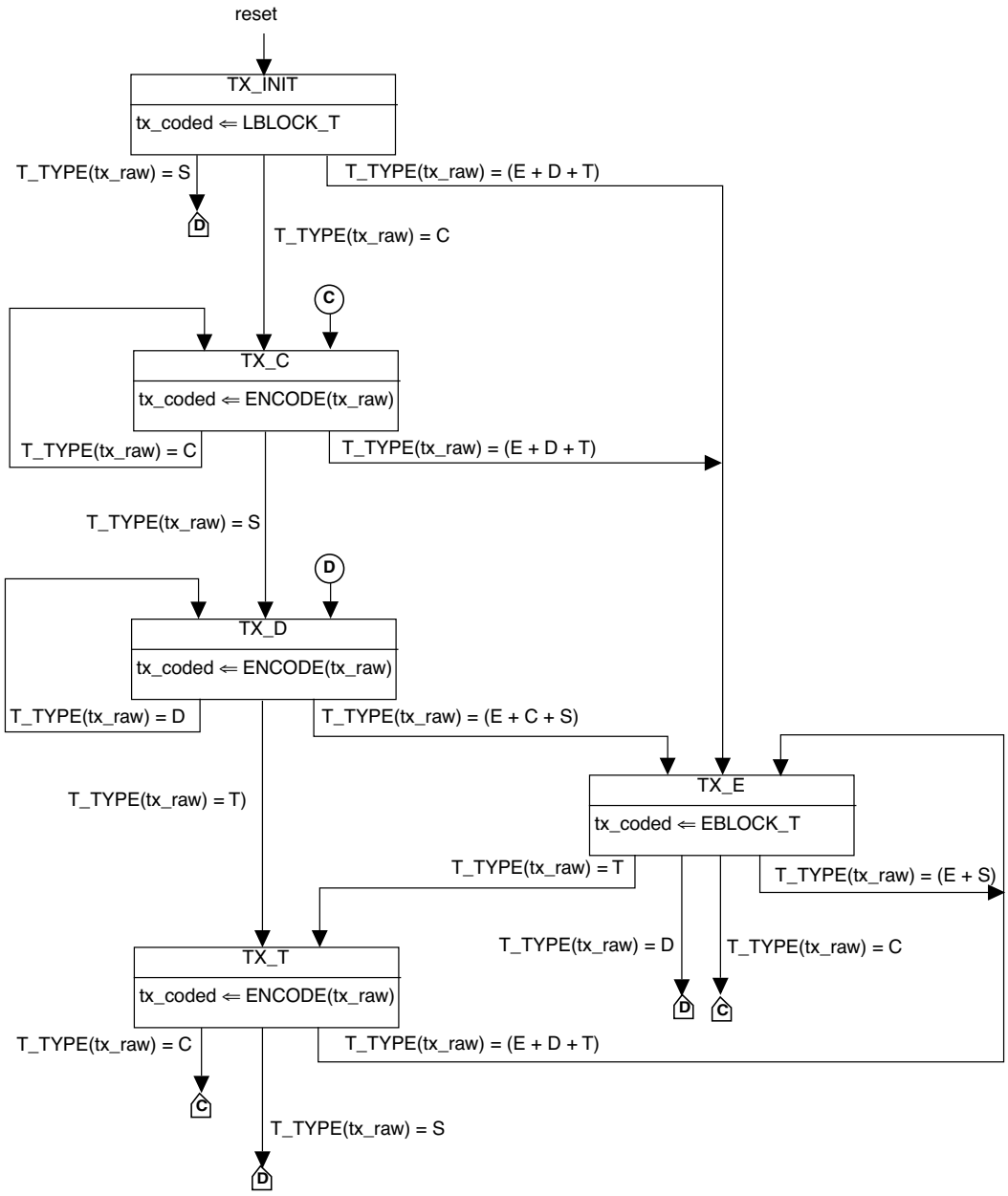


Figure 49–14—Transmit state machine

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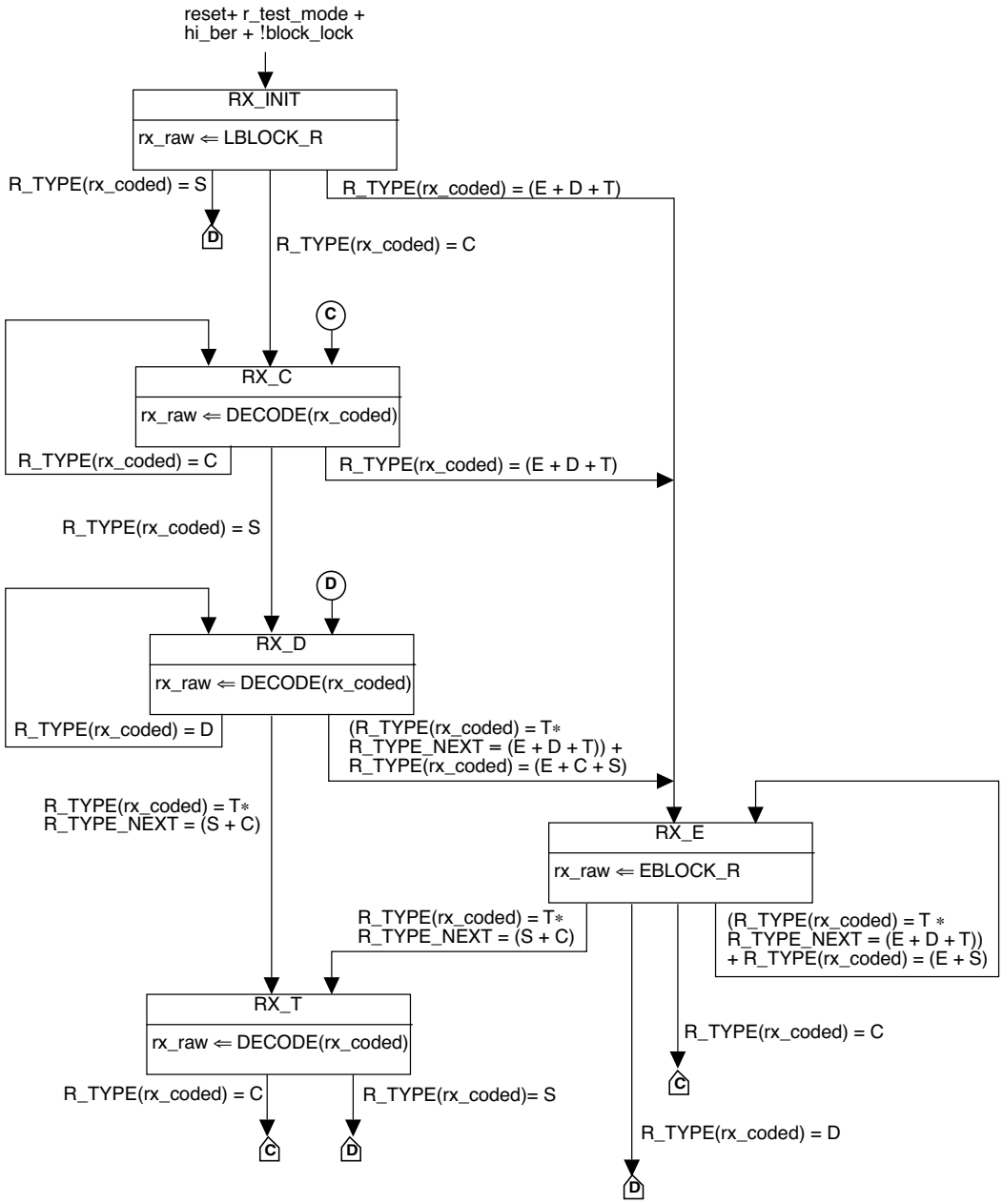


Figure 49–15—Receive state machine

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49.3 Protocol Implementation Conformance Statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[13]

49.3.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Coding Sublayer (PCS), type 10GBASE-R, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

49.3.2 Identification

49.3.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

49.3.2.2 Protocol summary

Identification of protocol standard	IEEE Std. 802.3ae-2002, Clause 49, Physical Coding Sublayer (PCS), type 10GBASE-R
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)	
Date of Statement	

[13]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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49.3.3 Major Capabilities/Options

Item	Feature	Subclause	Value/Comment	Status	Support
XSBI	XBSI compatibility interface	51, 49.1.5	Compatibility interface is supported	O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 49.1.5	Compatibility interface is supported	O	Yes [ ] No [ ]
MD	MDIO	45, 49.2.14	Registers and interface supported	O	Yes [ ] No [ ]
*WIS	Supports operation with a WIS	49.1.5		O.1	Yes [ ] No [ ]
PMA	Supports operation directly connected to a PMA	49.1.5		O.1	Yes [ ] No [ ]
*JTM	Supports test-pattern mode	49.2.2		PMA:M	Yes [ ] No [ ] N/A[ ]

49.3.4 PICS Proforma Tables for PCS, type 10GBASE-R

49.3.4.1 Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder implements the code as specified	49.2.13.2. 3 and 49.2.4		M	Yes [ ] No [ ]
C2	Decoder implements the code as specified	49.2.13.2. 349.2.4		M	Yes [ ] No [ ]
C3	IDLE control code insertion and deletion	49.2.4.7	Insertion or Deletion in groups of 4 /I/s	M	Yes [ ] No [ ]
C4	IDLE control code deletion	49.2.4.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	M	Yes [ ] No [ ]
C5	Sequence ordered_set deletion	49.2.4.10	Only one whole ordered_set of two consecutive sequence ordered sets may be deleted	M	Yes [ ] No [ ]

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49.3.4.2 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	49.2.6	Performs as shown in Figure 49–8	M	Yes [ ] No [ ]
S2	Descrambler	49.2.10	Performs as shown in Figure 49–10	M	Yes [ ] No [ ]

49.3.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Square wave and pseudo-random transmit test-pattern generators are implemented	49.2.8	Performs as in 49.2.8	JTM:M	Yes [ ] No [ ] N/A[ ]
JT2	Pseudo-random receive test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	JTM:M	Yes [ ] No [ ] N/A[ ]
JT3	Transmit and receive test-pattern modes can operate simultaneously	49.2.2		JTM:M	Yes [ ] No [ ] N/A[ ]
JT3	Reject transmit test-pattern mode when WIS is attached	49.2.8		JTM:O	Yes [ ] No [ ] N/A[ ]
JT4	Reject receive test-pattern mode when WIS is attached	49.2.12		JTM:O	Yes [ ] No [ ] N/A[ ]
*JT5	Support for PRBS31 test pattern	49.2.8		JTM:O	Yes [ ] No [ ] N/A[ ]
JT6	PRBS31 test-pattern generator is implemented	49.2.8	Performs as in 49.2.8	JT5:M	Yes [ ] No [ ] N/A[ ]
JT7	PRBS31 test-pattern checker is implemented	49.2.12	Performs as in 49.2.12	JT5:M	Yes [ ] No [ ] N/A[ ]

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49.3.5.1 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	49.2.7	Placement of bits into tx_data-group<15:0> as specified in 49.2.7	M	Yes [ ] No [ ]
B2	Receive bit order	49.2.9	Placement of bits from rx_data-group<15:0> into blocks as specified in 49.2.9	M	Yes [ ] No [ ]

49.3.6 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to PCS Management objects is provided	49.2.14		O	Yes [ ] No [ ]

49.3.6.1 State Machines

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Lock	49.2.13.3	Meets the requirements of Figure 49–12	M	Yes [ ] No [ ]
SM2	BER Monitor	49.2.13.3	Meets the requirements of Figure 49–13	M	Yes [ ] No [ ]
SM3	Transmit	49.2.13.3	Meets the requirements of Figure 49–14	M	Yes [ ] No [ ]
SM4	Receive	49.2.13.3	Meets the requirements of Figure 49–15	M	Yes [ ] No [ ]
SM5	PCS_R_Status	49.2.2	PCS_R_STATUS is FAIL in RX_INIT state; OK otherwise	M	Yes [ ] No [ ]

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49.3.6.2 WIS

Item	Feature	Subclause	Value/Comment	Status	Support
W1	Supports WIS_SIGNAL.request	49.2.2	PCS_R_STATUS is FAIL when in RX_INIT state	WIS:M	Yes [ ] No [ ] N/A[ ]

49.3.6.3 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports Loopback	49.2.14.4	Performs as in 49.2.14.4	M	Yes [ ] No [ ] N/A[ ]

49.3.6.4 Delay Constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	49.2.15	No more than 3584 BT for sum of transmit and receive path delays	M	Yes [ ] No [ ]

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50. WAN Interface Sublayer (WIS), type 10GBASE-W

50.1 Overview

The WAN Interface Sublayer (WIS) is an optional PHY sublayer that may be used to create a 10GBASE-W PHY that is data-rate and format compatible with the SONET STS-192c transmission format defined by ANSI, as well as the Synchronous Digital Hierarchy (SDH) VC-4-64c container specified by ITU. The purpose of the WIS is to allow 10GBASE-W equipment to generate Ethernet data streams that may be mapped directly to STS-192c or VC-4-64c streams at the PHY level, without requiring MAC or higher-layer processing. The WIS therefore specifies a subset of the logical frame formats in the SONET and SDH standards. In addition, the WIS constrains the effective data throughput at its service interface to the payload capacity of STS-192c / VC-4-64c, i.e., 9.58464 Gb/s. Multiplexed SONET/SDH formats are not supported.

The WIS does not render a 10GBASE-W PHY compliant with either SONET or SDH at any rate or format. A 10GBASE-W interface is not intended to interoperate directly with interfaces that comply with SONET or SDH standards, or other synchronous networks. Such interoperation would require full conformance to the optical, electrical, and logical requirements specified by SONET or SDH, and is outside the scope and intent of this standard. Operation over electrically multiplexed payloads of a transmission network is outside the scope of this standard.

From the perspective of the 10 Gb/s MAC layer, a 10GBASE-W PHY does not appear different (in either the functions or service interface) from a PHY without a WIS, with the exception of sustained data rate. However, a 10GBASE-W interface may interoperate only with another 10GBASE-W interface.

50.1.1 Scope

This clause specifies the functions, features, services, and protocol of the WIS. The WIS may be used with any of the PCS, PMA, and PMD sublayers that are defined for 10GBASE-W, as shown in Figure 50–1, it is placed between the PCS and PMA sublayers within the 10GBASE-W PHY. The WIS is common to all members of the family of 10GBASE-W WAN-compatible PHY implementations. There are currently three embodiments within this family: 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

The definition of the WIS is based on the subset of signaling rates and data formats standardized by ANSI T1.416-1999, which in turn is based on ANSI T1.105-1995. The WIS maps the encoded Ethernet data received (transmitted) from (to) the PCS into a frame structure that has the same format as that defined by T1.416-1999, implementing a minimal number of the standard SONET overhead fields and functions. The WIS does not adhere to the electrical and optical aspects of SONET specified by T1.416-1999, as it is intended to be used with PHYs that conform to the corresponding parameters defined by the 10GBASE-W standard.

The WIS shall meet all requirements of ANSI T1.416-1999 except those that are specifically excluded by this clause. The following sections of ANSI T1.416-1999 are excluded in their entirety:

a) Section 5 (Jitter)
b) Section 6 (Synchronization)
c) Section 7.2.2 (VT1.5 rate—Electrical Interface)
d) Section 7.4.2 (VT1.5 rate)
e) Section 7.6 (Performance and failure alarm monitoring)
f) Section 7.7 (Performance monitoring functions)
g) Annex A (SONET VT1.5 Line Interface Common Criteria)
h) Annex B (SONET maintenance signals for the NI)
i) Annex C (Receiver jitter tolerance and transfer)

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For convenience and clarity of explanation, this clause employs the notational conventions, nomenclature, and acronyms of SONET as defined by ANSI T1.416-1999. This should not, however, be taken as implying that the WIS excludes compatibility with ITU-defined SDH rates and formats.

50.1.2 Objectives

The following are the objectives for the WIS:

a) To support the full duplex mode of operation of the Ethernet MAC
b) To support the PCS, PMA and PMD sublayers defined for 10GBASE-W
c) To provide a 9.95328 Gb/s effective data rate at the service interface presented by the PMA sublayer, conforming with the requirements of SONET STS-192c and SDH VC-4-64c frame rates
d) To implement the framing, scrambling, and defect/anomaly detection to allow minimal compatibility with the requirements of both SONET and SDH transmission networks
e) To preserve the full duplex behavior and BER objectives of the PCS and PMD sublayers with which it may be used

NOTE—This clause will always use the term "WIS frames" when referring to the SONET-compatible frame format that is generated and terminated by the WIS, in order to distinguish such frames from those generated and terminated by the MAC. The WIS has no involvement with, or visibility into, the MAC framing processes. The "WIS frames" handled by the WIS are not propagated to higher layers via the WIS service interface; they are only exchanged between WIS peer entities on either side of a point-to-point link, and are unobservable and have no meaning outside WIS entities.

50.1.3 Relationship to other sublayers

Figure 50–1 depicts the relationships among the WIS (shown shaded), the 10 Gb/s MAC and Reconciliation Sublayers, the 10GBASE-R PCS and PMA, the ISO/IEC 8802-2 LLC, and the ISO/IEC Open System Interconnection (OSI) reference model.

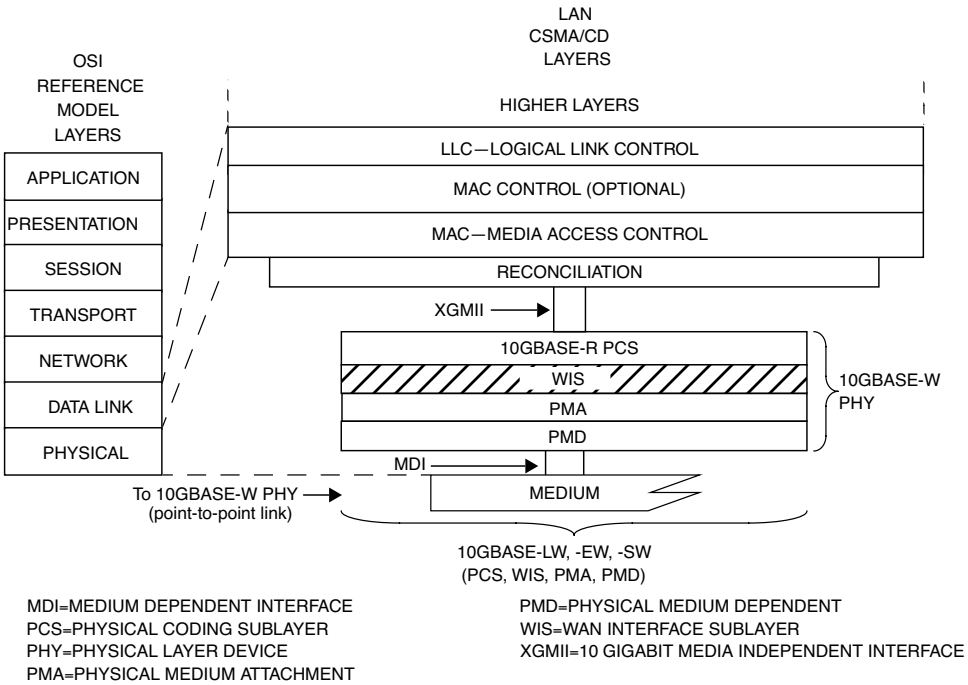


Figure 50–1—WIS relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

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50.1.4 Summary of functions

The following provides a summary of the principal functions implemented by the WIS.

In the transmit direction (i.e., when transferring data from the PCS to the PMA), the WIS performs the following functions:

a) Mapping of data-units received from the PCS via the WIS Service Interface to the payload capacity of the Synchronous Payload Envelope (SPE) defined for STS-192c
b) Addition of Path Overhead and fixed stuff octets to generate the actual SPE
c) Creation of frames consisting of Line Overhead and Section Overhead octets plus the SPE, and the generation and insertion of Section, Line, and Path Bit Interleaved Parity (BIP)
d) Scrambling of the generated WIS frames
e) Transmission of these frames to the PMA sublayer via the PMA Service Interface

In the receive direction, the functions performed by the WIS include the following:

a) Reception of data from the PMA sublayer via the PMA Service Interface
b) Delineation of octet boundaries as well as STS-192c frame boundaries within the unaligned data stream from the PMA
c) Descrambling of the payload and overhead fields within the incoming frames
d) Processing of the pointer field within the Line Overhead, and delineation of the boundaries of the Synchronous Payload Envelopes (SPE) within the received WIS frames
e) Generation and checking of Bit Interleaved Parity (BIP) within the Section, Line, and Path Overheads
f) Removal of Line, Section, and Path Overhead columns, as well as fixed stuff columns, in order to extract the actual payload field
g) Handling of errors and exception conditions detected within the incoming WIS frame stream, and reporting these errors to Layer Management
h) Mapping of octets extracted from the payload capacity of the incoming SPE to data-units that are passed to the PCS via the WIS Service Interface

50.1.5 Sublayer interfaces

A WIS Service Interface is provided to allow the WIS to transfer information to and from the 10GBASE-R PCS, which is the sole WIS client. An abstract service model is used to define the operation of this interface. In addition, the WIS utilizes the service interface provided by the PMA sublayer to transfer information to and from the PMA. This standard defines these interfaces in terms of bits, octets, data-units and signals; however, implementers may choose other data-path widths and other control mechanisms for implementation convenience, provided that the logical models of the service interfaces are adhered to.

NOTE—The PMA service interface may be optionally instantiated as an actual physical interface, referred to as the XSBI; in this case, the WIS must also implement the client portion of the XSBI, as defined in 51.4, and conform to its data-path widths and control mechanisms.

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50.1.6 Functional block diagram

Figure 50–2 provides a functional block diagram of the WIS.

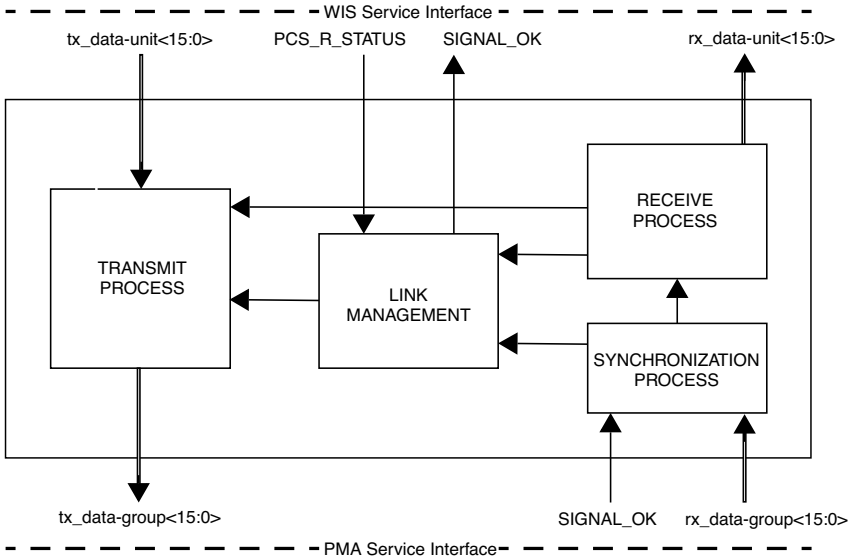


Figure 50–2—Functional block diagram

50.1.7 Notational conventions

The state diagrams within the body of this clause follow the notations and conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2.

The Path, Line, and Section Overhead fields handled by the WIS are referenced using the standard terminology given in Section 4.2 of ANSI T1.416-1999. Nomenclature relating to SONET Defects and Anomalies that must be processed by the WIS, as well as other definitions and abbreviations required by this clause, are defined by Section 3 of ANSI T1.416-1999.

The labeling and transmission order of bits within an octet is different between the SONET/SDH and Ethernet protocol families. SONET numbers bits within an octet from 1 to 8 inclusive, with the bit labeled 1 being the most-significant bit (MSB) and the bit labeled 8 being the least-significant bit (LSB); when serialized, bits are transmitted in order from MSB to LSB (i.e., the bit numbered 1 is transmitted first and the bit numbered 8 is transmitted last). The Ethernet numbering scheme, on the other hand, normally numbers bits from 0 to 7 inclusive, with bit 0 being the LSB and bit 7 being the MSB; bits are transmitted from LSB to MSB. This clause employs the SONET numbering scheme throughout, with the exception of the WIS service interface, which utilizes the Ethernet numbering scheme. Special provisions are made when mapping payload data into the WIS frame (see 50.3.1.1 and 50.3.1.2) to ensure that the reversed transmission order does not impact the properties of the Ethernet FCS.

50.2 WIS Service Interface

The WIS Service Interface is provided to allow the 10GBASE-R PCS to transfer information to and from the WIS. These services are defined in an abstract manner and do not imply any particular implementation. The WIS Service Interface supports the exchange of data-units between PCS entities on either side of a 10GBASE-W link using request and indicate primitives. Data-units are mapped into WIS frames by the WIS and passed to the PMA, and vice versa.

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The following primitives are defined within the WIS Service Interface:

WIS_UNITDATA.request(tx_data-unit<15:0>)
WIS_UNITDATA.indicate(rx_data-unit<15:0>)
WIS_SIGNAL.request(PCS_R_STATUS)
WIS_SIGNAL.indicate(SIGNAL_OK)

50.2.1 WIS_UNITDATA.request

This primitive defines the transfer of data, in the form of constant-width data-units, from the PCS to the WIS. The data supplied via WIS_UNITDATA.request is mapped by the WIS Transmit process into the payload capacity of the outgoing WIS frame stream.

50.2.1.1 Semantics of the service primitive

WIS_UNITDATA.request(tx_data-unit<15:0>)

The data conveyed by WIS_UNITDATA.request is a 16-bit vector representing a single data-unit which has been prepared for transmission by the 10GBASE-R PCS Transmit process. The element tx_data-unit<0> shall be interpreted as the least significant bit of the vector, and tx_data-unit<7:0> shall be interpreted as the least significant octet of the vector. The least significant octet of the vector is assumed to be generated first by the PCS; when the WIS transfers the provided data to the PMA, it is mapped such that the least significant octet is also transmitted first.

50.2.1.2 When generated

The 10GBASE-R PCS sends tx_data-unit<15:0> to the WIS at a nominal rate of 599.04 Mtransfers/s, corresponding to the STS-192c payload rate of 9.58464 Gb/s.

NOTE—The mapping of a constant-rate data stream into the payload capacity of a SONET-compatible SPE may require buffering in order to absorb the effects of periodically inserting overhead fields. In addition, the WIS and PCS may require some form of clock synchronization between the data-unit generation process and the normal SONET framing process. Both of these mechanisms are considered to be implementation-specific and outside the scope of this standard.

50.2.1.3 Effect of receipt

Upon receipt of this primitive, the WIS Transmit process maps the data conveyed by the tx_data-unit<15:0> parameter into the payload of the transmitted WIS frame stream, adds overhead octets as necessary, scrambles the data, and transfers the result to the PMA via one or more PMA_UNITDATA.request primitives.

50.2.2 WIS_UNITDATA.indicate

This primitive defines the transfer of received data, in the form of constant-width data-units, from the WIS to the PCS. WIS_UNITDATA.indicate is generated by the WIS Receive process in response to WIS frame data received from the PMA.

50.2.2.1 Semantics of the service primitive

WIS_UNITDATA.indicate(rx_data-unit<15:0>)

The rx_data-unit<15:0> parameter is a 16-bit vector that represents the data-unit transferred by the WIS to the 10GBASE-R PCS. The element rx_data-unit<0> shall be interpreted as the least significant bit of the vector, and rx_data-unit<7:0> shall be interpreted as the least significant octet of the vector. The least signif-

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icant octet of the vector is assumed to be processed first by the PCS; when the WIS obtains the data from the PMA, it is mapped such that the least significant octet was also received first.

50.2.2.2 When generated

The WIS sends one rx_data-unit<15:0> to the 10GBASE-R PCS whenever it has delineated exactly 16 bits of valid payload information from the incoming data stream received from the PMA sublayer. The nominal rate of generation of the WIS_UNITDATA.indicate primitive is 599.04 Mtransfers/s, as governed by the recovered bit clock and the reduction in data rate imposed by the removal and discard of overhead fields from the incoming WIS frame stream. This corresponds to the STS-192c payload rate of 9.58464 Gb/s.

NOTE—The removal of overhead fields creates variations in data rate that may have to be removed by suitable buffering before data are transferred to the PCS. These buffering and rate adaptation mechanisms are implementation dependent and outside the scope of this standard.

50.2.2.3 Effect of receipt

The effect of receipt of this primitive by the WIS client is unspecified by the WIS.

50.2.3 WIS_SIGNAL.request

This primitive is sent by the 10GBASE-R PCS to the WIS to indicate when the PCS has acquired or lost frame delineation, i.e., synchronization with respect to the code-words present in the received data transferred from the WIS to the PCS.

50.2.3.1 Semantics of the service primitive

WIS_SIGNAL.request(PCS_R_STATUS)

The PCS_R_STATUS parameter can take one of two values: OK or FAIL. A value of OK denotes that the PCS is successfully delineating valid code-words from the incoming data stream transferred to it by the WIS via the WIS_UNITDATA.indicate primitive. A value of FAIL denotes that errors have been detected by the PCS that prevent synchronization to these code-words.

50.2.3.2 When generated

The 10GBASE-R PCS generates the WIS_SIGNAL.request primitive to the WIS whenever there is a change in the value of the PCS_R_STATUS parameter.

50.2.3.3 Effect of receipt

The receipt of this primitive causes the WIS to identify the presence or absence of a Loss of Code-group Delineation condition, and to report this condition to the remote WIS entity via an LCD-P defect indication, as described in 50.3.5.3.

50.2.4 WIS_SIGNAL.indicate

This primitive is sent by the WIS to the PCS to indicate the status of the Receive process. WIS_SIGNAL.indicate is generated by the WIS Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

50.2.4.1 Semantics of the service primitive

WIS_SIGNAL.indicate(SIGNAL_OK)

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The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the WIS Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer, and this payload information is being presented to the PCS via the WIS_UNITDATA.indicate primitive. A value of FAIL denotes that errors have been detected by the Receive process that prevent valid data from being presented to the PCS, as described in 50.3.5; in this case the WIS_UNITDATA.indicate primitive and its associated rx_data-unit<15:0> parameter are meaningless.

50.2.4.2 When generated

The WIS generates the WIS_SIGNAL.indicate primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter.

50.2.4.3 Effect of receipt

The effect of receipt of this primitive by the WIS client is unspecified by the WIS.

50.3 Functions within the WIS

As shown in Figure 50–2, the WIS comprises the WIS Transmit and WIS Receive processes for 10GBASE-W, together with a Synchronization process and a Link Management function. Figure 50–3 depicts a conceptual view of the functions within each of the Transmit and Receive processes. Note that the figure does not show the interfaces to the Link Management function.

The WIS Transmit process accepts fixed-width tx_data-units from the PCS via the WIS Service Interface, and maps them into the payload capacity of the transmitted WIS frame stream. Fixed stuff octets are added, together with a set of Path Overhead octets, to create a Synchronous Payload Envelope (SPE). Line and Section Overhead octets are combined with the SPE and then scrambled using a frame-synchronous scrambler to produce the final transmitted WIS frame. The WIS continuously generates one SONET-compatible WIS frame, comprising overhead fields, fixed stuff and payload, every 125 microseconds. No gaps are present between WIS frames. The data produced by the Transmit process, depicted as tx_data-group<15:0> in Figure 50–2, are passed to the PMA via the PMA Service Interface.

The WIS Synchronization process accepts data from the PMA (via the PMA Service Interface, depicted as rx_data-group<15:0> in Figure 50–2) and performs an alignment operation to delineate both octet and frame boundaries within the received data stream. Aligned and framed data are passed to the WIS Receive process (depicted as sync_bits<15:0> in Figure 50–3), where Section and Line Overhead octets are extracted from the WIS frames and processed after de-scrambling the frame data. The payload pointer within the Line Overhead is used to delineate the start and end of the received SPE, and the Path Overhead is extracted from the SPE and processed. Finally, the fixed stuff is removed from the SPE as well, and the resulting data stream is conveyed to the PCS via the WIS Service Interface. Severe errors detected by the Synchronization and Receive processes (e.g., loss of WIS frame synchronization) cause a WIS_SIGNAL.indicate primitive to be sent to the PCS with a parameter of FAIL (see 50.2.4).

The WIS Link Management function implements the management registers defined in 45.2.2. These registers allow the local Station Management entity to control and monitor the operational status of the WIS Transmit and Receive processes. In addition, SONET Defects and Anomalies detected during the processing of the incoming data are sent to the management registers for reporting.

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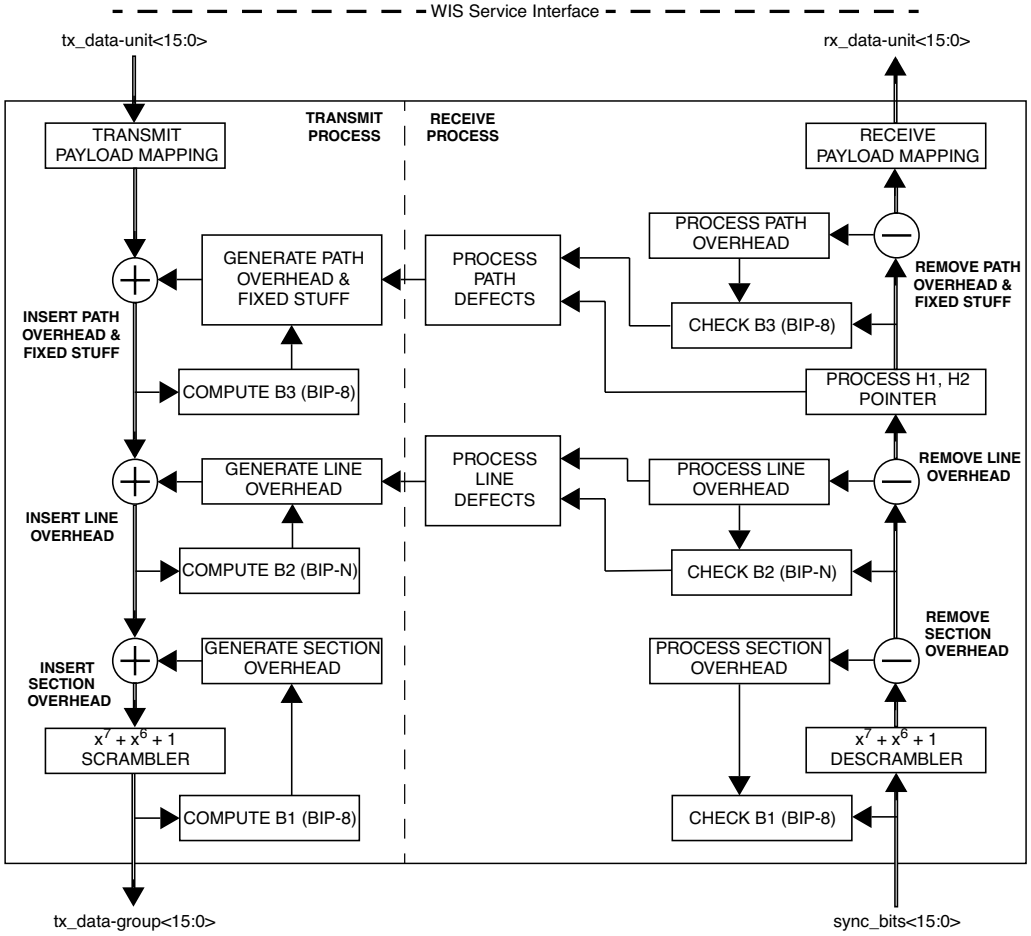


Figure 50–3—WIS Transmit and Receive processes

50.3.1 Payload mapping and data-unit delineation

The WIS maps the tx_data-unit<15:0> and rx_data-unit<15:0> parameters that are transferred via its service interface to/from the payload capacity of a standard STS-192c Synchronous Payload Envelope (SPE) structure. This structure is shown in Figure 50–4 for informative purposes. It is represented as a two-dimensional array with 9 rows and 16 704 columns, each row consisting of one octet of Path Overhead (added and removed as per 50.3.2.1 and 50.3.2.4), 63 octets of fixed stuff, and 16 640 octets of actual payload capacity.

The total payload capacity of the SPE comprises 149 760 octets (per WIS frame). As depicted in Figure 50–4, the octets of the payload capacity are numbered from left to right, starting at 0 (zero). The transmission order is also from left to right, i.e., lower-numbered octets are transmitted before higher-numbered octets.

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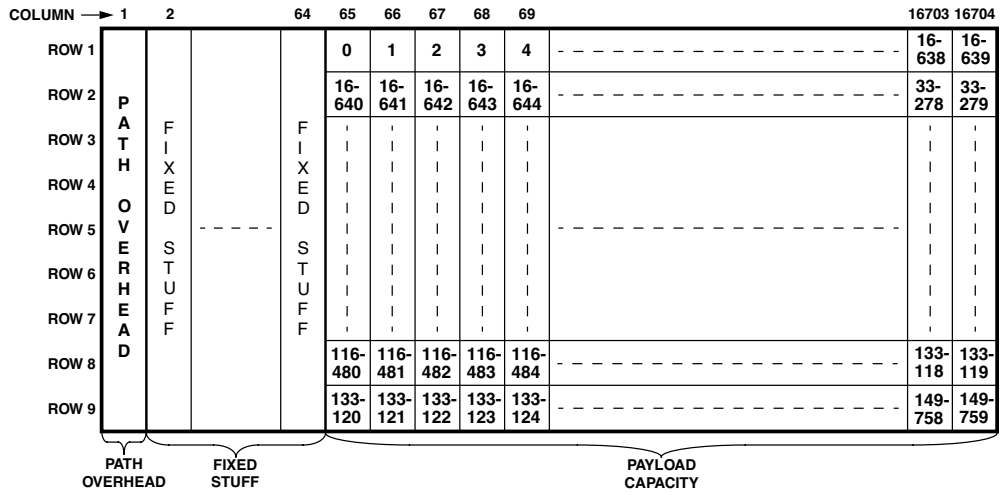


Figure 50–4—Structure of Synchronous Payload Envelope (informative)

50.3.1.1 Transmit payload mapping

The WIS Transmit function accepts a continuous stream of data-units from the PCS, conveyed by the tx_data-unit<15:0> parameter of the WIS_UNITDATA.request primitive of the WIS Service Interface. These data units shall be mapped to the SPE payload capacity and passed to the frame generation process described in 50.3.2 for insertion of the fixed stuff and Path Overhead columns. For each data-unit, tx_data-unit<7:0> shall be mapped to a lower-numbered (even) octet in the SPE payload capacity, and tx_data-unit<15:8> shall be mapped to the next higher-numbered (odd) octet.

A bit relabeling function is performed to map the bit numbering and ordering conventions followed by the WIS Service Interface to those implemented by the Transmit process (which follows the bit numbering and ordering conventions of SONET/SDH). The relabeling function shall be performed as shown in Figure 50–5. Bit 0 of tx_data-unit<15:0> is renumbered as bit 1 of the lower-numbered (even) octet within the SONET SPE, bit 15 of tx_data-unit<15:0> is renumbered as bit 8 of the higher-numbered octet within the SONET SPE, and the rest of the bits are renumbered in corresponding sequence.

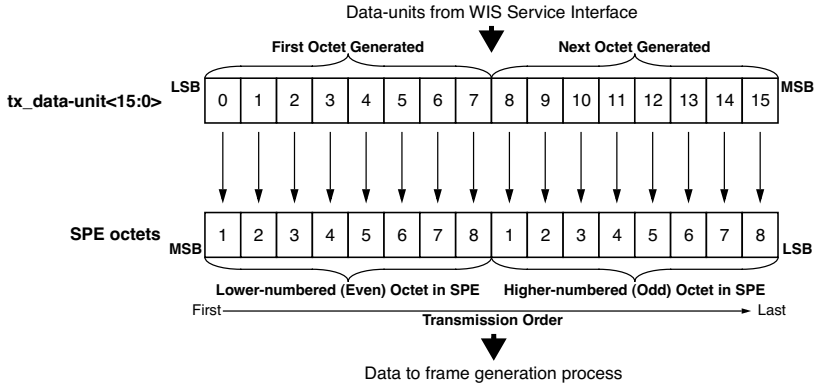


Figure 50–5—Transmit bit relabeling function

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NOTE—The transmit bit relabeling function is required because SONET transmission order is from MSB to LSB (i.e., bit 1 to bit 8 of each octet, in the SONET numbering convention) while the Ethernet transmission order is from LSB to MSB (i.e., bit 0 to bit 7 of each octet, in the Ethernet numbering convention). It is necessary to maintain the expected transmission order of Ethernet in order to preserve the error detection properties of the Ethernet FCS. Therefore, the renumbering scheme causes the payload portion of the SPE to be transmitted from LSB to MSB with reference to incoming data accepted from the WIS Service Interface, but the Path, Line, and Section Overhead octets are transmitted from MSB to LSB as required by SONET.

50.3.1.2 Receive payload mapping

The WIS Receive function accepts a continuous stream of octets from the frame reception process described in 50.3.2, corresponding to the payload capacity of the SPE as illustrated in Figure 50–4. It shall map the octets in the SPE payload capacity to a continuous stream of data-units that are supplied to the PCS via the rx_data-unit<15:0> parameter of the WIS_UNITDATA.indicate primitive of the WIS Service Interface. Within each data-unit, rx_data-unit<7:0> shall be mapped to a lower-numbered (even) octet in the SPE payload capacity, and rx_data-unit<15:8> shall be mapped to the next higher-numbered (odd) octet.

A bit relabeling function is performed to map the bit numbering and ordering conventions followed by the Receive process (which follows the bit numbering and ordering conventions of SONET/SDH) to those required by the WIS Service Interface. The relabeling function shall be performed as shown in Figure 50–6. Bit 1 of the lower-numbered (even) octet within the received SONET SPE is renumbered as bit 0 of rx_data-unit<15:0> at the WIS Service Interface, bit 8 of the higher-numbered octet within the SONET SPE is renumbered as bit 15 of rx_data-unit<15:0>, and the rest of the bits are renumbered in corresponding sequence.

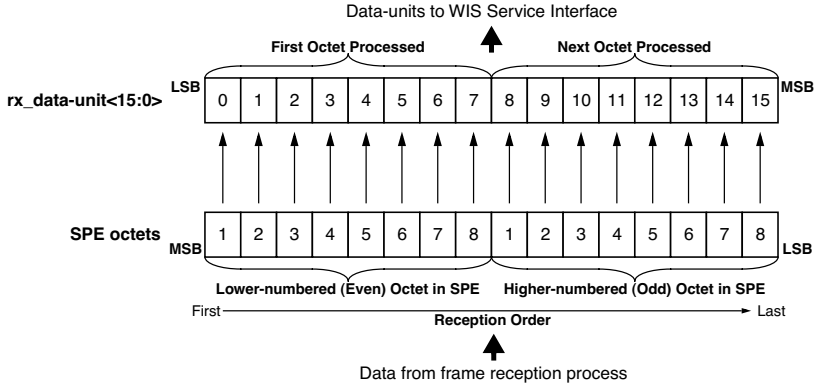


Figure 50–6—Receive bit relabeling function

NOTE—The receive bit relabeling function is required for the same reasons as the transmit bit relabeling function described in Section 50.3.1.1, i.e., to preserve the error detection properties of the Ethernet FCS in the face of the different transmission order required by SONET framing.

50.3.2 WIS frame generation

As part of the Transmit process, the WIS encapsulates the payload generated by the payload mapping function within a series of WIS frames. The Receive process performs the reverse operation, extracting payload from the incoming WIS frame stream and submitting it to the payload mapping function. SONET compatibility in the WIS follows ANSI T1.416-1999, with the exception of the superseding specifications in this document.

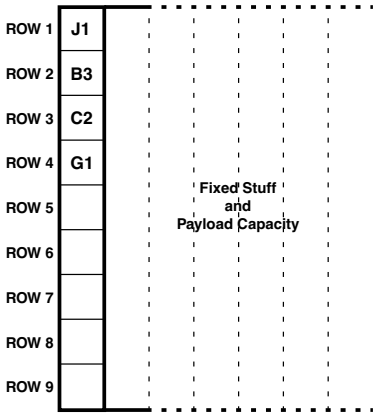
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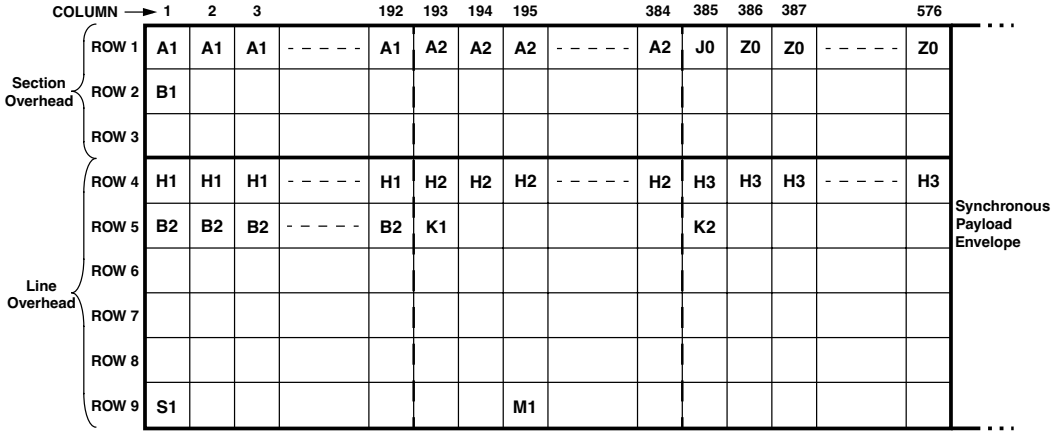
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Frame generation in both the transmit and receive directions is performed in three stages. Figure 50–3 illustrates the sequence of stages. The relevant octets in the Path Overhead portion of the frame are shown in Figure 50–7, and Figure 50–8 illustrates the Section and Line Overhead generated by the WIS.



NOTE—The Path Overhead comprises 9 octets in total. Only 4 octets are defined for the WIS. Octets that are undefined and unused by the WIS are indicated as blank boxes in this figure.

Figure 50–7—Structure of Path Overhead Generated by WIS (informative)



NOTE—The Section and Line Overhead comprise 5184 octets in total (576 x 9). Only 1349 octets are defined for the WIS. Octets that are undefined and unused by the WIS are indicated as blank boxes in this figure.

Figure 50–8—Structure of Section and Line Overhead Generated by WIS (informative)

NOTE—Figures 50–8 and 50–7 are provided for informative purposes only. In the event of any discrepancy observed between the figures and the normative portions of ANSI T1.416-1999, the latter shall take precedence.

50.3.2.1 Transmit Path Overhead insertion

The WIS Transmit process shall insert Path Overhead fields as defined in Section 4.2 of ANSI T1.416-1999, and specified in Table 50–1 of this standard. For the fields where the "Coding" column of Table 50–1 contains "per T1.416," the field is inserted according to the specifications of ANSI T1.416-1999. For the fields where the "Coding" column of Table 50–1 contains a specific value or "see text," this document supersedes the corresponding values in Table 1, "SONET overhead at NIs" in the ANSI document.

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Table 50–1—STS Path Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
B3	STS Path error monitoring (Path BIP-8)	supported	per T1.416
C2	STS Path signal label	specified value	00011010
F2	Path user channel	unsupported	00000000
G1	Path status	supported	per T1.416
H4	Multiframe indicator	unsupported	00000000
J1	STS Path trace	specified value	see text
N1	Tandem connection maintenance/Path data channel	unsupported	00000000
Z3-Z4	Reserved for Path growth	unsupported	00000000
NOTE—SONET/SDH and 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

NOTE—The value assigned to the C2 octet corresponds to the provisional Path signal label value assigned for 10 Gigabit Ethernet. The fixed stuff octets that follow the Path Overhead column in the SPE are transmitted as 00000000 and are not checked on receive.

The J1 octet shall transport a 16-octet continuously repeating Path Trace Message that is formatted as defined by Section 5 and Annex A of ANSI T1.269-2000. Each successive octet of the Path Trace Message, starting from the first, is placed in the J1 octet of a successive WIS frame; after all 16 octets have been transmitted in this way, the process repeats. The Station Management entity may modify the Path Trace Message being transmitted via the Link Management register facilities provided in 50.3.11.1. If the Station Management entity is not currently transmitting a Path Trace Message, a default Path Trace Message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000 shall be transmitted.

NOTE—The bit representation of the header octet of the default Path Trace Message is 10001001 (89 hexadecimal). This value is provided here for informational purposes only; ANSI T1.269-2000 shall take precedence in case of any discrepancy.

50.3.2.2 Transmit Line Overhead insertion

The WIS Transmit process shall insert Line Overhead fields as defined in Section 4.2 of ANSI T1.416-1999, and specified in Table 50–2 of this document. For the fields where the "Coding" column of Table 50–2 contains "per T1.416," the field is inserted according to the specifications of ANSI T1.416-1999. For the fields where the "Coding" column of Table 50–2 contains a specific value or "see text," this document supersedes the corresponding values in Table 1, "SONET overhead at NIs" in the ANSI document. In addition, Line Overhead octets not listed in the latter table shall be set to 00000000 by the Transmit process.

The H1 and H2 pointer octets shall be set by the Transmit process, in accordance with the pointer mechanism defined by ANSI T1.416-1999, to indicate a constant pointer value of 522 decimal, and shall also indicate a concatenated payload.

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The K1 octet shall be set to 00000000 by the Transmit process. In addition, bits 1 to 5 inclusive of the K2 octet shall be set to 00000 binary. Bits 6 through 8 inclusive shall either transport an RDI-L encoding, as defined by Section 7.4.1 of ANSI T1.416-1999, or be set to 000 binary. No other encodings of the K2 octet are allowed to be transmitted by the WIS Transmit process.

Table 50–2—Line Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
B2	Line error monitoring (Line BIP-1536)	supported	per T1.416
D4-D12	Line Data Communications Channel (DCC)	unsupported	00000000
E2	Orderwire	unsupported	00000000
H1-H2	Pointer	specified value	See text.
H3	Pointer action	specified value	00000000
K1, K2	Automatic protection switch (APS) channel and Line Remote Defect Identifier (RDI-L)	specified value	See text.
M0	STS-1 Line Remote Error Indication (REI)	unsupported	00000000
M1	STS-*N* Line Remote Error Indication (REI)	supported	per T1.416
S1	Synchronization messaging	unsupported	00001111
Z1	Reserved for Line growth	unsupported	00000000
Z2	Reserved for Line growth	unsupported	00000000
NOTE—SONET/SDH and IEEE 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

NOTE—The setting of the constant portions of the K1 and K2 octets denotes that the interface containing the WIS is acting as a working channel. The RDI-L encoding within the K2 octet serves to support the fault processing specified in 50.3.2.5. The setting of the S1 octet signifies that the transmit clock should not be used for synchronization. The bit numbering for these octets follows the SONET convention, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.

50.3.2.3 Transmit Section Overhead insertion

The WIS Transmit process shall insert Section Overhead fields as defined in Section 4.2 of ANSI T1.416-1999, and specified in Table 50–3 of this document. For the fields where the "Coding" column of Table 50–3 contains "per T1.416," the field is inserted according to the specifications of ANSI T1.416-1999. For the fields where the "Coding" column of Table 50–3 contains a specific value or "see text," this document supersedes the corresponding values in Table 1, "SONET overhead at NIs" in the ANSI document. In addition, Section Overhead octets not listed in the latter table shall be set to 00000000 by the Transmit process.

The J0 octet shall transport a 16-octet continuously repeating Section Trace Message that is formatted as defined by Section 5 and Annex A of ANSI T1.269-2000. Each successive octet of the Section Trace Message, starting from the first, is placed in the J0 octet of a successive WIS frame; after all 16 octets have been

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transmitted in this way, the process repeats. The Station Management entity may modify the Section Trace Message being transmitted via the Link Management register facilities provided in 50.3.11.1. If the Station Management entity is not currently transmitting a Section Trace Message, a default Section Trace Message consisting of 15 octets of zeros and a header octet formatted according to Section 5 of ANSI T1.269-2000 shall be transmitted.

NOTE—The bit representation of the header octet of the default Section Trace Message is 10001001 (89 hexadecimal). This value is provided here for informational purposes only; ANSI T1.269-2000 shall take precedence in case of any discrepancy.

Table 50–3—Section Overhead

Overhead octet	Function	Usage	Coding (bits 1..8)
A1	Frame alignment	supported	per T1.416
A2	Frame alignment	supported	per T1.416
B1	Section error monitoring (Section BIP-8)	supported	per T1.416
D1-D3	Section Data Communications Channel (DCC)	unsupported	00000000
E1	Orderwire	unsupported	00000000
F1	Section User Channel	unsupported	00000000
J0	Section trace	specified value	See text
Z0	Reserved for Section growth	unsupported	11001100
NOTE 1—The bit representations of the octet values assigned to A1 and A2 are 11110110 (F6 hexadecimal) and 00101000 (28 hexadecimal), respectively. These values are provided here for informational purposes only. ANSI T1.416-1999 shall take precedence in case of any discrepancy. NOTE 2—SONET/SDH and IEEE 802.3 differ in bit ordering conventions. The values in this table follow SONET bit ordering, in which bit index values range from 1 to 8, from left to right, and bit 8 is the least significant bit.			

50.3.2.4 Receive Path, Line, and Section Overhead extraction

The WIS Receive process shall extract Path, Line and Section Overhead fields as defined in Section 4.2 of ANSI T1.416-1999, and specified in Tables 50–1, 50–2, and 50–3 of this document. For the fields where the "Coding" columns of Tables 50–1, 50–2, and 50–3 contain "per T1.416," the field is extracted according to the specifications of ANSI T1.416-1999. For the fields where the "Coding" columns contain a specific value or "see text," this document supersedes the corresponding values in Table 1, "SONET overhead at NIs" in the ANSI document. Overhead octets marked as unsupported in Tables 50–1, 50–2, and 50–3 shall be ignored by the Receive process. In addition, overhead octets not listed in Table 1, "SONET overhead at NIs" in ANSI T1.416-1999 shall also be ignored by the Receive process.

The J0 octet in the received WIS frames shall be interpreted as transporting a 16-octet continuously repeating Section Trace Message. This Section Trace Message is extracted from the incoming WIS frame stream and passed to the Station Management entity via dedicated registers within the WIS MDIO register space (50.3.11.1). The WIS Receive process is not required to delineate Section Trace Message boundaries or process them in any way.

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Extraction of valid Section Trace Message data shall begin after the WIS Receive process has successfully synchronized to the incoming WIS frame stream. Each successive J0 octet received thereafter is placed in a successive octet of the WIS J0 receive register set, until 16 J0 octets have been received, after which the process repeats from the first octet of the register set. As the incoming Section Trace Message is 16 octets in size, the contents of the WIS J0 receive register set will remain static as long as the same message is being received. Extraction of Section Trace Messages in this fashion is performed continuously as long as valid WIS frames are being received. The WIS Receive process is not required to interpret or process the extracted message in any way.

The J1 octet in the received WIS frames shall be interpreted as transporting a 16-octet continuously repeating Path Trace Message. This Path Trace Message is extracted from the incoming WIS frame stream and passed to the Station Management entity via dedicated registers within the WIS MDIO register space (50.3.11.1). The WIS Receive process is not required to delineate Path Trace Message boundaries or process them in any way.

Extraction of valid Path Trace Message data shall begin after the WIS Receive process has successfully synchronized to the incoming WIS frame stream. Each successive J1 octet received thereafter is placed in a successive octet of the WIS J1 receive register set, until 16 J1 octets have been received, after which the process repeats from the first octet of the register set. As the incoming Path Trace Message is 16 octets in size, the contents of the WIS J1 receive register set will remain static as long as the same message is being received. Extraction of Path Trace Messages in this fashion is performed continuously as long as valid WIS frames are being received. The WIS Receive process is not required to interpret or process the extracted message in any way.

Bits 6 through 8, inclusive, of the K2 octet in the received Line Overhead shall be interpreted by the WIS Receive process as carrying the Line Alarm Indication Signal (AIS-L) or Line Remote Defect Indication (RDI-L) signals (see 50.3.2.5). All other encodings of these bits shall be ignored by the Receive process.

NOTE—Values of overhead fields encoded by the Transmit process within a WIS entity at one end of a link may be changed by intervening Line and Section equipment before it reaches the peer WIS entity at the other end of the link. In particular, the H1, H2, and H3 fields may take on values different from those originally encoded. The receive process must be able to handle these situations in accordance with ANSI T1.416-1999, and therefore must contain a pointer interpreter function compliant with the latter. Bits 5 and 6 of the H1 octet are ignored by the receiver.

50.3.2.5 Fault processing

Defects and anomalies detected by the Receive process are classified as defined in Section 7.1 of ANSI T1.416-1999. Section, Line, and Path defects and anomalies listed in Table 50–4 of this document shall be detected and processed as defined by Sections 7.3, 7.4.1, and 7.5 of ANSI T1.416-1999. Defects and anomalies not listed in Table 50–4 are ignored.

NOTE—The description of the LOP-P defect in Section 7.5 of ANSI T1.416-1999 is in error, and deviates from the underlying definitive reference, which is ANSI T1.231-1997. The reader should therefore consult section 8.1.2.4.1 of ANSI T1.231-1997 for the specification of the LOP-P defect until ANSI T1.416-1999 has been corrected.

The WIS shall additionally support the PLM-P (Path Label Mismatch) and LCD-P (Loss of Code-group Delineation) defects. The detection and reporting of the PLM-P defect follows Section 7.5 of ANSI T1.416-1999. The LCD-P defect shares the same coding value and reporting method as the PLM-P defect, but is detected according to 50.3.5.3.

The Receive process shall detect a Loss Of Signal (LOS) defect as defined by Section 7.2.1 of ANSI T1.416-1999 without using any services provided by the PMA or PMD sublayers for this purpose. The parameters *T* and *T'* in Section 7.2.1 of ANSI T1.416-1999 shall both be set to a value ranging between 2.3 and 100 microseconds.

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Table 50–4—WIS supported Near end events and Far end reports

	Physical media	Section		Line		Path	
	Defect	Anomaly	Defect	Anomaly	Defect	Anomaly	Defect
Near end	LOS	BIP-N(S)	SEF/LOF	BIP-N(L)	AIS-L	BIP-N(P)	LOP-P AIS-P
Far end	N/A	N/A	N/A	REI-L	RDI-L	REI-P	ERDI-P

NOTE—Section 7.2.2, "VT1.5 rate–Electrical Interface," Section 7.4.2 "VT1.5 Rate," Section 7.6, "Performance and Failure Monitoring," and Section 7.7 "Performance Monitoring Functions" of ANSI T1.416-1999 are not applicable and are not supported. Also, the AIS-L defect is only processed and reported by the WIS Receive process; it is never transmitted by the WIS Transmit process. In addition, a PLM-P defect is indistinguishable from an LCD-P defect at the far end, as the two defects are coded identically in the outgoing WIS frame stream; however, as both defects indicate a payload defect, this is of no consequence. They are detected separately for local reporting purposes.

50.3.3 Scrambling

The WIS shall implement a frame-synchronous scrambler within the Transmit process, and shall also implement a frame-synchronous descrambler within the Receive processes, both of sequence length 127 and as specified by Section 10.3 of ANSI T1.105-1995. The use of the scrambler is intended to provide for DC balance (i.e., an equal number of 1's and 0's on average) and for sufficient transition density within the bit stream transmitted on the medium. The scrambler is run over each bit of the entire WIS frame prior to transmission to the PMA, with the exception of all the A1, A2, J0 and Z0 octets (576 octets in total, per WIS frame), which are transmitted and received unscrambled. The scrambling function implemented by the Transmit process is identical in logical construction to the corresponding descrambling function in the Receive process.

Figure 50–9 illustrates the functional diagram of the frame-synchronous scrambler, in bit-serial form.

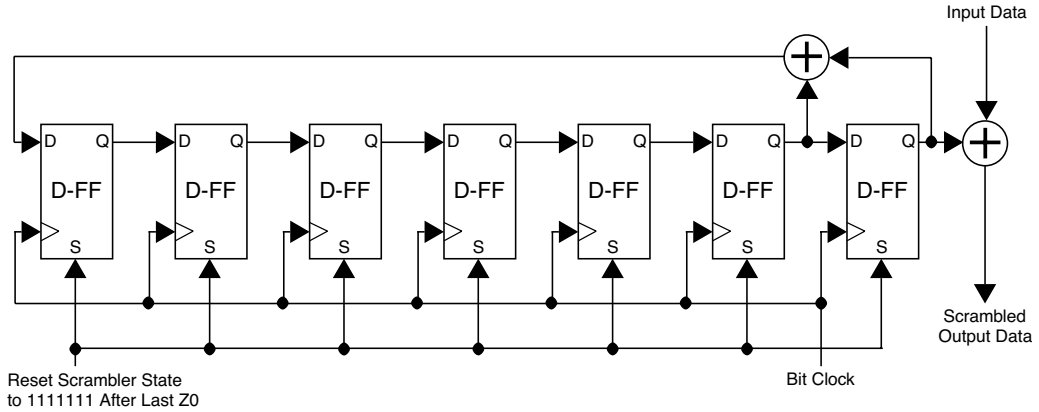


Figure 50–9—Scrambling function (informative)

NOTE—The diagram in Figure 50–9 is intended for reference and informative purposes only. Implementations may select any conforming means of realizing the scrambler function described herein. If a discrepancy is observed between the descriptions and diagram in this section and ANSI T1.105-1995, the latter takes precedence.

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50.3.3.1 Scrambler polynomial

The scrambler polynomial used follows that specified in Section 10.3 of ANSI T1.105-1995. The scrambler state is reset, as specified in the latter, to binary 1111111 prior to processing the octet immediately following the last Z0 octet in every WIS frame.

50.3.3.2 Scrambler bit ordering

The bit ordering considerations for the frame-synchronous scrambler in the WIS are illustrated in Figure 50–10. As shown, the scrambler in effect processes the transmitted (received) WIS frame octet-by-octet, starting with the most-significant (leftmost) bit of the first octet following the last Z0 octet in the WIS frame. The scrambler then proceeds bit-by-bit until the least-significant bit has been reached, after which it continues with the most-significant bit of the second octet.

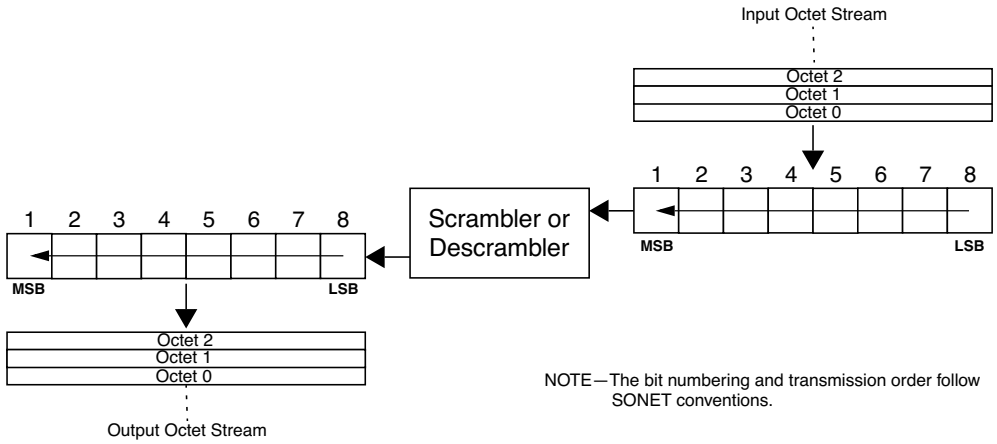


Figure 50–10—Scrambler bit ordering (informative)

NOTE—The above description and diagram are informative.

50.3.4 Octet and frame delineation

The WIS is required to delineate both octet and WIS frame boundaries within the stream of received data words presented by the PMA via its service interface to the Receive process. Delineation of these boundaries and alignment of the received data are done prior to performing the descrambling function (as opposed to the SPE delineation process, which is done after descrambling the received data). The delineation process employs the A1 and A2 octets in the Section Overhead portion of the received WIS frame stream, and searches for valid transitions between A1 and A2 patterns.

The WIS shall implement the synchronization process described in 50.4.2 to delineate octet and WIS frame boundaries. Failure to achieve or maintain synchronization shall result in Severely Errored Frame (SEF) or Loss Of Frame (LOF) Defects being indicated as described in 50.3.2.5.

50.3.5 Error propagation

The WIS Receive and Synchronization processes detect specific errors during reception that prevent delineation of valid data from the incoming WIS frame stream, and cause these errors to be propagated to the 10GBASE-R PCS. Error propagation shall be performed by generating a WIS_SIGNAL.indicate primitive with the SIGNAL_OK parameter set to FAIL, regardless of the actual contents of any payload that may be extracted from the incoming WIS frame stream. A subsequent WIS_SIGNAL.indicate primitive with

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SIGNAL_OK set to OK shall be issued only after the WIS determines that none of these particular errors exist, subject to the error propagation timing below.

In addition, the WIS Receive process detects a Loss of Code-group Delineation condition, and report it to the far end WIS as an LCD-P defect by the method described in 50.3.2.5.

50.3.5.1 Propagated errors

The following conditions shall be detected as errors and reported to the 10GBASE-R PCS via the mechanism of 50.3.5:

a) The Synchronization process is not in the SYNC state, as defined by the state machine of 50.4.2.
b) A PLM-P defect is detected (50.3.2.5).
c) An AIS-P defect is detected (50.3.2.5).
d) An LOP-P defect is detected (50.3.2.5).

NOTE—The error propagation mechanism may also be used to indicate when the WIS is unable to supply valid data to the PCS for any other reason, such as an internal error, a reset condition, or when disabled via layer management. This is considered to be implementation specific and is outside the scope of this clause.

50.3.5.2 Error propagation timing

Propagation of errors to the PCS according to the mechanism of 50.3.5 begins as soon as possible after the detection of one or more of the error conditions specified in 50.3.5.1. Error propagation shall terminate, and valid data shall be transferred to the PCS, within 125 microseconds of the removal of all of the error conditions in 50.3.5.1.

50.3.5.3 Loss of Code-group Delineation

The WIS Receive process shall identify a Loss of Code-group Delineation condition if the 10GBASE-R PCS signals, via the WIS_SIGNAL.request(PCS_R_STATUS) primitive of the WIS Service Interface (50.2.3), that synchronization has been lost and valid code-groups are no longer being delineated from the received payload stream being passed to the PCS. The LCD-P defect shall be reported to the far end WIS if this condition persists continuously for at least 3 ms. In addition, re-initialization of the WIS shall cause the LCD-P defect to be reported, with the same timing specification, until the PCS signals that valid code-groups are being delineated. The 3 millisecond timer is not allowed to start timing the false condition of WIS_SIGNAL.request(PCS_R_STATUS) while WIS_SIGNAL.indicate is false, thus inhibiting the reporting of the LCD-P defect whenever the WIS is unable to supply valid received data to the PCS.

The WIS Receive process shall identify the absence of a Loss of Code-group Delineation condition if the 10GBASE-R PCS signals, also via the WIS_SIGNAL.request(PCS_R_STATUS) primitive, that synchronization has been regained and valid code-groups are being delineated from the received payload stream. Reporting of the LCD-P defect to the far end WIS shall terminate if the condition has been absent continuously for at least 1 ms.

50.3.6 Mapping between WIS and PMA

As a client of the PMA sublayer, the WIS utilizes the PMA Service Interface to transfer transmitted (received) data-groups to (from) the PMA sublayer. The PMA Service Interface is described in 51.2. Note that the PMA Service Interface may optionally be instantiated as a physical interface, referred to as the XSBI. In this case, the WIS must implement the client portion of the XSBI, including the logical formats and protocols as well as the physical signals and electrical timing, conforming with the XSBI specification in 51.4.

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The WIS Transmit process transfers a continuous stream of 16-bit data-groups, containing the transmit WIS frame data generated as in 50.3.2, to the PMA via the PMA Service Interface. The octet boundaries in the transmit WIS frames shall be aligned to those in the data-groups, and the first data-group transmitted shall contain the first two octets in the Section Overhead (i.e., the first two A1 octets, as illustrated in Figure 50–8). Figure 50–11 depicts the transmission order required from the PMA for the data-groups. Each 16-bit data-group shall be transmitted from left to right, with lower-numbered bits being transmitted before higher-numbered bits. The data-groups themselves shall be transmitted in the sequence in which they are presented to the PMA by the WIS Transmit process.

A similar ordering is required during the reception process, as shown in Figure 50–11. Successive received bits shall be ordered from left to right in the 16-bit data-groups that are passed to the WIS (i.e., lower-numbered bits are received before higher-numbered bits), and the data-groups must be presented in the sequence in which they were received. The PMA sublayer is not required to align the data being presented to the WIS on any boundary.

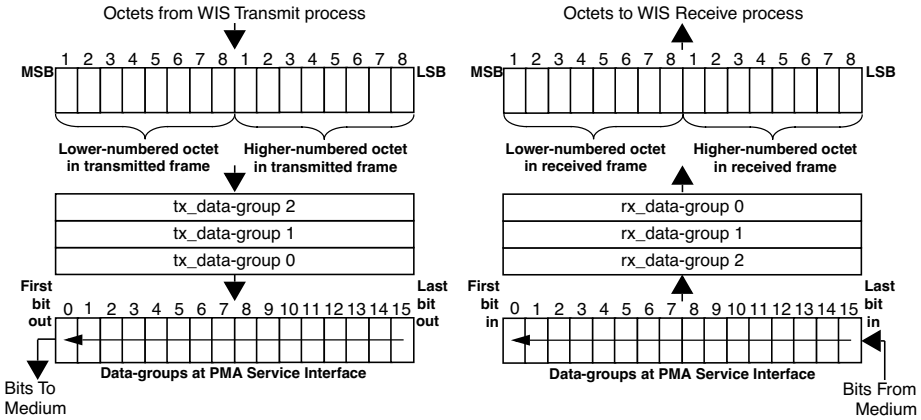


Figure 50–11—Transmission order

The WIS also utilizes the PMA_SIGNAL.indicate primitive received from the PMA sublayer to determine when the PMA is unable to provide valid data to the WIS via its service interface. This primitive is used to unlock the state machine implemented in the Synchronization process and force it to re-synchronize, as described in 50.4.

NOTE—The PMA_SIGNAL.indicate primitive received from the PMA differs from the Loss of Signal (LOS) defect described in 50.3.2.5. LOS is a status condition that is reported to Layer Management for error monitoring purposes, but otherwise does not affect the internal functioning of the Receive Process or the Synchronization Process. The PMA primitive, however, acts as a control signal that directly affects all parts of the WIS receive functionality.

50.3.7 WIS data delay constraints

The sum of the transmit and receive data delays for any implementation of the WIS shall not exceed 14336 BT. Transmit data delay is measured from the input of a given unit of data by the PCS at the WIS service interface to the presentation of the same unit of data by the WIS to the PMA at the PMA service interface. Receive data delay is measured from the input of a given unit of data by the PMA at the PMA service interface to the presentation of the same unit of data by the WIS to the PCS at the WIS service interface. The time required to insert or process any necessary overhead or stuff octets must be included as part of the data delay incurred by the WIS. No constraint is placed on the individual values of the transmit and receive data delays for a given implementation, provided their sum falls within the above limit.

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50.3.8 WIS test-pattern generator and checker

The WIS shall incorporate a test-pattern generator and a test-pattern checker to permit in-circuit testing using test patterns. These serial test patterns allow the 10GBASE-W PMA and PMD sublayers to be tested for compliance while in a system environment. Three patterns have been defined for testing: a fixed square wave pattern, an optional PRBS31 pattern, and a framed mixed frequency pattern. The patterns may be implemented at a bit or frame level and may be used for transmitter testing. The test-pattern checker has the ability to synchronize to the PRBS31 and mixed-frequency test patterns and report bit errors detected within the payload to the Station Management entity. The test-pattern checker is not required to synchronize to or analyze the square wave pattern.

The transmit and receive portions of the WIS can be placed in test-pattern mode separately by means of the WIS Transmit test-pattern enable and WIS Receive test-pattern enable control bits supported within its management registers (see 45.2.2.6). In addition, the three different types of transmit test pattern (square-wave, PRBS31 and mixed frequency) may be selected by means of the test-pattern control bits. (The test-pattern receiver only operates in PRBS31 and mixed-frequency test-pattern modes.) Errors detected during PRBS31 testing are recorded and provided to the Station Management entity via the 10G WIS test-pattern error counter register (45.2.2.8), while errors detected during mixed frequency testing are recorded and provided to the Station Management entity via the 10G WIS Section BIP Error Count register (45.2.2.17), the 10G WIS Line BIP Errors register (45.2.2.15), and the 10G WIS Path Block Error Count register (45.2.2.16). The WIS Service Interface is inoperative when either the WIS Transmit process or WIS Receive process is placed in test-pattern mode, regardless of the type of test pattern selected.

When the WIS transmit function is operating in test-pattern mode, the test-pattern generator produces a continuous test pattern that is sent 16 bits at a time to the underlying PMA sublayer via PMA_UNITDATA.request primitives. When the WIS receive function is operating in test-pattern mode, 16-bit data-groups received from the underlying PMA sublayer by means of PMA_UNITDATA.indicate primitives are accepted and processed by the test-pattern checker.

50.3.8.1 Square wave test pattern

In the square-wave test-pattern mode, the WIS Transmit process is disabled or otherwise prevented from processing data, and a square wave as defined in 52.9.1 shall be continuously transferred to the PMA via the PMA Service Interface. No checking is performed on the 16-bit data-groups received from the PMA sublayer in this mode.

50.3.8.2 PRBS31 test pattern

The PRBS31 test-pattern mode is optional. When the transmit portion of the WIS is operating in PRBS31 test-pattern mode, the WIS Transmit process is disabled or otherwise prevented from processing data, and the output of a Pseudo-Random Bit Sequence (PRBS) generator shall be continuously transferred to the PMA via the PMA Service Interface. The PRBS generator functionality is described in 49.2.8.

When the receive portion of the WIS is operating in PRBS31 test-pattern mode, the WIS Receive Process is disabled or otherwise prevented from processing data, and a PRBS pattern checker shall check the bits received from the PMA via the PMA Service Interface. The PRBS checker functionality is described in 49.2.12.

If no errors have occurred, the test-pattern error signal from the pattern checker will be zero. An isolated bit error will cause the test-pattern error signal to be asserted three times; once when it is received and once when it is at each tap. The 10G WIS test-pattern error counter register (45.2.2.8) shall be incremented whenever the test-pattern error signal is asserted.

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50.3.8.3 Mixed-frequency test pattern

In the mixed-frequency test-pattern mode, the WIS Transmit process is utilized to generate a transmitted test pattern (if activated by the WIS Transmit test-pattern enable control bit) and the WIS Synchronization and Receive processes are utilized to check a received test pattern (if separately activated by the WIS Receive test-pattern enable control bit). Figure 50–12 provides a functional diagram of the WIS when operating in this mode.

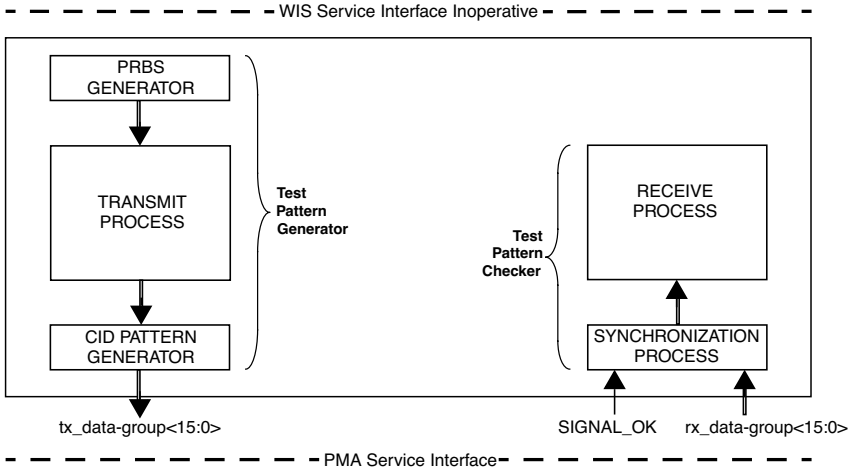


Figure 50–12—Mixed-frequency test-pattern mode operation

The mixed-frequency test pattern has the Test Signal Structure (TSS) described by 50.3.8.3.1, with a Consecutive Identical Digit (CID) pattern described by 50.3.8.3.2. The pattern is generated using the WIS Transmit process, with the SPE payload capacity being filled with a (2^{23}– 1) pseudo-random bit sequence (PRBS) as defined by ITU-T Recommendation O.150, 1996, in conjunction with a CID pattern generator that overwrites the last nine Z0 octets of the Section Overhead (see Figure 50–8) with an alternating pattern. The WIS Synchronization and Receive processes operate normally. Bit errors in the received pattern shall be detected by means of the Section, Line and Path BIP checking facilities, and reported to Station Management by means of the corresponding error counters within the MDIO register space (see 50.3.8).

NOTE—The PRBS is substituted for the payload data that would normally be sent to the WIS Transmit process from the 10GBASE-R PCS. The CID pattern is selected to stress the lock range of the receiver circuitry, and is placed in the Z0 octet locations as these are not scrambled by the WIS Transmit process. The values of the Z0 octets are required to be ignored by the WIS Receive process (see 50.3.2.4), and therefore no change to the latter is necessary.

The WIS Transmit, Receive and Synchronization processes shall function as described in 50.3.2, 50.3.3, and 50.3.4, with the exception that fault processing as per 50.3.2.5 and error propagation as per 50.3.5 shall not be carried out, the Z0 octets shall be overwritten with a CID pattern as specified, and the data output by the PRBS generator shall be used as the data source in place of the PCS.

NOTE—The implied re-use of the WIS Transmit, Receive, and Synchronization processes to implement the mixed-frequency test pattern functions is not a required attribute; implementations may select any physical means of realizing the test-pattern transmit and receive functionality, provided that the external behavior of the WIS conforms to that described herein.

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50.3.8.3.1 Test Signal Structure (TSS)

The TSS is defined as a repeating set of two consecutive WIS frames, i.e., 300 672 octets in length, and shall be formatted as shown in Figure 50–13. The first frame of the set has a CID pattern set to all zeros, and the second frame has the pattern set to all ones. The PRBS generator shall be reset to all ones prior to the start of the payload capacity of each SPE contained within the TSS. In addition, the PRBS generator output shall be placed directly into the payload capacity of the first SPE, and inverted before being placed into the second SPE. Both WIS frames include the Section, Line, and Path Overhead and fixed stuff as normally generated by the Transmit process. All overhead octets except for J1 shall be set to their default values.

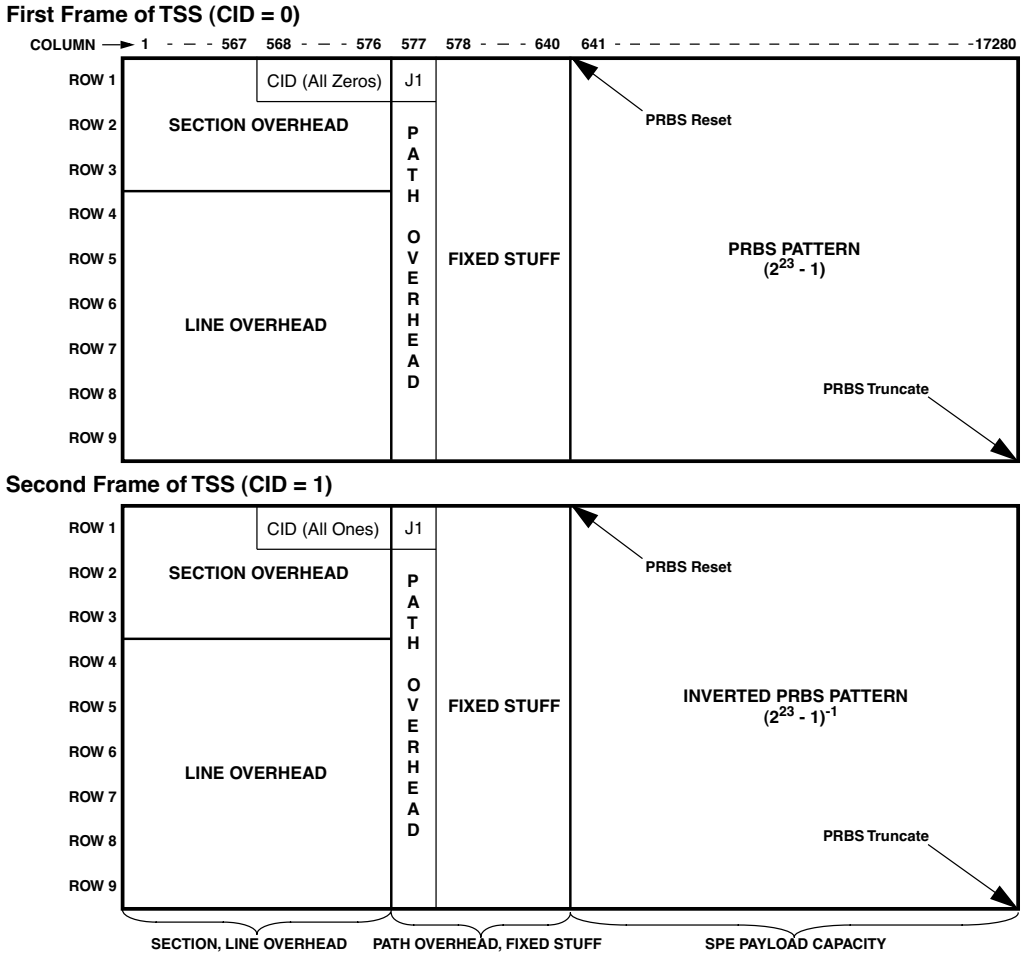


Figure 50–13—Test Signal Structure

As shown in Figure 50–13, the J1 octet of the Path Overhead is located immediately following the last octet of the CID pattern, and is hence the point of maximum stress with respect to the 10GBASE-W PMA and PMD. The J1 octet may therefore be programmed via the 10G WIS J1 transmit Registers (45.2.2.12) to a fixed value which, after scrambling, provides optimal stress to the PMA/PMD transmitter and receiver. If not used for this purpose, it shall be set to a value of 89 hexadecimal in both the WIS frames comprising the TSS.

NOTE—Standard SONET test equipment may not support the WIS test-pattern generator and checker as the PRBS is re-synchronized on every WIS frame, instead of the free-running PRBS described in ITU-T Recommendation O.172, 1999. Pattern-based bit error ratio testers will require 300 672 bytes of pattern storage memory to hold the complete TSS.

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50.3.8.3.2 Continuous Identical Digits

The CID pattern shall comprise 9 octets (72 bits) overwriting the Z0 octets at the end of the first row of the Section Overhead, as shown in Figure 50–14. The pattern shall alternate in consecutive WIS frames; in the first frame of the TSS, the pattern consists of 72 bits of zeros, and in the second frame the pattern consists of 72 bits of all ones.

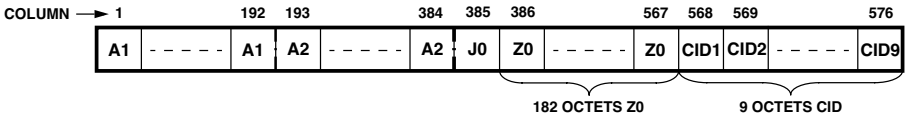


Figure 50–14—CID pattern structure

As the CID pattern is not scrambled, the string of ones (and, alternately, the string of zeros) forming the pattern produce transition-free areas within the TSS that stress the transmitter and receiver. Errors (eye closure at the transmitter or sampling errors at the receiver) are reflected as bit errors that are detected and reported via the BIP checking functionality in the WIS.

50.3.9 Loopback

The WIS is placed in Loopback mode when the Loopback bit in the WIS Control 1 register (45.2.2.1.2) is set to a logic one. In this mode, the WIS shall accept data on the transmit path from the 10GBASE-R PCS and return it on the receive path to the 10GBASE-R PCS. In addition, the WIS shall transmit a constant pattern to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer. The pattern output to the PMA transmit path at this time shall consist of a sequence of 8 logic zero bits and 8 logic one bits, forming the 16-bit word 00-FF hexadecimal. No SONET overhead or fixed stuff is output to the PMA at this time.

NOTE—The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that this signal path encompass as much of the WIS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data, while ensuring that remote entities do not interpret this test data as valid information. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

50.3.10 Link status

The WIS link status, as reported in the Link status bit of the WIS status 1 register (see 45.2.2.2.2), shall be set to down if a PLM-P, AIS-P, or LOP-P defect is detected (50.3.5.1), an AIS-L defect is detected (50.3.2.5), or the Synchronization process is not in the SYNC state (50.4.2). Otherwise, the WIS link status is set to up.

50.3.11 Management interface

The WIS supports a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the WIS is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.2, which are implemented by the Link Management function depicted in Figure 50–2.

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50.3.11.1 Management registers

The WIS management interface function shall utilize the following dedicated management registers:

a) WIS Control 1 register (Register 0)
b) WIS status 1 register (Register 1)
c) WIS Control 2 register (Register 7)
d) WIS status 2 register (Register 8)
e) WIS test-pattern error counter register (Register 9)
f) WIS Status 3 register (Register 33)
g) WIS J0 transmit register (Registers 64, 65, 66, 67, 68, 69, 70, 71)
h) WIS J0 receive register (Registers 72, 73, 74, 75, 76, 77, 78, 79)
i) WIS Far End Path Block Error Count register (Register 37)
j) WIS J1 transmit register (Registers 39, 40, 41, 42, 43, 44, 45, 46)
k) WIS J1 receive register (Registers 47, 48, 49, 50, 51, 52, 53, 54)
l) WIS Far End Line BIP Errors register pair (Registers 55 and 56)
m) WIS Line BIP Errors register pair (Register 57 and 58)
n) WIS Path Block Error Count register (Register 59)
o) WIS Section BIP Error Count register (Register 60)

These registers are implemented within the Device address space assigned to the WIS. The details of the register bit allocations and general usage are given in Clause 45. Note that Clause 45 also specifies several registers and register bits that are generic to every Device (e.g., Speed Ability and Identifier registers), and these are not covered by this clause.

NOTE—Clause 45 provides for additional vendor-specific registers within the address space assigned to the WIS. The presence, format, and function of these registers are implementation specific.

If the optional MDIO interface and associated register set are not implemented for the WIS, then equivalent capabilities are required to be provided.

50.3.11.2 WIS managed object class

The WIS Managed Object Class is defined in 30.8.1.

50.3.11.3 Management support objects

The following counters shall be provided to facilitate support of the WIS managed object class. If an MDIO interface is provided for the WIS, these counters are accessed via the WIS Far End Line BIP Errors and WIS Line BIP Errors registers, as described in 45.2.2.14 and 45.2.2.15 respectively. If no MDIO interface is implemented, these counters are to be accessible by equivalent means.

Far End Line BIP Errors
: A 32-bit counter that is incremented by the number of Line BIP errors detected by the far-end WIS and reported via the M1 octet present in each received WIS frame (see 50.3.2.5). This counter has a maximum increment rate of 2 040 000 counts per second. The counter is cleared to zero when the WIS is reset, and wraps around to zero when it is incremented beyond the maximum count value. The contents of this counter are reflected in the WIS Far End Line BIP Errors register pair.

Line BIP Errors
: A 32-bit counter that is incremented by the number of Line BIP errors detected by the Receive process while processing each received WIS frame (see 50.3.2.5). This counter has a maximum increment rate of 12 288 000 counts per second. The counter is cleared to zero when the WIS is reset, and wraps around to zero when it is incremented beyond the maximum count value. The contents of this counter are reflected in the WIS Line BIP Errors register pair.

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50.4 Synchronization state diagram

The WIS Synchronization process shall implement the state diagrams specified in this subclause and meet the corresponding state diagram interface requirements, also specified here. Additional requirements to this state diagrams are made in 50.3.4. In the case of any ambiguity between the text and the state diagrams, the state diagrams shall take precedence.

The notation used in the state diagrams is described in 21.5, and the conventions for state diagram timers in 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented by 1.

50.4.1 State diagram variables

Variables of the form name<x:0> indicate arrays or vectors of bits; for such variables, "<x>" indexes an element or set of elements in the array or vector, where "x" may be as follows:

— Any integer or set of integers.
— Any variable that takes on integer values.

In the variable and function descriptions in 50.4.1.2 and 50.4.1.3, the parameters *f*, *i*, *j*, *k*, *m*, and *n* are implementation-specific. Maximum and minimum values for these parameters are specified in 50.4.3.

50.4.1.1 Constants

A1
: An octet value (bits 1:8) of 11110110 as assigned to the A1 framing character within the SONET Section Overhead, as specified in Table 1 of Section 4.2 of ANSI T1.416-1999. Used to obtain octet and WIS frame alignment.

A2
: An octet value (bits 1:8) of 00101000 as assigned to the A2 framing character within the SONET Section Overhead, as specified in Table 1 of Section 4.2 of ANSI T1.416-1999. Used to obtain octet and WIS frame alignment.

Hunt_Pattern
: A sequence of *i* consecutive A1 octets.

Presync_Pattern
: A sequence of *j* consecutive A1 octets, immediately followed by a sequence of *k* consecutive A2 octets.

Sync_Pattern
: A sequence of *f* consecutive A1 octets immediately followed by a sequence of *f* consecutive A2 octets.

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50.4.1.2 Variables

power_on

A condition that is true until such time as the power supply to the device containing the WIS has reached the operating region.

Values: FALSE; The device is completely powered and ready to operate.
TRUE; The device has not been completely powered.

reset

A Boolean variable that is true when a hardware reset has been applied to the WIS, and false otherwise.

Values: TRUE; A hardware reset is being applied.
FALSE; A hardware reset is not being applied.

signal_fail

A condition that is true whenever the underlying PMA sublayer indicates by means of the PMA_SIGNAL.indicate primitive that valid data are not being supplied to the WIS. Once set to TRUE, signal_fail remains set until the PMA sublayer explicitly indicates that valid data are being recovered and supplied to the WIS, after which it is set to FALSE.

Values: FALSE; A PMA_SIGNAL.indicate(SIGNAL_OK) primitive was received with SIGNAL_OK set to OK, indicating that the PMA has begun to provide valid data to the WIS Receive process.
TRUE; A PMA_SIGNAL.indicate(SIGNAL_OK) primitive was received with SIGNAL_OK set to FAIL, indicating that the PMA is unable to provide valid data to the WIS Receive process.

in_HUNT

Boolean variable, set by the Primary Synchronization state machine to indicate to the Interval Pattern Search state machine to indicate that it has entered, or returned to, the HUNT state.

Values: TRUE; The Primary Synchronization state machine is presently in the HUNT state.
FALSE; The Primary Synchronization state machine is not in the HUNT state.

sync_start

Boolean variable, set by the Primary Synchronization state machine to trigger the operation of the Interval Pattern Search state machine.

Values: TRUE; The Interval Pattern Search state machine should begin scanning for framing sequences.
FALSE; The Interval Pattern Search state machine should not begin scanning.

50.4.1.3 Functions

found_Hunt

For each bit input to the Synchronization process, this function indicates whether the Hunt_Pattern pattern has been detected in the bit string formed by concatenating the current bit with the (i * 8 – 1) consecutive previously input bits. If the number of bits previously input is less than (i * 8 – 1), this function outputs a FALSE value. Note that this function inspects its input on a bit-by-bit basis.

Values: TRUE; The (i * 8) bits examined so far, consisting of the current bit plus previously input bits, matches Hunt_Pattern.
FALSE; The pattern is not matched, or less than (i * 8) bits have been input so far.

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found_Presync
: For the last ($j + k$) sets of 8 bits (1 octet) input to the Synchronization process, this function indicates whether the Presync_Pattern pattern has been matched. If the number of octets previously input is less than ($j + k$), or the string match is still proceeding, this function outputs a WAIT value. Note that this function inspects its input on an octet-by-octet basis.

  Values: TRUE; The octets examined so far, consisting of the current octet plus previously input bits, matches Presync_Pattern.
  FALSE; The pattern is not matched.
  WAIT; Insufficient data has been received so far to complete the match or declare failure.

found_Sync
: For the last $2f$ sets of 8 bits (1 octet) input to the Synchronization process, this function indicates whether the Sync_Pattern pattern has been matched. If the number of octets previously input is less than $2f$, the function outputs a FALSE value. Note that this function inspects its input on an octet-by-octet basis.

  Values: TRUE; The octets examined so far, consisting of the current octet plus previously input octets, matches Sync_Pattern.
  FALSE; The pattern is not matched, or insufficient octets have been received so far.

50.4.1.4 Counters

good_sync_cnt
: Count of the number of consecutive candidate Sync_Pattern pattern locations that contain a valid Sync_Pattern pattern. This counter is controlled by the Interval Pattern Search state machine, and used to report the number of valid framing locations to the Primary Synchronization state machine.

bad_sync_cnt
: Count of the number of consecutive candidate Sync_Pattern pattern locations that have failed to contain a valid Sync_Pattern pattern. This counter is controlled by the Interval Pattern Search state machine, and used to report the number of mismatched framing locations to the Primary Synchronization state machine.

octet_cnt
: Count of octets input to the Synchronization process; always increments for every octet input. This counter is forced to zero in specific states of the Interval Pattern Search state machine, but for all other states it increments by 1 for each octet received. It is used to force the state machine to wait in a given state until a required number of octets have been received.

50.4.2 State diagram

The Primary Synchronization state diagram is depicted in Figure 50–15, and the Interval Pattern Search state diagram in Figure 50–16. The WIS shall implement the Synchronization process according to these state diagrams, including compliance with the associated state variables as specified in 50.4.1. The Synchronization process is responsible for detecting octet and WIS frame boundaries and also for determining whether the underlying receive channel is ready for operation. Failure to achieve synchronization, as indicated by the Synchronization state machine not being in the SYNC state, shall cause the WIS Receive process to suspend normal operation and propagate the error to the PCS as described in 50.3.5.

The function of the Primary Synchronization state machine is to track the four phases through which the Synchronization process must progress in order to achieve and maintain lock to the incoming frame stream. In the first phase, the state machine performs a bit-by-bit hunt over the input data for a string of A1 octets. Successful location of several A1 octets indicates both a candidate octet and a candidate frame boundary; this is validated by scanning for additional A1 octets followed immediately by another string of A2 octets,

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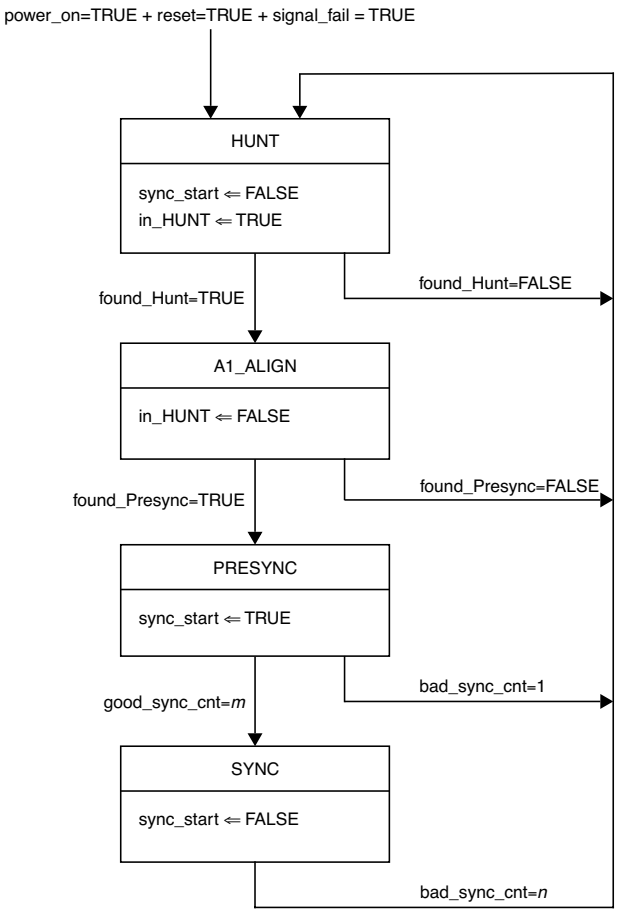


Figure 50–15—Primary Synchronization state diagram

which corresponds to the framing pattern present at the start of every WIS frame. The candidate frame boundary is now confirmed by searching for several consecutive such patterns, each separated by a frame size; if successful, frame lock is deemed to have been achieved. The state machine then remains in the frame lock state until a number of consecutive candidate pattern locations have failed to match the A1/A2 pattern. This behavior implements the necessary hysteresis required to reject transient bit errors.

The Interval Pattern Search state machine is activated when the Synchronization process has successfully located the first occurrence of the framing pattern, and performs the actual function of searching for subsequent framing patterns that are located 155520 octets apart, and counting failed and successful matches.

The functions fount_Hunt, found_Presync, and found_Sync implement bit and octet scanners that search through the incoming data stream for the respective data patterns that must be matched.

NOTE—Implementations may choose any conforming means of realizing the state diagram described herein, provided that the external behavior of the Synchronization process is unchanged.

50.4.3 Parameter values

Table 50–5 identifies the minimum and maximum values permissible for the parameters f, i, j, k, m, and n that are used in the preceding state diagram descriptions. Implementations shall set these parameters to values within the limits specified in the table.

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Table 50–5—Minimum and maximum parameter values

Parameters	Minimum values	Maximum values	Purpose
f	2	192	Controls width of Sync_Pattern pattern
i	1	192	Controls width of Hunt_Pattern pattern
j	16	190	Controls width of Presync_Pattern pattern
k	16	192	Controls width of Presync_Pattern pattern
m	4	8	Controls hysteresis for SYNC state entry
n	1	8	Controls hysteresis for SYNC state exit

NOTE—The ranges for the parameters stipulated in Table 50–5 are intended to provide the implementer with latitude in creating implementations of the Synchronization process. However, adherence to the stipulated minimum values for the parameters will result in an implementation that provides the minimum time-to-frame (5 WIS frame periods) and required bit error tolerance at the normal BER (10^{-12}).

50.5 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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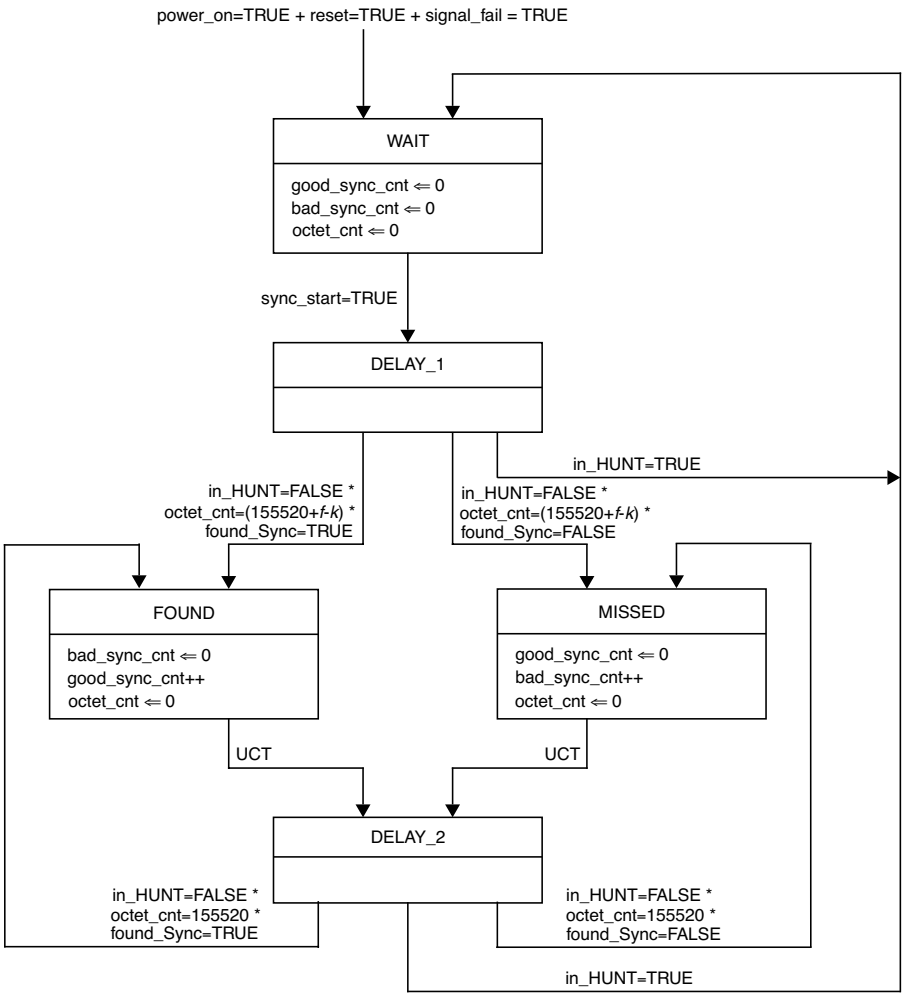


Figure 50–16—Interval Pattern Search state diagram

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50.6 Protocol Implementation Conformance Statement (PICS) proforma for Clause 50, WAN Interface Sublayer (WIS), type 10GBASE-W[14]

50.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 50, WAN Interface Sublayer, type 10GBASE-W, shall complete the following Protocol Implementation Conformation Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

50.6.2 Identification

50.6.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

50.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, WAN Interface Sublayer (WIS), type 10GBASE-W
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[14]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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50.6.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XSBI	XSBI compatibility interface	51, 50.3.6	Compatibility interface supported	O	Yes [ ] No [ ]
*MD	MDIO	50.3.11.1	Registers and interface supported	O	Yes [ ] No [ ]
*PRBS	PRBS31 Test-pattern mode	50.3.8.2	Registers and functionality supported	O	Yes [ ] No [ ]

50.6.4 PICS proforma tables for the WAN Interface Sublayer (WIS), type 10GBASE-W

50.6.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Meets requirements of ANSI T1.416-1999	50.1.1	Except as specifically excluded	M	
CC2	Precedence of ANSI T1.416-1999 and ANSI T1.269-2000 in case of discrepancies	50.3.2, 50.3.2.1, 50.3.2.3, 50.3.3	Unless specifically overridden by Clause 50.	M	
CC3	Environmental specifications	50.5		M	Yes [ ]

50.6.4.2 WIS transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
WT1	Bit significance of data-unit vector from 10GBASE-R PCS	50.2.1.1	Data-unit<0> is interpreted as the least-significant bit	M	Yes [ ]
WT2	Payload mapping of octets from data-units to SPE by Transmit process	50.3.1.1	Tx_data-unit<7:0> mapped to lower-numbered (even) octet and tx_data-unit<15:8> to next higher-numbered (odd) octet	M	Yes [ ]
WT3	Bit relabeling during transmit mapping	50.3.1.1	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WT4	Path Overhead generation	50.3.2.1		M	Yes [ ]
WT5	J1 octet in Path Overhead	50.3.2.1	Transports a 16-octet repeating Path Trace Message	M	Yes [ ]
WT6	Default Path Trace Message	50.3.2.1	Consists of 15 octets of zeros and a header octet	M	Yes [ ]
WT7	Line Overhead generation	50.3.2.2		M	Yes [ ]
WT8	Unspecified Line Overhead octets	50.3.2.2	Set to 00000000 binary if not specifically listed	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WT9	H1 and H2 octets in Line Overhead	50.3.2.2	Set to 522 decimal and also indicates concatenated payload	M	Yes [ ]
WT10	K1 octet in Line Overhead	50.3.2.2	Set to 00000000 binary	M	Yes [ ]
WT11	Bits 1 to 5 of K2 octet in Line Overhead	50.3.2.2	Set to 00000 binary	M	Yes [ ]
WT12	Bits 6 to 8 of K2 octet in Line Overhead	50.3.2.2	Set to either an RDI-L encoding, or 000 binary	M	Yes [ ]
WT13	Section Overhead generation	50.3.2.3		M	Yes [ ]
WT14	Unspecified Section Overhead octets	50.3.2.3	Set to 00000000 binary if not specifically listed	M	Yes [ ]
WT15	J0 octet in Section Overhead	50.3.2.3	Transports a 16-octet repeating Section Trace Message	M	Yes [ ]
WT16	Default Section Trace Message	50.3.2.3	Consists of 15 octets of zeros and a header octet	M	Yes [ ]
WT17	Frame scrambler	50.3.3		M	Yes [ ]
WT18	Octet ordering to PMA	50.3.6	First data-group transmitted contains the first two A1 octets	M	Yes [ ]
WT19	Bit ordering to PMA	50.3.6	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WT20	Data-group ordering to PMA	50.3.6		M	Yes [ ]
WT21	Transmit data delay constraint	50.3.7	Sum of transmit and receive data delays not to exceed 14336 BT	M	Yes [ ]

50.6.4.3 WIS receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
WR1	Bit significance of data-unit vector to 10GBASE-R PCS	50.2.2.1	Data-unit<0> is interpreted as the least-significant bit	M	Yes [ ]
WR2	Payload mapping of octets from SPE to data-units	50.3.1.2	Rx_data-unit<7:0> mapped from lower-numbered (even) octet and rx_data-unit<15:8> from next higher-numbered (odd) octet	M	Yes [ ]
WR3	Bit relabeling during receive mapping	50.3.1.2	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WR4	Section, Line, and Path Overhead extraction and processing	50.3.2.4		M	Yes [ ]
WR5	Unsupported overhead octets	50.3.2.4	Ignored if marked as unsupported in Tables 50–1, 50–2, and 50–3	M	Yes [ ]
WR6	Unlisted overhead octets	50.3.2.4	Ignored if not listed in Table 1 of ANSI T1.416-1999	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WR7	Interpretation of J1 octet in Path Overhead	50.3.2.4	Interpreted as carrying a 16-byte repeating Path Trace Message	M	Yes [ ]
WR8	Extraction of valid Path Trace Message data	50.3.2.4	After receiver accomplishes synchronization	M	Yes [ ]
WR9	Interpretation of bits 6 through 8 of K2 octet in Line Overhead	50.3.2.4	Interpreted as carrying AIS-L or RDI-L	M	Yes [ ]
WR10	Unsupported encodings of bits 6 through 8 of K2 octet in Line Overhead	50.3.2.4	Ignored by receiver	M	Yes [ ]
WR11	Interpretation of J0 octet in Path Overhead	50.3.2.4	Interpreted as carrying a 16-byte repeating Section Trace Message	M	Yes [ ]
WR12	Extraction of valid Section Trace Message data	50.3.2.4	After receiver accomplishes synchronization	M	Yes [ ]
WR13	Detection of Section, Line and Path Defects and Anomalies	50.3.2.5	Only Defects and Anomalies listed in Table 50–4 processed	M	Yes [ ]
WR14	Support for PLM-P and LCD-P defects	50.3.2.5		M	Yes [ ]
WR15	Detection of LOS defect	50.3.2.5	No services provided by the PMA or PMD are used	M	Yes [ ]
WR16	LOS defect detection parameters	50.3.2.5	Parameters *T* and *T'* between 2.3 and 100 microseconds	M	Yes [ ]
WR17	Frame descrambler	50.3.3		M	Yes [ ]
WR18	Bit, octet and data-group ordering from PMA	50.3.6	Ethernet FCS error detection properties to be maintained	M	Yes [ ]
WR19	Delineation of octet and WIS frame boundaries	50.3.4	According to Synchronization process	M	Yes [ ]
WR20	Reporting of errors on synchronization failure	50.3.4	SEF or LOF defects reported on synchronization failure	M	Yes [ ]
WR21	Receive data delay constraint	50.3.7	Sum of transmit and receive data delays not to exceed 14336 BT	M	Yes [ ]

50.6.4.4 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Synchronization state machine	50.4	Meets the requirements of Figures 50–15 and 50–16	M	Yes [ ]
SD2	Synchronization process	50.4.2		M	Yes [ ]
SD3	Receive process suspended upon failure to achieve synchronization	50.4.2		M	Yes [ ]
SD4	Synchronization parameters	50.4.3	Meets the requirements of Table 50–5	M	Yes [ ]

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50.6.4.5 Error notification

Item	Feature	Subclause	Value/Comment	Status	Support
EN1	Notification of fault presence to PCS	50.3.5	WIS_SIGNAL.indicate SIGNAL_OK set to FAIL	M	Yes [ ]
EN2	Removal of fault notification to PCS in the absence of faults	50.3.5	WIS_SIGNAL.indicate SIGNAL_OK set to OK	M	Yes [ ]
EN3	Faults notified to PCS	50.3.5.1	Detects and reports the following errors: Synchronization process not in SYNC state, PLM-P defect, AIS-P defect, and LOP-P defect	M	Yes [ ]
EN4	PCS fault notification timing	50.3.5.2	Error propagation terminates, and valid data transferred, within 125 microseconds after error conditions removed	M	Yes [ ]
EN5	Presence of Loss of Code-group Delineation condition	50.3.5.3	When indicated by the 10GBASE-R PCS	M	Yes [ ]
EN6	Reporting of Loss of Code-group Delineation presence	50.3.5.3	Reported only if condition persists for more than 3 ms	M	Yes [ ]
EN7	Reporting with respect to WIS re-initialization	50.3.5.3	Report Loss of Code-group Delineation on re-initialization	M	Yes [ ]
EN8	Absence of Loss of Code-group Delineation condition	50.3.5.3	When indicated by the 10GBASE-R PCS	M	Yes [ ]
EN9	Reporting of Loss of Code-group Delineation absence	50.3.5.3	Reported only if condition is absent for more than 1 ms	M	Yes [ ]

50.6.4.6 Management registers and functions

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Management registers	50.3.11.1	If management registers are not physically implemented, equivalent capabilities must be provided	MD:M	Yes [ ]
MR2	Management support objects	50.3.11.3	If management interface is not physically implemented, equivalent capabilities must be provided	MD:M	Yes [ ]
MR3	Loopback function	50.3.9	Data accepted on the transmit path from the 10GBASE-R PCS returned via the receive path	M	Yes [ ]
MR4	Data transmitted to PMA during loopback	50.3.9	The 16-bit pattern 00-FF hexadecimal must be transmitted	M	Yes [ ]
MR5	Data received from PMA during loopback	50.3.9	All data received from PMA during loopback must be ignored	M	Yes [ ]
MR6	WIS link status function	50.3.10	Set to up or down as defined	M	Yes [ ]

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50.6.4.7 WIS test-pattern generator and checker

Item	Feature	Subclause	Value/Comment	Status	Support
TP1	Test-pattern generator and checker	50.3.8	Separate generator and checker functionality for transmit and receive	M	Yes [ ]
TP2	Data pattern used in square-wave test-pattern mode	50.3.8.1	Data pattern as specified in 52.9.1	M	Yes [ ]
TP3	PRBS31 generator functionality	50.3.8.2		PRBS:M	Yes [ ]
TP4	PRBS31 checker functionality	50.3.8.2		PRBS:M	Yes [ ]
TP5	Bit error detection and reporting by PRBS31 checker	50.3.8.2	If management interface is not physically implemented, equivalent reporting capabilities must be provided	PRBS:M	Yes [ ]
TP6	Bit error detection in received mixed-frequency test pattern	50.3.8.3	Detection by Section, Line and Path BIP checking facilities	M	Yes [ ]
TP7	Functionality of WIS Transmit, Receive and Synchronization processed in mixed-frequency test-pattern mode	50.3.8.3	With the exceptions that fault processing and error propagation are not carried out, the Z0 octets are overwritten with CID pattern, and a PRBS used in place of the PCS data	M	Yes [ ]
TP8	Format of TSS	50.3.8.3.1		M	Yes [ ]
TP9	PRBS generator reset in TSS	50.3.8.3.1	Reset to all-ones prior to start of SPE	M	Yes [ ]
TP10	PRBS generator invert in TSS	50.3.8.3.1	Invert PRBS pattern in second SPE	M	Yes [ ]
TP11	Overhead octets in TSS	50.3.8.3.1	Set to defaults except for J1	M	Yes [ ]
TP12	Default value for J1 in TSS	50.3.8.3.1	Set to 89 hexadecimal if not used for providing stress	M	Yes [ ]
TP13	CID pattern used in TSS	50.3.8.3.2	72 bits of ones and 72 bits of zeros	M	Yes [ ]
TP14	Alternating value for CID pattern	50.3.8.3.2	72 bits of zeros in first frame and 72 bits of ones in second	M	Yes [ ]

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51. Physical Medium Attachment (PMA) sublayer, type Serial

51.1 Overview

This clause defines the functional characteristics for the Physical Media Attachment (PMA) used in 10GBASE-R and 10GBASE-W. Figure 51–1 depicts the relationships of the serial PMA (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

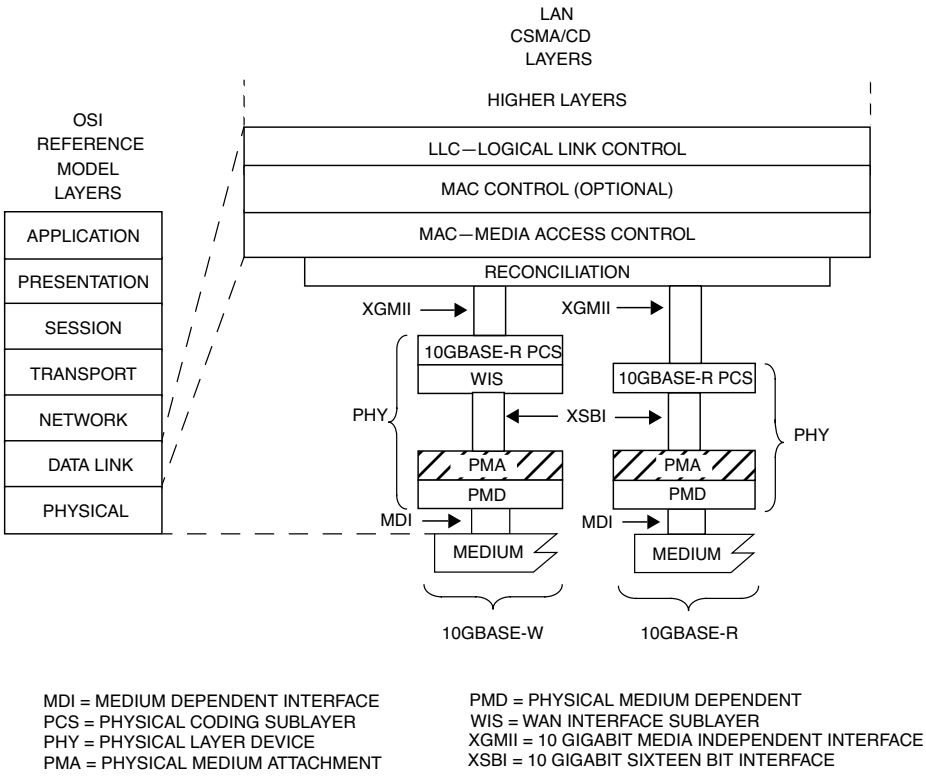


Figure 51–1—Relationship of serial PMA to PCS, WIS, and PMD

The purpose of the serial PMA is to attach the PMD of choice to its client, i.e., the PCS or WIS sublayer.

51.1.1 Scope

This clause specifies the functions, features, and services of the serial PMA sublayer, including electrical and timing specifications for the 10 Gigabit sixteen bit interface (XSBI). Specifications for the serial input and output of the PMA are left to the implementer with conformance and consideration of the serial PMD type. The serial PMA is used between the PMD and the PMA client as shown in Figure 51–1.

51.1.2 Summary of functions

The following is a summary of the principal functions implemented by the PMA.

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In the transmit direction (i.e., transmitting data from the PMA client to the PMD), the PMA performs the following functions:

a) Provide transmit source clock to PMA client.
b) Serialization of 16-bit data to serial bit stream.
c) Transmission of serial data to PMD.

In the receive direction (i.e., serial data from PMD to the PMA client), the PMA performs the following functions:

a) Bit clock recovery of serial data from PMD.
b) Provide receive clock to PMA client.
c) Deserialization of serial data to16-bit parallel data.
d) Transmission of parallel data to PMA client.
e) Provide link status information.

51.2 PMA Service Interface

The Serial PMA provides a Service Interface to the 10G BASE-R PCS or WIS sublayer, i.e., the PMA client. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface shall support the exchange of data-groups between the PMA and the PMA client. The PMA converts data-groups into bits and passes these to the PMD, and vice versa. It also generates an additional status indication for use by its client.

The following primitives are defined:

PMA_UNITDATA.request(tx_data-group<15:0>

PMA_UNITDATA.indicate(rx_data-group<15:0>)

PMA_SIGNAL.indicate(SIGNAL_OK)

51.2.1 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of data-groups) from the PMA client to the PMA. PMA_UNITDATA.request is generated by the PMA client's transmit process.

51.2.1.1 Semantics of the service primitive

PMA_UNITDATA.request(tx_data-group<15:0>)

The data conveyed by PMA_UNITDATA.request is a 16 bit vector representing a single data-unit which has been prepared for transmission by the PMA client.

51.2.1.2 When generated

The PMA client continuously sends tx_data-group<15:0> to the PMA at a nominal clock rate of 644.53125 MHz and 622.08 MHz in 10GBASE-R and 10GBASE-W operations, respectively.

51.2.1.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a series of sixteen PMD_UNITDATA.request primitives, requesting transmission of the indicated tx_data-group bit to the PMD.

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51.2.2 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of data-groups) from the PMA to its client. PMA_UNITDATA.indicate is used by the client's synchronization process.

51.2.2.1 Semantics of the service primitive

PMA_UNITDATA.indicate(rx_data-group<15:0>)

The data conveyed by PMA_UNITDATA.indicate is a 16 bit vector representing a single data-unit which has been prepared for transmission by the PMA receive process to the PMA client.

51.2.2.2 When generated

The PMA continuously sends one rx_data-group<15:0> to the PMA client corresponding to the receipt of each data-group of sixteen PMD_UNITDATA.indicate primitives received from the PMD. The PMA sends the rx_data-group<15:0> at a nominal rate derived from the recovered bit clock.

51.2.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

51.2.3 PMA_SIGNAL.indicate

This primitive is sent by the PMA to its client to indicate the status of the receive process. PMA_SIGNAL.indicate is generated by the PMA receive process to propagate the detection of severe error conditions (e.g. no valid signal being received from the PMD sublayer) to the PMA client.

51.2.3.1 Semantics of the service primitive

PMA_SIGNAL.indicate (SIGNAL_OK)

The SIGNAL_OK can take one of two values: OK or FAIL. A value of FAIL denotes that invalid data is being presented to the PMA client. A value of OK does not guarantee valid data is being presented to the PMA client.

51.2.3.2 When generated

The PMA generates a PMA_SIGNAL.indicate primitive to the PMA client whenever there is change in the value of the SIGNAL_OK parameter.

51.2.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer

51.3 Functions within the PMA

The PMA comprises the PMA Transmit and PMA Receive processes for 10GBASE-W and 10GBASE-R. The PMA Transmit process serializes the tx_data-groups and passes them to the PMD for transmission on the underlying medium. Similarly, the PMA Receive process deserializes received data from the PMD and presents the data as rx_data-groups to the PMA client. The PMA receiver continuously conveys sixteen-bit data-groups to the PMA client, independent of data-group alignment.

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NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clause 52. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

51.3.1 PMA transmit function

The PMA Transmit function passes data unaltered (except for serializing) from the PMA client directly to the PMD. Upon receipt of a PMA_UNITDATA.request primitive, the PMA Transmit function shall serialize the sixteen bits of the tx_data-group<15:0> parameter and transmit them to the PMD in the form of sixteen successive PMD_UNITDATA.request primitives.

51.3.2 PMA receive function

The PMA Receive function passes data unaltered from the PMD directly to the PMA client. Upon receipt of sixteen successive PMD_UNITDATA.indicate primitives, the PMA shall assemble the sixteen received bits into a single sixteen-bit value and pass that value to the PMA client as the rx_data-group<15:0> parameter of the primitive PMA_UNITDATA.indicate. The PMA receive function does not align rx_data-group<15:0> to the original tx_data-group<15:0> from the remote end of the link.

51.3.3 Delay Constraints

The PMA receives a one bit data stream from the PMD and presents a sixteen bit wide data unit to the PMA client. Received bits from the PMD are buffered to facilitate proper deserialization of the rx_data-group<15:0> to the PMA client. These functions necessitate an internal PMA delay of at least sixteen bit times. In practice, this serial to parallel conversion may necessitate even longer delays of the incoming data stream.

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers will conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay constraints for the serial PMA/PMD sublayer shall be no more than 512 BT. The serial PMA/PMD sublayer includes the serial PMA, the serial PMD, and two meters of fiber.

51.4 Sixteen-Bit Interface (XSBI)

A physical instantiation of the sixteen-bit PMA service interface (XSBI) is defined to provide compatibility among devices designed by different manufacturers for the operation of PHY implementations in either the 10GBASE-R family or the 10GBASE-W family. There is no requirement for an integrated compliant device to implement or expose the XSBI. A XSBI implementation is described in 51.4 through 51.9. Though the XSBI is an optional interface, it is used extensively in this standard as a basis for specification. The PMA is specified to the XSBI interface, so if the XSBI is not physically implemented, a conforming implementation shall behave as if the XSBI functions were implemented.

Table 51–1 defines terms used within the description of the XSBI interface and the rest of this clause. For the XSBI instantiation of the PMA service interface, the mapping of bits between the PMA service interface and the XSBI physical interface is defined for transmit in Table 51–2 and for receive in Table 51–3. Figure 51–2 depicts the relationship between the XSBI physical instantiation and the service interface provided by the PMA to its client.

NOTE—Document OIF SFI-4-01.0, an implementer's agreement, was used as a basis for the development of the XSBI instantiation.

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Table 51–1—Terms and definitions

Term	Definition
10GBASE-R nominal baud rate	10.3125Gb/s
10GBASE-W nominal baud rate	9.95328Gb/s
Data signals, data-group, clock signal	Operating rate is 1/16 of nominal baud rate
Differential signal name used without <P,N> (e.g., PMA_TX_CLK)	= signal<P> minus signal <N> (e.g., = PMA_TX_CLK<P-N>)

Table 51–2—Transmit bit mapping

	Name	Bit numbers															
PMA service interface	tx_data-group	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
XSBI physical interface	xsbi_tx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 51–3—Receive bit mapping

	Name	Bit numbers															
PMA service interface	rx_data-group	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
XSBI physical interface	xsbi_rx	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

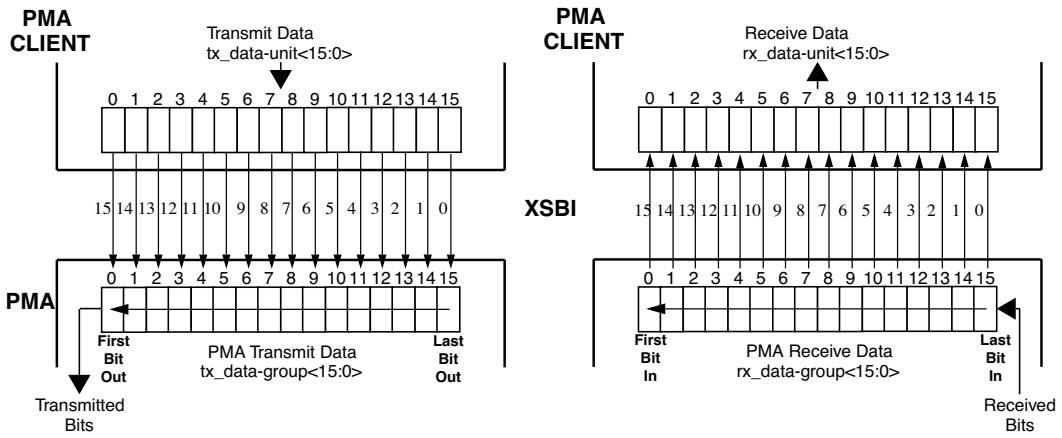


Figure 51–2—XSBI physical interface mapping into PMA service interface

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As depicted in Figure 51–3, the XSBI connects the PMA to its client, the PCS or WIS sublayer. It is equipped for full duplex transmission of data-groups with associated data-group clock signals. The PMA client provides data-groups on xsbi_tx<15:0> to the XSBI transmit function which latches the data on the rising edge of the PMA_TX_CLK. See section 51.6.1.2 for details. The PMA_TX_CLK signal is derived from PMA_TXCLK_SRC as provided by the PMA. An internal Transmit Clock Generation Unit (TXCGU) uses REFCLK to generate the internal bit clock that is used to serialize the latched data out of the PMA outputs.

The PMA Receive function accepts serial data from the PMD and extracts a bit clock and recovered data from the serial inputs in the Receive Clock Recovery Unit (RXCRU). The recovered data is deserialized and conveyed to the PMA client on xsbi_rx<15:0>. The rising edge of the recovered clock, PMA_RX_CLK, which is at 1/16 the bit rate, is used by the PMA to send the received 16-bit data-groups to the PMA client.

The PMA_SIGNAL.indicate is a function of PMD_SIGNAL.indicate, the Sync_Err signal and the optional PMA loopback signal. These signals can be seen in context in Figure 44A–7 and Figure 51–3. In the case of PMA loopback being inactive, the PMA_SIGNAL will indicate a FAIL whenever the PMD_SIGNAL.indicate indicates a FAIL. The PMA_SIGNAL will also indicate a FAIL when Sync_Err is valid, i.e., PMA unable to recover clock from the incoming data stream. If the PMA loopback function is implemented and activated, the PMA_SIGNAL.indicate will ignore the PMD_SIGNAL.indicate and behave as if PMD_SIGNAL.indicate is valid.

PMA_RX_CLK is derived from the serial input data whenever possible. When there is no valid input signal or the optional Sychronization Error (Sync_Err) asserted or other conditions where the PMA cannot derive the clock from the serial input data, a valid PMA_RX_CLK is provided as described in 51.7.2.

51.4.1 Required signals

In the event this XSBI is made accessible, the signals listed in Table 51–4 are provided, with the meanings described elsewhere in this subclause.

Table 51–4—XSBI required signals

Symbol	Signal name	Signal type	Active level
xsbi_tx<15:0>	Transmit Data	Input	H
PMA_TX_CLK<P,N>	Transmit Clock	Input	↑
PMA_TXCLK_SRC<P,N>	Transmit Clock Source	Output	either edge
xsbi_rx<15:0>	Receive Data	Output	H
PMA_RX_CLK<P,N>	Receive Clock	Output	↑
PMA_SI<P>	PMA Signal Indicate	Output	H

xsbi_tx<15:0>
: The 16-bit parallel low-voltage differential signaling (LVDS) data presented to the XSBI for serialization and transmission onto the media. Bit xsbi_tx<15> shall be transmitted first, followed by xsbi_tx<14> through xsbi_tx<0>.

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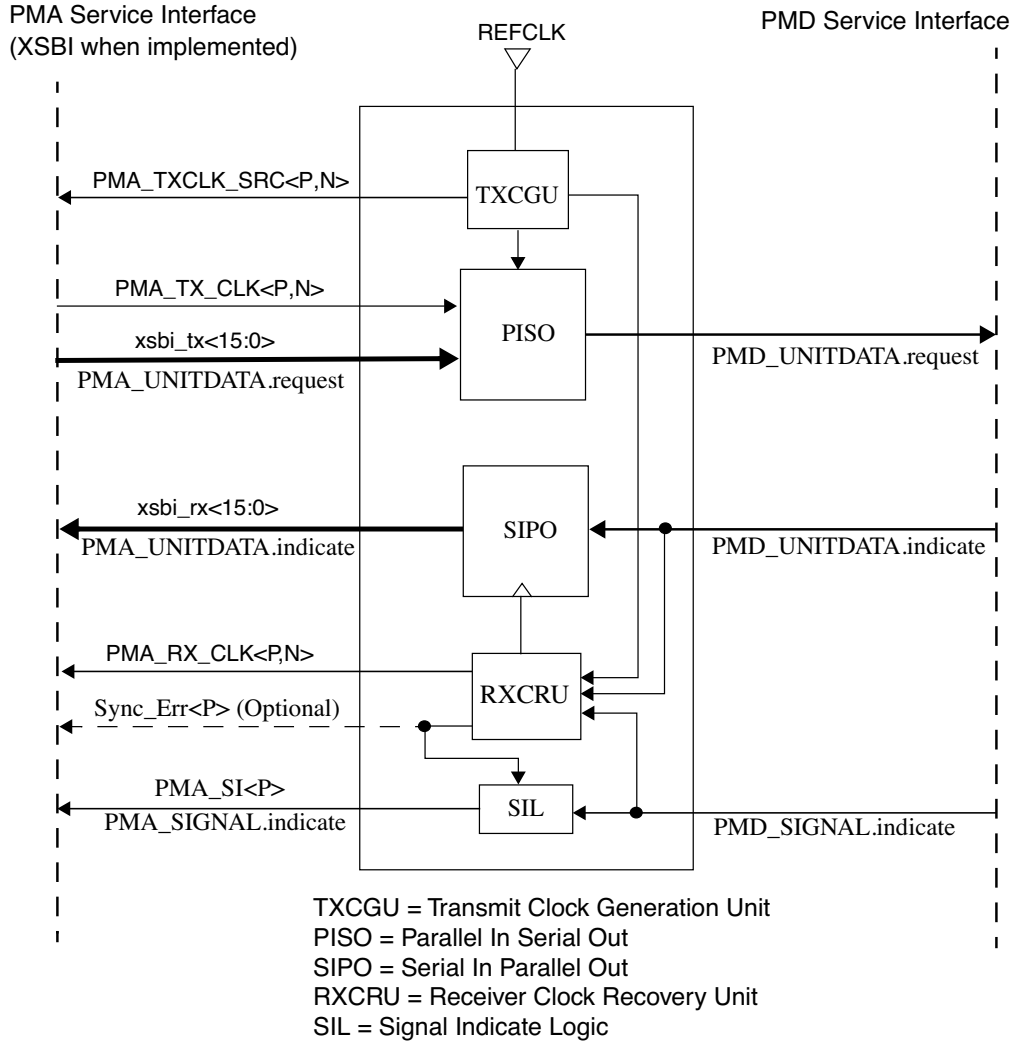


Figure 51–3—XSBI reference diagram

PMA_TX_CLK<P,N>

The LVDS transmit data-group clock. This data-group clock is used to latch data into the PMA for transmission. The PMA_TX_CLK<P,N> shall be derived from PMA_TXCLK_SRC<P,N>. The rising edge of PMA_TX_CLK is used to latch data into the PMA for transmission. Refer to 51.6.1.2 for details.

PMA_TXCLK_SRC<P,N>

The LVDS transmit data-group clock source. The PMA derives the PMA_TXCLK_SRC<P,N> from the local REFCLK. The PMA_TXCLK_SRC<P,N> is used by the PMA client to derive PMA_TX_CLK<P,N>.

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xsbi_rx<15:0>
: The 16-bit parallel LVDS data transmitted by the PMA and presented to the PMA client for further processing. The PMA deserializes the incoming data to 16-bit wide data groups, xsbi_rx<15:0>. Bit xsbi_rx<15> shall be received first, followed by xsbi_rx<14> through xsbi_rx<0>. Data alignment is NOT performed by the PMA.

PMA_RX_CLK<P,N>
: The LVDS receive data-group clock. The PMA derives the PMA_RX_CLK<P,N> from the line rate when the serial data from the PMD is present, or the REFCLK when the serial data from the PMD is absent, e.g. PMD_SI invalid or Sync_Err asserted. The xsbi_rx<15:0> data groups are presented to the PMA client on the rising edge of PMA_RX_CLK<P,N>.

PMA_SI<P>
: A logic 0 on PMA Signal Indicate (PMA_SI) indicates that the receiver is unable to properly recover the receive data. The indicator is a function of the PMD_SIGNAL.indicate status, the Sync_Err function and the optional PMA loopback signal. This signal is the physical instantiation of the SIGNAL_OK parameter as described in the PMA_Signal.indicate primitive. This signal shall be compliant with the EIA/JESD8-B Interface Standards for Nominal 3V/3.3V Supply Digital Integrated Circuits.

51.4.2 Optional Signals

Sync_Err<P>
: This signal is used to indicate the inability of the PMA to recover the clock from the serial data stream. A logic high indicates that there is a synchronization error. A logic low does not guarantee synchronization. This signal shall be compliant with the EIA/JESD8-B Interface Standards for Nominal 3V/3.3V Supply Digital Integrated Circuits.

51.5 General electrical characteristics of the XSBI

In the event this XSBI is made accessible, this subclause specifies the general electrical characteristics of the XSBI.

NOTE—All LVDS AC and DC parameters shall conform to the TIA/EIA-644 LVDS specification with the exception of those parameters specified by the tables of this clause.

51.5.1 DC characteristics

Table 51–5 documents the required DC parametric attributes of all inputs and outputs of the XSBI. The signal specification is based on low voltage differential signals (LVDS) as described in ANSI/TIA-644 LVDS specifications. Unless otherwise stated, all terms and test conditions related to electrical parameters (AC or DC) are as specified in the TIA/EIA-644 LVDS document.

51.5.2 Valid signal levels

All AC measurements are made from the cross-over level of the clock to the valid input or output data levels as shown in Figure 51–4. The CLK and DATA is defined to be the differential signal, i.e., <P-N>, of a clock or data signal.

51.5.3 Rise and fall time definition

The rise and fall time definition for PMA_TX_CLK, PMA_TXCLK_SRC, PMA_RX_CLK, and DATA is shown below in Figure 51–5. All signals are measured differentially.

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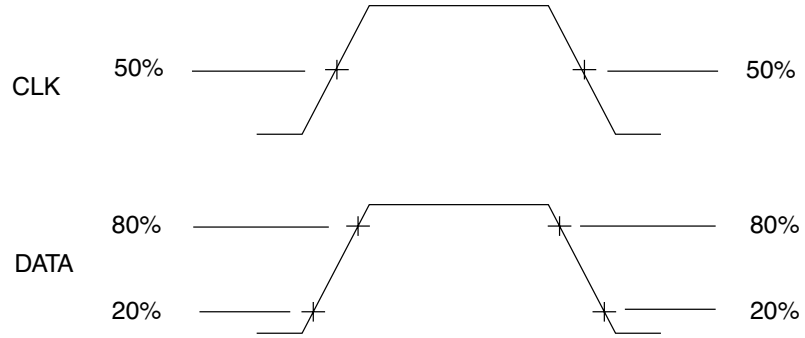


Figure 51–4—Input/output valid level for AC measurements

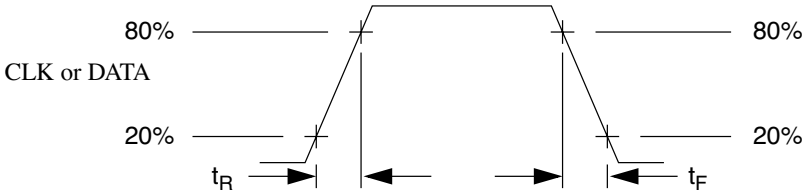


Figure 51–5—Rise and fall time definition

Table 51–5—Electrical specifications

Symbol	Parameter	Conditions	Min	Max	Units	Note
$\|V_{OD}\|$	Output differential voltage	Differential load, R_{load}=100Ω +/–1%	250	400	mV	
V_{OS}	Output offset voltage	Differential load, R_{load}=100Ω +/–1%	1125	1375	mV	
R_O	Output impedance, single ended		40	140	Ω	[a]
ΔR_O	R_O mismatch			10	%	*
$\|\Delta V_{OD}\|$	Change in VOD between “0” and “1”	Differential load, R_{load}=100Ω +/–1%		50	mV	
$\|\Delta V_{OS}\|$	Change in VOS between “0” and “1”	Differential load, R_{load}=100Ω +/–1%		50	mV	
V_I	Input voltage range	|Vgpd| <50mV	900	1600	mV	[b]
V_{ID}	Input differential voltage	|Vgpd| <50mV	100	600	mV	
R_{IN}	Receiver differential input impedance		70	130	Ω	*
t_R, t_F	20%-80% rise and fall times		100	400	ps	*

[a]Modified from or not specified in TIA/EIA-644 document.
[b]$|V_{gpd}|$ is the ground potential differential between PMA client and PMA.

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51.5.4 Output load

All AC measurements are assumed to have a differential output load of 100 Ω +/–1%.

51.6 XSBI transmit interface electrical characteristics

In the event this XSBI is made accessible, the electrical characteristics of the XSBI transmit interface are specified in this subclause. A XSBI receiver shall meet the specifications in sections 51.6.1 through 51.6.2.

NOTE—The following approach is taken for positioning clocks relative to the data. For both the PMA and PMA client drivers, the <P-N> clock edges are aligned to the data edges, to allow simplification of macro design. For both the PMA and PMA client receivers, the <P-N> clock edges are centered on the data bit, to allow simplification of macro design. The implementation to meet these requirements may be achieved on the system board. This can be done with either a delay of the clocks or by exchanging the positive and negative signals of the differential clock outputs.

51.6.1 XSBI transmit interface timing

The XSBI transmit interface timing specification consists of two separate specifications. The timing specifications at the PMA client output and the PMA input are described in 51.6.1.1 and 51.6.1.2, respectively. Data is latched into the PMA using rising edge of PMA_TX_CLK. The relationship between PMA_TX_CLK and PMA_TXCLK_SRC are described in 51.6.2. All transitions in Figure 51–6 and Figure 51–7 are specified from the PMA_TX_CLK reference level, to valid input signal levels (refer to 51.5.2).

51.6.1.1 PMA client output timing

Figure 51–6 and Table 51–6 detail the XSBI timing requirements for transmit data relative to PMA_TX_CLK at the PMA client outputs.

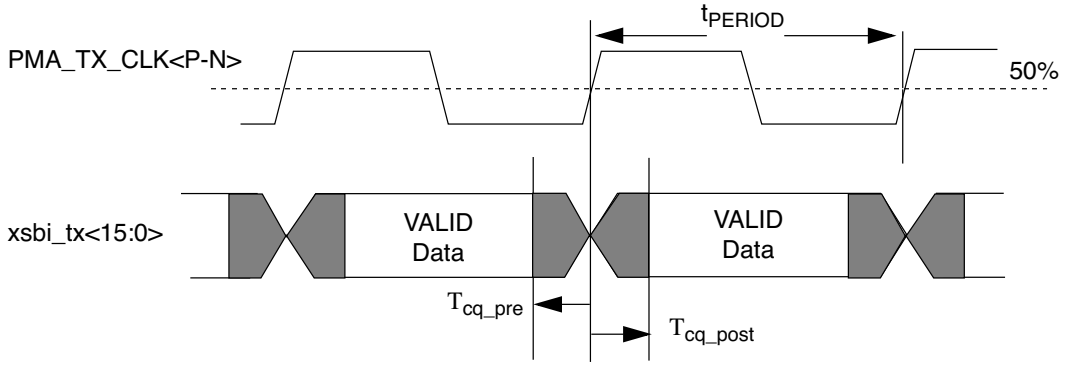


Figure 51–6—PMA client output timing

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Table 51–6—PMA client output timing specifications

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK Period 10GBASE-R 10GBASE-W		 1.55151 1.60751		ns[a]
T_{cq_pre}	data invalid window before ↑ PMA_TX_CLK<N-P>			200	ps
T_{cq_post}	data invalid window after ↑ PMA_TX_CLK<N-P>			200	ps
t_{DUTY}	PMA_TX_CLK Duty Cycle	40		60	%

[a]Period time value =1 / 644.53125 MHz for 10GBASE-R, similarly = 1/622.08 MHz for 10GBASE-W.

51.6.1.2 PMA input timing

Figure 51–7 and Table 51–7 detail the XSBI timing requirements for transmit data relative to the PMA_TX_CLK at the PMA inputs.

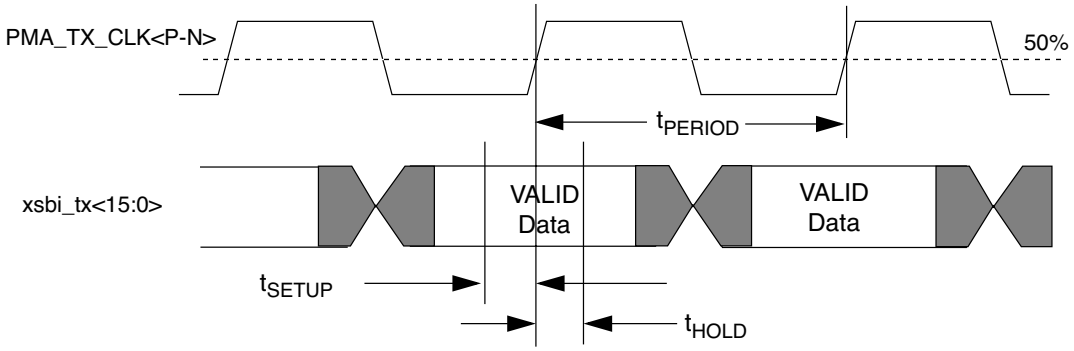


Figure 51–7—PMA input timing

Table 51–7—PMA input timing specifications

Parameter	Description	Min	Typ	Max	Units
t_{PERIOD}	PMA_TX_CLK Period 10GBASE-R 10GBASE-W		 1.55151 1.60751		ns
t_{SETUP}	Data Setup to ↑ PMA_TX_CLK	300			ps
t_{HOLD}	Data Hold from ↑ PMA_TX_CLK	300			ps
t_{DUTY}	PMA_TX_CLK Duty Cycle	40		60	%

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51.6.2 XSBI PMA_TX_CLK and PMA_TXCLK_SRC Specification

Table 51–8 specifies the XSBI interface transmit frequency. The frequency of xsbi_tx<15:0> and PMA_TX_CLK are derived from the frequency of PMA_TXCLK_SRC.

Table 51–9 specifies the phase variation between PMA_TX_CLK and PMA_TXCLK_SRC and the jitter requirements between PMA_TX_CLK and PMA_TXCLK_SRC. This specification describes the maximum delay variation through the PMA client (PMA_TXCLK_SRC to PMA_TX_CLK and xsbi_tx<15:0>). The absolute value of the delay is not specified, as it is not relevant to the operation of the interface.

Table 51–8—Transmit source clock specification

Parameter	Description	Value
$f_{PMA\_TXCLK\_SRC}$	PMA_TXCLK_SRC frequency 10GBASE-W 10GBASE-R	 622.08 MHz +/–20 ppm 644.53125 MHz +/–100 ppm

Table 51–9—Transmitter clocks specification

Parameter	Description	Condition	Value(max)
TD	Variation of PMA_TXCLK_SRC to PMA_TX_CLK delay	frequency < 10 kHz	2ns(p-p)
CJ	Jitter between PMA_TXCLK_SRC and PMA_TX_CLK	frequency >10 kHz	175ps(p-p)

NOTE—The +/–20 ppm clock tolerance is not intended to interoperate directly with interfaces that comply with SONET of SDH standards, or other synchronous networks. Operation over electrically multiplexed payloads of a transmission network is outside the scope of this standard.

The TD parameter is defined to be the peak-to-peak variation of the phase offset measured in time between an arbitrary clock edge of the PMA_TXCLK_SRC clock and a selected clock edge on the PMA_TX_CLK. Letting "X" be the offset parameter, then $TD = X_{max} - X_{min}$.

51.7 XSBI receive interface electrical characteristics

In the event this XSBI is made accessible, the electrical characteristics of the XSBI receive interface are specified in this subclause. A XSBI receiver shall meet the specifications in 51.7.1 through 51.7.2.

NOTE—The following approach is taken for positioning clocks relative to the data. For both the PMA and PMA client drivers, the <P-N> clock edges are aligned to the data edges, to allow simplification of macro design. For both the PMA and PMA client receivers, the <P-N> clock edges are centered on the data bit, to allow simplification of macro design. The implementation to meet these requirements may be achieved on the system board. This can be done with either a delay of the clocks or by exchanging the positive and negative signals of the differential clock outputs.

51.7.1 XSBI receive interface timing

The XSBI receive interface timing specification consists of two separate specifications. The timing specifications at the PMA output and the PMA client input are described in 51.7.1.1 and 51.7.1.2, respectively. Data

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is latched into the PMA client using the rising edge of PMA_RX_CLK. All transitions in Figure 51–8 and Figure 51–9 are specified from the PMA_RX_CLK reference level, to valid output signal levels (refer to 51.5.2).

51.7.1.1 PMA output timing

Figure 51–8 and Table 51–10 detail the XSBI timing requirements for receive data relative to the PMA_RX_CLK at the PMA outputs.

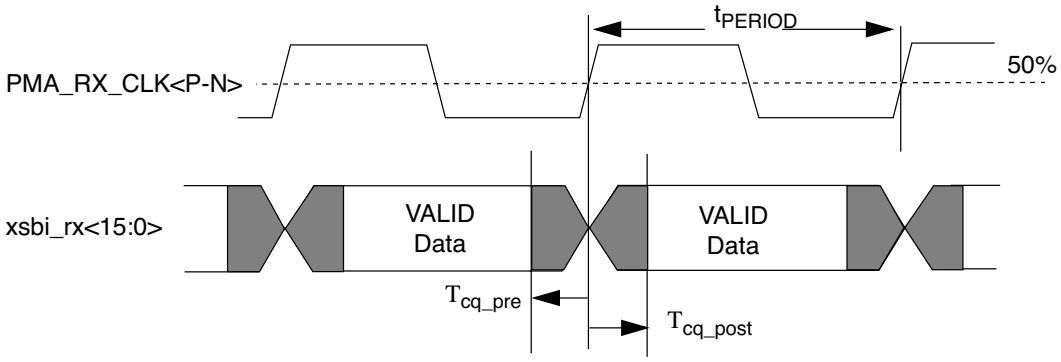


Figure 51–8—PMA output timing

Table 51–10—PMA output timing specifications

Parameter	Description	Min	Typical	Max	Units
t_{PERIOD}	PMA_RX_CLK Period 10GBASE-R 10GBASE-W	—	 1.55151 1.60751	—	ns
T_{cq_pre}	data invalid window before ↑ PMA_RX_CLK<N-P>	—	—	200	ps
T_{cq_post}	data invalid window after ↑ PMA_RX_CLK<N-P>	—	—	200	ps
t_{DUTY}	PMA_RX_CLK Duty Cycle	45	—	55	%

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51.7.1.2 PMA client input timing

Figure 51–9 and Table 51–11 detail the XSBI timing requirements for receive data relative to the PMA_RX_CLK at the PMA client inputs.

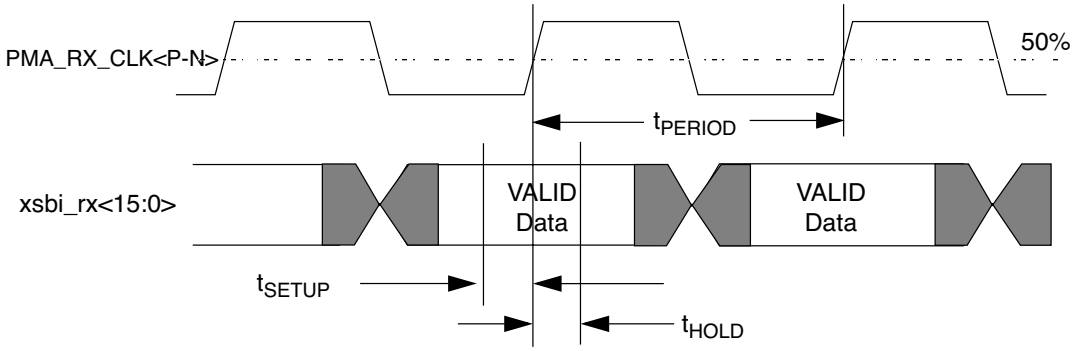


Figure 51–9—PMA client input timing

Table 51–11—PMA client input timing specifications

Parameter	Description	Min	Typical	Max	Units
t_{DUTY}	PMA_RX_CLK Duty Cycle	45	—	55	%
t_{SETUP}	Data Setup Before ↑PMA_RX_CLK	300	—	—	ps
t_{HOLD}	Data Hold After ↑PMA_RX_CLK	300	—	—	ps

51.7.2 XSBI PMA_RX_CLK Specification

Table 51–12 defines the PMA_RX_CLK frequency variation during PMA_SI valid and invalid conditions. PMA_RX_CLK is derived from the serial input data whenever possible. Under a loss-of-signal (LOS) or the optional Sychronization Error (Sync_Err) or other conditions where the PMA cannot derive the clock from the serial input data, a valid PMA_RX_CLK shall be provided with frequency characteristics as defined in Table 51–12. During the transitions from nominal clock to recovered clock or from recovered clock to nominal clock, the period and duty cycle requirements do not apply. However, the minimum pulse width should not change during the transitions between clock sources. During the transitions, the PMA_RX_CLK pulse width shall not be less than the minimum that is calculated by the period times the duty cycle as defined in Table 51–10 and Table 51–12.

51.8 PMA Loopback mode (optional)

PMA Loopback is optional. If PMA Loopback is implemented it shall conform to the requirements of this subclause, i.e., 51.8.

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Table 51–12—Receiver clock specification

PMA_SI	Parameter	Description	Value
valid	$f_{PMA\_RX\_CLK}$	PMA_RX_CLK frequency 10GBASE-W 10GBASE-R	 622.08 MHz+/–100 ppm 644.53125 MHz+/–100 ppm
invalid	$f_{PMA\_RX\_CLK}$	PMA_RX_CLK frequency 10GBASE-W 10GBASE-R	 622.08 MHz+/–2500 ppm 644.53125 MHz+/–2500 ppm

If a Clause 45 MDIO is supported, then this function maps to the PMA Loopback function as specified in 45.2.1.1.4. A device is placed in Loopback mode when the loopback bit in the PMA/PMD Control register 1 is set to a logic one. A device is removed from Loopback mode when this bit is set to a logic zero.

When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). The method of implementing Loopback mode is not defined by this standard.

NOTE—Loopback mode may be implemented either in the parallel or the serial circuitry of a device.

51.9 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801:1995.

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51.10 Protocol Implementation Conformance Statement (PICS) proforma for Clause 51, Physical Medium Attachment (PMA) sublayer, type Serial[15]

51.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 51, PMA Interface Sublayer, type Serial, shall complete the following Protocol Implementation Conformation Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the same, can be found in Clause 21.

51.10.2 Identification

51.10.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

51.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 51, PMA Interface Sublayer (PMA), type Serial
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[15]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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51.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*XSBI	XSBI interface	51.4	Physical instantiation of PMA service interface	O	Yes [ ] No [ ]
M1	XSBI functionality	51.4	Behave functionally as if the XSBI is implemented	M	Yes [ ]
M2	PMA Service Interface	51.2	Supports data group transfer between PMA and PMA client	M	Yes [ ]
M3	PMA_SI	51.4.1	EIA/JESD8-B compliance	M	Yes [ ]
M4	Sync_Err	51.4.2	Local PMA synchronization indicator and EIA/ JESD8-B compliance	O	Yes [ ] No [ ]
M5	Local PMA Loopback	51.8		O	Yes [ ] No [ ]
MD	MDIO interface	51.8	Registers and interface supported	O	Yes [ ] No [ ]

51.10.4 PICS proforma tables for the PMA Interface Sublayer, type Serial

51.10.4.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Environmental specifications	51.9		M	Yes [ ]

51.10.4.2 PMA transmit functions

Item	Feature	Subclause	Value/Comment	Status	Support
PT1	Serialization and transmission of datagroup	51.3.1		M	Yes [ ]
PT2	Order of transmission	51.4.1	Bit xsbi_tx<15> shall be transmitted first	M	Yes [ ]
PT3	PMA_TX_CLK	51.4.1	PMA_TX_CLK derived from PMA_TXCLK_SRC	XSBI:M	Yes [ ] N/A[ ]
PT4	LVDS electrical compliance	51.5	Conformance to TIA/EIA644 LVDS specifications and to Table 51–5	XSBI:M	Yes [ ] N/A[ ]
PT5	transmit electrical specifications	51.6	Electrical and timing specifications	XSBI:M	Yes [ ] N/A[ ]

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51.10.4.3 PMA receive functions

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	Deserialization and transmissions of datagroup to PMA client	51.3.2		M	Yes [ ]
PR2	Order of reception	51.4.1	Bit xsbi_rx<15> shall be received first	M	Yes [ ]
PR3	LVDS electrical compliance	51.5	conformance to TIA/EIA644 LVDS specifications and to Table 51–5	XSBI:M	Yes [ ] N/A:[ ]
PR4	Transmit electrical specifications	51.7	Electrical and timing specifications	XSBI:M	Yes [ ] N/A[ ]
PR5	Valid PMA_RX_CLK	51.7.2	A valid clock is provided as defined in Table 51–12	XSBI:M	Yes [ ] N/A[ ]
PR6	PMA_RX_CLK pulse width during valid and invalid transitions	51.7.2	Clock pulse width is greater than or equal to the period times the duty cycle	XSBI:M	Yes [ ] N/A[ ]

51.10.4.4 PMA delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Maximum delay for PMA/PMD functions	51.3.3	transmit and receive including PMD and fiber shall be less than 512 BT (bit times)	M	Yes [ ]

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52. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-S (Short Wavelength Serial), 10GBASE-L (Long Wavelength Serial), and 10GBASE-E (Extra Long Wavelength Serial)

52.1 Overview

This clause specifies the PMDs and baseband media, including both single and multimode optical fiber, for the following 10GBASE serial PHYs, shown in Table 52–1.

Table 52–1—10GBASE serial PHYs

Name	Description
10GBASE-SR	850 nm Serial LAN PHY
10GBASE-LR	1310 nm Serial LAN PHY
10GBASE-ER	1550 nm Serial LAN PHY
10GBASE-SW	850 nm Serial WAN PHY
10GBASE-LW	1310 nm Serial WAN PHY
10GBASE-EW	1550 nm Serial WAN PHY

In order to form a complete physical layer, each PMD is combined with the appropriate physical sublayers indicated in Table 52–2 and optionally with the management functions that may be accessible through the management interface defined in Clause 45.

Table 52–2—PMD type and associated clauses

Associated clause	10GBASE-R	10GBASE-W
46—RS	Required	Required
46—XGMII	Optional	Optional
47—XGXS and XAUI	Optional	Optional
49—Type R PCS	Required	Required
50—WIS	N/A	Required
51—Serial PMA	Required	Required

Figure 52–1 depicts the relationships of the serial PMD (shown shaded) with other sublayers and the ISO/IEC Open System Interconnection (OSI) reference model.

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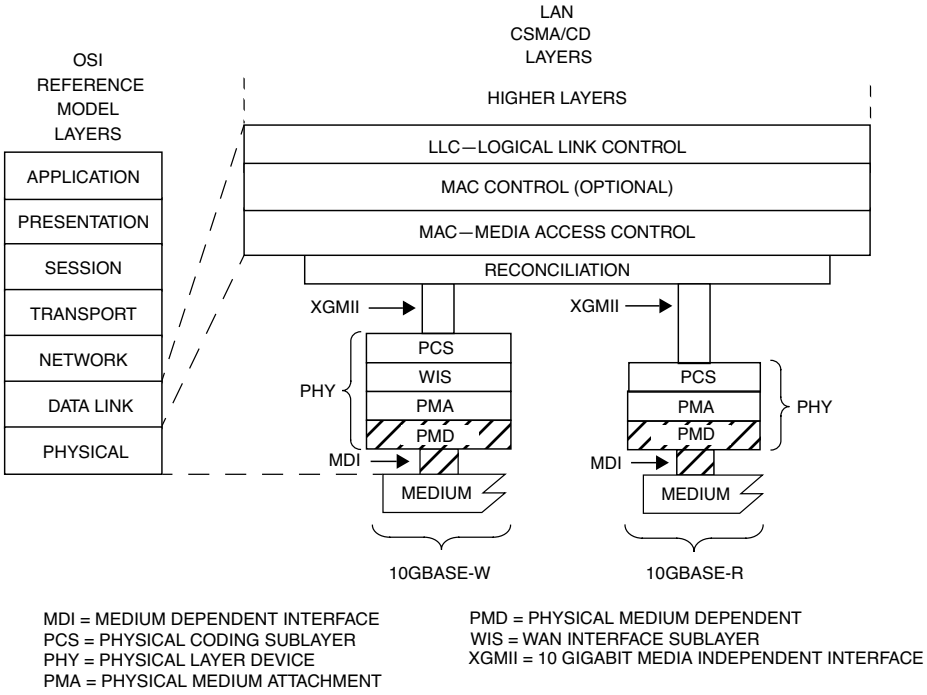


Figure 52–1—10GBASE-S, -L, and -E PMDs relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

52.1.1 Physical Medium Dependent (PMD) sublayer service interface

The following specifies the services provided by the 10GBASE-R and 10GBASE-W PMDs. These PMD sublayer service interfaces are described in an abstract manner and do not imply any particular implementation.

The PMD Service Interface supports the exchange of encoded and scrambled 64B/66B blocks between the PMA and PMD entities. In the case of the 10GBASE-W PMD types, these blocks are framed and scrambled by the WIS as described in Clause 50. The PMD translates the serialized data of the PMA to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indicate

PMD_SIGNAL.indicate

NOTE—Primitives are described in 1.2.2.

52.1.1.1 PMD_UNITDATA.request

This primitive defines the transfer of a serial data stream from the PMA to the PMD.

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52.1.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request(tx_bit)

The data conveyed by PMD_UNITDATA.request is a continuous stream of bits. The tx_bit parameter can take one of two values: ONE or ZERO.

52.1.1.1.2 When generated

The PMA continuously sends the appropriate stream of bits to the PMD for transmission on the medium, at a nominal 10.3125 GBaud signaling speed for 10GBASE-R PMD types and 9.95328 GBaud signaling speed for 10GBASE-W PMDs.

52.1.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

52.1.1.2 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of serialized data) from the PMD to the PMA.

52.1.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indicate(rx_bit)

The data conveyed by PMD_UNITDATA.indicate is a continuous stream of bits. The rx_bit parameter can take one of two values: ONE or ZERO.

52.1.1.2.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

52.1.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

52.1.1.3 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

52.1.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indicate(SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting light at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indicate(rx_bit) is undefined.

NOTE—SIGNAL_DETECT = OK does not guarantee that PMD_UNITDATA.indicate(rx_bit) is known good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

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52.1.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT. If the MDIO interface is implemented, then PMD_global_signal_detect shall be continuously set to the value of SIGNAL_DETECT.

52.1.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

52.2 Delay constraints

An upper bound to the delay through the PMA and PMD is required for predictable operation of the MAC Control PAUSE operation. The PMA and PMD shall incur a round-trip delay (transmit and receive) of not more than 512 bit-times, or 1 pause_quantum, including 2 meters of fiber. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 44.3.

52.3 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 52–3, and MDIO status variables to PMD status variables as shown in Table 52–4.

Table 52–3—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global Transmit Disable	Transmit disable register	1.9.0	PMD_global_transmit_disable

Table 52–4—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	PMD_global_signal_detect

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52.4 PMD functional specifications

The 10GBASE-R and 10GBASE-W PMDs perform the Transmit and Receive functions which convey data between the PMD service interface and the MDI.

52.4.1 PMD block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP2 and TP3 as shown in Figure 52–2. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 m in length, of a type consistent with the link type connected to the transmitter. Unless specified otherwise, all transmitter measurements and tests defined in 52.9 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) connected to the receiver. Unless specified otherwise, all receiver measurements and tests defined in 52.9 are made at TP3.

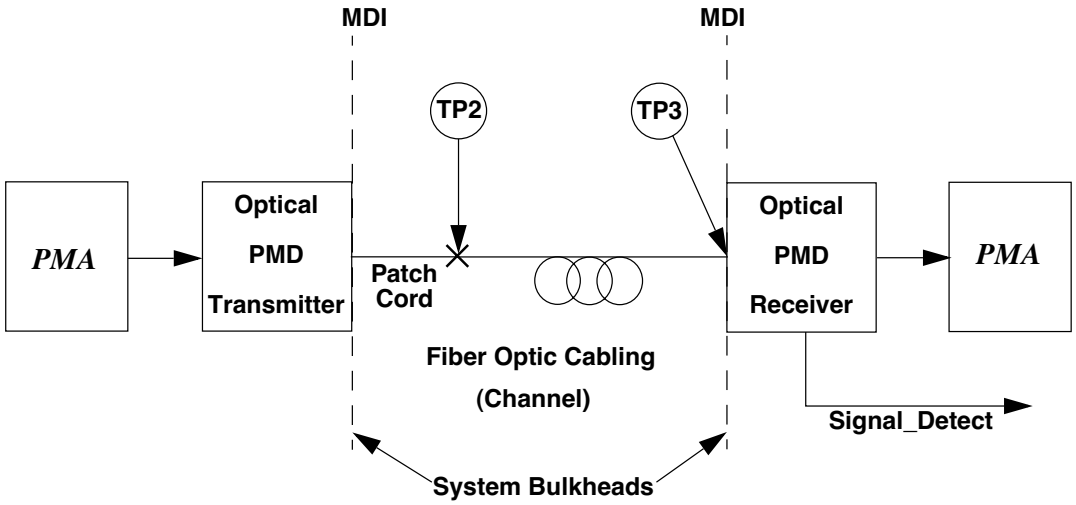


Figure 52–2—Block diagram

52.4.2 PMD Transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the optical specifications in this clause. The higher optical power level shall correspond to tx_bit = ONE.

52.4.3 PMD Receive function

The PMD Receive function shall convey the bits received from the MDI according to the optical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit). The higher optical power level shall correspond to rx_bit = ONE.

52.4.4 PMD Signal Detect function

The PMD Signal Detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indicate(SIGNAL_DETECT) which is signaled continuously. PMD_SIGNAL.indicate is intended to be an indicator of optical signal presence. If the MDIO interface is implemented, then

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PMD_global_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.5.

The value of the SIGNAL_DETECT parameter shall be generated according to the conditions defined in Table 52–5. The PMD receiver is not required to verify whether a compliant 10GBASE-R or 10GBASE-W signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to cross talk, power supply noise, etc.

Table 52–5—SIGNAL_DETECT value definition

Receive conditions	Signal Detect value
Input_optical_power ≤ -30 dBm average power	FAIL
Input_optical_power ≥ Receiver sensitivity (max) in OMA in Table 52–9, Table 52–13, or Table 52–17 AND compliant 10GBASE-R or 10GBASE-W signal input	OK
All other conditions	Unspecified

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

52.4.5 PMD_reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

52.4.6 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault and any other implementation specific fault.

52.4.7 PMD_global_transmit_disable function

The PMD_global_transmit_disable function is optional. When asserted, this function shall turn off the optical transmitter so that it meets the requirements of the average launch power of OFF Transmitter in Table 52–7, Table 52–12, or Table 52–16.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall map to the PMD_global_transmit_disable bit as specified in 45.2.1.8.5.

NOTE—PMD Transmit Disable 0 is not used for serial PMDs.

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52.4.8 PMD_transmit_fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the PMD_global_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the PMD_global_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

52.4.9 PMD_receive_fault function

The PMD_receive_fault function is optional. PMD_receive_fault is the logical OR of NOT SIGNAL_DETECT and any implementation specific fault.

If the MDIO interface is implemented, then this function shall contribute to PMA/PMD receive fault bit as specified in 45.2.1.7.5.

52.5 PMD to MDI optical specifications for 10GBASE-S

The operating ranges for 10GBASE-S are defined in Table 52–6. A 10GBASE-S compliant PMD supports multimode fiber media types listed in Table 52–6 according to the specifications defined in 52.14. A PMD that exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a 400 MHz km 50 μm solution operating at 80 m meets the operating range requirement of 2 to 66 m).

Table 52–6—10GBASE-S operating range for each optical fiber type

Fiber type	Minimum modal bandwidth @ 850 nm (MHz•km)	Operating range (meters)
62.5 μm MMF	160	2 to 26
	200	2 to 33
50 μm MMF	400	2 to 66
	500	2 to 82
	2000	2 to 300

52.5.1 10GBASE-S transmitter optical specifications

The 10GBASE-S transmitter shall meet the specifications defined in Table 52–7 per measurement techniques defined in 52.9. It shall also meet the center wavelength, maximum spectral width and minimum optical modulation amplitude as defined in Table 52–8.

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Table 52–7—10GBASE-S transmit characteristics

Description	10GBASE-SW	10GBASE-SR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	840 to 860		nm
RMS spectral width[a] (max)	See footnote[b]		
Average launch power (max)	See footnote[c]		
Average launch power[d] (min)	–7.3		dBm
Launch power (min) in OMA	See footnote[b]		
Average launch power of OFF transmitter[e] (max)	–30		dBm
Extinction ratio (min)	3		dB
$RIN_{12}OMA$ (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	12		dB
Encircled flux	See footnote[f]		
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		
Transmitter and dispersion penalty[g] (max)	3.9 dB		dB

[a]RMS spectral width is the standard deviation of the spectrum.
[b]Trade-offs are available between spectral width, center wavelength and minimum optical modulation amplitude. See Figure 52–3 and Table 52–8.
[c]The 10GBASE-S launch power shall be the lesser of the class 1 safety limit as defined by 52.10.2 or the average receive power (max) defined by Table 52–9.
[d]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[e]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut down conditions.
[f]The encircled flux at 19 μm shall be greater than or equal to 86% and the encircled flux at 4.5 μm shall be less than or equal to 30% when measured into Type A1a (50/125 μm multimode) fiber per ANSI/TIA/EIA-455-203-2001.
[g]TDP(max) and OMA(min) are at the respective wavelength and spectral width as specified in Table 52–8.

The tradeoffs between center wavelength, maximum RMS spectral width and minimum optical modulation amplitude are defined in Table 52–8 and are shown graphically in the informative Figure 52–3. In Table 52–8 the minimum Optical Modulation Amplitude (dBm) allowed by this standard is given for the various ranges of center wavelength and spectral width.

52.5.2 10GBASE-S receive optical specifications

The 10GBASE-S receiver shall meet the specifications defined in Table 52–9 per measurement techniques defined in 52.9.

52.5.3 10GBASE-S link power budgets (informative)

Example power budgets and penalties for a 10GBASE-S channel are shown in Table 52–10.

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Table 52–8—Minimum 10GBASE-S optical modulation amplitude (dBm) as a function of center wavelength and spectral width

Center Wavelength (nm)	RMS Spectral width (nm)								
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45
840 to 842	–4.2	–4.2	–4.1	–4.1	–3.9	–3.8	–3.5	–3.2	–2.8
842 to 844	–4.2	–4.2	–4.2	–4.1	–3.9	–3.8	–3.6	–3.3	–2.9
844 to 846	–4.2	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–2.9
846 to 848	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–2.9
848 to 850	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.3	–3.0
850 to 852	–4.3	–4.2	–4.2	–4.1	–4.0	–3.8	–3.6	–3.4	–3.0
852 to 854	–4.3	–4.2	–4.2	–4.1	–4.0	–3.9	–3.7	–3.4	–3.1
854 to 856	–4.3	–4.3	–4.2	–4.1	–4.0	–3.9	–3.7	–3.4	–3.1
856 to 858	–4.3	–4.3	–4.2	–4.1	–4.0	–3.9	–3.7	–3.5	–3.1
858 to 860	–4.3	–4.3	–4.2	–4.2	–4.1	–3.9	–3.7	–3.5	–3.2

52.6 PMD to MDI optical specifications for 10GBASE-L

The operating range for 10GBASE-L PMDs is defined in Table 52–11. A 10GBASE-L compliant PMD supports Types B1.1 and B1.3 single mode fibers according to the specifications defined in 52.14. A PMD which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 12.5 km meets the minimum range requirement of 2 m to 10 km).

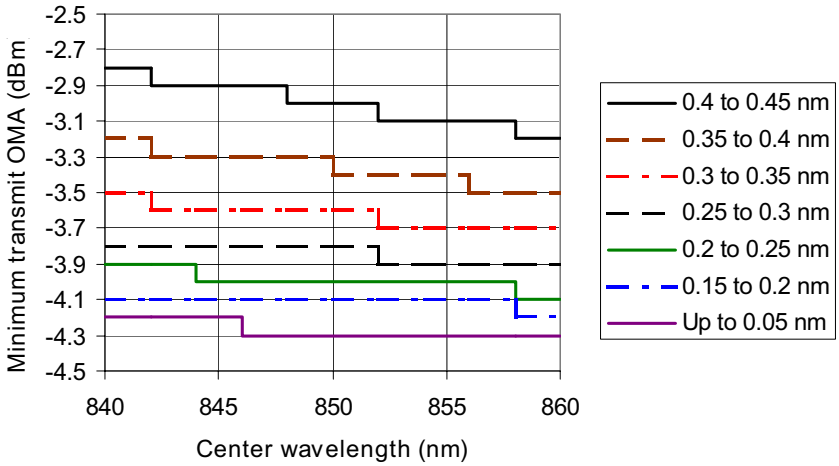


Figure 52–3—Triple tradeoff curve for 10GBASE-S (informative)

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Table 52–9—10GBASE-S receive characteristics

Description	10GBASE-S	Unit
Signaling speed (nominal) 10GBASE-SR 10GBASE-SW	 10.3125 9.95328	GBd
Signaling speed variation from nominal (max)	± 100	ppm
Center wavelength (range)	840 to 860	nm
Average receive power[a] (max)	–1.0	dBm
Average receive power[b] (min)	–9.9	dBm
Receiver sensitivity (max) in OMA[c]	0.077 (–11.1)	mW (dBm)
Receiver Reflectance (max)	–12	dB
Stressed receiver sensitivity in OMA[d] [e](max)	0.18 (–7.5)	mW (dBm)
Vertical eye closure penalty[f] (min)	3.5	dB
Stressed eye jitter[g] (min)	0.3	UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3	GHz

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the Average Receive Power (max) plus at least 1 dB.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity is informative.
[d]Measured with conformance test signal at TP3 (see 52.9.9.2) for BER = 10^{-12}.
[e]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits
[f]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[g]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

Table 52–10—10GBASE-S link power budgets[a,b]

Parameter	62.5 μm MMF		50 μm MMF			Unit
Modal bandwidth as measured at 850 nm	160	200	400	500	2000	MHz•km
Power budget	7.3	7.3	7.3	7.3	7.3	dB
Operating distance	26	33	66	82	300	m
Channel insertion loss[c, d]	1.6	1.6	1.7	1.8	2.6	dB
Allocation for penalties	4.7	4.8	5.1	5.0	4.7	dB
Additional insertion loss allowed[e]	1.0	0.8	0.5	0.5	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[c]Operating distances used to calculate the channel insertion loss are the maximum values specified in Table 52–6.
[d]The specifications for a wavelength of 840 nm and a spectral width of 0.29 nm in Table 52–8 is used to calculate channel insertion loss, allocation for penalties, and additional insertion loss allowed.
[e]This portion of the link budget is permitted to be used to overcome insertion loss higher than the "Channel insertion loss" value and in some cases may be less than the value shown.

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Table 52–11—10GBASE-L operating range

PMD Type	Nominal Wavelength (nm)	Minimum range
10GBASE-L	1310	2 m to 10 km

52.6.1 10GBASE-L transmitter optical specifications

The 10GBASE-L transmitter shall meet the specifications defined in Table 52–12 per measurement techniques defined in 52.9.

Table 52–12—10GBASE-L transmit characteristics

Description	10GBASE-LW	10GBASE-LR	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1260 to 1355		nm
Side Mode Suppression Ratio (min)	30		dB
Average launch power (max)	0.5		dBm
Average launch power[a] (min)	–8.2		dBm
Launch power (min) in OMA minus TDP[b]	–6.2		dBm
Optical Modulation Amplitude[c] (min)	–5.2		dBm
Transmitter and dispersion penalty (max)	3.2		dB
Average launch power of OFF transmitter[d] (max)	–30		dBm
Extinction ratio (min)	3.5		dB
$RIN_{12}OMA$ (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	12		dB
Transmitter Reflectance[e] (max)	–12		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		

[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]TDP is transmitter and dispersion penalty.
[c]Even if the TDP < 1 dB, the OMA(min) must exceed this value.
[d]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut down conditions.
[e]Transmitter reflectance is defined looking into the transmitter.

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52.6.2 10GBASE-L receive optical specifications

The 10GBASE-L receiver shall meet the specifications defined in Table 52–13 per measurement techniques defined in 52.9.

Table 52–13—10GBASE-L receive characteristics

Description	10GBASE-L	Unit
Signaling speed (nominal) 10GBASE-LR 10GBASE-LW	 10.3125 9.95328	GBd
Signaling speed variation from nominal (max)	± 100	ppm
Center wavelength (range)	1260 to 1355	nm
Average receive power[a] (max)	0.5	dBm
Average receive power[b] (min)	–14.4	dBm
Receiver sensitivity (max) in OMA[c]	0.055 (-12.6)	mW (dBm)
Receiver Reflectance (max)	–12	dB
Stressed receiver sensitivity (max) in OMA[d, e]	0.093 (–10.3)	mW (dBm)
Vertical eye closure penalty[f] (min)	2.2	dB
Stressed eye jitter[g] (min)	0.3	UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3	GHz

[a]The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the Average Receive Power (max) plus at least 1 dB.
[b]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[c]Receiver sensitivity is informative.
[d]Measured with conformance test signal at TP3 (see 52.9.9.2) for BER = 10^{-12}.
[e]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effect of CDR circuits.
[f]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[g]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

52.6.3 10GBASE-L link power budgets (informative)

An example power budget and penalties for a 10GBASE-L channel are shown in Table 52–14.

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Table 52–14—10GBASE-L link power budget[a,b]

Parameter	10GBASE-L	Unit
Power budget	9.4	dB
Operating distance	10	km
Channel insertion loss[c, d]	6.2	dB
Allocation for penalties	3.2	dB
Additional insertion loss allowed	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[c]The channel insertion loss is calculated using the maximum distance specified in Table 52–11 and fiber attenuation of 0.4 dB/km at 1310 nm plus an allocation for connection and splice loss given in 52.14.2.1.
[d]A transmitter wavelength of 1260 nm with a TDP of 3 dB is used to calculate channel insertion loss, and allocation for penalties in this table.

52.7 PMD to MDI optical specifications for 10GBASE-E

The operating range for 10GBASE-E PMDs is defined in Table 52–15. A 10GBASE-E compliant PMD supports Types B1.1 and B1.3 single mode fibers according to the specifications defined in 52.14. A PMD which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., operating at 42.5 km meets the minimum range requirement of 2 m to 30 km).

Table 52–15—10GBASE-E operating range

PMD Type	Nominal Wavelength (nm)	Minimum Range
10GBASE-E	1550	2 m to 30 km
		2 m to 40 km[a]

[a]Links longer than 30 km for the same link power budget are considered engineered links. Attenuation for such links needs to be less than the minimum specified for B1.1 or B1.3 single mode fiber.

Link attenuation requirements are specified in 52.14.3.

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52.7.1 10GBASE-E transmitter optical specifications

The 10GBASE-E transmitter shall meet the specifications defined in Table 52–16 per measurement techniques defined in 52.9.

Table 52–16—10GBASE-E transmit characteristics

Description	10GBASE-EW	10GBASE-ER	Unit
Signaling speed (nominal)	9.95328	10.3125	GBd
Signaling speed variation from nominal (max)	± 20	± 100	ppm
Center wavelength (range)	1530 to 1565		nm
Side Mode Suppression Ratio (min)	30		dB
Average launch power (max)	4.0		dBm
Average launch power[a] (min)	–4.7		dBm
Launch power (min) in OMA minus TDP[b]	–2.1		dBm
Average launch power of OFF transmitter[c] (max)	–30		dBm
Optical Modulation Amplitude[d] (min)	–1.7		dBm
Transmitter and dispersion penalty (max)	3.0		dB
Extinction ratio (min)	3		dB
$RIN_{21}OMA$[e] (max)	–128		dB/Hz
Optical Return Loss Tolerance (max)	21		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}		

[a]Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]TDP is transmitter and dispersion penalty.
[c]Examples of an OFF transmitter are: no power supplied to the PMD, laser shutdown for safety conditions, activation of a PMD_global_transmit_disable or other optional transmitter shut-down conditions.
[d]Even if the TDP < 0.4 dB, the OMA(min) must exceed this value.
[e]RIN measurement is made with a return loss at 21 dB.

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52.7.2 10GBASE-E receive optical specifications

The 10GBASE-E receiver shall meet the specifications defined in Table 52–17 per measurement techniques defined in 52.9.

Table 52–17—10GBASE-E receive characteristics

Description	10GBASE-E	Unit
Signaling speed (nominal) 10GBASE-ER 10GBASE-EW	 10.3125 9.95328	GBd
Signaling speed variation from nominal (max)	± 100	ppm
Center wavelength (range)	1530 to 1565	nm
Average receive power (max)	–1.0	dBm
Average receive power[a] (min)	–15.8	dBm
Maximum receive power (for damage)	4.0	dBm
Receiver sensitivity (max) in OMA[b]	0.039 (–14.1)	mW (dBm)
Receiver Reflectance (max)	–26	dB
Stressed receiver sensitivity (max) in OMA[c,d]	0.074 (-11.3)	mW (dBm)
Vertical eye closure penalty[e] (min)	2.7	dB
Stressed eye jitter (min)[f]	0.3	UI pk-pk
Receive electrical 3 dB upper cutoff frequency (max)	12.3	GHz

[a]Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[b]Receiver sensitivity is informative.
[c]Measured with conformance test signal at TP3 (see 52.9.9.2) for BER = 10^{-12}.
[d]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4 dB additional margin be allocated if component level measurements are made without the effects of CDR circuits.
[e]Vertical eye closure penalty is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.
[f]Stressed eye jitter is a test condition for measuring stressed receiver sensitivity. It is not a required characteristic of the receiver.

52.7.3 10GBASE-E link power budgets (informative)

Example power budgets and penalties for a 10GBASE-E channel are shown in Table 52–18.

52.8 Jitter specifications for 10GBASE-R and 10GBASE-W

Acceptable transmitted jitter is achieved by compliance with 52.9.7, transmitter optical waveform, and 52.9.10, transmitter and dispersion penalty. Tolerance to received jitter is achieved by compliance to 52.9.9, stressed receiver conformance, which includes sinusoidal jitter as in the following subclause. There is no jitter transfer specification.

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Table 52–18—10GBASE-E link power budgets[a,b]

Parameter	10GBASE-E		Unit
Power budget	15.0		dB
Operating distance	30	40[c]	km
Channel insertion loss[d, e]	10.9	10.9	dB
Maximum Discrete Reflectance (max)	–26		dB
Allocation for penalties	3.6	4.1	dB
Additional insertion loss allowed	0.5	0.0	dB

[a]Budget numbers are rounded to nearest 0.1 dB.
[b]Link penalties are built into the transmitter specifications by testing the PMD with a maximum dispersion fiber.
[c]Links longer than 30 km are considered engineered links. Attenuation for such links needs to be less than that guaranteed by B1.1 or B1.3 single mode fiber.
[d]Operating distances used to calculate the channel insertion loss are the maximum values specified in Table 52–15
[e]A wavelength of 1565 nm and 3dB transmitter and dispersion penalty (TDP) is used to calculate channel insertion loss, and allocation for penalties.

52.8.1 Sinusoidal jitter for receiver conformance test

The sinusoidal jitter is used to test receiver jitter tolerance. Sinusoidal jitter may vary over a magnitude range as required to accurately calibrate a stressed eye per 52.9.9. The range is limited by the constraints of Table 52–19.

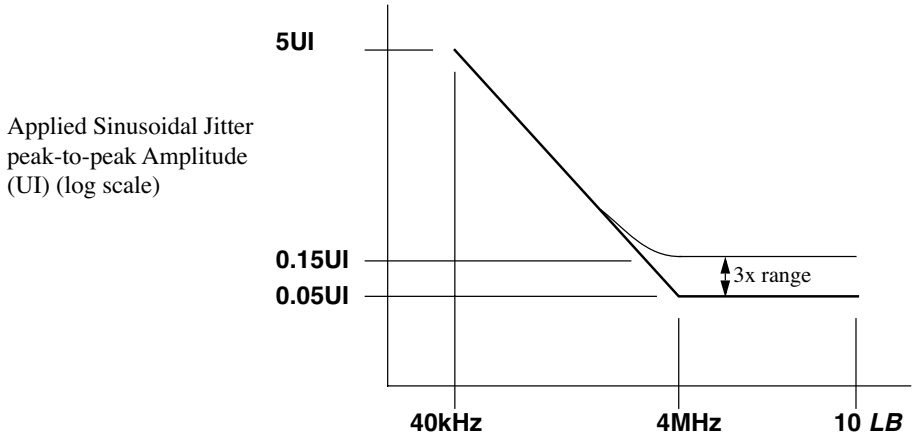


Figure 52–4—Mask of the sinusoidal component of jitter tolerance (informative)

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Table 52–19—Applied Sinusoidal Jitter

Frequency Range	Sinusoidal Jitter ($UI_{pk\ to\ pk}$)
$f < 40$kHz	NA
40 kHz $< f \leq$ 4MHz	$2 \times 10^5 / f + S - 0.05$[a]
4 MHz $< f <$ 10 LB[b]	$0.05 \leq S \leq 0.15$ [a]

[a]S is the magnitude of sine jitter actually used in the calibration of the stressed eye per the methods of 52.9.9.2.
[b]LB = Loop Bandwidth; Upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

52.9 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 and 5 m in length, unless otherwise specified.

52.9.1 Test patterns

Compliance is to be achieved in normal operation. Two types of test pattern are used, square wave (52.9.1.2) and other (52.9.1.1). Test patterns are as in Table 52–22 for 10GBASE-R and in 50.3.8 for 10GBASE-W unless specified otherwise.

NOTE—Test patterns for specific optical tests are designed to emulate system operation, which would entail passing valid 10GBASE-R or 10GBASE-W data.

52.9.1.1 Test-pattern definition

Patterns 1, 2, and 3 are defined in Table 52–21. Pattern 3 is optional.

For 10GBASE-R, two test pattern segments are specified, in two variants, “normal” (n) and “inverted” (i). Both are 8448 bits long. They may be generated dynamically by the 58 bit scrambler and “control block” sync header generation defined in 49.2.6, and using the scrambler starting seeds specified in Table 52–20 and the method of generation in 49.2.8. The segments are assembled into patterns, each containing four segments, as described in Table 52–21. Each may be held as a static pattern in test equipment, or generated or detected dynamically using the methods of 49.2.8 and 49.2.12 respectively, or otherwise.

Each segment contains a sync header transition every 66 bits.

Table 52–20—Pattern segments

Segments	Seed[57:0][a]
A_n	0x3C8B44DCAB6804F
B_n	0x34906BB85A38884

[a]The “invert” segments A_i and B_i are generated using the inverted seeds for A_n and B_n, respectively.

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Table 52–21—Test patterns

Pattern	Pattern for 10GBASE-R	Pattern for 10GBASE-W
1	$B_n B_i B_n B_i$	Mixed[a]
2	$A_n A_i A_n A_i$	
3	PRBS31[b]	PRBS31[c]

[a]The patterns for 10GBASE-W are defined in 50.3.8.
[b]This is the test-pattern checker defined in 49.2.12.
[c]This is the test-pattern checker defined in 50.3.8.2.

The test pattern 1 is generated with the data input mode programmed to select LF data input. The test pattern 2 is generated with the data input mode programmed to select all zero data input.

Pattern 1 represents typical scrambled data while pattern 2 represents a less typical pattern that could happen by chance and is thought to be more demanding of the transmission process including the clock recovery subsystem. Both patterns are balanced over their length of 33 792 bits.

NOTE—While other test methods and patterns could be used it is the implementer's responsibility to ensure that measurements carried out with the specified patterns achieve the requirements specified.

Table 52–22—Test-pattern definitions and related subclauses

Test	Pattern	Related subclause
Average optical power	1 or 3	52.9.3
OMA (modulated optical power)	Square	52.9.5
Extinction ratio	1 or 3	52.9.4
Transmit eye	1 or 3	52.9.7
Receive upper cutoff frequency	1 or 3	52.9.11
$RIN_x OMA$	Square	52.9.6
Wavelength, spectral width	1 or 3	52.9.2
Side mode suppression ratio	1 or 3	—
Vertical eye closure penalty calibration	2 or 3	52.9.9
Receiver sensitivity	1 or 3	52.9.9
Receiver overload	1 or 3	—
Stressed receive conformance	2 or 3	52.9.9
Transmitter and dispersion penalty	2 or 3	52.9.10

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52.9.1.2 Square wave pattern definition

A pattern consisting of four to eleven consecutive ones followed by an equal run of zeros may be used as a square wave. These patterns have fundamental frequencies between approximately 452 MHz (10GBASE-W) and 1289 MHz (10GBASE-R).

52.9.2 Center wavelength and spectral width measurements

The center wavelength and spectral width (RMS) shall be measured using an optical spectrum analyzer per TIA/EIA-455-127 under modulated conditions using an appropriate PRBS or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern.

52.9.3 Average optical power measurements

Average optical power shall be measured using the methods specified in TIA/EIA-455-95. This measurement may be made with the node transmitting test pattern 1 or 3 or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern.

52.9.4 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in ANSI/TIA/EIA-526-4A-1997 [B13]. This parameter is to be assured during system operation. However, measurements with an appropriate PRBS (2^{23} –1 or 2^{31}–1) or a valid 10GBASE-R or 10GBASE-W or OC192c or STM-64 signal will give equivalent results.

52.9.5 Optical modulation amplitude (OMA) test procedure

OMA is the difference in optical power for the nominal “1” and “0” levels of the optical signal, OMA in Figure 52–6, using waveform averaging or histogram means. OMA should be measured for a node transmitting the square wave pattern defined in 52.9.1.

The recommended technique for measuring optical modulation amplitude is illustrated in Figure 52–5. Optionally, a fourth-order Bessel-Thomson filter as specified in 52.9.7 can be used after the O/E converter. The measurement system consisting of the O/E converter, the optional filter and the oscilloscope has the following requirements:

a) The bandwidth of the measurement system shall be at least 3/T where T is the time at high or low (00001111 giving approximately T=400 ps and 7.5 GHz as an example); and
b) The measurement system is calibrated at the appropriate wavelength for the transmitter under test.

With the device under test transmitting the square wave described above, use the following procedure to measure optical modulation amplitude:

a) Configure the test equipment as illustrated in Figure 52–5.
b) Measure the mean optical power P_1 of the logic “1” as defined over the center 20% of the time interval where the signal is in the high state. (See Figure 52–6.)
c) Measure the mean optical power P_0 of the logic “0” as defined over the center 20% of the time interval where the signal is in the low state. (See Figure 52–6.)
d) OMA = $P_1 – P_0$.

A method of approximating OMA is shown in Figure 52–11.

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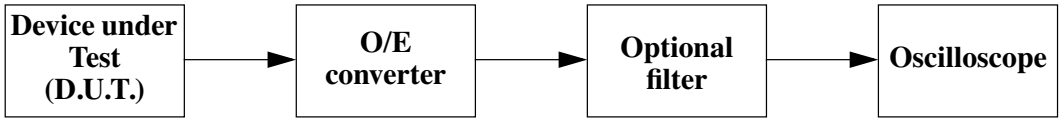


Figure 52–5—Recommended test equipment for measurement of optical modulation amplitude

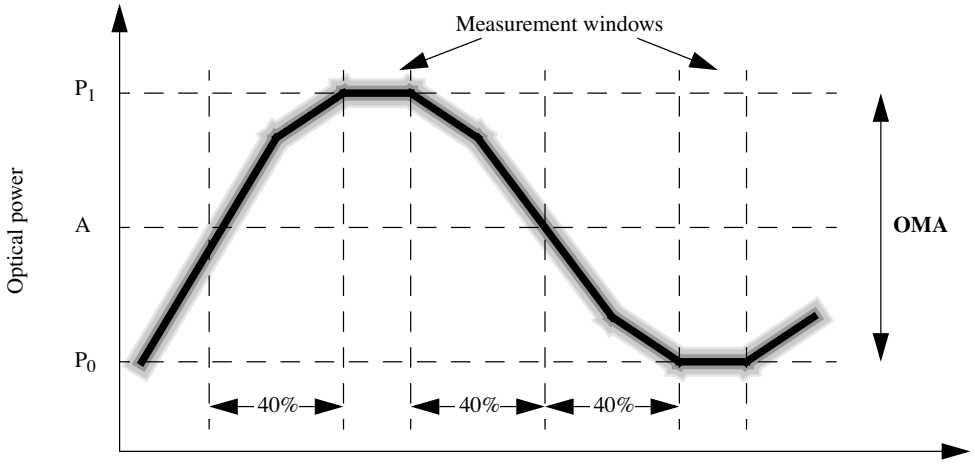


Figure 52–6—Optical modulation amplitude waveform measurement

52.9.6 Relative intensity noise optical modulation amplitude (RIN_xOMA) measuring procedure

This procedure describes a component test that may not be appropriate for a system level test depending on the implementation. If used, the procedure shall be performed as described in 52.9.6.1, 52.9.6.2, and 52.9.6.3.

52.9.6.1 General test description

The test arrangement is shown in Figure 52–7. The optical path between the Device Under Test (DUT) and the detector has a single discrete reflection with the specified optical return loss as seen by the DUT.

Both the OMA power and noise power are measured by AC coupling the O/E converter into the high-frequency electrical power meter. If needed, an amplifier may be used to boost the signal to the power meter. A low pass filter is used between the photodetector and the power meter to limit the noise measured to the passband appropriate to the data rate of interest. In order to measure the noise, the modulation to the DUT is turned off.

52.9.6.2 Component descriptions

Optical Path: The optical path and detector combination must be configured for a single dominant reflection with an optical return loss specified in Table 52–7 for 10GBASE-S, Table 52–12 for 10GBASE-L, and Table 52–16 for 10GBASE-E. (The Optical return loss may be determined by the method of FOTP-107.) The length of the test cable is not critical but should be in excess of 2 m.

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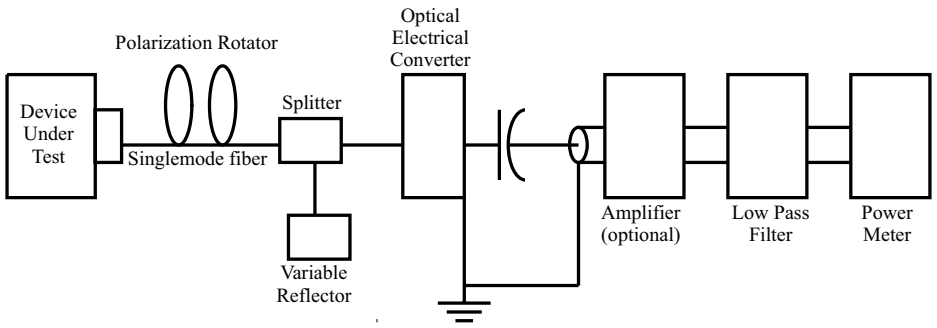


Figure 52–7—RIN$_x$OMA measurement setup

Polarization Rotator: The polarization rotator is required to be capable of transforming an arbitrary orientation elliptically polarized wave into a fixed orientation linearly polarized wave.

O/E converter (and amplifier): If necessary, the noise may be amplified to a level consistent with accurate measurement by the power meter.

Filter: The upper –3 dB limit of the measurement apparatus is to be approximately equal to the bit rate (i.e., 10 GHz). The total filter bandwidth used in the RIN calculation is required to take the low-frequency cutoff of the DC blocking capacitor into consideration. The low-frequency cutoff is recommended to be less than 1 MHz.

The filter should be placed in the circuit as the last component before the power meter so that any high-frequency noise components generated by the detector/amplifier are eliminated. If the power meter used has a very wide bandwidth, care should be taken to ensure that the filter does not lose its rejection at extremely high frequencies.

Power Meter: The RMS electrical power meter should be capable of being zeroed in the absence of input optical power to remove any residual noise.

52.9.6.3 Test Procedure

Use the following procedure to test relative intensity noise optical modulation amplitude:

a) With the DUT disconnected, zero the power meter;
b) Connect the DUT, turn on the laser, and ensure that the laser is not modulated;
c) Operate the polarization rotator while observing the power meter output to maximize the noise read by the power meter. Note the maximum power, P_N;
d) Turn on the modulation to the laser using the square wave pattern of 52.9.1 and note the power measurement, P_M. It may be necessary to change or remove the effective reflection to obtain an accurate reading;
e) Calculate RIN from the observed electrical signal power and noise power by use of Equation (52–1).

$$RIN_xOMA = 10\log\frac{P_N}{BW \times P_M} \text{ (dB/Hz)} \quad (52–1)$$

Where:

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RIN_xOMA= Relative Intensity Noise referred to optical modulation amplitude measured with x dB reflection,

P_N = Electrical noise power in Watts with modulation off,

P_M = Electrical noise power in Watts with modulation on,

BW = Low pass bandwidth of filter – high pass bandwidth of DC blocking capacitor [noise bandwidth of the measuring system (Hz)].

For testing multimode components or systems, the polarization rotator is removed from the setup and the single mode fiber replaced with a multimode fiber. Step c) of the test procedure is eliminated.

52.9.7 Transmitter optical waveform

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 52–8. Compliance is to be assured during system operation. However, measurements with pattern 3 or 1 defined in 52.9.1, or other patterns such as a 2^{23}–1 PRBS or a valid 10GBASE-R, or 10GBASE-W, or OC192c, or STM-64 signal are likely to give very similar results. Measurements should be made as per ANSI/TIA/EIA-526-4A-1997 (OFSTP-4A). Measurement at 10.3125 GBd shall qualify for 10GBASE-W and 10GBASE-R use, measurement at 9.95328 GBd shall qualify for 10GBASE-W use only.

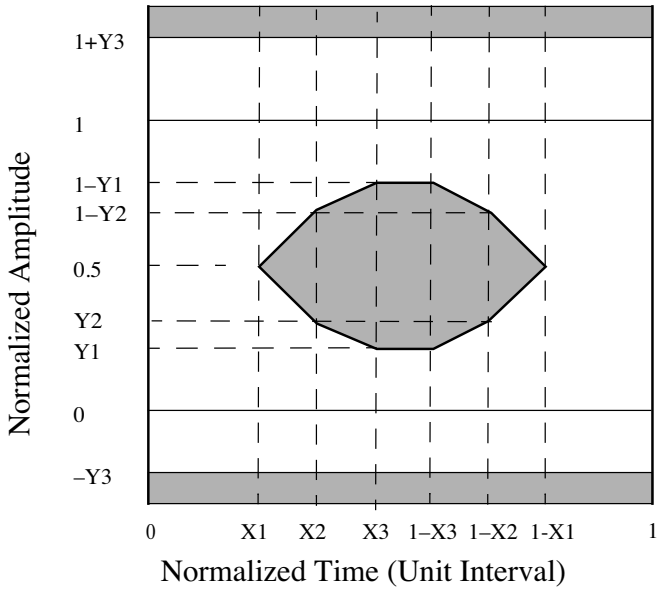


Figure 52–8—Transmitter eye mask definition

Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE respectively. Normalized times of 0 and 1 on the unit interval scale are to be determined by the eye crossing means measured at the average value of the optical eye pattern.

A clock recovery unit (CRU) should be used to trigger the scope for mask measurements as shown in Figure 52–9. It should have a high-frequency corner bandwidth of less than or equal to 4 MHz and a slope of –20 dB/decade.

The eye shall be measured with respect to the mask of the eye using a receiver with a fourth-order Bessel-Thomson response having a transfer function given by Equation (52-2) and Equation (52-3):

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$$H(y) = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4} \quad (52–2)$$

where:

$$y = 2.114p\ ; \quad p = \frac{j\omega}{\omega_r}\ ; \quad \omega_r = 2\pi f_r\ ; \quad f_r = 7.5GHz \quad (52–3)$$

and where the filter response vs. frequency range for this fourth-order Bessel-Thomson receiver is defined in ITU-T G.691, 2000, along with the allowed tolerances for its physical implementation.

This Bessel-Thomson receiver is not intended to represent the noise filter used within a compliant optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

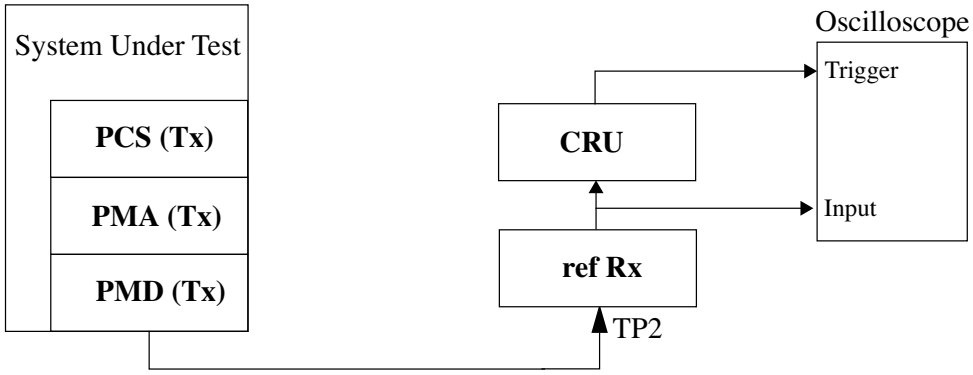


Figure 52–9—Transmitter optical waveform test block diagram

The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

52.9.8 Receiver sensitivity measurements

Receiver sensitivity, which is defined for an ideal input signal, is informative and testing is not required. If measured, the test signal should have negligible impairments such as intersymbol interference (ISI), rise/fall times, jitter and RIN. Instead, the normative requirement for receivers is stressed receiver sensitivity. Stressed sensitivity is measured with a conditioned input signal where both vertical eye closure and jitter have been added according to 52.9.9.

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52.9.9 Stressed receiver conformance test

Stressed receiver tolerance testing shall be performed in accordance with the requirements of 52.9.9.1, 52.9.9.2, and 52.9.9.3.

Receivers must operate with BER less than 10^{-12} when tested with a conditioned input signal that combines vertical eye closure and jitter according to this clause.

The measurements in this subclause are performed with asynchronous data flowing out of the optical transmitter of the system under test. The output data pattern from the transmitter of the system under test is to be the same pattern defined for this measurement in 52.9.1.

52.9.9.1 Stressed receiver conformance test block diagram

A block diagram for the receiver conformance test is shown in Figure 52–10. A suitable pattern generator is used to continuously generate a signal or test pattern according to 52.9.1. The optical test signal is conditioned (stressed) using the methodology, as defined in 52.9.9.2, while applying sinusoidal jitter, as defined in 52.8.1. The receiver of the system under test is tested for conformance by enabling the error counter on the receiving side. As defined in section 49.2.12 and 50.3.8, the PCS or WIS is capable of detecting the data pattern and reporting any errors received. The optical power penalty for the stressed eye is intended to be similar to its vertical eye closure penalty. This is not necessarily the same as the highest TDP anticipated in service, but represents a standardized test condition for the receiver.

A suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. The test fiber called out for LW/LR and EW/ER and the transversal filter called out for SW/SR are not needed to characterize the receiver input signal; nor are they used during testing.

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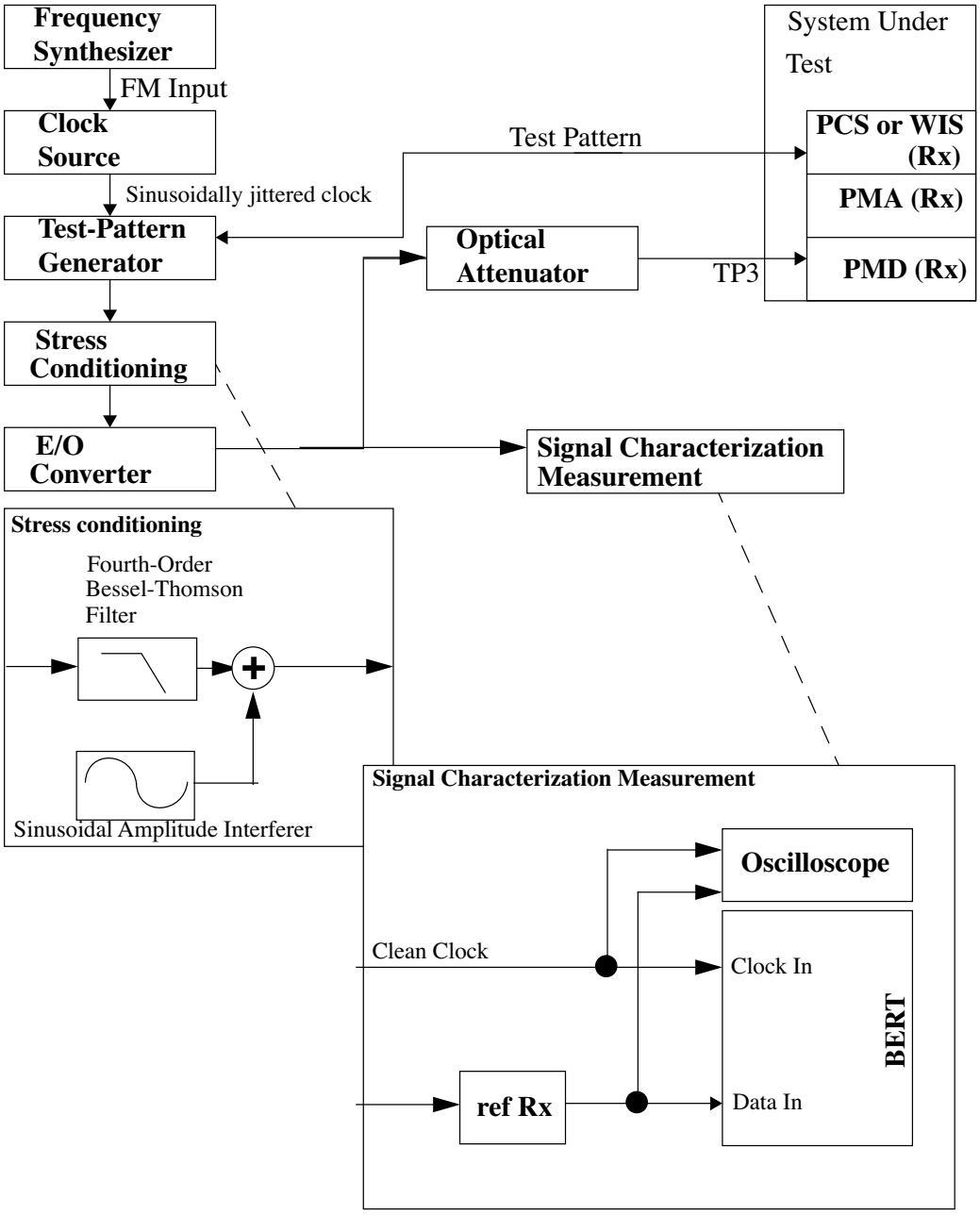


Figure 52–10—Stressed receiver conformance test block diagram

The fourth-order Bessel-Thomson filter is used to create ISI-induced vertical eye closure penalty (VECP). The sinusoidal amplitude interferer causes additional eye closure, but in conjunction with the slowed edge rates from the filter, also causes jitter. The nature of the jitter is intended to emulate instantaneous bit shrinkage that can occur with DDJ. This type of jitter cannot be created by simple phase modulation. The

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sinusoidal phase modulation represents other forms of jitter and also verifies that the receiver under test can track low-frequency jitter.

For improved visibility for calibration, it is imperative that the Bessel-Thomson filter and all other elements in the signal path (cables, DC blocks, E/O converter, etc.) have wide and flat frequency response and linear phase response throughout the spectrum of interest. Baseline wander and overshoot and undershoot should be minimized. If this is achieved, then data dependent effects should be minimal, and short data patterns can be used for calibration with the benefit of providing much improved trace visibility on sampling oscilloscopes. Actual patterns for testing the receiver shall be as specified in Table 52–22.

To further improve visibility for calibration, random noise effects, such as RIN and random clock jitter, should also be minimized. A small amount of residual noise and jitter from all sources is unavoidable, but should be less than 0.25 UI peak-peak of jitter.

The Bessel-Thomson filter should have the appropriate frequency response to result in the appropriate level of initial ISI eye closure before the sinusoidal terms are added. The E/O converter should be fast and linear such that the waveshape and edge rates are predominantly controlled or limited by the electrical circuitry. Electrical summing requires high linearity of all elements including the E/O modulator. Summing with an optical coupler after the modulator is an option that eases linearity requirements, but requires a second source for the interfering signal, will complicate settings of extinction ratio, and will add more RIN.

The vertical and horizontal eye closures to be used for receiver conformance testing are verified using an optical reference receiver with a 7.5 GHz fourth order ideal Bessel-Thomson response. Use of G.691 tolerance filters may significantly degrade this calibration. Care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator and the optical coupler, if used.

The clock output from the clock source in Figure 52–10 will be modulated with the sinusoidal jitter. To use an oscilloscope to calibrate the final stressed eye jitter that includes the sinusoidal jitter component, a separate clock source (clean clock of Figure 52–11) is required that is synchronized to the source clock, but not modulated with the jitter source.

52.9.9.2 Stressed receiver conformance test signal characteristics and calibration

The conformance test signal is used to validate that the PMD receiver meets BER requirements with near worst case waveforms including pulse width shrinkage, power, simulated channel penalties, and a swept frequency sinusoidal jitter contribution applied at TP3.

Signal characteristics are described below along with a suggested approach for calibration.

The test signal includes vertical eye closure and high-probability jitter components. For this test, these two components are defined by peak values that include all but 0.1% for VECP and all but 1% for jitter of their histograms. Histograms should include at least 10 000 hits, and should be about 1%-width in the direction not being measured. Residual low-probability noise and jitter should be minimized—that is, the outer slopes of the final histograms should be as steep as possible down to very low probabilities.

The following steps describe a suggested method for calibrating a stressed eye generator:

1) Set the signalling speed of the test-pattern generator to satisfy the requirements of 52.5.2, 52.6.2, or 52.7.2.
2) Turn on the calibration pattern. A short pattern may be used for calibration if the conditions described in 52.9.9.1 are met, but increases the risk that the longer test pattern used during testing will overstress the device under test. In any case, a pattern shorter than PRBS10 is not recommended.

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3) Set the extinction ratio to approximately the Extinction Ratio (min) value given in 52.5.1, 52.6.1, or 52.7.1. Sinusoidal interference and jitter signals should be turned off at this point. If optical summing is used, ER may need to be adjusted after the sinusoidal interference signal is added below.
4) Measure the OMA of the test signal (without attenuation). OMA is measured per the method in 52.9.5 using the square wave pattern.
5) The requirements for vertical eye closure and jitter of the stressed eye test signal are given by the Vertical eye closure penalty (VECP) and Stressed eye jitter (J) values given in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, or Table 52–17 for 10GBASE-E. Vertical closure is measured at the time center of the eye (halfway between 0 and 1 on the unit interval scale as defined in 52.9.7) and is the vertical eye closure penalty when calculated relative to the measured OMA value. J is measured at the average optical power, which can be obtained with AC coupling. The values of these components are defined as above by their histogram results.

   The vertical eye closure penalty is given by Equation (52–4).

$$\text{Vertical eye closure penalty [dB, optical]} = 10 \times \log \frac{OMA}{A_O} \tag{52–4}$$

   where, A_O is the amplitude of the eye opening and OMA is the normal amplitude without ISI, as shown in Figure 52–11.

   There are three components involved in calibration for vertical closure and J. These are a linear phase filter, sinusoidal interference, and sinusoidal jitter.

   Without sinusoidal jitter or sinusoidal interference, greater than two thirds of the vertical eye closure penalty value should be created by use of a linear phase, low jitter filter (such as Bessel-Thomson). The filter should be tested with the prescribed test patterns to verify that residual jitter and baseline wander are small, not to exceed 0.25 UI peak-peak. If not, the stress may be more than desired, leading to conservative results. However, compensation is not allowed. Once done, revert to the calibration pattern, if different than the final test pattern specified in Table 52–22.

   Any remaining vertical eye closure required must be created with sinusoidal interference or sinusoidal jitter.

   The frequency of the sinusoidal interference may be set at any frequency between 100 MHz and 2 GHz, although be careful to avoid a harmonic relationship between the sinusoidal interference, the sinusoidal jitter, the data rate and the pattern repetition rate.

   Sinusoidal jitter (phase modulation) must be added per the template of Table 52–19. For calibration purposes, sinusoidal jitter frequencies must be well within the flat portion of the template greater than 4 MHz.

   Iterate the settings for sinusoidal interference and/or jitter until all constraints are met, including jitter (J), vertical closure (VECP), and that sinusoidal jitter above 4 MHz is as specified in Table 52–19.

   Verify that the optical power penalty for the stressed eye (relative to the reference transmitter per 52.9.10) is greater than or equal to VECP.

   If high linearity exists, then the sinusoidal interference should not change the OMA value. OMA can be approximated with histograms as suggested in Figure 52–11. However, the

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normative definition for OMA is as given in 52.9.5.

To emulate the effects of DCD or data-dependent jitter, at least 5 ps peak-peak of pulse shrinkage jitter should have been achieved.

6) Decrease the amplitude with the optical attenuator until the OMA complies with the OMA values given in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, Table 52–17 for 10GBASE-E.

7) For testing, turn on the actual required test pattern(s) per 52.9.1.

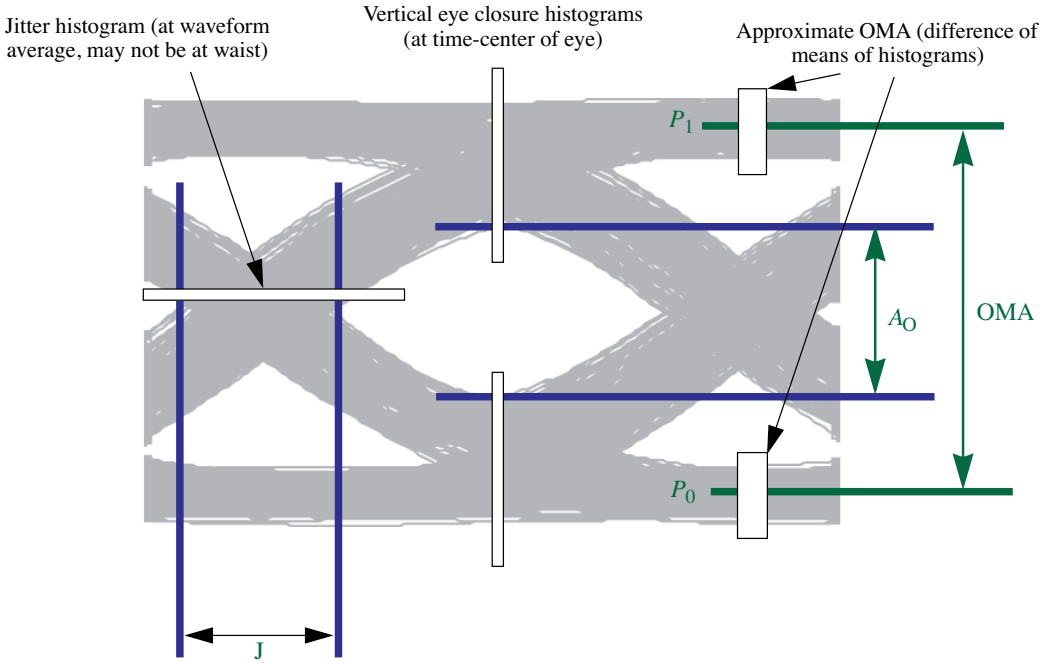


Figure 52–11—Required characteristics of the conformance test signal at TP3

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative impact on yield but will not effect interoperability. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize and/or correct for the noise/jitter introduced by the reference receiver, filters, oscilloscope, and BERT. While the details of measurement and test equipment are beyond the scope of this standard it is recommended that the implementer fully characterize their test equipment and apply appropriate guard bands to ensure that the receive input signal meets the specified requirements.

52.9.9.3 Stressed receiver conformance test procedure

The test apparatus is set up as described in 52.9.9.1 and 52.9.9.2. The sinusoidal jitter is then stepped across the frequency and amplitude range specified in 52.8.1 while monitoring BER at the receiver. The BER is to be compliant at all frequencies in the specified frequency range. This method does not result in values for jitter contributed by the receiver. It does, however, guarantee that a receiver meeting the requirements of this test will operate with the worst-case optical input.

The value for sinusoidal jitter must be met at all test frequencies.

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52.9.10 Transmitter and dispersion penalty measurement

The setup for measurement of transmitter and dispersion penalty is shown in Figure 52–12 and consists of a reference transmitter, the transmitter under test, a controlled optical reflection, an optical attenuator, a test fiber, a reference receiver, a transversal filter for 10GBASE-S, and a bit-error rate tester. All BER and sensitivity measurements are made with the test patterns in 52.9.1.

52.9.10.1 Reference transmitter requirements

The reference transmitter is a high-quality instrument-grade device, which can be implemented by a CW laser modulated by a high-performance modulator. It should meet the following basic requirements:

a) The rise/fall times should be less than 30ps at 20% to 80%.
b) The output optical eye is symmetric and passes the eye mask test of 52.9.7.
c) In the center 20% region of the eye, the worst case vertical eye closure penalty as defined in 52.9.9.2 is less than 0.5 dB.
d) Jitter less than 0.20 UI peak-peak.
e) RIN should be minimized to less than–136 dB/Hz

52.9.10.2 Channel requirements

The transmitter is tested using an optical channel that meets the requirements listed in Table 52–23.

Table 52–23—Transmitter compliance channel specifications

PMD Type	Dispersion[a] (ps/nm)		Insertion loss[b]	Optical return loss[c] (max)
	Minimum	Maximum		
10GBASE-S	N/A	N/A	Minimum	See ORLT in Table 52–7
10GBASE-L	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	21 dB
10GBASE-E	0 (maximum)	$0.93 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	Minimum	See ORLT in Table 52–16

[a]The dispersion is measured for the wavelength of the device under test. The coefficient assumes 10 km for 10GBASE-L and 40 km for 10GBASE-E.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The optical return loss is applied at TP2.

A 10GBASE-L/E transmitter is to be compliant with a total dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns specified in Table 52–23 for the wavelength of the device under test. This may be achieved with channels consisting of fibers with lengths chosen to meet the dispersion requirements.

To verify that the fiber has the correct amount of dispersion, the measurement method defined in ANSI/TIA/EIA-455-175A-92 may be used. The measurement is made in the linear power regime of the fiber.

The channel for 10GBASE-S is a 2 to 5 m patch cord meeting the requirements in Table 52–25.

The channel provides a maximum optical return loss specified in Table 52–23. The state of polarization of the back reflection is adjusted to create the greatest RIN. The methods of 52.9.6.2 and 52.9.6.3 may be used.

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52.9.10.3 Test receiver requirements

The reference receiver should have the bandwidth given in 52.9.7. The sensitivity of the reference receiver should be limited by Gaussian noise. The receiver should have minimal threshold offset, deadband, hysteresis, baseline wander, deterministic jitter or other distortions. Decision sampling should be instantaneous with minimal uncertainty and setup/hold properties.

The nominal sensitivity of the reference receiver, S, is measured in OMA using the set up of Figure 52–12 without the test fiber and with the transversal filter removed. The sensitivity S must be corrected for any significant reference transmitter impairments including any vertical eye closure. It should be measured while sampling at the eye center or corrected for off-center sampling. It is calibrated at the wavelength of the transmitter under test.

For all transmitter and dispersion penalty measurements, determination of the center of the eye is required. Center of the eye is defined as the time halfway between the left and right sampling points within the eye where the measured BER is greater than or equal to 1×10^{-3}.

For 10GBASE-S the reference receiver is followed by a transversal filter with two equal amplitude paths with a differential delay of 55ps. For 10GBASE-L/E the transversal filter is not used.

The clock recovery unit (CRU) used in the TDP measurement has a corner frequency of less than or equal to 4 MHz and a slope of 20dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.

52.9.10.4 Test procedure

To measure the transmitter and dispersion penalty (TDP) the following procedure shall be used. The decision threshold amplitude is defined to occur at the average signal level. The sampling instant is displaced from the eye center by ± 0.05 UI. The following procedure is repeated for early and late decision and the larger TDP value is used:

a) Configure the test equipment as described above and illustrated in Figure 52–12.
b) Adjust the attenuation of the optical attenuator to obtain a BER of 1×10^{-12}.
c) Record the optical power in OMA at the input to the test receiver, P_DUT, in dBm.
d) If P_DUT is larger than S, the transmitter and dispersion penalty (TDP) for the transmitter under test is the difference between P_DUT and S, TDP = P_DUT – S. Otherwise the transmitter and dispersion penalty is zero, TDP = 0.

It is to be ensured that the measurements are made in the linear power regime of the fiber.

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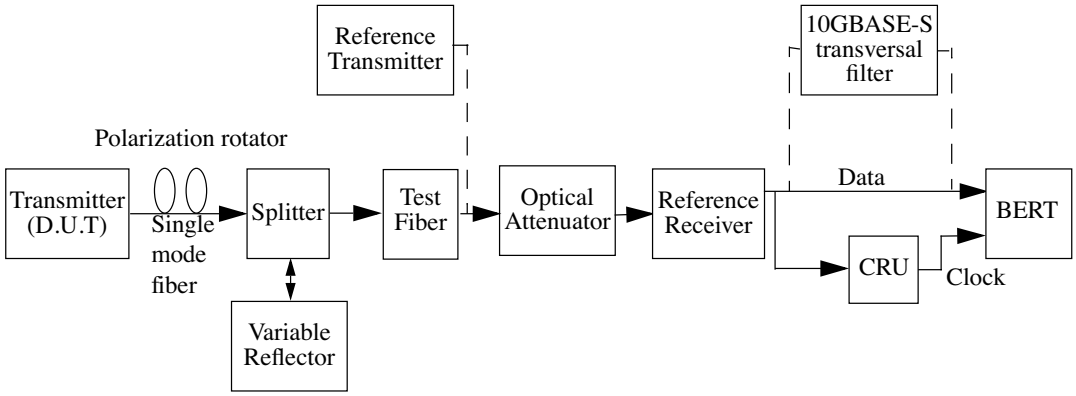


Figure 52–12—Test setup for measurement of transmitter and dispersion penalty

52.9.11 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver 3 dB electrical upper cutoff frequency may be measured as described in Figure 52–13 and the list below. The test setup is shown in Figure 52–13. The test uses two optical sources and an optical combiner. One source is modulated by a digital data signal. The other, approximately linear, source is modulated with an analog signal. The analog and digital signals should be asynchronous. The recommended patterns are test patterns 1 or 3 of 52.9.1. An appropriate PRBS or a valid 10GBASE-R or 10GBASE-W signal, OC-192 signal, STM-64 signal, or another representative test pattern may be used.

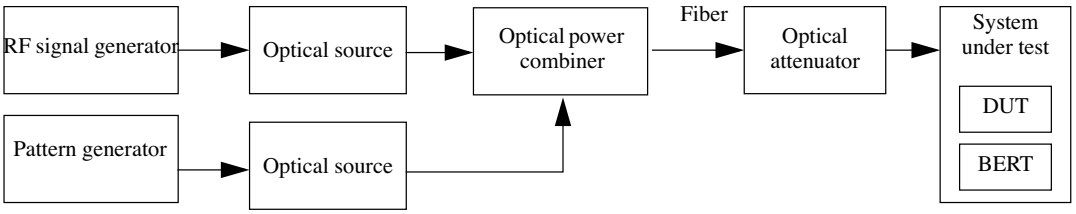


Figure 52–13—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency may be measured using the following steps:

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator and laser sources. The digital optical source meets the requirements of this clause.
b) Configure the test equipment as shown in Figure 52–13. Take care to minimize changes to the signal path which could affect the system frequency response after the calibration in step a. With the RF modulation turned off, and both optical sources turned on, set the Optical Modulation Amplitude to a level that approximates the stressed receiver sensitivity level in Table 52–9 for 10GBASE-S, Table 52–13 for 10GBASE-L, and Table 52–17 for 10GBASE-E.
c) Turn on the RF modulation while maintaining the same average optical power and OMA established in step b).
d) Measure the necessary RF modulation amplitude (in electrical dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.

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e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical).

52.10 Environmental specifications

52.10.1 General safety

All equipment meeting this standard shall conform to IEC-60950: 1991.

52.10.2 Laser safety

10GBASE-R and 10GBASE-W optical transceivers shall conform to Class 1 laser requirements as defined in the IEC 60825-1: 2001, under any condition of operation. This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation is required to explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[16]

52.10.3 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

52.11 Environment

Normative specifications in this clause shall be met by a system integrating a 10GBASE-R or 10GBASE-W over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

52.11.1 Electromagnetic emission

A system integrating a 10GBASE-R or 10GBASE-W PMD shall comply with applicable local and national codes for the limitation of electromagnetic interference.

[16]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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52.11.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

52.12 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user, with at least the applicable safety warnings and the applicable port type designation (e.g., 10GBASE-ER)

Labeling requirements for Class 1 lasers are given in the laser safety standards referenced in 52.10.2.

52.13 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 52–14.

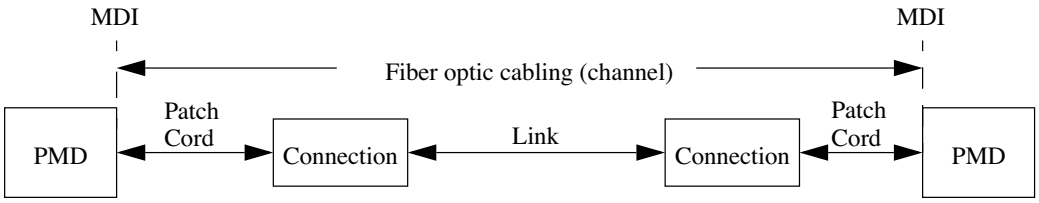


Figure 52–14—Fiber optic cabling model

The channel insertion loss is given in Table 52–24. A channel may contain additional connectors or other optical elements as long as the optical characteristics of the channel, such as attenuation, dispersion, reflections, polarization mode dispersion and modal bandwidth meet the specifications. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-14A/method B, and ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

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Table 52–24—Fiber optic cabling (channel)

Description	62.5 μm MMF		50 μm MMF			Type B1.1, B1.3 SMF			Unit
Nominal wavelength	**850[a]**					**1310[b]**	**1550**		**nm**
Modal bandwidth (min)	**160**	**200**	**400**	**500**	**2000**	**N/A**	**N/A**		**MHz•km**
Operating distance (max)	26 m	33 m	66 m	82 m	300 m	10 km	30 km	40 km	
Channel insertion loss (max) [c,d,e]	2.6	2.5	2.2	2.3	2.6	6.0	11.0[f]		dB
Channel insertion loss (min)	0	0	0	0	0	0	5		dB
Dispersion (max)	N/A	N/A	N/A	N/A	N/A	N/A	546	728	ps/nm
DGD_max[g]	N/A	N/A	N/A	N/A	N/A	10	19		ps
Optical return loss	N/A	N/A	N/A	N/A	N/A	N/A	21		dB

[a]Channel insertion loss at 850 nm includes cable, connectors, and splices.
[b]Channel insertion loss at 1310 nm includes cable, connectors, and splices.
[c]These channel insertion loss numbers are based on the nominal wavelength.
[d]Operating distances used to calculate channel insertion loss are those listed in this table.
[e]Maximum attenuation given in Table 52–25.
[f]Channel insertion loss at 1550 nm includes cable, connectors and splices.
[g]Differential Group Delay (DGD) is the time difference between the fractions of a pulse that are transmitted in the two principal states of polarization of an optical signal. DGD_max is the maximum differential group delay that the system must tolerate.

52.14 Characteristics of the fiber optic cabling (channel)

The 10GBASE-R and 10GBASE-W fiber optic cabling shall meet the specifications defined in Table 52–24. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together.

52.14.1 Optical fiber and cable

The fiber optic cable shall meet the requirements of IEC 60793-2 and the requirements of Table 52–25 where they differ for fiber types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), B1.1 (dispersion un-shifted single mode), or B1.3 (low water peak single mode).

NOTE—It is believed that for 10GBASE-E, type B4 fiber with positive dispersion may be substituted for B1.1 or B1.3. A link using B4 fiber with negative dispersion should be validated for compliance at TP3.

52.14.2 Optical fiber connection

An optical fiber connection, as shown in Figure 52–14, consists of a mated pair of optical connectors.

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Table 52–25—Optical fiber and cable characteristics

Description	62.5 μm MMF	50 μm MMF	Type B1.1, B1.3 SMF		Unit
Nominal fiber specification wavelength	**850**	**850**	**1310**	**1550**	**nm**
Fiber cable attenuation (max)	3.5	3.5	0.4[a] or 0.5[b]	see footnote[c]	dB/km
Modal Bandwidth (min)	160[d] or 200[d]	400[d] or 500[d] or 2000[e]	N/A		MHz km
Zero dispersion wavelength (λ_0)	$1320 \le \lambda_0 \le 1365$	$1295 \le \lambda_0 \le 1320$	$1300 \le \lambda_0 \le 1324$		nm
Dispersion slope (max) (S_0)	0.11 for $1320 \le \lambda_0 \le 1348$ and $0.001(1458-\lambda_0)$ for $1348 \le \lambda_0 \le 1365$	0.11 for $1300 \le \lambda_0 \le 1320$ and $0.001(\lambda_0-1190)$ for $1295 \le \lambda_0 \le 1300$	0.093		ps / nm^2 km

[a]For the single mode case, the 0.4 dB/km attenuation for optical fiber cables is defined in ITU-T G.652.
[b]For the single mode case, the 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA/EIA 568B.3-2000. Using 0.5 dB/km may not support operation at 10 km.
[c]Attenuation for 1550 nm links is based on the fiber channel and is specified in 52.14.3.
[d]Overfilled launch bandwidth per IEC 60793-1-41 or ANSI/TIA/EIA 455-204-2000.
[e]Effective modal bandwidth for fiber meeting TIA/EIA-492AAAC-2002 when used with sources meeting the wavelength (range) and encircled flux specifications of Table 52–7.

52.14.2.1 Connection insertion loss

The insertion loss is specified for a connection, which consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an insertion loss equal to 0.5 dB (or less) per connection, or two connections (as shown in Figure 52–14) with an insertion loss of 0.75 dB per connection. Connections with different loss characteristics may be used provided the requirements of Table 52–24 are met.

The maximum link distances for single mode fiber are calculated based on an allocation of 2 dB total connection and splice loss at 1310 nm for 10GBASE-L, and 2 dB for 30 km total connection and splice loss at 1550 nm for 10GBASE-E.

52.14.2.2 Maximum discrete reflectance

The Maximum discrete reflectance for 10GBASE-S shall be less than –20 dB.

The Maximum discrete reflectance for 10GBASE-L and 10GBASE-E shall be less than –26 dB.

52.14.3 10GBASE-E attenuator management

The 10GBASE-E channel shall have an attenuation between 5 and 11 dB. If required, an attenuator can be added to comply with this specification. The ideal channel attenuation is 8 dB. Figure 52–15 graphically shows the compliant region.

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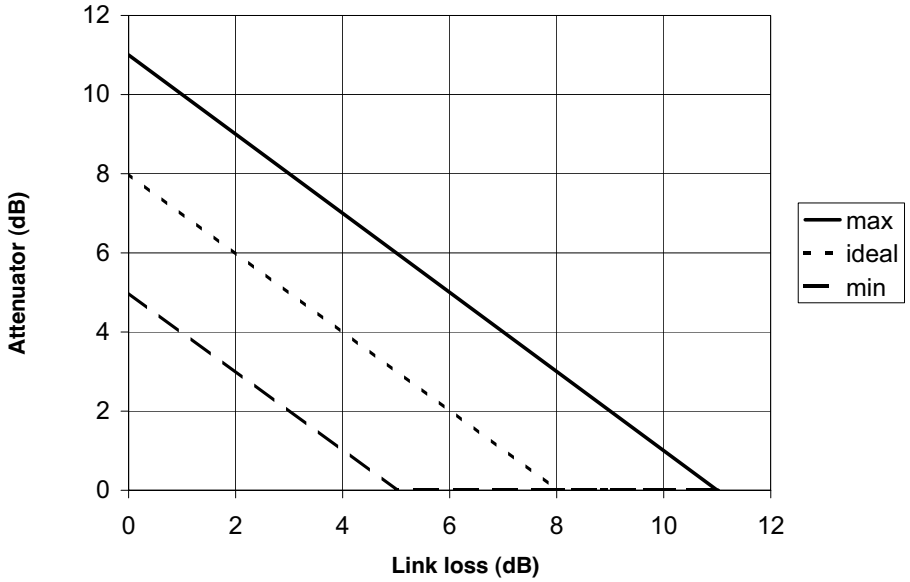


Figure 52–15—10GBASE-E attenuator management (informative)

52.14.4 Medium Dependent Interface (MDI) requirements

The 10GBASE-R and 10GBASE-W PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the "fiber optic cabling" (as shown in Figure 52–14). Examples of an MDI include the following:

a) Connectorized fiber pigtail;
b) PMD receptacle.

When the MDI is a connector plug and receptacle connection, it shall meet the interface performance specifications of the following:

a) IEC 61753-1-1—Fibre optic interconnecting devices and passive component performance standard—Part 1-1: General and guidance—Interconnecting devices (connectors);
b) IEC 61753-021-2—Fibre optic passive components performance standard—Part 021-2: Fibre optic connectors terminated on single mode fibre for Category C—Controlled environment;
c) IEC 61753-022-2—Fibre optic passive components performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for Category C—Controlled environment.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in 52.4.1, not at the MDI.

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52.15 Protocol Implementation Conformance Statement (PICS) proforma for Clause 52, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-S (Short Wavelength Serial), 10GBASE-L (Long Wavelength Serial), and 10GBASE-E (Extra Long Wavelength Serial)[17]

52.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-R and 10GBASE-W, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

52.15.2 Identification

52.15.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

52.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 52, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-R and 10GBASE-W
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[17] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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52.15.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*MD	MDIO capability	52.3	Registers and interface supported	O	Yes [ ] No [ ]
*SR	10GBASE-SR PMD	52.5	Device supports shortwave (850 nm) operation LAN PHY	O	Yes [ ] No [ ]
*LR	10GBASE-LR PMD	52.6	Device supports longwave (1310 nm) operation LAN PHY	O	Yes [ ] No [ ]
*ER	10GBASE-ER PMD	52.7	Device supports extra long wave (1550 nm) operation LAN PHY	O	Yes [ ] No [ ]
*SW	10GBASE-SW PMD	52.5	Device supports shortwave (850 nm) operation WAN PHY	O	Yes [ ] No [ ]
*LW	10GBASE-LW PMD	52.6	Device supports longwave (1310 nm) operation WAN PHY	O	Yes [ ] No [ ]
*EW	10GBASE-EW PMD	52.7	Device supports extra long wave (1550 nm) operation WAN PHY	O	Yes [ ] No [ ]
*INS	Installation / Cable	52.4.1	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
DLY	Delay constraints	52.2	Device conforms to delay constraints	M	Yes [ ]

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52.15.3 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, types 10GBASE-R and 10GBASE-W

52.15.3.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	52.4.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter optical signal	52.4.2	Higher optical power transmitted is a logic 1	M	Yes [ ]
FS3	Receive function	52.4.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver optical signal	52.4.3	Higher optical power received is a logic 1	M	Yes [ ]
FS5	Signal detect function	52.4.4	Mapping to PMD service interface	M	Yes [ ]
FS6	Signal detect parameter	52.4.4	Generated according to Table 52–5	M	Yes [ ]

52.15.3.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MD1	Management register set	52.3	Mapped as per Table 52–3 and Table 52–4	MD:M	Yes [ ] N/A [ ]
MD2	PMD_reset bit	52.4.5	As defined in 45.2.1.1.1	MD:M	Yes [ ] N/A[ ]
MD3	PMD_global_transmit_disable bit	52.4.7	As defined in 45.2.1.8.5	MD:O	Yes [ ] No [ ] N/A [ ]
MD4	PMD_transmit_fault bit	52.4.8	As defined in 45.2.1.7.4	MD:O	Yes [ ] No [ ] N/A [ ]
MD5	PMA/PMD receive fault bit	52.4.9	Contributes to receive fault bit as defined in 45.2.1.7.5	MD:O	Yes [ ] No [ ] N/A [ ]
MD6	PMD_signal_detect bit	52.4.4	As defined in 45.2.1.9.5	MD:M	Yes [ ] N/A [ ]

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52.15.3.3 PMD to MDI optical specifications for 10GBASE-SR

Item	Feature	Subclause	Value/Comment	Status	Support
SR1	10GBASE-SR transmitter	52.5.1	Meets specifications in Table 52–8 and Table 52–7	SR:M	Yes [ ] N/A [ ]
SR2	10GBASE-SR receiver	52.5.2	Meets specifications in Table 52–9	SR:M	Yes [ ] N/A [ ]

52.15.3.4 PMD to MDI optical specifications for 10GBASE-SW

Item	Feature	Subclause	Value/Comment	Status	Support
SW1	10GBASE-SW transmitter	52.5.1	Meets specifications in Table 52–8 and Table 52–7	SW:M	Yes [ ] N/A [ ]
SW2	10GBASE-SW receiver	52.5.2	Meets specifications in Table 52–9	SW:M	Yes [ ] N/A [ ]

52.15.3.5 PMD to MDI optical specifications for 10GBASE-LR

Item	Feature	Subclause	Value/Comment	Status	Support
LR1	10GBASE-LR transmitter	52.6.1	Meets specifications in Table 52–12	LR:M	Yes [ ] N/A [ ]
LR2	10GBASE-LR receiver	52.6.2	Meets specifications in Table 52–13	LR:M	Yes [ ] N/A [ ]

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52.15.3.6 PMD to MDI optical specifications for 10GBASE-LW

Item	Feature	Subclause	Value/Comment	Status	Support
LW1	10GBASE-LW transmitter	52.6.1	Meets specifications in Table 52–12	LW:M	Yes [ ] N/A [ ]
LW2	10GBASE-LW receiver	52.6.2	Meets specifications in Table 52–13	LW:M	Yes [ ] N/A [ ]

52.15.3.7 PMD to MDI optical specifications for 10GBASE-ER

Item	Feature	Subclause	Value/Comment	Status	Support
ER1	10GBASE-ER transmitter	52.7.1	Meets specifications in Table 52–16	ER:M	Yes [ ] N/A [ ]
ER2	10GBASE-ER receiver	52.7.2	Meets specifications in Table 52–17	ER:M	Yes [ ] N/A [ ]

NOTE— Link attenuation requirements are specified in 52.14.3.

52.15.3.8 PMD to MDI optical specifications for 10GBASE-EW

Item	Feature	Subclause	Value/Comment	Status	Support
EW2	10GBASE-EW transmitter	52.7.1	Meets specifications in Table 52–16	EW:M	Yes [ ] N/A [ ]
EW2	10GBASE-EW receiver	52.7.2	Meets specifications in Table 52–17	EW:M	Yes [ ] N/A [ ]

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52.15.3.9 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Measurement cable	52.9	2 to 5 meters in length	M	Yes [ ]
OM2	Center wavelength and spectral width measurement	52.9.2	Measured using an optical spectrum analyzer per TIA/EIA-455-127 under modulated conditions	M	Yes [ ]
OM3	Average optical power	52.9.3	Measured using the methods specified in TIA/EIA-455-95	M	Yes [ ]
OM4	Extinction ratio	52.9.4	Measured using the methods specified in ANSI/TIA/EIA-526-4A-1997 [B13]	M	Yes [ ]
OM5	OMA measurement bandwidth	52.9.5	At least 3/T	M	Yes [ ]
OM6	RIN_xOMA measurement procedure	52.9.6	As described in 52.9.6.1, 52.9.6.2, and 52.9.6.3	M	Yes [ ]
OM7	Transmit eye	52.9.7	10.3125 GBd shall qualify for 10GBASE-W and 10GBASE-R use, measurement at 9.95328 GBd shall qualify for 10GBASE-W use only	M	Yes [ ]
OM8	Stressed receiver conformance test	52.9.9	Performed in accordance with the requirements of 52.9.9.1, 52.9.9.2, and 52.9.9.3	M	Yes [ ]
OM9	Transmitter and dispersion penalty measurement	52.9.10.4		M	Yes [ ]

52.15.3.10 Characteristics of the fiber optic cabling and MDI

Item	Feature	Subclause	Value/Comment	Status	Support
FO1	Fiber optic cabling	52.14	Specified in Table 52–24	INS:M	Yes [ ] N/A [ ]
FO2	Optical fiber characteristics	52.14.1	Meet the requirements of IEC 60793-2 and the requirements of Table 52–25	INS:M	Yes [ ] N/A [ ]
FO3	Maximum discrete reflectance-multimode fiber	52.14.2.2	Less than –20 dB	INS:M	Yes [ ] N/A [ ]
FO4	Maximum discrete reflectance - singlemode fiber	52.14.2.2	Less than –26 dB	INS:M	Yes [ ] N/A [ ]
FO5	10GBASE-E attenuation management	52.14.3	An attenuation between 5 and 11 dB	INS:M	Yes [ ] N/A [ ]
FO6	MDI requirements	52.14.4	Meet the interface performance specifications listed	INS:M	Yes [ ] N/A [ ]

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52.15.3.11 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	52.10.1	Conforms to IEC-60950: 1991	M	Yes [ ]
ES2	Laser safety —IEC Class 1	52.10.2	Conform to Class 1 laser requirements defined in the IEC 60825-1	M	Yes [ ]
ES3	Installation	52.10.3	Follow applicable local codes and regulations	M	Yes [ ]

52.15.3.12 Environment

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	Electromagnetic interference	52.11.1	Comply with applicable local and national codes for the limitation of electromagnetic interference	M	Yes [ ]

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53. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4

53.1 Overview

This clause specifies the 10GBASE-LX4 PMD (including MDI) and the baseband medium for both multi-mode and single-mode optical fiber. In order to form a complete Physical Layer, the PMD shall be integrated with the appropriate physical sublayers (see Table 53–1) and with the management functions which are accessible through the Management Interface defined in Clause 45, all of which are hereby incorporated by reference.

Table 53–1—LX4 PMD type and associated physical layer clauses

Associated Clause	10GBASE-LX4
46—RS and	Required
XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
49—10GBASE-R PCS	n/a
50—10GBASE-W WIS	n/a

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

Figure 53–1 shows the relationship of the PMD and MDI sublayers to the ISO/IEC (IEEE) OSI reference model.

53.1.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 10GBASE-LX4 PMD. The service interface for this PMD is described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of encoded data between peer PMA entities. The PMD translates the encoded data to and from signals suitable for the specified medium.

The following PMD service primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indicate

PMD_SIGNAL.indicate

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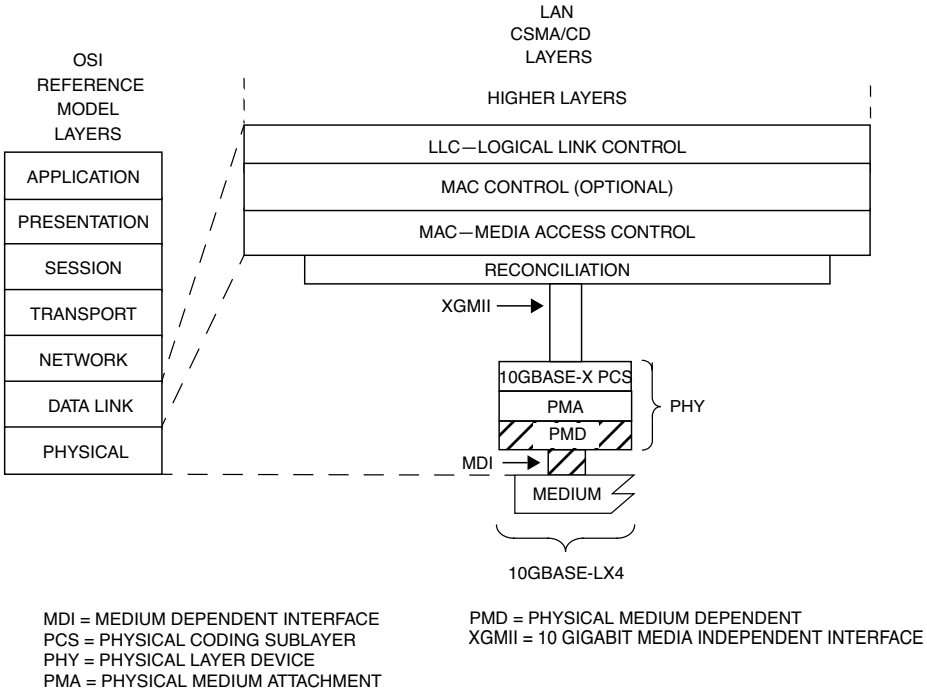


Figure 53–1—10GBASE-LX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

53.1.2 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

53.1.2.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit <0:3>)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of four parallel code-group streams, one stream for each lane. The tx_bit <0:3> correspond to the bits in the tx_lane<0:3> bit streams. Each bit in the tx_bit parameter can take one of two values: ONE or ZERO.

53.1.2.2 When generated

The PMA continuously sends four parallel code-group streams to the PMD at a nominal signaling speed of 3.125 GBaud.

53.1.2.3 Effect of Receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

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53.1.3 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

53.1.3.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_bit <0:3>)

The data conveyed by PMD_UNITDATA.indicate is a continuous sequence of four parallel encoded bit streams. The rx_bit<0:3> correspond to the bits in the rx_lane<0:3> bit streams. Each bit in the rx_bit parameter can take one of two values: ONE or ZERO.

53.1.3.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

53.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

53.1.4 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signals being received from the MDI.

53.1.4.1 Semantics of the service primitive

PMD_SIGNAL.indicate (SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indicate, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known to be good. It is possible for a poor quality link to provide sufficient light for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

53.1.4.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

53.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

53.2 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-LX4 PMD shall be no more than 512 BT (including 2 meters of fiber).

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53.3 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is shown in Table 53–2. Mapping of MDIO status variables to PMD status variables is shown in Table 53–3.

Table 53–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global transmit disable	Control register 1	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

Table 53–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Local fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

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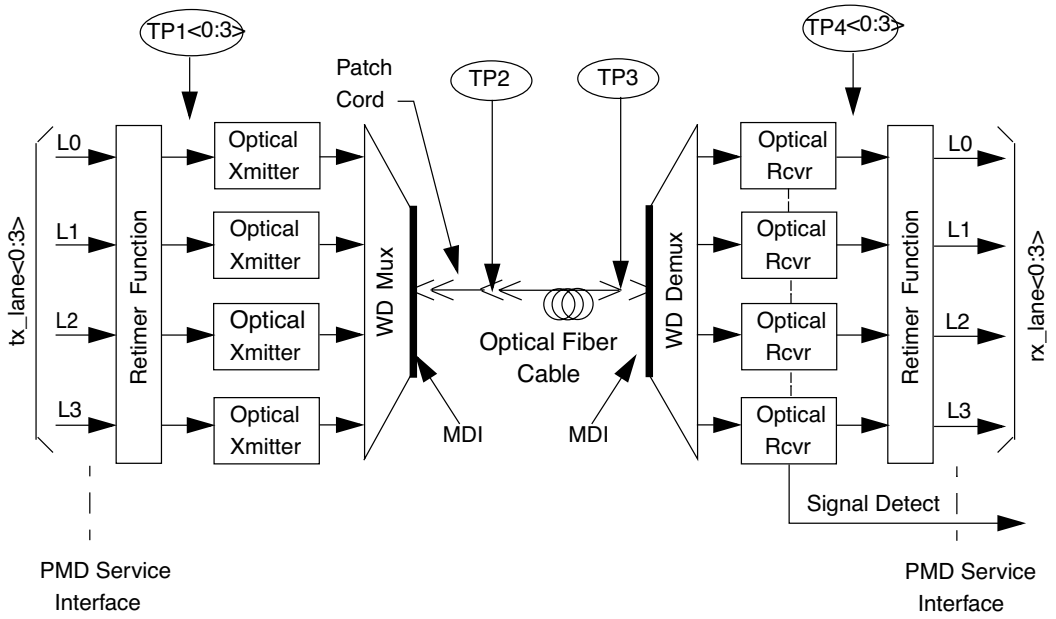
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53.4 PMD functional specifications

The 10GBASE-LX4 PMD performs the Transmit and Receive functions which convey data between the PMD service interface and the MDI plus various management functions if the optional MDIO is implemented.

53.4.1 PMD block diagram

The PMD block diagram is shown in Figure 53–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The optical transmit signal is defined at the output end of a patch cord (TP2), between 2 and 5 meters in length, of a type consistent with the link type connected to the transmitter receptacle defined in 53.14.2. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the end of this single-mode fiber offset-launch mode-conditioning patch cord at TP2. Unless specified otherwise, all transmitter measurements and tests defined in 53.9.1 through 53.9.8 are made at TP2. The optical receive signal is defined at the output of the fiber optic cabling (TP3) at the MDI (see 53.14.3). Unless specified otherwise, all receiver measurements and tests defined in 53.9.9 through 53.9.15 are made at TP3.



WD = Wavelength Division

NOTE—Specification of the retimer function is beyond the scope of this standard; however, a retimer may be required to ensure compliance at test points TP2 and TP3.

Figure 53–2—Block diagram for LX4 PMD transmit/receive paths

TP1 <0:3> and TP4 <0:3> are informative reference points that may be useful to implementers for testing components (these test points will not typically be testable in an implemented system).

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53.4.2 PMD transmit function

The PMD Transmit function shall convert the four electronic bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate optical signal streams. The four optical signal streams shall then be wavelength division multiplexed and delivered to the MDI, all according to the transmit optical specifications in this clause. The higher optical power level in each signal stream shall correspond to a tx_bit = ONE.

53.4.3 PMD receive function

The PMD Receive function shall demultiplex the composite optical signal stream received from the MDI into four separate optical signal streams. The four optical signal streams shall then be converted into four electronic bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indicate (rx_bit<0:3>), all according to the receive optical specifications in this clause. The higher optical power level in each signal stream shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the PMD_UNITDATA.request(tx_bit<0:3>) service primitive to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit<0:3>), where rx_bit<0:3> = tx_bit<0:3>.

53.4.4 Global PMD signal detect function

The Global PMD Receive Signal OK function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indicate message is generated when a change in the value of SIGNAL_DETECT occurs.

SIGNAL_DETECT shall be a global indicator of the presence of optical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-LX4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

Table 53–4—SIGNAL_DETECT value definition

Receive conditions	Receive Signal OK value
For any lane; Input_optical_power ≤ -30 dBm	FAIL
For all lanes; [(Input_optical_power ≥ Receiver sensitivity (max) in OMA in Table 53–8) AND (compliant 10GBASE-LX4 signal input)]	OK
All other conditions	Unspecified

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input optical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the optical signal and implementations that respond to the average optical power of the modulated optical signal.

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53.4.5 PMD lane by lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_n, where n represents the lane number in the range 0:3, value shall be continuously set in response to the amplitude of the average optical power of the modulated optical signal on its associated lane, according to the requirements of Table 53–4.

53.4.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

53.4.7 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional and allows all of the optical transmitters to be disabled.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the optical transmitters so that the each transmitter meets the requirements of the Average Launch Power of the OFF Transmitter in Table 53–7.
b) If a PMD_fault is detected, then the PMD may set the Global_PMD_transmit_disable to ONE, turning off the optical transmitter in each lane.

53.4.8 PMD lane by lane transmit disable function

The PMD_transmit_disable function is optional and allows the optical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the optical transmitter associated with that variable so that the transmitter meets the requirements of the Average Launch Power of the OFF Transmitter in Table 53–7.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_n to ONE, turning off the optical transmitter in each lane.

If the optional PMD_lane_by_lane_transmit_disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane.

53.4.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE.

53.4.10 PMD transmit fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE.

53.4.11 PMD receive fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE.

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53.5 Wavelength-division multiplexed-lane assignments

The wavelengths for each multiplexed lane of the 10GBASE-LX4 PMD shall be as defined in Table 53–5.

Table 53–5—Wavelength-division-multiplexed lane assignments

Lane	Wavelength ranges	PMD Service Interface transmit bit stream	PMD Service Interface receive bit stream
L_0	1269.0 – 1282.4 nm	tx_lane<0>	rx_lane<0>
L_1	1293.5 – 1306.9 nm	tx_lane<1>	rx_lane<1>
L_2	1318.0 – 1331.4 nm	tx_lane<2>	rx_lane<2>
L_3	1342.5 – 1355.9 nm	tx_lane<3>	rx_lane<3>

53.6 Operating ranges for 10GBASE-LX4 PMD

The operating ranges for 10GBASE-LX4 PMD are defined in Table 53–6. A 10GBASE-LX4 compliant transceiver supports all media types listed in Table 53–6 (i.e., 50 μm and 62.5 μm multimode fiber, and 10 μm single-mode fiber) according to the specifications defined in 53.14. A transceiver which exceeds the operational range requirement while meeting all other optical specifications is considered compliant (e.g., a single-mode solution operating at 10 500 m meets the minimum range requirement of 2 to 10 000 m).

Table 53–6—Operating range for 10GBASE-LX4 PMD over each optical fiber type

Fiber type	Modal bandwidth at 1300 nm (min. overfilled launch) (MHz•km)	Minimum range (meters)
62.5 μm MMF	500	2 to 300
50 μm MMF	400	2 to 240
50 μm MMF	500	2 to 300
10 μm SMF	n/a	2 to 10 000

For MMF links, to ensure that the specifications of Table 53–6 are met with MMF links, the wavelength-division-multiplexed 10GBASE-LX4 transmitter outputs shall be coupled through a single-mode fiber offset-launch mode-conditioning patch cord, as defined in 38.11.4.

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53.7 PMD to MDI optical specifications for 10GBASE-LX4

53.7.1 Transmitter optical specifications

The 10GBASE-LX4 transmitters shall meet the specifications defined in Table 53–7 per measurement techniques defined in 53.9.

Table 53–7—Transmit characteristics for the 10GBASE-LX4 over each optical fiber type

Description	62.5 μm and 50 μm MMF	10 μm SMF	Units
Transmitter Type	Longwave Laser		
Signaling speed per lane (nominal)	3.125 +/– 100 ppm		GBd
Lane wavelengths (range)	1269.0 – 1282.4 1293.5 – 1306.9 1318.0 – 1331.4 1342.5 – 1355.9		nm
Trise/Tfall (max. 20-80 % response time)	120		ps
Side-mode suppression ratio (SMSR), (min)	0.0		dB
RMS spectral width (max)[a]	0.62		nm
Average launch power, four lanes (max)	5.5		dBm
Average launch power, per lane (max)	–0.5		dBm
Optical Modulation Amplitude (OMA), per lane (max)	750 (–1.25)		μW (dBm)
Optical Modulation Amplitude (OMA), per lane (min)[b]	211 (–6.75)	237 (–6.25)	μW (dBm)
Extinction Ratio (min)	3.5		dB
Average launch power of OFF transmitter, per lane (max)	–30		dBm
RIN_{12} (OMA)	–120		dB/Hz

[a]For sources with a distribution of two discrete modes, the spectral window containing 90% of source spectral power (max) equals 1.0 nm and the spectral window containing 99% of source spectral power (max) equals 1.4 nm. For sources with a continuous spectral distribution, the spectral window containing 90% of source spectral power (max) equals 2.0 nm and the spectral window containing 99% of source spectral power (max) equals 3.2 nm. The spectral window specifications for the continuous case is consistent with a Gaussian spectral distribution having an RMS spectral width of 0.62 nm.

[b]Transmitter values are specified at TP2. For MMF, the values in the above table include a 0.5dB attenuation for the offset launch patch cord.

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53.7.2 Receive optical specifications

The 10GBASE-LX4 receiver shall meet the specifications defined in Table 53–8 per measurement techniques defined in 53.9. The receive sensitivity includes the extinction ratio penalty.

Table 53–8—10GBASE-LX4 receive characteristics

Description	62.5 μm MMF 50μm MMF	10 μm SMF	Unit
Signaling speed per lane (nominal)	3.125 ± 100 ppm		GBd
Lane wavelengths (range)	1269.0 – 1282.4 1293.5 – 1306.9 1318.0 – 1331.4 1342.5 – 1355.9		nm
Average receive power, four lanes (max)	5.5		dBm
Average receive power, per lane (max)	–0.5		dBm
Return loss (min)	12		dB
Receive sensitivity (OMA), per lane	37.4 (–14.25)	35.9 (–14.45)	μW (dBm)
Stressed receive sensitivity (OMA),[a,b] per lane	89.0 (–10.5)	45.7 (–13.4)	μW (dBm)
Vertical eye closure penalty,[c] per lane	3.7	1.1	dB
Receive electrical 3 dB upper cutoff frequency, per lane (max)	3750		MHz

[a]Measured with conformance test signal at TP3 (see 53.9.14) for BER = 10^{-12}.
[b]The stressed sensitivity values in the table are for system level BER measurements which include the effects of CDR circuits. It is recommended that at least 0.4dB additional margin be allocated if component level measurements are made without the effect of CDR circuits.
[c]Vertical eye closure penalty is a test condition for measuring stressed receive sensitivity. It is not a required characteristic of the receiver.

53.7.3 Worst case 10GBASE-LX4 link power budget and penalties (informative)

The worst case power budget and link penalties for a 10GBASE-LX4 channel are shown in Table 53–9.

53.8 Jitter specifications for each lane of the 10GBASE-LX4 PMD

53.8.1 Transmit jitter specification

The transmit jitter is tested using a bit error ratio tester[18] (BERT), where the tester horizontally scans the eye opening across the centerline at a virtual TP3 (hereafter referred to as simply TP3) and measures the bit error ratio at each point in time. The plot of BER as a function of sampling time is called the “bathtub curve.”

[18]In this document, BERT is intended to include any test measurement device that can generate a BER bathtub curve. Here, it is implied that the BERT includes the Reference Receiver, filters, PLLs, etc.

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Table 53–9—Worst case 10GBASE-LX4 link power budget and penalties[a]

Parameter	62.5 μm MMF	50 μm MMF		10 μm SMF	Unit
Modal bandwidth as measured at 1300 nm (minimum, overfilled launch)	500	400	500	n/a	MHz•km
Link power budget	7.5	7.5	7.5	8.2	dB
Operating distance[b]	300	240	300	10 000	m
Channel insertion loss[c, d]	2.0	1.9	2.0	6.2	dB
Allocation of penalties	5.0	5.5	5.5	1.9	dB
Additional insertion loss allowed[e]	0.5	0.1	0.0	0.1	dB

[a]Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.
[b]An offset launch patch cord is required for MMF.
[c]The channel insertion loss is calculated using the maximum distance values specified in Table 53–6 plus an allocation of 1.5dB for MMF and 2.0dB for SMF for connection and splice loss. Channel insertion loss is specified from TP2 to TP3 in Figure 53–2. The total insertion loss for multimode fiber, including the attenuation of the offset launch patch cord, is allowed to be 0.5 dB higher than shown in the table.
[d]A wavelength of 1269 nm, a minimum receiver bandwidth of 2550 MHz, and a DCD_DJ of 14 ps is used to calculate lane insertion loss, link power penalties, and unallocated margin.
[e]This portion of the link budget is permitted to be used to overcome insertion loss higher than the "Channel insertion loss" value.

All points on the BER "bathtub curve" shall have an eye opening greater than specified by the bit error ratio tester (BERT) mask at the respective BER when measured using the jitter compliance test methodology for the transmitter as defined in 53.9.10. The BERT mask (see example in Figure 53–3) is specified by the following polynomial:

$$\log_{10}(BER) \le A - B\left(\frac{t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}1)$$

$$\log_{10}(BER) \le A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}2)$$

where:

$$A = -1.75, B = \frac{\log_{10}(e)}{2} \approx 0.217$$

and the variables "W" and "σ" for the polynomial are specified in Table 53–10. The variables "W" and "σ" are the effective DJ and RJ respectively although the DJ and RJ values are not normative in the standard. In the above equations the variable "t" is time specified in unit intervals (UI). The BER mask is defined for $10^{-12} <$ BER $< 10^{-6}$. The DJ and RJ values do not need to be individually met, the required mask is defined by the formulas above.

Table 53–10—BERT mask specifications

PMD	W (UI pk to pk)	σ (UI rms)
10GBASE-LX4	0.3	0.015

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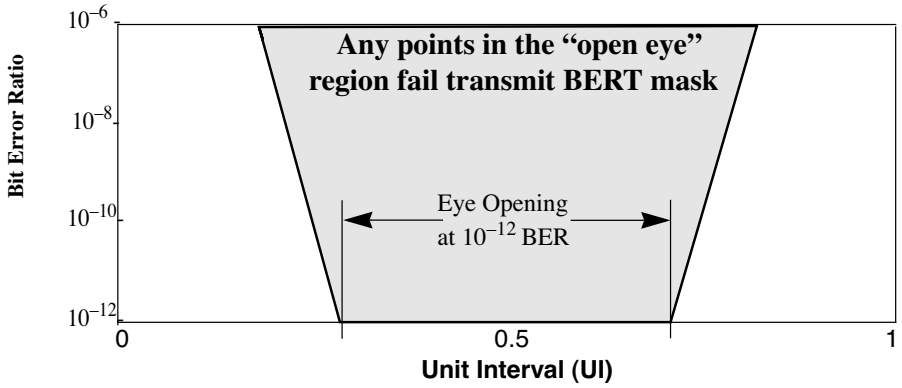


Figure 53–3—Example transmit BER mask at TP3 (informative)

53.8.1.1 Channel requirements for transmit jitter testing

The optical channel for 10GBASE-LX4 shall

a) Have an ITU-T G.652 fiber or fibers with lengths chosen to have a total dispersion larger than specified in Table 53–14 for the wavelength of the device under test. To verify that the fiber has the correct amount of dispersion, use the measurement method defined in ANSI/TIA/EIA-455-175A-92.
b) Meet these requirements in the linear regime of the singlemode fiber.
c) Meet the requirements in Table 53–14 for the case of a 2 to 5 meter offset launch patch cord.

The transmitter shall also be tested for multimode fiber use using the multimode simulation channel defined in 53.9.10.1.

53.8.1.2 Test pattern requirements for transmit jitter testing

Test patterns for 10GBASE-LX4 are specified in Annex 48A.

53.8.2 Receive jitter tolerance specification

The jitter compliance methodology for the receiver is defined in Annex 48B. The receiver shall operate at a BER less than 10^{-12} when tested with an input signal defined in 53.8.2.1 through 53.8.2.1.

The input signal used for jitter tolerance is comprised of the appropriate test pattern, the stressed receiver conformance test signal, the minimum specified input jitter (TJ and DJ) and added sinusoidal jitter.

53.8.2.1 Input jitter for receiver jitter test

The input jitter used to test receiver jitter tolerance shall meet the requirements of the receiver input jitter mask defined by the following equations and Table 53–10.

$$\log_{10}(BER) \geq A - B\left(\frac{t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}3)$$

$$\log_{10}(BER) \geq A - B\left(\frac{1 - t - 0.5W}{\sigma}\right)^2 \quad (53\text{–}4)$$

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where:

$$A = -1.75, B = \frac{\log_{10}(e)}{2} \approx 0.217$$

The mask is defined for a BER range of 10^{-12}<BER<10^{-6}. An explanation of the variables W, s, and t can be found in 53.7.1.

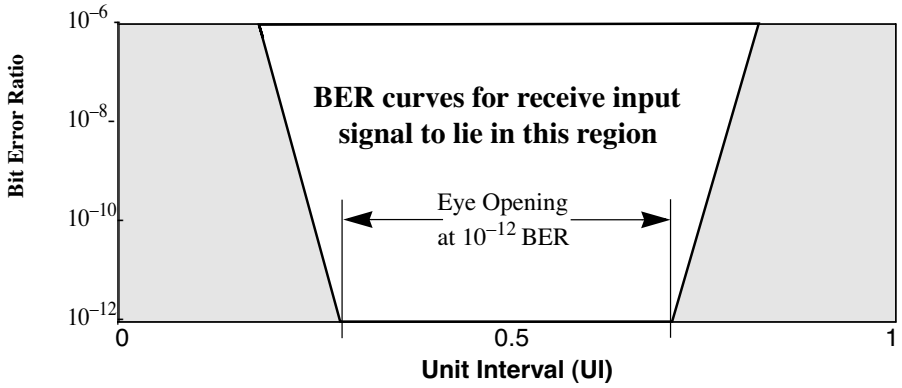


Figure 53–4—Input jitter mask for receiver test (informative)

The random jitter (RJ) component of the input signal shall have uniform spectral content over the measurement frequency range of 18.75kHz to 1.5GHz.

The test method for verification of the input jitter is defined in section 53.7.1. A Clock Recovery Unit shall be used for verification of the input jitter. It shall have a high-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade. The low-frequency corner corresponds to the point at which the PLL must begin to track low-frequency jitter. The filter used for RX input signal characterization shall be a fourth-order Bessel-Thomson filter as specified in section 53.9.7.

53.8.2.2 Added sinusoidal jitter for receiver jitter test

The sinusoidal jitter used to test receiver jitter tolerance shall meet the requirements of Table 53–11. Sinusoidal jitter shall be added to the test signal that complies with 53.8.2.1.

Table 53–11—Applied sinusoidal jitter

Frequency range	Sinusoidal amplitude jitter (UI pk-to-pk)
f<18.75kHz	NA
18.75kHz<f<1.875MHz	$\frac{93750}{f}$
1.875 MHz < f < 10 LB[a]	0.05

[a]LB = Loop Bandwidth; Recommended minimum value of upper bound of 0.05 UI added range is 10 times loop bandwidth.

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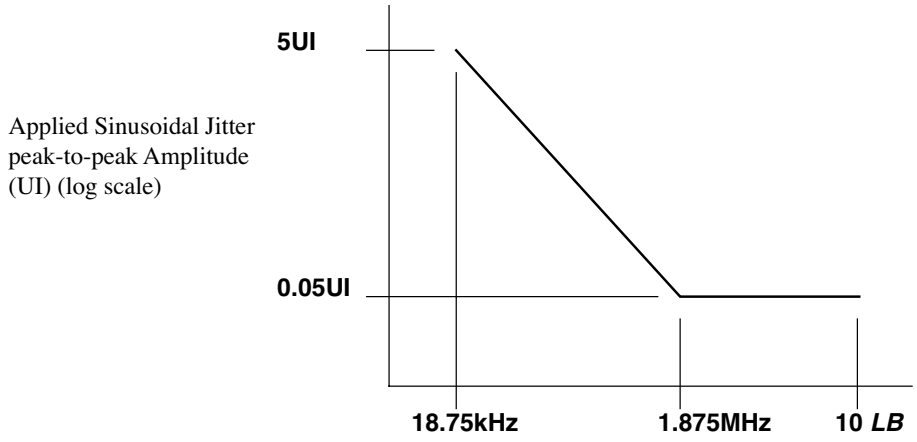


Figure 53–5—Mask of the sinusoidal component of jitter tolerance (informative)

53.9 Optical measurement requirements

All optical measurements shall be made through a short patch cable, between 2 and 5 meters in length. If a single-mode fiber offset-launch mode-conditioning patch cord is used, the optical transmit signal is defined at the output end (TP2) of the single-mode fiber offset-launch mode-conditioning patch cord.

It is recommended that wavelength measurements, RIN measurements, optical power measurements, source spectral window measurements, extinction ratio measurements, optical modulation amplitude measurements, and transmit rise/fall characteristics be performed using a low-frequency square-wave pattern (K28.7).

It is recommended that the receiver 3dB electrical upper cutoff frequency characterization be performed using CRPAT or another reasonable mixed frequency pattern.

Furthermore, it is recommended that the transmitter optical waveform, receive sensitivity measurements, transmitter jitter conformance tests, stressed receiver conformance tests, and jitter tolerance measurements be characterized using CJPAT.

The recommendation of specific test patterns is provided in an effort to meet the overall objective of ensuring compliance of the standard under any and all valid data patterns.

53.9.1 Wavelength range measurements

The wavelength ranges of each wavelength lane shall be measured with an optical spectrum analyzer (OSA) or equivalent device over the wavelength range specified in Table 53–8; with the following conditions:

a) The resolution bandwidth equal to the spectral window values for the particular source type as specified in Table 53–8, and
b) The channel under test is modulated using valid 10GBASE-LX4 signals.

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53.9.2 Optical power measurements

The absolute optical power of each channel shall be measured using the methods in TIA/EIA-455-95, with the sum of the optical power from all of the channels not under test below –30dBm, per the test set-up in Figure 53–6.

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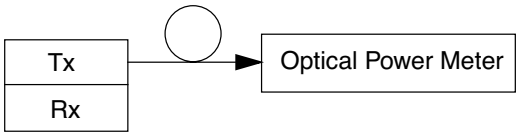


Figure 53–6—Optical power measurement test set-up

53.9.3 Source spectral window measurements

The source spectral window shall be measured for each channel individually with the sum of the optical power from all of the channels not under test below –30dBm, per the test set-up in Figure 53–7. The channel under test shall be modulated using valid 10GBASE-LX4 signals.

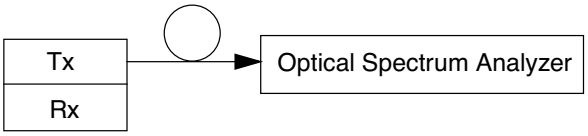


Figure 53–7—Source spectral window measurement test set-up

53.9.4 Extinction ratio measurements

Extinction ratio shall be measured using the methods specified in TIA/EIA-526-4A. The extinction ratio is measured under fully modulated conditions.

53.9.5 Optical Modulation Amplitude (OMA) measurements

The OMA measurement methodology is defined in 52.9.5 with the exception that each channel will be tested individually and the sum of the optical power from all of the channels not under test shall be below –30dBm.

53.9.6 Relative Intensity Noise [RIN_{12}(OMA)]

The RIN measurement methodology is defined in 52.9.6 with the exception that each channel will be tested individually, the sum of the optical power from all of the channels not under test shall be below –30dBm, and the upper –3 dB limit of the measurement apparatus is to be approximately equal to the bit rate (i.e., 3.125 GHz).

53.9.7 Transmitter optical waveform (transmit eye)

The required transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram as shown in Figure 53–8. Measurements shall be made as per ANSI/TIA/EIA-526-4A-1997 (OFSTP-4). The transmit mask is not used for response time and jitter specification.

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Normalized amplitudes of 0.0 and 1.0 represent the amplitudes of logic ZERO and ONE respectively.

The eye shall be measured with respect to the mask of the eye using a fourth-order Bessel-Thomson filter having a transfer function given by:

$$H(p) = \frac{105}{105 + 105\,y + 45\,y^2 + 10\,y^3 + y^4} \qquad (53\text{–}5)$$

where:

$$y = 2.114\,p; \quad p = \frac{j\omega}{\omega_r}; \quad \omega_r = 2\pi f_r; \quad f_r = 2.344\ \text{GHz}$$

and where the filter response vs. frequency range for this fourth-order Bessel-Thomson filter is defined in ITU-T G.957, along with the allowed tolerances for its physical implementation.

This Bessel-Thomson filter is not intended to represent the noise filter used within an optical receiver, but is intended to provide uniform measurement conditions at the transmitter.

The fourth-order Bessel-Thomson filter is reactive. In order to suppress reflections, a 6 dB attenuator may be required at the filter input and/or output.

A Clock Recovery Unit shall be used to trigger the scope for mask measurements. It shall have a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade.

For each lane, the transmit optical waveform is tested with the receive section in operation on all four lanes and with the transmit lanes not under test in operation. CJPAT, CRPAT, or valid 8B10B encoded data, may be sent to the receive section of the transmitter under test. The data being received must be asynchronous to the transmitted data.

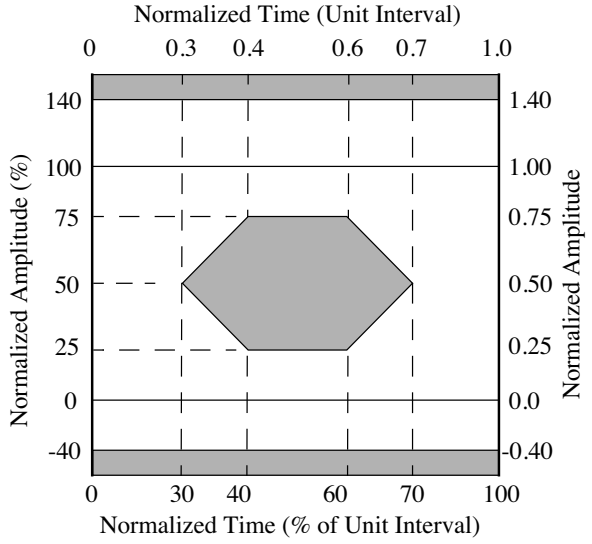


Figure 53–8—Transmitter Eye Mask Definition

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53.9.8 Transmit rise/fall characteristics

Optical response time specifications are based on unfiltered waveforms. Some lasers have overshoot and ringing on the optical waveforms, which, if unfiltered, reduce the accuracy of the measured 20–80% response times. For the purpose of standardizing the measurement method, measured waveforms shall conform to the mask defined in Figure 53–8. If a filter is needed to conform to the mask, the filter response shall be removed using Equation (53–6):

$$T_{rise,fall} = \sqrt{(T_{rise,fall\_measured})^2 - (T_{rise,fall\_filter})^2} \quad (53–6)$$

where the filter may be different for rise and fall. Any filter shall have an impulse response equivalent to a fourth-order Bessel-Thomson filter. The fourth-order Bessel-Thomson filter defined in 53.9.7 may be a convenient filter for this measurement; however, its low bandwidth adversely impacts the accuracy of the $T_{rise,fall}$ measurements.

53.9.9 Receive sensitivity measurements

The stressed receive sensitivity shall be measured using the conformance test signal at TP3, as specified in 53.9.14 and meet the conditions specified in Table 53–8.

53.9.10 Transmitter jitter conformance (per lane)

53.9.10.1 Block diagram and general description of test set up

A block diagram for the transmitter jitter conformance test is shown in Figure 53–9. The transmitter (Tx) of the system under test is tested for conformance by continuously generating the test pattern specified in Annex 48A. Depending on the port type, a “Test Fiber” is added to the channel so that the jitter can be measured at a virtual TP3 (hereafter simply referred to simply as TP3) and thus include dispersion and other chromatic and channel induced penalties.

A “Reference Optical Filter” selects the wavelength channel under test in the presence of all channels operating.

A “Reference Receiver (Rx)” converts the optical signal to the electrical domain for input to the BERT.

For 10GBASE-LX4 (singlemode) the receiver shall have a fourth-order Bessel-Thomson response with the transfer function specified in 53.9.7.

Since there is no known way to create a channel using multimode fiber that would yield consistent results, the fiber is omitted from TP2 to TP3.

For 10GBASE-LX4 (multimode), the receiver shall have a fourth-order Bessel-Thomson response with the transfer function specified in 53.9.7 followed by a transversal filter with two equal amplitude paths with a differential delay of 157ps.

The PLL is used in the jitter measurement. It shall have a corner frequency of less than or equal to 1.875MHz and a slope of 20dB/decade. When using a Clock Recovery Unit as a clock for BER measurements, passing of low-frequency jitter from the data to the clock removes this low-frequency jitter from the measurement. The corner frequency corresponds to the point at which the PLL must begin to track this low-frequency jitter.

Jitter shall be measured at the average value of the overall waveform. This can be accomplished with AC coupling to ground and measuring at ground.

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The measurement in this section shall be satisfied with asynchronous data flowing into all four optical receiver channels of the system under test.

The method by which the test pattern is loaded into, or generated by, the BERT is outside the scope of this document.

For each lane, the transmit jitter is tested with the receive section in operation on all four lanes and with the transmit lanes not under test in operation. CJPAT, CRPAT, or valid 8B10B encoded data, may be sent to the receive section of the transmitter under test. The data being received must be asynchronous to the transmitted data.

Annex 48B contains both theoretical and practical information on jitter testing.

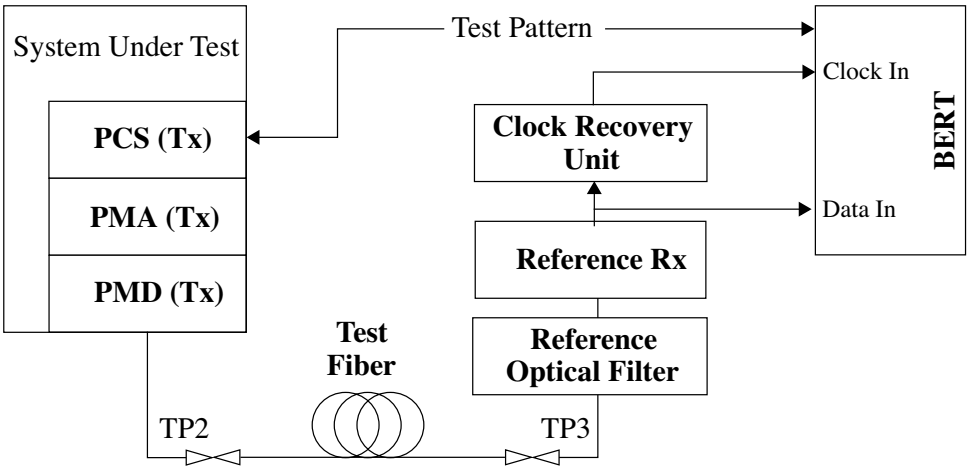


Figure 53–9—Transmit jitter test block diagram

53.9.10.2 Channel requirements for transmit jitter testing

The optical channel used to test the transmitter shall meet the requirements listed in Table 53–12.

Table 53–12—Transmit jitter compliance channel specifications

PMD Type	Minimum dispersion[a] (ps/nm)		Insertion loss[b]	Minimum Return loss[c]
	Minimum	Maximum		
10GBASE-LX4 (multimode)	N/A	N/A	Minimum	See Table 53–8
10GBASE-LX4 (singlemode)	$0.2325 \cdot \lambda \cdot [1 - (1300 / \lambda)^4]$	$0.2325 \cdot \lambda \cdot [1 - (1324 / \lambda)^4]$	Minimum	See Table 53–8

[a]The dispersion is measured for the wavelength of the device under test. The coefficient assumes 10 km for the case of singlemode fiber.
[b]There is no intent to stress the sensitivity of the BERT's optical receiver.
[c]The return loss is applied at TP2. Note that the referenced return losses are maximums. Here, the return loss is a minimum.

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For 10GBASE-LX4 (singlemode), the transmitter shall be compliant with dispersion at least as negative as the "minimum dispersion" and at least as positive as the "maximum dispersion" columns. This shall be achieved using ITU-T G.652 fiber (note 2) or fibers with lengths chosen to have a total dispersion larger than specified in Table 53–12 for the wavelength of the device under test. To verify that the fiber has the correct amount of dispersion, the measurement method defined in ANSI/TIA/EIA-455-175A-92 may be used. The channel shall meet these requirements in the linear regime of the fiber. The channel shall provide an optical back reflection specified in Table 53–7 for 10GBASE-LX4. The state of polarization of the back reflection shall be adjusted to create the greatest RIN. The methods of 52.9.6.2 and 52.9.6.3 may be used.

The channel for 10GBASE-LX4 (multimode) is a 2 to 5 meter patch cord meeting the requirements in Table 53–12. The channel shall provide back reflection to the transmitter at –12 dB. The polarization adjustment does not apply, as noted in 52.9.6.3 item c).

53.9.10.3 Transmit jitter test procedure

After setting up the test as described above, the BERT is scanned horizontally across the center of the eye, from 0 unit intervals (UI) to 1 unit interval, while measuring the error rate to develop a BER "bathtub curve" as described in 53.8.1.1. This clause also specifies the BER mask. It is not necessary to measure the error rate in the center of the eye where the BER is less than 10^{-12} or at the edges where the BER is worse than 10^{-4}. The mask natively includes those components of jitter (random, deterministic, bounded) historically measured independently.

A Clock Recovery Unit having a low-frequency corner of less than or equal to 1.875 MHz and a slope of 20 dB/decade shall be used to generate the reference clock for transmit jitter measurements.

NOTE—The specifications for the Reference Optical Filter, Reference Rx, Clock Recovery Unit, and BERT, except as specified above, are outside the scope of this document. The Reference Rx and Clock Recovery Unit are intended to provide consistent and repeatable measurements, not to represent the worst case receiver. It should also be noted that a poorer grade of test equipment will force a greater burden onto the system-under-test to meet specifications. Similarly, a better grade of test equipment will ease the development and manufacture of the system and system components. It is expected that trade-offs needed to optimize the overall cost of development, manufacture and test will change over time and are best left to the implementer.

53.9.11 Receive sensitivity measurements

The receiver sensitivity, which is defined for an ideal input signal is informative. Receivers are tested with a conditioned input signal where both vertical eye closure and jitter have been added according to 53.9.12. When tested according to 53.9.12, the stressed sensitivity shall meet the specifications in Table 53–8 for 10GBASE-LX4.

53.9.12 Stressed receiver conformance test

The measurements in this subclause shall be satisfied with asynchronous data flowing out of the optical transmitter of the system under test. This data shall be consistent with normal signal properties and content.

53.9.12.1 Block diagram of stressed receiver tolerance test set up

A block diagram for the receiver jitter conformance test is shown in Figure 53–10. The receiver of the system under test is tested for conformance by putting the PCS in test mode as specified in Annex 48A. A suitable pattern generator is used to continuously generate a test pattern defined in Annex 48A. The optical test signal is conditioned (stressed) using the stressed receiver methodology defined in 53.9.14 and applying sinusoidal jitter as defined in 53.8.2.2. As defined in section Annex 48A, the PCS is capable of detecting the data pattern and reporting any errors received.

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A BER test set or other suitable test set is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. This measurement is made using the same method as the transmit jitter test method described in 52.8. The "Test Fiber" called out for LX4 is not needed to characterize the receiver input signal. A "Clock Recovery Unit" meeting the requirements of 53.8.2.1 shall be used.

Jitter shall be calibrated at the average value of the overall optical waveform. This can be accomplished by AC coupling.

The method by which the test pattern is loaded into, or generated by, the BERT is outside the scope of this document.

Annex 48B contains both theoretical and practical information on jitter testing.

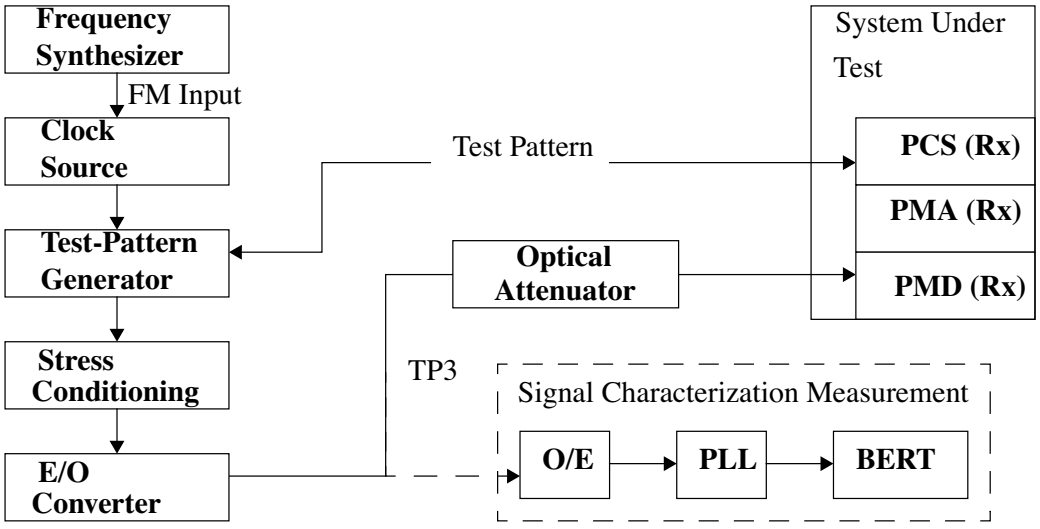


Figure 53–10—Receive jitter test block diagram

53.9.12.2 Stressed receiver conformance test procedure

A BER test set, or other suitable test set, is needed to characterize and verify that the signal used to test the receiver has the appropriate characteristics. This measurement is made using the same method as the transmit jitter test method described in 53.9.10. The "Test Fiber" called out for LX4 (single-mode) and the transversal filter called out for LX4 (multimode) are not needed to characterize the receiver input signal. A Clock Recovery Unit meeting the requirements of 53.8.2.1 shall be used.

53.9.12.3 Characterization of receiver input signal

Care should be taken when characterizing the signal used to make receiver tolerance measurements. In the case of a transmit jitter measurement, excessive and/or uncalibrated noise/jitter in the test system makes it more difficult to meet the specification and may have a negative impact on yield, but will not effect interoperability. In the case of the receiver input calibration measurement, however, excessive noise/jitter will result in an input signal that does not meet the mask requirements defined in 53.8.2.1. Running the receiver tolerance test with a signal that is under-stressed may result in the deployment of non-compliant receivers. Care should be taken to minimize the noise/jitter introduced by the reference O-E, filters and BERT and/or to cor-

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rect for this noise. While the details of a BER scan measurement and test equipment are beyond the scope of this document, it is recommended that the implementer fully characterize their test equipment and apply appropriate guard bands to ensure that the RX input signal meets the mask specified in 53.8.2.1.

53.9.12.4 Jitter tolerance test procedure

Set up the test apparatus as described in 53.9.12.1 and adjust the optical input power to the receiver under test to meet the requirements of 53.8.2.1. The sinusoidal jitter is then swept across the frequency and amplitude range specified in 53.8.2.1 while monitoring BER at the receiver. This method does not result in values for TJ, DJ, or RJ contributed by the receiver. It does, however, guarantee that a receiver meeting the requirements of this test will operate with the worst-case optical input

For each lane, the receive jitter tolerance is tested with the transmit section in operation on all four lanes and with the receive lanes not under test in operation. CJPAT, CRPAT, or valid 8B10B encoded data, may be sent from the transmit section of the receiver under test. The data being transmitted must be asynchronous to the received data.

53.9.13 Measurement of the receiver 3 dB electrical upper cutoff frequency

The receiver cutoff frequency measurement shall be performed on each wavelength channel independently using a laser source with its output wavelength within the specified wavelength range of the channel to be tested. The test setup is shown in Figure 53–11. The test is performed with a tunable laser that is suitable for analog signal transmission. The laser is modulated by a digital data signal. In addition to the digital modulation the laser is modulated with an analog signal. The analog and digital signals should be asynchronous. The data pattern to be used for this test is the short continuous random test pattern defined in Annex 48A. The frequency response of the laser must be sufficient to allow it to respond to both the digital modulation and the analog modulation. The laser should be biased so that it remains linear when driven by the combined signals. The test may use two optical sources and an optical combiner as defined in 52.9.12.

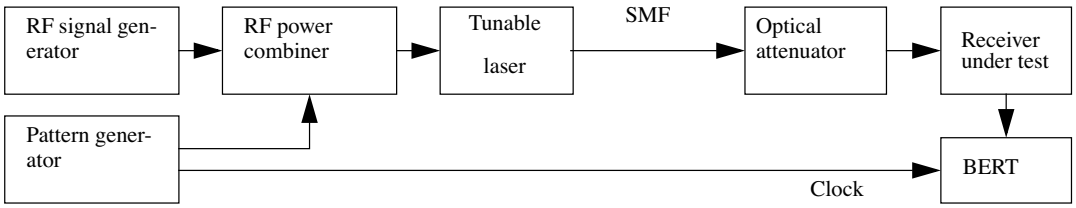


Figure 53–11—Test setup for receiver bandwidth measurement

The 3 dB upper cutoff frequency shall be measured using the following steps:

a) Calibrate the frequency response characteristics of the test equipment including the analog radio frequency (RF) signal generator, RF power combiner, and laser source, with the optical source meeting the requirements of this clause.
b) Configure the test equipment as shown in Figure 53–11. Take care to minimize changes to the signal path which could affect the system frequency response after the calibration in step a. Connect the laser output with no RF modulation applied to the receiver under test through an optical attenuator and taking into account the extinction ratio of the source, set the optical power to a level that approximates the stressed receive sensitivity level in Table 53–8.

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c) Locate the center of the eye with the BERT. Turn on the RF modulation while maintaining the same average optical power established in step b).
d) Measure the necessary RF modulation amplitude (in dBm) required to achieve a constant BER (e.g., 10^{-8}) for a number of frequencies.
e) The receiver 3 dB electrical upper cutoff frequency is that frequency where the corrected RF modulation amplitude (the measured amplitude in "d" corrected with the calibration data in "a") increases by 3 dB (electrical). If necessary, interpolate between the measured response values.

53.9.14 Conformance test signal at TP3 for receiver testing

Receivers being tested for conformance to the stressed receive sensitivity requirements of 53.9.9 and the total jitter requirements of 53.9.10 shall be tested using a conformance test signal at TP3 conforming to the requirements described in Figure 53–12. It is recommended that the conformance test signal be generated using a short continuous random test pattern as defined in Annex 48A. The conformance test signal is conditioned by applying deterministic jitter (DJ) and intersymbol interference (ISI). The conditioned conformance test signal is shown schematically in Figure 53–12. The horizontal eye closure (reduction of pulse width) caused by the duty cycle distortion (DCD) component of DJ shall be no less than 14ps.

The vertical eye closure penalty shall be greater than or equal to the value specified in Table 53–8. The DJ cannot be added with a simple phase modulation, which does not account for the DCD component of DJ.

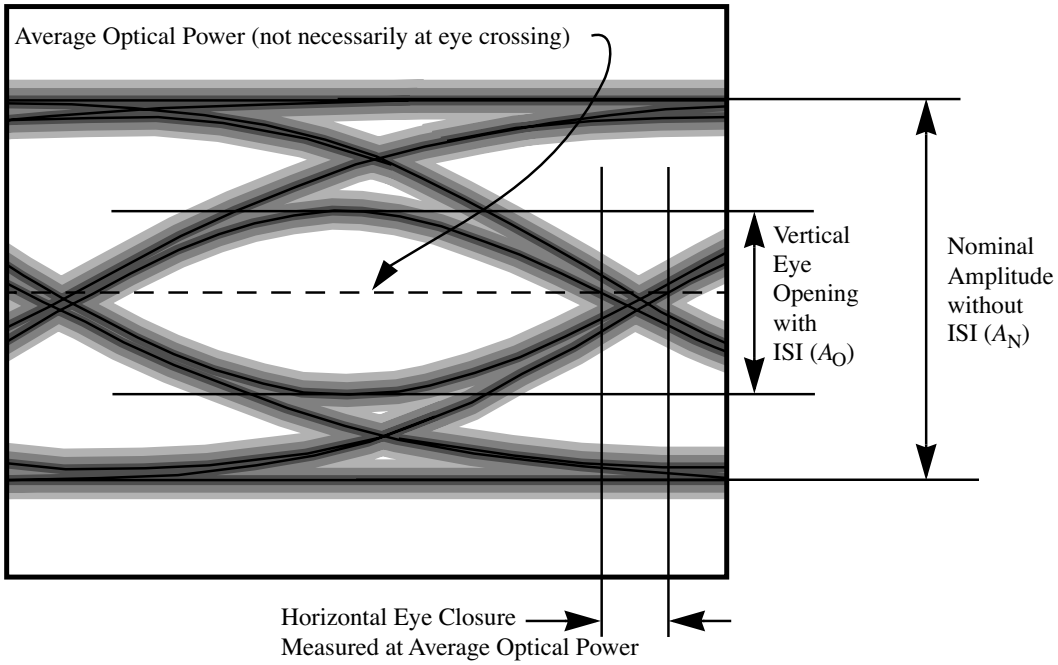


Figure 53–12—Required characteristics of the conformance test signal at TP3

The vertical eye closure penalty is given by:

$$\text{Vertical eye closure penalty [dB]} = 10 \times \log \frac{A_O}{A_N}$$

where, A_O is the amplitude of the eye opening and A_N is the normal amplitude without ISI, as measured in Figure 53–12.

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Figure 53–13 shows a possible test set up for producing the conformance test signal at TP3. The coaxial cable is adjusted in length to produce the correct DCD component of DJ. Since the coaxial cable can produce the incorrect ISI, a limiting amplifier is used to restore fast rise and fall times. A Bessel-Thomson filter is selected to produce the minimum ISI induced eye closure as specified per Figure 53–12. This conditioned signal is used to drive a high bandwidth, tunable, wavelength tunable source.

Figure 53–13 shows this function being performed by a tunable source in combination with an external optical modulator. However, any other method capable of this combined function will suffice. Similarly, the remaining sources supply to their respective channels modulated signals at specific wavelengths, as specified in 53.9.15. This could be accomplished with tunable or fixed sources at the wavelengths required. The vertical and horizontal eye closures to be used for receiver conformance testing are verified using a fast photodetector and amplifier coupled to the oscilloscope input through a filter. The combined filtering effect of the photodetector, amplifier, and filter shall be a fourth-order Bessel-Thomson filter of 2.34 GHz bandwidth. Special care should be taken to ensure that all the light from the fiber is collected by the fast photodetector and that there is negligible mode selective loss, especially in the optical attenuator.

The source for the channel under test shall be set to supply a signal at the output of the optical multiplexer at the minimum OMA with all other remaining channels set to the maximum OMA. Each channel is to be tested with its adjacent channels set at the near end of their wavelength range. This is to occur sequentially, as described in 53.9.15. The channel under test is to be tuned over its wavelength range during a given measurement to account for wavelength dependent losses within the channel.

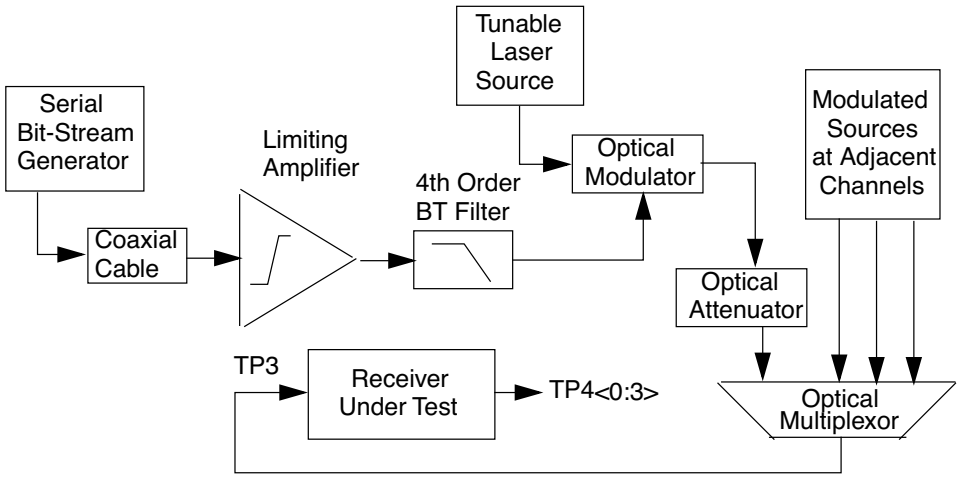


Figure 53–13—Setup for generating receiver conformance test signal at TP3

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53.9.15 Receiver test suite for WDM conformance testing

The receiver tests requiring the TP3 conformance test signal are performed on a per channel basis and shall meet the following test conditions:

a) All channels are modulated simultaneously, using valid 10GBASE-LX4 signals.
b) The center wavelengths of channels adjacent to the channel under test are tuned to the edge of their wavelength band nearest the channel under test.
c) When setting the wavelength of the channels adjacent to the channel under test, the center wavelength of the adjacent channels are set within 0.5nm of the edge of that channel's wavelength band while remaining within that channel's wavelength band.
d) In the case of the interior channels, which have two adjacent channels, each adjacent channel is tuned individually and receiver testing is done twice, once for each adjacent channel.
e) The non-adjacent channels are to be tuned to the center of their respective wavelength ranges.
f) The transmitter of the transceiver under test is operating with valid test patterns as defined in Annex 48A.

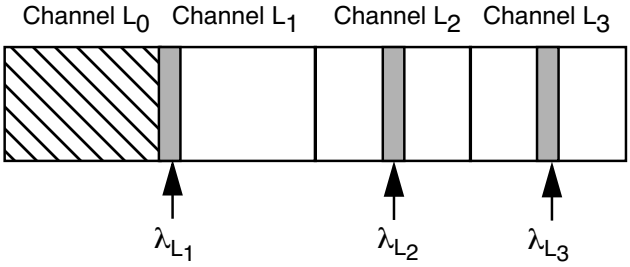
These conditions are summarized graphically in Figure 53–14 for each channel under test.

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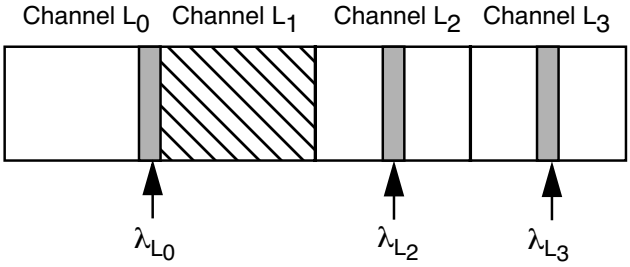
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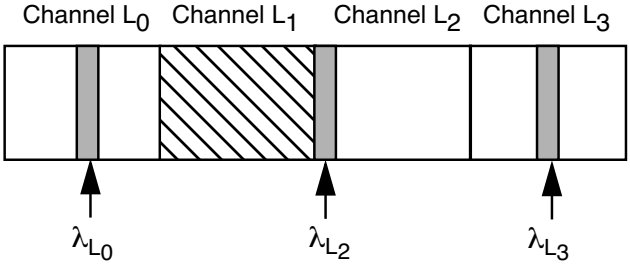
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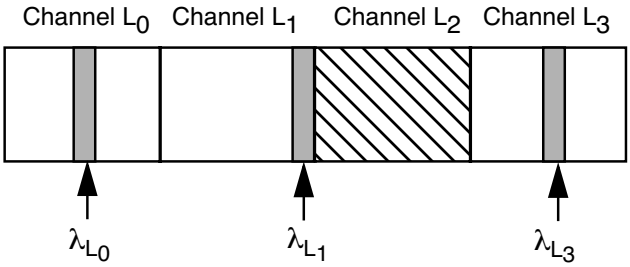
a) Channel L_0 under test



b) Channel L_1 under test (L_0 in extreme position)



c) Channel L_1 under test (L_2 in extreme position)



d) Channel L_2 under test (L_1 in extreme position)

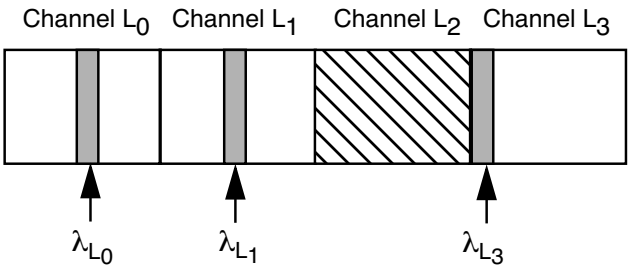
Figure 53–14—Channel test conditions for conformance test at TP3

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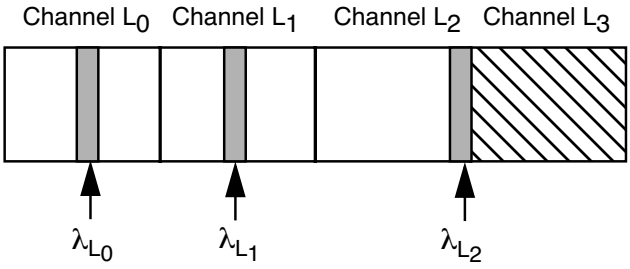
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e) Channel L_2 under test (L_3 in extreme position)



f) Channel L_3 under test (L_2 in extreme position)

Figure 53–14—Channel test conditions for conformance test at TP3 *(continued)*

NOTE—The two interior channels (L_1, L_2) require two different wavelength configurations since they have two adjacent channels. Therefore, there will be twice as many tests to perform on these channels as on exterior channels L_0, L_3.

53.10 Environmental specifications

53.10.1 General safety

All equipment meeting this standard shall conform to IEC-60950: 1991.

53.10.2 Laser safety

The 10GBASE-LX4 optical transceivers shall be Class 1 laser certified under any condition of operation in conformance to the IEC 60825-1, which has been updated by Amendment 2 (2001-01). This includes single fault conditions whether coupled into a fiber or out of an open bore.

Conformance to additional laser safety standards may be required for operation within specific geographic regions.

Laser safety standards and regulations require that the manufacturer of a laser product provide information about the product's laser, safety features, labeling, use, maintenance, and service. This documentation explicitly define requirements and usage restrictions on the host system necessary to meet these safety certifications.[19]

[19]A host system that fails to meet the manufacturers requirements and/or usage restrictions may emit laser radiation in excess of the safety limits of one or more safety standards. In such a case, the host manufacturer is required to obtain its own laser safety certification.

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53.10.3 Installation

It is recommended that proper installation practices, as defined by applicable local codes and regulation, be followed in every instance in which such practices are applicable.

53.11 Environment

Normative specifications in this clause shall be met by a system integrating a 10GBASE-LX4 PMD over the life of the product while the product operates within the manufacturer's range of environmental, power, and other specifications.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the optical link, the distance and operating environmental conditions over which the specifications of this clause will be met.

53.11.1 Electromagnetic emission

A system integrating a 10GBASE-LX4 PMD shall comply with applicable local, national, and international codes for the limitation of electromagnetic interference.

53.11.2 Temperature, humidity, and handling

The optical link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

53.12 PMD labeling requirements

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters, according to the PMD-MDI type.

PMD MDI type 10GBASE-LX4:

a) 10GBASE-LX4;
b) Applicable safety warnings.

Labeling requirements for Class 1 lasers are given in the laser safety standards referenced in 53.10.2.

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53.13 Fiber optic cabling model

The fiber optic cabling model is shown in Figure 53–15.

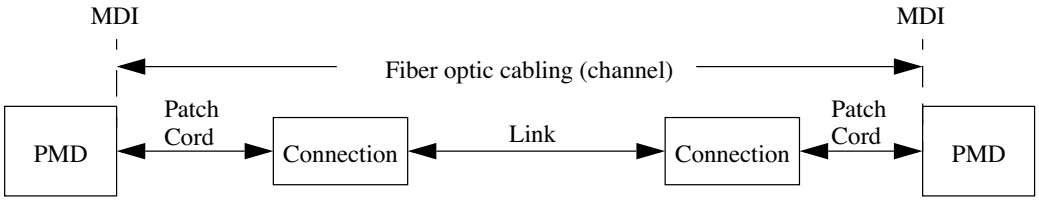


Figure 53–15—Fiber optic cabling model

The channel insertion loss is given in Table 53–13. Insertion loss measurements of installed fiber cables are made in accordance with ANSI/TIA/EIA-526-14A/method B, and ANSI/TIA/EIA-526-7/method A-1. The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment. The term channel is used here for consistency with generic cabling standards.

Table 53–13—Fiber optics cabling (channel) characteristics

Description	62.5 μm MMF	50 μm MMF		10 μm SMF	Unit
Modal bandwidth at 1300nm (min; overfilled launch)	**500**	**400**	**500**	**n/a**	**MHz•km**
Operating distance (max)	300	240	300	10 000	m
Channel insertion loss (max)[a]	2.5	2.0	2.0	6.6	dB

[a]These channel insertion loss numbers are calculated using a wavelength of 1300nm for MMF and 1310nm for SMF. An offset launch patch cord is assumed. Channel insertion loss is specified from TP2 to TP3 in Figure 53–2. The total insertion loss, when including the attenuation of the offset launch patch cord, is allowed to be 0.5dB higher than shown in the table.

53.14 Characteristics of the fiber optic cabling (channel)

The 10GBASE-LX4 fiber optic cabling shall meet the specifications defined in Table 53–13. The fiber optic cabling consists of one or more sections of fiber optic cable and any intermediate connections required to connect sections together. The fiber optic cabling spans from one MDI to another MDI, as shown in Figure 53–15.

53.14.1 Optical fiber and cable

The fiber optic cable requirements are satisfied by the fibers specified in IEC 60793-2:1992. Types A1a (50/125 μm multimode), A1b (62.5/125 μm multimode), and B1.1 (dispersion un-shifted single mode) and B1.3 (low water peak single mode) with the exceptions noted in Table 53–14.

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Table 53–14—Optical fiber and cable characteristics

Description	62.5 μm MMF	50 μm MMF	Type B1.1, B1.3 SMF	Unit
Nominal fiber specification wavelength	1300	1300	1310	nm
Fiber cable attenuation (max)	1.5	1.5	0.4[a] or 0.5[b]	dB/km
Modal Bandwidth	500	400	N/A	MHz km
(min; overfilled launch)		500	N/A	MHz km
Zero dispersion wavelength (λ_0)	$1320 \leq \lambda_0 \leq 1365$	$1295 \leq \lambda_0 \leq 1320$	$1300 \leq \lambda_0 \leq 1324$	nm
Dispersion slope (max) (S_0)	0.11 for $1320 \leq \lambda_0 \leq 1348$ and $0.001(1458 - \lambda_0)$ for $1348 \leq \lambda_0 \leq 1365$	0.11 for $1300 \leq \lambda_0 \leq 1320$ and $0.001(\lambda_0 - 1190)$ for $1295 \leq \lambda_0 \leq 1300$	0.093	ps/nm^2 km

[a]For the single-mode case, the 0.4 dB/km attenuation for optical fiber cables is defined in ITU-T G.652.
[b]For the single-mode case, the 0.5 dB/km attenuation is provided for Outside Plant cable as defined in ANSI/TIA/EIA 568-B.3-2000.
Using 0.5 dB/km may not support operation at 10 km.

53.14.2 Optical fiber connection

An optical fiber connection as shown in Figure 53–15 consists of a mated pair of optical connectors. The 10GBASE-LX4 PMD is coupled to the fiber optic cabling through a connector plug into the MDI optical receptacle, as shown in 53.14.3.

53.14.2.1 Connection insertion loss

The insertion loss is specified for a connection that consists of a mated pair of optical connectors.

The maximum link distances for multimode fiber are calculated based on an allocation of 1.5 dB total connection and splice loss. For example, this allocation supports three connections with an average insertion loss equal to 0.5 dB (or less) per connection. Connections with different loss characteristics may be used provided the requirements of Table 53–13 and Table 53–14 are met.

The maximum link distances for single-mode fiber are calculated based on an allocation of 2.0 dB total connection and splice loss. For example, this allocation supports four connections with an average insertion loss per connection of 0.5 dB. Connections with different loss characteristics may be used provided the requirements of Table 53–13 and Table 53–14 are met.

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53.14.2.2 Connection return loss

The return loss for multimode connections shall be greater than 20 dB.

The return loss for single-mode connections shall be greater than 26 dB.

53.14.3 Medium Dependent Interface (MDI)

The 10GBASE-LX4 PMD is coupled to the fiber optic cabling at the MDI. The MDI is the interface between the PMD and the fiber optic cabling. Examples of an MDI include:

a) Connectorized fiber pigtail;
b) PMD receptacle.

When connected to the fiber optic cabling, the MDI shall meet the interface performance specifications of:

a) IEC 61753-1-1—Fibre optic interconnecting devices and passive component performance standard—Part 1-1: General and guidance—Interconnecting devices (connectors).
b) IEC 61753-021-2—Fibre optic passive component performance standard—Part 021-2:Fibre optic connectors terminated on single mode fibre for Category C—Controlled environment.
c) IEC 61753-022-2—Fibre optic passive component performance standard—Part 022-2:Fibre optic connectors terminated on multimode fibre for Category C—Controlled environment.

NOTE—Compliance testing is performed at TP2 and TP3 as defined in 53.4.1, not at the MDI.

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53.15 Protocol Implementation Conformance Statement (PICS) proforma for Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4[20]

53.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4 (Long Wavelength Laser), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

53.15.2 Identification

53.15.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

53.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	

[20]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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53.15.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
LX4	10GBASE-LX4 PMD	53.1	Device supports long wavelength operation (1269-1356nm)	O/1	Yes [ ] No [ ]
*INS	Installation / cable	53.13	Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
OFP	Singlemode offset-launch mode-conditioning patch cord	53.6	Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
TP1	Standardized reference point TP1 exposed and available for testing	53.4.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Standardized reference point TP4 exposed and available for testing	53.4.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
DC	Delay constraints	53.2	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	53.3	Registers and interface supported	O	Yes [ ] No [ ]

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53.15.4 PICS proforma tables for 10GBASE-LX4 and baseband medium

53.15.4.1 PMD Functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
FN1	Integration with 10GBASE-X PCS and PMA and management functions	53.1		M	Yes [ ]
FN2	Transmit function	53.4.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
FN3	Optical multiplexing and delivery to the MDI	53.4.2	Optically multiplexes the four optical signal streams for delivery to the MDI	M	Yes [ ]
FN4	Mapping between optical signal and logical signal for transmitter	53.4.2	Higher optical power is a one	M	Yes [ ]
FN5	Receive function	53.4.3	Convey bits received from the MDI to PMD_UNITDATA.indicate(rx_bit<0:3>)	M	Yes [ ]
FN6	Conversion of four optical signals to four electrical signals	53.4.3	Converts the four optical signal streams into four electrical bit streams for delivery to the PMD service	M	Yes [ ]
FN7	Mapping between optical signal and logical signal for receiver	53.4.3	Higher optical power is a one	M	Yes [ ]
FN8	Receive function behavior	53.4.3	Conveys bits from PMD service primitive to the PMD service interface	M	Yes [ ]
FN9	Global Signal Detect function	53.4.4	Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT)	M	Yes [ ]
FN10	Global Signal Detect behavior	53.4.4	SIGNAL_DETECT is a global indicator of the presence of optical signals on all four lanes	M	Yes [ ]
FN11	Lane-by-Lane Signal Detect function	53.4.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of Table 53–4	MD:O	Yes [ ] No [ ] N/A [ ]
FN12	PMD_reset function	53.4.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] N/A [ ]

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53.15.4.2 PMD to MDI optical specifications for 10GBASE-LX4

Item	Feature	Subclause	Value/Comment	Status	Support
PMS1	Wavelength division multiplexed lane assignment	53.5	Device supports passbands defined in Table 53–5	M	Yes [ ] N/A [ ]
PMS2	Transmitter meets specifications in Table 53–7	53.7.1	Per measurement techniques in 53.9	M	Yes [ ] N/A [ ]
PMS3	Receiver meets specifications in Table 53–8	53.7.2	Per measurement techniques in 53.9	M	Yes [ ] N/A [ ]

53.15.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	Management register set	53.3		MD:M	Yes [ ] N/A [ ]
MR2	Global transmit disable function	53.4.7	Disables all of the optical transmitters with the Global_PMD_transmit_disable variable	MD:O	Yes [ ] No [ ] N/A [ ]
MR3	PMD_lane_by_lane_transmit_disable function	53.4.8	Disables the optical transmitter on the lane associated with the PMD_transmit_disable_n variable	MD:O	Yes [ ] No [ ] N/A [ ]
MR4	PMD_lane_by_lane_transmit_disable	53.4.8	Disables each optical transmitter independently if FN12 = NO	O	Yes [ ] No [ ]
MR5	PMD_fault function	53.4.9	Sets PMD_fault to a logical 1 if any local fault is detected	MD:O	Yes [ ] No [ ] N/A [ ]
MR6	PMD_transmit_fault function	53.4.10	Sets PMD_transmit_fault_n to a logical 1 if a local fault is detected on the transmit path x	MD:O	Yes [ ] No [ ] N/A [ ]
MR7	PMD_receive_fault function	53.4.11	Sets PMD_receive_fault_x to a logical 1 if a local fault is detected on the receive path x	MD:O	Yes [ ] No [ ] N/A [ ]

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53.15.4.4 Jitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
JS1	Transmit jitter	53.8.1	Meet BER “bathtub curve” specifications	M	Yes [ ]
JS2	Channel transmit jitter	53.8.1.1	As described in steps a) through c) in 53.8.1.1	M	Yes [ ]
JS3	Channel transmit jitter	53.8.1.1	Also tested on MMF as defined in 53.9.10.1	M	Yes [ ]
JS4	Receive jitter	53.8.2	BER less than 10^{-12}	M	Yes [ ]
JS5	Receive jitter	53.8.2.1	Meets requirements of the receiver input jitter mask	M	Yes [ ]
JS6	Receive jitter	53.8.2.1	Uniform spectral content over the measurement frequency range of 18.75kHz to 1.5GHz	M	Yes [ ]
JS7	Receive jitter	53.8.2.1	Using a Clock Recovery Unit	M	Yes [ ]
JS8	Receive jitter	53.8.2.1	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
JS9	Receive jitter	53.8.2.1	Using fourth-order Bessel-Thomson filter	M	Yes [ ]
JS10	Receive jitter	53.8.2.2	Meets the requirements of Table 53–11	M	Yes [ ]
JS11	Receive jitter	53.8.2.2	Sinusoidal jitter added to the test signal in compliance with 53.8.2.1	M	Yes [ ]

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53.15.4.5 Optical measurement requirements

Item	Feature	Subclause	Value/Comment	Status	Support
OM1	Length of patch cord used for measurements	53.9	2 to 5 m	M	Yes [ ]
OM2	Wavelength ranges	53.9.1	Wavelengths fall within ranges specified inTable 53–5, and under modulated conditions using valid 10GBASE-X signals	M	Yes [ ]
OM3	Optical power measurements	53.9.2	Per TIA/EIA-455-95	M	Yes [ ]
OM4	Source spectral window measurements	53.9.3	Individually measured per test setup in Figure 53–7, with all other channels below –30 dBm	M	Yes [ ]
OM5	Source spectral window measurements	53.9.3	Under modulated conditions using valid 10GBASE-X signals	M	Yes [ ]
OM6	Extinction ratio measurements	53.9.4	Per ANSI/TIA/EIA-526-4A	M	Yes [ ]
OM7	OMA measurements	53.9.5	Each channel tested individually per methodology defined in 52.9.5	M	Yes [ ]
OM8	$RIN_{12}OMA$	53.9.6	Each channel tested individually per methodology defined in 52.9.6		Yes [ ]
OM9	Transmit eye	53.9.7	Per ANSI/TIA/EIA-526-4A (OFSTP-4)	M	Yes [ ]
OM10	Transmit eye mask measurement conditions	53.9.7	Using fourth-order Bessel-Thomson filter	M	Yes [ ]
OM11	Transmit eye mask measurement conditions	53.9.7	Using a Clock Recovery Unit to trigger the scope	M	Yes [ ]
OM12	Transmit eye mask measurement conditions	53.9.7	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM13	Transmit rise/fall characteristics conditions	53.9.8	Waveforms conform to mask in Figure 53–8, measured from 20% to 80%, using a patch cord	M	Yes [ ]
OM14	Transmit rise/fall characteristics conditions	53.9.8	Removed mask conforming filter mathematically	M	Yes [ ]
OM15	Transmit rise/fall characteristics conditions	53.9.8	Mask filters use a fourth-order Bessel-Thomson filter	M	Yes [ ]
OM16	Receive sensitivity measurement conditions	53.9.9	Using conformance test at TP3 and meeting conditions specified in Table 53–8	M	Yes [ ]
OM17	Transmit jitter conformance measurement conditions	53.9.10.1	Using a fourth-order Bessel-Thomson filter for single-mode fiber	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM18	Transmit jitter conformance measurement conditions	53.9.10.1	Using a fourth-order Bessel-Thomson filter followed by a transversal filter with 2 equal amplitude paths with a differential delay of 157ps for multimode fiber	M	Yes [ ]
OM19	Transmit jitter conformance measurement conditions	53.9.10.1	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM20	Transmit jitter conformance measurement conditions	53.9.10.1	Measured at the average value of the overall waveform	M	Yes [ ]
OM21	Transmit jitter conformance measurement conditions	53.9.10.1	Asynchronous data flowing in all four optical receiver channels	M	Yes [ ]
OM22	Transmit jitter conformance measurement conditions	53.9.10.2	Meets requirements listed in Table 53–12	M	Yes [ ]
OM23	Transmit jitter conformance measurement conditions	53.9.10.2	For single-mode fiber; compliant with dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion”	M	Yes [ ]
OM24	Transmit jitter conformance measurement conditions	53.9.10.2	Achieved using ITU-T G.652 fiber	M	Yes [ ]
OM25	Transmit jitter conformance measurement conditions	53.9.10.2	Using the linear regime of the single-mode fiber	M	Yes [ ]
OM26	Transmit jitter conformance measurement conditions	53.9.10.2	Provide an optical back reflection specified in Table 53–7	M	Yes [ ]
OM27	Transmit jitter conformance measurement conditions	53.9.10.2	Back reflection adjusted to create the greatest RIN	M	Yes [ ]
OM28	Transmit jitter conformance measurement conditions	53.9.10.2	For multimode fiber, back reflection set to –12dB	M	Yes [ ]
OM29	Transmit jitter conformance measurement conditions	53.9.10.3	Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade	M	Yes [ ]
OM30	Receiver sensitivity	53.9.11	Meet the specifications in Table 53–8	M	Yes [ ]
OM31	Stressed receiver conformance conditions	53.9.12	Asynchronous data flowing out of the optical transmitter of the system under test	M	Yes [ ]
OM32	Stressed receiver conformance conditions	53.9.12	Data is consistent with normal signal properties and content	M	Yes [ ]
OM33	Stressed receiver conformance conditions	53.9.12.1	Using a Clock Recovery Unit meeting the requirements of 53.8.2.1	M	Yes [ ]
OM34	Stressed receiver conformance conditions	53.9.12.1	Calibrated at the average value of the overall optical waveform	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
OM35	Stressed receiver conformance conditions	53.9.12.3	Using a Clock Recovery Unit meeting the requirements of 53.8.2.1	M	Yes [ ]
OM36	Receiver 3dB electrical upper cutoff frequency	53.9.13	Performed on each channel independently using a laser source with its output wavelength within the specified wavelength range of the channel to be tested	M	Yes [ ]
OM37	Receiver 3dB electrical upper cutoff frequency	53.9.13	As described in steps a) through e) of 53.9.13	M	Yes [ ]
OM38	Compliance test signal at TP3	53.9.14	Meets the requirements of Figure 53–12	M	Yes [ ]
OM39	Compliance test signal at TP3	53.9.14	DJ eye closure no less than 14ps	M	Yes [ ]
OM40	Compliance test signal at TP3	53.9.14	Vertical eye-closure penalty meets requirements of Table 53–8	M	Yes [ ] N/A [ ]
OM41	Compliance test signal at TP3	53.9.14	Bandwidth of photodetector > 2.34GHz, and couple through fourth-order Bessel-Thomson filter	M	Yes [ ]
OM42	Receiver WDM conformance conditions	53.9.15	As described in steps a) through f) of 53.9.15	M	Yes [ ]
OM43	General safety	53.10.1	Conform to IEC-60950: 1991	M	Yes [ ]
OM44	Laser safety	53.10.2	Class 1	M	Yes [ ]
OM45	Compliance with all requirements over the life of the product	53.11		M	Yes [ ]
OM46	Compliance with applicable local and national codes for the limitation of electromagnetic interference	53.11.1		M	Yes [ ]

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53.15.4.6 Characteristics of the fiber optic cabling

Item	Feature	Subclause	Value/Comment	Status	Support
LI1	Fiber optic cabling	53.13	Meets specifications in Table 53–13	INS:M	Yes [ ] N/A [ ]
LI2	Return loss for multimode connections	53.14.2.2	> 20 dB	INS:M	Yes [ ] No [ ] N/A [ ]
LI3	Return loss for singlemode connections	53.14.2.2	> 26 dB	INS:M	Yes [ ] No [ ] N/A [ ]
LI4	MDI	53.14.3	IEC 61753-1-1 and IEC 61753-3-2	M	Yes [ ]

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Annex 44A

(informative)

Diagram of Data Flow

This annex contains diagrams of the data flow from the MAC to the MDI in the transmit direction and from the MDI to the MAC in the receive direction. The diagrams are provided as a reference, and the corresponding clause should be reviewed for the complete information.

44A.1 10GBASE-R bit ordering

Figure 44A–1 shows the bit ordering on the LAN serial transmit data path.

Figure 44A–2 shows the bit ordering on the LAN serial receive data path.

The 10GBASE-R diagrams reference the following clauses: 46 (XGMII and RS), 47 (XGXS and XAUI), 49 (64B/66B PCS), and 51 (serial PMA).

44A.2 10GBASE-W serial bit ordering

Figure 44A–3 shows the bit ordering on the WAN serial transmit data path.

Figure 44A–4 shows the bit ordering on the WAN serial receive data path.

The 10GBASE-W serial diagrams reference the following clauses: 46 (XGMII and RS), 47 (XGXS and XAUI), 49 (64B/66B PCS), 50 (WIS), and 51 (serial PMA).

44A.3 10GBASE-LX4 bit ordering

Figure 44A–5 shows the bit ordering on the LAN WDM transmit path.

Figure 44A–6 shows the bit ordering on the LAN WDM receive path.

The 10GBASE-LX4 diagrams reference the following clauses: 46 (XGMII and RS) and 48 (8B/10B PCS and PMA).

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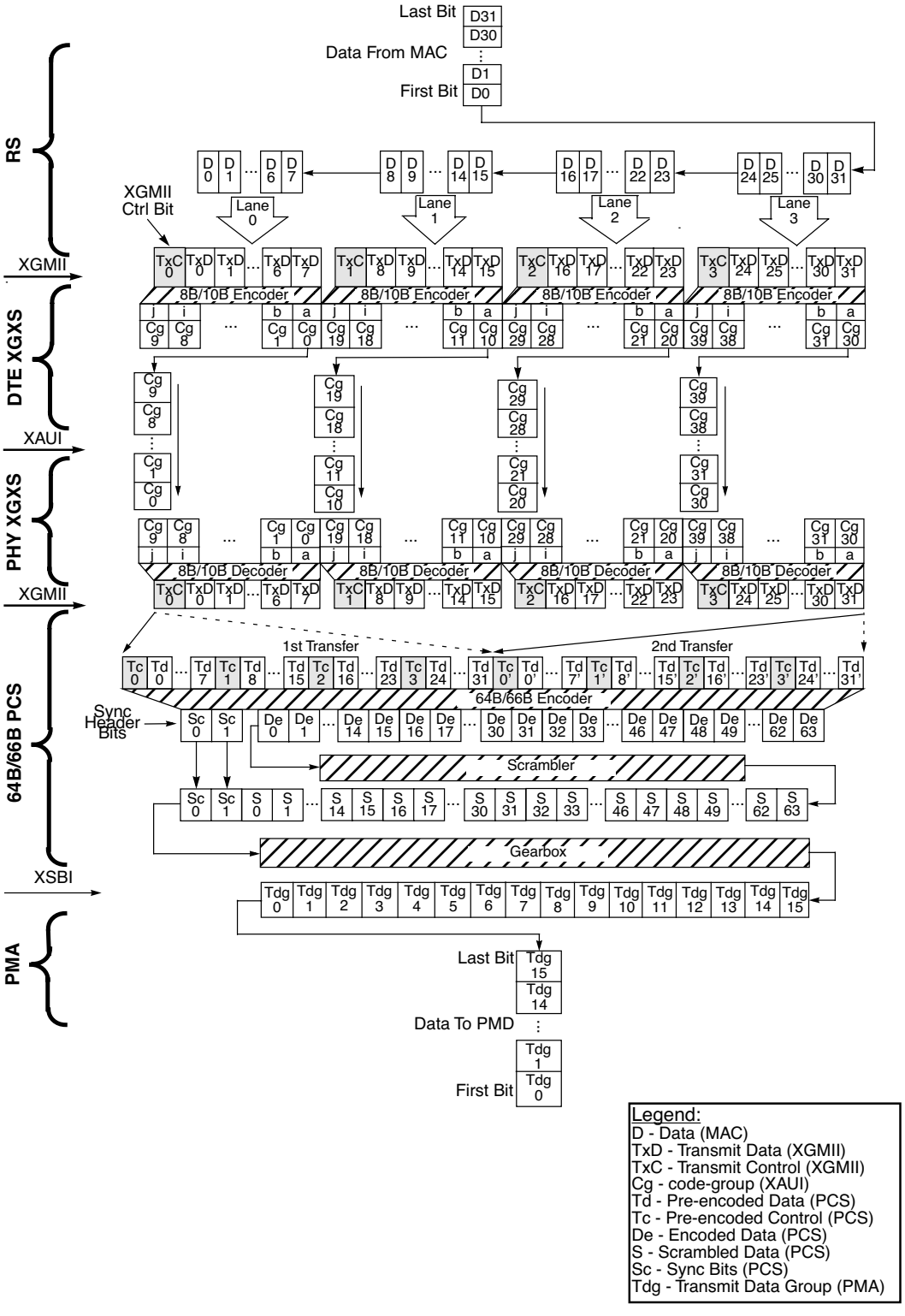


Figure 44A–1—10GBASE-R transmit data path bit ordering

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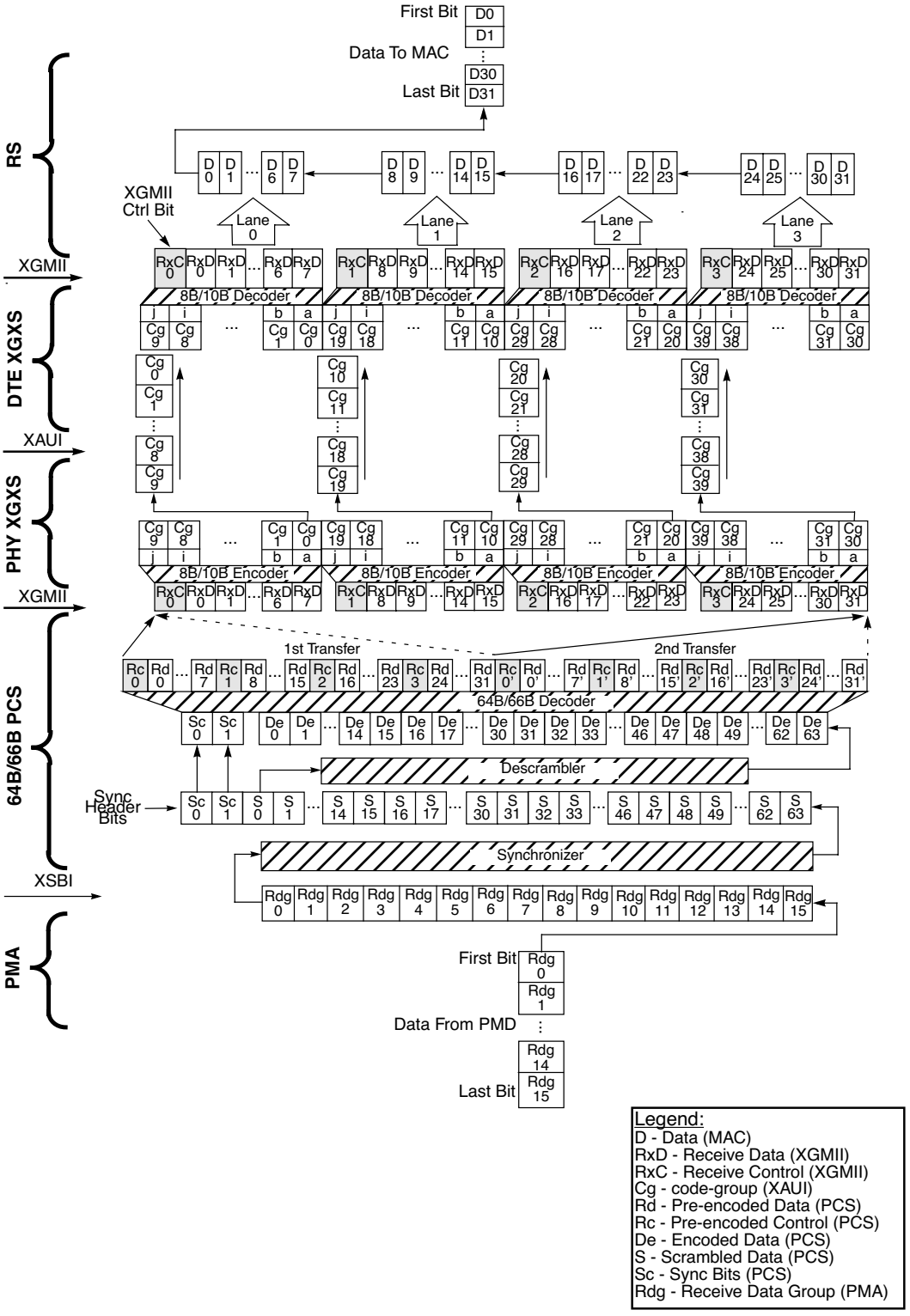


Figure 44A–2—10GBASE-R receive data path bit ordering

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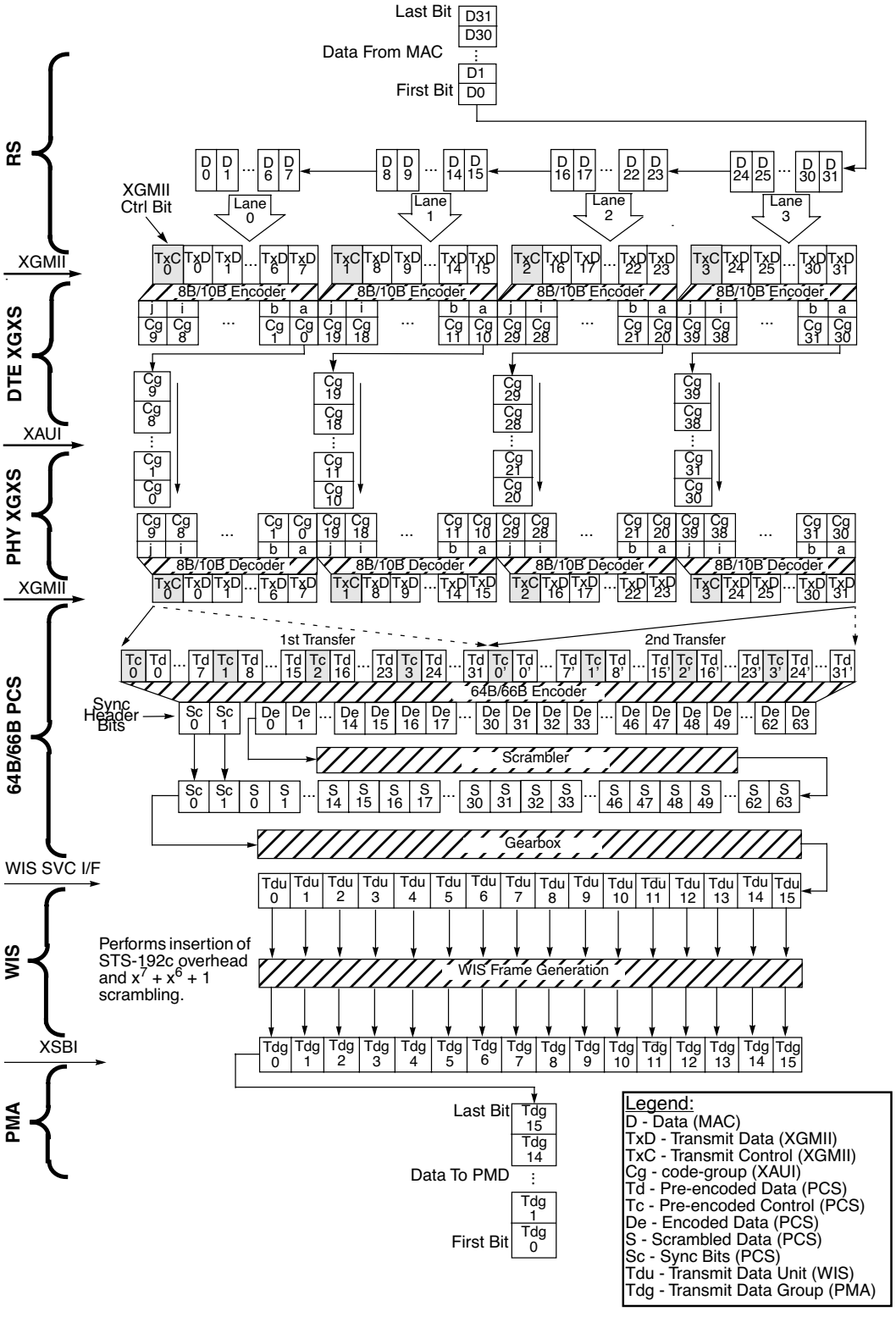


Figure 44A–3—10GBASE-W serial transmit data path bit ordering

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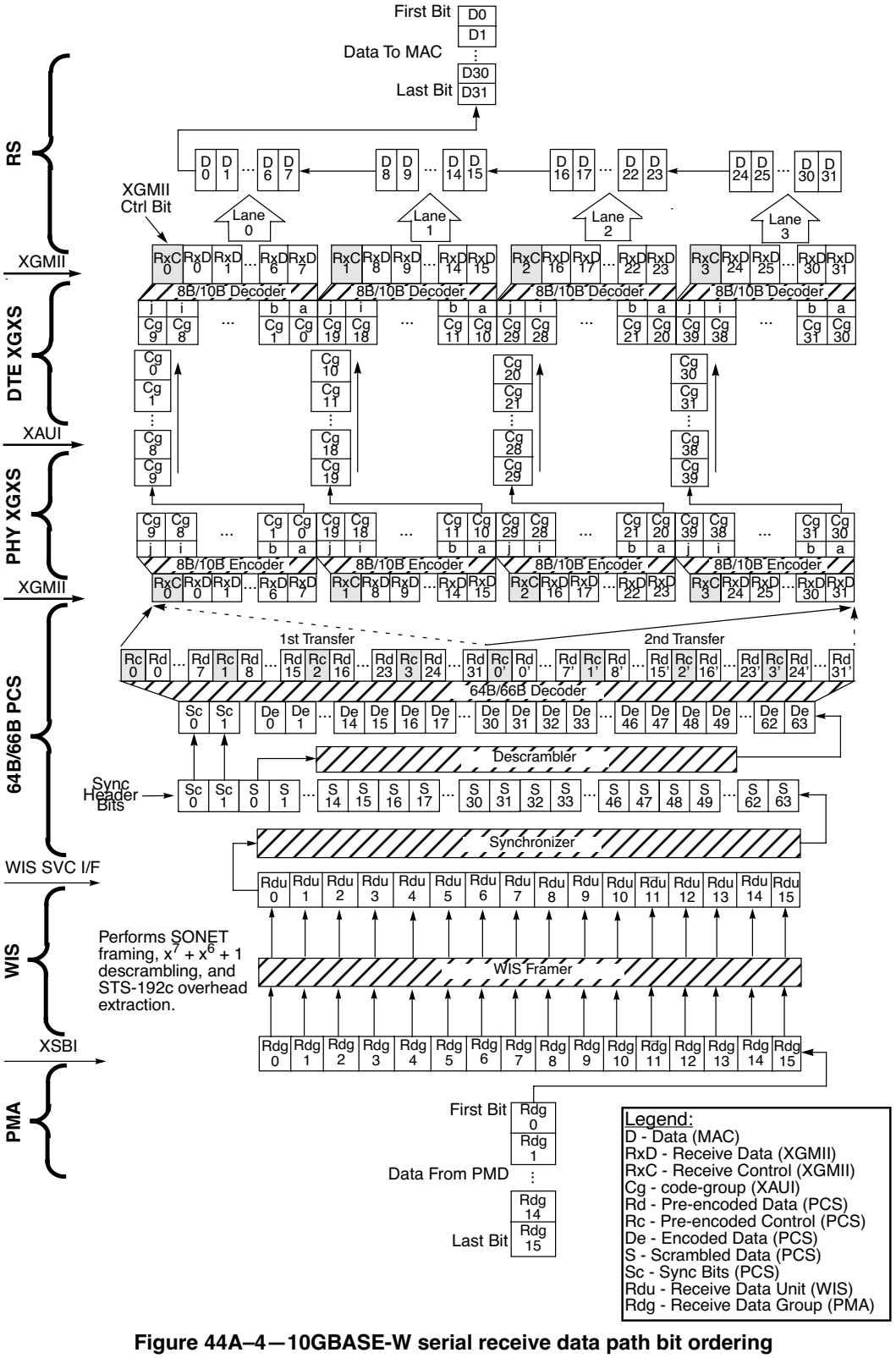


Figure 44A–4—10GBASE-W serial receive data path bit ordering

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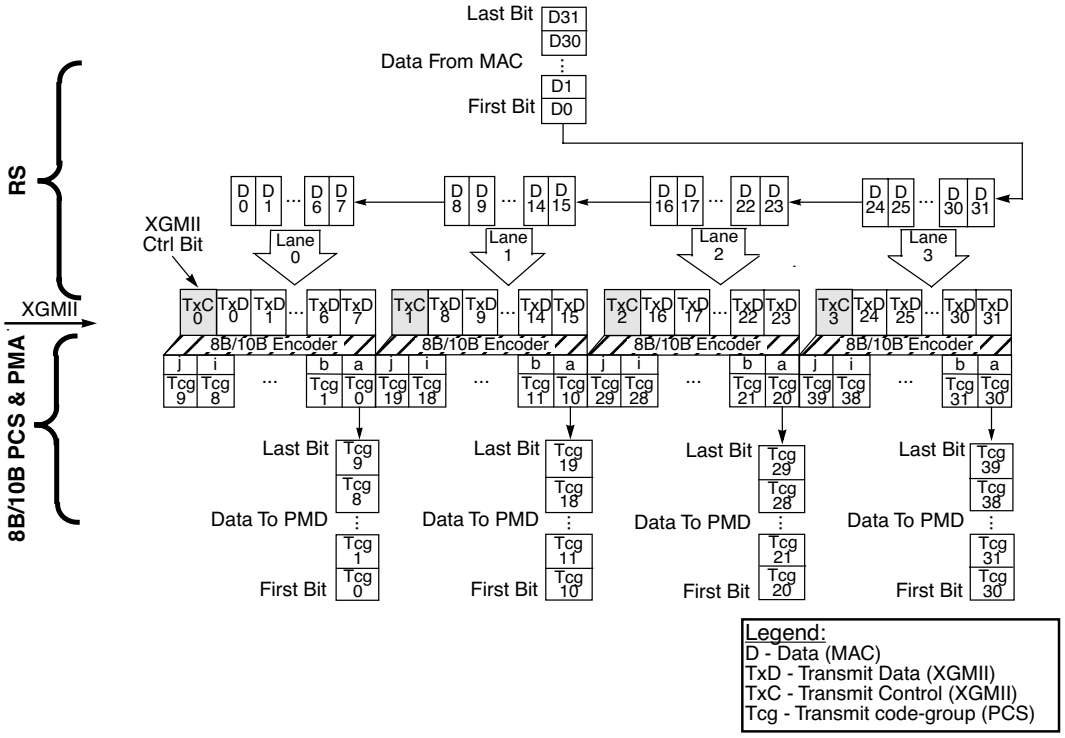


Figure 44A–5—10GBASE-LX4 transmit data path bit ordering

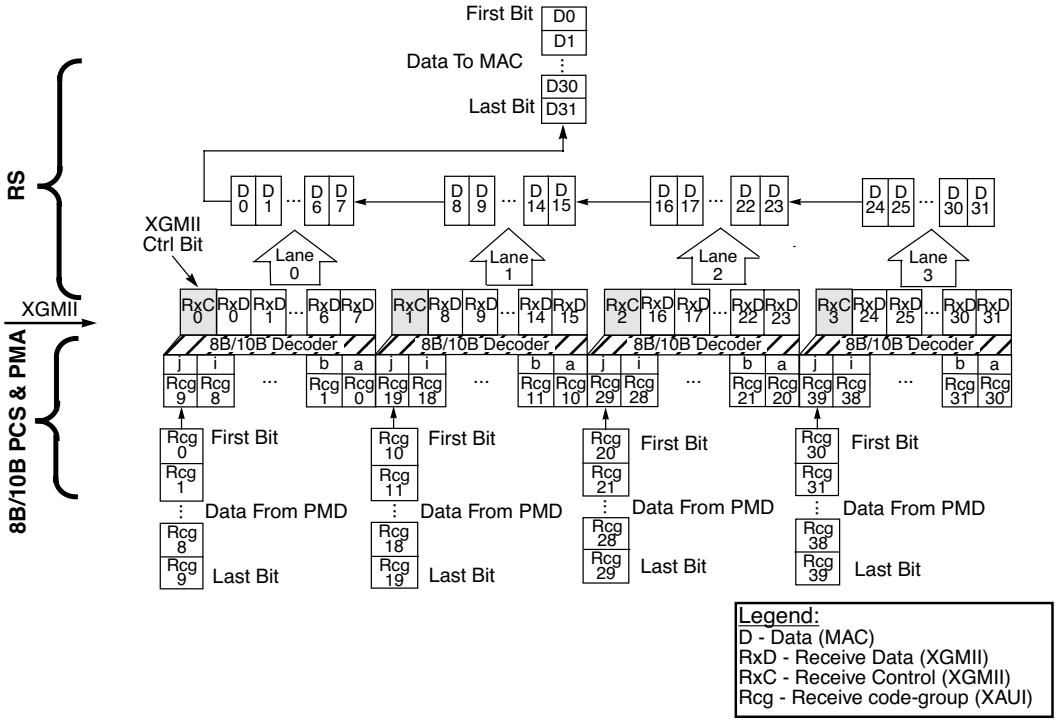


Figure 44A–6—10GBASE-LX4 receive data path bit ordering

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44A.4 Loopback locations

Figure 44A–7 diagrams the impact of the various loopback signals on the generation of signal detect and local fault. Clause 46 describes the handling of local fault via the XGMII. If the WIS is not present, the PMA_SIGNAL.indicate passes directly from the PMA sublayer to the PCS as is the case in 10GBASE-X and 10GBASE-R devices.

Figure 44A–7 represents an implementation of loopback where loopback is implemented in accordance with the recommendation that it exercises as much of the circuitry in the sublayer as possible. If the loopback is implemented above part of the circuitry in a sublayer, then any data valid signals produced below the loopback point should be ignored during loopback as are any data valid signals from below the sublayer. For instance, if loopback in a WIS implementation was done above the framer, then data valid signals from the framer should be logically OR'ed with loopback.

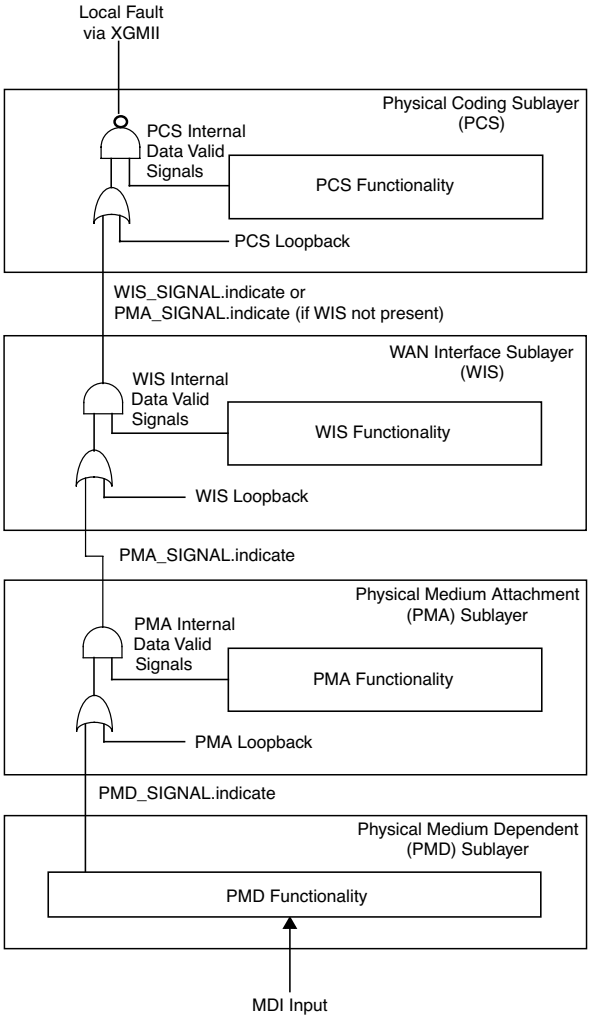


Figure 44A–7—Signal Detect handling across sublayers

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Annex 45A

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Clause 45 MDIO electrical interface

45A.1 MDIO driver

It is possible to implement the MDIO electrical driver using an open drain driver, as the MDIO signal is pulled up to 1.2V using a resistor. This is shown in Figure 45A–1.

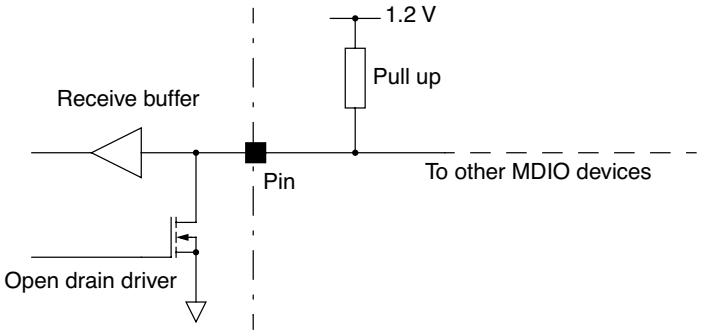


Figure 45A–1—Use of open drain driver for MDIO electrical interface

45A.2 Single Clause 45 electrical interface

As the Clause 45 MDIO electrical interface is significantly different from the Clause 22 MII Management electrical interface, it is not possible to directly attach a Clause 45 MMD to a Clause 22 MII Management Interface. Clause 45 MMDs that include Clause 22 registers may have their Clause 22 registers accessed via the Clause 45 electrical interface. This obviates the requirement to provide a Clause 22 compliant electrical interface in such systems. This is shown in Figure 45A–2.

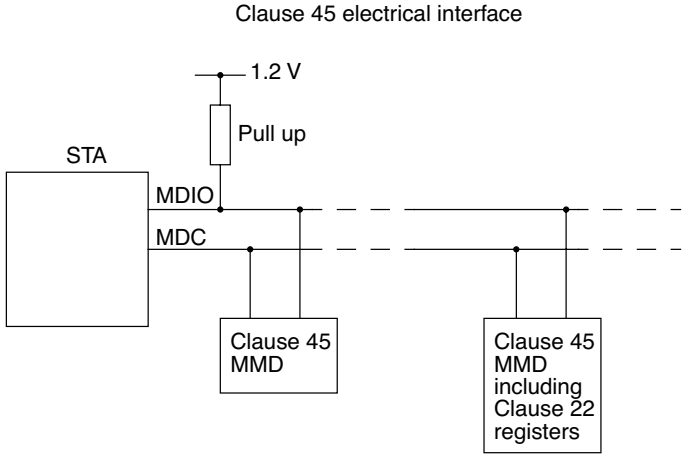


Figure 45A–2—Support of Clause 22 registers via the Clause 45 MDIO interface

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45A.3 Clause 45 electrical interface for STA with Clause 22 electrical interface to PHYs

If Clause 22 PHYs are to be attached to a Clause 45 MDIO interface, then a protocol aware voltage translation device is required. This arrangement is shown in Figure 45A–3. Such a translation device must correctly drive both the Clause 45 MDIO interface and the Clause 22 MII Management interface using the voltages and timings specified in the appropriate clause. In order to drive the interfaces correctly, the device must have knowledge of the Clause 22 PHY addresses present on the Clause 22 Management interface. When any PHY attached to the Clause 22 MII Management interface is driving the MDIO, the translation device must drive the Clause 45 MDIO interface with the same logical state that is being driven on to the Clause 22 Management interface by the PHY. Whenever the STA drives the Clause 45 MDIO interface, the translation device must drive the Clause 22 Management interface with the same logical state that is being driven on to the Clause 45 MDIO interface. In addition, the translation device must drive the Clause 45 MDC on to the Clause 22 Management interface. Even though the Clause 45 MDIO frames using the ST=00 frame code will also be driven on to the Clause 22 MII Management interface, the Clause 22 PHYs will ignore the frames.

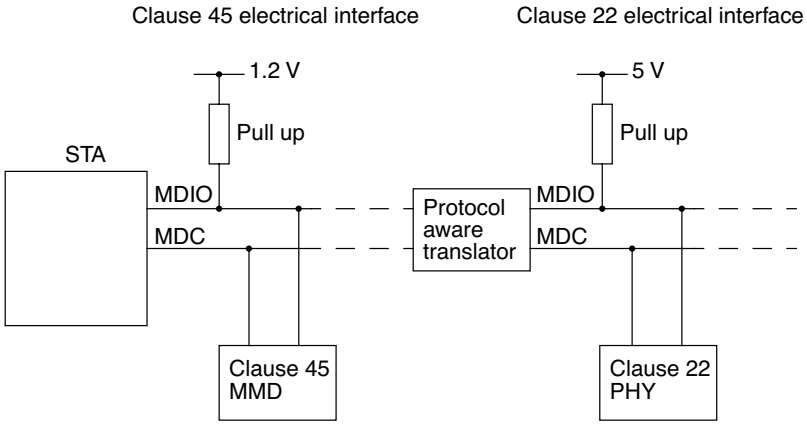


Figure 45A–3—Protocol aware voltage translator between Clause 45 and Clause 22

45A.4 Clause 22 electrical interface for STA with Clause 45 electrical interface to MMDs

If Clause 45 MMDs are to be attached to a Clause 22 MII management interface, then a protocol aware voltage translation device is required. This arrangement is shown in Figure 45A–4. Such a translation device must correctly drive both the Clause 22 MII Management interface and the Clause 45 MDIO interface using the voltages and timings specified in the appropriate clause. In order to drive the interfaces correctly, the device must have knowledge of any Clause 22 PHY addresses present within MMDs attached to the Clause 45 MDIO Management interface. When any Clause 45 MMD, including embedded Clause 22 PHYs, attached to the Clause 45 MDIO Management interface is driving the MDIO, the translation device must drive the Clause 22 MII Management interface with the same logical state that is being driven on to the Clause 45 MDIO interface by the PHY. Whenever the STA drives the Clause 22 MII Management interface, the translation device must drive the Clause 45 MDIO interface with the same logical state that is being driven on to the Clause 22 MII Management interface. In addition, the translation device must drive the Clause 22 MII Management interface MDC on to the Clause 45 MDIO interface. The Clause 22 MII Management interface must be capable of generating the MDIO frame structure specified in Clause 45. Even though the Clause 45 MDIO frames using the ST=00 frame code will be driven on to the Clause 22 MII Management interface, the Clause 22 PHYs will ignore such frames.

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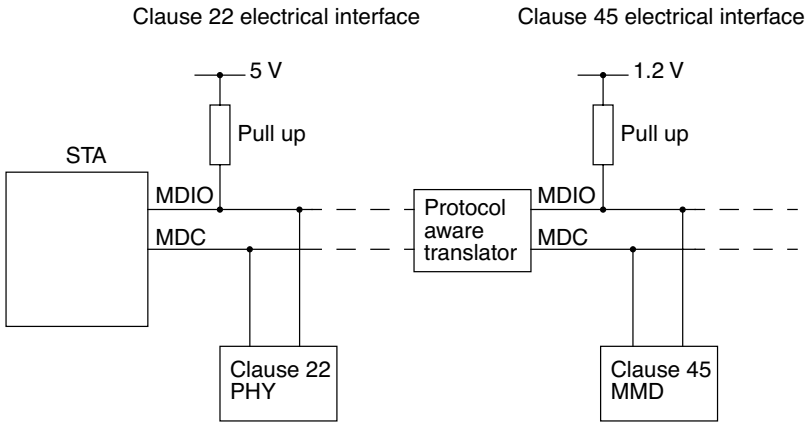


Figure 45A–4—Protocol aware voltage translator between Clause 22 and Clause 45

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Annex 48A

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Jitter test patterns

This annex defines test patterns which allow the 10GBASE-X PHY described in Clause 48 to test either its attached PMD described in Clause 53 or its XAUI interface described in Clause 47 for compliance in a system environment, or for unspecified diagnostic purposes. The patterns may be implemented at a bit, code-group or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences; however, system debug can be improved if a receiver is able to test for one or more of these patterns and report bit errors (e.g., 8B/10B decoder errors) back to the user.

48A.1 High-frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This pattern is not intended for jitter compliance testing. This high-frequency test pattern generates a one, or light on, for a duration of 1 bit time, followed by a zero, or light off, for a duration of 1 bit time. This pattern repeats continuously on each lane for the duration of the test. For example, 10101010101010101010101010101010101010...

NOTE—This pattern can be generated by the repeated transmission of the D21.5 code-group on each lane. Disparity rules are followed.

48A.2 Low-frequency test pattern

The intent of this test pattern is to test low-frequency RJ and also to test PLL tracking error. This pattern is not intended for jitter compliance testing. This low-frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 5 bit times. This pattern repeats continuously on each lane for the duration of the test. For example, 11111000001111100000111110000011111100000...

NOTE—This pattern can be generated by the repeated transmission of the K28.7 code-group on each lane. Disparity rules are followed.

48A.3 Mixed-frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ) due to high-frequency ISI. This pattern is not intended for jitter compliance testing. This mixed-frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously on each lane for the duration of the test. For example, 11111010110000010100111110101100000010100...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group on each lane. Disparity rules are followed.

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48A.4 Continuous random test pattern (CRPAT)

The continuous random test pattern is intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level. This pattern is not intended for jitter compliance testing.

NOTE—The basis of this pattern may be found in NCITS TR-25:1999, "Methodology of Jitter Specification". This Annex uses similar modifications to fit the RPAT test pattern into an IEEE 802.3 frame.

The continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in Clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

START/PREAMBLE/SFD:

FB 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (REPEAT ENTIRE SEQUENCE 31 TIMES CONSECUTIVELY):

BE for 4 Octets;

D7 for 4 Octets;

23 for 4 Octets;

47 for 4 Octets;

6B for 4 Octets;

8F for 4 Octets;

B3 for 4 Octets;

14 for 4 Octets;

5E for 4 Octets;

FB for 4 Octets;

35 for 4 Octets;

59 for 4 Octets.

CRC

F8 79 05 59

IPG

FD 07 07 07 07 07 07 07 07 07 07 07

END

NOTE—The data values for this pattern are in hexadecimal.

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48A.5 Continuous jitter test pattern (CJPAT)

The continuous jitter test pattern is intended to expose a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low-transition density patterns with repeating high-transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye. The following pattern is intended for receive jitter compliance testing.

NOTE—The basis of this pattern may be found in NCITS TR-25:1999. This annex uses similar modifications to fit the JTPAT test pattern into an IEEE 802.3 frame.

The continuous jitter test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters, as specified in Clause 48, in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous jitter test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1504 data octets, plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

START/PREAMBLE/SFD:

FB 55 55 55 55 55 55 D5

MODIFIED JTPAT SEQUENCE

0B for 1 Octet (lane 0);

7E for 3 Octets (lanes 1, 2, 3);

7E for 524 Octets—Low Density Transition Pattern;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

AB for 4 Octets—Phase Jump;

B5 for 160 Octets—High Density Transition Pattern;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

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F4 for 4 Octets—Phase Jump;

7E for 528 Octets—Low-Density Transition Pattern;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

AB for 4 Octets—Phase Jump;

B5 for 160 Octets—High-Density Transition Pattern;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump;

EB for 4 Octets—Phase Jump;

F4 for 4 Octets—Phase Jump.

CRC

BD 9F 1E AB

IPG

FD 07 07 07 07 07 07 07 07 07 07 07

END

NOTE—The data values for this pattern are in hexadecimal.

48A.5.1 Continuous jitter test pattern (CJPAT) 10 bit values

The following tables depict a 10-bit encoding for CJPAT. This is the encoding which will occur when each lane has negative disparity before the Start column. The actual 10-bit encoding sent when CJPAT is transmitted will be one of 16 encodings depending upon the disparity of each lane at the beginning of the packet. CJPAT has been designed to produce the same disparity on each lane after the Terminate

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column as that lane had before the Start column. When CJPAT is sent continuously, two of the sixteen possible encodings will occur because Idle will either leave the disparity the same or flip the disparity on all lanes.

Table 48A–1—Start/Preamble/SFD/First 8 Data Octets

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
FB	1101101000	55	1010100101	55	1010100101	55	1010100101
55	1010100101	55	1010100101	55	1010100101	D5	1010100110
0B	1101001011	7E	0111100011	7E	0111100011	7E	0111100011
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100

Table 48A–2—Low density transition pattern (repeat 65 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
7E	0111100011	7E	0111100011	7E	0111100011	7E	0111100011
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100

Table 48A–3—Phase Jump

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111
AB	1101001010	AB	1101001010	AB	1101001010	AB	1101001010

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Table 48A–4—High density transition pattern (repeat 20 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010

Table 48A–5—Phase jump (repeat 4 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
EB	1101001000	EB	1101001000	EB	1101001000	EB	1101001000
F4	0010110111	F4	0010110111	F4	0010110111	F4	0010110111

Table 48A–6—Low density transition pattern (repeat 66 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
7E	1000011100	7E	1000011100	7E	1000011100	7E	1000011100
7E	0111100011	7E	0111100011	7E	0111100011	7E	0111100011

Table 48A–7—Phase Jump

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001
AB	1101001010	AB	1101001010	AB	1101001010	AB	1101001010

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Table 48A–8—High density transition pattern (repeat 20 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010
B5	1010101010	B5	1010101010	B5	1010101010	B5	1010101010

Table 48A–9—Phase jump (repeat 4 times)

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
EB	1101001110	EB	1101001110	EB	1101001110	EB	1101001110
F4	0010110001	F4	0010110001	F4	0010110001	F4	0010110001

Table 48A–10—CRC/Terminate/IPG

Lane0 abcdei fghj		Lane1 abcdei fghj		Lane2 abcdei fghj		Lane3 abcdei fghj	
BD	1011101010	9F	1010110010	1E	0111100100	AB	1101001010
FD	0100010111	07	0011111010	07	0011111010	07	0011111010
07	1100001100	07	1100001100	07	1100001100	07	1100001100
07	0011110100	07	0011110100	07	0011110100	07	0011110100

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Annex 48B

(informative)

Jitter test methods

This annex specifies the definitions and measurement requirements for the jitter specification of the XGXS and XAUI described in Clause 47 and the 10GBASE-LX4 PMD described in Clause 53. These measurement methods and specifications are intended to be used for jitter and wander compliance testing, but are not definitive.

While jitter specifications are required to be met for all lanes during operation, the methods described in this annex are written for testing of a single lane. Each lane can be tested with these methods individually or concurrently.

48B.1 BER and jitter model

Measurement of BER within a data eye is not only the fundamental indicator of signal quality, it is a valuable tool to infer jitter properties. Insight into the relationship between jitter, eye opening and error rate can be gained through mathematical modeling.

48B.1.1 Description of dual dirac mathematical model

Figure 48B–1considers a typical eye diagram that may be seen on an oscilloscope. For the purpose of discussion, assume that an ideal trigger source is used so that the eye is accurately depicted. Jitter is indicated by distributed transitions (crossings) of the threshold as the data toggles between logic states. Histograms of transition regions can be taken at the threshold level. The width of the histograms can then be estimated, including standard deviation, etc.

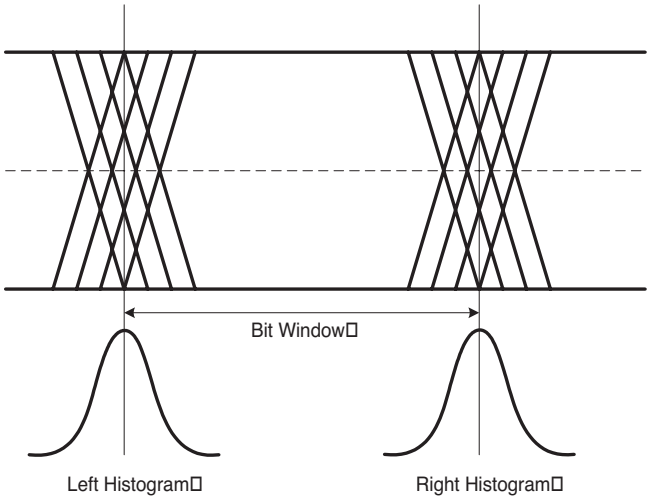


Figure 48B–1—Eye Diagram sketch

The histograms represent probability density functions (PDFs) of the jitter and statistically describe the locations in time of the transitions. The PDFs are placed with their means at the ideal transition times of the logic

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states. To simplify matters, the time scale is given in terms of unit intervals (UI) with 0.5 located at the exact center of the eye. The means of the two PDFs are at 0 and +1 UI.

Ideally, the receiver samples the eye at the center where the tails of the transition histograms are small, as shown in Figure 48B–2. To calculate the probability of either transition causing an error due to jitter, the area under its PDF tail on the errored side of the sample point (time) must be calculated. This is the complementary cumulative distribution function, or CDF. For the left hand PDF, the tail is integrated from to the sample point to $+\infty$; the right hand PDF's tail is integrated from $-\infty$ to the sample point. The overall probability of transition error is the sum of the two CDFs. It is assumed that the tails of the neighboring bits do not contribute to the probability of error.

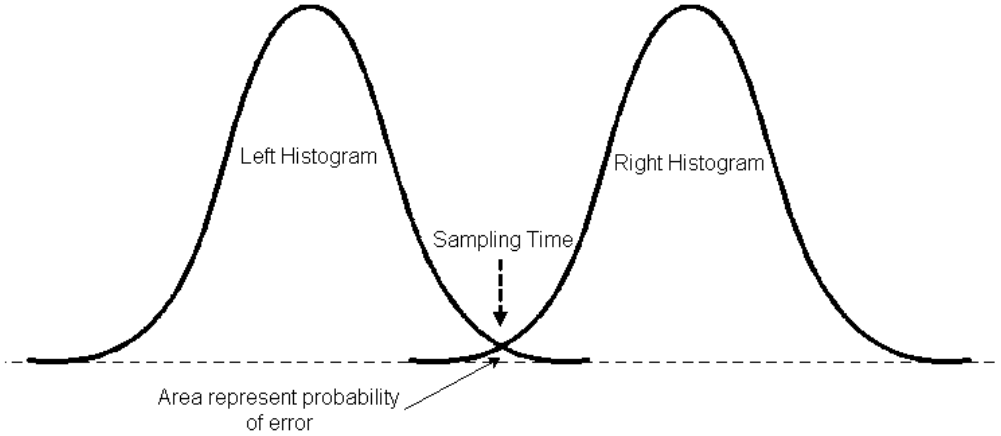


Figure 48B–2—Eye sampling and probability of error

To determine the BER, the probability of a transition-caused error must be multiplied by the probability of a transition occurring. Nominally, the latter may be seen as the average transition density. This model assumes typical data streams have a transition density of 50%.

To demonstrate these concepts, define a general jitter PDF, $JT(\tau, W, \sigma)$, centered at 0, where τ is time, W is the pk-pk value of deterministic jitter, and σ is the rms value of random jitter. The left PDF histogram (centered at 0) causes bit errors as:

$$BER_{left}(\tau_{sample}, W, \sigma) = \Gamma_{transistion} \cdot \int_{\infty}^{\tau_{sample}} JT(\tau, W, \sigma)\delta\tau \quad (48B\text{-}1)$$

where τ_{sample} is the sampling instant in time, and $\Gamma_{transistion}$ is the transition density. Similarly, the right PDF histogram (shifted and centered at 1 UI) causes bit errors as

$$BER_{right}(\tau_{sample}, W, \sigma) = \Gamma_{transistion} \cdot \int_{-\infty}^{\tau_{sample}} JT(\tau - UI, W, \sigma)\delta\tau \quad (48B\text{-}2)$$

The sum of these two functions provides the total (BER) due to jitter,

$$BER_{total}(\tau_{sample}, W, \sigma) = BER_{left}(\tau_{sample}, W, \sigma) + BER_{right}(\tau_{sample}, W, \sigma) \quad (48B\text{-}3)$$

In the BERT scan, BER is measured as the sample point, τ_{sample} , is swept between the two eye crossings. The probability of error as a function of the sample point is commonly known as a BER bathtub curve.

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48B.1.2 Random Jitter

For random or Gaussian jitter (RJ) only the standard deviation, σ , is necessary to define the PDF

$$RT(\tau, \sigma) = \frac{1}{\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot e^{-\left(\frac{\tau^2}{2\sigma^2}\right)} \quad \text{(48B-4)}$$

The CDF for this Gaussian PDF function is the complementary error function (erfc).

48B.1.3 Addition of Deterministic Jitter

Total jitter is comprised of both random and deterministic components. The DJ component can be defined, as for RJ, by a PDF, where the combined total jitter PDF is a convolution of the DJ and RJ PDFs.

Simple peak-to-peak is insufficient as the measurement of DJ. An overall weighting function that captures not only the peak-to-peak but also the shape of the density function is required. This may be known as "effective DJ." For purposes of simplicity, effective DJ in this annex is based on the dual Dirac function, where it is assumed that the DJ PDF is comprised only of a pair of delta functions. Other PDFs are certainly possible, however, in the prediction of low BERs, this simplication is sufficient. All references to DJ in Clauses 47 and 53 should be understood as effective DJ.

An example of effective DJ is duty cycle distortion (DCD), which when convolved with RJ results in two Gaussian functions, one centered at each of the two delta functions.

The magnitude of the DJ, is given as peak-to-peak amplitude, W. Therefore, each delta function is offset from the mean crossing position by the peak value of DJ, W/2. The PDF for deterministic jitter, centered at 0, is therefore defined as:

$$JT(\tau, W, \sigma) = \frac{\delta\left(\tau, -\frac{W}{2}\right)}{2} + \frac{\delta\left(\tau, \frac{W}{2}\right)}{2} \quad \text{(48B-5)}$$

When convolved with random jitter, the PDF, centered at 0, becomes:

$$JT(\tau, W, \sigma) = \frac{1}{2\sqrt{2\pi}} \cdot \frac{1}{\sigma} \cdot \left(e^{-\left(\frac{\left(\tau - \frac{W}{2}\right)^2}{2\sigma^2}\right)} + e^{-\left(\frac{\left(\tau + \frac{W}{2}\right)^2}{2\sigma^2}\right)} \right) \quad \text{(48B-6)}$$

48B.1.4 Effects of jitter high-pass filtering and CJPAT on deterministic jitter

It is understood that CDRs track low-frequency jitter, and that including this effect in the specifications could ease requirements on clock oscillators (lower cost designs tend to exhibit low-frequency RJ), serializer (SERDES, same advantage) designs and switching power supplies, layouts, bypassing, etc. All jitter specifications include the effects of a high-pass filter (to suppress the significance of low-frequency jitter) to emulate CDR tracking.

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It is also realized that, due to frequency content, long complex patterns cause phenomena that are not observed with short patterns—data dependent jitter (DDJ, a form of DJ) can have extreme ranges of frequency content from well below to well above the CDR corner frequencies. Effects are usually seen in both transmitters and receivers. Jitter test patterns are specified in Annex 48A.

48B.2 Jitter tolerance test methodologies

An important measurement in determining link integrity is the characterization of a receiver's (i.e., CDR's) ability to tolerate jittered inputs yet recover error-free data. This is accomplished by inputting a well-controlled, jittered signal to a CDR while measuring the BER at the output of the CDR. As the source signal is modified in amplitude and spectral content, the change in BER is measured. This subclause describes some useful test methodologies for testing a receiver's jitter tolerance.

48B.2.1 Calibration of a signal source using the BERT scan technique

The jitter model described in 48B.1 can be used to calibrate the signal source for tolerance measurements as well as to provide a method for extrapolating lower BER. In this approach, curve fitting of the dual dirac model onto bathtub curves derived from BERT Scans give the jitter content.

Figure 48B–3 shows an example of how to generate controlled amounts of jitter in a signal to be used for tolerance measurement.[21] Three sources of jitter are provided: Deterministic (DDJ and sinusoidal (SJ)) and Gaussian (RJ). Each of these is added to the serial signal generated by a BERT Pattern Generator. A sine-wave generator modulates the clock to the Pattern Generator to provide Sinusoidal jitter modulation from 10 Hz to 20 MHz. A filter or cable adds deterministic jitter. A white noise source[22] with a bandwidth greater than 500 MHz[23] is added to the signal to provide random jitter.

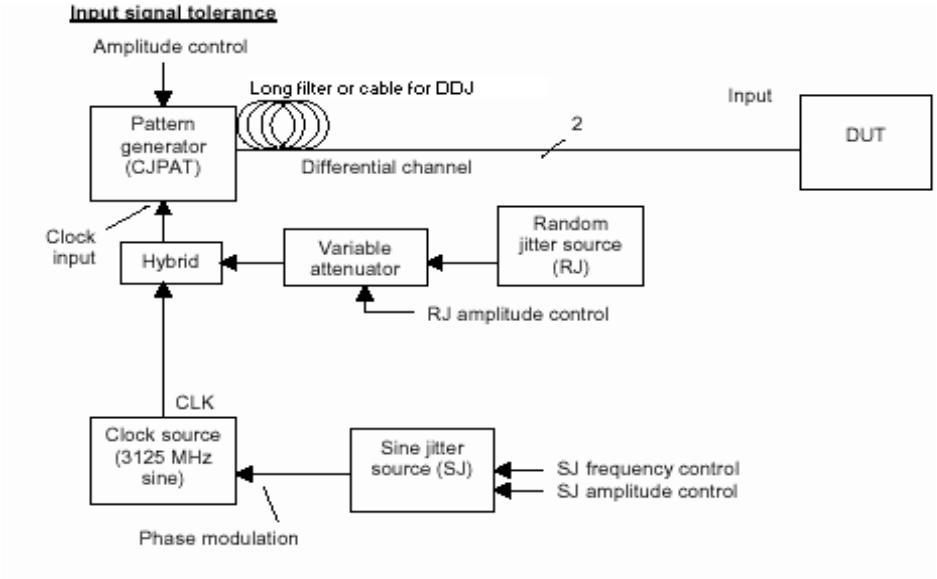


Figure 48B–3—BERT Jitter Tolerance Source

[21]Beware of instrument noise floors and data dependencies, as these may lead to test signals with less stress than intended.

[22]RJ must be Gaussian and not clipped out to >BER being tested (spec is 1E-12). Simply measuring the rms value does not guarantee that the tails exist and that the Rx will be sufficiently stressed as specified.

[23]The spectrum of the portion of RJ that is calibrated must be from greater than 20MHz. The sketch as shown assumes the pattern generator passes clock input jitter through to the data with >>20 MHz BW. This may not be the case. The RJ spectrum need not be white above 20 MHz, but a wider spectrum is preferred.

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Amplitude calibration is not possible on a scope due to the low probability of the pk-pk RJ effects. For better visibility for amplitude calibration, the RJ portion may be temporarily replaced with an equivalent amount of pk-pk SJ to bring TJ up to the same specified output jitter level, allowing the desired amplitude value to be met.[24,25]

If the clock data recovery circuit of the system under test has a corner frequency above the maximum sine wave generator frequency, be sure to increase the amount of the applied deterministic jitter by the amount of the specified high-frequency value sinusoidal jitter.

When calibrating the jitter tolerance test setup, the effects of high pass filtering in the time/jitter domain must be understood and included per the specifications. Per 48B1.4, high pass filtering can have profound effects on pattern dependent jitter (it will increase measured DJ with patterns such as CJPAT) and also track out jitter below the specified corner frequency. [26]

After complete, calibration must be verified using the methods described in 48B.3 and iterated as needed until the required specifications are met.

It should be noted that the XAUI is a differential input and calibration of the test signal must be performed using the differential signal. If test equipment only provides single-ended possibilities, care should be taken to calibrate and test with a balun to convert differential signals to single-ended signals. Single-ended signals should not be directly used, due to the possibility of asymmetric characteristics.

48B.3 Jitter output test methodologies

Three viable methodologies for measuring jitter output are described in this subclause. They are as follows:

a) Time domain measurement using an oscilloscope to characterize the data eye.
b) Time domain measurement using BERT scan by moving of the data sampling point within the data eye.
c) Time interval analysis based on accurate measurement of the time interval between threshold crossings of the transmitter waveform;

48B.3.1 Time domain measurement—Scope and BERT scan

It is easy to grasp that if the eye is larger than the eye mask, it must be ok. This is not necessarily true. Given the probabilistic nature of random jitter, it is necessary either to test for an extended amount of time to reach a high confidence level for achieving 1×10^{-12} BER or to perform some kind of statistical extrapolation.

48B.3.1.1 Jitter high pass filtering (using Golden PLL)

Due to the issues mentioned in 48B.1.4, when testing either at the component level or the system level, the test clock should be derived from the data with a given high pass filter function of the jitter using, for example, a golden PLL.

Given a typical test setup, the serial bit pattern is transmitted to the input of a BERT and a golden PLL. The golden PLL extracts a reference clock to trigger the sampling scope or clock the BERT.

---

[24]Amplitude calibration should be done before addition of SJ, as SJ is designed to add margin into the design. NOTE—This footnote is not referring to the suggestion of temporarily substituting SJ and RJ during amplitude calibration, but to the SJ that is required as part of the specifications.

[25]It may be required to add amplification to achieve the required test signal amplitude.

[26]Beware of autocorrelation effects.

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48B.3.1.2 Time domain scope measurement

Time domain measurement uses the high-speed sampling scopes to view the jitter output data eye. Most high-speed sampling scopes today provide features to collect and present data on the output jitter. Some oscilloscopes provide a feature to compare the measured data to an "eye mask." An eye mask is a specification for allowed eye opening. The advantage of an eye mask is that it tests for amplitude as well as timing compliance. The general physical media transmitter pulse shape characteristics are specified in the form of a mask of the transmitter eye diagram at any of the compliance measurement points. These characteristics include rise time, fall time, pulse overshoot, pulse undershoot, and ringing, all of which prevent excessive degradation of the receiver sensitivity. For the purpose of an assessment of the transmit signal, it is important to not only consider the eye opening, but also the overshoot and undershoot limitations. The parameters specifying the mask of the transmitter diagram (eye mask) can be found in the clause of the applicable physical layer specification whether it be copper or fiber physical media. The eye mask, through its use of a specified time range in which the transmit signal can change state from the logic low to logic high levels, is also specifying a measure of the allowed jitter.

It is strongly advised not to use the eye mask to verify that total jitter is within specification because of the nature of the test. The eye mask test is generally a short test, and thus the eye diagram is not captured for a sufficient time to capture the full extent of the random jitter's peak-to-peak value. It is necessary to capture the eye pattern for a sufficient period to insure the full extent of the deterministic jitter is captured by the test instrument. Since the peak-to-peak of the random jitter for a BER of 1×10^{-12} is 14 times the sigma, it is not possible to capture the full extent of random jitter's peak-to-peak value due to the low sampling rate.

48B.3.1.3 BERT Scan

As implied by the jitter model in 48B.1, a BERT scan approach can provide random and deterministic jitter components and provides a mechanism to extrapolate to lower BER (less than 1×10^{-12}) without impossibly long test times due to the inherent high sampling rate.

48B.3.1.3.1 Approximate curve-fitting for BERT scan

48B.3.1.3 describes a technique for using a BERT scan to determine eye opening and jitter. For highest accuracy, the bathtub curve should be measured over a high number points at low BER and curve-fitted with a least-squares method to estimate equivalent DJ, RJ, and TJ values. However, a simple and fast method for estimating these values may be applied using only two measurement points.

The following steps describe a process for estimating equivalent RJ, DJ, and TJ values from a two point BERT scan measurement:

a) Measure the eye opening at 2 different BER, $BER_0 \ @ \tau_0$ and $BER_1 \ @ \tau_1$ (e.g., 10^{-9} and 10^{-5}).

b) For each BER_n, determine the associated Q_n from the inverse normal cumulative probability distribution, adjusted for transition density, e.g., $Q = 3.94$ for BER = 10^{-5}, and $Q = 5.77$ for BER = 10^{-9}, where transition density is assumed to be 0.5.

c) Calculate the individual jitter components using the equations for Random Jitter and Deterministic Jitter, and then calculate the total jitter for the given BER = 10^{-12}, using the following three equations:

Random Jitter—

$$RJ_{RMS} = 0.5\left|\frac{t_1 - t_0}{Q_1 - Q_0}\right| \quad \text{(48B-7)}$$

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Deterministic Jitter—

$$DJ = UI - t_0 - (2Q_0 RJ_{RMS}) \quad (48B\text{-}8)$$

Total Jitter—

$$TJ = DJ + 13.8 \cdot RJ_{RMS} \quad (48B\text{-}9)$$

The minimum value for measured BER is constrained by test time (10 errors are suggested as an absolute minimum to get reasonable statistical confidence); the maximum value is constrained by potential departure of actual results from the assumed curve fit shape (BER = 10^{-5} should be the maximum value used).

48B.3.2 Time Interval Analysis

Time Interval Analysis (TIA) uses many accurate, single-shot, edge-to-edge time measurements. The statistics of these measurements can be used to perform jitter calculations. True random jitter (RJ) and true deterministic jitter (DJ) can be measured using this technique on repeated patterns as well as random data streams. From the true RJ and DJ measurements, an error probability density function, or bathtub curve can be generated. Using the bathtub curve, effective DJ and effective RJ can be calculated. There are two measurement methods defined for executing this test:

a) TIA with Golden PLL
b) TIA armed on pattern trigger

Each method uses the basic TIA methodology, but with different schemes for acquiring the data. In the first method, the TIA is used with a Golden PLL, as described in 48B3.1.1, and time measurements are made from the recovered reference clock to the data transitions. The low-frequency content that would be tracked by the receiver is presented on the reference clock, and thus eliminated from the jitter data before being presented to the TIA. The second method is used to acquire data when a Golden PLL is not available, or, when jitter on just the data is desired. This method requires a pattern trigger to synchronize the jitter measurements relative to a specific location in the pattern. The TIA can extract the pattern trigger from the data based on a unique bit sequence or pattern length.

48B.3.2.1 TIA with Golden PLL

In this option, a Golden PLL is required to provide a reference clock derived from the data stream to trigger the TIA. This scheme effectively removes low-frequency content from the measured data in a manner similar to that done in a receiver. The configuration used for this option is shown in Figure 48B–4 (note that only a single channel is shown). The Golden PLL in Figure 48B–4 is shown with a differential input; other approaches are possible, but it is important that the balance of the data signals is not disturbed and that both phases are included in clock recovery. A Golden PLL is used for each data signal so as to ensure proper CDR modeling on each data signal. Each Golden PLL is intended to track low-frequency jitter content occurring on the data signal applied to the input stage of that PLL. It cannot be assumed that the clock extracted from one data signal can be used for the other signals since the low-frequency jitter content may be different. Some TIA models have this algorithm integrated internally in the instrument, and some TIA models have integrated Golden PLL or high-pass filtering algorithms.

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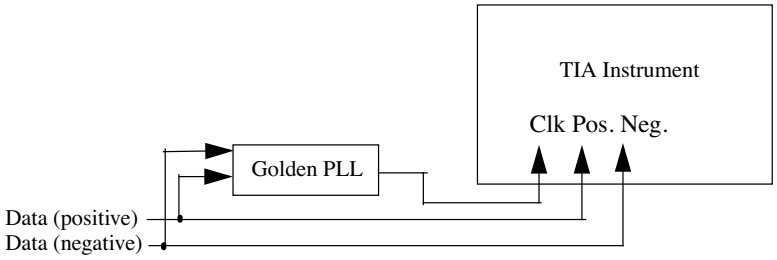


Figure 48B–4—TIA with Golden PLL configured for jitter measurement

48B.3.2.1.1 Test method

The TIA is capable of measuring the time from the data transitions to the reference clock as extracted with the Golden PLL. This results in a clock to data histogram that describes the jitter occurring on the data transitions relative to the reference clock (as is the case with a bit clock triggered BERT measurement). RJ can be estimated by fitting a Gaussian curve to the tail region of the histogram. DJ can be estimated by measuring the separation of the means of the fitted Gaussian curves. Some sampling TIA instruments have built in algorithms specifically designed for this process, and can automatically estimate RJ, DJ, and TJ in this configuration. Figure 48B–5 shows a typical clock to data histogram for a communication signal. Note the highlighted curves that represent the fitted Gaussian curves. Also note that the rising edges are treated separately from the falling edges so as to accurately group the jitter contributors. This is critical in cases where the cross point of the data signal is not at the measured voltage. In Figure 48B–5, the rising edge histogram is shifted to the right of the falling edge histogram, indicating that the cross point was below the test voltage. The outer most histogram on a given side is used for the RJ and DJ calculations for that side of the histogram. Each side is treated independently.

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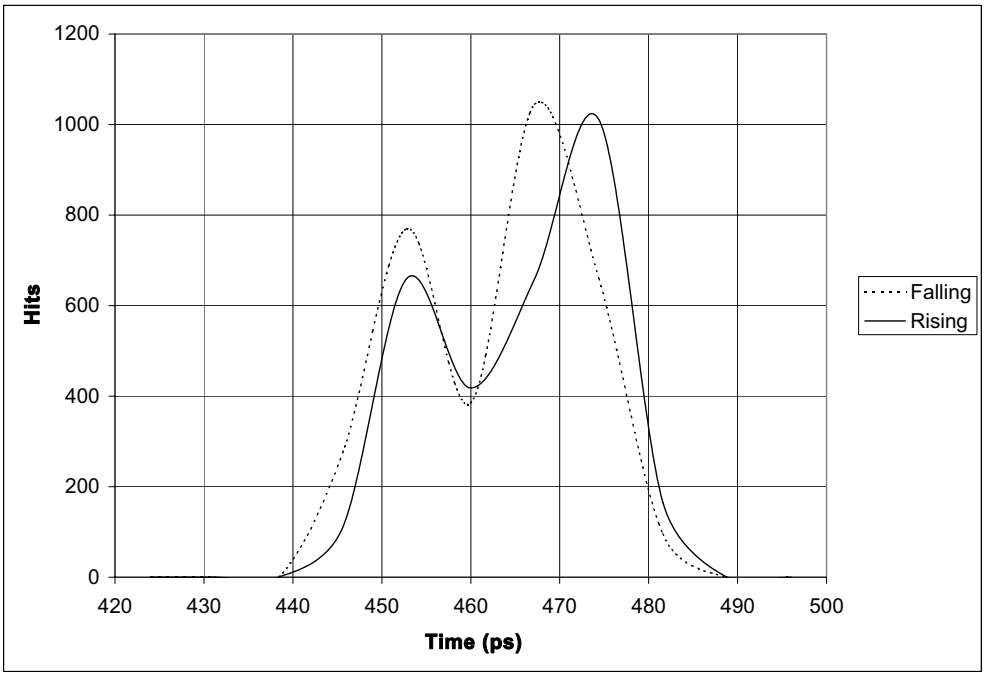


Figure 48B–5—Typical clock to data histogram with fitted Gaussian curves

Jitter values such as DJ, RJ, and TJ can also be displayed on the plot corresponding to 10E-12 BER as shown in Figure 48B–5. Effective Jitter is calculated from the bathtub curve using the same calculations used by the BERT scan method described in 48B3.1.3.1. To quantify the quality of the measurement, a goodness of fit calculation can be made which compares the quality of the fit of the Gaussian to the actual histogram. Acceptable goodness-of-fit values (χ) for probability confidence level (approximately 10E-4) should be in the range of $0.8 < \chi < 1.2$. The measured DJ and TJ values using this method can be compared against the maximum jitter as specified.

48B.3.2.2 TIA with pattern trigger

The basic setup for this option is shown in Figure 48B–6 (note that only one channel is shown). The pattern trigger can be generated internally to the TIA based on the identification of a unique bit sequence within the data stream or pattern length of the repeated pattern. No measurements are made from the pattern trigger. All measurements are made within the data signal thereby eliminating any error attributed to the bit clock. The high pass filter characteristic of the Golden PLL is applied using a DSP algorithm thereby eliminating the need for external hardware. Some TIA instruments have this algorithm fully integrated.

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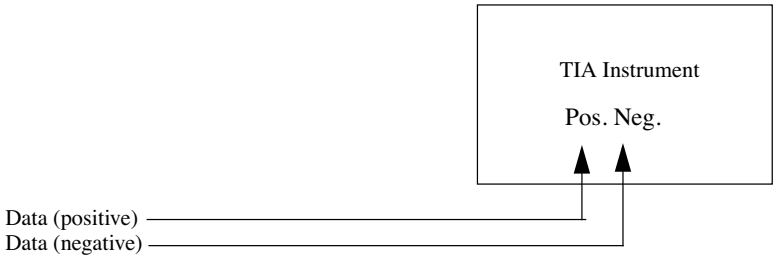


Figure 48B–6—TIA with pattern trigger configured for jitter measurement

48B.3.2.2.1 Test Method

All time measurement are made from the same reference edge within the data pattern. This edge is identified by the pattern trigger. Thousands of measurements are made of each transition within the data pattern relative to the reference edge. Histograms for each transition are captured from this data. An FFT of the autocorrelation algorithm of the variance information from these histograms is used to extract SJ. Using the tail fit algorithm described in 48B3.2.1.2, RJ is measured from each of these histograms and the results plotted in the FFT display. The RJ, bounded by the high pass filter function is calculated from the FFT of the autocorrelation function. Data dependent jitter is measured from the histograms of each transition based on the displacement of each histogram mean relative to integer multiples of the measured bit period. TJ is calculated and the bathtub curve generated based on the convolution of the RJ PDF, DDJ PDF, and the SJ PDF. This method directly measures the DJ PDF and thereby does not need to assume that the DJ PDF is a dual Dirac function. Effective DJ and Effective RJ is calculated from the bathtub curve using the same formulas used for the BERT scan method, thereby ensuring correlation. Some TIA instruments have this algorithm fully integrated, simplifying the measurement methodology.

48B.3.2.3 Approximate curve fitting for TIA bathtub curve

Since the TIA is capable of measuring true DJ and its probability density function (PDF), the TIA can accurately display total jitter (TJ) as a function of BER in the form of an error probability density function, or bathtub curve. From the Error PDF, the effective DJ can be estimated using the same curve fit technique described in 48B3.1.3.1.

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Annex 50A

(informative)

Thresholds for Severely Errored Second calculations

This annex provides tables of threshold values that may be used to determine the generation of Section, Line and Path Severely Errored Second (SES) events for various error rates. An SES event is deemed to have occurred when the number of bit errors, detected via the corresponding Bit Interleaved Parity (BIP) check, exceeds some predefined threshold value when accumulated over a 1 s interval; reporting of an SES event indicates that the actual bit error rate on the medium has increased to a point where Station Management must be notified. These threshold values are referred to as *x* in the Layer Management definitions in Clause 30. This annex also defines the terms "Path Block Error" and "Far End Path Block Error."

The values in these tables are derived according to the algorithms given in Annex C of ANSI T1.231-1997.

50A.1 Section SES threshold

The Section SES threshold is referenced as *x* in 30.8.1.1.3.

Table 50A–1 gives the values to be used for the Section SES threshold in order to report Section SES events at various limiting bit error rates. A BER of 10^{-6} corresponds to the default Section SES threshold of 8554 in 30.8.1.1.3.

Table 50A–1—Section SES

BER	Threshold, *x*
10^{-6}	8554
10^{-7}	980
10^{-8}	99
10^{-9}	10
10^{-10}	1

50A.2 Line SES threshold

The Line SES threshold is referenced as *x* in 30.8.1.1.11.

Table 50A–2 gives the values to be used for the Line SES threshold in order to report Line SES events at various limiting bit error rates. A BER of 10^{-6} corresponds to the default Line SES threshold of 9835 in 30.8.1.1.11.

50A.3 Path SES threshold

The Path SES threshold is referenced as *x* in 30.8.1.1.19.

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Table 50A–2—Line SES

BER	Threshold, *x*
10^{-6}	9835
10^{-7}	984
10^{-8}	98
10^{-9}	10
10^{-10}	1

Table 50A–3 gives the values to be used for the Path SES threshold in order to report Path SES events at various limiting bit error rates. The default Path SES threshold of 2400 in 30.8.1.1.19 corresponds to a situation where 30% of all the SPEs being received have parity errors detected via the Path BIP checks.

Table 50A–3—Path SES

Fraction of SPEs with parity errors	Threshold, *x*
30%	2400
25%	2000
20%	1600
15%	1200
10%	800

50A.4 Definition of Path Block Error

A Path Block Error (see Section 8.1.1.1.2 of ANSI T1.231-1997) is declared when one or more of the 8 BIP-8 parity bits that are computed over the received Synchronous Payload Envelope, and compared to the B3 octet of the Path Overhead, are found to be in error. At most one Path Block Error can be declared per WIS frame (i.e., a maximum rate of 8000 counts per second), regardless of the actual number of parity errors detected using a particular B3 octet.

50A.5 Definition of Far End Path Block Error

A Far End Path Block Error is declared when the G1 octet extracted from a received WIS frame indicates that the far end WIS has detected one or more BIP-8 parity errors in the SPE of a previously transmitted WIS frame. The far end WIS reports these parity errors via the REI-P field of the G1 octet. At most one Far End Path Block Error can be declared per received WIS frame (i.e., a maximum rate of 8000 counts per second), regardless of the actual number of parity errors reported in the REI-P field of a particular G1 octet.

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