**UNITED STATES DISTRICT COURT**
**EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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|---|---|
| UNIVERSAL CONNECTIVITY TECHNOLOGIES INC.,<br><br>Plaintiff,<br><br>v.<br><br>LENOVO GROUP LIMITED,<br><br>Defendant. | Case No. 2:23-cv-00449-JRG |

**DEFENDANT'S INVALIDITY AND ELIGIBILITY CONTENTIONS**

Pursuant to the Court's Patent Rules, Standing Order Regarding Subject Matter Eligibility Contentions, and Docket Control Order (Dkt. No. 27), Defendant Lenovo Group Limited respectfully submits these invalidity and eligibility contentions with respect to the asserted claims of U.S. Patent Nos. 7,154,905 ("the '905 Patent"), 7,187,307 ("the '307 Patent"), 7,746,798 ("the '798 Patent"), 9,232,265 ("the '265 Patent"), 8,680,712 ("the '712 Patent"), 7,856,520 ("the '520 Patent"), 7,921,231 ("the '231 Patent"), and 9,852,103 ("the '103 Patent") (collectively, the "Asserted Patents") identified by Plaintiff Universal Connectivity Technologies Inc., ("UCT" or "Plaintiff") in its May 15, 2024 Patent Rule 3-1 Disclosures and July 3, 2024 Notice Regarding Claim Reduction (together, "Infringement Contentions").

The currently Asserted Claims, as reflected in Plaintiff's Infringement Contentions, are:

- '905 Patent: Claims 1, 8, 12, 15, 16, 17, 21, 22, 23, 26
- '307 Patent: Claims 1, 7, 23, 31, 53, 68, 71, 72, 74, 75
- '798 Patent: Claims 11, 19, 20, 21, 22, 23, 24, 25, 26, 28

- ’265 Patent: Claims 1, 8, 11, 14, 16
- ’712 Patent: Claims 1, 2, 5, 7, 9
- ’520 Patent: Claims 1, 4, 8, 9, 12, 13, 15, 18, 19, 25
- ’231 Patent: Claims 1, 2, 10, 11, 12, 13, 14, 16, 17, 18
- ’103 Patent: Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, 22

As detailed further below, the asserted claims of each Asserted Patent are anticipated by and/or obvious in view of one more of the prior art references being produced concurrently pursuant to 35 U.S.C. § 102 and/or § 103, are directed to ineligible subject matter under 35 U.S.C. § 101, and are otherwise invalid under 35 U.S.C. § 112.

## I. PRELIMINARY STATEMENT

These invalidity contentions and eligibility contentions are based on Defendant’s current knowledge, understanding, and belief of the Asserted Patents and prior art, of Plaintiff’s infringement theories (inasmuch as they can be inferred from its Infringement Contentions), and of the facts and other information available as of the date of these contentions. Defendant’s investigation, discovery, and analysis of information related to this action is ongoing. Additional discovery, elucidation of Plaintiff’s impermissibly vague infringement contentions, Plaintiff’s expert report(s) regarding infringement, and/or orders of the Court may require Defendant to amend or supplement these invalidity contentions and eligibility contentions, and Defendant expressly reserves the right to do so, subject to the Court’s procedures, as the case proceeds. These contentions represent Defendant’s good-faith effort to provide a comprehensive identification of prior art relevant to this case, but Defendant reserves the right to modify or supplement its prior art list and invalidity contentions and eligibility contentions at a later time with, or based upon, pertinent information that may be subsequently discovered.



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In addition to the prior art that charted in the attached exhibits, additional background references are discussed herein and/or included in the document production accompanying these Invalidity and Eligibility Contentions. Defendant reserves the right to rely on these background references for any purpose including, for example, to demonstrate the knowledge of a POSITA at the relevant time.

To the extent UCT believes anything in these contentions (including the attached claim chart exhibits and accompanying document production) are insufficient, Defendant invites UCT to bring such issues to its attention as soon as reasonably possible.

**A. No Waiver**

Nothing in these contentions is intended, nor should be construed, as a waiver of any non-infringement position or argument under 35 U.S.C. §§ 101 or 112. To the contrary, as set forth herein, Defendant contends that all Asserted Claims are invalid pursuant to 35 U.S.C. §§ 101 and/or 112. Defendant's statements herein (including the accompanying claim charts) reflect Defendant's present understanding of the purported scope of the claims as alleged by Plaintiff in its Infringement Contentions (as best those contentions can be understood in light of their present deficiencies).

The patent claims have yet to be construed. As a result, Defendant has based these contentions upon its knowledge and understanding of the potential scope of the Asserted Claims at this time, and, in part, upon the apparent interpretations of the Asserted Claims advanced by Plaintiff in its Infringement Contentions. Defendant may disagree with Plaintiff's interpretation of the meaning of many terms and phrases in the Asserted Claims. Defendant has provided these contentions based in part on its present understanding of Plaintiff's apparent constructions and interpretations of the Asserted Claims. These contentions do not represent Defendant's agreement or view as to the proper interpretation of any claim term contained therein. Any similarity between

any apparent claim interpretation in any of Defendant's charts of prior art references and Plaintiff's contentions is not an admission or agreement with Plaintiff about the meaning of any claim term, but rather a reflection of the fact that the subject matter Plaintiff believes is claimed is present in the prior art, or that the claims are otherwise invalid. These contentions are made in the alternative, and should not be interpreted to rely upon, or in any way affect, the non-infringement arguments Defendant may assert in this case. Defendant reserves the right to amend, supplement, or materially modify these contentions as the case proceeds, including to identify additional prior art and/or additional bases for invalidity under 35 U.S.C. §§ 101 and/or 112. Defendant also reserves the right to amend, supplement, or materially modify its contentions based on any infringement and/or additional claim construction positions that Plaintiff may take in this case.

Defendant also reserves the right to amend, supplement, or materially modify its contentions in response to any claim construction or interpretation positions that Plaintiff may take or based on any claim construction the Court may further adopt in this case. Defendant also reserves the right to assert that a claim is indefinite, not enabled, or fails to meet the written description requirement of 35 U.S.C. § 112 based on any claim construction or interpretation position Plaintiff may take in this case or based on any claim construction the Court may further adopt in this case.

**B. No Admission**

Nothing disclosed herein is an admission or acknowledgement that any product accused of infringement by Plaintiff in its Infringement Contentions (the "Accused Products"), or any of Defendant's other products or services, infringes any of the Asserted Claims.

Defendant further notes that Plaintiff appears to rely upon overly broad interpretations of the Asserted Claims. At the same time, Plaintiff's Infringement Contentions are in most places too general and vague to discern Plaintiff's infringement theories and how exactly Plaintiff



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contends each Accused Product meets or practices each element of the Asserted Claims. As a result, Defendant has been prejudiced in its ability to prepare these contentions. In addition, Plaintiff's Infringement Contentions, in many cases, continue to fail to put Defendant on notice of Plaintiff's interpretation of the Asserted Claims, further prejudicing Defendant's ability to identify relevant prior art.

Patent Rule 3-1(d) required Plaintiff to identify "each element of each asserted claim" that is alleged to be present under the doctrine of equivalents. In its Contentions, Plaintiff identified no specific claim elements as allegedly being present under the doctrine of equivalents. In preparing these invalidity and eligibility contentions, Defendant has relied on Plaintiff's representation that it has no doctrine of equivalents theories for any specific claim element, and any attempt by Plaintiff to present an untimely doctrine of equivalents argument or allegation would be severely prejudicial to Defendant. To the extent Plaintiff attempts to or is later permitted by the Court to amend its contentions to pursue any currently undisclosed doctrine of equivalents theories for additional claim elements, Defendant expressly reserves the right to supplement or amend these contentions to account for such amendments.

To the extent that any of the prior art references discloses the same functionality or feature of any of the Accused Products, Defendant reserves the right to argue that said feature or functionality does not practice any element of any of the Asserted Claims, and to argue, in the alternative, that if said feature or functionality is found to practice any element of any of the Asserted Claims, then the prior art reference demonstrates that the element is not novel, is obvious, and/or is otherwise not patentable.

Attached hereto are representative claim charts that identify examples of where the elements of the Asserted Claims may be found in the prior art and further identifying why those



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claims are not novel or non-obvious. Defendant's claim charts cite particular teachings and disclosures of the prior art as applied to features of the Asserted Claims. Providing citations to portions of the prior art references should not be construed to mean that other portions of the prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art may additionally disclose, either expressly or inherently, information relevant to the validity of one or more elements of the Asserted Claims. And, persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, Defendant reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony to establish the state of the art and to aid in understanding and interpreting the cited portions, as providing context thereto, showing reasons to combine references and as additional evidence that the prior art discloses a claim limitation. Defendant further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish bases for combinations of certain cited references that render the asserted claims obvious. Defendant also reserves the right to rely on uncited portions of the prior art references that describe substantially the same functionality or features that are described in cited portions. Further, for any combination, Defendant reserves the right to rely on information generally known to those skilled in the art and/or common sense.

Where Defendant cites a particular drawing or figure in the accompanying charts, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not itself expressly cited). Similarly, where Defendant cites particular text concerning a drawing or figure in the accompanying charts, the citation encompasses that drawing or figure (even if the associated drawing or figure is not expressly cited).



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The references cited in the attached claim charts may disclose the limitations of the Asserted Claims expressly and/or inherently. Defendant may rely on inherency to demonstrate the invalidity of the Asserted Claims. Moreover, certain prior art references and solutions may inherently anticipate certain features of the asserted claims as construed by Plaintiff. Defendant may rely on cited or uncited portions of the prior art, other documents, and expert testimony to establish the inherency of certain features of the prior art to invalidate the Asserted Claims. Defendant also may rely on any reference identified in these contentions or any other reference to prove that the references are enabling, to provide a reason to combine the references, as an indication of the state of the art, or to explain the meaning of a term used in any reference.

The suggested obviousness combinations may be presented in conjunction with or in the alternative to Defendant's contentions regarding anticipation. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right. Further, to the extent that Plaintiff contends that any of the references identified does not constitute prior art under 35 U.S.C. § 102, Defendant reserves the right to rely upon other prior art references in the same patent family with substantially identical disclosures as evidence of invalidity based on the same theories as those disclosed below.

Throughout the charts, Defendant provides exemplary citations indicating where the cited references disclose subject matter recited in the preambles of the claims, without regard to whether the preambles are limitations of the claims. Defendant does not take any position at this time regarding whether or not the preambles of the Asserted Claims are limitations, and will address this topic, if necessary, during the scheduled claim construction process.

With regard to the prior art that Defendant identifies as rendering the Asserted Claims obvious, non-limiting examples of the reasons why the prior art renders the Asserted Claims



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obvious, including exemplary identification of combinations of prior art showing obviousness, are provided below. Generally, for all prior art combinations addressed herein, a reason or motivation to combine the prior art includes that each prior art reference is relevant to data communications and/or power distribution between devices, and one of ordinary skill in the art tasked with implementing such a system would have been motivated to investigate the various existing systems, patents, and other publications, including those identified herein, to address his or her particular needs. The combinations and modifications of the prior art to invalidate the Asserted Claims would have arisen from ordinary innovation, ordinary skill, or common sense and/or would have been obvious to try or otherwise predictable in the field of data communications and/or power distribution between devices.

A person having ordinary skill in the art would have had a reason to combine the prior art based on the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons having ordinary skill in the art. For example, each of the prior art references is relevant to data communications and/or power distribution between devices, including addressing problems such as symbol alignment, device and signal negotiation, and power provision. In addressing these problems, one of ordinary skill in the art would have been motivated to combine the teachings of research in the field.

Additionally, some prior art references cite or discuss other prior art references, illustrating the close technical relationship among the prior art. To the extent that any prior art reference refers to or discusses another prior art reference, either expressly or inherently, it would have been obvious to combine those references for at least that reason.

As shown in the accompanying claim charts, numerous books and research papers show that methods were being used to streamline packetized data transmission and power distribution

across device-to-device connections. Design incentives and other market forces would have prompted combinations and modifications of the prior art. Design needs and market pressures provide ample reason to combine prior art elements in the manner combined. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007). Defendant reserves the right to supplement these discloses if such evidence of design needs and/or market pressures become apparent through discovery in this case.

Moreover, the Asserted Claims are also obvious because they merely arrange old elements, with each performing the same function that had been known, to perform and yield no more than what one having ordinary skill in the art would expect from such an arrangement.

Because there were a finite number of predictable solutions in the art of packetized data transmission and power distribution across device-to-device connections with regard to any claimed feature, it would have been obvious to a person of ordinary skill in the art to pursue the known options. A person skilled in this art would have been familiar with all the claim elements that the patentees used to distinguish the prior art during prosecution. The identified prior art references merely use those familiar elements for their primary or well-known purposes and in a manner well within the ordinary level of skill in the art. Accordingly, common sense and the knowledge of one having ordinary skill in the art render the Asserted Claims invalid.

**C. Reservation of Rights**

Prior art not currently included in this disclosure may become relevant. Defendant is currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Defendant or contend that prior art identified by Defendant does not qualify as prior art. Defendant reserves the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device or method obvious or show that the allegedly missing limitation would have been known



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or readily apparent to one of ordinary skill in the art at the time of the invention in light of the disclosure of the prior art at issue or other prior art. Defendant further reserves the right to rely on any of the references produced concurrently with these contentions in order to demonstrate the state of art at the alleged times of invention and as evidence of the knowledge of one of ordinary skill in the art[1] in support of any motivations to modify or combine the charted prior art references with other references or knowledge.

To the extent that Defendant charted a published patent application that later issued as a patent that includes substantially the same disclosure, Defendant contends that the issued patent discloses the claims for at least the same reasons explained in connection with the published application and Defendant reserves its rights to rely on the issued patent to establish invalidity. Similarly, to the extent that Defendant charted an issued patent the application for which was previously published (and which contains substantially the same disclosure), Defendant contends that the published application discloses the claims for at least the same reasons explained in connection with the issued patent and Defendant reserves the right to rely on the published application to establish invalidity (including to establish an earlier prior art date).

Consistent with the Patent Rules and Docket Control Order (Dkt. No. 27), and in view of the following, Defendant reserves the right to supplement or otherwise amend these Invalidity and Eligibility Contentions. This is particularly true for all claims for which Plaintiff has not provided adequate infringement contentions.

Plaintiff may also be aware of additional prior art that is not known to Defendant. To the extent Plaintiff produces additional prior art responsive to Defendant's discovery requests after

[1] For purposes of these Invalidity and Eligibility Contentions, the term "general knowledge" includes the common knowledge and common sense of a POSITA as well as the general knowledge of POSITAs in the field.



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these contentions are served, Defendant may supplement its Invalidity and Eligibility Contentions with prior art contained in such production once it has had a fair opportunity to review, analyze, and chart such prior art. Defendant reserves the right to amend its Invalidity and Eligibility Contentions with any additional potential prior art known by Plaintiff but not yet disclosed to Defendant.

Defendant provides these Invalidity and Eligibility Contentions only for the claims that are asserted by Plaintiff, but reserves the right to seek invalidation of all claims in each of the Asserted Patents.

In addition to the prior art that is set forth in the charts, additional prior art references are being produced concurrently with these contentions. This additional art may be relevant to the validity of the Asserted Claims depending on the positions taken by Plaintiff, and in any event may be referenced to show the state and evolution of technology in these fields. Accordingly, for the foregoing reasons, Defendant reserves the right to supplement these Invalidity and Eligibility Contentions with specific claim charts and obviousness combinations with the additional references based on the allegations and contentions asserted by Plaintiff as these allegations and corresponding constructions of the claims become clear.

**D. Ongoing Investigation**

Defendant's investigation is ongoing, and Defendant expressly reserves the right to amend its disclosures and document production to account for evidence uncovered as its investigation continues. Such amendments include identifying and relying on additional references that may result from Defendant's further search and analysis. Defendant reserves the right to supplement these contentions in light of any additional prior art of which Plaintiff is aware and has not disclosed to Defendant in discovery, or that might be subsequently disclosed by Plaintiff in response to Defendant's discovery requests. An example of such prior art may include products

sold and offered for sale by Silicon Image and/or Lattice Semiconductor. Such products may have been offered for sale or publicly shown in a manner that renders them prior art under 35 U.S.C. §§ 102 and 103. Defendant reserves the right to supplement these contentions to rely on those and other products from Plaintiff. Defendant's investigation into prior art systems and products is ongoing, and Defendant reserves the right to amend these contentions to reflect the identification of and information about such systems and products learned through discovery.

Defendant anticipates issuing subpoenas to third parties believed to have knowledge, documentation and/or corroborating evidence concerning some of the prior art listed herein and/or additional prior art. These third parties include, but are not limited to, the authors, employers of authors, inventors, assignees, or former or current employees of assignees or previous assignees, of the references identified in these Invalidity and Eligibility Contentions. For example, Defendant anticipates issuing subpoenas to potential prior artists including but not limited to individuals and entities responsible for the development of prior art systems identified in these Invalidity and Eligibility Contentions. Defendant reserves the right to supplement these contentions in light of any newly discovered information produced by these or other companies from which Defendant may seek discovery.

**E. Incorporation by Reference**

Defendant hereby incorporates by reference all arguments made in all IPR petitions filed by any party or third party (and all Institution Decisions instituting IPR relating to such petitions) challenging any Asserted Claim, including any IPR petition or decision instituting IPR that is filed after the date of these contentions. Defendant further incorporates by reference the file history of each Asserted Patent and the prior art cited therein.



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## II. PRIORITY DATE OF THE ASSERTED PATENT CLAIMS

Plaintiff asserted the following priority dates for the Asserted Claims in its Infringement Contentions:

| Asserted Patent | "Priority Date" |
|---|---|
| '905 Patent | "at least a priority date of November 22, 2000" |
| '307 Patent | "at least a priority date of June 12, 2003" |
| '798 Patent | "at least a priority date of November 22, 2000" |
| '265 Patent | "at least a priority date of March 31, 2011" |
| '712 Patent | "at least a priority date of December 11, 2008" |
| '520 Patent | "at least a priority date of January 4, 2008" |
| '231 Patent | "at least a priority date of January 4, 2008" |
| '103 Patent | "at least a priority date of April 14, 2014" |

It is Plaintiff's burden to show entitlement to its asserted priority dates, and Defendant asserts that Plaintiff has failed to meet that burden, at least because it discloses ambiguous "priority dates" qualified with the phrase "at least as early as." To the extent Plaintiff attempts to rely on a different date from the specifically enumerated "Priority Dates" listed above (i.e., under the "at least" language), Defendant reserves the right to supplement these contentions. Moreover, because discovery has not yet been completed, Defendant has relied on Plaintiff's assertions for the purposes of identifying relevant prior art in these Invalidity and Eligibility Contentions, but Defendant does not concede that those priority dates are accurate. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions should discovery reveal that Plaintiff is not entitled to the asserted priority date. In addition, Defendant also reserves the right to supplement these contentions should Plaintiff subsequently attempt to amend its infringement

contentions in any way, or to otherwise modify its infringement allegations or seek to establish an earlier date of invention.

## III. THE ASSERTED CLAIMS OF THE '905 PATENT ARE INVALID

### A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits A-1 through A-6, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '905 Patent.

#### 1. The '905 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '905 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit A-1 through A-6 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art ("POSITA").

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '905 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '905 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.



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### a) Prior Art Patents and Applications[2]

| Number | Published/Issued Date | Short Name | Exhibit Number |
|---|---|---|---|
| UK Patent App. No. GB 2344029 | May 24, 2000 | Banes | A-1 |
| U.S. Patent No. 4,542,380 | September 17, 1985 | Beckner | A-2 |
| U.S. Patent No. 5,557,608 | September 17, 1996 | Calvignac | A-3 |
| U.S. Patent No. 5,845,085 | December 1, 1998 | Gulick | A-4 |
| U.S. Patent No. 5,574,934 | November 12, 1996 | Mirashrafi | A-5 |
| U.S. Patent No. 5,974,464 | October 26, 1999 | Shin | A-6 |

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the ’905 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not

[2] Where the accompanying charts cite a particular drawing or figure, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not by itself expressly cited). Similarly, where the accompanying charts cite particular text concerning a drawing or figure, the citation also encompasses that drawing or figure (even if the associated drawing or figure is not expressly cited).

specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

**b) Prior Art Systems**

On information and belief, the systems identified below were in public use, on sale, or otherwise available to the public before the priority date of the '905 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- G-Link chipset by HP (*e.g.*, HIPPI-6400, HIPPI-6400-SC, HIPPI-800).
- Alterra chipset ED8B10B
- Fast Ethernet devices, including those using 100-BASE chipsets employing IEEE 802.3u (*e.g.*, 100-BASE-TX, 100-BASE-FX, 100-BASE-T4)
- Fast Ethernet devices, including those using 100-BASE Chipset employing IEEE 802.z, or IEEE 802.ae. (*e.g.*, 1000-BASE-T, 1000-BASE-LX, 1000-BASE-CX, 1000-BASE-SX)
- Fibre Channel networks and devices
- Infiniband networks and devices
- 10GFC networks and devices
- Xaui

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '905 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

**2. The '905 Patent Claims Are Obvious Over the Prior Art**

To the extent Plaintiff argues that any limitation of the asserted claims of the '905 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits A-1 through A-6, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits A-1 through A-6 with each other, at least because these prior art references relate to data transmission methods and devices utilizing certain transmission schemes in the same field of endeavor and to solve similar problems. For example, the transmission schemes disclosed by the prior art include packet ordering, such as pausing, interrupting, prioritizing, and/or resuming paused transmissions of packetized data designed to solve a number of problems that were known in the art. *See, e.g.*,



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’905 Patent, 2:59-66 (“[e]xisting memory devices that are designed to support access patterns with a high temporal and spatial relationship may not be appropriate for uses having access patterns with a lower spatial relationship.”); 3:15-19 (“existing memory devices are not particularly suitable for many uses because the memory devices typically allow access by only one accessing device at a time and because the memory devices typically operate at different clock rates than the accessing devices.”); and 3:34-36 (“[e]xisting communications protocols, such as Fibre Channel, may have an unacceptable overhead for communicating with memory devices.”). Therefore, these references provide interrelated teachings and one of ordinary skill would have looked to the concepts in any of these references when attempting to solve the problems purportedly solved by the ’905 Patent, among other asserted patents.

Turning to the prior art, U.S. Patent No. 5,574,934 to Mirashrafi et. al (“Mirashrafi ’934”), issued on November 12, 1996, discloses a system for priority-based transmission of signals. Mirashrafi ’934 at Abstract. For instance, transmission of lower priority signals may be interrupted while signals of higher priority are transmitted before resumption of the lower priority signal transmission. *Id.* at 1:46-58. Signals may be transmitted in data packets over a communication link such as an ISDN channel. *Id.* at 71:11-23.

U.S. Patent No. 5,845,085 to Dale E. Gulick (“Gulick ’085”), issued on December 1, 1998, discloses a data-link controller for receiving and transmitting frames of serialized data over a data-link. Gulick ’085 at Abstract. Gulick ’085 specifically describes that data may often be transmitted or received in “packets” or “frames” of information. *Id.* at 1:17-25. Gulick ’085 further discusses the use of flag signals to mark states or conditions for the link controller transmitter or receiver. *Id.* at 2:18-44.

U.S. Patent No. 4,542,380 to Beckner, *et. al* ("Beckner '380"), issued September 17, 1985, discloses a method and apparatus for graceful preemption on a digital communications link. Beckner '380 at Abstract. A link controller is configured on a respective transmitting or receiving end of a communications link to interrupt and resume communications according to signals such as a "preemption signal" or "end preemption signal". *Id.* at 2:10-42.

U.S. Patent No. 5,974,464 to Shin, *et. al* ("Shin '464"), issued October 26, 1999, discloses a high speed digital interface for transmitting information (*e.g.*, video) over various transmission media. Shin '464 at Abstract. In particular, Shin '464 discloses an encoder and deserializer configured to distinguish encoded characters based on a number of logical transitions. *Id.* at 3:55-4:5. Shin '464 further discloses encoding and transmission of in-band and out-of-band characters such as control characters which can be distinguished from characters within the transmitted data stream. *Id.* at 9:49-10:8.

UK Patent Application No. GB 2,344,029 to David Banes ("Banes '029"), published on May 24, 2000, discloses a data communication network technique involving interruption of lower priority data packets such that higher priority packets can be transmitted. Banes '029 at Abstract. Banes '029 specifically discloses the use of priority flags, interrupt codes, and resumption codes in order to facilitate preemption and resumption of lower priority transmissions until higher priority packets are sent. *Id.* at 11:18-12:18.

U.S. Patent No. 5,557,608 to Calvignac et. al ("Calvignac '608"), issued September 17, 1996, discloses a method and apparatus for preempting low-priority traffic in favor of high-priority traffic transmission. Calvignac '608 at 2:25-38. Calvignac '608 discloses transmission of pieces of data in packets with headers used by each node of a packet switching network to send packets

toward their destination. *Id.* at 3:13-27. Calvignac '608 further discloses the use of byte aligned flags to signify starting and ending preemption. *Id.* at 4:44-49.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

To the extent that it is determined that any of the above references do not disclose a particular claim element, a person skilled in the art would have been motivated to combine any of the above references (as documented in the claim charts attached as Exhibits A-1 through A-6). In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to data transmission methods and devices utilizing certain transmission schemes.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the

problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards data transmission methods and devices utilizing certain transmission schemes, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

For example, to the extent that it is determined that any of the above references do not disclose the general concept of preempting and resuming data transmission as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934, Beckner '380, Calvignac '608, and Banes '029. As demonstrated in the attached claim charts for these references, each discloses preemption of data transmission on the basis of, *e.g.*, priority as was well known in the art at the time of the '905 filing. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose transmitting or receiving "packets" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934, Gulick '085, Calvignac '608, and Banes '029. As demonstrated in the attached claim charts for these references, each discloses transmission of data in various container formats including packets. For instance, Gulick '085 describes common data-link transmission in

"packets" or "frames" of information. Gulick '085 at 1:17-25. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose transmitting or receiving indicators such as a "preempt indicator" or "continue indicator" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Beckner '380, Banes '029, Calvignac '608, and Gulick '085. As demonstrated in the attached claim charts for these references, each discloses transmission of symbols or flags signifying preemption or resumption of data transmission. For instance, Beckner '380 describes a link controller for graceful preemption of data using characters such as "PREEMP", represented in binary as "111111110." Beckner '380 at 4:18-52. Similarly, Banes '029 discusses a priority detector and interrupt device to facilitate packet interruption and resumption using an "interrupt code" and "resume code," respectively. Banes '029 at 11:18-12:18. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "in-band symbols" and "out-of-band symbols" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Shin '464, Beckner '380, Calvignac '608, Banes '029, and Gulick '085. As demonstrated in the attached claim charts for these references, each discloses symbols or characters including those that are in-band and out-of-band. For instance, Shin '464 describes "selected out-of-band characters easily distinguishable from in-band characters." Shin '464 at 14:37-62. Similarly, Beckner '380 describes a link controller for graceful preemption of data using characters such as

"PREEMP," represented in binary as "111111110." Beckner '380 at 4:18-52. As discussed in the '905 Patent, in-band and out-of-band symbols may be distinguished by the number of bit transitions occurring in their binary representation. '905 Patent at 24:33-46. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "primitives" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934 and Shin '464. As demonstrated in the attached claim charts for these references, each discloses symbols or characters including in-band and out-of-band. For instance, Mirashrafi '934 describes a "set of primitives" such as "comm primitives" implemented for API calls. Mirashrafi '934 at 28:61-65. In addition, transmitting primitives for the purpose of communication and synchronization between networked components was well known in the art at the time of the '905 filing. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose a "header that is transmitted only once" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Calvignac '608, Mirashrafi '934, and Banes '029. As demonstrated in the attached claim charts for these references, each at least inherently discloses a header that is initially transmitted and is not repeated upon continuation of the packet transmission. For instance, Calvignac '608 at Fig. 5 depicts a first packet of data with a packet header, a second packet with a packet header, and the continuation of the first packet data without repeating the header. As discussed in the '905

specification, merging segmented packets of the same transaction would have been appreciated by a POSITA as a way to efficiently transmit packet switched data. '905 Patent at 13:18-39. Additionally, Mirashrafi '934 noted that it would be desirable for a computing system to avoid "being inundated with subsequent signal packets it may not be able to handle." *See* Mirashrafi '934, 78:9-15. To address this issue, Calvignac '608 provides a first packet of data with a packet header, a second packet with a packet header, and the continuation of the first packet data without repeating the header, to achieve the technological improvements contemplated by the existing prior art and the '905 Patent. Therefore, a POSITA would be motivated to make such a modification and/or combination.

In addition, one of ordinary skill in the art would have been motivated to combine the prior art references. One of skill in the art would have would have been motivated to combine these references: (1) by their education, knowledge, and experience; (2) by the state of the prior art as a whole; (3) by the nature of the problem to be solved; (4) by common sense and ordinary ingenuity; and (5) by a desire to create a device, system, and method of controlling communication of computer data. Moreover, one of ordinary skill in the art would have been well-equipped with sufficient education, knowledge, and training to make the specific combinations with a reasonable expectation of success given the simplicity of the electrical components to one of ordinary skill in the art, the predictability of the arts, and the minimal level of experimentation needed to combine the various teachings.

One of skill in the art, seeking to solve these problems, would have looked to analogous art to identify ways to solve the problem. Indeed, the solution identified by the patentee had already been identified by others in the field, and one of ordinary skill in the art would have been motivated to combine such analogous teachings in the same manner proposed by the patentee. Additionally,

one of skill in the art would have had a reasonable expectation of success because the references contained analogous teachings to those proposed by the patentee, the references describe relatively simple electrical technologies in predictable fields, and the modifications and combinations would not require undue experimentation. As such, one of skill would have been motivated to combine the references.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the ’905 Patent:

- Mirashrafi ’934 alone or in combination with Beckner ’380
- Mirashrafi ’934 alone or in combination with Shin ’464
- Calvignac ’608 alone or in combination with Beckner ’380
- Calvignac ’608 alone or in combination with Shin ’464
- Banes ’029 alone or in combination with Shin ’464

**B. Invalidity of the ’905 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)**

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’905 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that the Asserted Claims of the ’905 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- “the out-of-band symbols are not transition optimized.” (claim 3, 10, 17, and 23)
- “signals the transmission component to continue transmitting the first packet” (claim 21)

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do

not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

### C. Invalidity of the '905 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '905 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '905 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- "the indicators include one or more out-of-band symbols" (claims 1, 8, 15, and 21)
- "[the] packets include [one or more] in-band symbols" (claims 1, 15, and 21)
- "transition optimized." (claim 3, 10, 17, and 23)
- "the symbols of the packets include in-band symbols" (claim 8)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with or broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, at least claim 21 (and its dependent claims) of the '905 Patent recites functions without sufficient structure for performing the function, thus invoking 35 U.S.C. § 112,

¶ 6. Because the specification of the '905 Patent also does not recite structure for performing the function, the following terms are invalid as indefinite under 35 U.S.C. §§ 112, ¶ 2:

- "a transmission component that transmits a first packet" (claim 21)
- "a preemption component that signals the transmission component to stop transmitting the first packet, transmits a preempt indicator indicating that a second packet is to be transmitted, transmits the second packet, and signals the transmission component to continue transmitting the first packet" (claim 21)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

## IV. THE ASSERTED CLAIMS OF THE '307 PATENT ARE INVALID

### A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits B-1 through B-8, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '307 Patent.

#### 1. The '307 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '307 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit B-1 through B-9, or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

Dated: July 24, 2024

Respectfully Submitted,

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**CERTIFICATE OF SERVICE**

The undersigned certifies that a true and correct copy of the above and foregoing document has been served on July 24, 2024 to all counsel of record via electronic mail.

*/s/ Debbie Kakanas__*



Universal Connectivity Technologies Inc.
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# Exhibit A-0

## Cross-Reference Key for ’905 Patent Claim Charts

This chart provides a cross-reference key for use in understanding the mappings of prior art to the asserted claims of the ’905 patent in the claim charts of Exhibits A-1 through A-6. Those claim charts include internal cross-references. In particular, for claim elements in higher-numbered claims, rather than repeat the same evidence and analysis, the charts may cross-reference to the entry for a similar or identical claim element in a lower-numbered claim. The use of cross-references is not an admission that any claims or claim elements are indistinct or identical in scope. Rather, cross-references are used merely to simplify the charts where similar disclosure from a prior art reference may apply to multiple charted claim elements.

Where a first claim element is cross-referenced in the entry for a second claim element, it is intended that the cited disclosure and discussion in connection with the first element is fully incorporated by reference into the entry for the second claim element; if a third element cross-references the second claim element, therefore, the cited disclosure and discussion in connection with the first element would also be fully incorporated by reference into the entry for the third element.

To further clarify the cross-references and avoid confusion (and the possibility of inadvertent typographical errors), the right-hand column of the chart below identifies preceding claim elements from the ’905 patent for which the claim chart entries contain disclosure from the prior art reference that may be relevant to the claim element identified in the left two columns.

# Exhibit A-0

| Claim Limitation | | Relevant Disclosure Charted in Connection with Claim Limitation(s): |
|---|---|---|
| **Claim 1** | | |
| 1[p] | A method for transmitting packets, the method comprising: | N/A |
| 1[a] | receiving a first packet; | N/A |
| 1[b] | transmitting a portion of the received first packet; | N/A |
| 1[c] | receiving a second packet; | N/A |
| 1[d] | upon receiving the second packet, stopping the transmitting of the first packet so that not all of the first packet has been transmitted; | N/A |
| 1[e] | transmitting a preempt indicator; | N/A |
| 1[f] | transmitting the second packet; and | N/A |
| 1[g] | upon completion of transmitting the second packet, transmitting a continue indicator; and | N/A |
| 1[h] | transmitting the portion of the first packet that has not yet been transmitted; | N/A |
| 1[i] | wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols. | N/A |
| **Claim 8** | | |
| 8[p] | A method for receiving packets, the method comprising: | Claim element 1[p]: "A method for transmitting packets, the method comprising:" |
| 8[a] | receiving a first portion of symbols of a first packet; | Claim element 1[a]: "receiving a first packet;" |
| 8[b] | receiving a preempt indicator indicating that a second packet of symbols is to be received; | Claim element 1[e]: "transmitting a preempt indicator;" |

| | | |
|---|---|---|
| 8[c] | receiving the second packet of symbols; | Claim element 1[f]: "transmitting the second packet; and" |
| 8[d] | receiving a continue indicator indicating that a second portion of symbols of the first packet is to be received; and | Claim element 1[g]: "upon completion of transmitting the second packet, transmitting a continue indicator; and" |
| 8[e] | receiving the second portion of symbols of the first packet; | Claim element 1[h]: "transmitting the portion of the first packet that has not yet been transmitted;" |
| 8[f] | wherein the symbols of the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Claim element 1[i]: " wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 12** | | |
| 12 | The method of claim 8 wherein the first and second packets are received via the same communications link. | Claim element 8[p]: "A method for receiving packets, the method comprising:"<br><br>Claim element 8[a]: "receiving a first portion of symbols of a first packet;"<br><br>Claim element 8[b]: "receiving a preempt indicator indicating that a second packet of symbols is to be received;"<br><br>Claim element 8[c]: "receiving the second packet of symbols;"<br><br>Claim element 8[d]: "receiving a continue indicator indicating that a second portion of symbols of the first packet is to be received; and"<br><br>Claim element 8[e]: "receiving the second portion of symbols of the first packet;"<br><br>Claim element 8[f]: "wherein the symbols of the packets include in-band symbols and the indicators include one or more out-of-band symbols." |

## Exhibit A-0

| Claim 15 | | |
|---|---|---|
| 15[p] | A method for transmitting packets via a communications link, the method comprising: | Claim element 1[p]: "A method for transmitting packets, the method comprising:" |
| 15[a] | transmitting a first portion of a first packet; | Claim element 1[b]: "transmitting a portion of the received first packet;" |
| 15[b] | transmitting a preempt indicator indicating that a second packet is to be transmitted; | Claim element 1[e]: "transmitting a preempt indicator;" |
| 15[c] | transmitting the second packet; | Claim element 1[f]: "transmitting the second packet; and" |
| 15[d] | transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and | Claim element 1[g]: "upon completion of transmitting the second packet, transmitting a continue indicator; and" |
| 15[e] | transmitting the second portion of the first packet | Claim element 1[h]: "transmitting the portion of the first packet that has not yet been transmitted;" |
| 15[f] | wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link and | Claim 12: "The method of claim 8 wherein the first and second packets are received via the same communications link." |
| 15[f.1] | wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Claim element 1[i]: "wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 16** | | |
| 16 | The method of claim 15 wherein the indicators are primitives. | Claim element 15[p]: "A method for transmitting packets via a communications link, the method comprising:"<br><br>Claim element 15[a]: "transmitting a first portion of a first packet;"<br><br>Claim element 15[b]: "transmitting a preempt indicator indicating that a second packet is to be transmitted;" |

| | | |
|---|---|---|
| | | Claim element 15[c]: "transmitting the second packet;"<br><br>Claim element 15[d]: "transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and"<br><br>Claim element 15[e]: "transmitting the second portion of the first packet"<br><br>Claim element 15[f]: "wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link; and"<br><br>Claim element 15[f.1]: "wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 17** | | |
| 17 | The method of claim 15 wherein the in-band symbols are transition optimized and the out-of-band symbols are not transition optimized. | Claim element 15[p]: "A method for transmitting packets via a communications link, the method comprising:"<br><br>Claim element 15[a]: "transmitting a first portion of a first packet;"<br><br>Claim element 15[b]: "transmitting a preempt indicator indicating that a second packet is to be transmitted;"<br><br>Claim element 15[c]: "transmitting the second packet;"<br><br>Claim element 15[d]: "transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and" |

| | | |
|---|---|---|
| | | Claim element 15[e]: "transmitting the second portion of the first packet"<br><br>Claim element 15[f]: "wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link; and"<br><br>Claim element 15[f.1]: "wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 20** | | |
| 20 | The method of claim 15 wherein the first packet includes a header that is transmitted only once. | Claim element 15[p]: "A method for transmitting packets via a communications link, the method comprising:"<br><br>Claim element 15[a]: "transmitting a first portion of a first packet;"<br><br>Claim element 15[b]: "transmitting a preempt indicator indicating that a second packet is to be transmitted;"<br><br>Claim element 15[c]: "transmitting the second packet;"<br><br>Claim element 15[d]: "transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and"<br><br>Claim element 15[e]: "transmitting the second portion of the first packet"<br><br>Claim element 15[f]: "wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link; and" |

| | | |
|---|---|---|
| | | Claim element 15[f.1]: "wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 21** | | |
| 21[p] | A communications device for transmitting packets via a communications link, comprising: | Claim element 1[p]: "A method for transmitting packets, the method comprising:" |
| 21[a] | a transmission component that transmits a first packet; and | Claim element 1[b]: "transmitting a portion of the received first packet;" |
| 21[b] | a preemption component that signals the transmission component to stop transmitting the first packet, | Claim element 1[d]: "upon receiving the second packet, stopping the transmitting of the first packet so that not all of the first packet has been transmitted;" |
| 21[b.1] | transmits a preempt indicator indicating that a second packet is to be transmitted, | Claim element 1[d]: "upon receiving the second packet, stopping the transmitting of the first packet so that not all of the first packet has been transmitted;" |
| 21[b.2] | transmits the second packet, and | Claim element 1[f]: |
| 21[b.3] | signals the transmission component to continue transmitting the first packet; | Claim element 1[g]: "upon completion of transmitting the second packet, transmitting a continue indicator; and"<br><br>Claim element 1[h]: "transmitting the portion of the first packet that has not yet been transmitted;" |
| 21[c] | wherein packets include in-band symbols and the indicators include one or more out-of-band symbols. | Claim element 1[i]: "wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols." |
| **Claim 22** | | |
| 22 | The communications device of claim 21 wherein the indicators are primitives. | Claim element 21[p]: "A communications device for transmitting packets via a communications link, comprising:"<br><br>Claim element 21[a]: "a transmission component that transmits a first packet; and" |

| | | |
|---|---|---|
| | | Claim element 21[b]: "a preemption component that signals the transmission component to stop transmitting the first packet," Claim element 21[b.1]: "transmits a preempt indicator indicating that a second packet is to be transmitted,"<br><br>Claim element 21[b.2]: "transmits the second packet, and"<br><br>Claim element 21[b.3]: "signals the transmission component to continue transmitting the first packet;"<br><br>Claim element 21[c]: "wherein packets include in-band symbols and the indicators include one or more out-of-band symbols."<br><br>Claim 16: "The method of claim 15 wherein the indicators are primitives." |
| **Claim 23** | | |
| 23 | The communications device of claim 21 wherein the in-band symbols are transition optimized and the out-of-band symbols are not transition optimized. | Claim element 21[p]: "A communications device for transmitting packets via a communications link, comprising:"<br><br>Claim element 21[a]: "a transmission component that transmits a first packet; and"<br><br>Claim element 21[b]: "a preemption component that signals the transmission component to stop transmitting the first packet,"<br><br>Claim element 21[b.1]: "transmits a preempt indicator indicating that a second packet is to be transmitted,"<br><br>Claim element 21[b.2]: "transmits the second packet, and"<br><br>Claim element 21[b.3]: "signals the transmission component to continue transmitting the first packet;" |

| | | |
|---|---|---|
| | | Claim element 21[c]: "wherein packets include in-band symbols and the indicators include one or more out-of-band symbols."<br><br>Claim 17: " The method of claim 15 wherein the in-band symbols are transition optimized and the out-of-band symbols are not transition optimized." |
| **Claim 26** | | |
| 26 | The communications device of claim 21 wherein the first packet includes a header that is transmitted only once. | Claim element 21[p]: "A communications device for transmitting packets via a communications link, comprising:"<br><br>Claim element 21[a]: "a transmission component that transmits a first packet; and"<br><br>Claim element 21[b]: "a preemption component that signals the transmission component to stop transmitting the first packet,"<br><br>Claim element 21[b.1]: "transmits a preempt indicator indicating that a second packet is to be transmitted,"<br><br>Claim element 21[b.2]: "transmits the second packet, and"<br><br>Claim element 21[b.3]: "signals the transmission component to continue transmitting the first packet;"<br><br>Claim element 21[c]: "wherein packets include in-band symbols and the indicators include one or more out-of-band symbols."<br><br>Claim 20: "The method of claim 15 wherein the first packet includes a header that is transmitted only once." |

# Exhibit A-1

**Invalidity of the '905 Patent in View of UK Patent Application No. GB 2,344,029 to David Banes (Banes '029)**

This chart provides examples of where the prior art reference discloses, either expressly or inherently, the claim elements of asserted U.S. Patent No. 7,154,905 ("the '905 patent"). The citations herein are exemplary and are not exhaustive; Defendant has cited the most relevant portions of the identified prior art. For each citation, Defendant hereby incorporates by reference the entire cited prior art reference, and reserves the right to rely on uncited portions of each identified prior art reference. To provide context or identify the state of the art at the time of the alleged invention, Defendant reserves the right to rely on: (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art); (4) factual testimony from the inventors or authors of the prior art references, or purveyors of prior art devices; and (5) expert testimony.

Where Defendant cites a figure, the citation includes any text associated with the figure. Where Defendant cites passages relating to a figure, the citation includes the associated figure any other text associated with that figure. Where Defendant cites particular prior art as disclosing a claim element, that citation equally applies to all identical or similar claim elements in this chart. Defendant reserves the right to further assert that a claim element is inherent, the element would have been obvious to a person of ordinary skill in the art, or the element is disclosed in other prior art that may be combined with the cited prior art. To establish the inherency of certain features of the prior art to invalidate the asserted claims, Defendant may rely on cited or uncited portions of the prior art, other documents, factual testimony, and expert testimony.

This invalidity chart is based on information presently available to Defendant, and the information herein is provided as a non-limiting example.

Banes '029 was filed on October 2, 1998, and published on May 24, 2000; therefore, Banes '029 is prior art under at least 35 U.S.C. § 102(b).

# Exhibit A-1

| Claim Limitation | | Banes '029 |
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| | | **Claim 1** |
| 1[p] | A method for transmitting packets, the method comprising: | To the extent the preamble is limiting, Banes '029 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>"The transmission of a lower priority data packet over a network is interrupted so that a data packet of a higher priority can be transmitted, after which the transmission of the lower priority data packet is resumed. A code is inserted into the lower priority packet signifying interruption. Interruption may be decline if a count of interruptions reaches a maximum count. Data packets have a length or type field in the header signifying long or short packets. The packet size is selected according to voice or data applications. Application is to ATM or Ethernet networks." Banes '029 at Abstract.<br><br>"The present invention relates to a data communication network.<br><br>There are a number of data communication protocols in common usage.<br><br>As is well-known, a data communication protocol is defined as a series of hierarchal layers, the lowest layer defining the physical characteristics of the transfer medium (for example cable or fiber optic), and higher levels defining software interfacing to applications.<br><br>One example of a known communications network is an Ethernet network. In such a network data is transported in packets of a variable length of up to approximately 1500 bytes. This type of network is well suited to local area network (LAN) applications for transferring computer data files or for transferring TCP/IP data, which is generally transferred in large blocks. It is not, however, as well suited to voice or to telecommunications networks in which data needs to be switched rapidly and frequently between destinations.<br><br>Another example of a network is an ATM network. In such a network, data is transmitted in fixed length cells of 53 bytes, 48 bytes of which contain the data or "payload" and 5 bytes of which contain a header. Because of the small size of the packets, packets can be readily switched between several different destinations, and the network is well suited to the needs of |

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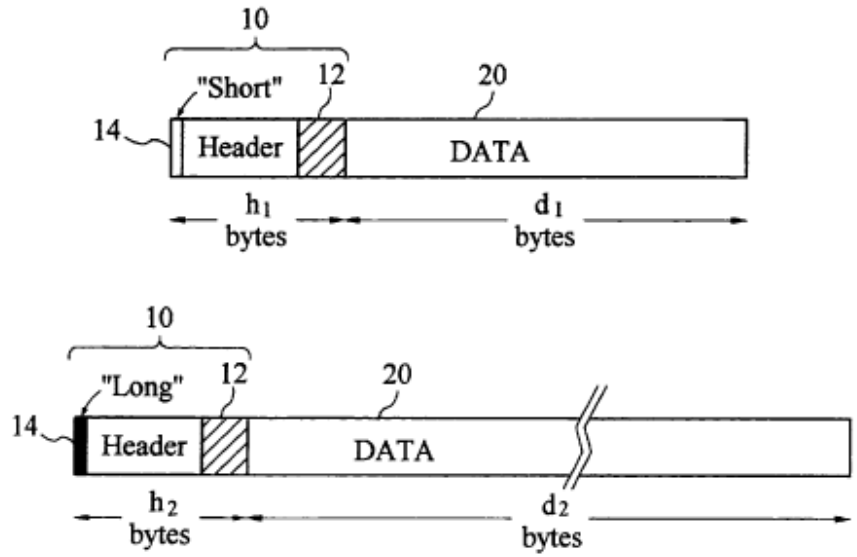
| | | telecommunications and voice traffic. Larger blocks of data can be accommodated simply by transmitting them over a series of ATM packets. ATM networks have been successfully used to carry both voice and computer data. The small size of the packets enables efficient statistical multiplexing.<br><br>In both the above prior art systems, the data packets are of a fixed maximum length. Division of a long data block into separate packets is performed at a higher level, by software."<br>Banes '029 at 1:1-26.<br><br>  <br><br>*Fig. 1*<br><br>Banes '029 at Fig. 1. |

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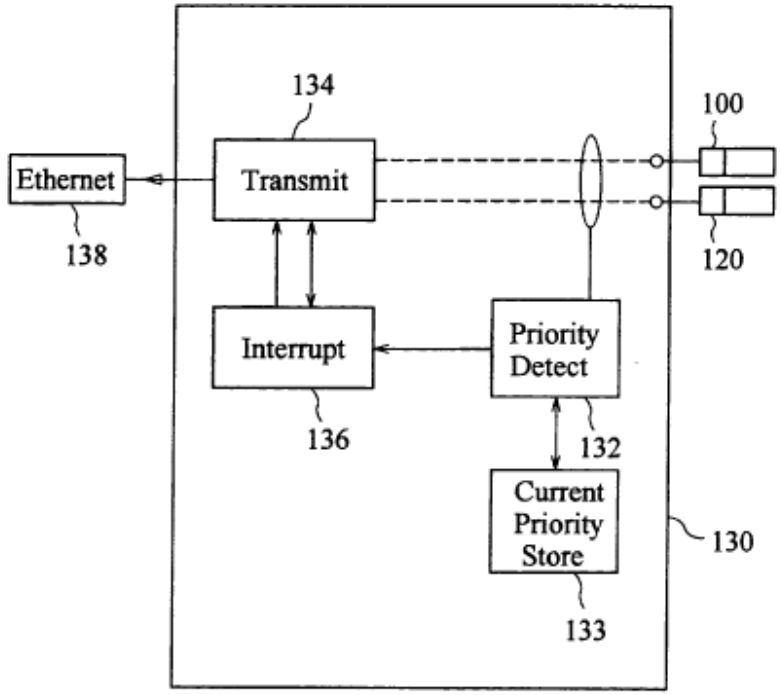
| | | *Fig. 5*<br>  <br><br>Banes '029 at Fig. 5.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(a) | receiving a first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"The inventor has appreciated that, whilst an ATM network can provide 2 an efficient and effective network for transmitting both voice and data, efficiency can be impaired when large |

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| | | amounts of data are transmitted. On the other hand, a network such as an ethernet may cause unacceptable delays between packets and cannot readily be used for voice traffic. Accordingly, it is an aim of the present invention to provide a network which can efficiently transfer both voice and computer data or which can transfer large blocks of data efficiently without unduly delaying transit of smaller or more important data packets.<br><br>In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data."<br>Banes '029 at 1:28-2:16.<br><br>"In a related apparatus aspect, the invention provides apparatus for communicating data over a network comprising means for transmitting a first data packet, means for receiving a higher priority data packet, means for interrupting transmitting the first data packet to transmit the higher priority data packet, and means for resuming transmission of the first data packet.<br><br>In a second method aspect, the invention provides a method of communicating data over a network comprising selecting one of at least two predetermined packet sizes based on the data type and transmitting a packet of the selected size over the network.<br><br>In this way, rather than using fixed length packets, a packet size is "intelligently" selected to be appropriate to the data being transmitted. For example, voice data may be transmitted in a relatively short packet, preferably of approximately 64 bytes or less, and other data may be transmitted in a relatively long packet, preferably of at least about 256 bytes, one kilobyte, or more. Of course, such a method may require a more complex routing system and physical arrangement, which must deal with data packets of different sizes. Surprisingly, however, an improvement in network performance may be gained by dividing data in this way prior to transmission." |

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| | | Banes ‘029 at 3:3-20.<br><br>“In a third aspect, the invention provides a transmitter for connection to a communication network comprising means for selecting a data packet length from a plurality of predetermined packet lengths; means for providing a header for the data packet, the header including at least one flag bit indicating the length or format of the data packet; and means for transmitting the data packet over the communication medium.<br><br>In a fourth aspect, the invention provides a receiver for receiving data from a communication network, the receiver including means for reading a flag bit contained in the header of a data packet transmitted on the communication medium; means for determining the size or format of data packet to receive based on the information; and means for receiving a data packet of said size or format.”<br>Banes ‘029 at 4:23-5:6.<br><br>“Fig. 1 is a schematic diagram of data packets according to the second aspect of the invention; Fig. 2 is a schematic diagram of a computer network embodying the invention; Fig. 3 is a simplified schematic diagram of a switch for use in a network of Fig. 2; Fig. 4 is a schematic diagram of transmission of data packets according to the first aspect of the invention; and Fig. 5 is a schematic diagram of apparatus for implementing the transmission of Fig. 4.<br><br>An embodiment of the invention based on an ATM network will be described. Whilst this embodiment is based closely on ATM protocol, for ease of implementation by modification of existing ATM network components it is to be understood that the principles are applicable to other data formats.<br><br>Referring to Fig. I a data packet according to the invention comprises a header 10 and a data portion 20. The header comprises routing information 12 and a length or type field 14, which in this embodiment comprises a single bit signifying "long" or "short". The header may also contain information such as priority information.”<br>Banes ‘029 at 5:9-27. |

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| | | "A network as shown in Fig. 2 includes a "short" packet assembler/disassembler 40 for interfacing a voice communication device such as a telephone 42 to the network. The short PAD 40 may receive signals in either analog or digital form from the telephone 42 and produces ATM-type packets with an additional initial flag bit signifying that the packet is a short packet. A single PAD 40 may be coupled to a plurality of voice input devices; in such a case, the PAD 40 is arranged to perform final routing of received packets to the appropriate voice terminal.<br><br>In a similar manner, a long PAD 50 is arranged to receive data from the data input terminals such as a computer 52. This produces packets similar to conventional ATM packets, but having a considerably longer data field, and an initial flag bit indicating that the packet is long. Optionally, the packet may contain a cyclic redundancy check (CRC) or other error-correcting or error detecting information, either in the header, or appended to the data. Referring back to Figure 1, it will be noted that the header for the short packets and for the long packets is not necessarily of the same length, nor is it necessarily in the same format.<br><br>The above described PADs 40, 50 are dedicated to either short or long packets. This may offer some advantages in terms of simplicity of hardware required.<br><br>In this embodiment, a network also includes a combined PAD 60, which incorporates a data type identifier, with a connection 62 for receiving combined data from a further telephone 42, a further computer 52, and a facsimile machine 64. The PAD 60 identifies the data, and in the case of voice data, assembles the data into short packets, but assembles data from the facsimile machine or computer 52 into long packets.<br><br>The three PADs 40, 50, 60 are connected to a multiplexer 70, which combines all packets, both short and long, for transmission along a common transmission medium 72, for example optical fibre, for example using a SONET protocol. It will appreciated that the multiplexer also serves as a demultiplexer, and performs routing of received data packets to the appropriate PAD. In this embodiment, transmission along the common transmission medium 72 is via separate physical optical fibres or received in transmitted data, as is conventional with ATM network."<br>Banes '029 at 6:22-7:26. |

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| | | To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(b) | transmitting a portion of the received first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"The inventor has appreciated that, whilst an ATM network can provide 2 an efficient and effective network for transmitting both voice and data, efficiency can be impaired when large amounts of data are transmitted. On the other hand, a network such as an ethernet may cause unacceptable delays between packets and cannot readily be used for voice traffic. Accordingly, it is an aim of the present invention to provide a network which can efficiently transfer both voice and computer data or which can transfer large blocks of data efficiently without unduly delaying transit of smaller or more important data packets.<br><br>In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data."<br>Banes '029 at 1:28-2:16.<br><br>"In a related apparatus aspect, the invention provides apparatus for communicating data over a network comprising means for transmitting a first data packet, means for receiving a higher priority data packet, means for interrupting transmitting the first data packet to transmit the higher priority data packet, and means for resuming transmission of the first data packet.<br><br>In a second method aspect, the invention provides a method of communicating data over a network comprising selecting one of at least two predetermined packet sizes based on the data type and transmitting a packet of the selected size over the network. |

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| | | In this way, rather than using fixed length packets, a packet size is "intelligently" selected to be appropriate to the data being transmitted. For example, voice data may be transmitted in a relatively short packet, preferably of approximately 64 bytes or less, and other data may be transmitted in a relatively long packet, preferably of at least about 256 bytes, one kilobyte, or more. Of course, such a method may require a more complex routing system and physical arrangement, which must deal with data packets of different sizes. Surprisingly, however, an improvement in network performance may be gained by dividing data in this way prior to transmission."<br>Banes '029 at 3:3-20.<br><br>"In a third aspect, the invention provides a transmitter for connection to a communication network comprising means for selecting a data packet length from a plurality of predetermined packet lengths; means for providing a header for the data packet, the header including at least one flag bit indicating the length or format of the data packet; and means for transmitting the data packet over the communication medium.<br><br>In a fourth aspect, the invention provides a receiver for receiving data from a communication network, the receiver including means for reading a flag bit contained in the header of a data packet transmitted on the communication medium; means for determining the size or format of data packet to receive based on the information; and means for receiving a data packet of said size or format."<br>Banes '029 at 4:23-5:6.<br><br>"Fig. 1 is a schematic diagram of data packets according to the second aspect of the invention; Fig. 2 is a schematic diagram of a computer network embodying the invention; Fig. 3 is a simplified schematic diagram of a switch for use in a network of Fig. 2; Fig. 4 is a schematic diagram of transmission of data packets according to the first aspect of the invention; and Fig. 5 is a schematic diagram of apparatus for implementing the transmission of Fig. 4.<br><br>An embodiment of the invention based on an ATM network will be described. Whilst this embodiment is based closely on ATM protocol, for ease of implementation by modification of |

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| | | existing ATM network components it is to be understood that the principles are applicable to other data formats.<br><br>Referring to Fig. I a data packet according to the invention comprises a header 10 and a data portion 20. The header comprises routing information 12 and a length or type field 14, which in this embodiment comprises a single bit signifying "long" or "short". The header may also contain information such as priority information."<br>Banes '029 at 5:9-27.<br><br>"A network as shown in Fig. 2 includes a "short" packet assembler/disassembler 40 for interfacing a voice communication device such as a telephone 42 to the network. The short PAD 40 may receive signals in either analog or digital form from the telephone 42 and produces ATM-type packets with an additional initial flag bit signifying that the packet is a short packet. A single PAD 40 may be coupled to a plurality of voice input devices; in such a case, the PAD 40 is arranged to perform final routing of received packets to the appropriate voice terminal.<br><br>In a similar manner, a long PAD 50 is arranged to receive data from the data input terminals such as a computer 52. This produces packets similar to conventional ATM packets, but having a considerably longer data field, and an initial flag bit indicating that the packet is long. Optionally, the packet may contain a cyclic redundancy check (CRC) or other error-correcting or error detecting information, either in the header, or appended to the data. Referring back to Figure 1, it will be noted that the header for the short packets and for the long packets is not necessarily of the same length, nor is it necessarily in the same format.<br><br>The above described PADs 40, 50 are dedicated to either short or long packets. This may offer some advantages in terms of simplicity of hardware required.<br><br>In this embodiment, a network also includes a combined PAD 60, which incorporates a data type identifier, with a connection 62 for receiving combined data from a further telephone 42, a further computer 52, and a facsimile machine 64. The PAD 60 identifies the data, and in the case of voice data, assembles the data into short packets, but assembles data from the facsimile machine or computer 52 into long packets. |

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| | | The three PADs 40, 50, 60 are connected to a multiplexer 70, which combines all packets, both short and long, for transmission along a common transmission medium 72, for example optical fibre, for example using a SONET protocol. It will appreciated that the multiplexer also serves as a demultiplexer, and performs routing of received data packets to the appropriate PAD. In this embodiment, transmission along the common transmission medium 72 is via separate physical optical fibres or received in transmitted data, as is conventional with ATM network."<br>Banes '029 at 6:22-7:26.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(c) | receiving a second packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"The inventor has appreciated that, whilst an ATM network can provide 2 an efficient and effective network for transmitting both voice and data, efficiency can be impaired when large amounts of data are transmitted. On the other hand, a network such as an ethernet may cause unacceptable delays between packets and cannot readily be used for voice traffic. Accordingly, it is an aim of the present invention to provide a network which can efficiently transfer both voice and computer data or which can transfer large blocks of data efficiently without unduly delaying transit of smaller or more important data packets.<br><br>In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data."<br>Banes '029 at 1:28-2:16. |

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| | | "In a related apparatus aspect, the invention provides apparatus for communicating data over a network comprising means for transmitting a first data packet, means for receiving a higher priority data packet, means for interrupting transmitting the first data packet to transmit the higher priority data packet, and means for resuming transmission of the first data packet.<br><br>In a second method aspect, the invention provides a method of communicating data over a network comprising selecting one of at least two predetermined packet sizes based on the data type and transmitting a packet of the selected size over the network.<br><br>In this way, rather than using fixed length packets, a packet size is "intelligently" selected to be appropriate to the data being transmitted. For example, voice data may be transmitted in a relatively short packet, preferably of approximately 64 bytes or less, and other data may be transmitted in a relatively long packet, preferably of at least about 256 bytes, one kilobyte, or more. Of course, such a method may require a more complex routing system and physical arrangement, which must deal with data packets of different sizes. Surprisingly, however, an improvement in network performance may be gained by dividing data in this way prior to transmission."<br>Banes '029 at 3:3-20.<br><br>"In a third aspect, the invention provides a transmitter for connection to a communication network comprising means for selecting a data packet length from a plurality of predetermined packet lengths; means for providing a header for the data packet, the header including at least one flag bit indicating the length or format of the data packet; and means for transmitting the data packet over the communication medium.<br><br>In a fourth aspect, the invention provides a receiver for receiving data from a communication network, the receiver including means for reading a flag bit contained in the header of a data packet transmitted on the communication medium; means for determining the size or format of data packet to receive based on the information; and means for receiving a data packet of said size or format."<br>Banes '029 at 4:23-5:6. |

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| | | "Fig. 1 is a schematic diagram of data packets according to the second aspect of the invention; Fig. 2 is a schematic diagram of a computer network embodying the invention; Fig. 3 is a simplified schematic diagram of a switch for use in a network of Fig. 2; Fig. 4 is a schematic diagram of transmission of data packets according to the first aspect of the invention; and Fig. 5 is a schematic diagram of apparatus for implementing the transmission of Fig. 4.<br><br>An embodiment of the invention based on an ATM network will be described. Whilst this embodiment is based closely on ATM protocol, for ease of implementation by modification of existing ATM network components it is to be understood that the principles are applicable to other data formats.<br><br>Referring to Fig. I a data packet according to the invention comprises a header 10 and a data portion 20. The header comprises routing information 12 and a length or type field 14, which in this embodiment comprises a single bit signifying "long" or "short". The header may also contain information such as priority information."<br>Banes '029 at 5:9-27.<br><br>"A network as shown in Fig. 2 includes a "short" packet assembler/disassembler 40 for interfacing a voice communication device such as a telephone 42 to the network. The short PAD 40 may receive signals in either analog or digital form from the telephone 42 and produces ATM-type packets with an additional initial flag bit signifying that the packet is a short packet. A single PAD 40 may be coupled to a plurality of voice input devices; in such a case, the PAD 40 is arranged to perform final routing of received packets to the appropriate voice terminal.<br><br>In a similar manner, a long PAD 50 is arranged to receive data from the data input terminals such as a computer 52. This produces packets similar to conventional ATM packets, but having a considerably longer data field, and an initial flag bit indicating that the packet is long. Optionally, the packet may contain a cyclic redundancy check (CRC) or other error-correcting or error detecting information, either in the header, or appended to the data. Referring back to Figure 1, it will be noted that the header for the short packets and for the long packets is not necessarily of the same length, nor is it necessarily in the same format. |

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| | | The above described PADs 40, 50 are dedicated to either short or long packets. This may offer some advantages in terms of simplicity of hardware required.<br><br>In this embodiment, a network also includes a combined PAD 60, which incorporates a data type identifier, with a connection 62 for receiving combined data from a further telephone 42, a further computer 52, and a facsimile machine 64. The PAD 60 identifies the data, and in the case of voice data, assembles the data into short packets, but assembles data from the facsimile machine or computer 52 into long packets.<br><br>The three PADs 40, 50, 60 are connected to a multiplexer 70, which combines all packets, both short and long, for transmission along a common transmission medium 72, for example optical fibre, for example using a SONET protocol. It will appreciated that the multiplexer also serves as a demultiplexer, and performs routing of received data packets to the appropriate PAD. In this embodiment, transmission along the common transmission medium 72 is via separate physical optical fibres or received in transmitted data, as is conventional with ATM network."<br>Banes '029 at 6:22-7:26.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(d) | upon receiving the second packet, stopping the transmitting of the first packet so that not all of the first packet has been transmitted; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data. |

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| | | Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme |

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| | | used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(e) | transmitting a preempt indicator; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet. |

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| | | A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet. |

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| | | Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(f) | transmitting the second packet; and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27. |

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| | | "Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more |

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| | | references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(g) | upon completion of transmitting the second packet, transmitting a continue indicator; and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt |

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| | | code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(h) | transmitting the portion of the first packet that has not yet been transmitted; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting |

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| | | transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet. |

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| | | Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(i) | wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then |

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| | | sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 8** | | |
| 8[p] | A method for receiving packets, the method comprising: | To the extent the preamble is limiting, Banes '029 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1[pre]. |

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| | | To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(a) | receiving a first portion of symbols of a first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.a.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(b) | receiving a preempt indicator indicating that a second packet of symbols is to be received; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.e.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(c) | receiving the second packet of symbols; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more |

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| | | references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(d) | receiving a continue indicator indicating that a second portion of symbols of the first packet is to be received; and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.g.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(e) | receiving the second portion of symbols of the first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.h.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(f) | wherein the symbols of the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 12** | | |
| 12 | The method of claim 8 wherein the first and | Banes '029 discloses, expressly or inherently, the transmitting device of claim 8 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: |

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| | second packets are received via the same communications link. | *See* exemplary disclosures and corresponding discussion for claim 8.<br><br>"The inventor has appreciated that, whilst an ATM network can provide 2 an efficient and effective network for transmitting both voice and data, efficiency can be impaired when large amounts of data are transmitted. On the other hand, a network such as an ethernet may cause unacceptable delays between packets and cannot readily be used for voice traffic. Accordingly, it is an aim of the present invention to provide a network which can efficiently transfer both voice and computer data or which can transfer large blocks of data efficiently without unduly delaying transit of smaller or more important data packets.<br><br>In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data."<br>Banes '029 at 1:28-2:16.<br><br>"In a related apparatus aspect, the invention provides apparatus for communicating data over a network comprising means for transmitting a first data packet, means for receiving a higher priority data packet, means for interrupting transmitting the first data packet to transmit the higher priority data packet, and means for resuming transmission of the first data packet.<br><br>In a second method aspect, the invention provides a method of communicating data over a network comprising selecting one of at least two predetermined packet sizes based on the data type and transmitting a packet of the selected size over the network.<br><br>In this way, rather than using fixed length packets, a packet size is "intelligently" selected to be appropriate to the data being transmitted. For example, voice data may be transmitted in a relatively short packet, preferably of approximately 64 bytes or less, and other data may be transmitted in a relatively long packet, preferably of at least about 256 bytes, one kilobyte, or |

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| | | more. Of course, such a method may require a more complex routing system and physical arrangement, which must deal with data packets of different sizes. Surprisingly, however, an improvement in network performance may be gained by dividing data in this way prior to transmission."<br>Banes '029 at 3:3-20.<br><br>"In a third aspect, the invention provides a transmitter for connection to a communication network comprising means for selecting a data packet length from a plurality of predetermined packet lengths; means for providing a header for the data packet, the header including at least one flag bit indicating the length or format of the data packet; and means for transmitting the data packet over the communication medium.<br><br>In a fourth aspect, the invention provides a receiver for receiving data from a communication network, the receiver including means for reading a flag bit contained in the header of a data packet transmitted on the communication medium; means for determining the size or format of data packet to receive based on the information; and means for receiving a data packet of said size or format."<br>Banes '029 at 4:23-5:6.<br><br>"Fig. 1 is a schematic diagram of data packets according to the second aspect of the invention; Fig. 2 is a schematic diagram of a computer network embodying the invention; Fig. 3 is a simplified schematic diagram of a switch for use in a network of Fig. 2; Fig. 4 is a schematic diagram of transmission of data packets according to the first aspect of the invention; and Fig. 5 is a schematic diagram of apparatus for implementing the transmission of Fig. 4.<br><br>An embodiment of the invention based on an ATM network will be described. Whilst this embodiment is based closely on ATM protocol, for ease of implementation by modification of existing ATM network components it is to be understood that the principles are applicable to other data formats.<br><br>Referring to Fig. I a data packet according to the invention comprises a header 10 and a data portion 20. The header comprises routing information 12 and a length or type field 14, which in this |

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| | | embodiment comprises a single bit signifying "long" or "short". The header may also contain information such as priority information."<br>Banes '029 at 5:9-27.<br><br>"A network as shown in Fig. 2 includes a "short" packet assembler/disassembler 40 for interfacing a voice communication device such as a telephone 42 to the network. The short PAD 40 may receive signals in either analog or digital form from the telephone 42 and produces ATM-type packets with an additional initial flag bit signifying that the packet is a short packet. A single PAD 40 may be coupled to a plurality of voice input devices; in such a case, the PAD 40 is arranged to perform final routing of received packets to the appropriate voice terminal.<br><br>In a similar manner, a long PAD 50 is arranged to receive data from the data input terminals such as a computer 52. This produces packets similar to conventional ATM packets, but having a considerably longer data field, and an initial flag bit indicating that the packet is long. Optionally, the packet may contain a cyclic redundancy check (CRC) or other error-correcting or error detecting information, either in the header, or appended to the data. Referring back to Figure 1, it will be noted that the header for the short packets and for the long packets is not necessarily of the same length, nor is it necessarily in the same format.<br><br>The above described PADs 40, 50 are dedicated to either short or long packets. This may offer some advantages in terms of simplicity of hardware required.<br><br>In this embodiment, a network also includes a combined PAD 60, which incorporates a data type identifier, with a connection 62 for receiving combined data from a further telephone 42, a further computer 52, and a facsimile machine 64. The PAD 60 identifies the data, and in the case of voice data, assembles the data into short packets, but assembles data from the facsimile machine or computer 52 into long packets.<br><br>The three PADs 40, 50, 60 are connected to a multiplexer 70, which combines all packets, both short and long, for transmission along a common transmission medium 72, for example optical fibre, for example using a SONET protocol. It will appreciated that the multiplexer also serves as a demultiplexer, and performs routing of received data packets to the appropriate PAD. In this |

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| | | embodiment, transmission along the common transmission medium 72 is via separate physical optical fibres or received in transmitted data, as is conventional with ATM network."<br>Banes '029 at 6:22-7:26.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 15** | | |
| 15[p] | A method for transmitting packets via a communications link, the method comprising: | To the extent the preamble is limiting, Banes '029 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1[pre].<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(a) | transmitting a first portion of a first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.b.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(b) | transmitting a preempt indicator indicating that a | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*: |

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| | second packet is to be transmitted; | *See* exemplary disclosures and corresponding discussion for Claim 1.e.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(c) | transmitting the second packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(d) | transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.g.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(e) | transmitting the second portion of the first packet | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.h.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more |

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| | | references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(f) | wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 12.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(f.1) | wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 16** | | |
| 16 | The method of claim 15 wherein the indicators are primitives. | Banes '029 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt |

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| | | code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 17** | | |
| 17 | The method of claim 15 wherein the in-band symbols are transition optimized and the out-of- | Banes '029 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15. |

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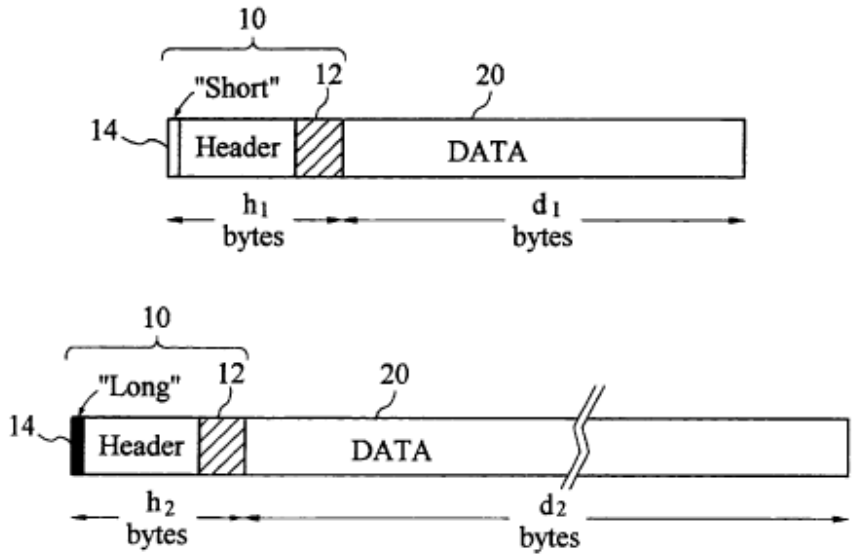
| | band symbols are not transition optimized. | To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 20** | | |
| 20 | The method of claim 15 wherein the first packet includes a header that is transmitted only once. | Banes '029 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. See, e.g.:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15.<br><br>  <br><br>*Fig. 1*<br><br>Banes '029 at Fig. 1. |

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| | | "Referring to Fig. I a data packet according to the invention comprises a header 10 and a data portion 20. The header comprises routing information 12 and a length or type field 14, which in this embodiment comprises a single bit signifying "long" or "short". The header may also contain information such as priority information."<br>Banes '029 at 5:23-25.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 21** | | |
| 21[p] | A communications device for transmitting packets via a communications link, comprising: | To the extent the preamble is limiting, Banes '029 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>"In a related apparatus aspect, the invention provides apparatus for communicating data over a network comprising means for transmitting a first data packet, means for receiving a higher priority data packet, means for interrupting transmitting the first data packet to transmit the higher priority data packet, and means for resuming transmission of the first data packet."<br>Banes '029 at 3:3-7.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1[pre].<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(a) | a transmission component that transmits a first packet; and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting |

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| | | transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet. |

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| | | Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.b.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b) | a preemption component that signals the transmission component to stop transmitting the first packet, | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet. |

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| | | In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data.<br><br>Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the |

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| | | normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.d.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b.1) | transmits a preempt indicator indicating that a second packet is to be transmitted, | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"In a first method aspect, the invention provides a method of communicating data over a network comprising transmitting a first data packet, receiving a higher priority data packet, interrupting transmitting the first data packet to transmit the higher priority data packet, and resuming transmission of the first data packet.<br><br>In this way, large blocks of data can be efficiently transmitted, without incurring the overhead associated with splitting them into several smaller packets, but without creating a bottleneck and holding up more urgent data. |

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| | | Preferably interrupting transmission comprises sending a special code to signify interruption. For example, in the case of high speed Ethernet, 10 bit coding is used to carry 8 bit data, and an unused code can be used to flag an interruption.<br><br>Interruptions may be nested and a variety of priority levels may be provided. Preferably, however, only two priority levels are provided, as this reduces the risk of multiple interruptions and possible corruption of a long data packet.<br><br>A count may be kept of the number of interruptions of a lower priority packet, and further interruptions may be denied after a maximum count is reached, or the priority threshold required for interruption may be increased."<br>Banes '029 at 2:9-27.<br><br>"Referring now to Fig. 4, a second embodiment will now be described; this schematic diagram illustrates the order of data transmission when a high priority packet interrupts a lower priority packet. A first, lengthy, data packet is transmitted as a header 100 including a priority flag 101 and an initial data portion 102a. During transmission of the initial data portion 102a, a higher priority packet is received for sending along the same path. The higher priority packet comprises a header portion 120 including a priority flag 121, in this case set to high priority, and a data portion 122. To send this packet without having to wait until the first packet has finished, an interrupt code I 10 is inserted in the data portion 102a, which signals to an appropriately configured receiver that sending of the first packet has been interrupted. The higher priority packet is then sent, followed by a resumption code I 11, followed by the remainder 102b of the data of the first packet.<br><br>Referring to Fig. 5, apparatus for performing the interruption described above will now be described. A network interface 130 is arranged to receive data packets for onward transmission. Received packets pass by priority detector 132 which determines whether interruption is required, by reference to the priority of the packet in transit stored in current priority store 133. In the normal course of events, packets are passed to transmitter 134 in the order received for transmission over a network, here a IGbit/s ethernet 138. However, if the priority detector determines that interruption is required, a signal is sent to interrupt device 136 which inserts an interrupt code, here chosen to be a pre-determined "spare" code from-the 10bit coding scheme |

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| | | used for the Ethernet, buffers the remainder of the packet in transit as necessary, and instructs the transmitter to commence output of the higher priority packet. After the higher priority packet has been sent, a resume code is sent (this may not always be necessary, as the header 120 of the higher priority packet will contain the packet length, but this may simplify reassembly of the fragmented packets and increase fault tolerance), followed by the remainder of the first packet.<br><br>Signaling of interruption is preferably implemented at the physical layer, for example by using an otherwise unused 10 bit code in the case of Ethernet."<br>Banes '029 at 11:18-12:18.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.d.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b.2) | transmits the second packet, and | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b.3) | signals the transmission component to continue transmitting the first packet; | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.g-h.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more |

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| | | references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(c) | wherein packets include in-band symbols and the indicators include one or more out-of-band symbols. | Banes '029 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 22** | | |
| 22 | The communications device of claim 21 wherein the indicators are primitives. | Banes '029 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 16i.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 23** | | |
| 23 | The communications device of claim 21 wherein the in-band symbols are transition optimized and the out-of- | Banes '029 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 17. |

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| | band symbols are not transition optimized. | To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 26** | | |
| 26 | The communications device of claim 21 wherein the first packet includes a header that is transmitted only once. | Banes '029 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 20.<br><br>To the extent that Plaintiff contends that Banes '029 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |

# Exhibit A-3

**Invalidity of the '905 Patent in View of U.S. Patent No. 5,557,608 to Calvignac et. al (Calvignac '608)**

This chart provides examples of where the prior art reference discloses, either expressly or inherently, the claim elements of asserted U.S. Patent No. 7,154,905 ("the '905 patent"). The citations herein are exemplary and are not exhaustive; Defendant has cited the most relevant portions of the identified prior art. For each citation, Defendant hereby incorporates by reference the entire cited prior art reference, and reserves the right to rely on uncited portions of each identified prior art reference. To provide context or identify the state of the art at the time of the alleged invention, Defendant reserves the right to rely on: (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art); (4) factual testimony from the inventors or authors of the prior art references, or purveyors of prior art devices; and (5) expert testimony.

Where Defendant cites a figure, the citation includes any text associated with the figure. Where Defendant cites passages relating to a figure, the citation includes the associated figure any other text associated with that figure. Where Defendant cites particular prior art as disclosing a claim element, that citation equally applies to all identical or similar claim elements in this chart. Defendant reserves the right to further assert that a claim element is inherent, the element would have been obvious to a person of ordinary skill in the art, or the element is disclosed in other prior art that may be combined with the cited prior art. To establish the inherency of certain features of the prior art to invalidate the asserted claims, Defendant may rely on cited or uncited portions of the prior art, other documents, factual testimony, and expert testimony.

This invalidity chart is based on information presently available to Defendant, and the information herein is provided as a non-limiting example.

Calvignac '608 was filed on May 22, 1995, and issued on September 17, 1996; therefore, Calvignac '608 is prior art under at least 35 U.S.C. §102(b) and (e).

# Exhibit A-3

| Claim Limitation | | Calvignac '608 |
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| **Claim 1** | | |
| 1[p] | A method for transmitting packets, the method comprising: | To the extent the preamble is limiting, Calvignac '608 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>"In a packet switched communications system an incoming real-time packet is imbedded after the next block of data of the non-real-time packet being transmitted. This object is accomplished by transmitting each packet along with at least a 1-byte trailer which is used to indicate the packet type, whether the current block of non real time data is preempted or whether the current block of non real time data is resumed."<br>Calvignac '608 at Abstract.<br><br>"It is a principal object of the invention to provide a method and an apparatus for embedding high-priority traffic in low-priority traffic for serial transmission through low speed communication links, without a delay incurred by having first to complete transmission of a low-priority traffic.<br>It is another object of the invention to preempt low-priority packet traffic with at least one high priority packet and later resume transmission of the preempted low-priority packet automatically, using an output adapter built with off-the-shelf scanners.<br>It is another object of the invention to allow a mode of operation that is compatible with the HDLC MAC-layer protocol."<br>Calvignac '608 at 2:25-38.<br><br>"According to the invention an incoming real-time packet is imbedded after the next block of data of the non-real-time packet being transmitted.<br>This object is accomplished by transmitting each packet along with at least a 1-byte trailer which is used to indicate the packet type, whether the current block of non real time data is preempted or whether the current block of non real time data is resumed."<br>Calvignac '608 at 2:42-49. |

**Exhibit A-3**

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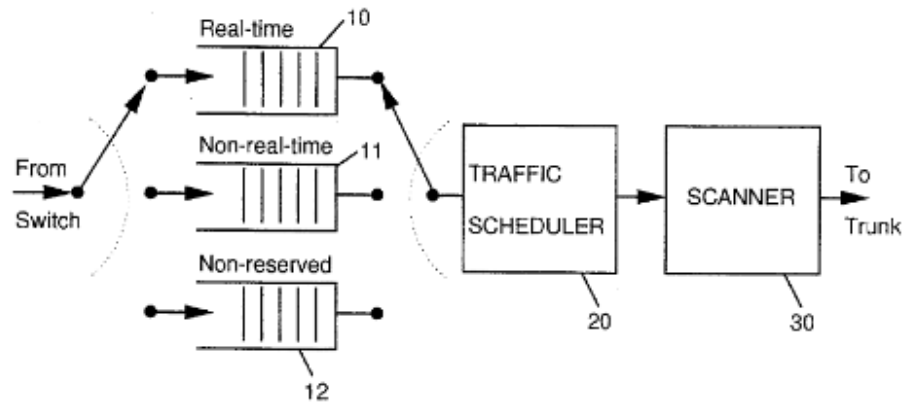
| | |  <br>**Figure 1**<br>Calvignac '608 at Fig. 1. |

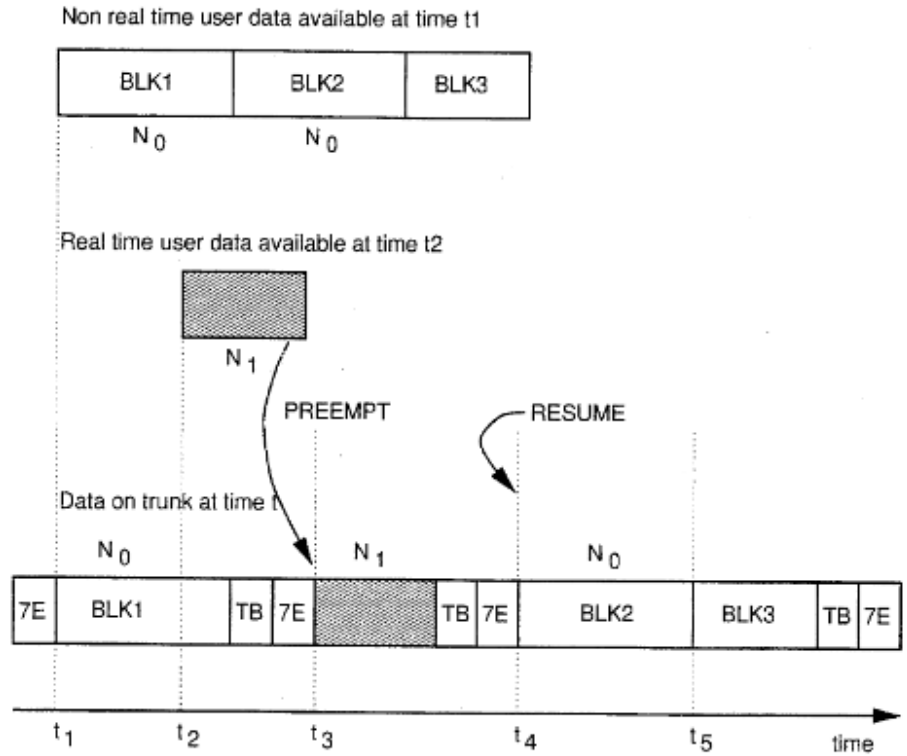



**Figure 2**

Calvignac '608 at Fig. 2.

"FIG. 1 is a block diagram representing the output adapter of a node of a network within which the invention may be practiced.
FIG. 2 represents the principle of the preempt/resume mechanism according to the invention."
Calvignac '608 at 2:56-60.

"A packet-switching network usually consists of switching nodes and communication links or trunks between these nodes. Each of those nodes is linked to at least one other node through one

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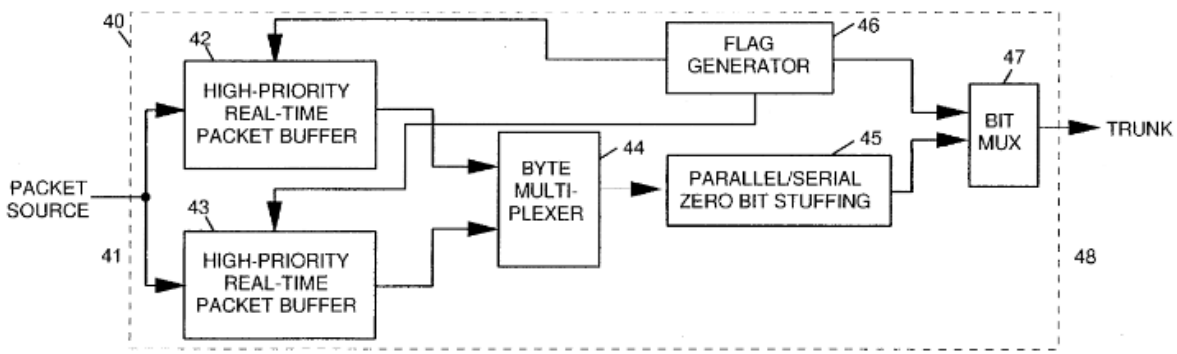
| | | or more communication links. The switching nodes are data processing systems including transmit/receive adapters connected to the communication links. At each node, incoming data packets are selectively routed to one or more of the outgoing communication links terminated at another node. Such routing decisions are made in response to information in the header of the data packet.<br>In a packet switching network, packets are pieces of data, which are prefixed with headers containing control and routing information that identifies the originating and destination users. Each node examines each header and decides where to send the packet to move it closer to its destination."<br>Calvignac '608 at 3:13-27.<br><br>"FIG. 1 represents the output adapter structure, featuring three buffers 10, 11, 12, a scheduler 20, and a scanner 30. Packets received from the switch are stored in one of the buffers, according to their class, and the scheduler implements a policy to forward these packets to the output trunk. The scanner implements the low-level functions of the DLC protocol (frame synchronization, 0 insert/delete, CRC). The scheduler implements the preempt/resume protocol which will be described later."<br>Calvignac '608 at 3:42-50.<br><br>  <br><br>Figure 13<br>Calvignac '608 at Fig. 13. |

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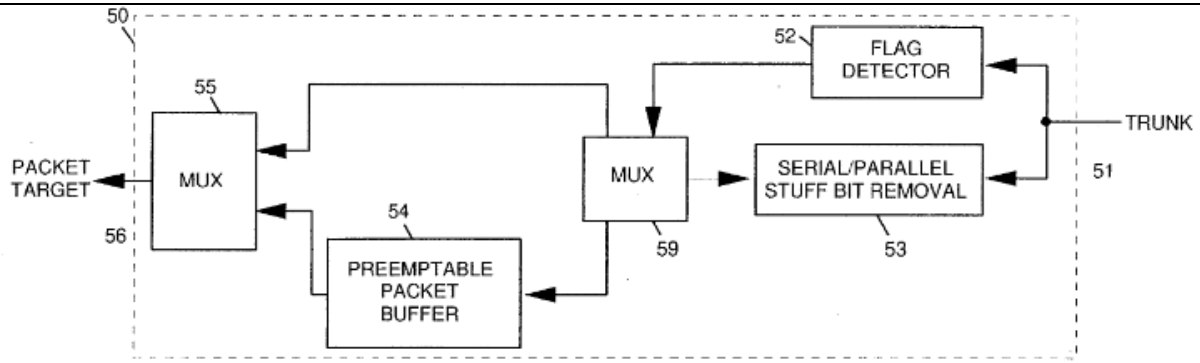
| | |  <br>**Figure 14**<br><br>Calvignac '608 at Fig. 14.<br><br>"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."<br>Calvignac '608 at 4:50-67.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(a) | receiving a first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

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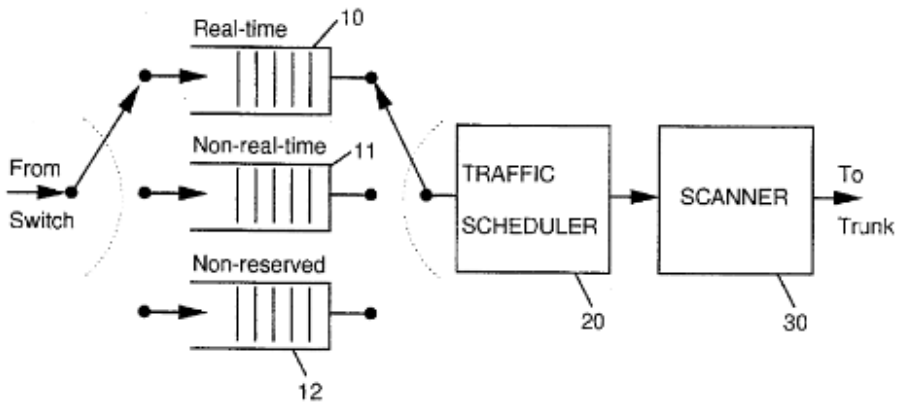
| | | "A packet-switching network usually consists of switching nodes and communication links or trunks between these nodes. Each of those nodes is linked to at least one other node through one or more communication links. The switching nodes are data processing systems including transmit/receive adapters connected to the communication links. At each node, incoming data packets are selectively routed to one or more of the outgoing communication links terminated at another node. Such routing decisions are made in response to information in the header of the data packet.<br>In a packet switching network, packets are pieces of data, which are prefixed with headers containing control and routing information that identifies the originating and destination users. Each node examines each header and decides where to send the packet to move it closer to its destination."<br>Calvignac '608 at 3:13-27.<br>  <br><br>**Figure 1**<br>Calvignac '608 at Fig. 1.<br><br>"FIG. 1 represents the output adapter structure, featuring three buffers 10, 11, 12, a scheduler 20, and a scanner 30. Packets received from the switch are stored in one of the buffers, according to their class, and the scheduler implements a policy to forward these packets to the output trunk. The scanner implements the low-level functions of the DLC protocol (frame synchronization, 0 |

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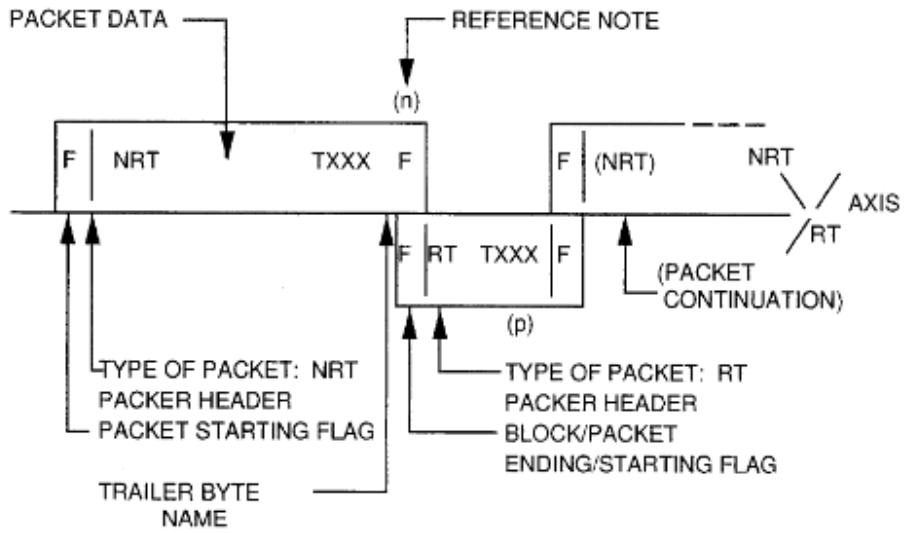
| | | insert/delete, CRC). The scheduler implements the preempt/resume protocol which will be described later."<br>Calvignac '608 at 3:42-50.<br>  <br><br>**Figure 5**<br>Calvignac '608 at Fig. 5. |

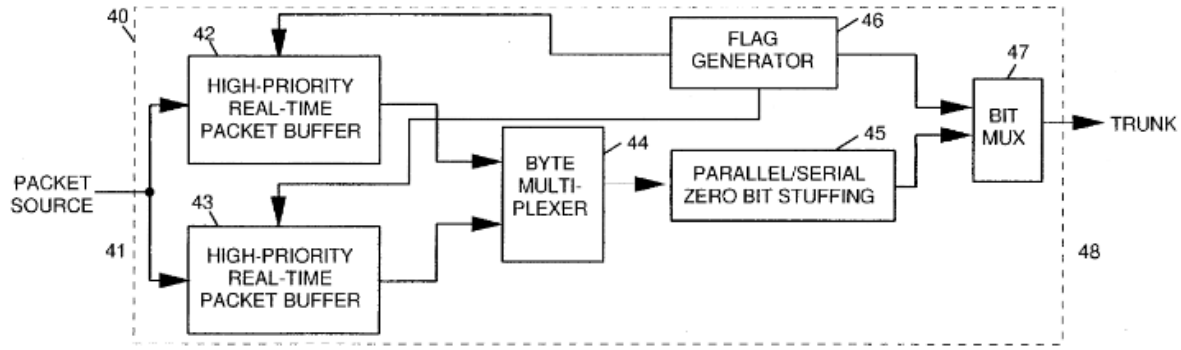



Figure 13

Calvignac '608 at Fig. 13.

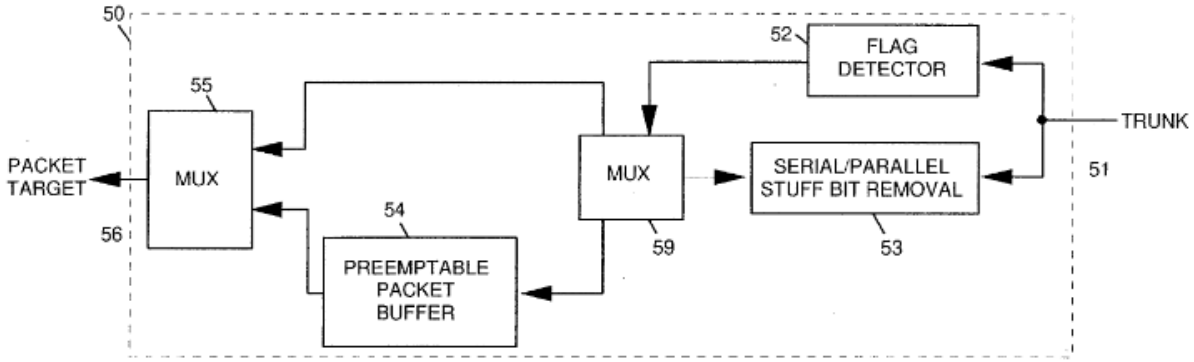



Figure 14

Calvignac '608 at Fig. 14.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt

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| | | flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."<br>Calvignac '608 at 4:50-67.<br><br>"FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits |

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| | | are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag generator 46 sends a trailer byte and an idle flag when the first high-priority packet is completed and transmitter 40 begins transmission of the next high-priority packets without exiting the preempt mode. When the last of the series of high-priority packets has been sent (there are not more packets waiting in the high priority buffer 42), the flag generator 46 sends again a trailer byte and an idle flag. The remaining bytes from the preempted low-priority packet in the low priority buffer 43 are released to the parallel/serial converter 45 and the communication link 48. If a subsequent high-priority packet arrives at the high-priority buffer 42 prior to the completion of the preempted low-priority packet, the preemption and resume sequence is repeated. When the transmission of the low-priority packet is completed, the flag generator 46 transmits an idle flag." Calvignac '608 at 8:41-9:3.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(b) | transmitting a portion of the received first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

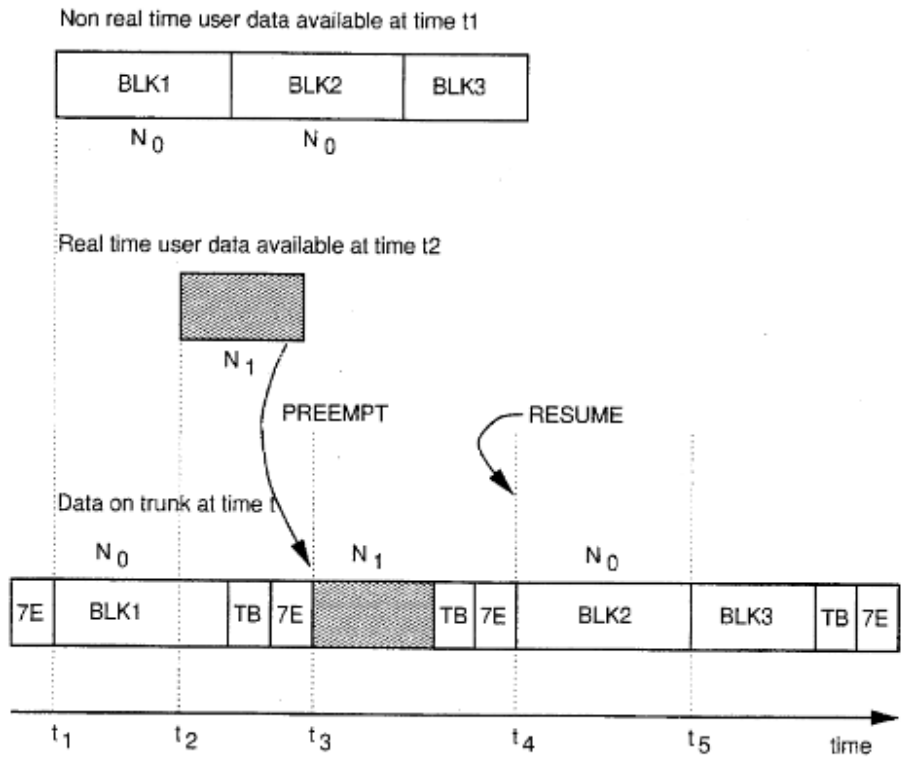


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

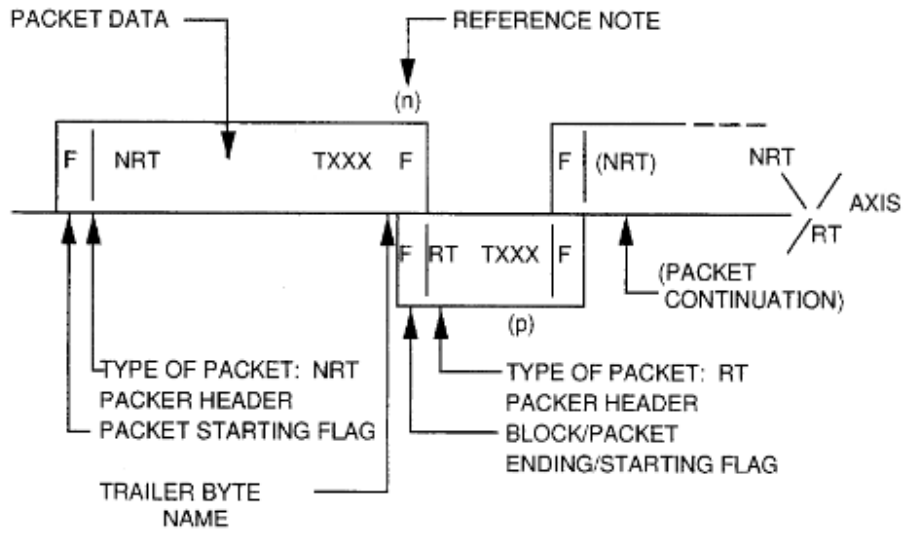


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag |

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| | | generator 46 sends a trailer byte and an idle flag when the first high-priority packet is completed and transmitter 40 begins transmission of the next high-priority packets without exiting the preempt mode. When the last of the series of high-priority packets has been sent (there are not more packets waiting in the high priority buffer 42), the flag generator 46 sends again a trailer byte and an idle flag. The remaining bytes from the preempted low-priority packet in the low priority buffer 43 are released to the parallel/serial converter 45 and the communication link 48. If a subsequent high-priority packet arrives at the high-priority buffer 42 prior to the completion of the preempted low-priority packet, the preemption and resume sequence is repeated. When the transmission of the low-priority packet is completed, the flag generator 46 transmits an idle flag." Calvignac '608 at 8:41-9:3.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(c) | receiving a second packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

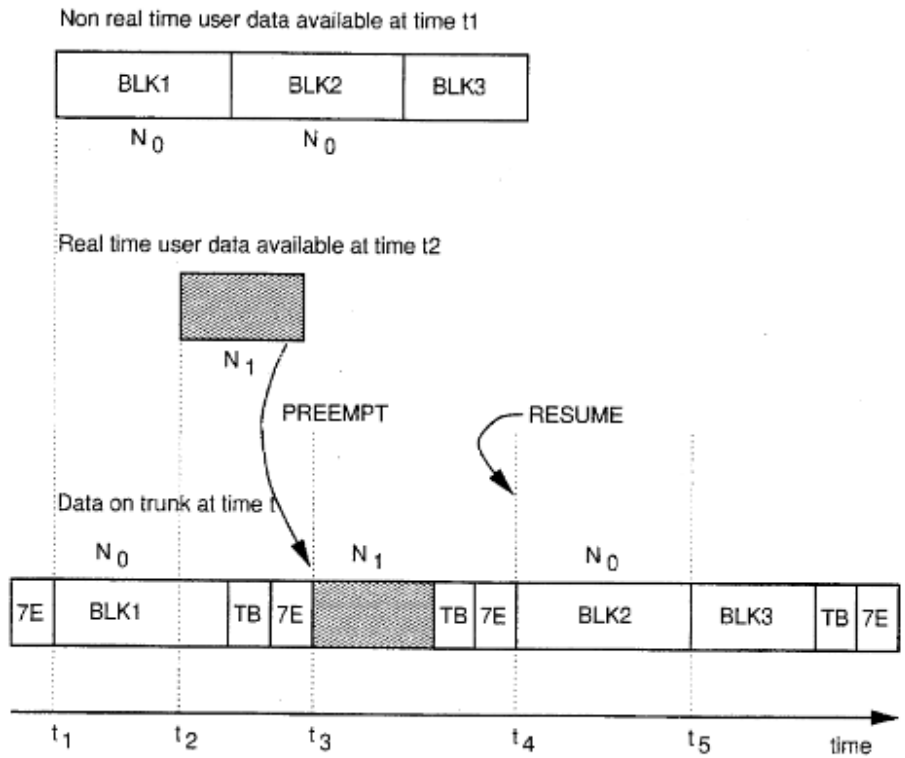


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

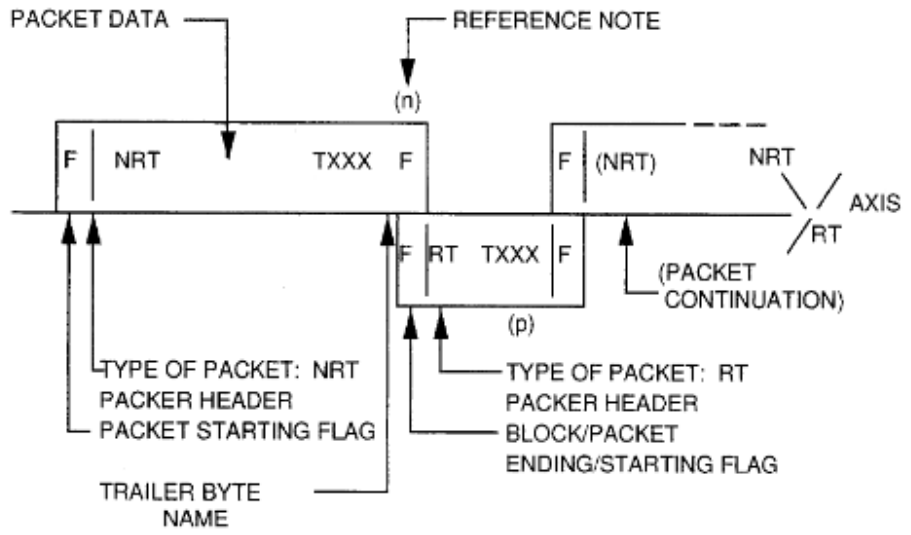


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag |

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| 1(d) | upon receiving the second packet, stopping the transmitting of the first packet so that not all of the first packet has been transmitted; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

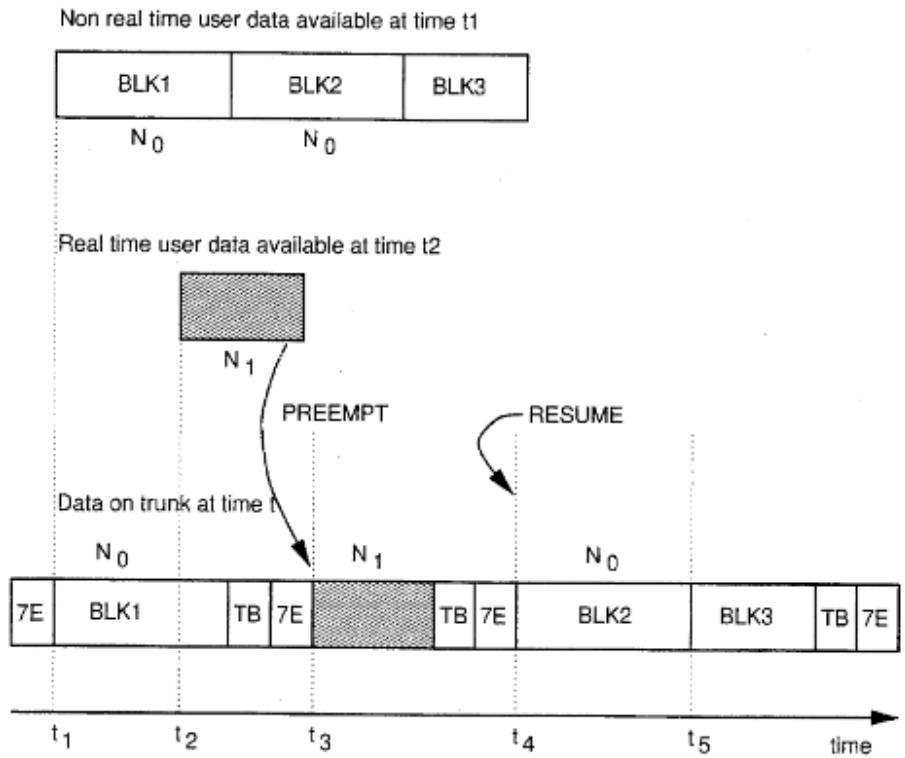


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

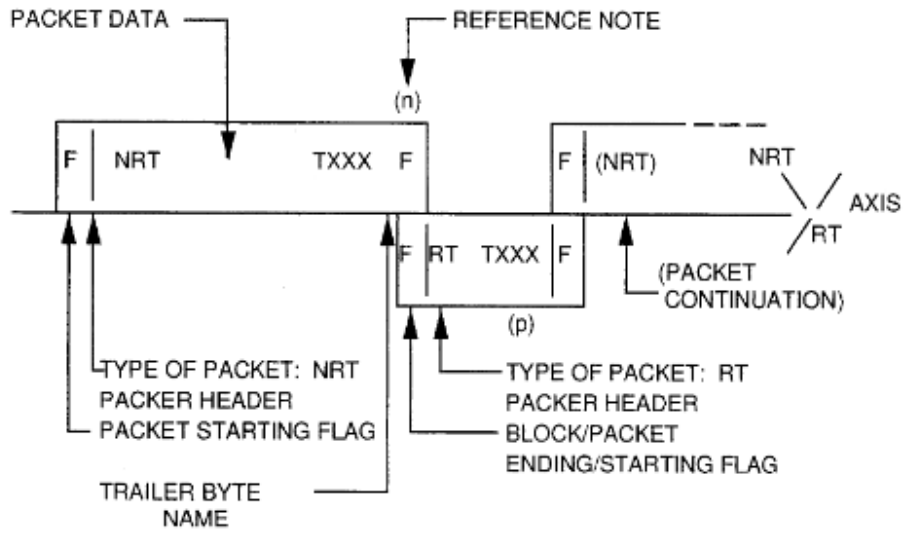


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag |

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| | | generator 46 sends a trailer byte and an idle flag when the first high-priority packet is completed and transmitter 40 begins transmission of the next high-priority packets without exiting the preempt mode. When the last of the series of high-priority packets has been sent (there are not more packets waiting in the high priority buffer 42), the flag generator 46 sends again a trailer byte and an idle flag. The remaining bytes from the preempted low-priority packet in the low priority buffer 43 are released to the parallel/serial converter 45 and the communication link 48. If a subsequent high-priority packet arrives at the high-priority buffer 42 prior to the completion of the preempted low-priority packet, the preemption and resume sequence is repeated. When the transmission of the low-priority packet is completed, the flag generator 46 transmits an idle flag." Calvignac '608 at 8:41-9:3.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(e) | transmitting a preempt indicator; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

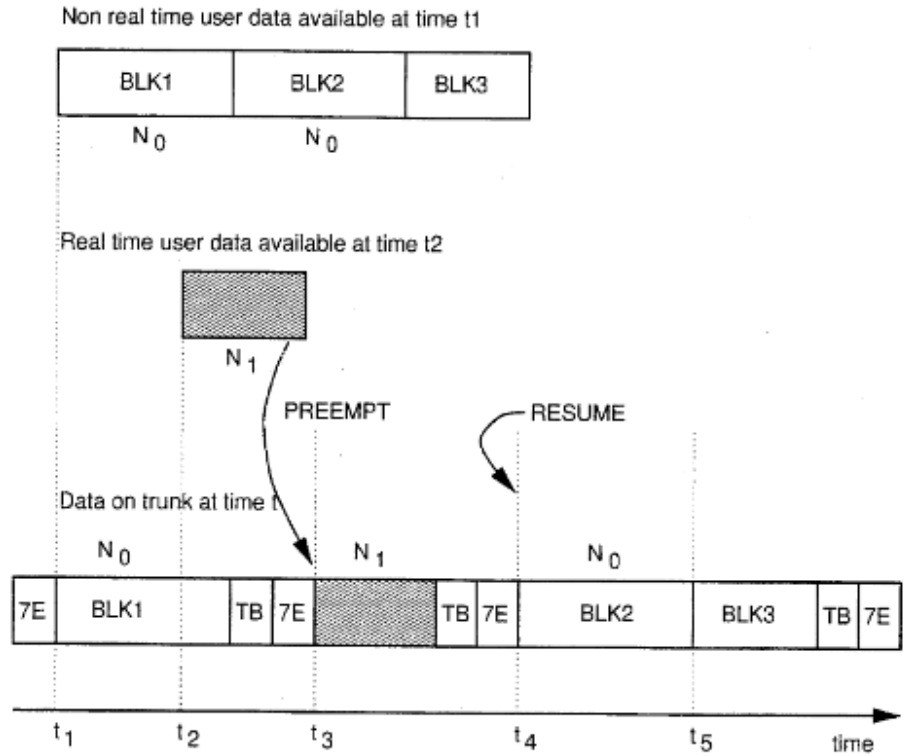


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

"Both the priority with no preemption and the preemption with retransmission service policies can be implemented using the existing HDLC MAC-layer protocol. For preemption with resume service policy, a modified HDLC MAC-layer protocol is described wherein three types of flags are used to delimit packets for allowing high-priority packets to temporarily preempt low-priority

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| | | packets. The HDLC starting, ending or idle flag is defined as the 8-bit sequence B`01111110`(X`7E`). The start preempt flag is defined as the 9-bit sequence B`011111110`and the end-preempt flag is defined as the 10-bit sequence B`0111111110`. All flags are on byte boundaries with respect to the packet data that they delineate."<br>Calvignac '608 at 2:3-15.<br><br>"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."<br>Calvignac '608 at 4:50-67.<br><br>"A flag detector 52 continuously monitors the bit stream received from a communication link 51 trailer byte and idle flags. If a sequence of bits other than a flag is detected immediately following an idle flag, it indicates the beginning of a new frame. A serial/parallel converter 53 receives the bit stream, discards any `0` bit if it immediately follows five consecutive `1` bits, and converts the remaining bits into byte-parallel form. If the received packet is a high-priority , packet, the parallel byte data is passed directly through a multiplexer 59 to a multiplexer 55 connected to the packet target 56 until a normal ending flag is detected by the flag detector 52. The receiver 50 indicates the end of the packet to the packet target 56. If the received packet can be preempted (i.e. low-priority, non-real-time packet), then the parallel byte data is instead passed through byte multiplexer 59 to the preemptable packet buffer 54 in order to permit the entire packet to be accumulated before passing it to the packet target 56. If flag detector 52 detects a trailer byte that there is no partial byte in the serial parallel converter 53, then it indicates the beginning of a high-priority preempting packet and therefore the beginning of preempt mode. The bit stream is passed through the serial/parallel converter 53 as before but this time the parallel byte data is passed |

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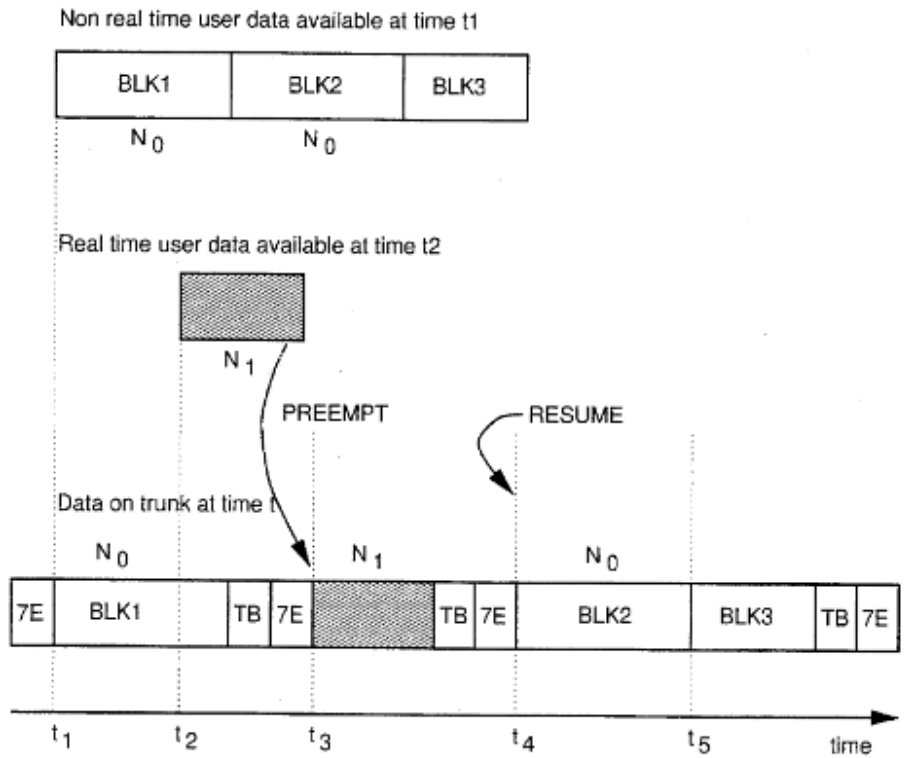
| | | directly through the multiplexers 59 and 55 to the packet target 56 within the communications system.<br>When the flag detector 52 detects either a normal ending flag or a trailer byte indicating the end of preemption, then the receiver 50 indicates the end of the packet to the packet target 56. If a normal ending flag is detected, then the serial/parallel converter 53 will continue to route the parallel byte data from subsequent packets directly to the multiplexer 55. If a trailer byte indicating the end of preemption is detected, the receiver 50 will end preempt mode. The received bit stream will be routed through the serial parallel converter 53 and multiplexer 59 to the preemptable packet buffer 54 thus resuming reception of the preempted low-priority packet. If the flag detector 52 detects a normal ending flag indicating the end of the low-priority packet, the receiver 50 transfers the entire low-priority packet stored in the preemptable packet buffer 54 through the multiplexer 55 to the packet target 56."<br>Calvignac '608 at 9:13-38.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(f) | transmitting the second packet; and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

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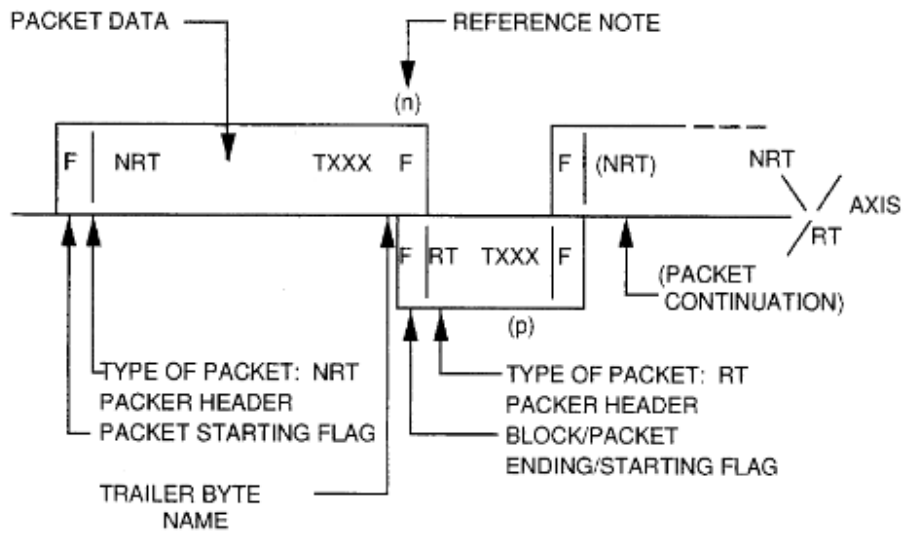


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag |

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| | | generator 46 sends a trailer byte and an idle flag when the first high-priority packet is completed and transmitter 40 begins transmission of the next high-priority packets without exiting the preempt mode. When the last of the series of high-priority packets has been sent (there are not more packets waiting in the high priority buffer 42), the flag generator 46 sends again a trailer byte and an idle flag. The remaining bytes from the preempted low-priority packet in the low priority buffer 43 are released to the parallel/serial converter 45 and the communication link 48. If a subsequent high-priority packet arrives at the high-priority buffer 42 prior to the completion of the preempted low-priority packet, the preemption and resume sequence is repeated. When the transmission of the low-priority packet is completed, the flag generator 46 transmits an idle flag." Calvignac '608 at 8:41-9:3.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(g) | upon completion of transmitting the second packet, transmitting a continue indicator; and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

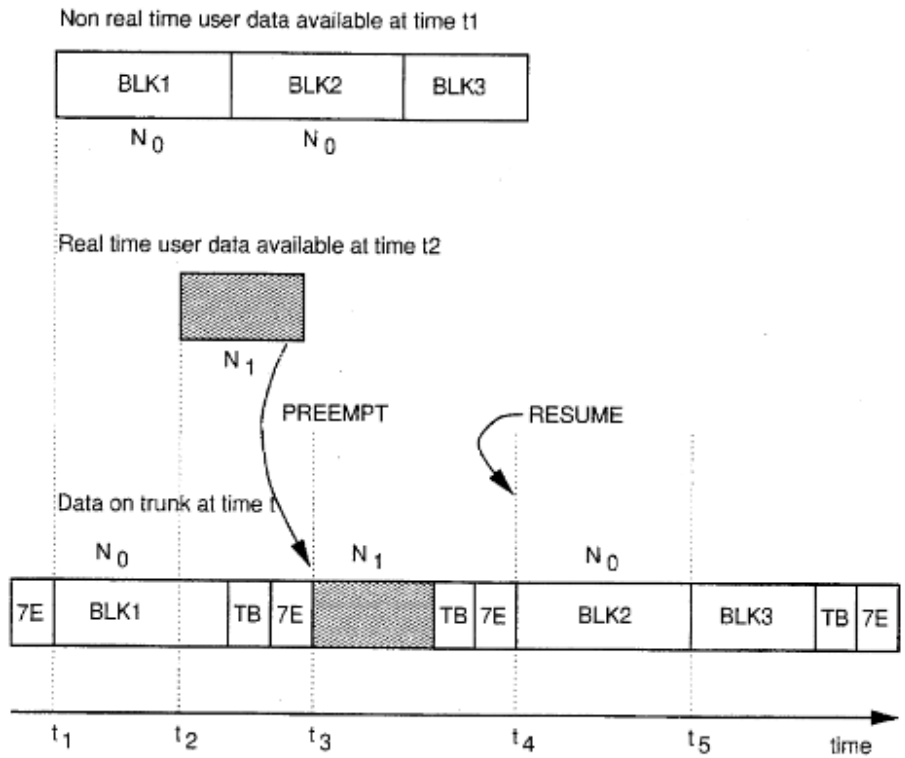


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

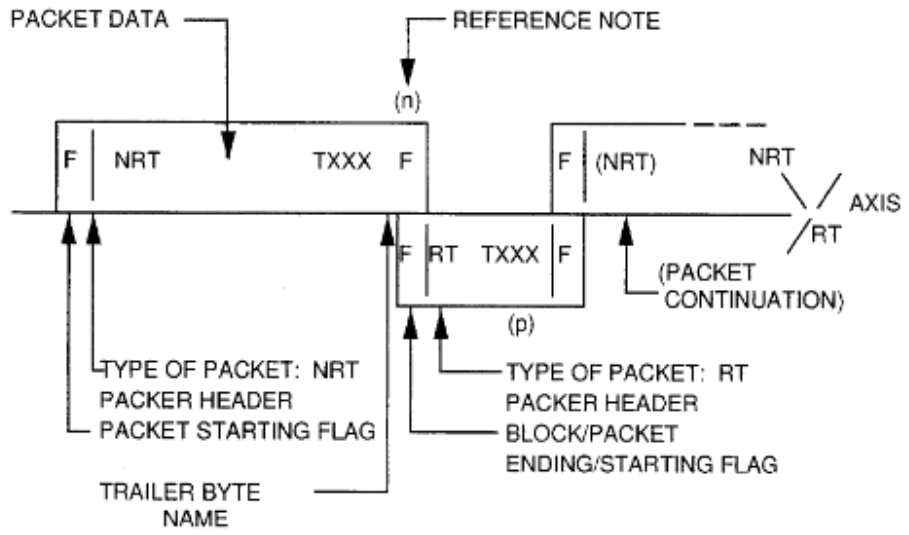


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "Both the priority with no preemption and the preemption with retransmission service policies can be implemented using the existing HDLC MAC-layer protocol. For preemption with resume service policy, a modified HDLC MAC-layer protocol is described wherein three types of flags are used to delimit packets for allowing high-priority packets to temporarily preempt low-priority packets. The HDLC starting, ending or idle flag is defined as the 8-bit sequence B`01111110`(X`7E`). The start preempt flag is defined as the 9-bit sequence B`011111110`and the end-preempt flag is defined as the 10-bit sequence B`0111111110`. All flags are on byte boundaries with respect to the packet data that they delineate."<br>Calvignac '608 at 2:3-15.<br><br>"A flag detector 52 continuously monitors the bit stream received from a communication link 51 trailer byte and idle flags. If a sequence of bits other than a flag is detected immediately following an idle flag, it indicates the beginning of a new frame. A serial/parallel converter 53 receives the bit stream, discards any `0` bit if it immediately follows five consecutive `1` bits, and converts the remaining bits into byte-parallel form. If the received packet is a high-priority , packet, the parallel byte data is passed directly through a multiplexer 59 to a multiplexer 55 connected to the packet target 56 until a normal ending flag is detected by the flag detector 52. The receiver 50 indicates the end of the packet to the packet target 56. If the received packet can be preempted (i.e. low-priority, non-real-time packet), then the parallel byte data is instead passed through byte multiplexer 59 to the preemptable packet buffer 54 in order to permit the entire packet to be accumulated before passing it to the packet target 56. If flag detector 52 detects a trailer byte that there is no partial byte in the serial parallel converter 53, then it indicates the beginning of a high-priority preempting packet and therefore the beginning of preempt mode. The bit stream is passed through the serial/parallel converter 53 as before but this time the parallel byte data is passed directly through the multiplexers 59 and 55 to the packet target 56 within the communications system.<br>When the flag detector 52 detects either a normal ending flag or a trailer byte indicating the end of preemption, then the receiver 50 indicates the end of the packet to the packet target 56. If a normal ending flag is detected, then the serial/parallel converter 53 will continue to route the parallel byte data from subsequent packets directly to the multiplexer 55. If a trailer byte indicating the end of preemption is detected, the receiver 50 will end preempt mode. The received bit stream will be routed through the serial parallel converter 53 and multiplexer 59 to the preemptable packet buffer 54 thus resuming reception of the preempted low-priority packet. If |

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| | | the flag detector 52 detects a normal ending flag indicating the end of the low-priority packet, the receiver 50 transfers the entire low-priority packet stored in the preemptable packet buffer 54 through the multiplexer 55 to the packet target 56."<br>Calvignac '608 at 9:13-38.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(h) | transmitting the portion of the first packet that has not yet been transmitted; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

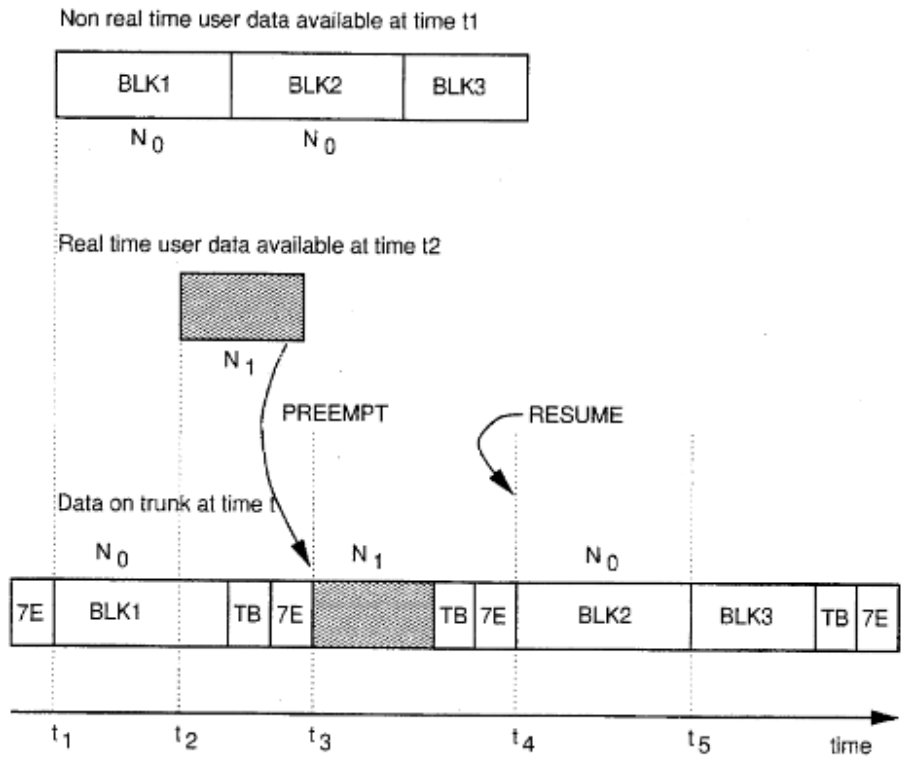


**Figure 2**

Calvignac '608 at Fig. 2.

FIG. 2 represents the principle of the preempt/resume mechanism according to the invention." Calvignac '608 at 2:58-60.

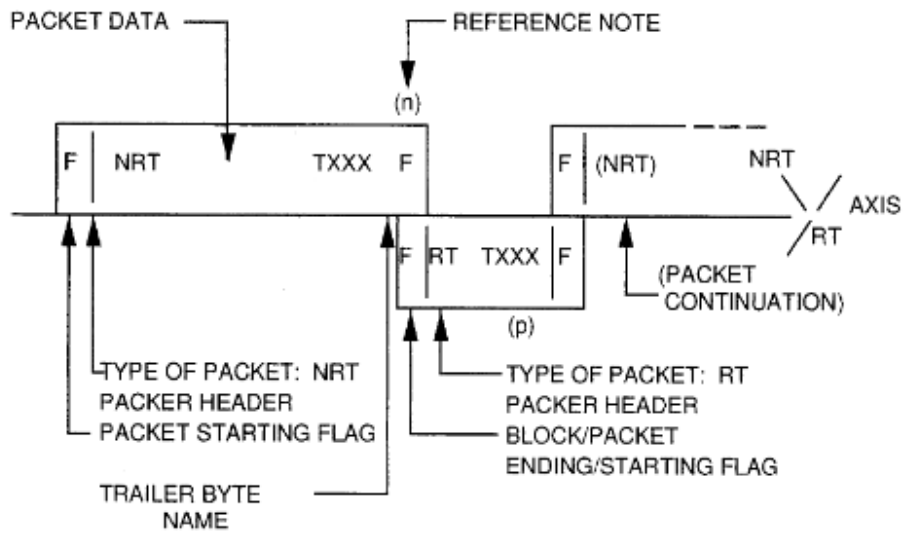


**Figure 5**

Calvignac '608 at Fig. 5.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

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| | | "FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"When a low-priority packet arrives in the low priority buffer 43 and a packet is currently being transmitted, the transmitter 40 waits until all earlier packets in the low priority buffer 43 have been transmitted and the high priority buffer 42 is empty. When a low-priority packet is at the head of the low priority buffer 43 and no other packet is being transmitted on the communication link 48, bytes from the low priority buffer 43 are transferred one at a time through a byte multiplexer 44 to a parallel/serial converter 45. The parallel/serial converter 45 serializes the data and monitors the outgoing data for sequences of five consecutive `1` bits. It also inserts a single `0` bit immediately after each set of five `1` bits. The resulting bit stream is routed through the bit multiplexer 47 the communication link 48. When the transmission of the low-priority packet is complete, the bit multiplexer 47 selects the flag generator 46 for transmission of one or more normal flags until the next packet is ready to be transmitted. Note that each time a flag is sent, the parallel/serial converter 45 resets its internal count of the number of consecutive `1` bits."<br>Calvignac '608 at 8:21-40.<br><br>"If a low-priority packet is being transmitted from low priority buffer 43 and a high-priority packet arrives in the high priority buffer 42, then the transmission of the low-priority packet is preempted. The remaining bits in the parallel serial converter 45 along with any stuffed zero bits are transmitted guaranteeing a block boundary for the preempted packet. Then the flag generator 46 sends a trailer byte, as described earlier and an idle flag X`7E`. Bytes from the high priority buffer 42 are then transferred through the byte multiplexer 44 to the parallel/serial converter 45 which performs serialization and zero bit stuffing. The resulting high-priority packet is then transferred to the communication link 48. If, during the transmission of the high-priority packet, another high-priority packet arrives in the high-priority buffer 42, then the flag |

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| | | generator 46 sends a trailer byte and an idle flag when the first high-priority packet is completed and transmitter 40 begins transmission of the next high-priority packets without exiting the preempt mode. When the last of the series of high-priority packets has been sent (there are not more packets waiting in the high priority buffer 42), the flag generator 46 sends again a trailer byte and an idle flag. The remaining bytes from the preempted low-priority packet in the low priority buffer 43 are released to the parallel/serial converter 45 and the communication link 48. If a subsequent high-priority packet arrives at the high-priority buffer 42 prior to the completion of the preempted low-priority packet, the preemption and resume sequence is repeated. When the transmission of the low-priority packet is completed, the flag generator 46 transmits an idle flag." Calvignac '608 at 8:41-9:3.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 1(i) | wherein the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"Both the priority with no preemption and the preemption with retransmission service policies can be implemented using the existing HDLC MAC-layer protocol. For preemption with resume service policy, a modified HDLC MAC-layer protocol is described wherein three types of flags are used to delimit packets for allowing high-priority packets to temporarily preempt low-priority packets. The HDLC starting, ending or idle flag is defined as the 8-bit sequence B`01111110`(X`7E`). The start preempt flag is defined as the 9-bit sequence B`011111110`and |

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| | | the end-preempt flag is defined as the 10-bit sequence B`0111111110`. All flags are on byte boundaries with respect to the packet data that they delineate."<br>Calvignac '608 at 2:3-15.<br><br>"In the system described in the prior art, the preempt/resume protocol uses a couple of special flags:<br>`011111110`: Starting preempt flag<br>`0111111110`: Ending preempt flag<br>Both flags are byte aligned."<br>Calvignac '608 at 4:44-49.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 8** | | |
| 8[p] | A method for receiving packets, the method comprising: | To the extent the preamble is limiting, Calvignac '608 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>"In a packet switched communications system an incoming real-time packet is imbedded after the next block of data of the non-real-time packet being transmitted. This object is accomplished by transmitting each packet along with at least a 1-byte trailer which is used to indicate the packet type, whether the current block of non real time data is preempted or whether the current block of non real time data is resumed."<br>Calvignac '608 at Abstract.<br><br>"It is a principal object of the invention to provide a method and an apparatus for embedding high-priority traffic in low-priority traffic for serial transmission through low speed communication links, without a delay incurred by having first to complete transmission of a low-priority traffic. |

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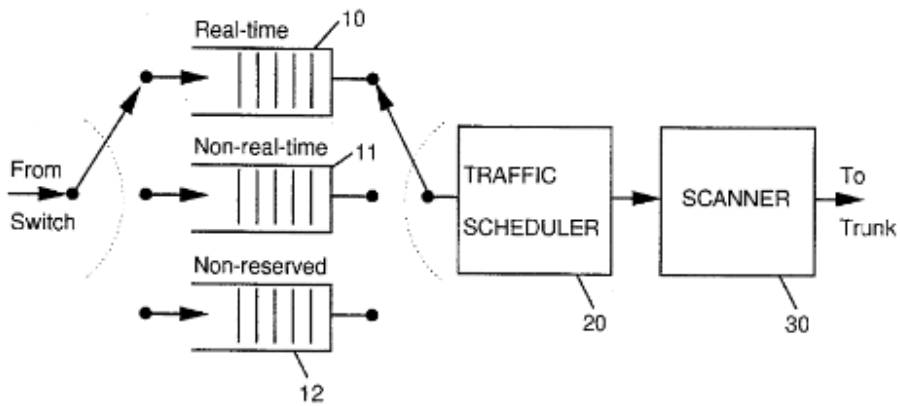
| | | It is another object of the invention to preempt low-priority packet traffic with at least one high priority packet and later resume transmission of the preempted low-priority packet automatically, using an output adapter built with off-the-shelf scanners.<br>It is another object of the invention to allow a mode of operation that is compatible with the HDLC MAC-layer protocol."<br>Calvignac '608 at 2:25-38.<br><br>"According to the invention an incoming real-time packet is imbedded after the next block of data of the non-real-time packet being transmitted.<br>This object is accomplished by transmitting each packet along with at least a 1-byte trailer which is used to indicate the packet type, whether the current block of non real time data is preempted or whether the current block of non real time data is resumed."<br>Calvignac '608 at 2:42-49.<br><br>  <br><br>**Figure 1**<br>Calvignac '608 at Fig. 1. |

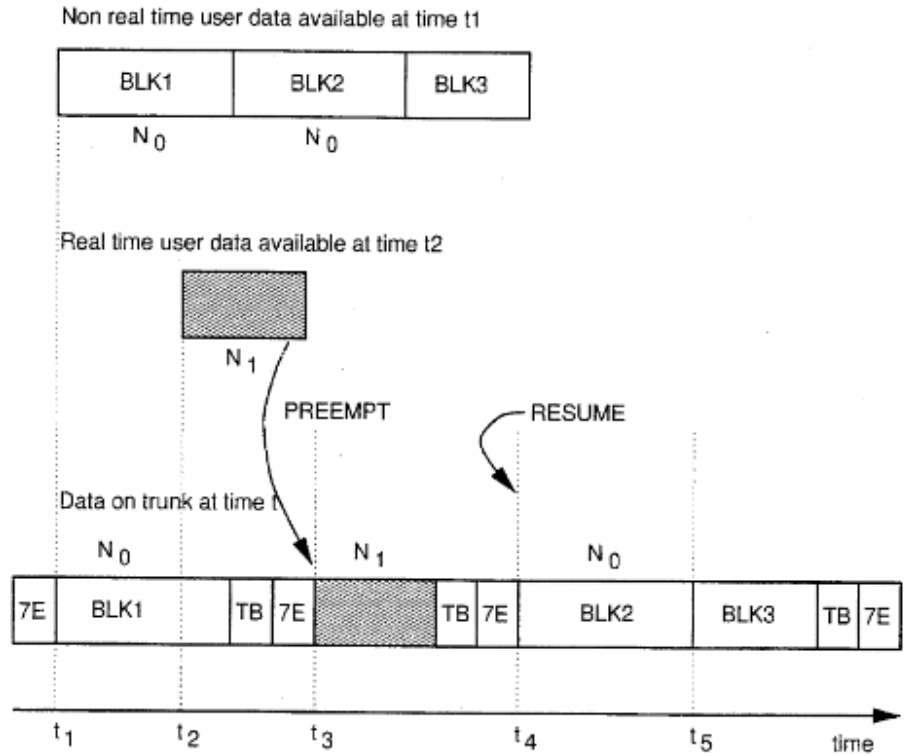



**Figure 2**

Calvignac '608 at Fig. 2.

"FIG. 1 is a block diagram representing the output adapter of a node of a network within which the invention may be practiced.
FIG. 2 represents the principle of the preempt/resume mechanism according to the invention."
Calvignac '608 at 2:56-60.

"A packet-switching network usually consists of switching nodes and communication links or trunks between these nodes. Each of those nodes is linked to at least one other node through one

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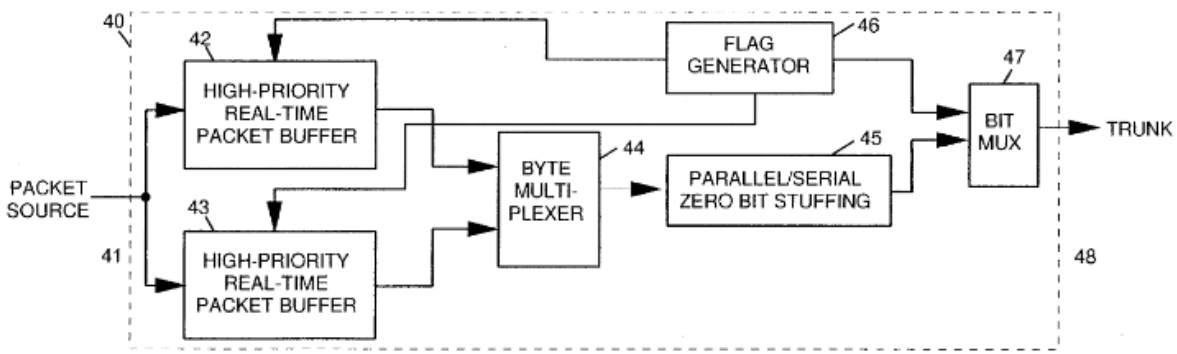
| | | or more communication links. The switching nodes are data processing systems including transmit/receive adapters connected to the communication links. At each node, incoming data packets are selectively routed to one or more of the outgoing communication links terminated at another node. Such routing decisions are made in response to information in the header of the data packet.<br>In a packet switching network, packets are pieces of data, which are prefixed with headers containing control and routing information that identifies the originating and destination users. Each node examines each header and decides where to send the packet to move it closer to its destination."<br>Calvignac '608 at 3:13-27.<br><br>"FIG. 1 represents the output adapter structure, featuring three buffers 10, 11, 12, a scheduler 20, and a scanner 30. Packets received from the switch are stored in one of the buffers, according to their class, and the scheduler implements a policy to forward these packets to the output trunk. The scanner implements the low-level functions of the DLC protocol (frame synchronization, 0 insert/delete, CRC). The scheduler implements the preempt/resume protocol which will be described later."<br>Calvignac '608 at 3:42-50.<br><br>  <br><br>Figure 13<br>Calvignac '608 at Fig. 13. |

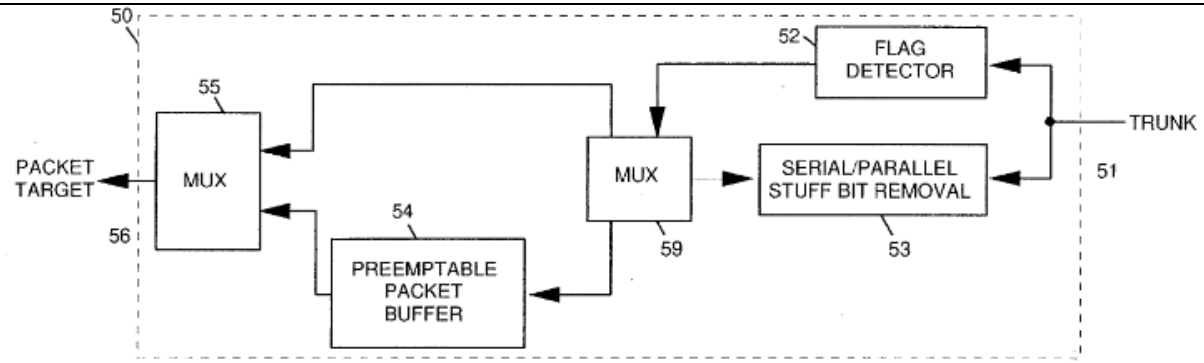



**Figure 14**

Calvignac '608 at Fig. 14.

"Let's assume that a non-real-time packet is ready to be transmitted at time t1, and that no real-time packet is ready to be transmitted. Then, the transmission of the non-real-time packet can begin at time t1. Now assume that a real-time packet arrives at the output trunk at time t2 before the end of the transmission of the non-real-time packet. The packets are sent from the queue to the trunk adapter on a byte basis, and a real-time packet can be inserted after any byte of a non-real-time packet, provided it is encapsulated between a starting preempt flag (SP) and an ending preempt flag (EP). During the reception of the packet, the receiver looks for the starting preempt flag. Upon detection of this flag, it checks the validity of the detection, and eventually starts receiving the real-time packet that has been imbedded within the non-real-time packet. It also continues looking at the received bits, detects the ending preempt flag, then checks the validity and resumes the reception of the non-real-time packet."
Calvignac '608 at 4:50-67.

*See also* exemplary disclosures and corresponding discussion for Claim 1[pre].

To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

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| 8(a) | receiving a first portion of symbols of a first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.a.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(b) | receiving a preempt indicator indicating that a second packet of symbols is to be received; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.e.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(c) | receiving the second packet of symbols; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(d) | receiving a continue indicator indicating that a second portion of | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*: |

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| | symbols of the first packet is to be received; and | *See* exemplary disclosures and corresponding discussion for Claim 1.g.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(e) | receiving the second portion of symbols of the first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.h.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 8(f) | wherein the symbols of the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 12** | | |
| 12 | The method of claim 8 wherein the first and second packets are received via the same communications link. | Calvignac '608 discloses, expressly or inherently, the method of claim 8 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 8.<br><br>"A packet-switching network usually consists of switching nodes and communication links or trunks between these nodes. Each of those nodes is linked to at least one other node through one |

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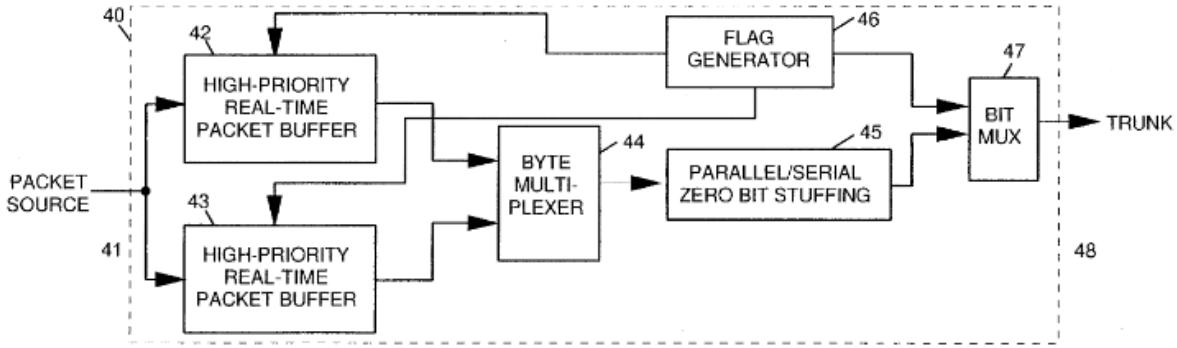
| | | or more communication links. The switching nodes are data processing systems including transmit/receive adapters connected to the communication links. At each node, incoming data packets are selectively routed to one or more of the outgoing communication links terminated at another node. Such routing decisions are made in response to information in the header of the data packet.<br>In a packet switching network, packets are pieces of data, which are prefixed with headers containing control and routing information that identifies the originating and destination users. Each node examines each header and decides where to send the packet to move it closer to its destination."<br>Calvignac '608 at 3:13-27.<br>  <br><br>**Figure 13**<br>Calvignac '608 at Fig. 13. |

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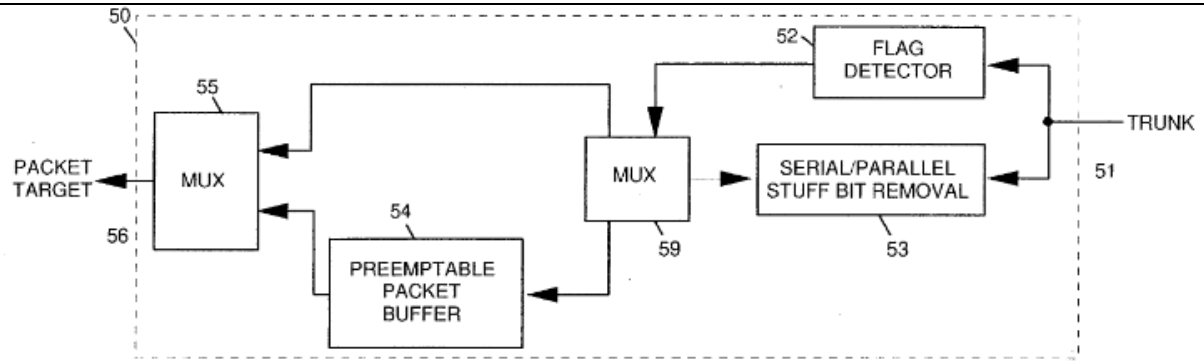
| | |  <br>**Figure 14**<br><br>Calvignac '608 at Fig. 14.<br><br>"FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 15** | | |
| 15[p] | A method for transmitting packets via a | To the extent the preamble is limiting, Calvignac '608 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*: |

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| | communications link, the method comprising: | *See* exemplary disclosures and corresponding discussion for Claim 1[pre].<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(a) | transmitting a first portion of a first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.b.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(b) | transmitting a preempt indicator indicating that a second packet is to be transmitted; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.e.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(c) | transmitting the second packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f. |

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| | | To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(d) | transmitting a continue indicator indicating that a second portion of the first packet is to be transmitted; and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.g.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(e) | transmitting the second portion of the first packet | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.h.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 15(f) | wherein the first and second packets and the preempt and continue indicators are transmitted via the same communications link and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 12.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |

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| 15(f.1) | wherein further the packets include in-band symbols and the indicators include one or more out-of-band symbols. | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 16** | | |
| 16 | The method of claim 15 wherein the indicators arrives. | Calvignac '608 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15.<br><br>"Both the priority with no preemption and the preemption with retransmission service policies can be implemented using the existing HDLC MAC-layer protocol. For preemption with resume service policy, a modified HDLC MAC-layer protocol is described wherein three types of flags are used to delimit packets for allowing high-priority packets to temporarily preempt low-priority packets. The HDLC starting, ending or idle flag is defined as the 8-bit sequence B`01111110`(X`7E`). The start preempt flag is defined as the 9-bit sequence B`011111110`and the end-preempt flag is defined as the 10-bit sequence B`0111111110`. All flags are on byte boundaries with respect to the packet data that they delineate."<br>Calvignac '608 at 2:3-15.<br><br>"In the system described in the prior art, the preempt/resume protocol uses a couple of special flags:<br>`011111110`: Starting preempt flag<br>`0111111110`: Ending preempt flag<br>Both flags are byte aligned."<br>Calvignac '608 at 4:44-49. |

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| | | To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| | | **Claim 17** |
| 17 | The method of claim 15 wherein the in-band symbols are transition optimized and the out-of-band symbols are not transition optimized. | Calvignac '608 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15.<br><br>"Both the priority with no preemption and the preemption with retransmission service policies can be implemented using the existing HDLC MAC-layer protocol. For preemption with resume service policy, a modified HDLC MAC-layer protocol is described wherein three types of flags are used to delimit packets for allowing high-priority packets to temporarily preempt low-priority packets. The HDLC starting, ending or idle flag is defined as the 8-bit sequence B`01111110`(X`7E`). The start preempt flag is defined as the 9-bit sequence B`011111110`and the end-preempt flag is defined as the 10-bit sequence B`0111111110`. All flags are on byte boundaries with respect to the packet data that they delineate."<br>Calvignac '608 at 2:3-15.<br><br>"In the system described in the prior art, the preempt/resume protocol uses a couple of special flags:<br>`011111110`: Starting preempt flag<br>`0111111110`: Ending preempt flag<br>Both flags are byte aligned."<br>Calvignac '608 at 4:44-49.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |

## Exhibit A-3

| Claim 20 | | |
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| 20 | The method of claim 15 wherein the first packet includes a header that is transmitted only once. | Calvignac '608 discloses, expressly or inherently, the method of claim 15 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for claim 15.<br><br>"A packet-switching network usually consists of switching nodes and communication links or trunks between these nodes. Each of those nodes is linked to at least one other node through one or more communication links. The switching nodes are data processing systems including transmit/receive adapters connected to the communication links. At each node, incoming data packets are selectively routed to one or more of the outgoing communication links terminated at another node. Such routing decisions are made in response to information in the header of the data packet.<br>In a packet switching network, packets are pieces of data, which are prefixed with headers containing control and routing information that identifies the originating and destination users. Each node examines each header and decides where to send the packet to move it closer to its destination."<br>Calvignac '608 at 3:13-27. |

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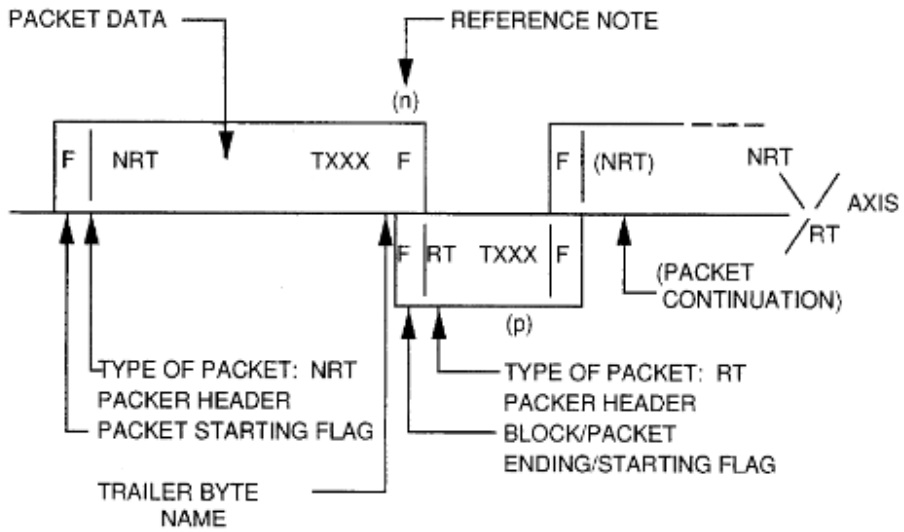
| | |  <br>**Figure 5**<br>Calvignac '608 at Fig. 5.<br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 21** | | |
| 21[p] | A communications device for transmitting packets via a communications link, comprising: | To the extent the preamble is limiting, Calvignac '608 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*:<br><br>"In a packet switched communications system an incoming real-time packet is imbedded after the next block of data of the non-real-time packet being transmitted. This object is accomplished by transmitting each packet along with at least a 1-byte trailer which is used to indicate the packet |

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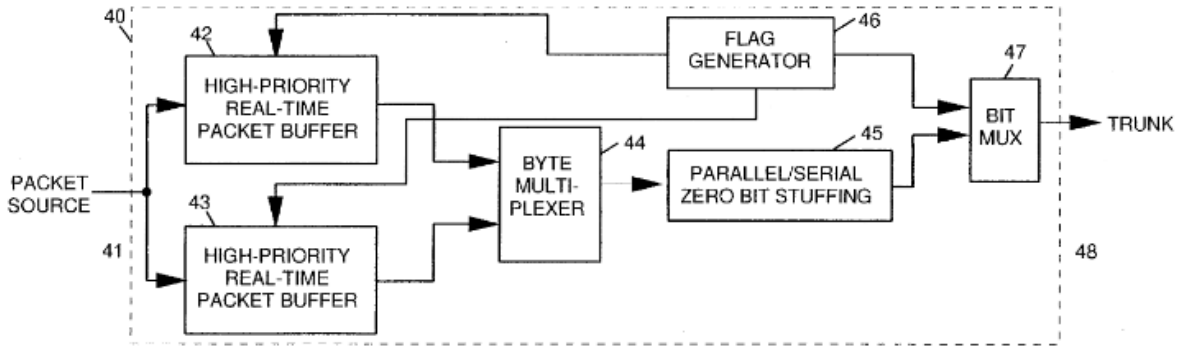
| | | type, whether the current block of non real time data is preempted or whether the current block of non real time data is resumed."<br>Calvignac '608 at Abstract.<br><br>"It is a principal object of the invention to provide a method and an apparatus for embedding high-priority traffic in low-priority traffic for serial transmission through low speed communication links, without a delay incurred by having first to complete transmission of a low-priority traffic.<br>It is another object of the invention to preempt low-priority packet traffic with at least one high priority packet and later resume transmission of the preempted low-priority packet automatically, using an output adapter built with off-the-shelf scanners.<br>It is another object of the invention to allow a mode of operation that is compatible with the HDLC MAC-layer protocol."<br>Calvignac '608 at 2:25-38.<br><br>  <br><br>Figure 13<br><br>Calvignac '608 at Fig. 13. |

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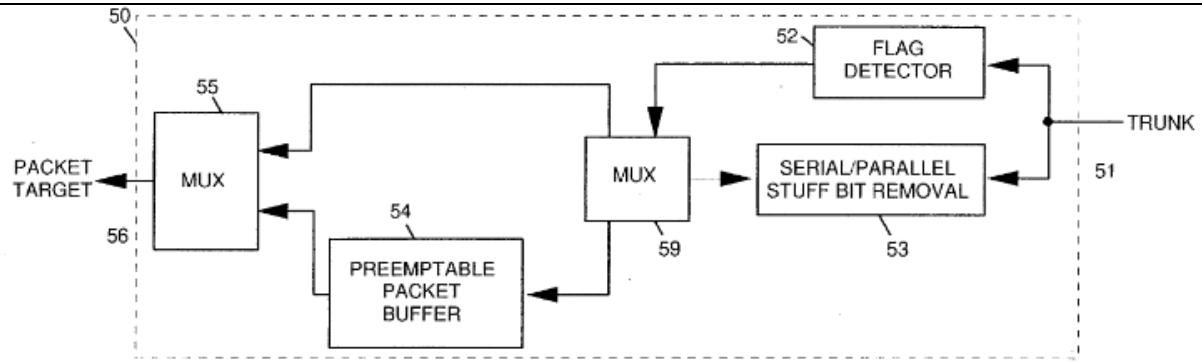
| | |  <br>**Figure 14**<br><br>Calvignac '608 at Fig. 14.<br><br>"FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1[pre]. |

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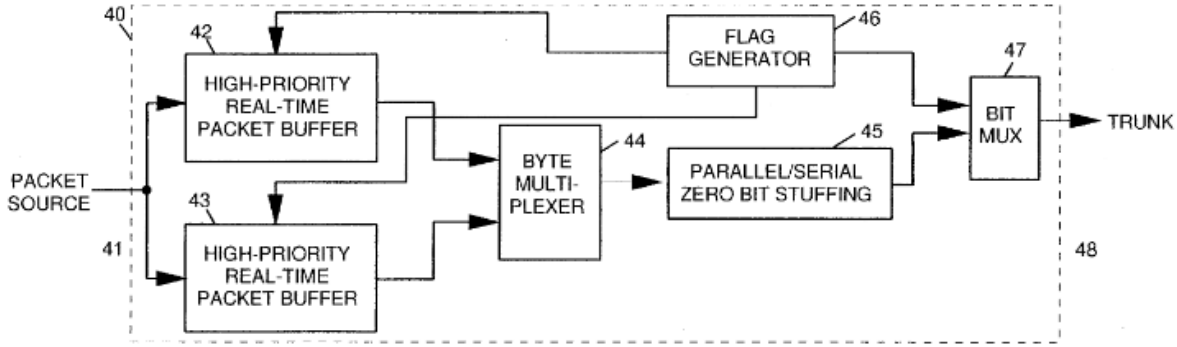
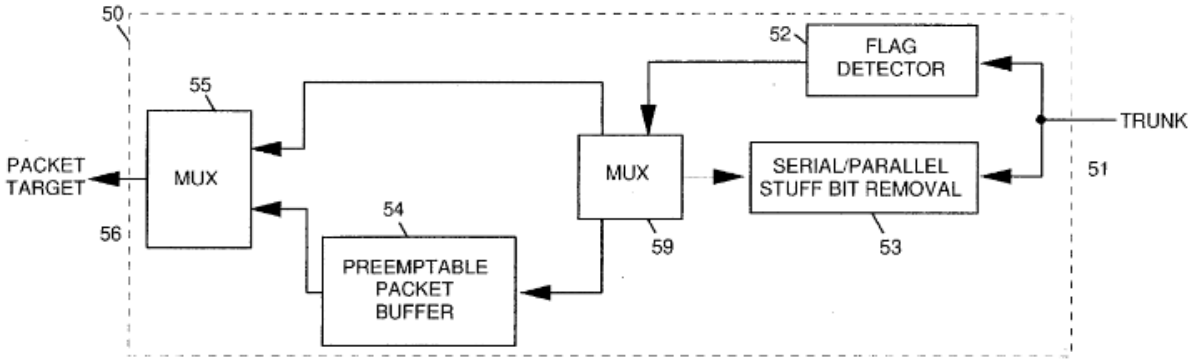
| | | To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(a) | a transmission component that transmits a first packet; and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br>  <br><br>**Figure 13**<br>Calvignac '608 at Fig. 13.<br>  <br><br>**Figure 14** |

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| | | Calvignac '608 at Fig. 14.<br><br>"FIG. 13 shows a block diagram of the transmitter 40 portion of the trunk interface of that communications system. Packets arrive from the communications system's packet source 41 for transmission on communication link 48. The packets may have been generated locally by this system or may have been received from another trunk on this system (e.g. an intermediate node in a packet net work). The communications system places the high-priority packets into a high priority buffer 42 and places the low-priority packets into a low priority buffer 43. If no packets are stored in either high priority buffer 42 or low priority buffer 43, a flag generator 46 is connected to the communication link 48 via a bit multiplexer 47. The flag generator 46 repeatedly generates an idle flag X`7E`, when no packets are stored for transmission."<br>Calvignac '608 at 8:6-20.<br><br>"FIG. 14 shows a block diagram of the receiver 50 portion of the communication link interface of the communications system up to a point at which received whole packets are passed to a packet target 56 within the communications system. The packet target 56 could be the final destination for the received packets or could be a packet switch used to route packets to other trunks for transmission to other nodes in a packet network. Any buffering associated with the packet target 56 is outside the receiver 50 and is not included in FIG. 14."<br>Calvignac '608 at 9:4-13.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.b.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b) | a preemption component that signals the transmission component | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"A flag detector 52 continuously monitors the bit stream received from a communication link 51 trailer byte and idle flags. If a sequence of bits other than a flag is detected immediately following an idle flag, it indicates the beginning of a new frame. A serial/parallel converter 53 receives the |

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| | to stop transmitting the first packet, | bit stream, discards any `0` bit if it immediately follows five consecutive `1` bits, and converts the remaining bits into byte-parallel form. If the received packet is a high-priority , packet, the parallel byte data is passed directly through a multiplexer 59 to a multiplexer 55 connected to the packet target 56 until a normal ending flag is detected by the flag detector 52. The receiver 50 indicates the end of the packet to the packet target 56. If the received packet can be preempted (i.e. low-priority, non-real-time packet), then the parallel byte data is instead passed through byte multiplexer 59 to the preemptable packet buffer 54 in order to permit the entire packet to be accumulated before passing it to the packet target 56. If flag detector 52 detects a trailer byte that there is no partial byte in the serial parallel converter 53, then it indicates the beginning of a high-priority preempting packet and therefore the beginning of preempt mode. The bit stream is passed through the serial/parallel converter 53 as before but this time the parallel byte data is passed directly through the multiplexers 59 and 55 to the packet target 56 within the communications system.<br>When the flag detector 52 detects either a normal ending flag or a trailer byte indicating the end of preemption, then the receiver 50 indicates the end of the packet to the packet target 56. If a normal ending flag is detected, then the serial/parallel converter 53 will continue to route the parallel byte data from subsequent packets directly to the multiplexer 55. If a trailer byte indicating the end of preemption is detected, the receiver 50 will end preempt mode. The received bit stream will be routed through the serial parallel converter 53 and multiplexer 59 to the preemptable packet buffer 54 thus resuming reception of the preempted low-priority packet. If the flag detector 52 detects a normal ending flag indicating the end of the low-priority packet, the receiver 50 transfers the entire low-priority packet stored in the preemptable packet buffer 54 through the multiplexer 55 to the packet target 56."<br>Calvignac '608 at 9:13-38.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.d.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |

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| 21(b.1) | transmits a preempt indicator indicating that a second packet is to be transmitted, | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>"A flag detector 52 continuously monitors the bit stream received from a communication link 51 trailer byte and idle flags. If a sequence of bits other than a flag is detected immediately following an idle flag, it indicates the beginning of a new frame. A serial/parallel converter 53 receives the bit stream, discards any `0` bit if it immediately follows five consecutive `1` bits, and converts the remaining bits into byte-parallel form. If the received packet is a high-priority , packet, the parallel byte data is passed directly through a multiplexer 59 to a multiplexer 55 connected to the packet target 56 until a normal ending flag is detected by the flag detector 52. The receiver 50 indicates the end of the packet to the packet target 56. If the received packet can be preempted (i.e. low-priority, non-real-time packet), then the parallel byte data is instead passed through byte multiplexer 59 to the preemptable packet buffer 54 in order to permit the entire packet to be accumulated before passing it to the packet target 56. If flag detector 52 detects a trailer byte that there is no partial byte in the serial parallel converter 53, then it indicates the beginning of a high-priority preempting packet and therefore the beginning of preempt mode. The bit stream is passed through the serial/parallel converter 53 as before but this time the parallel byte data is passed directly through the multiplexers 59 and 55 to the packet target 56 within the communications system.<br><br>When the flag detector 52 detects either a normal ending flag or a trailer byte indicating the end of preemption, then the receiver 50 indicates the end of the packet to the packet target 56. If a normal ending flag is detected, then the serial/parallel converter 53 will continue to route the parallel byte data from subsequent packets directly to the multiplexer 55. If a trailer byte indicating the end of preemption is detected, the receiver 50 will end preempt mode. The received bit stream will be routed through the serial parallel converter 53 and multiplexer 59 to the preemptable packet buffer 54 thus resuming reception of the preempted low-priority packet. If the flag detector 52 detects a normal ending flag indicating the end of the low-priority packet, the receiver 50 transfers the entire low-priority packet stored in the preemptable packet buffer 54 through the multiplexer 55 to the packet target 56."<br>Calvignac '608 at 9:13-38.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 1.d. |

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| | | To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b.2) | transmits the second packet, and | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.f.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(b.3) | signals the transmission component to continue transmitting the first packet; | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.g-h.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| 21(c) | wherein packets include in-band symbols and the indicators include one or more out-of-band symbols. | Calvignac '608 discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 1.i.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 22** | | |

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| 22 | The communications device of claim 21 wherein the indicators are primitives. | Calvignac '608 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 16i.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 23** | | |
| 23 | The communications device of claim 21 wherein the in-band symbols are transition optimized and the out-of-band symbols are not transition optimized. | Calvignac '608 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 17.<br><br>To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |
| **Claim 26** | | |
| 26 | The communications device of claim 21 wherein the first packet includes a header that is transmitted only once. | Calvignac '608 discloses, expressly or inherently, the communications device of claim 21 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*:<br><br>*See* exemplary disclosures and corresponding discussion for Claim 21.<br><br>*See also* exemplary disclosures and corresponding discussion for Claim 20. |

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| | | To the extent that Plaintiff contends that Calvignac '608 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions. |