PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5533419

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	05/17/2019

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SILICON IMAGE, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	SIBEAM, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124
Name:	DVDO, INC.
Street Address:	5555 NE MOORE CT
City:	HILLSBORO
State/Country:	OREGON
Postal Code:	97124

PROPERTY NUMBERS Total: 1143

Property Type	Number
Patent Number:	5574678
Patent Number:	5510738
Patent Number:	5493205
Patent Number:	5617064
Patent Number:	5670907

Property Type	Number
Patent Number:	5490074
Patent Number:	5596524
Patent Number:	5491433
Patent Number:	5756367
Patent Number:	5594687
Patent Number:	5570046
Patent Number:	5583451
Patent Number:	5621650
Patent Number:	5521529
Patent Number:	5818254
Patent Number:	5781030
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Patent Number:	5589782
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Patent Number:	5764078
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Patent Number:	5594365
Patent Number:	5811986
Patent Number:	5754471
Patent Number:	5594657
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Property Type	Number
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Patent Number:	5672521
Patent Number:	5809522
Patent Number:	5739713
Patent Number:	5736888
Patent Number:	5719516
Patent Number:	5598346
Patent Number:	5623217
Patent Number:	5926841
Patent Number:	5646901
Patent Number:	5751163
Patent Number:	5666087
Patent Number:	5748525
Patent Number:	5864486
Patent Number:	5789939
Patent Number:	5723984
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Patent Number:	5751164
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Patent Number:	5991907
Patent Number:	5805607
Patent Number:	5811987
Patent Number:	5892962
Patent Number:	5717342
Patent Number:	6028993

Property Type	Number
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Patent Number:	5885904
Patent Number:	6190966
Patent Number:	5905385
Patent Number:	5844912
Patent Number:	5835405
Patent Number:	6087275
Patent Number:	6034541
Patent Number:	5949279
Patent Number:	5989957
Patent Number:	5978272
Patent Number:	6028447
Patent Number:	6072351
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Property Type	Number
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Patent Number:	6093946
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Patent Number:	6064225
Patent Number:	5982683
Patent Number:	6556154
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Patent Number:	6133769
Patent Number:	6404006
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Patent Number:	6175266
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Patent Number:	6524911
Patent Number:	6287916
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Patent Number:	6414521
Patent Number:	6496969
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Patent Number:	6993108
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Patent Number:	6870395
Application Number:	10392751
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Patent Number:	6873187
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Patent Number:	6924664
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Patent Number:	6975137
Patent Number:	7382293
Patent Number:	7589648
Patent Number:	7532646
Patent Number:	7245154
Patent Number:	7057397

Property Type	Number
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Patent Number:	7414913
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Patent Number:	7599457
Patent Number:	7295035
Patent Number:	7411419
Patent Number:	7606851
Patent Number:	7187586
Application Number:	11206282
Patent Number:	7301182
Patent Number:	7167405
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Patent Number:	7263024
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Patent Number:	7317343
Patent Number:	7212051
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Property Type	Number
Patent Number:	7538574
Patent Number:	7620839
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Patent Number:	7382169
Patent Number:	7439783
Patent Number:	7547995
Patent Number:	7554357
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Patent Number:	7466190
Patent Number:	7521969
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Property Type	Number
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Patent Number:	7663401
Patent Number:	7535258
Patent Number:	7725803
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Property Type	Number
Patent Number:	7630259
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Patent Number:	8069329
Patent Number:	7652500
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Patent Number:	7459935
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Property Type	Number
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Patent Number:	7768300
Patent Number:	8255733
Patent Number:	7969248
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Property Type	Number
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Patent Number:	8654600
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Patent Number:	8797064
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Application Number:	13155261
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Application Number:	13466463
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Property Type	Number
Application Number:	14021513
Application Number:	14043920
Application Number:	14053026
Application Number:	14070975
Application Number:	14095310
Application Number:	14136482
Application Number:	14137443
Application Number:	14147796
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Application Number:	14482001
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Property Type	Number
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Application Number:	14611069
Application Number:	14611095
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Application Number:	12242665
Application Number:	14196978
Application Number:	14474005
Application Number:	61989417
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Application Number:	61989415

Property Type	Number
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Application Number:	61989411
Application Number:	14463146
Application Number:	14578266
Application Number:	14578257
Application Number:	62089767
Patent Number:	8482462
Patent Number:	8207892
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Application Number:	14196993
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Patent Number:	8571126
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Application Number:	14234623
Application Number:	14240405
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Patent Number:	6374361
Patent Number:	6738417

Property Type	Number
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Patent Number:	6473476
Patent Number:	6867814
Patent Number:	7203557
Patent Number:	7408992
Patent Number:	7123307

Property Type	Number
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Patent Number:	6809567
Patent Number:	7062004
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Patent Number:	7035290
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Patent Number:	7187307
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Patent Number:	7269673
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Patent Number:	7793179
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Application Number:	13984018
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Application Number:	13773534
Application Number:	13460393
Patent Number:	8925003
Patent Number:	8885435
Application Number:	13770984
Patent Number:	8920188

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Application Number:	13738768
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Application Number:	14123037
Application Number:	13776577
Application Number:	13940038
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Patent Number:	8786776
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Application Number:	14371973
Application Number:	14115324
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Application Number:	14391382
Application Number:	14165340
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Application Number:	14279316
Application Number:	14383865
Application Number:	61949901
Application Number:	14563797

Property Type	Number
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Application Number:	62075554
Application Number:	14570817
Application Number:	14589889
Application Number:	14589925
Application Number:	14591845
Application Number:	14449095
Application Number:	12842190

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NAME OF SUBMITTER:	URMILA KARANDIKAR
SIGNATURE:	/Urmila Karandikar/
DATE SIGNED:	05/21/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 97

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RELEASE OF A SECURITY INTEREST -- PATENTS

May 17, 2019

WHEREAS, pursuant to that certain (i) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035222, Frame 0866, (ii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0428, (iii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0001, (iv) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0289, (v) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035223, Frame 0387, (vi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035226, Frame 0147, (vii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0048, (viii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035220, Frame 0226, (ix) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035309, Frame 0142, (x) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035308, Frame 0345, (xi) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0839 and (xii) Grant of Security Interest in United States Patents, dated as of March 10, 2015, Reel 035225, Frame 0352, LATTICE SEMICONDUCTOR CORPORATION, SILICON IMAGE, INC., SIBEAM, INC. and DVDO, INC., each a Delaware corporation (each, a "Releasee"), granted to JEFFERIES FINANCE LLC, as collateral agent for the ratable benefit of the Secured Creditors (the "Releasor"), a continuing security interest in all right, title and interest of the Releasees in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations;

WHEREAS, the Releasees have satisfied their Obligations; and

WHEREAS, the Releasee has requested and the Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, the Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grants of Security Interests in United States Patents.

2. Release of Security Interest. The Releasor hereby, without any representation and warranty and without any recourse to the Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

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IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Collateral Agent and Releasor

By: _____
Name: Paul Chisholm
Title: Managing Director

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SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/396,994	5574678	United States	Continuous Time Programmable Analog Block Architecture	Issued	Lattice Semiconductor Corporation
08/403,359	5510738	United States	CMOS Programmable Resistor-Based Transconductor	Issued	Lattice Semiconductor Corporation
08/403,354	5493205	United States	Low Distortion Differential Transconductor Output Current Mirror	Issued	Lattice Semiconductor Corporation
08/403,352	5617064	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/403,595	5670907	United States	VBB Reference for Pumped Substrates	Issued	Lattice Semiconductor Corporation
08/423,303	5490074	United States	Constant delay interconnect for coupling configurable logic blocks	Issued	Lattice Semiconductor Corporation
08/427,117	5596524	United States	CMOS memory cell with gate oxide of both NMOS and PMOS transistors as tunneling window for program and erase	Issued	Lattice Semiconductor Corporation
08/444,306	5491433	United States	Cascode array cell partitioning for a sense amplifier of a programmable logic device	Issued	Lattice Semiconductor Corporation
08/449,384	5756367	United States	Method of making a spacer based antifuse structure for low capacitance and high reliability	Issued	Lattice Semiconductor Corporation
08/447,991	5594687	United States	Completely complementary MOS memory cell with tunneling through the NMOS and PMOS transistors during program and erase	Issued	Lattice Semiconductor Corporation

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/453,184	5570046	United States	Lead frame with noisy and quiet Vss and Vdd leads	Issued	Lattice Semiconductor Corporation
08/453,479	5583451	United States	Polarity control circuit which may be used with a ground bounce limiting buffer	Issued	Lattice Semiconductor Corporation
08/456,946	5621650	United States	Programmable gate array with improved interconnect structure, input/output structure and configurable logic block	Issued	Lattice Semiconductor Corporation
08/459,960	5521529	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/459,230	5818254	United States	Multi-tiered hierarchical high speed switch matrix structure for very high-density complex programmable logic devices	Issued	Lattice Semiconductor Corporation
08/459,234	5781030	United States	Programmable uniform symmetrical distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/459,786	5638018	United States	P-type flip flop	Issued	Lattice Semiconductor Corporation
08/458,865	5589782	United States	Macrocell and clock signal allocation circuit for a programmable logic device (PLD) enabling PLD resources to provide multiple functions	Issued	Lattice Semiconductor Corporation
08/459,570	6531890	United States	Programmable optimized-distribution logic allocator for a high-density complex PLD	Issued	Lattice Semiconductor Corporation
08/461,196	5586044	United States	Array of configurable logic blocks including cascadable lookup tables	Issued	Lattice Semiconductor Corporation
08/462,934	5469368	United States	Array of configurable logic blocks each including a first	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			lookup table coupled to selectively replace an output of second lookup with an alternate function output		Corporation
08/486,178	5764078	United States	Family of multiple segmented programmable logic blocks interconnected by a high speed centralized switch matrix	Issued	Lattice Semiconductor Corporation
08/474,629	5612631	United States	An I/O macrocell for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/479,872	5869981	United States	A High density programmable logic device	Issued	Lattice Semiconductor Corporation
08/486,174	5594365	United States	Architecture of a multiple array high density programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/474,635	5811986	United States	Flexible synchronous/asynchronous cell structure for a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/466,438	5754471	United States	Low power CMOS array for a PLD with program and erase using controlled avalanche injection	Issued	Lattice Semiconductor Corporation
08/473,620	5594657	United States	Field Programmable Gate Array Using Look-Up Tables, Multiplexers and Decoders	Issued	Lattice Semiconductor Corporation
08/483,623	5617042	United States	Multiple array programmable logic device with a plurality of programmable switch matrices	Issued	Lattice Semiconductor Corporation
08/492,604	5526278	United States	System for Synthesizing Field Programmable Gate Array	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Implementations From High Level Circuit Descriptions		Corporation
08/493,640	5679599	United States	Isolation using self-aligned trench formation and conventional LOCOS	Issued	Lattice Semiconductor Corporation
08/494,271	5565794	United States	Voltage range tolerant CMOS output buffer with reduced input capacitance	Issued	Lattice Semiconductor Corporation
08/497,992	5742542	United States	Nonvolatile memory cells using only positive charge to store data	Issued	Lattice Semiconductor Corporation
08/500,295	5700698	United States	Method for screening non-volatile memory and programmable logic devices	Issued	Lattice Semiconductor Corporation
08/501,230	5604370	United States	Field Implant For Semiconductor Device	Issued	Lattice Semiconductor Corporation
08/505,837	5635855	United States	Method for Simultaneous Programming of In-System Programmable Integrated Circuits	Issued	Lattice Semiconductor Corporation
08/507,893	5570039	United States	Method and Apparatus for Converting Field-Programmable Gate Array Implementations Into Mask-Programmable Logic Cell Implementations	Issued	Lattice Semiconductor Corporation
08/507,957	5559450	United States	Programmable Function Unit As Parallel Multiplier Cell	Issued	Lattice Semiconductor Corporation
08/528,030	5581126	United States	Interlaced layout configuration for differential pairs of interconnect lines	Issued	Lattice Semiconductor Corporation
08/535,362	5528170	United States	Low-Skew Signal Routing In A Programmable Array	Issued	Lattice Semiconductor Corporation
08/551,974	5615150	United States	control gate-addressed cmos non-volatile cell that programs through gates of CMOS transistors	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/554,092	5587945	United States	CMOS EEPROM cell with tunneling window in the read path	Issued	Lattice Semiconductor Corporation
08/560,038	5666309	United States	Memory cell for a programmable logic device (PLD) avoiding pumping programming voltage above an NMOS threshold	Issued	Lattice Semiconductor Corporation
08/560,933	5587921	United States	Array of configurable logic blocks each including a lookup table having inputs coupled to a first multiplexer and having outputs to a second multiplexer	Issued	Lattice Semiconductor Corporation
08/561,306	5672521	United States	Method of forming multiple gate oxide thicknesses on a wafer substrate	Issued	Lattice Semiconductor Corporation
08/573,622	5809522	United States	Microprocessor system with process identification tag entries to reduce cache flushing after a context switch	Issued	Lattice Semiconductor Corporation
08/574,776	5739713	United States	Deconvolution input buffer compensating for capacitance of a switch matrix of a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/575,898	5736888	United States	Capacitance elimination circuit	Issued	Lattice Semiconductor Corporation
08/575,852	5719516	United States	Clock generator circuit for use with a dual edge register that provides a separate enable for each edge over an input clock signal	Issued	Lattice Semiconductor Corporation
08/596,679	5598346	United States	Array of configurable logic blocks including network means for broadcasting clock signals to different pluralities of logic blocks	Issued	Lattice Semiconductor Corporation
08/606,702	5623217	United States	Field Programmable Gate Array With Write-Port Enabled Memory	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/614,728	5926841	United States	Segment descriptor cache for a processor	Issued	Lattice Semiconductor Corporation
08/625,403	5646901	United States	CMOS memory cell with tunneling during program and erase through the NMOS and PMOS transistors and a pass gate separating the NMOS and PMOS transistors	Issued	Lattice Semiconductor Corporation
08/632,811	5751163	United States	Parallel Programming of ISP Devices Using An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/635,184	5666087	United States	Active Resistor For Stability Compensation [of Transconductor & Op-Amp Based Gain & Filter Stages]	Issued	Lattice Semiconductor Corporation
08/643,807	5748525	United States	Array cell circuit with split read/write line	Issued	Lattice Semiconductor Corporation
08/643,291	5864486	United States	Method And Apparatus For In-System Programming of A Programmable Logic Device Using a Two-Wire Interface	Issued	Lattice Semiconductor Corporation
08/653,186	5789939	United States	Very high-density complex programmable logic device with a multi-tiered hierarchical switch matrix and optimized flexible logic allocation	Issued	Lattice Semiconductor Corporation
08/659,279	5723984	United States	Field programmable gate array (FPGA) with interconnect encoding	Issued	Lattice Semiconductor Corporation
08/659,941	5808942	United States	Field programmable gate array (FPGA) having an improved configuration memory and look up table	Issued	Lattice Semiconductor Corporation
08/664,190	5830795	United States	Simplified masking process for programmable logic device manufacture	Issued	Lattice Semiconductor Corporation
08/666,193	5760609	United States	Clock signal providing circuit with enable and a pulse generator with enable for use	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			in a block clock circuit of a programmable logic device		
08/668,141	5796295	United States	Reference for CMOS memory cell having PMOS and NMOS transistors with a common floating gate	Issued	Lattice Semiconductor Corporation
08/668,896	5751164	United States	Programmable logic device with multi-level power control	Issued	Lattice Semiconductor Corporation
08/683,685	5734275	United States	Programmable logic device having a sense amplifier with virtual ground	Issued	Lattice Semiconductor Corporation
08/683,373	5818294	United States	Temperature insensitive current source	Issued	Lattice Semiconductor Corporation
08/690,768	5801551	United States	Depletion mode pass gates with controlling decoder and negative power supply for a programmable logic device	Issued	Lattice Semiconductor Corporation
08/689,523	5942780	United States	An integrated circuit having, and process providing, different oxide layer thicknesses on a substrate	Issued	Lattice Semiconductor Corporation
08/696,444	5796750	United States	Method for Programming a PLD In An Automatic Tester	Issued	Lattice Semiconductor Corporation
08/700,616	5740069	United States	Logic device (PLD) having direct connections between configurable logic blocks (CLBs) and configurable input/output blocks (IOBs)	Issued	Lattice Semiconductor Corporation
08/699,401	5960274	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
08/702,846	5959336	United States	Decoder circuit with short channel depletion transistors	Issued	Lattice Semiconductor Corporation
08/710,445	5862365	United States	Configuration Pin Emulation Circuit For a Field Programmable Array	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/723,082	5760605	United States	Programmable high speed routing switch	Issued	Lattice Semiconductor Corporation
08/726,512	5761116	United States	Vpp only scalable EEPROM memory cell having transistors with thin tunnel gate oxide	Issued	Lattice Semiconductor Corporation
08/729,117	5991907	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/734,888	5805607	United States	Method for user-controlled I/O switching during in-circuit programming of CPLDs through the IEEE 1149.1 test access port	Issued	Lattice Semiconductor Corporation
08/740,948	5811987	United States	Block clock and initialization circuit for a complex high density PLD	Issued	Lattice Semiconductor Corporation
08/748,041	5892962	United States	FPGA-based Processor	Issued	Lattice Semiconductor Corporation
08/745,410	5717342	United States	Output buffer incorporating shared intermediate nodes	Issued	Lattice Semiconductor Corporation
08/781,882	6028993	United States	Timed Circuit Simulation In Hardware Using FPGAs	Issued	Lattice Semiconductor Corporation
08/785,096	5841701	United States	Method of charging and discharging floating gage transistors to reduce leakage current	Issued	Lattice Semiconductor Corporation
08/799,153	5904575	United States	Method and apparatus incorporating nitrogen selectively for differential oxide growth	Issued	Lattice Semiconductor Corporation
08/799,235	5885904	United States	Method to incorporate, and a device having, oxide enhancement dopants using gas immersion laser doping (GILD) for selectively growing an oxide layer	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/823,953	6190966	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion	Issued	Lattice Semiconductor Corporation
08/828,520	5905385	United States	Memory bits used to couple look up table inputs to facilitate increased availability to routing resources particularly for variable sized look up tables for a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/831,372	5844912	United States	Fast verify for CMOS memory cell	Issued	Lattice Semiconductor Corporation
08/827,671	5835405	United States	Application Specific Modules in a Programmable Logic Device	Issued	Lattice Semiconductor Corporation
08/843,150	6087275	United States	Reduction of n-channel parasitic transistor leakage by using low power/low pressure phosphosilicate glass	Issued	Lattice Semiconductor Corporation
08/838,487	6034541	United States	In-System Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
08/856,926	5949279	United States	Devices for sourcing constant supply current from power supply in system with integrated circuit having variable supply current requirement	Issued	Lattice Semiconductor Corporation
08/859,761	5989957	United States	Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration	Issued	Lattice Semiconductor Corporation
08/871,589	5978272	United States	Nonvolatile memory structure for programmable logic devices	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/899,428	6028447	United States	FPGA Having Predictable Open-Drain Drive Mode	Issued	Lattice Semiconductor Corporation
08/912,763	6072351	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt) semiconductor process	Issued	Lattice Semiconductor Corporation
08/931,798	6359466	United States	Circuitry to provide fast carry	Issued	Lattice Semiconductor Corporation
08/938,550	6020755	United States	Hybrid Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/948,306	6097212	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/947,888	5854114	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
08/949,992	6028463	United States	Programmable Clock Manager For A Programmable Logic Device that Can Generate At Least Two Different Output Clocks	Issued	Lattice Semiconductor Corporation
08/950,444	6216191	United States	Field Programmable Gate Array Having A Dedicated Processor Interface	Issued	Lattice Semiconductor Corporation
08/950,446	5986471	United States	Bi-directional Buffers and Supplemental Logic and Interconnect Cells for Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
08/950,448	6060902	United States	A Programmable Clock Manager For A Programmable Logic Device that Can Be Programmed Without Reconfiguring the Device	Issued	Lattice Semiconductor Corporation
08/950,624	6049224	United States	Programmable Logic Device With Logic Cells Having A Flexible Input Structure	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/951,128	6043677	United States	Programmable Clock Manager For A Programmable Logic Device that Can Implement Delay-Locked Loop Functions	Issued	Lattice Semiconductor Corporation
08/964,421	6389321	United States	Simultaneous Wired and Wireless Remote In-System Programming of Multiple Remote Systems	Issued	Lattice Semiconductor Corporation
08/974,799	6003150	United States	Method for Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
08/996,361	6275064	United States	Symmetrical, extended and fast direct connections between variable grain blocks in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,049	6127843	United States	Dual port SRAM memory for run time use in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,615	6034544	United States	Programmable input/output block (IOB) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,614	5982193	United States	Input/output block (IOB) connections to MAXL lines, NOR lines and dendrites in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/995,612	5990702	United States	Flexible direct connections between input/output blocks (IOBs) and variable grain blocks (VBGs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/997,221	6107823	United States	Programmable control multiplexing for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
08/996,119	5986480	United States	Multiple input zero power and/nor gate for use in a field programmable gate array (FPGA)	Issued	Lattice Semiconductor Corporation
08/996,530	6134703	United States	A Process for Programming PLDs and Embedded Non-Volatile Memories	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
08/998,978	6102963	United States	Electrically erasable and reprogrammable, nonvolatile integrated storage device with in-system programming and verification (ISPAV) capabilities for supporting in-system reconfiguring of PLD's	Issued	Lattice Semiconductor Corporation
09/008,762	6130551	United States	Synthesis-friendly FPGA architecture with variable length and variable timing interconnect	Issued	Lattice Semiconductor Corporation
09/010,000	6034538	United States	Virtual Logic System For Reconfigurable Hardware	Issued	Lattice Semiconductor Corporation
09/023,669	6025637	United States	Spacer based antifuse structure for low capacitance and high reliability and method of fabrication thereof	Issued	Lattice Semiconductor Corporation
09/023,506	6023570	United States	Sequential and Simultaneous Manufacturing Programming of Multiple In-System Programmable Systems Through a Data Network	Issued	Lattice Semiconductor Corporation
09/026,814	6093946	United States	EEPROM cell with field-edgeless tunnel window using shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/037,095	6128770	United States	Configurable logic array including IOB to longlines interconnect means for providing selectable access to plural longlines from each IOB (input/output block)	Issued	Lattice Semiconductor Corporation
09/045,128	6064225	United States	Global Signal Distribution With Reduced Routing Tracks In An FPGA	Issued	Lattice Semiconductor Corporation
09/046,404	5982683	United States	Enhanced method of testing semiconductor devices having nonvolatile elements	Issued	Lattice Semiconductor Corporation
09/053,251	6556154	United States	Offset Voltage Calibration DAC With Reduced Sensitivity To Mismatch	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Errors		
09/059,552	6108806	United States	Method of Testing and Diagnosing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/067,320	6154050	United States	Internal tristate bus with arbitration logic	Issued	Lattice Semiconductor Corporation
09/067,318	6104207	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/069,035	6133750	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/069,768	6002610	United States	Non-Volatile Memory Element For Programmable Logic Applications and Operational Methods Therefor	Issued	Lattice Semiconductor Corporation
09/080,906	6225821	United States	Package migration for related programmable logic devices	Issued	Lattice Semiconductor Corporation
09/083,335	6304099	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/083,336	6066977	United States	Programmable Output Voltage Levels	Issued	Lattice Semiconductor Corporation
09/083,205	6255847	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/086,437	6087696	United States	Stacked tunneling dielectric technology for improving data retention of EEPROM cell	Issued	Lattice Semiconductor Corporation
09/109,123	6202182	United States	Method and Apparatus For Testing Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/114,385	6028758	United States	Electrostatic discharge (ESD) protection for a 5.0 volt compatible input/output (I/O) in a 2.5 volt semiconductor process	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/114,717	6091595	United States	Electrostatic discharge (ESD) protection for NMOS pull up transistors of a 5.0 volt compatible output buffer using 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/114,718	6043969	United States	Ballast resistors with parallel stacked NMOS transistors used to prevent secondary breakdown during ESD with 2.5 volt process transistors	Issued	Lattice Semiconductor Corporation
09/115,683	6124732	United States	Signaling Voltage Range Discriminator	Issued	Lattice Semiconductor Corporation
09/118,200	6028446	United States	Flexible Synchronous and Asynchronus Circuits for A Very High Density Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/134,174	6064105	United States	Data retention of EEPROM cell with shallow trench isolation using thicker liner oxide	Issued	Lattice Semiconductor Corporation
09/145,793	6087854	United States	High Speed Line Driver With Direct and Complementary Outputs	Issued	Lattice Semiconductor Corporation
09/169,848	6347387	United States	Test Circuits For Multiple FPGA Systems	Issued	Lattice Semiconductor Corporation
09/169,492	6424003	United States	EEPROM cell with self-aligned tunneling window	Issued	Lattice Semiconductor Corporation
09/187,691	6228696	United States	Semiconductor-oxide-semiconductor capacitor formed in integrated circuit	Issued	Lattice Semiconductor Corporation
09/187,689	6154051	United States	Tileable and compact layout for super variable grain blocks within FPGA device	Issued	Lattice Semiconductor Corporation
09/186,917	6229336	United States	Programmable integrated circuit device with slew control and skew control	Issued	Lattice Semiconductor Corporation
09/188,778	6169432	United States	High voltage switch for	Issued	Lattice

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			providing voltages higher than 2.5 volts with transistors made using a 2.5 volt process		Semiconductor Corporation
09/192,094	6291327	United States	Optimization of S/D annealing to minimize random S/D shorts in memory array	Issued	Lattice Semiconductor Corporation
09/192,096	6221733	United States	Reduction of mechanical stress in shallow trench isolation process	Issued	Lattice Semiconductor Corporation
09/196,449	6191612	United States	Enhanced I/O control flexibility for generating control signals	Issued	Lattice Semiconductor Corporation
09/196,080	5912550	United States	Power converter with 2.5 semiconductor process components	Issued	Lattice Semiconductor Corporation
09/198,796	6218857	United States	Variable sized line driving amplifiers for input/output blocks (IOBs) in FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/200,395	6261944	United States	Semiconductor device having high reliability passivation and fabrication method	Issued	Lattice Semiconductor Corporation
09/198,653	6009033	United States	Method of programming and erasing an EEPROM device under an elevated temperature and apparatus thereof	Issued	Lattice Semiconductor Corporation
09/199,664	6353352	United States	Clock tree topology	Issued	Lattice Semiconductor Corporation
09/201,081	6133769	United States	Phase locked loop with a lock detector	Issued	Lattice Semiconductor Corporation
09/203,149	6404006	United States	EEPROM cell with tunneling across entire separated channels	Issued	Lattice Semiconductor Corporation
09/217,647	5969992	United States	EEPROM cell using p-well for	Issued	Lattice Semiconductor Corporation
09/207,558	6175266	United States	Operational amplifier with CMOS transistors made using	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			2.5 volt process transistors		Corporation
09/208,203	6163168	United States	Efficient interconnect network for use in FPGA device having variable grain architecture	Issued	Lattice Semiconductor Corporation
09/212,022	6124730	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,330	6100715	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/212,331	6081473	United States	FPGA integrated circuit having embedded SRAM memory blocks each with statically and dynamically controllable read mode	Issued	Lattice Semiconductor Corporation
09/216,662	6204686	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/216,051	6214666	United States	Method of forming a non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/217,648	6232631	United States	Floating gate memory cell structure with programming mechanism outside the read path	Issued	Lattice Semiconductor Corporation
09/217,646	6282123	United States	Method of fabricating, programming, and erasing a dual pocket two sided program/erase non-volatile memory cell	Issued	Lattice Semiconductor Corporation
09/218,987	6294810	United States	EEPROM cell with tunneling at separate edge and channel regions	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/220,469	6157568	United States	Avalanche programmed floating gate memory cell structure with program element in first polysilicon layer	Issued	Lattice Semiconductor Corporation
09/221,360	6294809	United States	Avalanche programmed floating gate memory cell structure with program element in polysilicon	Issued	Lattice Semiconductor Corporation
09/226,702	6215700	United States	PMOS avalanche programmed floating gate memory cell structure	Issued	Lattice Semiconductor Corporation
09/227,981	6197638	United States	Oxide formation process for manufacturing programmable logic device	Issued	Lattice Semiconductor Corporation
09/235,356	6097664	United States	Multi-port SRAM cell array having plural write paths including for writing through addressable port and through serial boundary scan	Issued	Lattice Semiconductor Corporation
09/235,351	6181163	United States	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control	Issued	Lattice Semiconductor Corporation
09/235,615	6211695	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
09/239,072	5999449	United States	Two transistor EEPROM cell using P-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/240,560	6297128	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/245,813	6294811	United States	Two transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/255,410	6075724	United States	Method for sorting	Issued	Lattice

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor devices having a plurality of non-volatile memory cells		Semiconductor Corporation
09/255,053	6255169	United States	Process for fabricating a high-endurance non-volatile memory device	Issued	Lattice Semiconductor Corporation
09/256,245	6133164	United States	Fabrication of oxide regions having multiple thicknesses using minimized number of thermal cycles	Issued	Lattice Semiconductor Corporation
09/261,776	6256758	United States	Fault Tolerance Operation of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/263412	6075293	United States	Semiconductor device having a multi-layer metal interconnect structure	Issued	Lattice Semiconductor Corporation
09/268,897	6207989	United States	Non-volatile memory device having a high-reliability composite insulation layer	Issued	Lattice Semiconductor Corporation
09/276,991	6031365	United States	Band gap reference using a low voltage power supply	Issued	Lattice Semiconductor Corporation
09/276,990	6163175	United States	High voltage detector to control a power supply voltage pump for a 2.5 volt semiconductor process device	Issued	Lattice Semiconductor Corporation
09/277,441	6326663	United States	Avalanche injection EEPROM memory cell with p-type control gate	Issued	Lattice Semiconductor Corporation
09/280,887	6172392	United States	Boron doped silicon capacitor plate	Issued	Lattice Semiconductor Corporation
09/286,830	6284626	United States	Angled nitrogen ion implantation for minimizing mechanical stress on side walls of an isolation trench	Issued	Lattice Semiconductor Corporation
09/288,062	6265900	United States	High Speed Logical OR Circuit	Issued	Lattice Semiconductor Corporation
09/287,976	6413826	United States	Gate insulator process for	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			nanometer MOSFETs		Corporation
09/310,071	6424000	United States	Floating gate memory apparatus and method for selected programming thereof	Issued	Lattice Semiconductor Corporation
09/316,241	6274898	United States	Triple-well EEPROM cell using p-well for tunneling across a channel	Issued	Lattice Semiconductor Corporation
09/318,570	6552595	United States	High Voltage Discharge Scheme	Issued	Lattice Semiconductor Corporation
09/320389	6118693	United States	Electrically erasable non-volatile memory cell with integrated SRAM to reduce testing time	Issued	Lattice Semiconductor Corporation
09/320,392	6067252	United States	Electrically erasable non-volatile memory cell with no static power dissipation	Issued	Lattice Semiconductor Corporation
09/326,940	6184713	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/326,140	6150841	United States	Enhanced storage macrocell module for high density CPLD architectures	Issued	Lattice Semiconductor Corporation
09/330,753	6628660	United States	Finite State Machine with Associated Memory	Issued	Lattice Semiconductor Corporation
09/334,051	6028789	United States	Zero-power CMOS non-volatile memory cell having an avalanche injection element	Issued	Lattice Semiconductor Corporation
09/334,052	6034893	United States	Non-volatile memory cell having dual avalanche injection elements	Issued	Lattice Semiconductor Corporation
09/400,029	6404226	United States	Integrated Circuit With Standard Cell Logic and Spare Gates	Issued	Lattice Semiconductor Corporation
09/405,958	6550030	United States	On-Line Testing of the Programmable Logic Blocks In Field Programmable Gate	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Arrays		
09/406,219	6574761	United States	On-Line Testing of the Programmable Interconnect Network In Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/433,642	6191609	United States	Combination of global clock and localized clocks	Issued	Lattice Semiconductor Corporation
09/440,460	6294925	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/440,207	6278311	United States	Method for minimizing instantaneous currents when driving bus signals	Issued	Lattice Semiconductor Corporation
09/441,220	6208559	United States	Method of operating EEPROM memory cells having transistors with thin gate oxide and reduced disturb	Issued	Lattice Semiconductor Corporation
09/452,017	6137738	United States	Method For In-System Programming of Serially Configured EEPROMS Using a JTAG Interface of an FPGA	Issued	Lattice Semiconductor Corporation
09/454,322	6326808	United States	Inversion of Product Term Line Before or Logic in a Programmable Logic Device (PLD)	Issued	Lattice Semiconductor Corporation
09/472,645	6150842	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/506,180	6362684	United States	Amplifier Having an Adjustable Resistor Network	Issued	Lattice Semiconductor Corporation
09/507,580	6424209	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
09/548,171	6351157	United States	Output buffer for making a high voltage (5.0 volt) compatible input/output in a low voltage (2.5 volt)	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			semiconductor process		
09/567,898	6288937	United States	Decoded Generic Routing Pool	Issued	Lattice Semiconductor Corporation
09/578,086	6570212	United States	Complementary avalanche injection EEPROM cell	Issued	Lattice Semiconductor Corporation
09/603,119	6292930	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/603,807	6216257	United States	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	Issued	Lattice Semiconductor Corporation
09/611,449	6530049	United States	On-line Fault Tolerant Operation Via Incremental Reconfiguration of Field Programmable Gate Arrays	Issued	Lattice Semiconductor Corporation
09/626,094	6380759	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
09/632,319	6567969	United States	Configurable Logic Array Including Lookup Table Means For Generating Functions of Different Numbers Of Input Terms	Issued	Lattice Semiconductor Corporation
09/643,279	6627947	United States	Compact single-poly two-transistor EEPROM cell	Issued	Lattice Semiconductor Corporation
09/651,689	6433602	United States	High speed schmitt trigger with low supply voltage	Issued	Lattice Semiconductor Corporation
09/660,707	6370071	United States	High Voltage CMOS switch	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
09/661,585	6462576	United States	Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/668,896	6701340	United States	Double Differential Comparator and Programmable Analog Block Architecture Using Same	Issued	Lattice Semiconductor Corporation
09/669,186	6249144	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/671,853	6631487	United States	On-Line Testing of Field Programmable Gate Array Resources	Issued	Lattice Semiconductor Corporation
09/692,694	6470485	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
09/704,487	6507212	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
09/651,805	6455912	United States	Process for manufacturing shallow trenches filled with dielectric material having low mechanical stress	Issued	Lattice Semiconductor Corporation
09/712,000	6356107	United States	Method and structure for dynamic in-system programming	Issued	Lattice Semiconductor Corporation
09/721,153	6348813	United States	Scalable architecture for high density CPLD's having two-level hierarchy of routing resources	Issued	Lattice Semiconductor Corporation
09/732,216	6735706	United States	Programmable power management system and method	Issued	Lattice Semiconductor Corporation
09/731,184	6524911	United States	Combination of BPTEOS oxide film with CMP and RTA to achieve good data	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			retention		
09/731,185	6287916	United States	Method for forming a semiconductor device using LPCVD nitride to protect floating gate from charge loss	Issued	Lattice Semiconductor Corporation
09/733,878	6526558	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	Issued	Lattice Semiconductor Corporation
09/775,488	6462602	United States	Voltage Level Translator Systems And Methods	Issued	Lattice Semiconductor Corporation
09/775,489	6414521	United States	Improved sense amplifier systems and methods	Issued	Lattice Semiconductor Corporation
09/818,257	6496969	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
09/841,209	6590415	United States	Methods for configuring FPGA's having variable grain blocks and shared logic for providing time-shared access to interconnect resources	Issued	Lattice Semiconductor Corporation
09/863,656	6535043	United States	Clock Signal Selection System, Method of Generating A Clock Signal And Programmable Clock Manager Including Same	Issued	Lattice Semiconductor Corporation
09/864,276	6486705	United States	Signal Distribution Scheme In Field Programmable Gate Array (FPGA) or Field Programmable Systems Chip (FPSC) Including Cycle Stealing Units	Issued	Lattice Semiconductor Corporation
09/864,284	6472904	United States	Double Data Rate Input And Output In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
09/864,289	6480026	United States	Multi-functional I/O Buffers In a Field Programmable Gate	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Array (FPGA)		Corporation
09/864,277	6483342	United States	Multi-Master Multi-Slave Bus In Field Programmable Gate Array (FPGA)	Issued	Lattice Semiconductor Corporation
09/864,290	6772230	United States	Field Programmable Gate Array (FPGA) Bit Stream Format	Issued	Lattice Semiconductor Corporation
09/870,877	6498538	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
09/870,541	6455375	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
09/881,950	6614291	United States	Low Voltage, High Speed CMOS CML Latch and MUX Devices	Issued	Lattice Semiconductor Corporation
09/885,243	6429692	United States	High Speed Data Sampling With Reduced Metastability	Issued	Lattice Semiconductor Corporation
09/927,289	6492877	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
09/927,612	6525617	United States	Buffering For LC-Based Stage	Issued	Lattice Semiconductor Corporation
09/927,793	6653860	United States	Enhanced logic macrocell with expanded PT (product term) sharing capability for Use in High Density CPLD Architectures	Issued	Lattice Semiconductor Corporation
09/941,454	6489835	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
09/949,112	6593222	United States	Method to improve the reliability of thermosonic gold to aluminum wire bonds	Issued	Lattice Semiconductor Corporation
09/966,967	6832231	United States	Multiple Width Random Number Generation	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/011,549	6693830	United States	Single Poly Two-Transistor EEPROM Cell With Differentially Doped Floating Gate	Issued	Lattice Semiconductor Corporation
10/053,004	6989551	United States	Test structure for determining the minimum tunnel opening size in a non-volatile memory cell	Issued	Lattice Semiconductor Corporation
10/010,011	6515899	United States	Non-Volatile Memory Cell With Enhanced Cell Drive Current	Issued	Lattice Semiconductor Corporation
09/991,245	6611463	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
09/992,493	6489806	United States	Zero power logic cell for use in programmable logic devices	Issued	Lattice Semiconductor Corporation
10/006,559	7003066	United States	Digital Phase locked Loop with Phase Selector having Minimized Number of Phase Interpolators	Issued	Lattice Semiconductor Corporation
10/006,610	6999543	United States	Clock Data Recovery Deserializer With Programmable Sync Detect Logic	Issued	Lattice Semiconductor Corporation
10/006,516	6993108	United States	Digital Phase Locked Loop With Programmable Digital Filter	Issued	Lattice Semiconductor Corporation
10/021,873	6661254	United States	Programmable Interconnect Circuit With A Phase-Locked Loop	Issued	Lattice Semiconductor Corporation
10/017,725	6674303	United States	Programmable I/O cell with bidirectional and shift register capabilities	Issued	Lattice Semiconductor Corporation
10/017,859	6605959	United States	Structure and Method for Implementing Wide Multiplexers	Issued	Lattice Semiconductor Corporation
10/022,464	7154298	United States	Block oriented architecture for programmable interconnect circuit	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/021,844	6703860	United States	I/O Block for Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,053	6653861	United States	Multi-level Routing Structure for a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/023,226	6650141	United States	High Speed Interface For a Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/059,624	6636442	United States	Non-volatile memory element having a cascoded transistor scheme to reduce oxide field stress	Issued	Lattice Semiconductor Corporation
10/061,057	6845044	United States	Method of preventing high Icc at start-up in zero-power EEPROM cells for PLD applications	Issued	Lattice Semiconductor Corporation
10/066,031	6680625	United States	Symmetrical CML Logic Gate System	Issued	Lattice Semiconductor Corporation
10/082,050	6781170	United States	Integrated Circuit Base Transistor Structure And Associated Programmable Cell Library	Issued	Lattice Semiconductor Corporation
10/083,728	6600188	United States	An EEPROM with neutralized doping at tunnel window edge	Issued	Lattice Semiconductor Corporation
10/090,209	6621298	United States	Variable grain architecture for FPGA integrated circuits	Issued	Lattice Semiconductor Corporation
10/103,100	6795959	United States	Integrated Delay Discriminator For Use With a Field- Programmable Gate Array and A Method of Determining a Time Delay Thereof	Issued	Lattice Semiconductor Corporation
10/106,509	6907439	United States	FFT address generation method and apparatus	Issued	Lattice Semiconductor Corporation
10/108,401	6976047	United States	Skipped carry incrementer for FFT address generation	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/112,370	6639431	United States	Differential Input Comparator	Issued	Lattice Semiconductor Corporation
10/128,943	6660579	United States	Zero Power Memory Cell With Improved Data Retention	Issued	Lattice Semiconductor Corporation
10/131,883	7032162	United States	Polynomial Expander for Generating Coefficients of a Polynomial from Roots of the Polynomial	Issued	Lattice Semiconductor Corporation
10/133,016	6765408	United States	Device and Method with Generic Logic Blocks	Issued	Lattice Semiconductor Corporation
10/135,308	6814296	United States	Integrated Circuit and Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/135,325	6600341	United States	Integrated Circuit and Associated Design Method Using Spare Gate Islands	Issued	Lattice Semiconductor Corporation
10/146,739	6714048	United States	Input Buffer With Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/146,826	6657458	United States	Output Buffer With Feedback From An Input Buffer To Provide Selectable PCL, GTL, or PECL Compatability	Issued	Lattice Semiconductor Corporation
10/146,769	6870391	United States	Input Buffer With CMOS Driver Gate Current Control Enabling Selectable PCL, GTL, or PECL Compatibility	Issued	Lattice Semiconductor Corporation
10/147,199	6714043	United States	Output Buffer Having Programmable Drive Current And Output Voltage Limits	Issued	Lattice Semiconductor Corporation
10/146,734	6720755	United States	Band Gap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/147,011	6760209	United States	Electrostatic Discharge Protection Circuit	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/151,753	6798244	United States	Output Buffer With Overvoltage Protection	Issued	Lattice Semiconductor Corporation
10/150,410	6848095	United States	Method of Assigning Logic Functions To Macrocells In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/159,009	6583652	United States	Highly linear programmable transconductor with large input-signal range	Issued	Lattice Semiconductor Corporation
10/159,089	6717451	United States	Precision analog level shifter with programmable options	Issued	Lattice Semiconductor Corporation
10/159,681	6806771	United States	Multimode output stage converting differential to single-ended signals using current-mode input signals	Issued	Lattice Semiconductor Corporation
10/162,337	6596587	United States	Shallow junction EEPROM Device and Process for Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/160,855	6794236	United States	EEPROM Device with Improved Capacitive Coupling and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/161,283	6716705	United States	EEPROM Device having a Retrograde Program Junction Region And Process for Fabrication the Device	Issued	Lattice Semiconductor Corporation
10/164,484	6703305	United States	Semiconductor Device Having Metallized Interconnect Structure And Method Of Fabricaton	Issued	Lattice Semiconductor Corporation
10/187,236	6844757	United States	Converting Bits to Vectors In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/191,888	6650143	United States	FPGA Based Upon Transistor gate Oxide Breakdown	Issued	Lattice Semiconductor Corporation
10/194,771	7028281	United States	FPGA With Register-Intensive Architecture	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/200,645	6714066	United States	Integrated Programmable Continuous Time Filter with Programmable Capacitor Arrays	Issued	Lattice Semiconductor Corporation
10/207,292	6683477	United States	Wide input programmable logic system and method	Issued	Lattice Semiconductor Corporation
10/210,367	6938197	United States	CRC Calculation System And Method For A Packet Arriving On An N-Byte Wide Bus	Issued	Lattice Semiconductor Corporation
10/211,125	6545313	United States	EEPROM tunnel window for program injection via P+ contacted inversion	Issued	Lattice Semiconductor Corporation
10/219,046	6650142	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-based Resource Allocation and Methods of Use	Issued	Lattice Semiconductor Corporation
10/233,021	7043511	United States	Performing Conditional Operations In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/232,912	6841447	United States	EEPROM Device Having An Isolation -Bounded Tunnel Capacitor And Fabrication Process	Issued	Lattice Semiconductor Corporation
10/235,380	6725442	United States	Scalable and parallel processing methods and structures for testing configurable interconnect network in FPGA device	Issued	Lattice Semiconductor Corporation
10/236,829	6842372	United States	EEPROM Cell Having Floating Gate Transistor Within a Cell Well And a Process For Fabricating the Memory Cell	Issued	Lattice Semiconductor Corporation
10/236,114	6833602	United States	Device Having Electrically Isolated Low Voltage And High Voltage Regions And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/236,718	6649514	United States	EEPROM Device Having Improved Data Retention And Process for Fabricating The Device	Issued	Lattice Semiconductor Corporation
10/242,809	6738306	United States	Multiport SRAM Cell	Issued	Lattice Semiconductor Corporation
10/243,014	6917536	United States	Memory access Circuit and Method for reading and writing data with the same clock signal	Issued	Lattice Semiconductor Corporation
10/251,608	6700154	United States	EEPROM cell with trench coupling capacitor	Issued	Lattice Semiconductor Corporation
10/255,474	6907592	United States	Method of Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,875	6809551	United States	Method of Optimizing Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,499	6803787	United States	State Machine In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/255,656	6812738	United States	Vector Routing In A Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/263,251	6748575	United States	Programming Programmable Logic Devices Using Hidden Switches	Issued	Lattice Semiconductor Corporation
10/263,507	6846714	United States	Voltage Limted EEPROM Device And Process For Fabricating the Device	Issued	Lattice Semiconductor Corporation
10/266,361	6639434	United States	Low voltage differential signaling systems and methods	Issued	Lattice Semiconductor Corporation
10/269,804	7111183	United States	Expansion method for complex power-sequencing applications	Issued	Lattice Semiconductor Corporation
10/269,450	6791394	United States	Power Supply Control Circuits	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/269,439	6762618	United States	Innovative verify scheme for two level GRP fuse in programmable bus switching family	Issued	Lattice Semiconductor Corporation
10/272,582	6901572	United States	Power Sequence Controller Programming Technique	Issued	Lattice Semiconductor Corporation
10/278,415	6639449	United States	Asynchronous glitch-free clock multiplexer	Issued	Lattice Semiconductor Corporation
10/282,524	7051261	United States	Turbo Encoder With Reduced Processing Delay	Issued	Lattice Semiconductor Corporation
10/283,765	6700823	United States	Programmable common mode termination for differential input/output circuits	Issued	Lattice Semiconductor Corporation
10/288,667	7000210	United States	Adaptive Adjustment Of Constraints During PLD Placement Processing	Issued	Lattice Semiconductor Corporation
10/288,668	6813754	United States	Placement Processing For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/300,190	6825733	United States	Low Jitter Integrated Phase Locked Loop With Broad Tuning Range	Issued	Lattice Semiconductor Corporation
10/302,439	6797568	United States	Flash Technology Transistors and Method For Forming Same	Issued	Lattice Semiconductor Corporation
10/308,420	6710641	United States	Low Voltage Bandgap Reference Circuit	Issued	Lattice Semiconductor Corporation
10/309,302	6650188	United States	Improved Coupling For LC-Based VCO	Issued	Lattice Semiconductor Corporation
10/334,642	6777979	United States	FIFO memory architecture	Issued	Lattice Semiconductor Corporation
10/338,619	6753696	United States	Programmable optimized-distribution logic allocator for	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			a high-density complex PLD		Corporation
10/365,083	7034596	United States	Adaptive input logic for phase adjustments	Issued	Lattice Semiconductor Corporation
10/368,023	6915323	United States	Macrocells Supporting A Carry Cascade	Issued	Lattice Semiconductor Corporation
10/366,956	6788101	United States	Programmable input buffer for differential and single-ended signals	Issued	Lattice Semiconductor Corporation
10/367,323	6812869	United States	Noise Reduction Techniques For Programmable I/O Circuits	Issued	Lattice Semiconductor Corporation
10/370,232	6861870	United States	Dynamic Cross point Switch With Shadow Memory Architecture	Issued	Lattice Semiconductor Corporation
10/377,320	6859066	United States	Bank based input/output buffers in field programmable gate arrays with multiple reference voltages	Issued	Lattice Semiconductor Corporation
10/387,814	7305047	United States	Automatic lane assignment for Receiver	Issued	Lattice Semiconductor Corporation
10/387,243	7339952	United States	Pointer Processing For Optical Communication Systems	Issued	Lattice Semiconductor Corporation
10/391,094	6870395	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
10/392,751	RE39510	United States	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	Issued	Lattice Semiconductor Corporation
10/397,669	6967500	United States	Electronic Circuit With OnChip Programmable Terminations	Issued	Lattice Semiconductor Corporation
10/400,705	6873187	United States	Method and Apparatus for Controlling Signal Distribution In An Electronic	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Circuit		
10/406,050	7000212	United States	Hierarchical General Interconnect Architecture For High Density FPGA's	Issued	Lattice Semiconductor Corporation
10/409,543	6986004	United States	FIFO memory with programmable data port widths	Issued	Lattice Semiconductor Corporation
10/417,290	6879184	United States	Programmable logic device architecture based on arrays of LUT-based Boolean terms	Issued	Lattice Semiconductor Corporation
10/425,863	6903575	United States	Scalable device architecture for high-speed interfaces	Issued	Lattice Semiconductor Corporation
10/425,862	6894530	United States	Programmable And Fixed Logic Circuitry For High-Speed Interfaces	Issued	Lattice Semiconductor Corporation
10/428,889	6879182	United States	CPLD with multi-function blocks and distributed memory	Issued	Lattice Semiconductor Corporation
10/428,885	6861871	United States	Cascaded logic block architecture for complex programmable logic devices	Issued	Lattice Semiconductor Corporation
10/428,888	6864713	United States	Multi-Stage Interconnect Architecture For Complex Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/428,982	6922078	United States	Enhanced wide and deep logic capability for high density, high performance CPLDs	Issued	Lattice Semiconductor Corporation
10/439,602	6828823	United States	Non-volatilie and reconfigurable PLDs	Issued	Lattice Semiconductor Corporation
10/441,814	7039842	United States	Measuring Propagation Delays of Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
10/447,120	7301996	United States	skew cancellation for source synchronous clock and data signals	Issued	Lattice Semiconductor Corporation
10/447,451	7009433	United States	Digitally Controlled Delay Cells	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
10/457,630	7304863	United States	Integrated Circuit Including External Electronic Components With Low Insertion Loss	Issued	Lattice Semiconductor Corporation
10/459,091	6879598	United States	Flexible Media Access Control Architecture	Issued	Lattice Semiconductor Corporation
10/460,385	6856171	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
10/463,781	6861868	United States	High Speed Interface For A Programmable Interconnect Circuit	Issued	Lattice Semiconductor Corporation
10/464,083	6882555	United States	Bi-directional buffering for memory data lines	Issued	Lattice Semiconductor Corporation
10/600,042	6822477	United States	Integrated Circuit And Associated Design Method Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/610,253	6977408	United States	High-Performance Non-volatile Memory Device and Fabrication Process	Issued	Lattice Semiconductor Corporation
10/613,460	7132903	United States	Noise-shielding, switch-controlled load circuitry for oscillators and the like	Issued	Lattice Semiconductor Corporation
10/613,462	6952115	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
10/617,980	6958625	United States	PLD With Hardwired Microsequencer	Issued	Lattice Semiconductor Corporation
10/619,711	6903573	United States	Programmable Logic Device With Enhanced Wide Input Product Term Cascading	Issued	Lattice Semiconductor Corporation
10/620,286	6919736	United States	FPGA having partitionable embedded memory with configurable depth and width	Issued	Lattice Semiconductor Corporation
10/619,645	7098685	United States	Scalable Serializer-Deserializer Architecture and	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Programmable Interface		Corporation
10/620,147	7032203	United States	Algorithm to increase logic input width by cascading product terms	Issued	Lattice Semiconductor Corporation
10/624,965	6940309	United States	Programmable Logic Device With A Memory-Based Finite State Machine	Issued	Lattice Semiconductor Corporation
10/626,089	6737702	United States	Zero Power Memory Cell with Reduced Threshold Voltage	Issued	Lattice Semiconductor Corporation
10/628,656	6970047	United States	Programmable lock detector and corrector	Issued	Lattice Semiconductor Corporation
10/628,657	6924659	United States	Programmable Signal Termination for FPGAs and the Like	Issued	Lattice Semiconductor Corporation
10/629,223	7019577	United States	Clock Generator	Issued	Lattice Semiconductor Corporation
10/629,512	6903574	United States	Memory Access Via Serial Memory Interface	Issued	Lattice Semiconductor Corporation
10/629,221	6885227	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
10/640,804	6877667	United States	Integrated Circuit And Associated Design Method With Antenna Error Control Using Spare Gates	Issued	Lattice Semiconductor Corporation
10/640,828	6838904	United States	Enhanced CPLD Macrocell Module Having Selectable Bypass of Steering-Based Resource Allocation	Issued	Lattice Semiconductor Corporation
10/641,260	6940779	United States	Programmable broadcasting initialization of embedded memory blocks on FPGA	Issued	Lattice Semiconductor Corporation
10/642,370	6924664	United States	FPGA	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/655,686	6842037	United States	Shared Transmission Line Communication System and Method	Issued	Lattice Semiconductor Corporation
10/660,814	7038490	United States	Delay matched ASIC conversion of a PLD	Issued	Lattice Semiconductor Corporation
10/665,920	6970022	United States	Controlled hysteresis comparator with rail-to-rail input	Issued	Lattice Semiconductor Corporation
10/671,378	6943583	United States	Programmable I/O structure for FPGAs and the like having reduced pad capacitance	Issued	Lattice Semiconductor Corporation
10/671,363	6943582	United States	Programmable I/O structure for FPGAs and the Like Having Shared Circuitry	Issued	Lattice Semiconductor Corporation
10/671,756	6909663	United States	Multiport Memory With Twisted Bitlines	Issued	Lattice Semiconductor Corporation
10/676,536	7269771	United States	Semiconductor Device Adapted For Forming Multiple Scan Chains	Issued	Lattice Semiconductor Corporation
10/687,468	6809674	United States	Analog-to-digital converters	Issued	Lattice Semiconductor Corporation
10/699,321	7067883	United States	Lateral High-Voltage Junction Device	Issued	Lattice Semiconductor Corporation
10/701,005	7091763	United States	Clock generation	Issued	Lattice Semiconductor Corporation
10/704,025	7088134	United States	PLD With Flexible Memory Allocation And Routing	Issued	Lattice Semiconductor Corporation
10/726,972	7100058	United States	Programmable Power Management System And Method	Issued	Lattice Semiconductor Corporation
10/728,685	7187157	United States	Power supply remote voltage sensing	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/737,514	6981381	United States	Linear Thermoelectric Device Driver	Issued	Lattice Semiconductor Corporation
10/744,353	7132864	United States	Method for configuring multiple-output phase-locked loop frequency synthesizer	Issued	Lattice Semiconductor Corporation
10/769,174	7024646	United States	Electrostatic Discharge Simulation	Issued	Lattice Semiconductor Corporation
10/768,643	7019584	United States	Output Stages For High Current Low Noise Bandgap Reference Circuit Implementations	Issued	Lattice Semiconductor Corporation
10/782,564	6972986	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/783,886	7081771	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
10/791,073	7191388	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation
10/794,079	7257727	United States	Timer Systems and Methods	Issued	Lattice Semiconductor Corporation
10/794,524	7017063	United States	systems and methods for controlling voltage regulator module power supplies	Issued	Lattice Semiconductor Corporation
10/794,498	7028201	United States	Powering up a device having digital and analog circuitry	Issued	Lattice Semiconductor Corporation
10/797,759	7068556	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
10/809,180	7234030	United States	Table based scheduler for FIFOs and the like	Issued	Lattice Semiconductor Corporation
10/809,658	7095247	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/815,403	7167032	United States	Self-adjusting schmitt trigger	Issued	Lattice Semiconductor Corporation
10/817,215	7081781	United States	Charge pump for a low-voltage wide-tuning range phase-locked loop	Issued	Lattice Semiconductor Corporation
10/829,865	6998896	United States	Dynamic gain adjustment systems and method for metastability resistance	Issued	Lattice Semiconductor Corporation
10/834,528	6998906	United States	Low pass filter systems and methods	Issued	Lattice Semiconductor Corporation
10/837,086	7307319	United States	High Voltage Protection Device And Process	Issued	Lattice Semiconductor Corporation
10/842,345	7002418	United States	Control Signal Generation ...	Issued	Lattice Semiconductor Corporation
10/841,987	7224213	United States	switched-capacitor ripple-smoothing filter	Issued	Lattice Semiconductor Corporation
10/843,708	7061269	United States	IO buffer architecture for programmable devices	Issued	Lattice Semiconductor Corporation
10/856,100	7196551	United States	Current Mode Logic Buffer	Issued	Lattice Semiconductor Corporation
10/857,667	7064973	United States	Combination FPGA	Issued	Lattice Semiconductor Corporation
10/885,419	7116585	United States	Memory Systems And Methods	Issued	Lattice Semiconductor Corporation
10/910,091	7215591	United States	Byte enable logic for memory	Issued	Lattice Semiconductor Corporation
10/912,943	7471752	United States	Data Transmission Synchronization	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/928,563	7078286	United States	Process for fabricating a semiconductor device having electrically isolated low voltage and high voltage regions	Issued	Lattice Semiconductor Corporation
10/929,199	7484144	United States	Testing embedded memory in an integrated circuit	Issued	Lattice Semiconductor Corporation
10/944,978	7135886	United States	FPGA Using Both Volatile and NonVolatile Memory Cell Properties	Issued	Lattice Semiconductor Corporation
10/974,453	7307912	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
10/973,750	7149129	United States	memory output data systems and methods with feedback	Issued	Lattice Semiconductor Corporation
10/974,107	7164290	United States	FPGA Logic Unit	Issued	Lattice Semiconductor Corporation
10/974,305	7129749	United States	PLD Having A Configurable DRAM With Transparent Refresh	Issued	Lattice Semiconductor Corporation
10/978,899	7376872	United States	Testing embedded memory in integrated circuits such as progammable logic circuits	Issued	Lattice Semiconductor Corporation
10/996,283	7161862	United States	Low power asynchronous sense amp	Issued	Lattice Semiconductor Corporation
11/007,954	7230810	United States	Dynamic over-voltage protection scheme for integrated circuit devices	Issued	Lattice Semiconductor Corporation
11/012,550	7215149	United States	Interface circuitry for electrical systems	Issued	Lattice Semiconductor Corporation
11/012,548	7215148	United States	Programmable current LVDS output buffer	Issued	Lattice Semiconductor Corporation
11/015,265	7177221	United States	Method of initializing configurable multi-port	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			embedded memory blocks in an FPGA		Corporation
11/016,665	7187203	United States	Cascadable memory	Issued	Lattice Semiconductor Corporation
11/015,369	7177207	United States	Sense amplifier timing	Issued	Lattice Semiconductor Corporation
11/036,630	7257750	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/036,738	7242053	United States	EEPROM Device with voltage-limiting charge pump circuit	Issued	Lattice Semiconductor Corporation
11/040,772	7208975	United States	Serdes with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
11/041,319	7183798	United States	Synchronous memory	Issued	Lattice Semiconductor Corporation
11/044,089	7109754	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,149	7109756	United States	Synchronization of programmable multiplexers and demultiplexers	Issued	Lattice Semiconductor Corporation
11/044,508	7034599	United States	Clock Generator With Skew Control	Issued	Lattice Semiconductor Corporation
11/054,011	7221607	United States	Mult-port memory systems and methods for bit line coupling	Issued	Lattice Semiconductor Corporation
11/055,280	6975137	United States	PLDs With Integrated Standard Cell Logic Blocks	Issued	Lattice Semiconductor Corporation
11/054,750	7382293	United States	Data Decompression	Issued	Lattice Semiconductor Corporation
11/054,855	7589648	United States	Data Decompression	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/064,477	7532646	United States	Distributed multiple channel alignment scheme	Issued	Lattice Semiconductor Corporation
11/071,356	7245154	United States	Differential Input Receiver with Programmable Failsafe	Issued	Lattice Semiconductor Corporation
11/070,926	7057397	United States	Output Impedance Measurement Techniques	Issued	Lattice Semiconductor Corporation
11/083,625	7376204	United States	Detection of Unknown symbol rate in a digitally modulated signal	Issued	Lattice Semiconductor Corporation
11/098,713	7265578	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/100,718	7397274	United States	In-System Programming Of a Non-Compliant Device Using Multiple Interfaces Of A PLD	Issued	Lattice Semiconductor Corporation
11/108,927	7193436	United States	Fast Processing Path Using FPGA Logic Units	Issued	Lattice Semiconductor Corporation
11/109,301	7630464	United States	Analog-to-digital systems and methods	Issued	Lattice Semiconductor Corporation
11/109,966	6977521	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/121,326	7400171	United States	Electronic Switch Having Extended Voltage Range	Issued	Lattice Semiconductor Corporation
11/134,152	7009423	United States	Programmable I/O Interfaces For FPGAs And Other PLDs	Issued	Lattice Semiconductor Corporation
11/157,345	7685483	United States	Design-For-Test features for a memory in an FPGA	Issued	Lattice Semiconductor Corporation
11/157,349	7378879	United States	Decoding systems and methods	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/165,709	7256613	United States	Programmable Interconnect Architecture for PLDs	Issued	Lattice Semiconductor Corporation
11/165,853	7342838	United States	PLD With A Double Data Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
11/185,242	7519139	United States	Signal monitoring systems and methods	Issued	Lattice Semiconductor Corporation
11/187,179	7342846	United States	address decoding systems and methods	Issued	Lattice Semiconductor Corporation
11/187,114	7253674	United States	Fine output clock phase alignment circuitry	Issued	Lattice Semiconductor Corporation
11/189,067	7505752	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
11/194,871	7414913	United States	Bitline twisting scheme for a multiport memory	Issued	Lattice Semiconductor Corporation
11/194,356	7262630	United States	Dynamic programmable termination for parallel and differential schemes	Issued	Lattice Semiconductor Corporation
11/199,287	7599457	United States	clock-and-data-recovery system having a multi-phase clock generator for one or more channel circuits	Issued	Lattice Semiconductor Corporation
11/200,983	7295035	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/200,941	7411419	United States	I/O Systems and Methods	Issued	Lattice Semiconductor Corporation
11/202,149	7606851	United States	Correlator having user-defined processing	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/201,620	7187586	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/206,282	RE40311	United States	Zero Power Programmable Memory Cell	Issued	Lattice Semiconductor Corporation
11/226,695	7301182	United States	Circuit layout for improved performance while preserving or improving density	Issued	Lattice Semiconductor Corporation
11/230,087	7167405	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/235,616	7376037	United States	PLD with power-saving architecture	Issued	Lattice Semiconductor Corporation
11/236,967	7405446	United States	Electrostatic Protection Systems and Methods	Issued	Lattice Semiconductor Corporation
11/243,255	7088132	United States	Configuring FPGAs and the like using one or more serial memory devices	Issued	Lattice Semiconductor Corporation
11/251,682	7196963	United States	Address isolation for user-defined configuration memory in programmable devices	Issued	Lattice Semiconductor Corporation
11/252,094	7263024	United States	Clock reset address decoder for block memory	Issued	Lattice Semiconductor Corporation
11/252,126	7061275	United States	FPGA	Issued	Lattice Semiconductor Corporation
11/257,137	7685215	United States	Fast-carry arithmetic circuit using a multi-input LUT	Issued	Lattice Semiconductor Corporation
11/257,641	7317343	United States	PULSE-GENERATION CIRCUIT HAVING PULSE GENERATORS AND SET-RESET LATCHES	Issued	Lattice Semiconductor Corporation
11/260,097	7212051	United States	Control signal generation for a low jitter switched-capacitor frequency synthesizer	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/281,651	7495495	United States	Digital I/O Timing Control	Issued	Lattice Semiconductor Corporation
11/287,720	7327159	United States	Interface Block Architectures	Issued	Lattice Semiconductor Corporation
11/290,205	7242634	United States	Pseudo-dynamic word-line driver	Issued	Lattice Semiconductor Corporation
11/293,941	7538574	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor Corporation
11/302,097	7620839	United States	Jitter Tolerant Delay-Locked Loop Circuit	Issued	Lattice Semiconductor Corporation
11/300,886	7495467	United States	Temperature independent, linear on-chip termination resistance	Issued	Lattice Semiconductor Corporation
11/332,986	7382169	United States	Systems and Methods for Reducing Static Phase Error	Issued	Lattice Semiconductor Corporation
11/335,890	7439783	United States	Phase-Locked Loop Systems And Methods	Issued	Lattice Semiconductor Corporation
11/345,713	7547995	United States	dynamic over voltage protection scheme for interface circuitry	Issued	Lattice Semiconductor Corporation
11/346,817	7554357	United States	Efficient Configuration of Daisy-Chained Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
11/350,436	7375549	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
11/356,805	7277348	United States	Memory Cell Comprising And OTP NV Memory Unit And SRAM Unit	Issued	Lattice Semiconductor Corporation
11/360,337	7355441	United States	PLD with distributed memory and non-volatile memory	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/361,584	7596744	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
11/362,289	7759926	United States	dynamic phase offset measurement	Issued	Lattice Semiconductor Corporation
11/361,643	7446573	United States	Comparator Systems And Methods	Issued	Lattice Semiconductor Corporation
11/398,437	7459931	United States	PLDs with transparent field reconfiguration	Issued	Lattice Semiconductor Corporation
11/397,985	7554358	United States	PLDs with user non-volatile memory	Issued	Lattice Semiconductor Corporation
11/416,881	7623378	United States	Selective programming of non-volatile memory facilitated by security fuses	Issued	Lattice Semiconductor Corporation
11/435,956	7102934	United States	Sense Amplifier Systems and Methods	Issued	Lattice Semiconductor Corporation
11/442,186	7411417	United States	Selective loading of configuration data into configuration memory cells	Issued	Lattice Semiconductor Corporation
11/446,548	7378873	United States	PLD providing a serial peripheral interface	Issued	Lattice Semiconductor Corporation
11/445,620	7378872	United States	PLD architecture with multiple slice types	Issued	Lattice Semiconductor Corporation
11/446,542	7385417	United States	Dual slice architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,351	7397276	United States	Logic block control architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/446,308	7546498	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/446,309	7495970	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/447,591	7631223	United States	PLD methods and systems for providing multi-boot configuration data support	Issued	Lattice Semiconductor Corporation
11/452,714	7463060	United States	PLD and method of testing	Issued	Lattice Semiconductor Corporation
11/455,315	7215139	United States	Upgradeable And Reconfigurable Programmable Logic Device	Issued	Lattice Semiconductor Corporation
11/425,273	7702100	United States	Key generation for advanced encryption standard (AES) decryption and the like	Issued	Lattice Semiconductor Corporation
11/425,881	7657773	United States	Clock distribution chip for generating both zero-delay and non-zero-delay clock signals	Issued	Lattice Semiconductor Corporation
11/477,759	7348914	United States	Methods and systems to align output signals of an analog-to-digital converter	Issued	Lattice Semiconductor Corporation
11/487,647	7636259	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
11/487,751	7512015	United States	Negative voltage blocking for embedded memories	Issued	Lattice Semiconductor Corporation
11/492,687	7466190	United States	Charge pump with four-well transistors	Issued	Lattice Semiconductor Corporation
11/494,862	7521969	United States	Switch sequencing circuit systems and methods	Issued	Lattice Semiconductor Corporation
11/461,222	7411432	United States	Integrated circuits and complementary CMOS circuits for frequency dividers	Issued	Lattice Semiconductor Corporation
11/498,645	7675313	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/498,646	7605606	United States	Area efficient routing architectures for PLDs	Issued	Lattice Semiconductor Corporation
11/530,620	7456672	United States	Clock systems and methods	Issued	Lattice Semiconductor Corporation
11/533,188	7511641	United States	Efficient bitstream compression	Issued	Lattice Semiconductor Corporation
11/551,459	7831754	United States	Multiple Communication Channel Configuration Systems And Methods	Issued	Lattice Semiconductor Corporation
11/556,528	7663401	United States	Multiplexer initialization systems and methods	Issued	Lattice Semiconductor Corporation
11/593,274	7535258	United States	Programmable Voltage LVDS Output Buffer	Issued	Lattice Semiconductor Corporation
11/557,808	7725803	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation
11/638,156	7429875	United States	Low Static Current Drain Logic Circuit	Issued	Lattice Semiconductor Corporation
11/643,288	7443192	United States	Output buffer with digital slew control	Issued	Lattice Semiconductor Corporation
11/624,021	7623391	United States	Data transfer verification systems and methods	Issued	Lattice Semiconductor Corporation
11/671,948	7576563	United States	Flexible High Fan-out Signal Routing Systems and Methods	Issued	Lattice Semiconductor Corporation
11/675,246	7313025	United States	Flash memory erase verification systems and methods	Issued	Lattice Semiconductor Corporation
11/676,071	7430706	United States	Fast diagonal interleaved parity (DIP) calculator	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/680,526	7598765	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
11/691,003	7536615	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/691,040	7743296	United States	Logic analyzer systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/737,702	7509598	United States	Clock Boosting Systems and Methods	Issued	Lattice Semiconductor Corporation
11/750,790	7401280	United States	Self-verification of configuration memory in PLDs	Issued	Lattice Semiconductor Corporation
11/750,616	7632011	United States	Integrated Circuit Temperature Sensors Systems and Methods	Issued	Lattice Semiconductor Corporation
11/760,411	8065574	United States	Real Soft Error Detect Scheme for Testing	Issued	Lattice Semiconductor Corporation
11/761,221	7570078	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
11/778,457	7573770	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
11/779,246	7446679	United States	FPGA data compression using combined RLE BE, LZ, Row LZ and BE ROW encoding	Issued	Lattice Semiconductor Corporation
11/863,016	7681160	United States	Weight based look up table collapsing for programmable logic devices	Issued	Lattice Semiconductor Corporation
11/865,556	7539076	United States	Variable data width memory systems and methods	Issued	Lattice Semiconductor Corporation
11/869,019	7616029	United States	Hysteresis-based processing for applications such as signal bias monitors	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/872,950	7586344	United States	Dynamic delay or advance adjustment of oscillating signal phase	Issued	Lattice Semiconductor Corporation
11/875,748	7757198	United States	Scan chain systems and methods for PLDs	Issued	Lattice Semiconductor Corporation
11/877,434	7411414	United States	Single-Ended Output Driver Buffer	Issued	Lattice Semiconductor Corporation
11/924,088	8132040	United States	Channel-to-channel deskew systems and methods	Issued	Lattice Semiconductor Corporation
11/934,711	7573291	United States	Programmable Logic Device With Enhanced Logic Block Architecture	Issued	Lattice Semiconductor Corporation
11/937,328	7788620	United States	An IO placement systems and methods to reduce SSO noise	Issued	Lattice Semiconductor Corporation
11/937,300	7895555	United States	Simultaneous Switching Output Noise Estimation and Reduction Systems and Methods	Issued	Lattice Semiconductor Corporation
11/939,787	7863931	United States	Flexible Delay Cell Architecture	Issued	Lattice Semiconductor Corporation
11/941,031	7902865	United States	Compression and decompression of configuration data using repeated data frames	Issued	Lattice Semiconductor Corporation
11/941,006	7535253	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
11/947,662	7788623	United States	Composite wire indexing for PLDs	Issued	Lattice Semiconductor Corporation
11/949,130	7586325	United States	IC having independent voltage and process/temperature control	Issued	Lattice Semiconductor Corporation
12/001,600	7728625	United States	Serial interface for PLDs	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
11/957,598	7605609	United States	A programmable level shifter optimized for high performance and low power.	Issued	Lattice Semiconductor Corporation
11/959,329	7630259	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
11/970,212	7646643	United States	Process charging monitor for nonvolatile memory	Issued	Lattice Semiconductor Corporation
12/019,526	7787326	United States	PLD With Mult-Rate SDRAM Interface	Issued	Lattice Semiconductor Corporation
12/021,202	8069329	United States	Dynamic Multiple Pattern Configuration Scheme For Volatile FPGAs	Issued	Lattice Semiconductor Corporation
12/044,842	7652500	United States	Reconfiguration of PLDs	Issued	Lattice Semiconductor Corporation
12/055,170	7890913	United States	Wire Mapping For PLDs	Issued	Lattice Semiconductor Corporation
12/060,776	7459935	United States	PLD With Distributed Memory	Issued	Lattice Semiconductor Corporation
12/061,885	7831856	United States	Detection of Timing Errors in Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/099,933	7661878	United States	On-Chip Temperature Sensor For An Integrated Circuit	Issued	Lattice Semiconductor Corporation
12/100,859	7558143	United States	Programmable Logic Device With Power-Saving Architecture	Issued	Lattice Semiconductor Corporation
12/105,146	7557606	United States	Synchronization Of Data Signals And Clock Signals For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/105,959	7696784	United States	PLD With Multiple Slice	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Types		Corporation
12/107,883	7560953	United States	Power Management Systems And Methods for PLDs	Issued	Lattice Semiconductor Corporation
12/122,489	7897448	United States	Formation Of High Voltage Transistor With High Breakdown Voltage	Issued	Lattice Semiconductor Corporation
12/146,042	8463832	United States	Digital Signal Processing Block Architecture For PLD	Issued	Lattice Semiconductor Corporation
12/164,265	7592834	United States	Logic Block Control Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/182,940	8261160	United States	Serial data recovery out of 8 samples with FPGAs	Issued	Lattice Semiconductor Corporation
12/186,027	7579865	United States	Selective Loading Of Configuration Data Into Configuration Memory Cells	Issued	Lattice Semiconductor Corporation
12/188,120	7605602	United States	Low-Power Output Driver Buffer Circuit	Issued	Lattice Semiconductor Corporation
12/238,959	7911229	United States	Programmable Signal Routing Systems	Issued	Lattice Semiconductor Corporation
12/273,868	7663419	United States	Clock Systems And Methods	Issued	Lattice Semiconductor Corporation
12/277,217	8112731	United States	Congestion-driven placement based on region interconnection for FPGA	Issued	Lattice Semiconductor Corporation
12/323,974	7992120	United States	congestion estimation based on pass probability net estimation process	Issued	Lattice Semiconductor Corporation
12/327,128	7656193	United States	Programmable Logic Device And Method Of Testing	Issued	Lattice Semiconductor Corporation
12/337,502	8856718	United States	Precise Congestion Estimation for FPGA Router	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/341,929	8181139	United States	Multi-Priority Placement	Issued	Lattice Semiconductor Corporation
12/370,039	7714608	United States	Temperature-Independent, Linear On-Chip Termination Resistance	Issued	Lattice Semiconductor Corporation
12/389,149	7957208	United States	Flexible memory architectures for PLDs	Issued	Lattice Semiconductor Corporation
12/402,751	7844243	United States	Receiver used for differential signaling and reference voltage signaling with programmable common mode	Issued	Lattice Semiconductor Corporation
12/406,772	8069431	United States	An alternative method for pin swapping in FPGA routing	Issued	Lattice Semiconductor Corporation
12/408,047	8086986	United States	Clock Boosting Systems And Methods	Issued	Lattice Semiconductor Corporation
12/409,757	7675321	United States	Dual-Slice Architectures For PLDs	Issued	Lattice Semiconductor Corporation
12/413,787	7808405	United States	Efficient Bitstream Compression	Issued	Lattice Semiconductor Corporation
12/430,848	7741865	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/464,822	7876125	United States	Method of Retaining Register Data during Field Update of PLD	Issued	Lattice Semiconductor Corporation
12/465,444	7868654	United States	Economical way to improve volatile FPGA boot up data throughput by utilizing one or more SPI boot PROMs w/o sacrificing additional FPGA pins	Issued	Lattice Semiconductor Corporation
12/467,800	7737723	United States	Transparent Field Reconfiguration for PLDs	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
12/476,155	8044682	United States	FPGA Having Low Power, Fast Carry Chain	Issued	Lattice Semiconductor Corporation
12/480,565	7702977	United States	PLDs with custom identification systems and methods	Issued	Lattice Semiconductor Corporation
12/494,822	8165164	United States	Circuit For In-System Reconfigurable Mapping Of IQ Data Into A CPRI Basic Frame	Issued	Lattice Semiconductor Corporation
12/502,141	7724029	United States	Power Management For Integrated Circuits Such As Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
12/511,388	7768300	United States	PLD Providing A Serial Peripheral Interfaces	Issued	Lattice Semiconductor Corporation
12/512,944	8255733	United States	Method of selecting precise delay or skew shifts	Issued	Lattice Semiconductor Corporation
12/512,961	7969248	United States	VCO digital center frequency coarse tune algorithm	Issued	Lattice Semiconductor Corporation
12/538,810	7808855	United States	Distributed front-end FIFO for source-synchronized interfaces with non-continuous clocks	Issued	Lattice Semiconductor Corporation
12/561,140	8010871	United States	Auto recovery from volatile soft error upsets (SEUs)	Issued	Lattice Semiconductor Corporation
12/564,781	7746107	United States	Redundancy for Configuration RAM	Issued	Lattice Semiconductor Corporation
12/578,470	8122277	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation
12/578,492	8112656	United States	Clock distribution chip	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/607,868	7989911	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/607,333	7985656	United States	STI with trench liner of increased thickness	Issued	Lattice Semiconductor Corporation
12/611,262	8059470	United States	Flash memory array with independently erasable sectors	Issued	Lattice Semiconductor Corporation
12/626,289	7944765	United States	PLD with built in self test	Issued	Lattice Semiconductor Corporation
12/630,163	8060784	United States	PLD And Methods For Providing Multi-Boot Configuration Data Support	Issued	Lattice Semiconductor Corporation
12/637,884	8200179	United States	Combined Variable Gain Amplifier And Linear Equalizer With Independent Gain And Frequency Control	Issued	Lattice Semiconductor Corporation
12/698,283	8040152	United States	IO Ring Configuration Scheme with sharing of BC7 register	Issued	Lattice Semiconductor Corporation
12/706,227	7924054	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
12/709,685	7834652	United States	Methods and systems for storing a security key using programmable fuses	Issued	Lattice Semiconductor Corporation
12/729,952	8040159	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
12/752,455	8384427	United States	Serial Peripheral Interface Daisy Chaining using a Flow-Through Option	Issued	Lattice Semiconductor Corporation
12/757,087	8664774	United States	A Method for Arranging IC Bondwires for the Reduction of Crosstalk	Issued	Lattice Semiconductor Corporation
12/786,359	8108754	United States	PLD programming verification systems and methods	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/813,540	8164499	United States	Shared-Array Multiple-Output Digital to Analog Converter	Issued	Lattice Semiconductor Corporation
12/813,573	8441292	United States	Method of delaying data from clock in 1UI steps	Issued	Lattice Semiconductor Corporation
12/818,544	7868646	United States	Soft Error Upset Hardened Integrated Circuit Systems And Methods	Issued	Lattice Semiconductor Corporation
12/871,764	8286116	United States	Composite Wire Indexing For PLDs	Issued	Lattice Semiconductor Corporation
12/977,011	8522126	United States	Method Of Blocking PLC Distributed SRAM Readback In User Mode	Issued	Lattice Semiconductor Corporation
12/976,412	8351287	United States	Bitline Floating Circuit For Power Reduction On SRAM Array	Issued	Lattice Semiconductor Corporation
12/976,520	8477549	United States	Strobed And Latched Readback Of SRAM Bits In A FPGA	Issued	Lattice Semiconductor Corporation
12/987,393	8274412	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/006,622	8384428	United States	Programmable IO Pad - embedded function block	Issued	Lattice Semiconductor Corporation
13/007,804	8248136	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/007,688	8324934	United States	Programmable Ratio Input Buffer	Issued	Lattice Semiconductor Corporation
13/026,555	8104009	United States	Wire Mapping For Programmable Logic Devices	Issued	Lattice Semiconductor Corporation
13/034,174	8058898	United States	Compression and Decompression Of Configuration Data Using	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Repeated Data Frames		
13/038,259	8368424	United States	Wakeup from sleep mode using slave I2C port or slave SPI port with powered down core logic	Issued	Lattice Semiconductor Corporation
13/038,270	8816718	United States	Slow Respond Mode Protocol For Synchronous Read	Issued	Lattice Semiconductor Corporation
13/037,703	8654600	United States	Current Sense Amplifier With Low Voltage Operation	Issued	Lattice Semiconductor Corporation
13/052,142	8553463	United States	Positive-To-Negative Voltage Discharge Circuit	Issued	Lattice Semiconductor Corporation
13/076,300	8319521	United States	Safe programming of key information into NV memory	Issued	Lattice Semiconductor Corporation
13/079,578	8314634	United States	Power Saving Standby Mode With Glitch-Less Output Controls	Issued	Lattice Semiconductor Corporation
13/079,595	8531222	United States	PLL Switchable Feedback Loops Among Internal And External Feedback Paths	Issued	Lattice Semiconductor Corporation
13/083,889	8138790	United States	Latency measurement circuit for wireless communications applications	Issued	Lattice Semiconductor Corporation
13/154,885	8441284	United States	Flexible Way To Incrementally Update Multi-Bit Data Registers	Issued	Lattice Semiconductor Corporation
13/155,547	8547075	United States	Filter And Stability Capacitor Reuse For On-Chip Dual Output Voltage Regulators	Issued	Lattice Semiconductor Corporation
13/164,108	8555217	United States	Cross-Probing Technology Between Software Plug-In Modules	Issued	Lattice Semiconductor Corporation
13/178,599	8539409	United States	Multiple silicon products from a common base set of masks	Issued	Lattice Semiconductor Corporation
13/178,536	8495264	United States	Packet And Control Symbol	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Alignment Circuit For SRIO		Corporation
13/193,984	8314632	United States	Placing ICs Into Ultra-Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/212,121	8451679	United States	Bit-Line Clamping Circuit To Improve Write Performance Of Dual-Port SRAM	Issued	Lattice Semiconductor Corporation
13/275,102	8169237	United States	High Speed Comparator with Data Dependent Jitter Mitigation	Issued	Lattice Semiconductor Corporation
13/299,507	8370691	United States	Testing of Soft Error Detection Logic For PLDs	Issued	Lattice Semiconductor Corporation
13/452,060	8823561	United States	In-System Reconfigurable Circuit For Mapping Data Words Of Different Lengths	Issued	Lattice Semiconductor Corporation
13/585,142	8461894	United States	Low Power And Glitch-less Delay Element For High Speed Receiver Interface	Issued	Lattice Semiconductor Corporation
13/616,173	8912933	United States	Low Power SerDes With Built- In Word Alignment For Odd And Even Gearing Ratios	Issued	Lattice Semiconductor Corporation
13/653,827	8710898	United States	Bandgap Reference Circuit Design With Triple-Trim Methodology For Mass Production	Issued	Lattice Semiconductor Corporation
13/680,947	8643398	United States	Placing ICs Into Low Voltage Mode For Standby Purposes	Issued	Lattice Semiconductor Corporation
13/685,385	8643168	United States	Input Capacitance Compensation In Package	Issued	Lattice Semiconductor Corporation
13/721,867	8686773	United States	In-System Margin Measurement Circuit	Issued	Lattice Semiconductor Corporation
13/738,265	8797064	United States	Low power, optimized H-bridge and CML driver	Issued	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/764,221	RE45200	United States	Programmable Signal Routing Systems Having Low Static Leakage	Issued	Lattice Semiconductor Corporation
13/857,919	8786482	United States	Analog-To-Digital-Converter	Issued	Lattice Semiconductor Corporation
13/892,948	8648636	United States	Method of Delaying Data from Clock in 1UI steps	Issued	Lattice Semiconductor Corporation
14/040,955	8829944	United States	Dynamic Power Supply Switching For Clock Signals	Issued	Lattice Semiconductor Corporation
13/155,261		United States	JTAG Based Parallel Measuring And Trimming for Time Based Parameters	Pending	Lattice Semiconductor Corporation
13/412,408		United States	Double Rate Throughput Processing Booster For DSP Slices	Pending	Lattice Semiconductor Corporation
13/466,463		United States	Early Match FIFO	Pending	Lattice Semiconductor Corporation
13/681,782		United States	Multi-channel transmitter synchronization circuitry	Pending	Lattice Semiconductor Corporation
13/777,243		United States	RAM Data Path Sense Leakage Abatement Circuit	Pending	Lattice Semiconductor Corporation
13/858,422		United States	Method To Enable And Disable Scan Test Mode Reliably Through JTAG Port With Maximum Scan Coverage	Pending	Lattice Semiconductor Corporation
13/868,738		United States	Loss of signal detection in high-speed serial link	Pending	Lattice Semiconductor Corporation
13/901,853		United States	Dual-Port SRAM With Bit Line Clamping	Pending	Lattice Semiconductor Corporation
13/904,861		United States	Bring up sequence for configurable PCIe IP in an	Pending	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			FPGA		Corporation
13/947,553		United States	Method For Hot Swapping Or Hot Plugging With Stable Supply-Side Reference Over Wide Voltage Range	Pending	Lattice Semiconductor Corporation
14/021,513		United States	Phase Locked Loop Circuit With Selectable Feedback Paths	Pending	Lattice Semiconductor Corporation
14/043,920		United States	Robust Serialized State-machine Interface Architecture Optimized for Implementation in Programmable Devices	Pending	Lattice Semiconductor Corporation
14/053,026		United States	ASB SW modeling methodology	Pending	Lattice Semiconductor Corporation
14/070,975		United States	Method to enable system board pin escape for tight ball pitch packages	Pending	Lattice Semiconductor Corporation
14/095,310		United States	A Novel ESD Implementation for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/136,482		United States	Automatic Quadrant Clock Assignment For Programmable Logic Devices	Pending	Lattice Semiconductor Corporation
14/137,443		United States	Using Critical Groups in FPGA Routing	Pending	Lattice Semiconductor Corporation
14/147,796		United States	A Hot Socket Implementation for General Purpose IO for 40nm FPGA	Pending	Lattice Semiconductor Corporation
14/172,678		United States	All Mosfet Circuit for Generating Accurate Collector Currents	Pending	Lattice Semiconductor Corporation
14/179,651		United States	LOW-VOLTAGE CURRENT SENSE AMPLIFIER	Pending	Lattice Semiconductor Corporation
14/194,484		United States	Logic Element Placement with Repacking Optimization	Pending	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/220,377		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/223,096		United States	DPHY using FPGA differential & single ended I/Os	Pending	Lattice Semiconductor Corporation
14/245,920		United States	Deterministic Dynamic Element Matching for Generating Precise Current Ratios	Pending	Lattice Semiconductor Corporation
14/271,331		United States	Inline Defect To Sort Test Correlation In Semiconductor Manufacturing	Pending	Lattice Semiconductor Corporation
14/271,955		United States	Performance-focused Adaptive Automatic Incremental Flow	Pending	Lattice Semiconductor Corporation
14/283,329		United States	Configuration logic controlled memory BIST (built-in self-test) for back-to-back initialization and readback of embedded block RAMs in FPGAs	Pending	Lattice Semiconductor Corporation
14/308,747		United States	A novel Output Driver drive strength and termination resistor continuously calibrating PVT compensation scheme	Pending	Lattice Semiconductor Corporation
14/313,443		United States	FPGA Hardware debug during post-config power-up and before logic analyzer connect	Pending	Lattice Semiconductor Corporation
14/313,778		United States	IOLOGIC Delay Cell Stealing for Holdtime Correction	Pending	Lattice Semiconductor Corporation
14/316,049		United States	Mapping Constant Multipliers To ICE Devices	Pending	Lattice Semiconductor Corporation
14/319,481		United States	Incrementer Absorption into Multiplier Logic	Pending	Lattice Semiconductor Corporation
14/320,169		United States	Method to Implement Mixed-	Pending	Lattice

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Width Mode Memory in Fixed-Mode Memory Architecture with Masking		Semiconductor Corporation
14/320,074		United States	Two Level Voltage Regulator scheme for SRAM Operation	Pending	Lattice Semiconductor Corporation
14/327,811		United States	Implementing Dual Boot For XO2 and Multiple ASCs	Pending	Lattice Semiconductor Corporation
14/339,164		United States	A unique method to optimize clock to out path	Pending	Lattice Semiconductor Corporation
14/339,229		United States	New method on bus-based clock_to_out timing optimization	Pending	Lattice Semiconductor Corporation
14/482,001		United States	Physically-aware Programmable Multiport Memory BIST with on-the-fly ATE-configurable memory tests	Pending	Lattice Semiconductor Corporation
14/509,564		United States	Dont-care based mux absorption into ice40 carry chain	Pending	Lattice Semiconductor Corporation
14/525,240		United States	Level shifter that eliminates static power dissipation	Pending	Lattice Semiconductor Corporation
14/535,454		United States	Low power and high performance class AB amplifier control common mode in SerDes Transmitter	Pending	Lattice Semiconductor Corporation
14/535,351		United States	ICO metastability prevention during start-up	Pending	Lattice Semiconductor Corporation
14/558,851		United States	Low Power and Flexible TX FFE With Programmable Tap Positions And Coefficients Driver Architecture	Pending	Lattice Semiconductor Corporation
14/576,348		United States	Reconfigurable and Scalable Hardware Management Architecture	Pending	Lattice Semiconductor Corporation

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/576,245		United States	Methodology that allows multiple hardware or hardware-software controllers with different bus interfaces to share a common resource	Pending	Lattice Semiconductor Corporation
14/604,515		United States	Enhancement of FPGA hardware debugger to be used as a design controller/exerciser with user registers	Pending	Lattice Semiconductor Corporation
14/609,181		United States	Algorithm to Optimize Hot Swapping	Pending	Lattice Semiconductor Corporation
14/610,074		United States	Ripple Mode using 3-LUT for Generate	Pending	Lattice Semiconductor Corporation
14/610,127		United States	Combine OFX with LUT output and SUM into a single output to reduce number of signals to routing block	Pending	Lattice Semiconductor Corporation
14/611,069		United States	High speed complementary NMOS LUT logic	Pending	Lattice Semiconductor Corporation
14/611,095		United States	Shared Logic for Multiple Registers with asynchronous initialization with preload	Pending	Lattice Semiconductor Corporation
11/949,454	7,427,874	United States	Interface block architectures	Issued	Lattice Semiconductor Corporation
11/676,196	7,327,160	United States	SERDES with programmable I/O architecture	Issued	Lattice Semiconductor Corporation
6,786,564	6,786,564	United States	Inkjet printer, drive method and drive device for same	Issued	Lattice Semiconductor Corporation
11/839,107	7,856,050	United States	Receiver and transmitter calibration to compensate for frequency dependent I/Q imbalance	Issued	Lattice Semiconductor Corporation
07/679,370	5,255,221	United States	Fully configurable versatile field programmable function	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			element		Corporation
06/551,735	4,642,797	United States	High speed first-in-first-out memory	Issued	Lattice Semiconductor Corporation
08/042,533	5,394,037	United States	Sense amplifiers and sensing methods	Issued	Lattice Semiconductor Corporation
08/115,533	5,404,055	United States	Input routing pool	Issued	Lattice Semiconductor Corporation
08/115,723	5,394,033	United States	Structure and method for implementing hierarchical routing pools in a programmable logic circuit	Issued	Lattice Semiconductor Corporation
08/342,675	5,506,517	United States	Output enable structure and method for a programmable logic device	Issued	Lattice Semiconductor Corporation
07/911,841	5,357,156	United States	Active clamp circuit scheme for CMOS devices	Issued	Lattice Semiconductor Corporation
08/179,887	5,886,378	United States	Single polysilicon layer flash E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/853,453	5,231,316	United States	Temperature compensated CMOS voltage to current converter	Issued	Lattice Semiconductor Corporation
08/108,363	5,353,246	United States	Programmable semiconductor antifuse structure and method of fabricating	Issued	Lattice Semiconductor Corporation
07/785,442	5,281,906	United States	Tunable voltage reference circuit to provide an output voltage with a predetermined temperature coefficient independent of variation in supply voltage	Issued	Lattice Semiconductor Corporation
07/696,453	5,251,169	United States	Non-volatile erasable and programmable interconnect cell	Issued	Lattice Semiconductor Corporation
07/538,211	5,255,203	United States	Interconnect structure for programmable logic device	Issued	Lattice Semiconductor

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
					Corporation
08/106,263	5,412,260	United States	Multiplexed control pins for in-system programming and boundary scan state machines in a high density programmable logic device	Issued	Lattice Semiconductor Corporation
08/033,934	5,418,390	United States	Single polysilicon layer E.sup.2 PROM cell	Issued	Lattice Semiconductor Corporation
07/993,711	5,452,229	United States	Programmable integrated-circuit switch	Issued	Lattice Semiconductor Corporation
07/957,311	5,329,179	United States	Arrangement for parallel programming of in-system programmable IC logical devices	Issued	Lattice Semiconductor Corporation
07/288,945	4,896,296	United States	Programmable logic device configurable input/output cell	Issued	Lattice Semiconductor Corporation
06/882,602	4,887,239	United States	One-time programmable data security system for programmable logic device	Issued	Lattice Semiconductor Corporation
06/871,063	4,766,569	United States	Programmable logic array	Issued	Lattice Semiconductor Corporation
06/862,815	4,879,688	United States	In-system programmable logic device	Issued	Lattice Semiconductor Corporation
06/707,670	4,833,646	United States	Programmable logic device with limited sense currents and noise reduction	Issued	Lattice Semiconductor Corporation
07/236,348	4,852,044	United States	Programmable data security circuit for programmable logic device	Issued	Lattice Semiconductor Corporation
11/400,924	7411424	United States	Programmable logic function generator using non-volatile programmable memory switches	Issued	Lattice Semiconductor Corporation
13/403,146		United States	Surface Mountable Integrated Circuit Packaging Scheme	Pending	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/242,665		United States	High Speed Integrated Circuit Interface	Pending	SiBEAM, Inc.
14/196,978		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
14/474,005		United States	Inter-Device Conflict Resolution on a Multimedia Link	Pending	Silicon Image, Inc.
61/989,417		United States	Control Target Selection	Pending	Silicon Image, Inc.
61/988,812		United States	Lip Sync Delay Compensation	Pending	Silicon Image, Inc.
61/989,415		United States	Streaming Data and Metadata Synchronization	Pending	Silicon Image, Inc.
61/991,126		United States	Stream Creation with Limited Topology Information	Pending	Silicon Image, Inc.
61/989,411		United States	Topology Discovery	Pending	Silicon Image, Inc.
14/463,146		United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.
14/578,266		United States	Control Target Selection	Pending	Silicon Image, Inc.
14/578,257		United States	System for Dynamic Audio Visual Capabilities Exchange	Pending	Silicon Image, Inc.
62/089,767		United States	High-Bandwidth Digital Content Protection over Audio Return Channel	Pending	Silicon Image, Inc.
12/573,492	8482462	United States	MULTI-ANTENNA BEAM-FORMING SYSTEM FOR TRANSMITTING CONSTANT ENVELOPE SIGNALS DECOMPOSED FROM A VARIABLE ENVELOPE SIGNAL	Issued	Silicon Image, Inc.
12/678,463	8207892	United States	TECHNIQUE FOR DETERMINING AN ANGLE OF ARRIVAL IN A COMMUNICATION SYSTEM	Issued	Silicon Image, Inc.

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/675,269	8374558	United States	ANTENNA ARRAY WITH FLEXIBLE INTERCONNECT FOR A MOBILE WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/333,134	8213872	United States	TECHNIQUE FOR LOW-POWER OPERATION OF A WIRELESS DEVICE	Issued	Silicon Image, Inc.
12/933,876	8256123	United States	DISPLACEMENT SENSING USING A FLEXIBLE SUBSTRATE	Issued	Silicon Image, Inc.
14/196,993		United States	Calibration of Single-Ended High-Speed Interfaces	Pending	Silicon Image, Inc.
13/988,047		United States	INTEGRATED PHASE-SHIFTING-AND-COMBINING CIRCUITRY TO SUPPORT MULTIPLE ANTENNAS	Pending	Silicon Image, Inc.
14/002,353		United States	TRACKING SYSTEM WITH ORTHOGONAL POLARIZATIONS AND A RETRO-DIRECTIVE ARRAY	Pending	Silicon Image, Inc.
13/726,822		United States	HIGH-ACCURACY DETECTION IN COLLABORATIVE TRACKING SYSTEMS	Pending	Silicon Image, Inc.
13/859,764		United States	ANTENNA SELECTION AND PILOT COMPRESSION IN MIMO SYSTEMS	Pending	Silicon Image, Inc.
62/100,841		United States	I/Q Imbalance Correction for the Combination of Multiple Radio Frequency Frontends	Pending	Silicon Image, Inc.
12/532,107	8571126	United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Issued	Silicon Image, Inc.
14/065,420		United States	MULTI-ANTENNA TRANSMITTER FOR MULTI-TONE SIGNALING	Pending	Silicon Image, Inc.
12/679,764	8605823	United States	COMMUNICATION USING	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			CONTINUOUS-PHASE MODULATED SIGNALS		Inc.
14/101,274		United States	COMMUNICATION USING CONTINUOUS-PHASE MODULATED SIGNALS	Pending	Silicon Image, Inc.
12/746,526	8484277	United States	TRANSFORMING SIGNALS USING PASSIVE CIRCUITS	Issued	Silicon Image, Inc.
13/498,884	8610474	United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED MET	Issued	Silicon Image, Inc.
14/089,094		United States	SIGNAL DISTRIBUTION NETWORKS AND RELATED METHODS	Pending	Silicon Image, Inc.
13/519,302		United States	Phase Detection Circuits and Methods	Pending	Silicon Image, Inc.
13/574,586	8795082	United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Issued	Silicon Image, Inc.
14/331,144		United States	DIRECTIONAL BEAM STEERING SYSTEM AND METHOD TO DETECT LOCATION AND MOTION	Pending	Silicon Image, Inc.
13/704,564		United States	Methods and Systems for Near-Field MIMO Communications	Pending	Silicon Image, Inc.
14/235,783		United States	HIGH-ACCURACY AND LOW-POWER TRACKING SYSTEM FOR MOBILE DEVICES	Pending	Silicon Image, Inc.
14/234,623		United States	LOW-COST TRACKING SYSTEM	Pending	Silicon Image, Inc.
14/240,405		United States	CALIBRATING A RETRO-DIRECTIVE ARRAY FOR AN ASYMMETRIC WIRELESS LINK	Pending	Silicon Image, Inc.
14/364,002		United States	COLLABORATIVE CHANNEL SOUNDING IN MULTI-ANTENNA	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			SYSTEMS		
08/815,486	6,157,360	United States	System And Method For Driving Columns Of An Active Matrix Display	Issued	Silicon Image, Inc.
08/920,336	5,955,929	United States	Voltage-Controlled Oscillator Resistant To Supply Voltage Noise	Issued	Silicon Image, Inc.
09/007,707	5,969,552	United States	Dual Loop Delay-Locked Loop	Issued	Silicon Image, Inc.
09/298,647	6,259,427	United States	Scaling Multi-Dimensional Signals Using Variable Weighting Factors	Issued	Silicon Image, Inc.
09/298,369	6,374,361	United States	Skew-Insensitive Low Voltage Differential Receiver	Issued	Silicon Image, Inc.
09/393,849	6,738,417	United States	Method And Apparatus For Bidirectional Data Transfer Between A Digital Display And A Computer	Issued	Silicon Image, Inc.
09/326,503	6,940,496	United States	Display Module Driving System And Digital To Analog Converter For Driving Display	Issued	Silicon Image, Inc.
09/392,229	6,564,269	United States	Bi-Directional Data Transfer Using The Video Blanking Period In A Digital Data Stream	Issued	Silicon Image, Inc.
09/393,234	6,307,543	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/947,008	6,492,984	United States	Bi-Directional Data Transfer Using Two Pair Of Differential Lines As A Single Additional Differential Pair	Issued	Silicon Image, Inc.
09/759,624	6,891,910	United States	Baud-Rate Timing Recovery	Issued	Silicon Image, Inc.
09/574,571	6,326,826	United States	Wide Frequency-Range Delay- Locked Loop Circuit	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/881,271	6,954,491	United States	Methods And Systems For Sending Side-Channel Data During Data Inactive Period	Issued	Silicon Image, Inc.
09/922,990	6,961,095	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
11/219,323	7,557,863	United States	Digital Display Jitter Correction Apparatus And Method	Issued	Silicon Image, Inc.
09/989,587	6,717,478	United States	Multi-Phase Voltage Controlled Oscillator (VCO) With Common Mode Control	Issued	Silicon Image, Inc.
10/371,220	7,231,009	United States	Data Synchronization Across An Asynchronous Boundary Using, For Example, Multi-Phase Clocks	Issued	Silicon Image, Inc.
09/989,580	7,103,013	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
11/441,669	7,599,316	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
12/573,847	8,116,240	United States	Bi-Directional Bridge Circuit Having High Common Mode Rejection And High Input Sensitivity	Issued	Silicon Image, Inc.
10/045,297	7,257,129	United States	Memory Architecture With Multiple Serial Communications Ports	Issued	Silicon Image, Inc.
11/828,286	7,903,684	United States	Communications Architecture For Transmission Of Data Between Memory Bank Caches And Ports	Issued	Silicon Image, Inc.
09/167,527	6,380,978	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.
10/032,136	7,215,376	United States	Digital Video System And Methods For Providing Same	Issued	DVDO, INC. and Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/942,740	7,359,624	United States	Portable DVD Player	Issued	Silicon Image, Inc.
09/372,713	6,489,998	United States	Method And Apparatus For Deinterlacing Digital Video	Issued	Silicon Image, Inc.
09/941,949	6,909,469	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
10/251,642	7,027,099	United States	Method And Apparatus For Deinterlacing Digital Video Images	Issued	Silicon Image, Inc.
11/054,748	7,391,481	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
11/357,364	7,499,103	United States	Method And Apparatus For Detecting Frequency In Digital Video Images	Issued	Silicon Image, Inc.
11/932,808	7,633,559	United States	Interlace Motion Artifact Detection Using Vertical Frequency Detection And Analysis	Issued	Silicon Image, Inc.
09/410,543	6,700,622	United States	Method And Apparatus For Detecting The Source Format Of Video Images	Issued	Silicon Image, Inc.
09/396,993	6,515,706	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
10/191,764	6,829,013	United States	Method And Apparatus For Detecting And Smoothing Diagonal Features In Video Images	Issued	Silicon Image, Inc.
09/363,312	6,681,059	United States	Method And Apparatus For Efficient Video Scaling	Issued	Silicon Image, Inc.
09/359,530	6,587,158	United States	Method And Apparatus For Reducing On-Chip Memory In Vertical Video Processing	Issued	Silicon Image, Inc.
09/226,776	6,219,747	United States	Methods And Apparatus For Variable Length SDRAM	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Transfers		
09/805,588	6,385,692	United States	Methods and Apparatus for Variable Length SDRAM Transfers	Issued	Silicon Image, Inc.
09/227,502	6,393,505	United States	Methods And Apparatus For Data Bus Arbitration	Issued	Silicon Image, Inc.
09/226,381	6,473,476	United States	Method And Apparatus For Providing Deterministic Resets For Clock Divider Systems	Issued	Silicon Image, Inc.
09/837,894	6,867,814	United States	Method, System And Article Of Manufacture For Identifying The Source Type And Quality Level Of A Video Sequence	Issued	Silicon Image, Inc.
09/478,122	7,203,557	United States	Audio Signal Delay Apparatus And Method	Issued	Silicon Image, Inc.
10/663,413	7,408,992	United States	Detection And Repair Of MPEG-2 Chroma Upconversion Artifacts	Issued	Silicon Image, Inc.
09/905,318	7,123,307	United States	Clock Jitter Limiting Scheme In Video Transmission Through Multiple Stages	Issued	Silicon Image, Inc.
09/905,615	6,944,804	United States	System And Method For Measuring Pseudo Pixel Error Rate	Issued	Silicon Image, Inc.
09/904,783	6,625,560	United States	Method Of Testing Serial Interface	Issued	Silicon Image, Inc.
09/989,590	6,845,461	United States	High-Speed Bus With Embedded Clock Signals	Issued	Silicon Image, Inc.
09/989,645	6,809,567	United States	System And Method For Multiple-Phase Clock Generation	Issued	Silicon Image, Inc.
09/905,511	7,062,004	United States	Method And Apparatus For Adaptive Control Of PLL Loop Bandwidth	Issued	Silicon Image, Inc.
10/057,823	7,023,487	United States	Deinterlacing Of Video Sources Via Image Feature Edge Detection	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/954,663	7,558,326	United States	Method And Apparatus For Sending Auxiliary Data On A TMDS-Like Link	Issued	Silicon Image, Inc.
10/036,234	7,359,437	United States	Encoding Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/095,422	7,257,163	United States	Method And System For Reducing Inter-Symbol Interference Effects In Transmission Over A Serial Link With Mapping Of Each Word In A Cluster Of Received Words To A Single Transmitted Word	Issued	Silicon Image, Inc.
10/171,860	7,088,398	United States	Method And Apparatus For Regenerating A Clock For Auxiliary Data Transmitted Over A Serial Link With Video Data	Issued	Silicon Image, Inc.
10/192,296	6,914,637	United States	Method And System For Video And Auxiliary Data Transmission Over A Serial Link	Issued	Silicon Image, Inc.
10/357,750	7,283,566	United States	Method And Circuit For Generating Time Stamp Data From An Embedded-Clock Audio Data Stream And A Video Clock	Issued	Silicon Image, Inc.
10/016,247	6,714,206	United States	Method And System For Spatial-Temporal Dithering For Displays With Overlapping Pixels	Issued	Silicon Image, Inc.
10/133,813	7,136,484	United States	Cryptosystems Using Commuting Pairs In A Monoid	Issued	Silicon Image, Inc.
10/047,772	7,109,958	United States	Supporting Circuitry And Method For Controlling Pixels	Issued	Silicon Image, Inc.
10/045,393	7,039,121	United States	Method And System For Transition-Controlled Selective Block Inversion	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Communications		
08/656,032	6,018,456	United States	Enclosure For Removable Computer Peripheral Equipment	Issued	CMD Technology Inc. and Silicon Image, Inc.
08/906,775	5,991,546	United States	System And Method For Interfacing Manually Controllable Input Devices To A Universal Computer Bus System	Issued	CMD Technology Inc. and Silicon Image, Inc.
10/171,820	7,225,282	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/713,241	7,441,065	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	Silicon Image, Inc.
10/210,839	7,171,525	United States	Method And System For Arbitrating Priority Bids Sent Over Serial Links To A Multi-Port Storage Device	Issued	Silicon Image, Inc.
09/688,536	6,380,783	United States	Cyclic Phase Signal Generation From A Single Clock Source Using Current Phase Interpolation	Issued	Silicon Image, Inc.
09/847,837	6,535,029	United States	Fully Differential Continuous-Time Current-Mode High Speed CMOS Comparator	Issued	Silicon Image, Inc.
10/270,882	7,009,827	United States	Voltage Swing Detection Circuit For Hot Plug Event Or Device Detection Via A Differential Link	Issued	Silicon Image, Inc.
10/162,046	6,843,674	United States	Method And Apparatus For Connecting Serial ATA Storage Components	Issued	Silicon Image, Inc.
09/945,278	7,131,004	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
11/499,124	7,900,047	United States	Method And Apparatus For Encrypting Data Transmitted	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Over A Serial Link		Inc.
11/543,501	7,757,085	United States	Method And Apparatus For Encrypting Data Transmitted Over A Serial Link	Issued	Silicon Image, Inc.
10/224,995	7,218,737	United States	System And Method For An Adaptive State Machine To Control Signal Filtering In A Serial Link	Issued	Silicon Image, Inc.
09/991,057	7,242,766	United States	Method And System For Encrypting And Decrypting Data Using An External Agent	Issued	Silicon Image, Inc.
10/085,177	7,035,290	United States	Method And System For Temporary Interruption Of Video Data Transmission	Issued	Silicon Image, Inc.
10/036,794	6,976,201	United States	Method And System For Host Handling Of Communications Errors	Issued	Silicon Image, Inc.
10/053,461	7,113,507	United States	Method And System For Communicating Control Information Via Out-Of-Band Symbols	Issued	Silicon Image, Inc.
10/045,625	7,746,798	United States	Method And System For Integrating Packet Type Information With Synchronization Symbols	Issued	Silicon Image, Inc.
10/035,911	7,154,905	United States	Method And System For Nesting Of Communications Packets	Issued	Silicon Image, Inc.
10/045,600	6,771,192	United States	Method And System For DC-Balancing At The Physical Layer	Issued	Silicon Image, Inc.
10/045,601	7,340,558	United States	Multisection Memory Bank System	Issued	Silicon Image, Inc.
09/989,647	7,058,121	United States	Logic Gates Including Diode-Connected Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) To Control Input Threshold Voltage Levels And Switching Transients Of	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Output Logic Signals		
09/989,487	6,985,005	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
11/330,047	7,456,648	United States	Differential Amplifiers Using Asymmetric Transfer Characteristics To Suppress Input Noise In Output Logic Signals	Issued	Silicon Image, Inc.
12/275,686	7,847,583	United States	Transmitter And Receiver Using Asymmetric Transfer Characteristics In Differential Amplifiers To Suppress Noise	Issued	Silicon Image, Inc.
10/403,477	6,819,166	United States	Continuous-Time, Low-Frequency-Gain/High-Frequency-Boosting	Issued	Silicon Image, Inc.
10/417,712	7,348,991	United States	Video Graphics Text Mode Enhancement Method For Digitally Processed Data	Issued	Silicon Image, Inc.
10/287,976	6,873,341	United States	Detection Of Video Windows And Graphics Windows	Issued	Silicon Image, Inc.
10/298,722	7,539,304	United States	Integrated Circuit Having Self Test Capability Using Message Digest And Method For Testing Integrated Circuit Having Message Digest Generation Circuitry	Issued	Silicon Image, Inc.
10/215,936	6,717,468	United States	Dynamically Biased Full-Swing Operation Amplifier For An Active Matrix Liquid Crystal Display Driver	Issued	Silicon Image, Inc.
10/268,832	7,412,053	United States	Cryptographic Device With Stored Key Data And Method For Using Stored Key Data To Perform An Authentication Exchange Of Self Test	Issued	Silicon Image, Inc.
11/950,088	7,797,536	United States	Cryptographic Device With Stored Key Data And Method	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			For Using Stored Key Data To Perform An Authentication Exchange Of Self Test		
10/244,152	6,814,583	United States	Through-Broad PCB Edge Connector, System And Method	Issued	Silicon Image, Inc.
10/247,675	8,064,508	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
11/796,175	8,275,026	United States	Equalizer With Controllably Weighted Parallel High Pass And Low Pass Filters And Receiver Including Such An Equalizer	Issued	Silicon Image, Inc.
10/651,500	7,551,909	United States	CMOS Transceiver With Dual Current Path VCO	Issued	Silicon Image, Inc.
10/099,533	7,158,593	United States	Combining A Clock Signal And A Data Signal	Issued	Silicon Image, Inc.
10/642,259	7,409,031	United States	Data Sampling Method And Apparatus With Alternating Edge Sampling Phase Detection For Loop Characteristic Stabilization	Issued	Silicon Image, Inc.
10/459,989	7,187,307	United States	Method And System For Encapsulation Of Multiple Levels Of Communication Protocol Functionality Within Line Codes	Issued	Silicon Image, Inc.
10/794,015	7,502,411	United States	Method And Circuit For Adaptive Equalization Of Multiple Signals In Response To A Control Signal Generated From One Of The Equalized Signals	Issued	Silicon Image, Inc.
10/459,992	6,747,580	United States	Method And Apparatus For Encoding Or Decoding Data In Accordance With An Nb/(N+1)B Block Code, And Method For Determining Such A Block Code	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
10/781,405	7,269,673	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/848,758	7,500,032	United States	Cable With Circuitry For Asserting Stored Cable Data Or Other Information To An External Device Or User	Issued	Silicon Image, Inc.
11/123,353	7,375,960	United States	Apparatus For Removably Securing Storage Components In An Enclosure	Issued	Silicon Image, Inc.
10/763,905	7,236,553	United States	Reduced Dead-Cycle, Adaptive Phase Tracking Method And Apparatus	Issued	Silicon Image, Inc.
10/835,301	6,897,793	United States	Method And Apparatus For Run Length Limited TMDS-Like Encoding Of Data	Issued	Silicon Image, Inc.
10/842,231	7,991,096	United States	Data Sampling Method And Apparatus Using Through-Transition Counts To Reject Worst Sampling Position	Issued	Silicon Image, Inc.
10/439,446	7,031,858	United States	Method And Circuit For DC Measurement Of Phase Uniformity Of Multi-Phase Clocks	Issued	Silicon Image, Inc.
10/302,436	7,274,690	United States	An Age Selection Switching Scheme For Data Traffic In A Crossbar Switch	Issued	Silicon Image, Inc.
10/645,786	7,505,422	United States	Preference Programmable First-One Detector And Quadrature Based Random Grant Generator	Issued	Silicon Image, Inc.
10/645,787	7,461,167	United States	A Method For Multicast Service In A Crossbar Switch	Issued	Silicon Image, Inc.
10/762,950	7,352,764	United States	Content Addressable Merged Queue Architecture For Switching Data	Issued	Silicon Image, Inc.
10/434,785	7,519,066	United States	A Method For Switching Data In A Crossbar Switch	Issued	Silicon Image, Inc.
11/372,866	7,694,204	United States	Error Detection In Physical	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Interfaces For Point-To-Point Communications Between Integrated Circuits		Inc.
12/712,124	7,937,644	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
13/099,254	8,099,648	United States	Error Detection In Physical Interfaces For Point-To-Point Communications Between Integrated Circuits	Issued	Silicon Image, Inc.
11/669,416	7,844,762	United States	Parallel Interface Bus To Communicate Video Data Encoded For Serial Data Links	Issued	Silicon Image, Inc.
11/056,995	7,102,446	United States	Phase Lock Loop With Coarse Control Loop Having Frequency Lock Detector And Device Including Same	Issued	Silicon Image, Inc.
11/643,388	7,589,559	United States	Current Mode Circuitry To Modulate A Common Mode Voltage	Issued	Silicon Image, Inc.
12/555,300	7,872,498	United States	Current Mode Circuitry to Modulate a Common Mode Voltage	Issued	Silicon Image, Inc.
11/477,049	7,793,179	United States	Test Clock Control Structures To Generate Configurable Test Clocks For Scan-Based Testing Of Electronic Circuits Using Programmable Test Clock Controllers	Issued	Silicon Image, Inc.
11/856,640	7,782,934	United States	Parameter Scanning For Signal Over-Sampling	Issued	Silicon Image, Inc.
11/592,792	7,450,038	United States	Determining Oversampled Data To Be Included In Unit Intervals	Issued	Silicon Image, Inc.
11/510,254	8,595,434	United States	Smart Scalable Storage Switch Architecture	Issued	Silicon Image, Inc.
14/067,363		United States	Smart Scalable Storage Switch Architecture	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/314,162	7,571,269	United States	A Covert Channel For Conveying Supplemental Messages In A Protocol-Defined Link For A System Of Storage Devices	Issued	Silicon Image, Inc.
11/637,254	7,602,253	United States	Adaptive Bandwidth Phase Locked Loop With Feedforward Divider	Issued	Silicon Image, Inc.
11/656,331	7,984,369	United States	Concurrent Code Checker And Hardware Efficient High-Speed I/O Having Built-In Self-Test And Debug Features	Issued	Silicon Image, Inc.
11/694,819	7,949,863	United States	Multi-Port Memory Device Having Variable Port Speeds	Issued	Silicon Image, Inc.
11/694,813	7,639,561	United States	Power-Saving Clocking Technique	Issued	Silicon Image, Inc.
11/690,629	7,831,778	United States	Mechanism For Streaming Media Data Over Wideband Wireless Networks	Issued	Silicon Image, Inc.
11/476,457	7,840,861	United States	Scan-Based Testing Of Devices Implementing A Test Clock Control Structure (â€œTCCSâ€)	Issued	Silicon Image, Inc.
11/861,175	8,160,192	United States	Signal Interleaving for Serial Clock and Data Recovery	Issued	Silicon Image, Inc.
11/690,642	7,908,501	United States	Shared Nonvolatile Memory Architecture	Issued	Silicon Image, Inc.
11/742,358	7,698,088	United States	Interface Test Circuitry And Methods	Issued	Silicon Image, Inc.
11/848,641	8,233,432	United States	Ensuring Physical Locality Of Entities Sharing Data	Issued	Silicon Image, Inc.
11/683,608	7,831,877	United States	Method And Apparatus For A Two-Wire Serial Command Bus Interface	Issued	Silicon Image, Inc.
11/690,659	7,849,339	United States	Progressive Power Control Of A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/567,514	7,365,659	United States	Method Of Context Adaptive Binary Arithmetic Coding	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			And Coding Apparatus Using The Same		
12/778,882		United States	Multi-Level Port Expansion For Port Multipliers	Pending	Silicon Image, Inc.
12/147,248	7,836,223	United States	Operation Of Media Interface To Provide Bidirectional Communications	Issued	Silicon Image, Inc.
11/849,163	8,695,034	United States	Delivering On Screen Display Data To Existing Display Devices	Issued	Silicon Image, Inc.
11/828,219	8,599,315	United States	On Screen Displays Associated With Remote Video Source Devices	Issued	Silicon Image, Inc.
14/070,373		United States	On Screen Displays Associated With Remote Video Source Devices	Pending	Silicon Image, Inc.
11/829,800	7,903,550	United States	Bandwidth Reservation For Data Flows In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,223	8,149,711	United States	Data Stream Control For Network Devices	Issued	Silicon Image, Inc.
13/541,390	8,924,509	United States	Automated Service Discovery And Dynamic Connection Management	Issued	Silicon Image, Inc.
11/836,082	8,468,212	United States	Network Repository For Metadata	Issued	Silicon Image, Inc.
13/919,773		United States	Network Repository For Metadata	Pending	Silicon Image, Inc.
11/829,790	7,911,956	United States	Packet Level Prioritization In Interconnection Networks	Issued	Silicon Image, Inc.
11/828,226		United States	Streaming Data Content In A Network	Pending	Silicon Image, Inc.
11/848,153	7,936,790	United States	Synchronizing Related Data Streams In Interconnection Networks	Issued	Silicon Image, Inc.
11/952,052	8,001,334	United States	Bank Sharing And Refresh In A Shared Multi-Port Memory Device	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/075,954	7,979,589	United States	Method, Apparatus, And System For Port Multiplier Enhancement	Issued	Silicon Image, Inc.
13/298,001		United States	Iddq Testing Of CMOS Devices	Pending	Silicon Image, Inc.
10/788,704	6,944,086	United States	Semiconductor Memory Device	Issued	Silicon Image, Inc.
10/876,231	7,016,255	United States	Multi-Port Memory Device	Issued	Silicon Image, Inc.
10/877,318	7,089,465	United States	Multi-Port Memory Device Having Serial I/O Interface	Issued	Silicon Image, Inc.
12/075,906	7,904,566	United States	Method, Apparatus, And System For Employing An Enhanced Port Multiplier	Issued	Silicon Image, Inc.
12/497,391	8,386,867	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
13/776,508	8,667,354	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
14/145,751	8,924,805	United States	Computer Memory Test Structure	Issued	Silicon Image, Inc.
12/197,020	8,086,886	United States	Group Power Management Of Network Devices	Issued	Silicon Image, Inc.
12/683,365	8,543,873	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
14/035,795	8,839,058	United States	Multi-Site Testing Of Computer Memory Devices And Serial I/O Ports	Issued	Silicon Image, Inc.
11/969,847	8,090,030	United States	Method, Apparatus And System For Generating And Facilitating Mobile High-Definition Multimedia Interface	Issued	Silicon Image, Inc.
11/969,852	7,856,520	United States	Control Bus For Connection Of Electronic Devices	Issued	Silicon Image, Inc.
11/969,865	7,921,231	United States	Discovery Of Electronic Devices Utilizing A Control	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Bus		
12/172,187	8,238,653	United States	Methods And Mechanisms For Probabilistic Color Correction	Issued	Silicon Image, Inc.
12/392,000		United States	Method, Apparatus, And System For Pre-Authentication And Processing Of Data Streams	Pending	Silicon Image, Inc.
12/391,987	8,644,504	United States	Method, Apparatus, And System For Deciphering Media Content Stream	Issued	Silicon Image, Inc.
12/605,134	8,407,427	United States	Method And System For Improving Serial Port Memory Communication Latency And Reliability	Issued	Silicon Image, Inc.
13/850,147	8,892,825	United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Issued	Silicon Image, Inc.
12/260,970	8,036,248	United States	Method, Apparatus, And System For Automatic Data Aligner For Multiple Serial Receivers	Issued	Silicon Image, Inc.
12/359,025	8,026,726	United States	Fault Testing For Interconnections	Issued	Silicon Image, Inc.
12/486,969	8,793,723	United States	Detection Of Encryption Utilizing Error Detection For Received Data	Issued	Silicon Image, Inc.
12/570,874	8,644,334	United States	Messaging To Provide Data Link Integrity	Issued	Silicon Image, Inc.
12/260,972	7,777,652	United States	Coding System For Memory Systems Employing High-Speed Serial Links	Issued	Silicon Image, Inc.
12/847,416	7,978,099	United States	17b/20b Coding System	Issued	Silicon Image, Inc.
12/351,698	8,374,346	United States	Method, Apparatus, And System For Pre-Authentication And Keep-Authentication Of Content Protected Ports	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/316,305	8,347,081	United States	Method, Apparatus And System For Employing A Content Protection System	Issued	Silicon Image, Inc.
12/577,707	8,275,914	United States	Method And System For Transmitting Or Receiving N-Bit Video Data Over A Serial Link	Issued	Silicon Image, Inc.
12/606,096	8,176,214	United States	Transmission Of Alternative Content Over Standard Device Connectors	Issued	Silicon Image, Inc.
12/351,712	8,185,739	United States	Method And System For Detecting Successful Authentication Of Multiple Ports In A Time Based Roving Architecture	Issued	Silicon Image, Inc.
12/512,877	8,458,343	United States	Signaling For Transitions Between Modes Of Data Transmission	Issued	Silicon Image, Inc.
12/983,233	8,489,784	United States	Adaptive Interconnection Scheme For Multimedia Devices	Issued	Silicon Image, Inc.
13/004,359	8,755,431	United States	Transmission And Detection Of Multi-Channel Signals In Reduced Channel Format	Issued	Silicon Image, Inc.
12/650,357		United States	Method, Apparatus, And System For Simultaneously Previewing Contents From Multiple Protected Sources	Pending	Silicon Image, Inc.
12/712,933	8,692,937	United States	Video Frame Synchronization	Issued	Silicon Image, Inc.
12/966,194		United States	Transmission And Handling Of Three-Dimensional Video Content	Pending	Silicon Image, Inc.
12/873,124	8,325,757	United States	De-Encapsulation Of Data Streams Into Multiple Links	Issued	Silicon Image, Inc.
12/704,417	8,510,487	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.
13/934,147	8,751,709	United States	Hybrid Interface For Serial And Parallel Communication	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/842,165	8,930,692	United States	Mechanism For Internal Processing Of Content Through Partial Authentication On Secondary Channel	Issued	Silicon Image, Inc.
12/842,190		United States	Mechanism For Partial Encryption Of Data Streams	Pending	Silicon Image, Inc.
13/021,958		United States	Determination Of Physical Connectivity Status Of Devices Based On Electrical Measurement	Allowed	Silicon Image, Inc.
12/898,528	8,598,898	United States	Testing Of High-Speed Input-Output Devices	Issued	Silicon Image, Inc.
13/434,273		United States	Method, Apparatus And System For Transitioning An Audio/Video Device Between A Source Mode And A Sink Mode	Pending	Silicon Image, Inc.
12/848,037	8,624,960	United States	Multi-View Display System	Issued	Silicon Image, Inc.
14/094,668		United States	Multi-View Display System	Pending	Silicon Image, Inc.
12/816,437	8,698,958	United States	Mechanism For Memory Reduction In Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
13/753,408		United States	Communication Bridging Between Devices Via Multiple Bridge Elements	Pending	Silicon Image, Inc.
13/198,584		United States	Conversion Of Multimedia Data Streams For Use By Connected Devices	Pending	Silicon Image, Inc.
12/906,939	8,537,201	United States	Combining Video Data Streams Of Differing Dimensionality For Concurrent Display	Issued	Silicon Image, Inc.
13/172,745	8,484,387	United States	Detection Of Cable Connections For Electronic Devices	Issued	Silicon Image, Inc.
13/172,742	8,601,173	United States	Detection Of Cable Connections For Electronic	Issued	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Devices		
13/362,930		United States	Mechanism For Low Power Standby Mode Control Circuit	Allowed	Silicon Image, Inc.
13/217,138	8,379,145	United States	Conversion And Processing Of Deep Color Video In A Single Clock Domain	Issued	Silicon Image, Inc.
12/979,995	8,874,820	United States	Mechanism For Facilitating A Configurable Port-Type Peripheral Component Interconnect Express/Serial Advanced Technology Attachment Host Controller Architecture	Issued	Silicon Image, Inc.
12/950,850	8,504,672	United States	Discovery Of Electronic Devices In A Combined Network	Issued	Silicon Image, Inc.
13/959,592	8,799,443	United States	Discovery of Electronic Devices in a Combined Network	Issued	Silicon Image, Inc.
13/348,378		United States	Proxy Device Operation In Command And Control Network	Pending	Silicon Image, Inc.
12/950,867		United States	Transfer Of Control Bus Signaling On Packet-Switched Network	Pending	Silicon Image, Inc.
13/339,339		United States	Mechanism For Recovering Clock For Streaming Content Over A Packetized Network	Pending	Silicon Image, Inc.
13/302,452		United States	Multimedia I/O System Architecture for Advanced Digital Television	Pending	Silicon Image, Inc.
13/107,031		United States	Audio And Video Data Multiplexing For Multimedia Stream Switch	Pending	Silicon Image, Inc.
13/174,630		United States	Single-Ended Configurable Multi-Mode Driver	Pending	Silicon Image, Inc.
13/173,302		United States	Fine-Grained Self Refresh Control For DRAM Devices	Pending	Silicon Image, Inc.
13/174,616	8,760,188	United States	Configurable Multi-Dimensional Driver And	Issued	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Receiver		Inc.
13/083,399	8,611,486	United States	Adjustment Of Clock Signals Regenerated From A Data Stream	Issued	Silicon Image, Inc.
11/437,357	7,982,798	United States	Edge Detection	Issued	Silicon Image, Inc.
13/153,230	8,446,525	United States	Edge Detection	Issued	Silicon Image, Inc.
10/753,909	7,400,359	United States	Video Stream Routing And Format Conversion Unit With Audio Delay	Issued	Silicon Image, Inc.
10/889,855	7,710,501	United States	Time Base Correction And Frame Rate Conversion	Issued	Silicon Image, Inc.
11/487,144	8,004,606	United States	Original Scan Line Detection	Issued	Silicon Image, Inc.
11/941,050	8,086,067	United States	Noise Cancellation	Issued	Silicon Image, Inc.
11/512,754	8,120,703	United States	Source-Adaptive Video Deinterlacer	Issued	Silicon Image, Inc.
12/204,760	8,559,746	United States	System, Method And Apparatus For Smoothing Of Edges In Images To Remove Irregularities	Issued	Silicon Image, Inc.
14/054,575		United States	System, Method and Apparatus for Smoothing of Edges in Images to Remove Irregularities	Pending	Silicon Image, Inc.
12/703,623	8,452,117	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/899,222	8,891,897	United States	Block Noise Detection And Filtering	Issued	Silicon Image, Inc.
13/335,398		United States	Ringing Suppression In Video Scalers	Pending	Silicon Image, Inc.
13/546,904		United States	Transmission Of Multiple Protocol Data Elements Via An Interface Utilizing A Data Tunnel	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
11/202,995	7,904,117	United States	Wireless Communication Device Using Adaptive Beamforming	Issued	SiBEAM, Inc.
11/706,711	7,710,319	United States	HD Physical Layer Of A Wireless Communication Device	Issued	SiBEAM, Inc.
12/748,276	7,982,669	United States	Adaptive Beam-Steering Methods To Maximize Wireless Link Budget And Reduce Delay-Spread Using Multiple Transmit And Receive Antennas	Issued	SiBEAM, Inc.
11/706,470	8,014,416	United States	Inter-Port Communication In A Multi-Port Memory Device	Issued	Silicon Image, Inc.
11/689,386	7,881,258	United States	Circuitry To Prevent Peak Power Problems During Scan Shift	Issued	SiBEAM, Inc.
11/726,874	8,155,712	United States	Low Power Very High-Data Rate Device	Issued	SiBEAM, Inc.
11/588,472	8,022,887	United States	Planar Antenna	Issued	SiBEAM, Inc.
11/752,073		United States	A Compact Millimeter Wave Vertical Interconnection Scheme By Combining Flip-Chip, Layer Transition	Pending	SiBEAM, Inc.
11/752,083	7,675,465	United States	Surface Mountable Integrated Circuit Packaging Scheme	Issued	SiBEAM, Inc.
12/215,959		United States	Mechanism For Communication With Multiple Wireless Video Area Networks	Pending	SiBEAM, Inc.
11/981,935		United States	Wireless HD Mac Frame Format	Pending	SiBEAM, Inc.
11/938,126	8,170,522	United States	Multi-Transformer Architecture For An RF Active Circuit	Issued	SiBEAM, Inc.
11/999,810	8,750,241	United States	Concurrent Association With Multiple WVAN Network	Issued	SiBEAM, Inc.
12/079,133	8,831,225	United States	Data Security	Issued	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
12/011,404	7,948,961	United States	Wireless Proximity Estimation	Issued	SiBEAM, Inc.
11/982,209	8,279,784	United States	Wireless HD AV Packet Format	Issued	SiBEAM, Inc.
12/055,160	8,170,617	United States	Extensions To Adaptive BeamSteering Method	Issued	SiBEAM, Inc.
12/164,757		United States	Exchanging Information Between Components Coupled With An I2C Bus Via Separate Banks	Pending	SiBEAM, Inc.
12/167,195	8,229,352	United States	Wireless Architecture For 60 GHz	Issued	SiBEAM, Inc.
11/901,069	7,986,753	United States	Modified Branch Metric For Decoders And Equalizers	Issued	SiBEAM, Inc.
12/059,757	7,915,909	United States	RF Integrated Circuit Test Methodology And System	Issued	SiBEAM, Inc.
12/164,907		United States	Dispatch Capability Using A Single Physical Interface	Pending	SiBEAM, Inc.
12/165,468		United States	Bitmap Device Identification In A Wireless Communication System	Pending	SiBEAM, Inc.
12/165,472	8,897,719	United States	Initializing A Transceiver In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,849	8,341,271	United States	Device Discovery In A Wireless Communication System	Issued	SiBEAM, Inc.
12/164,810	8,116,333	United States	Connection Control In A Wireless Communication System	Issued	SiBEAM, Inc.
12/699,758	8,588,193	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
12/699,781	8,457,026	United States	Enhanced Wireless Data Rates Using Multiple Beams	Issued	SiBEAM, Inc.
13/113,318		United States	Apparatus, System, And Method For A Compact Symmetrical Transition Structure For Radio	Allowed	SiBEAM, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Frequency Applications		
14/128,551		United States	Method To Drive HDMI Or MHL Or USB Data Through One Set Of Pins	Pending	Silicon Image, Inc.
13/984,018		United States	Concept And Method Of Reducing Data Dependent Jitter	Pending	Silicon Image, Inc.
13/269,450		United States	Identification And Handling Of Data Streams Using Coded Preambles	Allowed	Silicon Image, Inc.
13/611,786		United States	Combining Video And Audio Streams Utilizing Pixel Repetition Bandwidth	Pending	Silicon Image, Inc.
14/118,832		United States	Compensation Scheme For MHL Common Mode Clock Swing	Pending	Silicon Image, Inc.
13/773,534		United States	Transmitting Multiple Differential Signals Over a Reduced Number of Physical Channels	Pending	Silicon Image, Inc.
13/460,393		United States	Cost-Efficient And Low-Latency Motion Picture Encoding For Limited Channel Bandwidth	Pending	Silicon Image, Inc.
13/791,494	8,925,003	United States	Mechanism For Facilitating Syncronization Of Audio And Video Between Multiple Media Devices	Issued	Silicon Image, Inc.
13/622,286	8,885,435	United States	Interfacing Between Integrated Circuits With Asymmetric Voltage Swing	Issued	Silicon Image, Inc.
13/770,984		United States	Configurable Single Ended Driver	Pending	Silicon Image, Inc.
13/779,372	8,920,188	United States	Integrated Connector/Flex Cable	Issued	Silicon Image, Inc.
13/834,927		United States	Simultaneous Transmission Of Clock And Bidirectional Data Over A Communication Channel	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
13/605,708	8,841,974	United States	Test Solution For Ring Oscillators	Issued	Silicon Image, Inc.
14/193,932		United States	Test Solution for a Random Number Generator	Pending	Silicon Image, Inc.
13/787,664		United States	Auxiliary Data Encoding In Video Data	Pending	Silicon Image, Inc.
13/738,768		United States	Method And Apparatus For Reducing Digital Video Image Data	Pending	Silicon Image, Inc.
13/736,765	8,832,338	United States	Mechanism For Facilitating Dynamic Timestamp-Less Clock Regeneration For Transmitting Media Streams Over Shared Channels	Issued	Silicon Image, Inc.
14/123,037		United States	Timing Controlled Cascade Feed-Through High Speed Line Driver	Pending	Silicon Image, Inc.
13/776,577		United States	Apparatus, System And Method For Providing Clock And Data Signaling	Pending	Silicon Image, Inc.
13/940,038		United States	Integrated Mobile Desktop	Pending	Silicon Image, Inc.
13/915,586		United States	Multiple Protocol Tunneling Using Time Division Operations	Pending	Silicon Image, Inc.
13/891,842	8,786,776	United States	Method, Apparatus And System For Communicating Sideband Data With Non-Compressed Video	Issued	Silicon Image, Inc.
13/671,527		United States	Methods And Apparatuses To Provide And Electro-Optical Alignment	Pending	Silicon Image, Inc.
14/371,973		United States	Charge Pump Calibration for Dual-Path Phase-Locked Loop	Pending	Silicon Image, Inc.
14/115,324		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Allowed	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/135,470		United States	Apparatus, System and Method for Formatting Audio-Video Information	Pending	Silicon Image, Inc.
13/839,671		United States	Full Frame Buffer To Improve Video Performance In Low- Latency Video Communication Systems	Pending	Silicon Image, Inc.
12/057,051		United States	Bi-Directional Digital Interface For Video And Audio (DIVA)	Pending	Silicon Image, Inc.
11/760,164	7,940,809	United States	Digital Video Interface With Bi-Directional Half-Duplex Clock Channel Used As Auxiliary Data Channel	Issued	Silicon Image, Inc.
11/865,621	7,916,780	United States	Adaptive Equalizer For Use With Clock And Data Recovery Circuit Of Serial Communication Link	Issued	Silicon Image, Inc.
12/222,745	7,737,802	United States	Passive Equalizer With Negative Impedance To Increase A Gain	Issued	Silicon Image, Inc.
12/636,063	8,680,712	United States	Power Delivery Over Digital Interactive Interface For Video And Audio (DIIVA)	Issued	Silicon Image, Inc.
13/521,739		United States	Multi-Media USB Data Transfer Over Digital Interaction Interface for Video and Audio (DIIVA)	Pending	Silicon Image, Inc.
13/521,762		United States	Video Management And Control In Home Multimedia Network	Pending	Silicon Image, Inc.
14/381,186		United States	Linear Regulator with Improved Power Supply Ripple Rejection	Pending	Silicon Image, Inc.
13/844,152		United States	Electronic Alignment Of Optical Signals	Pending	Silicon Image, Inc.
14/391,382		United States	Frequency Response Compensation in a Digital to Analog Converter	Pending	Silicon Image, Inc.
14/165,340		United States	Apparatus, System and	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			Method for Providing Switching with a T-Coil Circuit		Inc.
13/836,895	8,928,411	United States	Integration Of Signal Sampling Within Transistor Amplifier Stage	Issued	Silicon Image, Inc.
14/165,345		United States	Apparatus, Method and System for Asymmetric Full-Duplex Communication	Pending	Silicon Image, Inc.
14/209,785		United States	Method And Apparatus For Implementing Wide Data Range And Wide Common-Mode Receivers	Pending	Silicon Image, Inc.
14/296,377		United States	Transmitting Apparatus with Source Termination	Pending	Silicon Image, Inc.
14/368,781		United States	Caching of Capabilities Information of Counterpart Device for Efficient Handshaking Operation	Pending	Silicon Image, Inc.
14/163,981		United States	Mechanism for Facilitating Dynamic Counter Synchronization and Packetization in High-Definition Multimedia Interface and Mobile High-Definition Link	Pending	Silicon Image, Inc.
14/253,808		United States	Communication of Multimedia Data Streams Over Multiple Communication Lanes	Pending	Silicon Image, Inc.
14/279,316		United States	HDCP2.2 Authentication Engine and Stream Cipher Engine Sharing in Digital Content Protection Architectures	Pending	Silicon Image, Inc.
14/383,865		United States	Techniques for Fractional-N Phase Locked Loops	Pending	Silicon Image, Inc.
61/949,901		United States	Compressed Video Transfer Over HDMI and MHL	Pending	Silicon Image, Inc.
14/563,797		United States	Electrical Duplex to Optical Conversion	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
14/470,750		United States	Arbitration Signaling within a Multimedia High Definition Link (MHL 3) Device	Pending	Silicon Image, Inc.
14/275,692		United States	Error Detection and Mitigation in Video Channels	Pending	Silicon Image, Inc.
14/339,393		United States	Phase-Modulated On-Off Keying for Millimeter Wave Spectrum Control	Pending	Silicon Image, Inc.
14/145,715		United States	Messaging to Provide Data Link Integrity	Pending	Silicon Image, Inc.
14/145,736	8,854,548	United States	Mechanism for Memory Reduction in Picture-In-Picture Video Generation	Issued	Silicon Image, Inc.
14/470,613		United States	Compressed Video Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/184,647		United States	Video Frame Synchronization	Pending	Silicon Image, Inc.
14/181,446		United States	Power Delivery Over Digital Interaction Interface for Video and Audio (DiiVA)	Pending	Silicon Image, Inc.
14/470,804		United States	Phase Relationship Control for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
14/470,809		United States	Retry Disparity for Control Channel of a Multimedia Communication Link	Pending	Silicon Image, Inc.
61/943,267		United States	Pre-Processor and Post-Processor for Compression of 4:2:0 Encoded Video Streams with Video Compression Codecs Embedded within an Audio/Video Standard	Pending	Silicon Image, Inc.
14/278,255		United States	Encoding Guard Band Data for Transmission Via a Communications Interface Utilizing Transition-Minimized Differential Signaling (Tmds) Coding	Pending	Silicon Image, Inc.
14/322,753		United States	Calibration Of Single-Ended	Pending	Silicon Image,

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
			High-Speed Interfaces		Inc.
61/947,704		United States	Reversible Connector	Pending	Silicon Image, Inc.
14/460,737		United States	System and Method for Transcoding Data	Pending	Silicon Image, Inc.
14/502,928		United States	Electrical Connector with Optical Channel	Pending	Silicon Image, Inc.
14/322,753		United States	Cable with Circuitry for Communicating Performance Information	Pending	Silicon Image, Inc.
61/973,837		United States	Error Correction for Transmission of Compressed Video Data Over Standards-Defined Coded Audio/Video Links	Pending	Silicon Image, Inc.
61/975,517		United States	(MHL) Connector Cable Detect, Cable Orientation Detect and/or Lane Re-Mapping	Pending	Silicon Image, Inc.
61/979,477		United States	MHL3 Router without HDCP2.2 Decryption and Encryption Operation	Pending	Silicon Image, Inc.
61/979,483		United States	TDD over 5-Pin Interface	Pending	Silicon Image, Inc.
14/470,620		United States	Compressed Blanking Period Transfer Over a Multimedia Link	Pending	Silicon Image, Inc.
14/273,400		United States	Transmission and Detection of Multi-Channel Signals in Reduced Channel Format	Pending	Silicon Image, Inc.
61/989,409		United States	System for Dynamic Capabilities, Status, and Metadata Exchange	Pending	Silicon Image, Inc.
14/300,166		United States	Configurable Multi-Dimensional Driver and Receiver	Pending	Silicon Image, Inc.
14/483,013		United States	Enhanced Communication Link Using Synchronization Signal as Link Command	Pending	Silicon Image, Inc.

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App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
62/043,218		United States	Run Length Programmable Unified Built-In Self-Test (BIST) Scheme for Various High-Speed Serial IO Standards	Pending	Silicon Image, Inc.
14/559,523		United States	Determination of Physical Connectivity Status of Devices Based on Electrical Measurement	Pending	Silicon Image, Inc.
14/516,136		United States	Method and System for Improving Serial Port Memory Communication Latency and Reliability	Pending	Silicon Image, Inc.
62/061,630		United States	Secure Control Communication Between an Application Processor and a Transmitter	Pending	Silicon Image, Inc.
62/075,554		United States	Metadata Transfer for HDMI/MHL	Pending	Silicon Image, Inc.
14/570,817		United States	Mechanism for Facilitating Dynamic Phase Detection with High Jitter Tolerance for Images of Media Streams	Pending	Silicon Image, Inc.
14/589,889		United States	Displaying Multiple Videos on Sink Device Using Display Information of Source Device	Pending	Silicon Image, Inc.
14/589,925		United States	Lower Power Operations in a Wireless Tunneling Transceiver	Pending	Silicon Image, Inc.
14/591,845		United States	Simultaneous Transmission of Clock and Bidirectional Data Over a Communication Channel	Pending	Silicon Image, Inc.
14/449095	20150036756	United States	Radio Frequency Interference Reduction In Multimedia Interfaces	Pending	Silicon Image, Inc.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	03/06/2007	7187307	SII-3000 [SIMG0158]	4911

60974 7590 02/14/2007

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 528 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Brian K. Schmidt, Mountain View, CA;
James G. Hanko, Redwood City, CA;
J. Duane Northcutt, Menlo Park, CA;
Alan T. Ruberg, Menlo Park, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Jacob Zweig	(Depositor's name)
	(Signature)
January 23, 2007	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	06/12/2003	Brian K. Schmidt	SII-3000 [SIMG0158]	4911

TITLE OF INVENTION: METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	02/07/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
YOUNG, BRIAN K	2819	341-050000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Girard & Equitz LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SILICON IMAGE, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): SUNNYVALE, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

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- ☒ A check is enclosed. **Deficiencies Only**
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-1697 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Alfred A Equitz Date January 23, 2006

Typed or printed name Alfred A. Equitz Registration No. 30,922

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, Virginia 22313-1450.

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JAN 23 2007
PATENT & TRADEMARK OFFICE

PATENT B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. 10/459,989

Filed: June 12, 2003

For: **METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES**

Group Art Unit: 2819

Confirmation No. 4911

Examiner: Young, Brian K.

TRANSMITTAL OF FORMAL DRAWINGS

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 18, 2007.

GIRARD & EQUITZ LLP Date: 01/18/07

By: _____
Jacob Zweig

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed are 2 sheets of formal drawings for filing in the above-referenced case.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 50-1697. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 1/18/07 By: _____

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No.: SII-3000 [SIMG0158]

OIPE IAP41
JAN 23 2007
PATENT & TRADEMARK OFFICE

Patent Application No. 10/459,989
Inventors' Name: Brian K. Schmidt, et al.
Attorney Docket No.: SII-3000 [SIMG0158]
Alfred A. Equitz/(415) 433-2250
Replacement Sheet 1 of 2

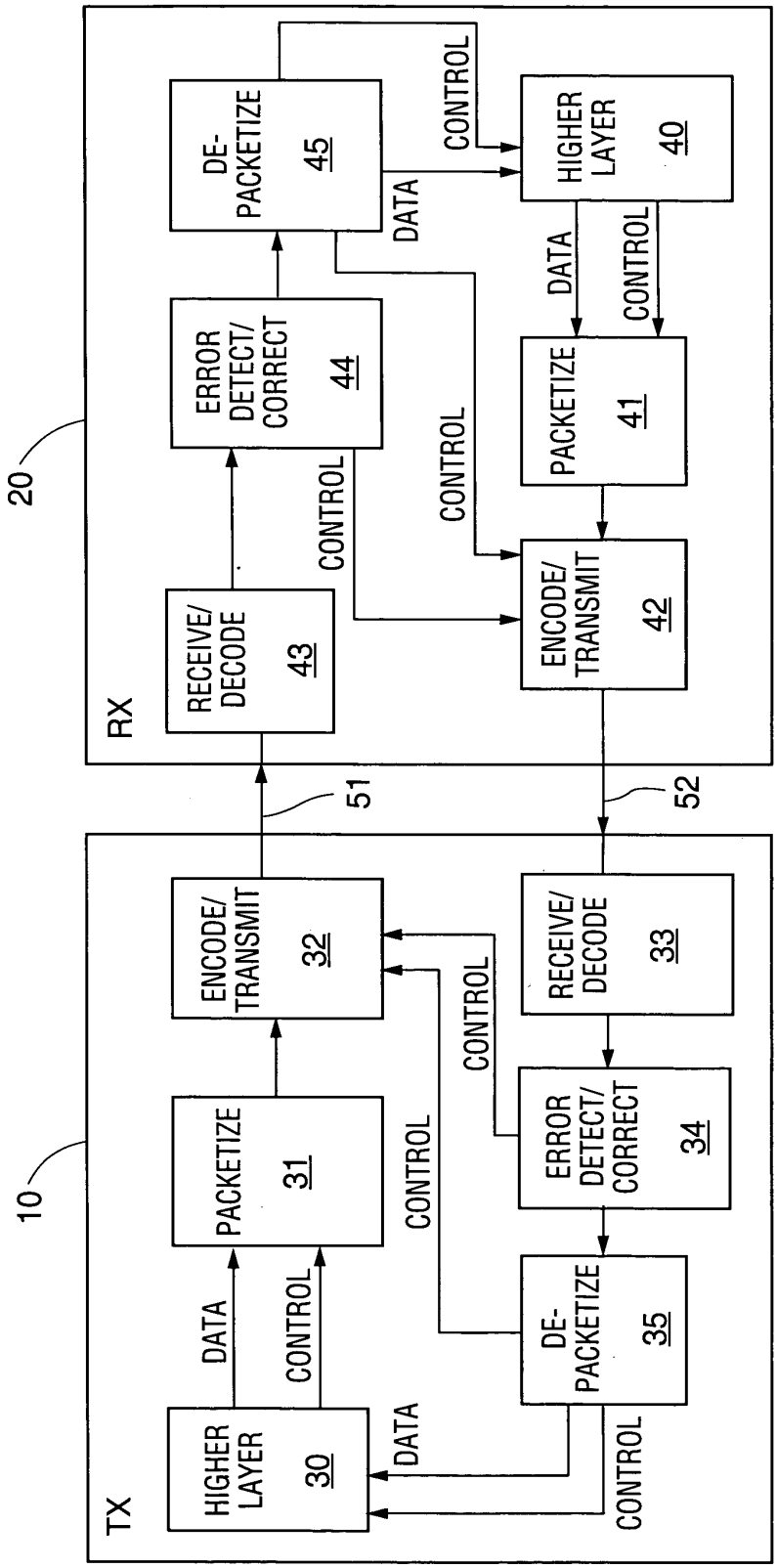


FIG. 1

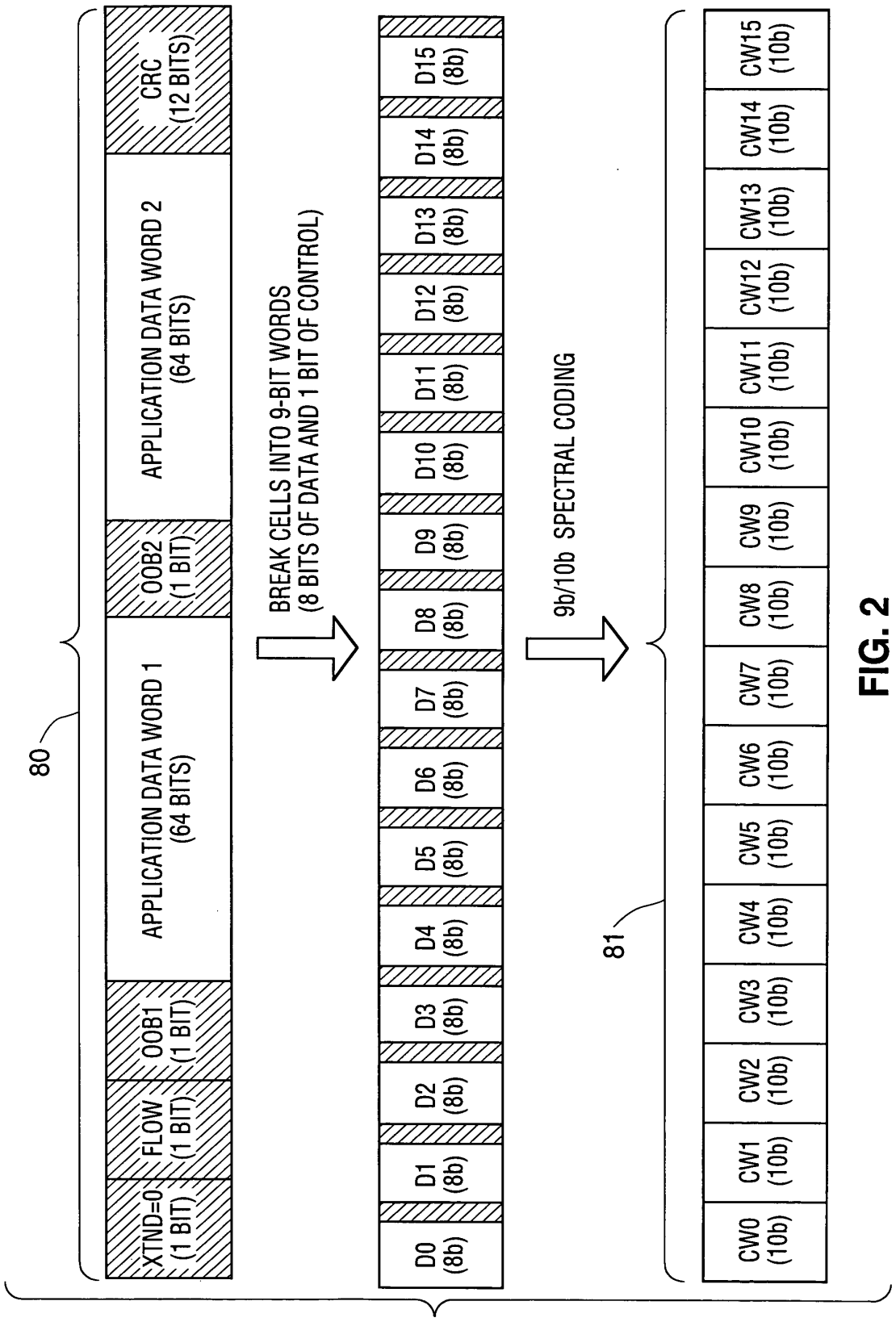

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OOB2 (1 BIT)
APPLICATION DATA WORD 2 (64 BITS)
CRC (12 BITS)
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D0 (8b)
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D7 (8b)
D8 (8b)
D9 (8b)
D10 (8b)
D11 (8b)
D12 (8b)
D13 (8b)
D14 (8b)
D15 (8b)
9b/10b SPECTRAL CODING
81
CW0 (10b)
CW1 (10b)
CW2 (10b)
CW3 (10b)
CW4 (10b)
CW5 (10b)
CW6 (10b)
CW7 (10b)
CW8 (10b)
CW9 (10b)
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CW11 (10b)
CW12 (10b)
CW13 (10b)
CW14 (10b)
CW15 (10b)

FIG. 2

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NOTICE OF ALLOWANCE AND FEE(S) DUE

60974 7590 11/07/2006

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO, CA 94104

EXAMINER	
YOUNG, BRIAN K	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/07/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	06/12/2003	Brian K. Schmidt	SII-3000 [SIMG0158]	4911

TITLE OF INVENTION: METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	02/07/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

IPR2024-001429
HP – EX1002, Page 137 of 357

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	06/12/2003	Brian K. Schmidt	SII-3000 [SIMG0158]	4911

TITLE OF INVENTION: METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$0	$1400	02/07/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
YOUNG, BRIAN K	2819	341-050000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	06/12/2003	Brian K. Schmidt	SII-3000 [SIMG0158]	4911

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EXAMINER	
YOUNG, BRIAN K	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/07/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 571 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 571 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

IPR2024-001429
HP – EX1002, Page 139 of 357

Notice of Allowability	Application No.	Applicant(s)	
	10/459,989	SCHMIDT ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the response filed 1/10/06*.

2. ☒ The allowed claim(s) is/are *1-109*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
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4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
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   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Brian Young
Primary Examiner
Art Unit: 2819

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Bib Data Sheet

CONFIRMATION NO. 4911

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,989	06/12/2003 RULE	341	2819	SII-3000 [SIMG0158]

APPLICANTS

Brian K. Schmidt, Mountain View, CA;
James G. Hanko, Redwood City, CA;
J. Duane Northcutt, Menlo Park, CA;
Alan T. Ruberg, Menlo Park, CA;

** CONTINUING DATA ********** (no)

** FOREIGN APPLICATIONS ********** (no)

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/05/2003

Foreign Priority claimed	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☒ no	CA	2	109	7
35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials				

ADDRESS
60974

TITLE
Method and system for encapsulation of multiple levels of communication protocol functionality within line codes

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Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/459,989	SCHMIDT ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
341	50	51	

INTERNATIONAL CLASSIFICATION	
h 0 3 m	7/00
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(Assistant Examiner) (Date)

(Legal Instruments Examiner) 11/30/06 (Date)

Brian Young 10/30/06

(Primary Examiner) (Date)

Total Claims Allowed: 109

O.G. Print Claim(s)	O.G. Print Fig.
1	1

☒ **Claims renumbered in the same order as presented by applicant** ☐ CRA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
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	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
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	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
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	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/459,989	SCHMIDT ET AL.	
Examiner	**Art Unit**	
Brian Young	2819	

SEARCHED			
Class	Subclass	Date	Examiner
341	50,51	10/30/2006	BY

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
341	**50**	**10/30/2006**	**BY**
PGPUB	only		

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
East (see attached) NPL (see attached)	10/30/2006	BY

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1 Teapot: language support for writing memory coherence protocols
Satish Chandra, Brad Richards, James R. Larus
May 1996 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1996 conference on Programming language design and implementation PLDI '96**, Volume 31 Issue 5
Publisher: ACM Press
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

Recent shared-memory parallel computer systems offer the exciting possibility of customizing memory coherence protocols to fit an application's semantics and sharing patterns. Custom protocols have been used to achieve message-passing performance---while retaining the convenient programming model of a global address space---and to implement high-level language constructs. Unfortunately, coherence protocols written in a conventional language such as C are difficult to write, debug, understand, or ...

2 Generating efficient protocol code from an abstract specification
Walid Dabbous, Sean O'Malley, Claude Castelluccia
August 1996 **ACM SIGCOMM Computer Communication Review , Conference proceedings on Applications, technologies, architectures, and protocols for computer communications SIGCOMM '96**, Volume 26 Issue 4
Publisher: ACM Press
Full text available: pdf(293.87 KB) Additional Information: full citation, abstract, references, citings, index terms

A protocol compiler takes as input an abstract specification of a protocol and generates an implementation of that protocol. Protocol compilers usually produce inefficient code both in terms of code speed and code size. In this paper, we show that the combination of two techniques makes it possible to build protocol compilers that generate efficient code. These techniques are i) the use of a compiler that generates from the specification a unique tree-shaped automaton (rather than multiple indep ...

3 Generating efficient protocol code from an abstract specification
Claude Castelluccia, Walid Dabbous, Sean O'Malley
August 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 4
Publisher: IEEE Press
Full text available: pdf(163.38 KB) Additional Information: full citation, references, citings, index terms

IPR2024-001429
HP – EX1002, Page 144 of 357

Keywords: code optimization, formal languages, protocol compilers, transport protocols

4 Speeding up protocols for small messages

Trevor Blackwell

August 1996 **ACM SIGCOMM Computer Communication Review , Conference proceedings on Applications, technologies, architectures, and protocols for computer communications SIGCOMM '96**, Volume 26 Issue 4

Publisher: ACM Press

Full text available: pdf(98.82 KB) Additional Information: full citation, abstract, references, citings, index terms

Many techniques have been discovered to improve performance of bulk data transfer protocols which use large messages. This paper describes a technique that improves protocol performance for protocols that use small messages, such as signalling protocols, by reducing memory system penalties. Detailed measurements show that for TCP, most memory system costs are due to poor locality in the protocol code itself, rather than movement of data. We present a new technique, analogous to blocked matrix mu ...

5 The priority ceiling protocol: A method for minimizing the blocking of high priority Ada tasks

J. B. Goodenough, L. Sha

June 1988 **ACM SIGAda Ada Letters , Proceedings of the second international workshop on Real-time Ada issues IRTAW '88**, Volume VIII Issue 7

Publisher: ACM Press

Full text available: pdf(1.01 MB) Additional Information: full citation, references, citings, index terms

6 Special Section on Science of Network Design: Building the blocks of protocol design and analysis: challenges and lessons learned from case studies on mobile ad hoc routing and micro-mobility protocols

Fan Bai, Ganesha Bhaskara, Ahmed Helmy

July 2004 **ACM SIGCOMM Computer Communication Review**, Volume 34 Issue 3

Publisher: ACM Press

Full text available: pdf(573.77 KB) Additional Information: full citation, abstract, references, index terms

With the emergence of new application-specific sensor and Ad-hoc networks, increasingly complex and custom protocols will be designed and deployed. We propose a framework to systematically design and evaluate networking protocols based on a 'building block' approach. In this approach, each protocol is broken down into a set of parameterized modules called "building blocks", each having its own specific functionality. The properties of these building blocks and their interaction define the ove ...

Keywords: building block, micro-mobility, mobile ad hoc network, protocol analysis, protocol design

7 Design and performance of the Shasta distributed shared memory protocol

Daniel J. Scales, Kourosh Gharachorloo

July 1997 **Proceedings of the 11th international conference on Supercomputing**

Publisher: ACM Press

Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

IPR2024-001429
HP – EX1002, Page 145 of 357

8 Ace: a language for parallel programming with customizable protocols

Mukund Raghavachari, Anne Rogers

August 1999 **ACM Transactions on Computer Systems (TOCS)**, Volume 17 Issue 3

Publisher: ACM Press

Full text available: pdf(297.50 KB) Additional Information: full citation, abstract, references, index terms, review

Customizing the protocols that manage accesses to different data structures within an application can improve the performance of software shared-memory programs substantially. Existing systems for using customizable protocols are hard to use directly because the mechanisms they provide for manipulating protocols are low-level ones. This article is an in-depth study of the issues involved in providing language support for application-specific protocols. We describe the design and implementat ...

Keywords: parallel processing

9 Cryptographic protocols/ network security: Automatic generation of two-party computations

Philip MacKenzie, Alina Oprea, Michael K. Reiter

October 2003 **Proceedings of the 10th ACM conference on Computer and communications security**

Publisher: ACM Press

Full text available: pdf(238.90 KB) Additional Information: full citation, abstract, references, index terms

We present the design and implementation of a compiler that automatically generates protocols that perform two-party computations. The input to our protocol is the specification of a computation with secret inputs (e.g., a signature algorithm) expressed using operations in the field Zq of integers modulo a prime q and in the multiplicative subgroup of order q in Z*p for q|p-1 with generator g. The output of our compiler is an implementation of each party in a two ...

Keywords: automatic generation of protocols, secure two-party computation, threshold cryptography

10 Poster 1: systems track: rStream: resilient peer-to-peer streaming with rateless codes

Chuan Wu, Baochun Li

November 2005 **Proceedings of the 13th annual ACM international conference on Multimedia MULTIMEDIA '05**

Publisher: ACM Press

Full text available: pdf(125.79 KB) Additional Information: full citation, abstract, references, index terms

The inherent instability and unreliability of peer-to-peer networks introduce several fundamental engineering challenges to multimedia streaming over peer-to-peer networks. First, multimedia streaming sessions need to be resilient to the volatile network dynamics in peer-to-peer networks. Second, they need to take full advantage of the existing bandwidth capacities, by minimizing the delivery of redundant content during streaming. In this paper, we propose to use a recent coding technique, refer ...

Keywords: content reconciliation, failure resilience, media streaming, peer-to-peer, rateless codes

11 Effective erasure codes for reliable computer communication protocols

Luigi Rizzo

IPR2024-001429
HP – EX1002, Page 146 of 357

April 1997 **ACM SIGCOMM Computer Communication Review**, Volume 27 Issue 2
Publisher: ACM Press
Full text available: pdf(890.73 KB) Additional Information: full citation, abstract, citings, index terms

Reliable communication protocols require that all the intended recipients of a message receive the message intact. Automatic Repeat reQuest (ARQ) techniques are used in unicast protocols, but they do not scale well to multicast protocols with large groups of receivers, since segment losses tend to become uncorrelated thus greatly reducing the effectiveness of retransmissions. In such cases, Forward Error Correction (FEC) techniques can be used, consisting in the transmission of redundant packets ...

Keywords: FEC, erasure codes, reliable multicast

12 Spread-sprectrum CDMA packet radio MAC protocol using channel overload detection and blocking
Garth Judge, Fambirai Takawira
December 2000 **Wireless Networks**, Volume 6 Issue 6
Publisher: Kluwer Academic Publishers
Full text available: pdf(283.75 KB) Additional Information: full citation, abstract, references, index terms

An analytical and simulation performance evaluation is presented for a multi‐access protocol for a data packet radio network with a limited user capacity. The network employs direct‐sequence code division multiple access (DS‐CDMA) in a centralised channel load‐sensing scheme with channel overload (collision) detection and blocking via a separate ancillary channel state information broadcast system. Traffic models that incorporate both a finite populat ...

13 Shared-memory performance profiling
Zhichen Xu, James R. Larus, Barton P. Miller
June 1997 **ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming PPOPP '97**, Volume 32 Issue 7
Publisher: ACM Press
Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a new approach to finding performance bottlenecks in shared-memory parallel programs and its embodiment in the Paradyn Parallel Performance Tools running with the Blizzard fine-grain distributed shared memory system. This approach exploits the underlying system's cache coherence protocol to detect data sharing patterns that indicate potential performance bottlenecks and presents performance measurements in a data-centric manner. As a demonstration, Parodyn helped us improve ...

14 Comprehension processes during large scale maintenance
A. von Mayrhauser, A. M. Vans
May 1994 **Proceedings of the 16th international conference on Software engineering**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.01 MB) Additional Information: full citation, references, citings

15 An evaluation of directory protocols for medium-scale shared-memory multiprocessors
Shubhendu S. Mukherjee, Mark D. Hill
July 1994 **Proceedings of the 8th international conference on Supercomputing**

IPR2024-001429
HP – EX1002, Page 147 of 357

Publisher: ACM Press

Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, references, citings, index terms, review

This paper considers alternative directory protocols for providing cache coherence in shared-memory multiprocessors with 32 to 128 processors, where the state requirements of DirN may be considered too large. We consider DiriB, i=1,2,4, DirN, Tristate (also called superset), Coarse Vector, and three new protocols. The new protoc ...

Keywords: cache coherence, directory protocols, gray code, multiprocessors, shared-memory

16 Region division assignment: a new OVSF code reservation and assignment scheme for downlink capacity in W-CDMA systems

Rujipun Assarut, Ken'ichi Kawanishi, Ushio Yamamoto, Yoshikuni Onozato
May 2006 **Wireless Networks**, Volume 12 Issue 3

Publisher: Kluwer Academic Publishers

Full text available: pdf(3.18 MB) Additional Information: full citation, abstract, references, index terms

This work focuses on the efficient management of orthogonal-variable-spreading-factor (OVSF) codes for multimedia communications in the W-CDMA systems. Because these systems must assign only OVSF codes that are mutually orthogonal, even if they have sufficient transmission capacity they block connections for which no orthogonal OVSF codes are available. This code blocking can, with extra overhead, be eliminated by reassigning codes, but in this paper we propose an OVSF code management scheme des ...

Keywords: OVSF, W-CDMA, code assignment, code blocking

17 SPINS: security protocols for sensor netowrks

Adrian Perrig, Robert Szewczyk, Victor Wen, David Culler, J. D. Tygar
July 2001 **Proceedings of the 7th annual international conference on Mobile computing and networking**

Publisher: ACM Press

Full text available: pdf(242.17 KB) Additional Information: full citation, abstract, references, citings, index terms

As sensor networks edge closer towards wide-spread deployment, security issues become a central concern. So far, much research has focused on making sensor networks feasible and useful, and has not concentrated on security.

We present a suite of security building blocks optimized for resource-constrained environments and wireless communication. SPINS has two secure building blocks: SNEP and &mgr;TESLA SNEP provides the following important baseline security primitives: Data confidentia ...

18 SPINS: security protocols for sensor networks

Adrian Perrig, Robert Szewczyk, J. D. Tygar, Victor Wen, David E. Culler
September 2002 **Wireless Networks**, Volume 8 Issue 5

Publisher: Kluwer Academic Publishers

Full text available: pdf(213.37 KB) Additional Information: full citation, abstract, references, citings, index terms

Wireless sensor networks will be widely deployed in the near future. While much research has focused on making these networks feasible and useful, security has received little

IPR2024-001429
HP – EX1002, Page 148 of 357

attention. We present a suite of security protocols optimized for sensor networks: SPINS. SPINS has two secure building blocks: SNEP and μTESLA. SNEP includes: data confidentiality, two-party data authentication, and evidence of data freshness. μTESLA provides authenticated broadcast for severely resource-constrained ...

Keywords: MANET, authentication of wireless communication, cryptography, mobile ad hoc networks, secrecy and confidentiality, secure communication protocols, sensor networks

19 Efficient user-space protocol implementations with QoS guarantees using real-time upcalls

R. Gopalakrishnan, Gurudatta M. Parulkar

August 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 4

Publisher: IEEE Press

Full text available: pdf(205.42 KB) Additional Information: full citation, references, citings, index terms

Keywords: multimedia communication, networks, operating system kernals, processor scheduling, protocols, real-time systems, transport protocols

20 Efficient multicast stream authentication using erasure codes

Jung Min Park, Edwin K. P. Chong, Howard Jay Siegel

May 2003 **ACM Transactions on Information and System Security (TISSEC)**, Volume 6 Issue 2

Publisher: ACM Press

Full text available: pdf(312.98 KB) Additional Information: full citation, abstract, references, index terms

We describe a novel method for authenticating multicast packets that is robust against packet loss. Our focus is to minimize the size of the communication overhead required to authenticate the packets. Our approach is to encode the hash values and the signatures with Rabin's Information Dispersal Algorithm (IDA) to construct an authentication scheme that amortizes a single signature operation over multiple packets. This strategy is especially efficient in terms of space overhead, because just th ...

Keywords: Digital signatures, Information Dispersal Algorithm (IDA), erasure codes, multicast

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HP – EX1002, Page 149 of 357

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1428	(341/50,51).CCLS.	USPAT	OR	OFF	2006/10/30 09:37
L2	442	(341/50,51).CCLS.	US-PGPUB	OR	OFF	2006/10/30 09:37
L3	53	protocol function$4 block code	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/10/30 09:38
L4	0	protocol function$4 block code and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/10/30 09:38
L5	0	protocol function$4 block code and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/10/30 09:40
L6	4	protocol block code and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/10/30 09:45
L7	25	protocol block code and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/10/30 09:45

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HP – EX1002, Page 150 of 357

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OCT 10 2006
PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. 10/459,989

Filed: June 12, 2003

For: **METHOD AND APPARATUS FOR ENCODING OR DECODING DATA IN ACCORDANCE WITH AN NB/(N+1)B BLOCK CODE, AND METHOD FOR DETERMINING SUCH A BLOCK CODE**

Confirmation No.: 4900

Group Art Unit: 2819

Examiner: Brian K. Young

RESPONSE TO OFFICE ACTION MAILED ON MAY 8, 2006

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 4, 2006.

GIRARD & EQUITZ LLP Date: 10/04/06

By: _____
Alfred A. Equitz

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed May 8, 2006, in the referenced application. Please amend the application as follows and consider the following remarks.

A listing of claims begins on page 2 of this paper.

Remarks begin on page 23 of this paper.

The following listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original) A communication system, including:

a first endpoint;

a second endpoint, including physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and

wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data to recover application data and control bits, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

2. (original) The system of claim 1, wherein the line code specifies a block code and special characters, the first endpoint is configured to encode M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, where $N > M$, the code word sequence is indicative of at least one cell of the input words, and the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

3. (original)The system of claim 2, wherein the physical and link layer circuitry is configured to distinguish each of the special characters of the encoded data from each bit sequence of the code word sequence.

4. (original) The system of claim 2, wherein said at least one of the special characters is a link training character, and the physical and link layer circuitry is configured to perform physical level framing and link level framing in response to the link training character.

5. (original) The system of claim 2, wherein said at least one of the special characters is a state exchange character.

6. (original) The system of claim 2, wherein said at least one of the special characters is an idle character.

7. (original) The system of claim 6, wherein the physical and link layer circuitry is configured to perform simplex link flow control by inserting idle characters between subsequences of the code word sequence, where each of the subsequences is indicative of a different cell of the input words.

8. (original) The system of claim 2, wherein said at least one of the special characters is a flow control character.

9. (original) The system of claim 2, wherein the input words of each said cell are indicative of application data and control bits, and the control bits have multiple levels of communication protocol functionality.

10. (original) The system of claim 9, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

11. (original) The system of claim 9, wherein each said cell has a predetermined structure such that position of each bit within the cell determines whether the bit is an application data bit or a control bit, and position of each control bit within the cell determines a function of said control bit.

12. (original) The system of claim 9, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

13. (original) The system of claim 9, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension, and the physical and link layer circuitry is configured to assert to the higher level circuitry an extension-indicating control signal indicative of the value of the extension-indicating bit.

14. (original) The system of claim 13, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

15. (original) The system of claim 9, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the code word sequence is indicative of at least one cell of the input words, and the input words of each said cell are indicative of application data and control bits, and wherein the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint, and

wherein the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits therefrom, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry of the first endpoint, and the higher level circuitry of the first endpoint is configured to perform at least one higher level function in response to the at least one control signal.

16. (original) The system of claim 15, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry of the first

endpoint is configured to assert, to the higher level circuitry of the first endpoint, at least one flow control signal indicative of at least one said end-to-end flow control bit recovered by the physical and link layer circuitry of the first endpoint, and the higher level circuitry of the first endpoint includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

17. (original) The system of claim 15, wherein the additional encoded data are a sequence of the code words of the code word sequence and at least one of the special characters specified by the line code, the special characters include at least one link training character, and the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data and at least one said link training character in the additional encoded data.

18. (original) The system of claim 17, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the special characters include at least one state exchange character indicative of a received cell sequence number,

the physical and link layer circuitry of the first endpoint is configured to resume transmission of the encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the second endpoint during the training phase, and

the physical and link layer circuitry of the second endpoint is configured to resume transmission of the additional encoded data over the second channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the first endpoint during the training phase.

19. (original) The system of claim 15, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, and the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, and the special characters include an idle character, and

wherein the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform duplex link flow control in which the physical and link layer circuitry of the first endpoint inserts idle characters between subsequences of the code word sequence of the encoded data and the physical and link layer circuitry of the second endpoint inserts idle characters between subsequences of the code word sequence of the additional encoded data, where each of the subsequences is indicative of a different cell of the input words.

20. (original) The system of claim 15, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, and the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint,

wherein at least one of the control bits is a data-validity indicating bit, each said cell is indicative of at least one said data-validity indicating bit, and

the physical and link layer circuitry of the first endpoint is configured to cause each cell of the encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data and the physical and link layer circuitry of the second endpoint is configured to cause each cell of the additional encoded data to include at least one said data-indicating bit indicating that the cell includes no valid application data, at times sufficient to accomplish duplex link flow control.

21. (original) The system of claim 9, wherein the control bits of each said cell include error control bits, and the physical and link layer circuitry of the second endpoint is

configured to perform at least one of error detection and error correction, on the application data and at least some of the control bits recovered from the encoded data, using the error control bits.

22. (original) The system of claim 2, wherein N = M +1.

23. (original) A communication system, including:

a first endpoint;

a second endpoint; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to encode M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where N > M, the code word sequence is indicative of at least one cell of the input words, the input words of each said cell are indicative of application data and control bits, the control bits have multiple levels of communication protocol functionality, and the first endpoint is configured to transmit encoded data including the code words of the code word sequence over the link to the second endpoint.

24. (original) The system of claim 23, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

25. (original) The system of claim 23, wherein the block code is specified by a line code that also specifies special characters, the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, and none of the special characters of the encoded data matches a bit sequence of the code word sequence.

26. (original) The system of claim 25, wherein said at least one of the special characters is a link training character.

27. (original) The system of claim 25, wherein said at least one of the special characters is a state exchange character.

28. (original) The system of claim 25, wherein said at least one of the special characters is an idle character.

29. (original) The system of claim 25, wherein said at least one of the special characters is a flow control character.

30. (original) The system of claim 25, wherein the link has at least a first channel and a second channel, the first endpoint includes physical and link layer circuitry coupled and configured to transmit the encoded data over the first channel to the second endpoint, the second endpoint includes physical and link layer circuitry coupled and configured to transmit additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the additional encoded data include N-bit code words of a second code word sequence, and at least one of the special characters is an idle character, and

the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform duplex link flow control in which the physical and link layer circuitry of the first endpoint inserts idle characters between code words of the encoded data and the physical and link layer circuitry of the second endpoint inserts idle characters between code words of the additional encoded data.

31. (original) The system of claim 23, wherein each of the first endpoint and the second endpoint is a transceiver, and the second endpoint is configured to generate additional encoded data in response to input words in accordance with the line code and to transmit the encoded data over the link to the first endpoint.

32. (original) The system of claim 23, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

33. (original) The system of claim 23, wherein $N = M + 1$.

34. (original) The system of claim 23, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

35. (original) The system of claim 23, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension, the second endpoint includes physical and link layer circuitry coupled to the link and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry is configured to identify each extension-indicating bit indicated by the encoded data and assert to the higher level circuitry an extension-indicating control signal indicative of the value of each said extension-indicating bit.

36. (original) The system of claim 23, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry of the second endpoint includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

37. (original) The system of claim 23, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the code word sequence is indicative of at least one cell of the input words, and the input words of each said cell are indicative of application data and control bits, and wherein the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint, and

wherein the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits

therefrom, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry of the first endpoint, and the higher level circuitry of the first endpoint is configured to perform at least one higher level function in response to the at least one control signal.

38. (original) The system of claim 37, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry of the first endpoint is configured to assert, to the higher level circuitry of the first endpoint, at least one flow control signal indicative of at least one said end-to-end flow control bit recovered by the physical and link layer circuitry of the first endpoint, and the higher level circuitry of the first endpoint includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

39. (original) The system of claim 23, wherein the link has at least a first channel and a second channel, the first endpoint includes physical and link layer circuitry coupled and configured to transmit the encoded data over the first channel, the second endpoint includes physical and link layer circuitry coupled and configured to transmit additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the additional encoded data include N-bit code words of a second code word sequence, the second code word sequence is indicative of at least one cell of M-bit input words, at least one of the control bits is a data-validity indicating bit, each said cell is indicative of at least one said data-validity indicating bit, and

the physical and link layer circuitry of the first endpoint is configured to cause each cell of the encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data and the physical and link layer circuitry of the second endpoint is configured to cause each cell of the additional encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data, at times sufficient to accomplish duplex link flow control.

40. (original) The system of claim 23, wherein the control bits of each said cell include error control bits, the second endpoint includes physical and link layer circuitry

coupled to the link and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry is configured is configured to perform at least one of error detection and error correction, on the application data and at least some of the control bits recovered from the encoded data, using the error control bits.

41. (original) A communication system, including:

a first endpoint;

a second endpoint; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to generate encoded data, including by encoding M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein $N > M$, the input words are indicative of application data and control bits, the code word sequence is indicative of at least one cell of the input words, the cell includes at least one block of the application data and at least one of the control bits, the block code is specified by a line code that also specifies special characters, the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, and the first endpoint is configured to transmit the encoded data over the link to the second endpoint, wherein the control bits indicated by the encoded data, with said at least one of the special characters of the encoded data, have multiple levels of communication protocol functionality.

42. (original) The system of claim 41, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

43. (original) The system of claim 41, wherein said at least one of the special characters is a link training character.

44. (original) The system of claim 41, wherein said at least one of the special characters is a state exchange character.

45. (original) The system of claim 41, wherein said at least one of the special characters is an idle character.

46. (original) The system of claim 41, wherein said at least one of the special characters is a flow control character.

47. (original) The system of claim 41, wherein each of the first endpoint and the second endpoint is a transceiver, and the second endpoint is configured to generate additional encoded data in response to input words in accordance with the line code and to transmit the additional encoded data over the link to the first endpoint.

48. (original) The system of claim 41, wherein each said cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

49. (original) The system of claim 41, wherein $N = M + 1$.

50. (original) The system of claim 41, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

51. (original) The system of claim 41, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the input words are indicative of application data and control bits, the code word sequence is indicative of at least one cell of the input words, each said cell includes at least one block of the application data and at least one of the control bits, the additional encoded data are a sequence of the code words of the code word sequence and at least one of the special characters, the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint,

the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits therefrom, and

the second endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data transmitted by the first endpoint to recover application data and control bits therefrom,

wherein the special characters include at least one link training character, and the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data and at least one said link training character in the additional encoded data.

52. (original) The system of claim 51, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the special characters include at least one state exchange character indicative of a received cell sequence number,

the physical and link layer circuitry of the first endpoint is configured to resume transmission of the encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the second endpoint during the training phase, and

the physical and link layer circuitry of the second endpoint is configured to resume transmission of the additional encoded data over the second channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the first endpoint during the training phase.

53. (original) A receiver for receiving encoded data that have propagated over a serial link, the encoded data having been generated in accordance with a line code, said receiver including:

physical and link layer circuitry, coupled and configured to receive and decode the encoded data to recover application data and control bits, to perform at least one link level function in response to at least one of the control bits; and

higher level circuitry coupled to the physical and link layer circuitry, wherein the physical and link layer circuitry is coupled and configured to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

54. (original) The receiver of claim 53, wherein the line code specifies a block code and special characters, the encoded data are a sequence of at least one of the special characters and N-bit code words of a code word sequence, where each of the code words has been generated by encoding an M-bit input word in accordance with the block code, wherein $N > M$, the code word sequence is indicative of at least one cell of the input words, and the physical and link layer circuitry is configured to distinguish each of the special characters of the encoded data from each bit sequence of the code word sequence.

55. (original) The receiver of claim 54, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension, and the physical and link layer circuitry is configured to assert to the higher level circuitry an extension-indicating control signal indicative of the value of the extension-indicating bit.

56. (original) The receiver of claim 55, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

57. (original) The receiver of claim 54, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry is configured to assert to the higher level circuitry at least one flow control signal indicative of at least one said end-to-end flow control bit recovered by the physical and link layer circuitry, and the higher level circuitry includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

58. (original) The receiver of claim 54, wherein the special characters include at least one link training character, and the physical and link layer circuitry is configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data.

59. (original) The receiver of claim 54, wherein the control bits of each said cell include error control bits, and the physical and link layer circuitry is configured to perform at least one of error detection and error correction, on the application data and at least some of the control bits recovered from the encoded data, using the error control bits.

60. (original) The receiver of claim 54, wherein the special characters include at least one flow control character.

61. (original) The receiver of claim 53, wherein the receiver is a transceiver, the transceiver is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where $N > M$, the code word sequence is indicative of at least one cell of the input words, the input words are indicative of application data and control bits, each said cell includes at least one block of the application data and at least one of the control bits, and the transceiver is configured to transmit the additional encoded data over the link,

wherein the line code also specifies special characters, the additional encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

62. (original) The receiver of claim 61, wherein said at least one of the special characters is an idle character, and the physical and link layer circuitry is configured to perform link flow control by inserting idle characters between subsequences of the code word sequence of the additional encoded data, where each of the subsequences is indicative of a different cell of the input words.

63. (original) The receiver of claim 61, wherein each cell of the code word sequence of the additional encoded data has a predetermined structure such that position of each bit within the cell determines whether the bit is an application data bit or a control bit, and position of each control bit within the cell determines a function of said control bit.

64. (original) The receiver of claim 61, wherein each cell of the code word sequence of the additional encoded data includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

65. (original) The receiver of claim 61, wherein the special characters include at least one link training character, the physical and link layer circuitry is configured to cease transmission of the additional encoded data and enter a training phase in response to at least one said link training character in the encoded data, and the physical and link layer circuitry is configured to perform physical level and link level framing during the training phase.

66. (original) The receiver of claim 65, wherein the special characters include at least one state exchange character indicative of a received cell sequence number, and the physical and link layer circuitry is configured to resume transmission of the additional encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received over the link during the training phase.

67. (original) The receiver of claim 65, wherein the physical and link layer circuitry is configured to resume transmission of the additional encoded data over the first channel

after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by a cell sequence number indicated by data received over the link during the training phase.

68. (original) A transmitter including physical and link layer circuitry, wherein the physical and link layer circuitry include:

packetizing circuitry configured to generate M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding and transmission circuitry coupled to the packetizing circuitry and configured to encode the input words in accordance with a block code to generate a code word sequence of N-bit code words, where $N > M$, the code word sequence is indicative of at least one cell of the input words, the cell includes at least two of the control bits, and said at least two of the control bits have multiple levels of communication protocol functionality, wherein the encoding and transmission circuitry is configured to be coupled to a serial link and to transmit encoded data over the serial link, said encoded data including the code words of the code word sequence.

69. (original) The transmitter of claim 68, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

70. (original) The transmitter of claim 68, wherein the block code is specified by a line code, the line code also specifies special characters, and the encoding and transmission circuitry is configured to generate the encoded data such that said encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

71. (original) The transmitter of claim 70, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

72. (original) The transmitter of claim 70, wherein said at least one of the special characters is a link training character.

73. (original) The transmitter of claim 70, wherein said at least one of the special characters is a state exchange character.

74. (original) The transmitter of claim 70, wherein said at least one of the special characters is an idle character.

75. (original) The transmitter of claim 70, wherein said at least one of the special characters is a flow control character.

76. (original) The transmitter of claim 68, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

77. (original) The transmitter of claim 68, wherein $N = M + 1$.

78. (original) The transmitter of claim 68, wherein at least one of the control bits of each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

79. (original) The transmitter of claim 68, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension.

80. (original) The transmitter of claim 79, wherein at least one said cell also includes an address extension, and the value of the extension-indicating bit in said cell indicates that said cell includes the address extension.

81. (original) The transmitter of claim 68, wherein the control bits of each said cell include an end-to-end flow control bit.

82. (original) The transmitter of claim 68, wherein the control bits of each said cell include error control bits.

83. (original) The transmitter of claim 68, wherein the transmitter is a transceiver and the transmitter also includes:

higher level circuitry coupled to the physical and link layer circuitry, and wherein the physical and link layer circuitry also includes:

receiving and decoding circuitry configured to be coupled to the serial link and configured to receive and decode additional encoded data that have been generated in accordance with the line code and propagated over the serial link, thereby recovering application data and control bits from the additional encoded data, wherein the receiving and decoding circuitry is coupled and configured to perform at least one link level function in response to at least one of the control bits recovered from the additional encoded data, and to assert at least one control signal indicative of at least another one of the control bits recovered from the additional encoded data to the higher level circuitry, wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

84. (original) A method of encoding data, including the steps of:

generating M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding the input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein $N > M$, the code word sequence is indicative of at least one cell of the input words, the cell includes at least some of the application data and at least two of the control bits, and said at least two of the control bits have multiple levels of communication protocol functionality.

85. (original) The method of claim 84, wherein the block code is specified by a line code, the line code also specifies special characters, said method also including the step of:

generating encoded data such that the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

86. (original) The method of claim 85, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

87. (original) The method of claim 85, wherein said at least one of the special characters is a link training character.

88. (original) The method of claim 85, wherein said at least one of the special characters is a state exchange character.

89. (original) The method of claim 85, wherein said at least one of the special characters is an idle character.

90. (original) The method of claim 84, also including the step of transmitting the encoded data over a serial link.

91. (original) The method of claim 84, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

92. (original) The method of claim 84, wherein $N = M + 1$.

93. (original) The method of claim 84, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

94. (original) The method of claim 84, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension.

95. (original) The method of claim 84, wherein at least one said cell also includes an address extension, and the value of the extension-indicating bit in said cell indicates that said cell includes the address extension.

96. (original) The method of claim 84, wherein the control bits of each said cell include an end-to-end flow control bit.

97. (original) The method of claim 84, wherein the control bits of each said cell include error control bits.

98. (original) The method of claim 84, wherein the code words of each said cell belong to a virtual control channel, each said cell includes at least one block of the application data, and each said block belongs to different virtual data channel.

99. (original) The method of claim 84, wherein the levels of communication protocol functionality include at least one level of communication protocol functionality higher than link level functionality.

100. (original) A method for encoding data, including the steps of:

generating M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding the input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein $N > M$, the code word sequence is indicative of at least one cell of the input words, the cell includes at least some of the application data and at least one of the control bits, and the block code is specified by a line code that also specifies special characters; and

generating encoded data, such that the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, wherein the control bits indicated by the encoded data, with said at least one of the special characters of the encoded data, have multiple levels of communication protocol functionality.

101. (original) The method of claim 100, wherein said at least one of the special characters is a link training character.

102. (original) The method of claim 100, wherein said at least one of the special characters is a state exchange character.

103. (original) The method of claim 100, wherein said at least one of the special characters is an idle character.

104. (original) The method of claim 100, wherein said at least one of the special characters is a flow control character.

105. (original) The method of claim 100, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

106. (original) The method of claim 100, wherein $N = M + 1$.

107. (original) The method of claim 100, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

108. (original) The method of claim 100, wherein the control bits of each said cell include an end-to-end flow control bit.

109. (original) The method of claim 100, wherein the levels of communication protocol functionality include at least one level of communication protocol functionality higher than link level functionality.

REMARKS:

Claims 1-83 and 100-109 have been allowed.

Claim 84 stands rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,324,602 ("Chen"). In response, Applicant respectfully contends that this claim is patentable over the cited reference for the following reasons.

Chen fails to teach or suggest a data encoding method including either of the following limitations of claim 84:

encoding M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein N > M,

encoding input words to generate a code word sequence of code words, where the code word sequence is indicative of at least one cell (of the input words) that includes at least some application data and at least at least two control bits having multiple levels of communication protocol functionality.

Chen teaches circuitry (block 24 of Fig. 1) for encoding "n" binary bits (corresponding to an "M-bit" input word of claim 84) as a single "ternary" bit (or more than three-level bit). Thus, the output of Chen's block 24 is a voltage having one of three (or more) levels that is indicative of a single, non-binary bit (a single bit having one of at least three possible values). Chen also teaches circuitry (block 26 of Fig. 1) for encoding a single, non-binary bit (a single bit having one of at least three possible values) as "n" binary bits (corresponding to an "N-bit" code word of claim 84). Thus, the output of Chen's block 26 in response to a single voltage is a set of "n" binary bits, where "n" is greater than one. Chen fails to teach or suggest encoding M-bit input words to generate a code word sequence of N-bit code words, wherein N > M, as recited in claim 84.

Applicants disagree with the apparent assertion at page 3 of the Office Action that it would have been obvious to one of ordinary skill in the art to modify Chen's block 24 to cause it to generate a code word comprising "N" binary bits (where N is greater than "n") in response to each input word comprising "n" binary bits. This is contrary to Chen's teaching

to employ block 24 to encode "n" binary input bits as a single non-binary bit that is a voltage having one of n^2 voltage levels (e.g., to encode 2 binary input bits as a single voltage having one of 4 voltage levels), so that the non-binary bit can be transmitted over a link having fewer pin connections than would be required to transmit the same information if the information were encoded as binary bits (see Chen's teaching at col. 2, lines 43-54, for example).

Chen teaches generation of code words (e.g., the output of Chen's block 24 or 26) but fails to teach or suggest any such code word (or any sequence of such code words) is indicative of both application data and at least two control bits. At col. 5, lines 61-67, Chen teaches that the "n" binary bits input to block 24 (to be encoded as a single multi-level voltage) or output from block 26 (in response to a single multi-level voltage) consists entirely of data or control information; not both application data and control bits. Chen neither teaches nor suggests encoding input words to generate a code word sequence indicative of at least one cell (of the input words) that includes both application data and at least two control bits, and the Office Action cites no such teaching or suggestion in Chen or any other reference of record. Nor does Chen teach or suggest encoding input words to generate a code word sequence indicative of at least one cell (of the input words) that includes application data and at least two control bits having multiple levels of communication protocol functionality, and the Office Action cites no such teaching or suggestion in Chen or any other reference of record. The cited passage at Chen's col. 6, lines 22-40 refers to generation of a single multi-level voltage (a "multi-level protocol" signal, which can be considered a single-bit, non-binary "code word") having any of at least three different values; not a code word code word (or code word sequence) indicative of application data and control bits having multiple levels of communication protocol functionality as recited in claim 84. Indeed, Chen fails to teach or suggest encoding control bits having multiple levels of communication protocol functionality.

Thus, claim 84 is patentable over Chen.

The Examiner has objected to claims 85-99 (which depend directly or indirectly from claim 84) but indicated that claims 85-99 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the

foregoing explanation as to patentability of claim 84, Applicants respectfully contend that all of claims 84-99 are patentable over the art of record and in condition for allowance.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 10/4/06 By: Alfred A. Equitz

Alfred A. Equitz
Reg. No.30,922
Attorneys for Applicant(s)

Attorney Docket No. SII-3000 [SIMG0158]

OIPE IAP74
OCT 10 2006
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. 10/459,989

Filed: June 12, 2003

For: **METHOD AND APPARATUS FOR ENCODING OR DECODING DATA IN ACCORDANCE WITH AN NB/(N+1)B BLOCK CODE, AND METHOD FOR DETERMINING SUCH A BLOCK CODE**

Confirmation No.: 4900

Group Art Unit: 2819

Examiner: Brian K. Young

PETITION FOR A TWO MONTH EXTENSION OF TIME TO RESPOND UNDER 37 C.F.R. 1.136(a)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 4, 2006.

GIRARD & EQUITZ LLP Date: 10/04/06

By: _____
Jacob S. Zweig

Sir:

Applicants hereby petition for a two month extension of time to respond to the Office Action mailed May 8, 2006 in the above-referenced patent application. Please find enclosed a check in the amount of $450.00 to cover the extension fee.

The Commissioner is hereby authorized to charge payment of any **additional** fees associated with this communication, or credit any overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

10/10/2006 MGEBREM1 00000059 10459989
01 FC:1252 450.00 OP

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 10/4/06 By: _____
Alfred A. Equitz
Reg. No. 30,922

Attorneys for Applicant(s)

Attorney Docket No. SII-3000 [SIMG0158]

Rev.02/14/01

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OCT 10 2006
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GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

In re Patent Application of: BRIAN K. SCHMIDT, ET AL. Attorney's Docket No. SII-3000 [SIMG0158]

Application No. 10/459,989 Group Art Unit: 2819

Filed June 12, 2003 Confirmation No. 4900

Examiner: Brian K. Young

For: **METHOD AND APPARATUS FOR ENCODING OR DECODING DATA IN ACCORDANCE WITH AN NB/(N+1)B BLOCK CODE, AND METHOD FOR DETERMINING SUCH A BLOCK CODE**

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith are a (1) *Response to Office Action Mailed on May 8, 2006*; (2) *Petition for a Two Month Extension of Time to Respond*; and (3) *Return Postcard* in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment	Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total	109	109	0	$50	$0
Independent	7	7	0	$200	$0
☐ First Presentation of Multiple Dependent Claims				$360	$0
				Total	$0
☐ Small Entity 50 percent Filing Fee Reduction (if applicable)					$0

1. ☐ No additional fee is required.

2. ☒ A check in the amount of $450 is attached to cover the extension of time fee.

3. ☒ Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

4. ☐ Petition for extension of time. The undersigned attorney of record hereby petitions for an extension of time pursuant to 37 C.F.R. § 1.136(a), as may be required, to file this response.

GIRARD & EQUITZ LLP

October 4, 2006
Date

By: Alfred A. Equitz
Alfred A. Equitz
Registration Number 30,922
Attorney(s) or Agent(s) of Record

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Dated: 10.4.06

By: J. Zweig
Jacob Zweig

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GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

In re Patent Application of: BRIAN K. SCHMIDT, ET AL. Attorney's Docket No. SII-3000 [SIMG0158]

Application No. 10/459,989 Group Art Unit: 2819

Filed June 12, 2003 Confirmation No. 4900

Examiner: Brian K. Young

For: **METHOD AND APPARATUS FOR ENCODING OR DECODING DATA IN ACCORDANCE WITH AN NB/(N+1)B BLOCK CODE, AND METHOD FOR DETERMINING SUCH A BLOCK CODE**

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The fee has been calculated as shown below.

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Total	109	109	0	$50	$0
Independent	7	7	0	$200	$0
☐ First Presentation of Multiple Dependent Claims				$360	$0
				Total	$0
☐ Small Entity 50 percent Filing Fee Reduction (if applicable)					$0

1. ☐ No additional fee is required.

2. ☒ A check in the amount of $450 is attached to cover the extension of time fee.

3. ☒ Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed.**

4. ☐ Petition for extension of time. The undersigned attorney of record hereby petitions for an extension of time pursuant to 37 C.F.R. § 1.136(a), as may be required, to file this response.

GIRARD & EQUITZ LLP

October 4, 2006
Date

By: Alfred A. Equitz
Alfred A. Equitz
Registration Number 30,922
Attorney(s) or Agent(s) of Record

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Dated: 10.4.06

By: J. Zweig
Jacob Zweig

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: S11 - 3000

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	109	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	109 minus 20=	* 89
INDEPENDENT CLAIMS	7 minus 3 =	* 4
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OR	OTHER THAN SMALL ENTITY	
RATE	FEE			RATE	FEE
BASIC FEE	375.00		OR	BASIC FEE	750.00
X$ 9=			OR	X$18=	1602
X42=			OR	X84=	336
+140=			OR	+280=	
TOTAL			OR	TOTAL	2688

10/10/04

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 109	Minus	** 109	0
Independent	* 7	Minus	*** 7	0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE			RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X42=			OR	X84=	
+140=			OR	+280=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		OR	RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X42=			OR	X84=	
+140=			OR	+280=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		OR	RATE	ADDITIONAL FEE
X$ 9=			OR	X$18=	
X42=			OR	X84=	
+140=			OR	+280=	
TOTAL ADDIT. FEE			OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/459,989		2819	28M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 60974 on 03/16/2006

- Correspondence Address

The address of record for Customer Number 60974 is:
GIRARD & EQUITZ LLP
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,989	06/12/2003	Brian K. Schmidt	SII-3000 [SIMG0158]	4911

60974 7590 05/08/2006

GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/459,989	SCHMIDT ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-109* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-83 and 100-109* is/are allowed.

6)☒ Claim(s) *84* is/are rejected.

7)☒ Claim(s) *85-99* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/12/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

35 U.S.C. 103 Rejection

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 84 rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al.

Chen et al disclose (see figure 1) a method of encoding communication signal (between a memory device (12) and a control device (14)) data (see Data Path 18) including encoding "n" signals into a single string (block) code (Bit Compression Circuit 24). The code also includes control bits for the multiple level communication protocol data.

Chen et al recites (col. 6, lns.6-18):

> "Each BCC 24 receives the **data and control signals** from its respective bus 30. Generally, each BCC 24 functions to convert the n signals carried by the respective bus 30 into a single, multiplexed signal, which is then output on a respective bi-directional line 32. This is accomplished by compressing **the two-level protocol signals**".

Chen et al further recites (col. 6, lns.22-30):

> "Each BCC 24 has a compression rate of n-to-1--i.e., compressing n two-level protocol signals from timing generator and data path circuitry 18 into a single, **multi-level protocol signal**. For this compression, the number of distinct signal levels needed in the multi-level protocol signal is 2.sup.n. For example, if two two-level protocol signals are fed into a BCC 24 (i.e.,

n=2), four (i.e., 2.sup.2) distinct signal levels should be available in the **multi-level protocol signal**."

Chen et al further disclose that the protocol data includes "at least two control bits".

Chen et al recite (col. 6, ln.18-21):

"That is, the multi-level protocol uses three or more voltage levels for signaling, with each voltage level representing a predetermined set of values **for at least two bits of information**."

It is noted that Chen et al do not specifically recite generating "N-bit code words, wherein N is greater than M" with "M" being the "input words".

However, it would have been obvious to one of ordinary skill in the art, that the "M" input words could be represented by the input signals depicted as "n" (fig.1) of Chen et al, and further, that the "N- bit code words" of claim 84 would represent the output of the BCC encoder (24). It is further obvious that by combining the "n" code words into one codeword (block) the BCC encoder would increase the number of bits over the input code bits. This would be an obvious effect from the combination of the codewords. Further, increasing the number of bits would have been desirable so as to not reduce the information of the protocol bits and would obviously reduce the error rate.

3. Claims 85-99 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 1-83 and 100-109 are allowed.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Duvvuru, et al disclose an apparatus for processing data packets of differing protocols across different channels within signals.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

***

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-3000 [SIMG0158]	Appln. No. NEW
	Applicant(s) BRIAN K. SCHMIDT, et al.	
	Filing Date Herewith	Group Unknown

16235 U.S. PTO 10/459989 06/12/03

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
BK	AA	4,486,739	12/04/84	FRANASZEK et al.	340	347	06/30/82
BK	AB	5,144,304	09/01/92	McMAHON et al.	341	58	09/10/91
BK	AC	5,740,186	04/14/98	WIDMER	371	37.1	06/13/96
BK	AD	6,198,413 B1	03/06/01	WIDMER	341	59	07/01/99
	AE						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	NO
	AF							

OTHER DOCUMENTS

BK	AG	Widmer, Albert X., *"Partitioned DC-Balanced (0,6) 16B/18B Transmission Code"*, downloaded from the Internet on December 16, 2002 from http://www.grouper.ieee.org/groups/802/3/10G_study/public/july99/widmer_2_0799.pdf, cover sheet and pages 1-8.
BK	AH	Zhou, Tao, *"ISO/OSI, IEE 82.02, and TCP/IP, InstantDoc #22"*, dated May 1997, downloaded from the Internet on May 21, 2003 from http://www.winnetmag.com/Articles/Print.cfm?ArticleID=22, two pages.
	AI	

Examiner	Date Considered
B.K.	4/13/06

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 10/459,989	Applicant(s)/Patent Under Reexamination SCHMIDT ET AL.	
	Examiner Brian Young	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,765,916	07-2004	Duvvuru et al.	370/395.5
*	B	US-6,324,602	11-2001	Chen et al.	710/68
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/459,989	SCHMIDT ET AL.
Examiner	**Art Unit**
Brian Young	2819

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/459,989	SCHMIDT ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

SEARCHED			
Class	Subclass	Date	Examiner
341	50,67,65, 101,59, 106	4/26/2006	BY
370	389,392	4/26/2006	by

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
East (see attached) NPL (see attached) consulted Pri. Ex. H.Williams and Pri. Ex. P. JeanPierre.	4/26/2006	BY

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Bib Data Sheet

CONFIRMATION NO. 4911

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,989	06/12/2003 RULE	341	2819	SII-3000 [SIMG0158]

APPLICANTS

Brian K. Schmidt, Mountain View, CA;

James G. Hanko, Redwood City, CA;
J. Duane Northcutt, Menlo Park, CA;Alan T. Ruberg, Menlo Park, CA;

** CONTINUING DATA ********** (no)

** FOREIGN APPLICATIONS ********** (no)

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/05/2003

Foreign Priority claimed ☐ yes ☑ no 35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance Verified and Acknowledged Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 2	TOTAL CLAIMS 109	INDEPENDENT CLAIMS 7

ADDRESS
60974
GIRARD & EQUITZ LLP
400 MONTGOMERY STREET
SUITE 1110
SAN FRANCISCO , CA
94104

TITLE
Method and system for encapsulation of multiple levels of communication protocol functionality within line codes

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

IPR2024-001429
HP – EX1002, Page 190 of 357

EAST Search History

L36	1032	protocol.ti. multiple.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/27 13:30
L37	888	protocol.ti. multiple.ti.	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/27 13:31
L38	2648	(370/389,392,395.5).CCLS.	USPAT	OR	OFF	2006/04/27 13:31

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **VHDL implementation of a bidirectional interface for 3ATI avionic sub-sys**
Mahdian, P.; Griebling, M.;
Digital Avionics Systems Conference, 2004. DASC 04. The 23rd
Volume 2, 24-28 Oct. 2004 Page(s):11.C.5 - 11.1-7 Vol.2
AbstractPlus | Full Text: PDF(688 KB) **IEEE CNF**
Rights and Permissions

2. **Transmission of embedded VBR multimode encoded speech on UMTS cc channels**
Babich, E.; Deotto, L.; Vatta, E.;
Vehicular Technology Conference, 2000. IEEE VTS-Fall VTC 2000. 52nd
Volume 3, 24-28 Sept. 2000 Page(s):1405 - 1411 vol.3
Digital Object Identifier 10.1109/VETECF.2000.886327
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3. **Adaptive bandwidth-constrained media-specific forward error correction Internet Protocol**
Lee Kah Wah; Tan Chee Heng;
Networks, 2002. ICON 2002. 10th IEEE International Conference on
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4. **Analysis of a joint video coding system**
Teixeira, L.;
Data Compression Conference, 1998. DCC '98. Proceedings
30 March-1 April 1998 Page(s):576
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25-28 May 1997 Page(s):149 - 157
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6. **JPEG2000 - choices and tradeoffs for encoders**
Varma, K.; Bell, A.;
Signal Processing Magazine, IEEE
Volume 21, Issue 6, Nov. 2004 Page(s):70 - 75
Digital Object Identifier 10.1109/MSP.2004.1359144
AbstractPlus | References | Full Text: PDF(1472 KB) **IEEE JNL**
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7. **Error-resilient wireless video transmission using motion-based unequal e and intraframe packet interleaving**
Qu, Q.; Pei, Y.; Modestino, J.W.; Tian, X.;
Image Processing, 2004. ICIP '04. 2004 International Conference on
Volume 2, 24-27 Oct. 2004 Page(s):837 - 840 Vol.2
Digital Object Identifier 10.1109/ICIP.2004.1419429
AbstractPlus | Full Text: PDF(669 KB) **IEEE CNF**
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8. **A feedback system for graphics video coding and networking**
Dongmei Wang; Mersereau, R.M.;
Acoustics, Speech, and Signal Processing, 2001. Proceedings. (ICASSP '01). International Conference on
Volume 3, 7-11 May 2001 Page(s):1473 - 1476 vol.3
Digital Object Identifier 10.1109/ICASSP.2001.941209
AbstractPlus | Full Text: PDF(552 KB) **IEEE CNF**
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9. **Network-aware error control using smooth and fast rate adaptation mech friendly Internet video**
Young-Gook Kim; JongWon Kim; Kuo, C.-C.J.;
Computer Communications and Networks, 2000. Proceedings. Ninth Internatio on
16-18 Oct. 2000 Page(s):320 - 325
Digital Object Identifier 10.1109/ICCCN.2000.885509
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Best 200 shown Relevance scale

1 Mixed-level cosimulation for fine gradual refinement of communication in SoC design
G. Nicolescu, S. Yoo, A. Jerraya
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Publisher: IEEE Press
Full text available: pdf(172.53 KB) Additional Information: full citation, references, citings, index terms

2 Case studies: A low-cost and low-power multi-standard video encoder
R. Peset Llopis, R. Sethuraman, C. Alba Pinto, H. Peters, S. Maul, M. Oosterhuis
October 2003 **Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**
Publisher: ACM Press
Full text available: pdf(541.20 KB) Additional Information: full citation, abstract, references, index terms

Video encoders are an important IP block in mobile multimedia systems. In this paper, we describe a low-cost low-power multi-standard (MPEG4, JPEG, and H.263) video/image encoder. The low-cost and low-power aspects are achieved by the right choice of algorithms and architectures. In the algorithm front, an embedded compression technique for reducing the size of loop memory has enabled a single-chip low-cost realization of the encoder. In the architectural front, an efficient hardware-software pa ...

Keywords: ASIPs, hardware/software partitioning, low-cost, low-power, multi-standard, video encoder

3 A simple encoder for fieldbus applications
Raja Prasad, Ulloa Gonzalo
January 1993 **ACM SIGCOMM Computer Communication Review**, Volume 23 Issue 1
Publisher: ACM Press
Full text available: pdf(482.64 KB) Additional Information: full citation, abstract, index terms

In this paper we present a Simple Encoder for Fieldbus applications. The Simple Encoder is tailored to support the special kind of data transfer in a Fieldbus. The encoding rules have been simplified to such an extent that only required information between peers are exchanged, so that the coding/decoding process does not cause any significant delay during real time operation of the network. The PDUs obtained are upto 55% shorter than PDUs of Basic Encoding Rules, *BER*, and the Simple Encod ...

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HP – EX1002, Page 194 of 357

4 High level and architectural synthesis: System-level abstraction semantics

Andreas Gerstlauer, Daniel D. Gajski
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
Publisher: ACM Press

Full text available: pdf(167.46 KB) Additional Information: full citation, abstract, references, citings, index terms

Raising the level of abstraction is widely seen as the solution for closing the productivity gap in system design. They key for the success of this approach, however, are well-defined abstraction levels and models. In this paper, we present such system level semantics to cover the system design process. We define properties and features of each model. Formalization of the flow enables design automation for synthesis and verification to achieve the required productivity gains. Through customizati ...

Keywords: abstraction levels, design semantics, methodology, modeling, system-level design

5 On-Chip Stochastic Communication

Tudor Dumitras, Radu Marculescu
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society

Full text available: pdf(214.47 KB) Publisher Site Additional Information: full citation, abstract, index terms

As CMOS technology scales down into the deep-submicron (DSM) domain, the costs of design and verification for Systems-On-Chip (SoCs) are rapidly increasing due to the inefficiency of traditional CAD tools. Relaxing the requirement of 100% correctness for devices and interconnects drastically reduces the costs of design but, at the same time, requires that SoCs be designed with some system-level fault-tolerance. In this paper, we introduce a new communication paradigm for SoCs, namely stochastic ...

6 SoC and NoC: Towards on-chip fault-tolerant communication

Tudor Dumitraş, Sam Kerner, Radu Mărculescu
January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**
Publisher: ACM Press

Full text available: pdf(465.99 KB) Additional Information: full citation, abstract, references

As CMOS technology scales down into the deep-submicron (DSM) domain, devices and interconnects are subject to new types of malfunctions and failures that are harder to predict and avoid with the current system-on-chip (SoC) design methodologies. Relaxing the requirement of 100% correctness in operation drastically reduces the costs of design but, at the same time, requires SoCs be designed with some degree of system-level fault-tolerance. In this paper, we introduce a high-level model of DSM fai ...

7 Performance evaluation of an adaptive-rate MPEG encoder matching intserv traffic constraints

Alfio Lombardo, Giovanni Schembra
February 2003 **IEEE/ACM Transactions on Networking (TON)**, Volume 11 Issue 1
Publisher: IEEE Press

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, index terms

Promoting the evolution of the Internet from a simple data network to a true multiservice

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HP – EX1002, Page 195 of 357

network today constitutes a challenging task. To this end, the Internet Engineering Task Force (IETF) has set up the Integrated Services (Intserv) and Differentiated Services (DiffServv) Working Groups, with the goal of defining a next-generation Internet, in which traditional best-effort datagram delivery and additional enhanced quality of service delivery classes coexist. The IntServ framework, in particul ...

Keywords: MPEG, Markov modeling, TSpec, performance evaluation, quantizer scale parameter, rate control

8 De-layered grid storage server

H. Shrikumar

July 2005 **ACM SIGBED Review**, Volume 2 Issue 3

Publisher: ACM Press

Full text available: pdf(750.59 KB) Additional Information: full citation, abstract, references, index terms

Networks have become faster and disks have become fatter at a pace that, despite Moore's law, CPU developments have simply not been been able to keep up with. We present a Grid Storage Server which is capable of scaling up to meet the "terabit-terabyte" demands of very large scale grid computation applications with large data sets.The Grid Storage Server is implemented almost completely in silicon, whether FPGA or ASIC; the fast-path of this server does not use a CPU or von Neumann style (instru ...

9 RMDP: an FEC-based reliable multicast protocol for wireless environments

Luigi Rizzo, Lorenzo Vicisano

April 1998 **ACM SIGMOBILE Mobile Computing and Communications Review**, Volume 2 Issue 2

Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings

In this paper we present a Reliable Multicast data Distribution Protocols (RMDP), and discuss its performance. The protocol is based on the use of FEC techniques to drastically reduce the impact of independent losses for different receivers, which make ARQ-based protocols perform very poorly as the number of receivers grows. The protocol is well-suited to the use with mobile equipment because of its simplicity, robustness to losses, moderate demand for feedback, and scalability.

10 Dimensions: why do we need a new data handling architecture for sensor networks?

Deepak Ganesan, Deborah Estrin, John Heidemann

January 2003 **ACM SIGCOMM Computer Communication Review**, Volume 33 Issue 1

Publisher: ACM Press

Full text available: pdf(214.08 KB) Additional Information: full citation, abstract, references, index terms

An important class of networked systems is emerging that involve very large numbers of small, low-power, wireless devices. These systems offer the ability to sense the environment densely, offering unprecedented opportunities for many scientific disciplines to observe the physical world. In this paper, we argue that a data handling architecture for these devices should incorporate their extreme resource constraints - energy, storage and processing - and spatio-temporal interpretation of the phys ...

11 Addressing the system-on-a-chip interconnect woes through communication-based design

M. Sgroi, M. Sheets, A. Mihal, K. Keutzer, S. Malik, J. Rabaey, A. Sangiovanni-Vencentelli

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: Additional Information: full citation, abstract, references, citings, index

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pdf(180.03 KB) terms

Communication-based design represents a formal method approach to of system-on-a-chip design that considers communication between components as important as the computations they perform. "Our network-on-chip&rdqo ; approach partitions the communication into layers to maximize reuse and provide a programmer with an abstraction of the underlying communication framework. This layered approach is cast in the structure advocated by the OSI Reference network model and is demonstrated with ...

Keywords: communication-based design, network-on-chip, platform-based design, protocol stack

12 (Special session) presentation + poster disscussion: university design contest: A bandwidth and memory efficient MPEG-4 shape encoder

Kun-Bin Lee, Nelson Yen-Chung Chang, Hao-Yun Chin, Hui-Cheng Hsu, Chein-Wei Jen

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(95.79 KB) Publisher Site Additional Information: full citation, abstract, references

We have developed a shape encoder hardware for MPEG-4 video coding. On the one hand, the alpha component is compressed and therefore, the size and memory access of alpha frame memory can be reduced to 50% and 56.25% respectively. On the other hand, an efficient data transfer scheme combining the run length coding and addressing mode can reduce average data transfer time to 9.39% and accelerate the shape encoding process. The shape encoder can support MPEG-4 Main Profile at Level 4 in real-time. ...

13 A Memory-based Architecture for MPEG2 System Protocol LSIs

Minoru Inamori, Jiro Naganuma, Haruo Wakabayashi, Makoto Endo

March 1996 **Proceedings of the 1996 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(778.55 KB) Publisher Site Additional Information: full citation, abstract

This paper proposes a memory-based architecture implementing the MPEG2 System protocol LSIs, and demonstrates its flexibility and performance. The memory-based architecture implements the full functionality of the MPEG2 System protocol for both multiplexing and de-multiplexing MPEG2-encoded streams. It consists of a core CPU, memories, and dedicated application-specific hardware. It is designed and optimized by hardware/software co-design techniques. The LSIs provide sufficient performance and f ...

Keywords: MPEG2, Multiplexor, De-multiplexor, HW/SW co-design

14 Efficient encoding of application layer PDU's for fieldbus networks

J. R. Pimentel

May 1988 **ACM SIGCOMM Computer Communication Review**, Volume 18 Issue 3

Publisher: ACM Press

Full text available: pdf(1.35 MB) Additional Information: full citation, abstract, index terms

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A new and efficient encoder suitable for encoding application layer PDU's is suggested. Because of its good efficiency, it is particularly useful for fieldbus networks where real time behaviour is a major requirement. The encoder is able to work with ASN. 1 syntax rules and produces a new transfer syntax which can be negotiated with the ISO presentation layer. The overhead length required by the new encoder is at least half of that required by ASN. 1 encoding. Several examples using MMS protocol ...

15 Automatic generation of application-specific architectures for heterogeneous multiprocessor system-on-chip

Damien Lyonnard, Sungjoo Yoo, Amer Baghdadi, Ahmed A. Jerraya

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(285.15 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a design flow for the generation of application-specific multiprocessor architectures. In the flow, architectural parameters are first extracted from a high-level system specification. Parameters are used to instantiate architectural components, such as processors, memory modules and communication networks. The flow includes the automatic generation of communication coprocessor that adapts the processor to the communication network in an application-specific way. Experiments with ...

16 Automated testing of protocol specifications and their implementations

H. Ural, R. L. Probert

June 1984 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM symposium on Communications architectures and protocols: tutorials & symposium SIGCOMM '84**, Volume 14 Issue 2

Publisher: ACM Press

Full text available: pdf(565.31 KB) Additional Information: full citation, abstract, references, citings, index terms

A highly automated approach is proposed for validating the consistency of distinct representations of an identical software functionality. This approach is based on checking whether the observable behaviors presented by software functionality representations given in different levels of abstraction are consistent with one another. These representations are encoded in a relatively mechanical way as procedures in sequential PROLOG, a very high level language. The approach is extremely flexibl ...

17 Leading edge design methodology for SoCs and SiPs: High-level architecture exploration for MPEG4 encoder with custom parameters

Marius Bonaciu, Aimen Bouchhima, Wassim Youssef, Xi Chen, Wander Cesario, Ahmed Jerraya

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(428.49 KB) Additional Information: full citation, abstract, references

this paper proposes the use of a high-level architecture exploration method for different MPEG4 video encoders using different customization parameters. The targeted architecture is a heterogeneous MP-SoC which may include up 2 coarse grain SIMD (task level SIMD) subsystems to perform the computations. The customization parameters are related to video resolution, frame rate, Communication Network, level of parallelism and CPU types. These parameters are determined during the high-level architect ...

Keywords: MPEG4, architecture exploration, customization, multiprocessors SOC architecture, video encoder

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18 Papers: A novel wide-band audio transmission scheme over the Internet with a smooth quality degradation

Fulvio Babich, Marko Vitez
January 2000 **ACM SIGCOMM Computer Communication Review**, Volume 30 Issue 1
Publisher: ACM Press
Full text available: pdf(768.81 KB) Additional Information: full citation, abstract, references

Real-time delivery of multimedia information over the Internet is finding increasing interest. This paper considers wide-band audio transmission utilizing a priority scheme. The proposed scheme complies with both the new Internet Protocol Version 6 (IPv6) and the current Internet Protocol Version 4 (IPv4), providing that, in the latter case, routers are set to manage priority. A new queuing algorithm, namely Priority Weighted Fair Queuing (PWFQ), is defined and evaluated. A scalable audio encode ...

Keywords: Audio on Demand, INternet applications, Multimedia, Quality of Service, Technical subjects, Weighted Fair Queuing

19 An integrated test center for SL-10 packet networks

M. W. A. Hornbeek
September 1985 **ACM SIGCOMM Computer Communication Review , Proceedings of the ninth symposium on Data communications SIGCOMM '85**, Volume 15 Issue 4
Publisher: ACM Press
Full text available: pdf(742.99 KB) Additional Information: full citation, abstract, references, index terms

The sheer scale and complexity of large data networks makes testing them a daunting task. System commissioning, release acceptance, network troubleshooting, performance testing, host conformance testing, and certification are all operational activities that involve testing. Packet switching systems typically provide built-in features to help with hardware level test operations such as modem loopback commands, system failure alarms and system selftests. However, testing system and protocol l ...

20 Controller optimization for protocol intensive applications

A. Crews, F. Brewer
September 1996 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(140.14 KB) Additional Information: full citation, references, citings, index terms

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"20040136401"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 10:02
L2	122	protocol code block control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:03
L3	27	protocol code block control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:03
L4	16	protocol code block control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:04
L5	0	protocol code block control bit m n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:04
L6	6	protocol code block control bit m n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:05
L7	0	protocol code block control bit m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:06
L8	1	protocol code block control bit m NEAR1 n	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:07

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EAST Search History

L9	2	protocol code control bit m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:09
L10	0	protocol layer code bit m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:09
L11	4	protocol layer bit m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:10
L12	1	protocol layer bit m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:10
L13	89	protocol m NEAR1 n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:10
L14	10	protocol m NEAR1 n bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:11
L15	0	protocol "n &GT m" bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:13
L16	12	"n &GT m" bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:13
L17	0	protocol "n &GT m" bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:13
L18	3	protocol "n &GT m" bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 10:14

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L19	3	protocol "n &GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 12:44
L20	0	protocol "n GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 10:16
L21	89	protocol n NEAR1 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:17
L22	2	protocol n NEAR1 m control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:22
L23	3	protocol layer n NEAR1 m control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:34
L24	3443	protocol level communication	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:36
L25	1	protocol level communication n m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 10:37
L26	60	protocol level communication n m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:37
L27	3	protocol WITH level WITH communication n NEAR3 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 10:39
L28	0	protocol NEAR3 level NEAR3 communication n NEAR5 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:39

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L29	682	protocol NEAR3 level and n NEAR5 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:37
L30	1677	protocol layer and n NEAR5 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:31
L31	501	protocol NEAR1 layer and n NEAR5 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:31
L32	34	protocol NEAR1 layer n NEAR5 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:34
L33	24	protocol NEAR1 layer n NEAR5 m control	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 12:34
L35	934	protocol NEAR2 level application	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:40
L36	0	protocol NEAR2 level n ADJ2 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:40
L37	0	protocol NEAR2 level n near2 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:41
L38	3	protocol NEAR2 level same n near2 m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:42
L39	8	protocol NEAR2 level block code	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:43

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L40	0	protocol NEAR2 level block code n m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:43
L41	0	protocol NEAR2 level block n m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:43
L42	1	protocol NEAR2 level same block same n m	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:43
L43	0	block communication control bit "n &GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:45
L44	0	block control bit "n &GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:45
L45	1	control bit "n &GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:45
L46	0	protocol "n &GT m"	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:46
L47	3128	protocol greater	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:46
L48	168	protocol level greater	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:48
L49	0	protocol multiple level greater than	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:48

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L50	541	protocol multiple level	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:49
L51	103	protocol NEAR3 multiple NEAR4 level	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:51
L52	0	protocol NEAR3 multiple NEAR4 level bit block	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:51
L53	0	protocol NEAR3 multiple NEAR4 level SAME bit block	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 12:51
L54	6	protocol NEAR3 multiple NEAR4 level bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:01
L55	1	protocol NEAR3 multiple NEAR4 level same control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:02
L56	2	protocol NEAR3 multiple NEAR4 level same control same bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:23
L57	2	protocol NEAR3 multiple NEAR4 level same control same bit and serial	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:09
L58	1	protocol NEAR3 multiple NEAR4 level same control same bit and serial and error	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:08
L59	1	protocol NEAR3 multiple NEAR4 level same control same bit and link	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:09

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L60	6	protocol NEAR3 multiple NEAR4 layer same control same bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:40
L61	7	protocol NEAR4 multiple NEAR4 layer same control same bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:40
L62	1	protocol NEAR4 multiple NEAR4 layer same control same bit not l60	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:41
L63	11	protocol NEAR2 multiple control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:43
L64	2	protocol NEAR multiple control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:44
L65	0	protocol NEAR multiple same control near bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:44
L66	1	protocol NEAR multiple same control near2 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:45
L67	3	protocol NEAR2 multiple same control near2 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:51
L68	54	protocol NEAR2 layer same control near2 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:49
L69	7	protocol NEAR2 layer with control near2 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:49

EAST Search History

L70	381	protocol NEAR2 multiple control	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:51
L71	11	protocol NEAR2 multiple control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:57
L72	2	protocol NEAR multiple control bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 13:57
L73	69	protocol NEAR multiple control ADJ1 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 13:59
L74	222	protocol NEAR multiple.ti.	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 13:59
L75	5	protocol NEAR multiple NEAR3 bit	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 14:02
L76	123	protocol NEAR multiple bit NEAR2 protocol	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 14:24
L77	62	protocol NEAR multiple data WITH bit NEAR2 protocol	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/26 14:25
L78	0	protocol NEAR multiple and data WITH bit NEAR2 protocol m n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/26 15:09
L79	1	protocol NEAR multiple and data WITH bit NEAR2 protocol m n	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 15:11

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L80	0	protocol NEAR multiple and data WITH bit NEAR2 protocol block	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 15:11
L81	5	protocol NEAR multiple and data bit NEAR2 protocol block	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/26 15:11

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Employee number: **66033**
Art Unit: **GROUP ART UNIT 2819**
Office Location: **JEF 05A55**
Phone Number: **(571)272-1816**
Maibox Number:

Case serial number: **10/459989**
Class / Subclass(es): **341/50**
Earliest Priority Filing Date: **6/12/03**
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Young, Brian

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Email address: **BRIAN.YOUNG@USPTO.GOV**
Employee number: **66033**
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Office Location: **JEF 05A55**
Phone Number: **(571)272-1816**
Maibox Number:

Case serial number: **10/459989**
Class / Subclass(es): **341/50**
Earliest Priority Filing Date: **6/12/03**
Format preferred for results: **E-mail**
Search Topic Information:
encoding data application data control bit multiple levels communication protocol
Special Instructions and Other Comments:

4/25/06

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	scrambl$.ti. "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:26
L2	178	(341/87).CCLS.	USPAT	OR	OFF	2006/04/25 11:26
L3	3	l2 and scrambl$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:29
L4	23	("20020044767"|"20020049949"|"5377265"|"5712863"|"5815514"|"5931968"|"6177890"|"6260171"|"6308295"|"6363512"|"6438724"|"6513139").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:42
L5	3	l4 and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:30
L6	763	"380".clas. scrambl$.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:45
L7	0	"380".clas. scrambl$.ti. rll.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:45
L8	0	"380".clas. scrambl$.ti. and rll	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 11:45

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EAST Search History

L9	763	"380".clas. scrambl$.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/25 13:36
L10	3	control bit multiple levels communication protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/25 13:37
S1	2792	control bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:52
S2	285	control bit level protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:52
S3	11	control NEAR1 bit level protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:59
S4	0	Schmidt Brian "K."	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00
S5	0	Schmidt Brian "K."	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/24 10:00
S6	103	Schmidt Brian	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00

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EAST Search History

S7	4	Schmidt Brian k	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00
S8	4	Schmidt Brian k and protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:01
S9	3	Schmidt Brian k and protocol control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:04
S10	2494	(341/50,67,65,101,59,106).CCLS.	USPAT	OR	OFF	2006/04/24 10:04
S11	2	protocol block code control NEAR1 bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:17
S12	2	protocol block code control NEAR1 bit and protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:09
S13	6	protocol block code control NEAR3 bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:32
S14	12	protocol level block code control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 15:32
S15	62	protocol level block bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 11:07

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EAST Search History

S16	1032	protocol level block	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 11:07
S17	285	protocol level control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 12:55
S18	15	protocol level block code bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/25 11:24

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2792	control bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:52
L2	285	control bit level protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:52
L3	11	control NEAR1 bit level protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 09:59
L4	0	Schmidt Brian "K."	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00
L5	0	Schmidt Brian "K."	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/24 10:00
L6	103	Schmidt Brian	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00
L7	4	Schmidt Brian k	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:00
L8	4	Schmidt Brian k and protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:01

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EAST Search History

L9	3	Schmidt Brian k and protocol control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:04
L10	2494	(341/50,67,65,101,59,106).CCLS.	USPAT	OR	OFF	2006/04/24 10:04
L11	2	protocol block code control NEAR1 bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:17
L12	2	protocol block code control NEAR1 bit and protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:09
L13	6	protocol block code control NEAR3 bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 10:32
L14	12	protocol level block code control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 15:32
L15	62	protocol level block bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 11:07
L16	1032	protocol level block	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 11:07
L17	285	protocol level control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 12:55

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EAST Search History

L18	15	protocol level block code bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/24 15:32

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"4,736,189".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 08:55
L2	1	"4,736,189".pn. averag$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 09:22
L3	349	ieee "802.2"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	NEAR	ON	2006/04/13 09:23
L4	74	ieee "802.2" control protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 09:25
L5	1	ieee "802.2" control bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 09:26
L6	5	ieee "802.2" control with bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:29
L7	0	ieee "802.2" control with bit protocol level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:28
L8	1	ieee "802.2" control with bit protocol and n m	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:30

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EAST Search History

L9	5	ieee "802.2" control with bit protocol and application	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:31
L10	5	ieee "802.2" control with bit protocol and a	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:33
L11	0	ieee "802.2" control with bit protocol and functionality	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:32
L12	13	ieee "802.2" functionality	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:32
L13	12	ieee "802.2" protocol functionality	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:32
L14	9	ieee "802.2" control with bit and protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:33
L15	0	ieee "802.2" control with bit and protocol functionality	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:34
L16	7	ieee "802.2" control same bit and protocol functionality	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:36

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EAST Search History

L17	4	ieee "802" control same bit protocol llc mac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:43
L18	0	ieee "802" control with bit protocol llc mac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:37
L19	0	ieee "802" control with bit protocol llc mac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:49
L20	0	ieee "802" control with bit protocol mac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:49
L21	2	ieee "802" control with bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:51
L22	4	ieee "802" multiple level control bit protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:55
L23	3	ieee "802" multiple WITH protocol control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:56
L24	29	ieee "802" multiple WITH protocol and control WITH bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:56

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EAST Search History

L25	4	ieee "802" multiple NEAR3 protocol and control WITH bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:58
L26	0	ieee "802" multiple NEAR3 protocol level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 09:58
L27	34	ieee "802" protocol NEAR3 level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/04/13 10:06
L28	24	(multiple level protocol).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 10:07
L29	1	(multiple level protocol).ti. control NEAR1 bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 10:08
L30	0	(multiple level protocol).ti. control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:08
L31	1	(multiple level protocol).ti. and control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:09
L32	9	(multiple level protocol).ti. and control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:12

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EAST Search History

L33	3	(multiple NEAR2 level NEAR2 protocol).ti. and control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:13
L34	108	(multiple NEAR2 level NEAR2 protocol)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:13
L35	0	(multiple NEAR2 level NEAR2 protocol) control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:14
L36	0	(multiple NEAR2 level NEAR2 protocol) SAME control bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:14
L37	14	(multiple NEAR2 level NEAR2 protocol) SAME control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:15
L38	0	(multiple NEAR2 level NEAR2 protocol) SAME control same bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:15
L39	31	(multiple NEAR2 level NEAR2 protocol) and control same bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 10:15
L40	18	(multiple NEAR2 level NEAR2 protocol) and control with bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 12:19

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EAST Search History

L41	8	("4486739"|"5144304"|"5740186"|"6198413").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 12:19
L42	8	("4486739"|"5144304"|"5740186"|"6198413").PN.	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/04/13 12:19
L43	108	(multiple NEAR2 level NEAR2 protocol)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 12:19
L44	0	(multiple NEAR2 level NEAR2 protocol) and l42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 12:20
L45	422819	protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 12:20
L46	2	protocol and l42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/04/13 12:20

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OIPE JC61
FEB 13 2004
PATENT & TRADEMARK OFFICE

2688

PATENT

#3/3-3-04
V-Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
FEB 18 2004

APPLICATION FOR UNITED STATES PATENT

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. 10/459,989

Filed: June 12, 2003

For: **METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES**

Group Art Unit: 2688 Technology Center 2600

Examiner: Unknown

TRANSMITTAL OF POWER OF ATTORNEY BY ASSIGNEE

RECEIVED
FEB 19 2004
TC 2600

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 10, 2004.

GIRARD & EQUITZ LLP Date: 02/10/04

By: Marsha A. Townsend
Marsha A. Townsend

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The *Power of Attorney by Assignee and Establishment of Right of Assignee to Prosecute Under 37 C.F.R. § 3.73(b)* is hereby submitted in the above application and it is respectfully requested that it be made of record.

Respectfully submitted,

GIRARD & EQUITZ LLP

Dated: 2/10/04 By: Alfred A Equitz

Alfred A. Equitz
Reg. No.30,922

Attorneys for Applicant(s)

Attorney Docket No.: SII-3000 [SIMG0158]

OIPE JC61
FEB 13 2004
PATENT & TRADEMARK OFFICE

Attorney Docket No.: SII-3000 [SIMG0158]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR UNITED STATES PATENT

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. 10/459,989

Filed: June 12, 2003

For: **METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES**

Group Art Unit: 2688

Examiner: Unknown

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 C.F.R. §3.73(b)

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

RECEIVED
FEB 18 2004
Technology Center 2600

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SILICON IMAGE, INC., assignee of the entire right title and interest in the above-identified application by assignment dated **June 11, 2003**, which assignment is [X] recorded in the Patent and Trademark Office at **Reel 014174, Frame 0541**, or [ ] a copy of which is submitted herewith, and hereby appoints the members of the firm of GIRARD & EQUITZ LLP, a firm composed of

Philip A. Girard 28,848 Alfred A. Equitz 30,922

400 Montgomery Street, Suite 1110, San Francisco, CA 94104, (415) 433-2250, FAX (415) 433-2255, as its attorneys/agents with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith. The undersigned is empowered to sign this statement and appointment on behalf of assignee.

Please direct all correspondence regarding this application to the following:

GIRARD & EQUITZ LLP
Attn: Alfred A. Equitz
400 Montgomery Street. Suite 1110
San Francisco, CA 94104
Telephone: (415) 433-2250
Facsimile: (415) 433-2255

The assignee certifies that it has reviewed the assignment and to the best of the assignee's knowledge and belief, title is in the assignee.

SILICON IMAGE, INC.

Dated: 2/5/04 By: _____

Name: Howard Freedland

Title: V.P., & General Counsel

06-13-03

15592 U.S. PTO 06/12/03

GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110, San Francisco, CA 94104
415/433-2250

Address to:
Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney's Docket No. SII-3000
[SIMG0158]
First Named Inventor BRIAN K. SCHMIDT

16235 U.S. PTO 10/459989 06/12/03

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:

METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, June 12, 2003, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EV 322540235 US addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Marsha A. Townsend Marsha A. Townsend
(Name of person mailing paper) (Signature)

Enclosed are:

1. X Transmittal Form (two copies required)

2. The papers required for filing date under CFR § 1.53(b):
   a. 111 Pages of specification (including claims and abstract);
   b. 2 Sheets of drawings.
      X formal _ informal

3. Declaration or oath

   a. X New original

   b. _ Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Item 12 completed)

   _ Incorporation By Reference (to be used if Item 3b is checked)

   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

   i. _ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

4. _ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

5. _ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

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ACCOMPANYING APPLICATION PARTS

6. X An assignment of the invention to SILICON IMAGE, INC. is attached (including Form PTO-1595).

7. __ Power of Attorney

8. X An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and 6 references.

9. __ Preliminary Amendment.

10. X Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

11. X Other - Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i).

12.. FOREIGN PRIORITY
[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

13. FEE CALCULATION

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($750)
Total Claims	109 – 20	*89	x $18.00	1602.00
Independent Claims	7 – 3	*4	x $84.00	336.00
__ Multiple dependent claim(s), if any			$280.00	0

*If less than zero, enter "0".

Filing Fee Calculation $2,688.00

50% Filing Fee Reduction (if applicable) . . . . . $

14. Small Entity Status
a. __ A small entity statement is enclosed.
b. __ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. __ is no longer claimed.

15. Other Fees
X Recording Assignment [$40.00] $40.00
__ Other fees
Specify _____ .....$

Total Fees $2,728.00

16. Payment of Fees
X Checks in the amount of $2,688.00 (for application fee) and $40.00 (for recordation of assignment) are enclosed.
__ Charge Account No. 50-1697 in the amount of $.
A duplicate of this transmittal is attached.

17. All correspondence regarding this application should be forwarded to the undersigned attorney:

Alfred A. Equitz
GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
Telephone: 415/433-2250
Facsimile: 415/433-2255

18. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 50-1697. **A duplicate of this transmittal is attached**.

GIRARD & EQUITZ LLP

June 12, 2003
(Date)

By: Alfred A. Equitz
Alfred A. Equitz
Registration No. 30,922
Attorney(s) or Agent(s) of Record

Attorney Docket No. SII-3000 [SIMG0158]

10/459969 .061203

Express Mail Number EV 322540235 US

PTO/SB/35 (11-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)		
	First Named Inventor	BRIAN K. SCHMIDT
	Title	METHOD AND APPARATUS FOR ENCAPSULATION OF MULTIPLE LEVELS OF...
	Atty Docket Number	SII-3000 [SIMG0158]

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

June 12, 2003
Date

Alfred A. Equitz
Signature

ALFRED A. EQUITZ, Registration No. 30, 922
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

06-13-03

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney's Docket No. SII-3000
[SIMG0158]
First Named Inventor BRIAN K. SCHMIDT



UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:

METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, June 12, 2003, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EV 322540235 US addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Marsha A. Townsend Marsha A. Townsend
(Name of person mailing paper) (Signature)

Enclosed are:

1. X Transmittal Form (two copies required)

2. The papers required for filing date under CFR § 1.53(b):
   a. 111 Pages of specification (including claims and abstract);
   b. 2 Sheets of drawings.
      X formal _ informal

3. Declaration or oath

   a. X New original

   b. _ Copy from a prior application (37 CFR 1.63(d))
      (for continuation/divisional with Item 12 completed)

   _ Incorporation By Reference (to be used if Item 3b is checked)

   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

   i. _ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)

4. _ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

5. _ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

IPR2024-001429
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ACCOMPANYING APPLICATION PARTS

6. X An assignment of the invention to SILICON IMAGE, INC. is attached (including Form PTO-1595).

7. __ Power of Attorney

8. X An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and 6 references.

9. __ Preliminary Amendment.

10. X Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

11. X Other - Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i).

12.. FOREIGN PRIORITY
[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

13. FEE CALCULATION

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($750)
Total Claims	109 – 20	*89	x $18.00	1602.00
Independent Claims	7 – 3	*4	x $84.00	336.00
__ Multiple dependent claim(s), if any			$280.00	0

*If less than zero, enter "0".

Filing Fee Calculation $2,688.00

50% Filing Fee Reduction (if applicable) . . . . . $

14. Small Entity Status
a. __ A small entity statement is enclosed.
b. __ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. __ is no longer claimed.

15. Other Fees
X Recording Assignment [$40.00] $40.00
__ Other fees
Specify _____ .....$

Total Fees $2,728.00

16. Payment of Fees
X Checks in the amount of $2,688.00 (for application fee) and $40.00 (for recordation of assignment) are enclosed.
__ Charge Account No. 50-1697 in the amount of $.
A duplicate of this transmittal is attached.

17. All correspondence regarding this application should be forwarded to the undersigned attorney:

Alfred A. Equitz
GIRARD & EQUITZ LLP
400 Montgomery Street, Suite 1110
San Francisco, CA 94104
Telephone: 415/433-2250
Facsimile: 415/433-2255

18. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 50-1697. **A duplicate of this transmittal is attached**.

GIRARD & EQUITZ LLP

June 12, 2003
(Date)

By: Alfred A. Equitz
Alfred A. Equitz
Registration No. 30,922
Attorney(s) or Agent(s) of Record

Attorney Docket No. SII-3000 [SIMG0158]

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METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

TECHNICAL FIELD OF THE INVENTION

The invention pertains to methods and systems for transmitting encoded data over a serial link and recovering cells of decoded data from the transmitted data, where each cell includes control bits (having multiple levels of communication protocol functionality) and application data, and to transmitters and receivers for use in such systems. Various embodiments of the invention are useful to implement simplex communication over individual channels (unidirectional links), duplex communication over pairs of coordinated simplex channels (bidirectional links), and routed communication over hierarchical sets of interconnected bidirectional links (networks).

BACKGROUND OF THE INVENTION

Communication protocols are often described in terms of a stack with well-defined interfaces between the layers. For example, the OSI reference model (and the TCP/IP architecture) defines seven protocol layers: application, presentation, session, transport, network, link, and physical. A system having the OSI seven-layer architecture (or the TCP/IP architecture) typically includes application layer circuitry, presentation layer circuitry, session layer circuitry, transport layer circuitry, network layer circuitry, link layer circuitry, and physical layer circuitry.

Line coding techniques are often employed in serial, digital transmission (at the physical layer) to transform the frequency spectrum of the transmitted data stream to adapt to channel characteristics and facilitate clock/data recovery by receiver systems. This is typically accomplished using a block code which encodes a number of user data bits as a larger number of bits, according to some pre-determined table or function. The added bits of overhead typically ensure a high transition density to facilitate clock/data recovery, and accomplish DC balancing to maintain running disparity near zero, which enables the use of AC-coupling. Since the code space is larger than the data space, a modest error detection capability is also afforded.

Various serial links for transmitting data and clock signals over various media (including but not limited to fiber optics and conductors) are well known. One conventional serial link, used primarily for high-speed transmission of video data from

a host processor (e.g., a personal computer) to a monitor, is known as a transition minimized differential signaling interface ("TMDS" link). The characteristics of a TMDS link include the following:

1. video data are encoded and then transmitted as encoded words (each 8-bit word of digital video data is converted to an encoded 10-bit word before transmission);

a. the encoding determines a set of "in-band" words and a set of "out-of-band" words (the encoder can generate only "in-band" words in response to video data, although it can generate "out-of-band" words in response to control or sync signals. Each in-band word is an encoded word resulting from encoding of one input video data word. All words transmitted over the link that are not in-band words are "out-of-band" words);

b. the encoding of video data is performed such that the in-band words are transition minimized (a sequence of in-band words has a reduced or minimized number of transitions);

c. the encoding of video data is performed such that the in-band words are DC balanced (the encoding prevents each transmitted voltage waveform that is employed to transmit a sequence of in-band words from deviating by more than a predetermined threshold value from a reference potential. Specifically, the tenth bit of each "in-band" word indicates whether eight of the other nine bits thereof have been inverted during the encoding process to correct for an imbalance between running counts of ones and zeroes in the stream of previously encoded data bits);

2. the encoded video data and a video clock signal are transmitted as differential signals (the video clock and encoded video data are transmitted as differential signals over conductor pairs);

3. three conductor pairs are employed to transmit the encoded video, and a fourth conductor pair is employed to transmit the video clock signal; and

4. signal transmission occurs in one direction, from a transmitter (typically associated with a desktop or portable computer, or other host) to a receiver (typically an element of a monitor or other display device).

A use of the TMDS serial link is the "Digital Visual Interface" interface ("DVI" link) adopted by the Digital Display Working Group. A DVI link can be implemented to include two TMDS links (which share a common conductor pair for transmitting a

video clock signal) or one TMDS link, as well as additional control lines between the transmitter and receiver.

A typical DVI link includes a transmitter, a receiver, and a cable between the transmitter and receiver. The transmitter includes three encoder/serializer circuits, and the receiver includes three decoder circuits. The cable includes a conductor pair (Channel 0) for transmitting a stream of serialized data from a first encoder/serializer to a first decoder, a conductor pair (Channel 1) for transmitting another stream of serialized data from a second encoder/serializer to a second decoder, a conductor pair (Channel 2) for transmitting another stream of serialized data from a third encoder/serializer to a third decoder, and a conductor pair (Channel C) for transmitting a video clock from the transmitter to the receiver. The cable also include wires for a Display Data Channel ("DDC") channel (which can be used for bidirectional I2C communication between the transmitter and receiver), a Hot Plug Detect (HPD) line (on which a monitor associated with the receiver transmits a signal that enables a processor associated with the transmitter to identify the monitor's presence), "Analog" lines for analog video transmission from the transmitter to the receiver, and "Power" lines for provision of power from the transmitter to the receiver.

In the transmitter, one encoder/serializer encodes data to be transmitted over Channel 0 (and serializes the encoded bits), another encoder/serializer encodes data to be transmitted over Channel 1 (and serializes the encoded bits), and a third encoder/serializer encodes data to be transmitted over Channel 2 (and serializes the encoded bits). Each encoder/serializer responds to a control signal (an active high binary control signal referred to as a "data enable" or "DE" signal) by selectively encoding either digital video words (in response to DE having a high value) or a control or synchronization signal pair (in response to DE having a low value). Each encoder/serializer receives a different pair of control or synchronization signals: one receives horizontal and vertical synchronization signals (HSYNC and VSYNC); another receives control bits CTL0 and CTL1; and a third receives control bits CTL2 and CTL3. Thus, each encoder/serializer generates in-band words indicative of video data (in response to DE having a high value), the first encoder/serializer generates out-of-band words indicative of the values of HSYNC and VSYNC (in response to DE having a low value), the second encoder/serializer generates out-of-band words indicative of the values of CTL0 and CTL1 (in response to DE having a low value), and the third encoder/serializer generates out-of-band words indicative of the values of

CTL2 and CTL3 (in response to DE having a low value). In response to DE having a low value, each of the second and third encoder/serializers generates one of four specific out-of-band words indicative of the values 00, 01, 10, or 11, respectively, of control bits CTL0 and CTL1 (or CTL2 and CTL3).

Another serial link is the "High Definition Multimedia Interface" interface ("HDMI" link) developed by Silicon Image, Inc., Matsushita Electric, Royal Philips Electronics, Sony Corporation, Thomson Multimedia, Toshiba Corporation, and Hitachi. It has been proposed to transmit encrypted video and audio data over an HDMI link.

Another serial link (sometimes referred to as a "SATA" link) complies with the standard known as Serial ATA, Revision 1.0, adopted on August 29, 2001, by the Serial ATA Working Group, for communication between a host and storage device. A host can be coupled to each of one or more storage devices, with a SATA link between the host and each storage device.

Other serial links differ from TMDS links by encoding data as N-bit code words that are not 10-bit TMDS code words, or by transmitting encoded video over more than three or less than three conductor pairs.

The term "transmitter" is used herein in a broad sense to denote any device capable of encoding data and transmitting the encoded data over a serial link (and optionally also performing additional functions, which can include encrypting the data to be transmitted and other operations related to encoding, transmission, or encryption of the data). The term "receiver" is used herein in a broad sense to denote any device capable of receiving and decoding data that has been transmitted over a serial link (and optionally also performing additional functions, which can include decrypting the received data and other operations related to decoding, reception, or decryption of the received data). For example, the term transmitter can denote a transceiver that performs the functions of a receiver as well as the functions of a transmitter. For another example, in a system including two transceivers which communicate via a serial link, each transceiver can be both a receiver and a transmitter.

Some serial links encode input video data (and other data) to be transmitted into encoded words comprising more bits than the incoming data using a coding algorithm other than the specific algorithm used in a TMDS link, and transmit the encoded video data as in-band characters and the other encoded data as out-of-band characters. The characters need not be classified as in-band or out-of-band characters based according

to whether they satisfy transition minimization and DC balance criteria. Rather, other classification criteria could be used. An example of an encoding algorithm, other than that used in a TMDS link but which is used in some serial links, is IBM 8b10b coding. The classification (between in-band and out-of-band characters) need not be based on just a high or low number of transitions. For example, the number of transitions of each of the in-band and out-of-band characters could (in some embodiments) be in a single range (e.g., a middle range defined by a minimum and a maximum number of transitions).

The data transmitted between the transmitter and receiver of a serial link can, but need not, be transmitted differentially (over a pair of conductors). Also, although a TMDS link has four differential pairs (in the single pixel version), three for video data and the other for a video clock, other serial links include a different number of conductors or conductor pairs.

Typically, the primary data transmitted by a TMDS link are video data. What is often significant about this is that the video data are not continuous, and instead have blanking intervals. These blanking intervals provide an opportunity for auxiliary data to be transported, and they represent unused bandwidth. However, many serial links do not transmit data having blanking intervals. For example, audio serial links would typically transmit continuous data.

The term "stream" of data, as used herein, denotes that all the data are of the same type and are transmitted with the same clock frequency. The term "channel," as used herein, refers to that portion of a serial link that is employed to transmit data serially (e.g., a particular conductor or conductor pair between a transmitter and receiver over which the data are transmitted, and specific circuitry within the transmitter and/or receiver used for transmitting and/or recovery of the data), where "data" is used in a broad sense to denote any content (e.g., application data, a clock, control information, or other content), and to the technique employed to transmit the data over the link.

SUMMARY OF THE INVENTION

In a class of embodiments of the invention, application data and control bits are encoded in accordance with a line code to generate sequences of code words that, when decoded, are indicative (at a "link" level of communication protocol functionality) of cells of the application data and control bits. The line code provides packet-based (cell-

based) communication with multiple logical communication paths (virtual channels). The virtual channels include a virtual channel (a "control" channel) for the control bits (or a control channel for each of two or more subsets of the control bits in each cell) and at least one virtual channel (a "data" channel) for the application data (e.g., a data channel for each of two or more blocks of application data in each cell). Each block of application data in a cell can have a different priority level (indicated by one of the control bits) or can belong to a different virtual channel (specified by one of the control bits). At least some of the control bits have at least one level of communication protocol functionality higher than link level functionality (e.g., are used by network layer circuitry and/or application layer circuitry).

In accordance with preferred embodiments of the invention, M-bit input words comprising application data bits and control bits are encoded using a block code to generate N-bit code words, where $M < N$. The code words are transmitted in a predetermined sequence, and the transmitted code words can be recognized and decoded by physical layer circuitry in a receiver to generate M-bit decoded words. At a "link" level of communication protocol functionality (i.e., in "link layer" circuitry), a sequence of a predetermined number of the M-bit decoded words is indicative of a cell of the application data and control bits. Each cell has a predetermined structure, so that the position of a bit within the cell determines whether the bit is an application data bit or a control bit and determines the type (function) of each control bit. The control bits in each cell typically have multiple levels of communication protocol functionality. Link layer circuitry in the receiver recognizes the cells in response to the M-bit decoded words (including by determining which of the bits of each cell are data bits and which are control bits), performs link level functions in response to appropriate ones of the control bits, and asserts the decoded application data bits and appropriate ones of the decoded control bits to higher-level circuitry (circuitry that operates at at least one level of communication protocol functionality higher than the link level). The decoded control bits are used by the higher-level circuitry (which can be network layer circuitry and/or application layer circuitry, for example) to implement communication protocol functions at least one level higher than the link level.

In typical embodiments of the inventive system, the line code employed to transmit encoded data over a serial link specifies not only a block code (for encoding cells) but also special characters that are typically transmitted between cells. Preferably, the code words employed to encode cells and the special characters are

chosen such that no special character can unintentionally occur in a sequence of code words indicative of a cell (i.e., no special character matches any of the code words, and no sequence of bits from any possible sequence of consecutively transmitted code words matches any of the special characters). In such preferred embodiments, a special character can be transmitted at any time (including at a time that interrupts transmission of a cell).

Typically, each cell includes a small number of blocks (e.g., one or two blocks) of application data, a priority-level-indicating control bit (sometimes referred to herein as an "out-of-band" or "OOB" bit) for each application data block, and other control bits (including cyclic redundancy check bits). The OOB bit for each application data block is indicative of a priority level for the block's application data, and/or specifies a virtual channel to which the block belongs. For example, the OOB can occur as the Nth bit of a cell, and can indicate whether a first block of application data bits are "in-band" application data (e.g., video or audio data, or data read from a memory or to be written to a memory) or "out-of-band" application data (e.g., application control bits, which could be sync words, for example). A single OOB bit for one application data block can be indicative of a priority level for the block's application data, and also specify a virtual channel to which the block belongs and also otherwise identify the block's application data.

In a typical embodiment, each cell consists of a base portion (e.g., a base portion consisting of 144 bits, including 128 application data bits and 16 control bits) and an optional extension. The extension can be an L-bit address for the base portion. A receiver recovers the cell from K received ten-bit code words. In some embodiments, K = 16 (if the cell has no extension), and each code word is a 10-bit encoded version of a nine-bit input word consisting of eight application data bits concatenated with a control bit. The receiver decodes each sequence of sixteen transmitted code words to recover a sequence of sixteen, 9-bit input words. The receiver identifies these decoded bits as a 144-bit cell (having no extension) if the "J"th bit in the decoded bit sequence indicates that there is no cell extension, determines which bits of each decoded bit sequence are application data bits and which are control bits, and determines the type (and thus the function) of each such control bit by its position in the sequence. In a class of embodiments, the receiver decodes a sequence of K transmitted 10-bit code words to recover a sequence of K nine-bit decoded input words, handles every 9th bit of the resulting stream of 9-bit decoded words as a control

bit, and handles the other 8-bit quantities of data of the stream of 9-bit words as application data.

In other embodiments, the input words to be encoded include other patterns of application data and control bits, e.g., to improve the efficiency with which the code words can be generated and transmitted by the transmitter and/or processed by the receiver. For example, CRC bits for a cell are determined only once the CRC-bit generating circuitry has seen all the data of the cell, and thus CRC bits are typically the last bits to be generated. Since the CRC bits are control bits, the embodiment described in the previous paragraph would require that transmission of each cell be delayed while the encoding circuitry waits for the CRC bits to be generated, so that all control bits for the cell (including the CRC bits) can be uniformly distributed across the 9-bit input words (one control bit per input word). In applications in which there is a sufficient degree of transmission latency, the control bits of each cell can be distributed among the input words in any convenient pattern for timing. For example, in one embodiment in which a cell consists of 16 control bits and 128 application data bits, the first 9-bit input word of the cell consists of two control bits concatenated with seven application data bits, the next six input words of the cell consist of application data bits, the next input word of the cell consists of two control bits concatenated with seven application data bits, the next six input words of the cell consist of application data bits, the next-to-last input word of the cell consists of six application data bits concatenated with three CRC bits, and the last input word of the cell consists of nine CRC bits. For two other examples, the pattern of control and application data bits of a 144-bit cell can be a repeating pattern of 4 control bits followed by 32 application data bits, or it can be 4 control bits followed by 128 application data bits followed by 12 CRC bits. Many other patterns are possible.

The application data of a cell can be video data, audio data, application control bits, memory data (read from or to be written to a memory), or application data of any other type. The control bits included in a cell (and any transmitted special characters) can be used at any protocol level (layer) of communication protocol functionality (e.g., any layer of the Open Systems Interconnection ("OSI") seven-layer reference model). For example, in a system having the OSI seven-layer architecture (or the TCP/IP architecture), the control bits (and any transmitted special characters) can be used by application layer circuitry, presentation layer circuitry, session layer circuitry, transport

layer circuitry, network layer circuitry, link layer circuitry, and/or physical layer circuitry.

An example of a control bit (of the inventive cell) that is used by link layer and network layer circuitry (of a system having the OSI seven-layer architecture) is a bit (sometimes referred to herein as an "XTND" bit) that indicates whether the cell is an extended cell (a cell having an extension of predetermined length). For example, the XTND bit can be the first bit of a cell, and can indicate whether the cell is a 144-bit non-extended cell or a (K*9)-bit extended cell, where K is an integer greater than 16. For example, XTND = 1 can indicate that a 9-bit extension follows the first 144 bits of each cell (so that the 145th through 153rd bits after the XTND bit are an extension (e.g., an address for use by "network" layer circuitry) that is part of the same cell as the 2nd through 144th bits after the XTND bit, and XTND = 0 can indicate that no extensions are enabled so that each set of consecutive 144 decoded bits belong to a different cell.

Another example of a control bit (of the inventive cell) that is used by network layer circuitry (of a system having the OSI seven-layer architecture) is an address bit (e.g., a bit of an address extension of an extended cell).

An example of a control bit (of the inventive cell) for use by application layer circuitry of a system having the OSI seven-layer architecture is a "Valid" bit that indicates whether or not a specific block of application data is valid. Use of a Valid bit allows cells to contain multiple blocks of application data, not all of which are utilized.

An end-to-end flow control bit (sometimes referred to herein as a "FLOW" bit) of the inventive cell is another example of a control bit used by application layer circuitry of a system that has the OSI seven-layer architecture and includes two transceivers (one referred to as a transmitter and the other as a receiver) connected by a serial link. The FLOW bit is set by the receiver, in a cell transmitted by the receiver to the transmitter, to indicate whether the transmitter should send code words indicative of cells to the receiver. For example, FLOW = 1 indicates that the transmitter should enter an "ON" state in which the transmitter sends code words indicative of cells to the receiver, and FLOW = 0 indicates that the transmitter should enter an "OFF" state in which the transmitter does not send such code words to the receiver. A FLOW bit can apply to one priority level of application data (e.g., a cell can include two FLOW bits, one for each of two blocks of application data, each block having a different priority, and the transmitter can respond to each FLOW bit by sending or ceasing to send application data of the relevant priority level) or to more than one priority level of

application data. If a cell also includes a "Valid" bit (mentioned in the previous paragraph), it is permissible to send empty cells in the OFF state. If a cell includes a Valid bit for each of multiple blocks of application data, it is permissible to send (in each cell) at least one empty block and at least one full block in the OFF state. A FLOW bit can be used in any of several contexts, including to provide end-to-end flow control between applications on different devices that communicate over two or more serial link hops (e.g., devices that communicate via a repeater, over a first serial link between one of the devices and the receiver, and over a second serial link between the receiver and the other device), and to provide end-to-end flow control between directly connected transmitters and receivers that require rate matching due to clock differences or application-level service rates.

The above-mentioned OOB (out-of-band) bit is another example of a control bit (of the inventive cell) that is used by application layer circuitry of a system having the OSI seven-layer architecture. The OOB bit for an application data block can indicate a priority level for the block's application data, or can specify a virtual channel to which the block belongs. OOB bits can be used to create virtual channels, possibly having different priorities.

An example of control bits (of the inventive cell) providing transport layer functionality in a system having the OSI seven-layer architecture are sequence number bits (an ordered set of bits indicative of a sequence number of the current cell being transmitted or of particular cells received from a remote node).

CRC (cyclic redundancy check) bits (or other error control bits) in the inventive cell are an example of control bits used by link layer circuitry of a system having the OSI seven-layer architecture to perform error detection and/or error correction on the decoded bits that determine each cell. In the transmitter, the CRC bits can be generated for the entire amount of data (application data and control bits) to be transmitted in a cell (before the application data and control bits undergo spectral encoding), the application data and control bits of the cell (including the CRC bits) then arranged in the proper sequence, and the properly sequenced application data and control bits of the cell then encoded. It is typical to generate twelve CRC bits for each 144-bit cell. Although a shorter length CRC could be used for a cell of this size, the effective error detection probability would be reduced if such a shorter length CRC were used. A longer length CRC could alternatively be used.

Control bits can be inserted into cells so as to enhance the cells' spectral properties. For example, the possible values for a multi-bit field of control bits can be restricted so that transitions (0 to 1 or 1 to 0) within the field are guaranteed. For example, a 2-bit sequence number can be restricted to take on only three values, where 00 and 11 indicate the same value. Thus, 01 and 10 include a transition, and either 00 or 11 is used depending on the preceding or following bit so that a transition is guaranteed.

In accordance with the invention, multiple levels of communication protocol functionality can be efficiently incorporated within a line code, thereby increasing the line code's utility. Physical layer and link layer circuitry transmit and receive data encoded in accordance with the line code. In preferred embodiments, the invention eases the design and reduces the complexity of protocols layered above the physical layer and link layer. In typical embodiments, features of the line code include all or some of the following: 1) guaranteed transition bandwidth, 2) DC balance, 3) simplex link flow control, 4) framing, 5) simplex link error detection, 6) simplex link error correction, 7) duplex link flow control, 8) network addressing, 9) sequenced, reliable connections, 10) end-to-end flow control, and 11) out-of-band signaling. These features can all be incorporated with minimal overhead, e.g., no worse than the 20% overhead of the commonly used 8B/10B coding scheme.

In a class of embodiments, the invention is a communication system including two endpoints (e.g., a transmitter and receiver or two transceivers) and a serial link (having at least one channel) between the endpoints, wherein at least one of the endpoints is configured to generate encoded data in accordance with a line code and transmit the code words over each of one or more channels of the link to the other endpoint, where the line code specifies a block code for encoding cells (including application data and control bits) and typically also specifies special characters that are distinguishable from bit sequences of encoded cells. Another aspect of the invention is an endpoint device (i.e., a transmitter, receiver, or transceiver) configured to generate encoded data in accordance with a line code (where the line code specifies a block code for encoding cells of application data and control bits, and typically also specifies special characters that are distinguishable from bits of encoded cells) and to transmit the encoded data over a serial link, and/or to receive and process (in accordance with the invention) encoded data that have been generated in accordance with such a line code and propagated over a serial link.

Other aspects of the invention are methods for generating encoded data in accordance with a line code (where the line code specifies a block code for encoding cells of application data and control bits, and typically also specifies special characters that are distinguishable from bits of encoded cells) and methods for performing functions of multiple layers of a communication protocol in response to such encoded data.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an embodiment of the inventive system.

Fig. 2 is a diagram of a cell of data (cell 80), an ordered set of 9-bit words (indicative of the cell) generated in accordance with the invention, and an ordered set (81) of 10-bit code words (indicative of the cell) generated in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides mechanisms for collapsing functionality provided by at least one higher layer (e.g., the link layer) of a communication protocol into the physical layer, and/or for collapsing functionality provided by at least one layer above the link layer (e.g., the application, transport, and network layers) into the link layer. For example, special characters (e.g., N-bit code words known as "link training" and "state exchange" characters, where N = 10 in preferred embodiments) are recognized by physical layer circuitry and used in accordance with the invention by the physical layer circuitry not only for "physical layer" framing to determine the boundaries of N-bit code words to be decoded to produce M-bit decoded words (where $M < N$) to be utilized by link layer circuitry, but also for "link layer" framing to allow link layer circuitry to determine the boundaries of blocks of application data (and blocks of control bits) within cells of the M-bit decoded words, where the blocks of application data (or control bits) are to be utilized by network layer or higher layer circuitry. For another example, special characters (e.g., N-bit code words known as "idle" characters, where N = 10 in preferred embodiments) which can be recognized by physical layer circuitry are used in accordance with the invention by link layer circuitry for flow control.

The functionality collapsing mechanisms mentioned in the previous paragraph yield several benefits including the following: physical and/or link layer circuitry that

embodies the invention is imbued with much greater functionality than conventional circuitry of the corresponding type; higher level protocols designed on top of layers that embody the invention can be made much simpler (e.g., transport layer protocols would not require support for handling the re-ordering of cells since link re-training after detection of an uncorrectable error in a transmitted cell can be accomplished in accordance with the invention without the need to re-order cells in a manner to be described herein); and higher level protocol implementations on top of layers that embody the invention can be much more efficient (e.g., error control coding and large packet buffers are not needed to support re-transmission in accordance with the invention in a manner to be described herein, after detection of an uncorrectable error in a transmitted cell).

Fig. 1 is a block diagram of a typical system that embodies the invention. The Fig. 1 system includes transceivers 10 and 20, and a serial link between them. The serial link includes primary channel 51 and back channel 52 (and optionally also other channels, not shown). Transceiver 10 will be referred to as a transmitter since it transmits application data to transceiver 20 over the serial link. Transceiver 20 will be referred to as a receiver since it does not transmit application data to transceiver 10 over the serial link, although it does transmit other data to transceiver 10. The Fig. 1 system implements a bidirectional communication path in which primary channel 51 carries application traffic, and back channel 52 (which typically is smaller than channel 51 in the sense that it carries a smaller volume of data than channel 51) carries link management traffic that is not exposed to the application. Primary channel 51 carries code words indicative of control data (e.g., OOB bits) and application data, and typically also special characters (e.g., idle characters used for simplex or duplex link flow control, and link training characters) that are not indicative of application data. Back channel 52 carries information related to error control, end-to-end flow control, and data sequencing. For example, back channel 52 carries code words indicative of control data related to error control, end-to-end flow control, and data sequencing, and typically also special characters (e.g., link training characters). Typically, the same physical layer requirements are applied across both channels 51 and 52. Preferably, a block code is used, and the length of the block code is chosen to ensure that total overhead is comparable to other common line codes while simultaneously minimizing design and implementation complexity.

Some but not all elements of transmitter 10 are shown in Fig. 1. The physical layer and link layer circuitry of transmitter 10 includes packetizing circuit 31, encoding and transmission circuit 32, receiving and decoding circuit 33, error detection and correction circuit 34, and de-packetizing circuit 35, connected as shown. Transmitter 10 also includes higher layer circuitry 30, which typically includes network layer circuitry, transport layer circuitry, and application layer circuitry. In operation, higher layer circuitry 30 provides application data and control data to packetizing circuit 31. For example, the control data provided to circuit 31 by circuitry 30 can determine the XTND, FLOW, OOB1, and OOB2 bits to be described with reference to Fig. 2. In response, packetizing circuit 31 generates (and asserts to circuit 32) sequences of input words (e.g., the 9-bit input words of Fig. 2, each of which comprises eight application data bits and one control bit) that are indicative of cells (e.g., a sequence of code words having the form shown in Fig. 2, with each cell including two 64-bit application data blocks and 16 control bits). In typical implementations, packetizing circuit 31 generates CRC bits for each cell and includes the CRC bits in the input word sequences asserted to circuit 32. Packetizing circuit 31 performs any necessary serialization of the application data and control data from circuitry 30, and asserts the input word sequences as serial data to circuit 32.

Circuit 32 encodes the input words from circuit 31 (e.g., to generate one of the 10-bit code words shown in Fig. 2 in response to each 9-bit input word), and transmits the code words serially over channel 51 to receiver 20. Circuit 32 can also transmit (over channel 51) one or more special characters. In some implementations, circuit 32 transmits each special character before or after a cell of code words (i.e., before or after a sequence of code words indicative of a cell), but does not transmit any special character during a cell. However, in preferred implementations, the set of code words employed to encode cells (for transmission over channel 51) and the special characters are chosen such that no special character can unintentionally occur in a sequence of code words indicative of a cell (i.e., no special character matches any of the code words, and no sequence of bits from any possible sequence of consecutively transmitted code words matches any of the special characters). In such preferred implementations, circuit 32 can transmit any special character at any time (including by interrupting transmission of a cell to transmit the special character), and the circuitry (e.g., circuit 43 of receiver 20) employed for receiving and decoding code words transmitted by circuit 32 can be configured (e.g., can include logic configured) to

recognize each transmitted special character, regardless of whether transmission of the special character has or has not interrupted transmission of a cell.

An example of special character transmission by an implementation of circuit 32 is the transmission of special "idle" characters at appropriate times between cells (e.g., for duplex link flow control, in a manner to be described below). For another example, in response to control signals from error detection and correction circuit 34, an implementation of circuit 32 asserts special "link training" characters and special "state exchange" characters with embedded sequence numbers during a link re-training operation (to be described below) initiated by a control signal from circuit 34.

Receiving and decoding circuit 33 decodes code words received sequentially on back channel 52 to generate a stream of decoded words (e.g., 9-bit words as shown in Fig. 2, each comprising eight application data bits and one control bit). In various implementations of the Fig. 1 system (and variations thereon) which implement different line codes, the decoded words generated by the receiver are M-bit words (where M can be any positive integer, although M is odd in preferred embodiments), and the decoded words of a cell can include any predetermined pattern of application data and control bits (e.g., each cell can include a repeating pattern of four control bits followed by thirty-two application data bits, or can consist of four control bits followed by 128 application data bits followed by twelve CRC bits, or any of many other patterns of application data and control bits).

For another example, each cell can consist of eight, 27-bit subcells, each subcell having the following format: 24 bits of application data, followed by one OOB bit (indicative of a priority level for the application data and/or specifying a virtual channel to which the application data belongs), followed by two CRC bits. Each cell includes 16 CRC bits. For another example, each cell can consist of eight, 36-bit subcells, each subcell having the following format: 32 bits of application data, followed by one OOB bit (indicative of a priority level for the application data and/or specifying a virtual channel to which the application data belongs), followed by another control bit (of any predetermined type), followed by two CRC bits. Each cell also includes 16 CRC bits. When encoded using a 9B/10B block code, these cells have the same overhead as application data encoded using a conventional 8B/10B block code. These cells can be used in a wormhole routing system, in which they are referred to as flits (flow control units), and could be used in a storage network application. In a typical wormhole routing system, credit-based flow control is used, and each flit must be delivered in

order over the next serial link hop of a predetermined route. The OOB bit (sometimes referred to as a type field) can distinguish between multiple virtual channels and between header data and other data (in wormhole routing, a packet consists of a train of flits, the first of which contains routing information, that lock down a route through a communication fabric).

For another example, each cell can consist of N, 36-bit subcells (where N is a small positive integer), each subcell having the following format: 32 bits of application data, followed by two OOB bits (indicative of a priority level for the application data and/or specifying a virtual channel to which the application data belongs), followed by two credit bits. These cells include no CRC (or error control) bit, and could be used in a wormhole routing system. When encoded using a 9B/10B block code, these cells also have the same overhead as application data encoded using a conventional 8B/10B block code. The OOB bits could indicate a virtual channel for the application data or could indicate that the application data are control channel data (e.g., for wormhole circuit set-up or exchange of information between communicating nodes in a network). The credit bits would be used to exchange flow control credits between communicating endpoints. Typically, there would be two virtual channels in this scheme.

Another application domain that would utilize larger cells would be to support a network of packet switching. An exemplary cell useful in such application domain cell consists of N, 54-bit subcells (where N is a small positive integer), each subcell having the following format: 48 bits of application data, followed by two CRC bits, followed by one src address bit, followed by one dst address bit, followed by one sequence number bit, followed by one OOB bit (indicative of a priority level for the application data and/or specifying a virtual channel to which the application data belongs). When encoded using a 9B/10B block code, these cells also have the same overhead as application data encoded using a conventional 8B/10B block code. An advantage of use of such cells in the noted application domain is to enable packet switching for relatively small networks, all embedded within the line code.

With reference again to Fig. 1, a typical implementation of error detection and correction circuit 34 identifies CRC bits in the stream of decoded words, uses the CRC bits to perform error detection and correction on a cell of the decoded words (e.g., on a sequence of sixteen 9-bit words having the Fig. 2 format), and asserts the corrected decoded words to de-packetizing circuit 35 (except in the event that circuit 34 identifies an uncorrectable error in a cell).

De-packetizing circuit 35 then determines which of the bits of the corrected, decoded words are application data bits and which are control data bits, and asserts the application data, and appropriate ones of the control bits (separately from the application data) to higher layer circuitry 30 for processing. Circuit 35 performs any necessary deserialization of the data it receives from circuit 34 (e.g., to assert application data and control bits in parallel to circuitry 30).

Some but not all elements of receiver 20 are shown in Fig. 1. The physical layer and link layer circuitry of receiver 20 includes packetizing circuit 41, encoding and transmission circuit 42, receiving and decoding circuit 43, error detection and correction circuit 44, and de-packetizing circuit 45, connected as shown. Receiver 20 also includes higher layer circuitry 40, which typically includes network layer circuitry, transport layer circuitry, and application layer circuitry. In operation, higher layer circuitry 40 can provide application data and control data to packetizing circuit 41. For example, circuitry 40 can provide (to circuit 41) control data (generated by application layer circuitry) that determine the FLOW bits to be described with reference to Fig. 2. In response, packetizing circuit 41 generates (and asserts to circuit 42) sequences of input words (e.g., the 9-bit input words of Fig. 2, each of which comprises eight application data bits and one control bit) that are indicative of cells (e.g., a sequence of code words having the form shown in Fig. 2, with each cell including two 64-bit application data blocks, and 16 control bits). In typical implementations, packetizing circuit 41 generates CRC bits for each cell and includes the CRC bits in the input word sequences asserted to circuit 42. Packetizing circuit 41 performs any necessary serialization of the application data and control data from circuitry 40, and asserts the input word sequences as serial data to circuit 42.

Circuit 42 encodes the input words from circuit 41 (e.g., to generate one of the 10-bit code words shown in Fig. 2 in response to each 9-bit input word), and transmits the code words serially over channel 52 to transmitter 10. Circuit 42 can also transmit one or more special characters over channel 52. In some implementations, circuit 42 transmits each special character before or after a cell of code words (i.e., before or after a sequence of code words indicative of a cell), but does not transmit any special character during a cell. However, in preferred implementations, the set of code words employed to encode cells (for transmission over channel 52) and the special characters are chosen such that no special character can unintentionally occur in a sequence of code words indicative of a cell (i.e., no special character matches any of the code

words, and no sequence of bits from any possible sequence of consecutively transmitted code words matches any of the special characters). In such preferred implementations, circuit 42 can transmit any special character at any time (including by interrupting transmission of a cell to transmit the special character), and the circuitry (e.g., circuit 33 of transmitter 10) employed for receiving and decoding code words transmitted by circuit 42 can be configured (e.g., can include logic configured) to recognize each transmitted special character, regardless of whether transmission of the special character has or has not interrupted transmission of a cell.

An example of special character transmission by an implementation of circuit 42 is the transmission of special "idle" characters at appropriate times between cells (in a manner to be described below). For another example, in response to control signals from error detection and correction circuit 44, an implementation of circuit 42 asserts special "link training" characters and special "state exchange" characters with embedded sequence numbers during a link re-training operation (to be described below) initiated by a control signal from circuit 44.

Receiving and decoding circuit 43 (of receiver 40) decodes code words received sequentially on channel 51 to generate a stream of decoded words (e.g., 9-bit words as shown in Fig. 2, each comprising eight application data bits and one control bit). In a typical implementation, error detection and correction circuit 44 identifies CRC bits in the stream of decoded words, uses the CRC bits to perform error detection and correction on a cell of the decoded words (e.g., on a sequence of sixteen 9-bit words having the Fig. 2 format), and asserts the corrected decoded words to de-packetizing circuit 45 (except in the event that circuit 44 identifies an uncorrectable error in a cell). De-packetizing circuit 45 then determines which of the bits of the corrected, decoded words are application data bits and which are control data bits, and asserts the application data, and appropriate ones of the control bits (separately from the application data) to higher layer circuitry 40 for processing. Circuit 45 performs any necessary deserialization of the data it receives from circuit 44 (e.g., to assert application data and control bits in parallel to circuitry 40).

In a class of preferred embodiments, code words indicative of cells (of application data and control data) having the format shown in Fig. 2 are transmitted over a serial link. The following steps are performed to accomplish this.

First, logical blocks of application data are defined (e.g. 64-bit blocks as shown in Fig. 2, or 32-bit blocks). This can be accomplished, for example, by application

layer circuitry within circuitry 30 (or circuitry 40) of Fig. 1. For each application data block, an out-of-band ("OOB") bit is provided to indicate the priority level of the block, or to specify a virtual channel to which the block belongs. For example, the "OOB1" bit in Fig. 2 can indicate whether the block labeled "Application Data Word 1" consists of low priority data (e.g., application data) or high priority data (e.g., control data), and the "OOB2" bit can similarly indicate whether the block labeled "Application Data Word 2" consists of low priority data (e.g., application data) or high priority data (e.g., control data.

The application data blocks (sometimes referred to as words) are grouped into cells (e.g., by packetizing circuit 31 or 41 of Fig. 1). To minimize latency associated with re-transmission (e.g., after an uncorrectable error during transmission), the number of application data words per cell should be minimized (e.g., there are only two words per cell). A flow control bit (identified as "FLOW" in Fig. 2) is included in each cell. The flow control bits and application data blocks are the only data visible to the application. In each cell, at least one additional control bit (e.g., the XTND control bit of Fig. 2) is included, and additional bits (e.g., an address extension) can be included to provide optional functionality, such as network addressing. Also, error control bits (e.g., parity bits, or the CRC bits of Fig. 2) are generated for (and included in) each cell to enable error detection and/or correction. Fig. 2 shows an example of such a cell, consisting of 144 bits and not including an extension.

The bits of each cell are grouped into input words (e.g., in packetizing circuit 31 or 41 of Fig. 1). For example, the 144 bits of cell 80 of Fig. 2 are grouped into the sixteen 9-bit input words shown in Fig. 2, each comprising eight application data bits (D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, or D15) and one control bit.

Finally, the input words indicative of each cell are encoded, preferably to transform the frequency spectrum of the serial data stream so as to adapt to channel requirements. For example, each code word indicative of a 9-bit input word can be a 10-bit code word having enhanced spectral properties. Preferably a block code is used which limits the length of runs without transitions in the encoded data stream (to meet requirements) and allows the encoded data to be transmitted in DC balanced fashion to avoid baseline wander. Different codebooks (mappings between input words and code words) can be used to perform the encoding, depending on the spectral properties of the

previously encoded values (e.g., one code book can be used when the current running disparity is negative, and a different codebook used when the current running disparity is non-negative).

In the Fig. 2 example, the sixteen 9-bit input words indicative of cell 80 are encoded (e.g., by circuit 32 or 42 of Fig. 1) using a 9-Bit-to-10-Bit ("9B/10B") block code to produce the sixteen 10-bit code words (CW0-CW15) shown in Fig. 2. The code words are transmitted in an appropriate sequence over a serial link. Thus, an ordered set of 160 code word bits (identified by reference numeral 81 in Fig. 2) is indicative of the 144-bit cell identified by reference numeral 80 in Fig. 2. Cell 80 includes a control bit (denoted as "XTND" in Fig. 2) that indicates whether the cell has an extension. The value XTND = 0 indicates that cell 80 has no extension. The value XTND = 1 would indicate that the cell has an extension of predetermined length (e.g., an extension of M*9 bits, where M is a small integer). The XTND bit can be the first bit of the cell, and can indicate whether the cell is a 144-bit non-extended cell or a (N*9)-bit extended cell, where N is an integer greater than 16. For example, XTND = 1 can indicate that a 9-bit extension follows the first 144 bits of each cell (so that the 145th through 153rd bits after the XTND bit are an extension (e.g., an address for use by "network" layer circuitry) that is part of the same cell as the 2nd through 144th bits after the XTND bit.

The extension for a cell can serve any of various functions, and can include bits that indicate what functionality is enabled (by the extension) as well as bits of additional protocol fields. For example, a 9-bit extension field could be added to cell 80 of Fig. 1 (if the XTND bit is set to XTND = 1), to provide a network address or connection identifier for routing the cell. After coding, the extended cell's size would be 170 bits.

Cell 80 also includes an end-to-end flow control bit (the bit identified as "FLOW") for use by application layer circuitry (e.g., application circuitry within circuitry 30 of transmitter 10 of Fig. 1). In typical implementations of the Fig. 1 system, circuitry 40 in receiver 20 ignores the FLOW bits in cells received on channel 51 from transmitter 10, and when generating data to be transmitted (by circuit 42) in cells over channel 52, circuitry 40 sets the FLOW bit of such data to one or zero to cause transmitter 10 to respond to the cells by continuing or ceasing transmission of data over channel 51 to receiver 20. In response to reception (at transmitter 10) of a cell that has propagated over channel 52, the transmitter's de-packetizing circuit 35

identifies the FLOW bit in the cell, and asserts a signal indicative of the FLOW bit's value to circuitry 30. In response to FLOW = 1, application circuitry within circuitry 30 causes transmitter 10 to enter a data transmitting state (an "ON" state) in which transmitter 10 sends code words indicative of cells to receiver 20 over channel 51. In response to FLOW = 0, application circuitry within circuitry 30 causes transmitter 10 to enter a state (an "OFF" state) in which transmitter 10 does not send such code words to receiver 20 over channel 51. In some embodiments, transmitter 10 transmits "idle" characters (of the type discussed below) while in the OFF state. In other embodiments, transmitter 10 transmits empty cells (i.e., cells in which one or more "Valid" bits are set to indicate that the cells include no valid application data) while in the OFF state. In other embodiments, each cell includes a "Valid" bit for each of two or more blocks of application data, and a FLOW bit for each priority level (or virtual channel) of application data. For example, the "XTND" bit of Fig. 2 can function as a "Valid" bit, rather than as an extension-indicating bit as described above. In the latter embodiments, in response to one of the FLOW bits (in a cell sent by receiver 20) having a value indicating an OFF state for one priority level (or virtual channel) of application data, transmitter 10 transmits cells each having an empty block of application data of the relevant type (as indicated by a Valid bit having a first value) and at least one full block of application data of another type (each such block indicated by a Valid bit having a second value).

Cell 80 also includes twelve cyclic redundancy check (CRC) bits. Preferably, the CRC bits are generated for the entire cell (e.g., by packetizing circuit 31 or 41 of Fig. 1) before the data comprising the cell are encoded, and later applied (e.g., by circuit 44 or 34) to the entire cell after the data comprising the cell have been transmitted and decoded. After the CRC bits are generated, the control bits (including the CRC bits) and application data of the cell are asserted in the proper sequence (e.g., by packetizing circuit 31 or 41) to encoding circuitry (e.g., within circuit 32 or 42) in which the properly sequenced application data and control bits are encoded for transmission. In such preferred embodiments, because the CRC is applied to the contents of each cell before spectral encoding, burst errors will be magnified. Thus, in such embodiments, it is typical to use a relatively long length CRC (i.e., twelve CRC bits for each 144-bit cell). Although a shorter length CRC could be used for a cell (e.g., less than twelve CRC bits for each 144-bit cell), the effective error detection probability would be reduced if a shorter length CRC were used.

In different embodiments of the invention, the sizes of words, cells, blocks of CRC bits (or other error control bits), and other parameters are adjusted according to desired features and coding efficiency. For a cell having the Fig. 2 format, the above-described coding method provides 131 bits of application information (128 bits of application data, two OOB bits, and one FLOW bit) with 29 bits of protocol overhead per cell, which gives an 82% coding efficiency. The commonly used conventional 8B/10B coding scheme achieves only 80% efficiency for the physical layer alone.

In many contemplated embodiments, code words indicative of cells (of application data and control data) having format other than that shown in Fig. 2 are transmitted. For example, in some embodiments the XTND bit discussed with reference to Fig. 2 is replaced by a second FLOW bit so that there is a FLOW bit for each application data block. In other exemplary embodiments, the FLOW bit of Fig. 2 is removed and replaced by a "Valid" bit that indicates whether or not the second 64-bit block of application data in the cell contains valid data (in such embodiments the first 64-bit application data block is always valid; otherwise, the transmitter would transmit "idle" characters, of the type mentioned above and discussed further below, rather than code words indicative of cells). The line code employed in some embodiments of the invention has a coding efficiency of less than 80%, although many other embodiments have a coding efficiency greater than 80%.

We next describe examples of special characters that can be transmitted in accordance with the invention. In some implementations, the circuitry (e.g., circuit 32 or 42 of Fig. 1) employed to transmit each special character can transmit a special character before or after a cell of code words (i.e., before or after a sequence of code words indicative of a cell), but does not interrupt transmission of a cell to transmit any special character. However, in preferred implementations, the set of code words employed to encode cells for transmission in accordance with the invention is such that no special character (in a set of special characters) can occur in a sequence of code words indicative of a cell. In such preferred embodiments, the special character transmission circuitry can transmit any special character in the set at any time (including by interrupting transmission of a cell to transmit the special character), and the circuitry (e.g., circuit 33 or 43 of Fig. 1) employed for receiving and decoding transmitted code words is configured (e.g., includes logic configured) to recognize each transmitted special character, regardless of whether transmission of the special character has or has not interrupted transmission of a cell.

In preferred embodiments of the invention in which N-bit code words indicative of cells are transmitted, each special character transmitted is an N-bit word or a sequence of a small number of N-bit words (e.g., two or three N-bit words). Examples of special characters are "link training," "state exchange (or "synchronization"), and "idle" characters.

Special characters ideally include some inherent redundancy to protect against errors in transmission. For example, bit errors in a state exchange character should not should cause the system to interpret it as another valid state exchange character. Thus, the special character should be resilient to errors, or it can be transmitted repeatedly a small number of times (e.g. two or three times) to ensure proper delivery.

To establish symbol framing upon startup or after a link error during operation of typical implementations of the Fig. 1 system, transmitter 10 and receiver 20 transmit at least one special "link training" character (sometimes referred to herein as a training character "T") and optionally also at least one special "synchronization" or "state exchange" character. State exchange characters are sometimes denoted herein as "Si" characters, where the notation "Si" indicates that there are "i" different state exchange characters. For example, the "i"th state exchange character can communicate the value "i" to the endpoint that receives it, in order to exchange state information. The endpoint that receives a state exchange character "Si" interprets its value "i" in a predetermined manner. For example, the value "i" can be a sequence number which takes on the values 0,1,...,7. In some contemplated embodiments of the invention, less than ten different "Si" characters would be needed.

Preferably, no link training (or state exchange) character appears in any valid stream of code words that is indicative of a cell, and each such special character is self-identifying. Preferably, each such special character includes a preamble used for link training (e.g., to establish framing) and also a discriminant pattern that distinguishes the character from other characters. The discriminant pattern can be indicative of state information (e.g., state information useful for recovery from a link error).

In a class of implementations of the Fig. 1 system, upon startup or after a link error, a communications endpoint (e.g., transmitter 10 upon startup, or receiver 20 after a link error) enters a link training phase (or training "mode" or "state") having an initial handshake phase. In response to one or more special characters sent by one endpoint in the handshake phase, the other endpoint enters the link training phase and participates in the handshake phase. During the handshake phase (which is implemented at the

physical level), the endpoints establish symbol alignment (typically by exchanging one or more link training characters). After the handshake phase (during or after the link training phase), the endpoints exchange state information and establish cell alignment.

In typical implementations in this class, at least one state exchange character is sent (potentially with redundancy to guard against link errors) after the handshake phase. Typically, both endpoints exchange state information after the handshake phase (i.e., each endpoint sends one state exchange character, or a number of state exchange characters, to the other endpoint). Ideally, each state exchange character contains the same preamble as does each link training character sent during the handshake phase, or has some other unique property that enables link training to occur.

In some implementations, each state exchange character indicates state information regarding the endpoint that sends it. For example, one state exchange character identifies the last cell successfully received (by the endpoint that sends the state exchange character) before the link training operation, or a sequence of state exchange characters (which need not all be identical) identifies the last cell successfully received (by the endpoint that sends the state exchange character) before the link training operation. For example, each state exchange character can include a preamble (for framing) and a sequence number indicative of the last cell successfully received (by the endpoint that sends the state exchange character) before the link training operation.

In other implementations in this class, at least one state exchange character sent (potentially with redundancy to guard against link errors) after the handshake phase indicates that the first cell of normal data to be transmitted after the link training operation contains state information to be exchanged, and optionally indicates a number of cells (after such first cell) that contain additional state information. Alternatively, some portion of the first cell indicates the total number of cells that contain state information.

In other implementations in this class, no state exchange character is sent after the handshake phase. Instead, by convention, the first cell (or each of the first few cells) sent after the handshake phase contains state information to be exchanged.

In some implementations, after the handshake phase of a link training operation, at least one endpoint sends a sequence of state exchange characters, rather than a single state exchange character, whenever it sends a state exchange character. For example, a first endpoint can send a sequence of a predetermined number of Si characters (e.g., X

"Si" characters, each "Si" character including a sequence number indicative of the last cell received by the first endpoint from the second endpoint). Each such sequence can be indicative of arbitrary state information. For example, such a sequence can be indicative of the sequence number of the last cell received by the endpoint that sends the state exchange character sequence (e.g., if each state exchange character in the sequence is indicative of a binary "1" or "0" and the sequence consists of N characters, the sequence number of the cell can be an N-bit binary number determined by the N-character sequence).

Transmission of code word sequences indicative of cells (and special characters that are distinguishable from the bit sequences that can occur in such code word sequences) in accordance with the invention allows transmitters and receivers to implement multiple levels (layers) of communication protocol functionality in an improved manner. In preferred embodiments of the invention, the control bits included in a cell can be used at more than one level (layer) of communication protocol functionality. For example, in a system having the OSI seven-layer architecture (or the TCP/IP architecture), the control bits can be used by two or more of application layer circuitry, presentation layer circuitry, session layer circuitry, transport layer circuitry, network layer circuitry, link layer circuitry, and physical layer circuitry.

In a system having the OSI seven-layer (or TCP/IP) architecture, transmission in accordance with the invention of code word sequences indicative of cells, and special characters that are distinguishable from the bit sequences that can occur in such code word sequences, allows transmitters and receivers to provide improved physical layer functionality. We next describe this improved physical layer functionality.

The goal of a line code is to transform the frequency spectrum of a serial data stream so as to adapt to channel requirements, for example by limiting the length of runs without transitions to improve CDR (clock/data recovery), transmitting the data in DC balanced fashion to avoid baseline wander, and providing specialized patterns for symbol framing. Preferred embodiments of the invention employ a low overhead block code, such as an N-bit-to-(N+1)-bit code in which N bit words are encoded as (N+1) bit code words to meet these requirements. For example, the block code employed to generate the code words described with reference to Fig. 2 is a 9-bit-to-10-bit code in which 9 bit words are encoded as 10 bit code words to meet these requirements. Alternatively, a 7-bit-to-8-bit code in which 7 bit words are encoded as 8 bit code

words block code could be employed to generate the code words transmitted in accordance with the invention.

Another class of embodiments uses a low overhead block code in which K-bit words (where K = L + M) are broken into L-bit and M-bit fragments, each L-bit fragment is encoded as an (L+1)-bit code using an L-bit-to-(L+1)-bit block code, each M-bit fragment is encoded as an (M+1)-bit code using an M-bit-to-(M+1)-bit block code, and the (L+1)-bit and (M+1)-bit codes are concatenated to produce (L+M+2)-bit code words which are transmitted in an appropriate sequence (indicative of a cell) over a serial link. For example, L and M can satisfy L = 7 and M = 9, giving a total of 16 bits encoded into 18 bits.

In some N-bit-to-(N+1)-bit block codes that can be employed to implement the invention, a mapping is defined from N-bit input words to a "positive" codebook containing only (N+1)-bit code words of neutral or positive disparity, where a word of "positive disparity" includes more ones than zeros and a word of "neutral disparity" has an equal number of ones and zeros. The mapping of each code word of the positive codebook to a code word of a corresponding "negative" codebook is determined simply by complementing the former code word to generate the latter code word. Ideally, a mapping function from input words to the code words of the positive codebook (or the negative codebook) is found that is bijective and simple to implement as logic circuitry. However, even if such an ideal mapping function cannot be found, a simple mapping function can typically be identified that covers a large subset of the input symbol space, and the remaining input symbols are handled as special cases (e.g., special input symbols for which encoding must be accomplished using table lookup circuitry or other "secondary" encoding circuitry).

Throughout the disclosure, the expression "table lookup" denotes a mapping operation that is implemented in any manner (not necessarily by searching a ROM or CAM type memory for an output value in response to an input value). For example, table lookup can be implemented using a memory-based lookup table or a logic-based lookup table, as a complex logic function (that performs the equivalent of a memory-based table lookup), as a logic truth table/Karnaugh map, or in any other suitable manner.

For many applications, full lookup tables (for encoding or decoding) are not practical implementation choices. Preferred embodiments for such applications use a systematic mapping technique implemented by simple logic circuitry without any table

lookup circuitry (or with circuitry implementing only a small lookup table for handling a small subset of the full set of input words) for encoding and decoding. The encoder in each of circuit 32 and 42 of the Fig. 1 system preferably implements such a systematic mapping technique.

We next provide examples of low overhead block codes that can be employed to implement preferred embodiments of the invention. One such block code is a 9B/10B code defined by the positive and negative codebooks set forth as Table 1, another is a 9B/10B code defined by the positive and negative codebooks set forth as Table 4, another is a 9B/10B code defined by the positive and negative codebooks set forth as Table 5, and another such block code is a 7B/8B code defined by the positive and negative codebooks set forth as Table 3. Table 2 sets forth special characters that are suitable for use with the 10-bit code words set forth in Table 1.

We first describe the 9B/10B code whose code words are set forth as Table 1.

TABLE 1

Symbol	Positive Code	Positive Disparity	Negative Code	Negative Disparity	Primary Mapping?
0	1001000111	0	0110111000	0	
1	1000011110	0	0111100001	0	
2	1000011101	0	0111100010	0	
3	1110011000	0	0001100111	0	
4	1000011011	0	0111100100	0	
5	1110100010	0	0001011101	0	
6	1100010101	0	0011101010	0	
7	1110101000	0	0001010111	0	
8	1000010111	0	0111101000	0	
9	1110000110	0	0001111001	0	
10	1110000101	0	0001111010	0	
11	1110110000	0	0001001111	0	
12	1100100011	0	0011011100	0	
13	1100010110	0	0011101001	0	
14	1100100101	0	0011011010	0	
15	1100011010	0	0011100101	0	
16	1000101011	0	0111010100	0	
17	1100001110	0	0011110001	0	
18	1100001101	0	0011110010	0	
19	1100100110	0	0011011001	0	

20	1100001011	0	0011110100	0
21	1100101010	0	0011010101	0
22	1100101001	0	0011010110	0
23	1100101100	0	0011010011	0
24	1001001011	0	0110110100	0
25	1100110010	0	0011001101	0
26	1100110001	0	0011001110	0
27	1100110100	0	0011001011	0
28	1001010011	0	0110101100	0
29	1101001010	0	0010110101	0
30	1000101101	0	0111010010	0
31	1101010010	0	0010101101	0
32	1001100011	0	0110011100	0
33	1101010100	0	0010101011	0
34	1000110101	0	0111001010	0
35	1101011000	0	0010100111	0
36	1010001011	0	0101110100	0
37	1101100010	0	0010011101	0
38	1001001101	0	0110110010	0
39	1101101000	0	0010010111	0
40	1010010011	0	0101101100	0
41	1101110000	0	0010001111	0
42	1001010101	0	0110101010	0
43	1000101110	0	0111010001	0
44	1010100011	0	0101011100	0
45	1000110110	0	0111001001	0
46	1001011001	0	0110100110	0
47	1000111010	0	0111000101	0
48	1001100101	0	0110011010	0
49	1001001110	0	0110110001	0
50	1001101001	0	0110010110	0
51	1001010110	0	0110101001	0
52	1001110001	0	0110001110	0
53	1001011010	0	0110100101	0
54	1010001101	0	0101110010	0
55	1001100110	0	0110011001	0
56	1010010101	0	0101101010	0
57	1001101010	0	0110010101	0
58	1010011001	0	0101100110	0

59	1001110010	0	0110001101	0	
60	1010100101	0	0101011010	0	
61	1001110100	0	0110001011	0	
62	1010101001	0	0101010110	0	
63	1010001110	0	0101110001	0	
64	1110100001	0	0001011110	0	
65	1110111110	6	0001000001	-6	Y
66	1110111101	6	0001000010	-6	Y
67	1110111100	4	0001000011	-4	Y
68	1110111011	6	0001000100	-6	Y
69	1110111010	4	0001000101	-4	Y
70	1110111001	4	0001000110	-4	Y
71	1110111000	2	0001000111	-2	Y
72	1110110111	6	0001001000	-6	Y
73	1110110110	4	0001001001	-4	Y
74	1110110101	4	0001001010	-4	Y
75	1110110100	2	0001001011	-2	Y
76	1110110011	4	0001001100	-4	Y
77	1110110010	2	0001001101	2	Y
78	1110110001	2	0001001110	-2	Y
79	0001001111	0	1110110000	0	Y
80	1110101111	6	0001010000	-6	Y
81	1110101110	4	0001010001	-4	Y
82	1110101101	4	0001010010	-4	Y
83	1110101100	2	0001010011	-2	Y
84	1110101011	4	0001010100	-4	Y
85	1110101010	2	0001010101	-2	Y
86	1110101001	2	0001010110	-2	Y
87	0001010111	0	1110101000	0	Y
88	1110100111	4	0001011000	-4	Y
89	1110100110	2	0001011001	-2	Y
90	1110100101	2	0001011010	-2	Y
91	0001011011	0	1110100100	0	Y
92	1110100011	2	0001011100	-2	Y
93	0001011101	0	1110100010	0	Y
94	0001011110	0	1110100001	0	Y
95	1110100100	0	0001011011	0	
96	1110010001	0	0001101110	0	
97	1110011110	4	0001100001	-4	Y

98	1110011101	4	0001100010	-4	Y
99	1110011100	2	0001100011	-2	Y
100	1110011011	4	0001100100	-4	Y
101	1110011010	2	0001100101	-2	Y
102	1110011001	2	0001100110	-2	Y
103	0001100111	0	1110011000	0	Y
104	1110010111	4	0001101000	-4	Y
105	1110010110	2	0001101001	-2	Y
106	1110010101	2	0001101010	-2	Y
107	0001101011	0	1110010100	0	Y
108	1110010011	2	0001101100	-2	Y
109	0001101101	0	1110010010	0	Y
110	0001101110	0	1110010001	0	Y
111	0001101111	2	1110010000	-2	Y
112	1110001010	0	0001110101	0	
113	1110001110	2	0001110001	-2	Y
114	1110001101	2	0001110010	-2	Y
115	0001110011	0	1110001100	0	Y
116	1110001011	2	0001110100	-2	Y
117	0001110101	0	1110001010	0	Y
118	0001110110	0	1110001001	0	Y
119	0001110111	2	1110001000	-2	Y
120	1110010010	0	0001101101	0	
121	0001111001	0	1110000110	0	Y
122	0001111010	0	1110000101	0	Y
123	0001111011	2	1110000100	-2	Y
124	1110010100	0	0001101011	0	
125	0001111101	2	1110000010	-2	Y
126	1110001001	0	0001110110	0	
127	1110001100	0	0001110011	0	
128	1101000011	0	0010111100	0	
129	1101111110	6	0010000001	-6	Y
130	1101111101	6	0010000010	-6	Y
131	1101111100	4	0010000011	-4	Y
132	1101111011	6	0010000100	-6	Y
133	1101111010	4	0010000101	-4	Y
134	1101111001	4	0010000110	-4	Y
135	1101111000	2	0010000111	-2	Y
136	1101110111	6	0010001000	-6	Y

137	1101110110	4	0010001001	-4	Y
138	1101110101	4	0010001010	-4	Y
139	1101110100	2	0010001011	-2	Y
140	1101110011	4	0010001100	-4	Y
141	1101110010	2	0010001101	-2	Y
142	1101110001	2	0010001110	-2	Y
143	0010001111	0	1101110000	0	Y
144	1101101111	6	0010010000	-6	Y
145	1101101110	4	0010010001	-4	Y
146	1101101101	4	0010010010	-4	Y
147	1101101100	2	0010010011	-2	Y
148	1101101011	4	0010010100	-4	Y
149	1101101010	2	0010010101	-2	Y
150	1101101001	2	0010010110	-2	Y
151	0010010111	0	1101101000	0	Y
152	1101100111	4	0010011000	-4	Y
153	1101100110	2	0010011001	-2	Y
154	1101100101	2	0010011010	-2	Y
155	0010011011	0	1101100100	0	Y
156	1101100011	2	0010011100	-2	Y
157	0010011101	0	1101100010	0	Y
158	0010011110	0	1101100001	0	Y
159	1101100100	0	0010011011	0	
160	1101000101	0	0010111010	0	
161	1101011110	4	0010100001	-4	Y
162	1101011101	4	0010100010	-4	Y
163	1101011100	2	0010100011	-2	Y
164	1101011011	4	0010100100	-4	Y
165	1101011010	2	0010100101	-2	Y
166	1101011001	2	0010100110	-2	Y
167	0010100111	0	1101011000	0	Y
168	1101010111	4	0010101000	-4	Y
169	1101010110	2	0010101001	-2	Y
170	1101010101	2	0010101010	-2	Y
171	0010101011	0	1101010100	0	Y
172	1101010011	2	0010101100	-2	Y
173	0010101101	0	1101010010	0	Y
174	0010101110	0	1101010001	0	Y
175	0010101111	2	1101010000	-2	Y

176	1101001111	4	0010110000	-4	Y
177	1101001110	2	0010110001	-2	Y
178	1101001101	2	0010110010	-2	Y
179	0010110011	0	1101001100	0	Y
180	1101001011	2	0010110100	-2	Y
181	0010110101	0	1101001010	0	Y
182	0010110110	0	1101001001	0	Y
183	0010110111	2	1101001000	-2	Y
184	1101000111	2	0010111000	-2	Y
185	0010111001	0	1101000110	0	Y
186	0010111010	0	1101000101	0	Y
187	0010111011	2	1101000100	-2	Y
188	0010111100	0	1101000011	0	Y
189	0010111101	2	1101000010	-2	Y
190	0010111110	2	1101000001	-2	Y
191	1101001100	0	0010110011	0	
192	1101001001	0	0010110110	0	
193	1100111110	4	0011000001	-4	Y
194	1100111101	4	0011000010	-4	Y
195	1100111100	2	0011000011	-2	Y
196	1100111011	4	0011000100	-4	Y
197	1100111010	2	0011000101	-2	Y
198	1100111001	2	0011000110	-2	Y
199	0011000111	0	1100111000	0	Y
200	1100110111	4	0011001000	-4	Y
201	1100110110	2	0011001001	-2	Y
202	1100110101	2	0011001010	-2	Y
203	0011001011	0	1100110100	0	Y
204	1100110011	2	0011001100	-2	Y
205	0011001101	0	1100110010	0	Y
206	0011001110	0	1100110001	0	Y
207	0011001111	2	1100110000	-2	Y
208	1100101111	4	0011010000	-4	Y
209	1100101110	2	0011010001	-2	Y
210	1100101101	2	0011010010	-2	Y
211	0011010011	0	1100101100	0	Y
212	1100101011	2	0011010100	-2	Y
213	0011010101	0	1100101010	0	Y
214	0011010110	0	1100101001	0	Y

215	0011010111	2	1100101000	-2	Y
216	1100100111	2	0011011000	-2	Y
217	0011011001	0	1100100110	0	Y
218	0011011010	0	1100100101	0	Y
219	0011011011	2	1100100100	-2	Y
220	0011011100	0	1100100011	0	Y
221	0011011101	2	1100100010	-2	Y
222	0011011110	2	1100100001	-2	Y
223	1100111000	0	0011000111	0	
224	1101010001	0	0010101110	0	
225	1100011110	2	0011100001	-2	Y
226	1100011101	2	0011100010	-2	Y
227	0011100011	0	1100011100	0	Y
228	1100011011	2	0011100100	-2	Y
229	0011100101	0	1100011010	0	Y
230	0011100110	0	1100011001	0	Y
231	0011100111	2	1100011000	-2	Y
232	1100010111	2	0011101000	-2	Y
233	0011101001	0	1100010110	0	Y
234	0011101010	0	1100010101	0	Y
235	0011101011	2	1100010100	-2	Y
236	0011101100	0	1100010011	0	Y
237	0011101101	2	1100010010	-2	Y
238	0011101110	2	1100010001	-2	Y
239	0011101111	4	1100010000	-4	Y
240	1101100001	0	0010011110	0	
241	0011110001	0	1100001110	0	Y
242	0011110010	0	1100001101	0	Y
243	0011110011	2	1100001100	-2	Y
244	0011110100	0	1100001011	0	Y
245	0011110101	2	1100001010	-2	Y
246	0011110110	2	1100001001	-2	Y
247	0011110111	4	1100001000	-4	Y
248	1101000110	0	0010111001	0	
249	0011111001	2	1100000110	-2	Y
250	0011111010	2	1100000101	-2	Y
251	0011111011	4	1100000100	-4	Y
252	1100010011	0	0011101100	0	
253	0011111101	4	1100000010	-4	Y

254	1100011001	0	0011100110	0	
255	1100011100	0	0011100011	0	
256	1010000111	0	0101111000	0	
257	1011111110	6	0100000001	-6	Y
258	1011111101	6	0100000010	-6	Y
259	1011111100	4	0100000011	-4	Y
260	1011111011	6	0100000100	-6	Y
261	1011111010	4	0100000101	-4	Y
262	1011111001	4	0100000110	-4	Y
263	1011111000	2	0100000111	-2	Y
264	1011110111	6	0100001000	-6	Y
265	1011110110	4	0100001001	-4	Y
266	1011110101	4	0100001010	-4	Y
267	1011110100	2	0100001011	-2	Y
268	1011110011	4	0100001100	-4	Y
269	1011110010	2	0100001101	-2	Y
270	1011110001	2	0100001110	-2	Y
271	0100001111	0	1011110000	0	Y
272	1011101111	6	0100010000	-6	Y
273	1011101110	4	0100010001	-4	Y
274	1011101101	4	0100010010	-4	Y
275	1011101100	2	0100010011	-2	Y
276	1011101011	4	0100010100	-4	Y
277	1011101010	2	0100010101	-2	Y
278	1011101001	2	0100010110	-2	Y
279	0100010111	0	1011101000	0	Y
280	1011100111	4	0100011000	-4	Y
281	1011100110	2	0100011001	-2	Y
282	1011100101	2	0100011010	-2	Y
283	0100011011	0	1011100100	0	Y
284	1011100011	2	0100011100	-2	Y
285	0100011101	0	1011100010	0	Y
286	0100011110	0	1011100001	0	Y
287	1011100100	0	0100011011	0	
288	1011000011	0	0100111100	0	
289	1011011110	4	0100100001	-4	Y
290	1011011101	4	0100100010	-4	Y
291	1011011100	2	0100100011	-2	Y
292	1011011011	4	0100100100	-4	Y

293	1011011010	2	0100100101	-2	Y
294	1011011001	2	0100100110	-2	Y
295	0100100111	0	1011011000	0	Y
296	1011010111	4	0100101000	-4	Y
297	1011010110	2	0100101001	-2	Y
298	1011010101	2	0100101010	-2	Y
299	0100101011	0	1011010100	0	Y
300	1011010011	2	0100101100	-2	Y
301	0100101101	0	1011010010	0	Y
302	0100101110	0	1011010001	0	Y
303	0100101111	2	1011010000	-2	Y
304	1011001111	4	0100110000	-4	Y
305	1011001110	2	0100110001	-2	Y
306	1011001101	2	0100110010	-2	Y
307	0100110011	0	1011001100	0	Y
308	1011001011	2	0100110100	-2	Y
309	0100110101	0	1011001010	0	Y
310	0100110110	0	1011001001	0	Y
311	0100110111	2	1011001000	-2	Y
312	1011000111	2	0100111000	-2	Y
313	0100111001	0	1011000110	0	Y
314	0100111010	0	1011000101	0	Y
315	0100111011	2	1011000100	-2	Y
316	0100111100	0	1011000011	0	Y
317	0100111101	2	1011000010	-2	Y
318	0100111110	2	1011000001	-2	Y
319	1011001100	0	0100110011	0	
320	1011000101	0	0100111010	0	
321	1010111110	4	0101000001	-4	Y
322	1010111101	4	0101000010	-4	Y
323	1010111100	2	0101000011	-2	Y
324	1010111011	4	0101000100	-4	Y
325	1010111010	2	0101000101	-2	Y
326	1010111001	2	0101000110	-2	Y
327	0101000111	0	1010111000	0	Y
328	1010110111	4	0101001000	-4	Y
329	1010110110	2	0101001001	-2	Y
330	1010110101	2	0101001010	-2	Y
331	0101001011	0	1010110100	0	Y

332	1010110011	2	0101001100	-2	Y
333	0101001101	0	1010110010	0	Y
334	0101001110	0	1010110001	0	Y
335	0101001111	2	1010110000	-2	Y
336	1010101111	4	0101010000	-4	Y
337	1010101110	2	0101010001	-2	Y
338	1010101101	2	0101010010	-2	Y
339	0101010011	0	1010101100	0	Y
340	1010101011	2	0101010100	-2	Y
341	0101010101	0	1010101010	0	Y
342	0101010110	0	1010101001	0	Y
343	0101010111	2	1010101000	-2	Y
344	1010100111	2	0101011000	-2	Y
345	0101011001	0	1010100110	0	Y
346	0101011010	0	1010100101	0	Y
347	0101011011	2	1010100100	-2	Y
348	0101011100	0	1010100011	0	Y
349	0101011101	2	1010100010	-2	Y
350	0101011110	2	1010100001	-2	Y
351	1010111000	0	0101000111	0	
352	1011001001	0	0100110110	0	
353	1010011110	2	0101100001	-2	Y
354	1010011101	2	0101100010	-2	Y
355	0101100011	0	1010011100	0	Y
356	1010011011	2	0101100100	-2	Y
357	0101100101	0	1010011010	0	Y
358	0101100110	0	1010011001	0	Y
359	0101100111	2	1010011000	-2	Y
360	1010010111	2	0101101000	-2	Y
361	0101101001	0	1010010110	0	Y
362	0101101010	0	1010010101	0	Y
363	0101101011	2	1010010100	-2	Y
364	0101101100	0	1010010011	0	Y
365	0101101101	2	1010010010	-2	Y
366	0101101110	2	1010010001	-2	Y
367	0101101111	4	1010010000	-4	Y
368	1010001111	2	0101110000	-2	Y
369	0101110001	0	1010001110	0	Y
370	0101110010	0	1010001101	0	Y

371	0101110011	2	1010001100	-2	Y
372	0101110100	0	1010001011	0	Y
373	0101110101	2	1010001010	-2	Y
374	0101110110	2	1010001001	-2	Y
375	0101110111	4	1010001000	-4	Y
376	0101111000	0	1010000111	0	Y
377	0101111001	2	1010000110	-2	Y
378	0101111010	2	1010000101	-2	Y
379	0101111011	4	1010000100	-4	Y
380	0101111100	2	1010000011	-2	Y
381	0101111101	4	1010000010	-4	Y
382	0101111110	4	1010000001	-4	Y
383	1010011100	0	0101100011	0	
384	1011010001	0	0100101110	0	
385	1001111110	4	0110000001	-4	Y
386	1001111101	4	0110000010	-4	Y
387	1001111100	2	0110000011	-2	Y
388	1001111011	4	0110000100	-4	Y
389	1001111010	2	0110000101	-2	Y
390	1001111001	2	0110000110	-2	Y
391	0110000111	0	1001111000	0	Y
392	1001110111	4	0110001000	-4	Y
393	1001110110	2	0110001001	-2	Y
394	1001110101	2	0110001010	-2	Y
395	0110001011	0	1001110100	0	Y
396	1001110011	2	0110001100	-2	Y
397	0110001101	0	1001110010	0	Y
398	0110001110	0	1001110001	0	Y
399	0110001111	2	1001110000	-2	Y
400	1001101111	4	0110010000	-4	Y
401	1001101110	2	0110010001	-2	Y
402	1001101101	2	0110010010	-2	Y
403	0110010011	0	1001101100	0	Y
404	1001101011	2	0110010100	-2	Y
405	0110010101	0	1001101010	0	Y
406	0110010110	0	1001101001	0	Y
407	0110010111	2	1001101000	-2	Y
408	1001100111	2	0110011000	-2	Y
409	0110011001	0	1001100110	0	Y

410	0110011010	0	1001100101	0	Y
411	0110011011	2	1001100100	-2	Y
412	0110011100	0	1001100011	0	Y
413	0110011101	2	1001100010	-2	Y
414	0110011110	2	1001100001	-2	Y
415	1001111000	0	0110000111	0	
416	1011100001	0	0100011110	0	
417	1001011110	2	0110100001	-2	Y
418	1001011101	2	0110100010	-2	Y
419	0110100011	0	1001011100	0	Y
420	1001011011	2	0110100100	-2	Y
421	0110100101	0	1001011010	0	Y
422	0110100110	0	1001011001	0	Y
423	0110100111	2	1001011000	-2	Y
424	1001010111	2	0110101000	-2	Y
425	0110101001	0	1001010110	0	Y
426	0110101010	0	1001010101	0	Y
427	0110101011	2	1001010100	-2	Y
428	0110101100	0	1001010011	0	Y
429	0110101101	2	1001010010	-2	Y
430	0110101110	2	1001010001	-2	Y
431	0110101111	4	1001010000	-4	Y
432	1001001111	2	0110110000	-2	Y
433	0110110001	0	1001001110	0	Y
434	0110110010	0	1001001101	0	Y
435	0110110011	2	1001001100	-2	Y
436	0110110100	0	1001001011	0	Y
437	0110110101	2	1001001010	-2	Y
438	0110110110	2	1001001001	-2	Y
439	0110110111	4	1001001000	-4	Y
440	0110111000	0	1001000111	0	Y
441	0110111001	2	1001000110	-2	Y
442	0110111010	2	1001000101	-2	Y
443	0110111011	4	1001000100	-4	Y
444	0110111100	2	1001000011	-2	Y
445	0110111101	4	1001000010	-4	Y
446	0110111110	4	1001000001	-4	Y
447	1000111100	0	0111000011	0	
448	1010110001	0	0101001110	0	

449	1000111110	2	0111000001	-2	Y
450	1000111101	2	0111000010	-2	Y
451	0111000011	0	1000111100	0	Y
452	1000111011	2	0111000100	-2	Y
453	0111000101	0	1000111010	0	Y
454	0111000110	0	1000111001	0	Y
455	0111000111	2	1000111000	-2	Y
456	1000110111	2	0111001000	-2	Y
457	0111001001	0	1000110110	0	Y
458	0111001010	0	1000110101	0	Y
459	0111001011	2	1000110100	-2	Y
460	0111001100	0	1000110011	0	Y
461	0111001101	2	1000110010	-2	Y
462	0111001110	2	1000110001	-2	Y
463	0111001111	4	1000110000	-4	Y
464	1000101111	2	0111010000	-2	Y
465	0111010001	0	1000101110	0	Y
466	0111010010	0	1000101101	0	Y
467	0111010011	2	1000101100	-2	Y
468	0111010100	0	1000101011	0	Y
469	0111010101	2	1000101010	-2	Y
470	0111010110	2	1000101001	-2	Y
471	0111010111	4	1000101000	-4	Y
472	0111011000	0	1000100111	0	Y
473	0111011001	2	1000100110	-2	Y
474	0111011010	2	1000100101	-2	Y
475	0111011011	4	1000100100	-4	Y
476	0111011100	2	1000100011	-2	Y
477	0111011101	4	1000100010	-4	Y
478	0111011110	4	1000100001	-4	Y
479	1001011100	0	0110100011	0	
480	1011000110	0	0100111001	0	
481	0111100001	0	1000011110	0	Y
482	0111100010	0	1000011101	0	Y
483	0111100011	2	1000011100	-2	Y
484	0111100100	0	1000011011	0	Y
485	0111100101	2	1000011010	-2	Y
486	0111100110	2	1000011001	-2	Y
487	0111100111	4	1000011000	-4	Y

488	0111101000	0	1000010111	0	Y
489	0111101001	2	1000010110	-2	Y
490	0111101010	2	1000010101	-2	Y
491	0111101011	4	1000010100	-4	Y
492	0111101100	2	1000010011	-2	Y
493	0111101101	4	1000010010	-4	Y
494	0111101110	4	1000010001	-4	Y
495	0111101111	6	1000010000	-6	Y
496	1011001010	0	0100110101	0	
497	0111110001	2	1000001110	-2	Y
498	0111110010	2	1000001101	-2	Y
499	0111110011	4	1000001100	-4	Y
500	0111110100	2	1000001011	-2	Y
501	0111110101	4	1000001010	-4	Y
502	0111110110	4	1000001001	-4	Y
503	0111110111	6	1000001000	-6	Y
504	1000100111	0	0111011000	0	
505	0111111001	4	1000000110	-4	Y
506	0111111010	4	1000000101	-4	Y
507	0111111011	6	1000000100	-6	Y
508	1000110011	0	0111001100	0	
509	0111111101	6	1000000010	-6	Y
510	1000111001	0	0111000110	0	
511	1001101100	0	0110010011	0	

A "primary" mapping for the 9B/10B code of Table 1 prepends a 0 bit to the input symbol so that disparity of the resulting code word (the number of "one" bits thereof minus the number of "0" bits thereof) is less than the disparity of the input symbol, and complements the resulting code word if its disparity is negative. This determines the 408 code words of the positive disparity codebook (set forth in Table 1 in the second column from the left) to which the input symbols are mapped by the primary mapping. Each code word in the positive disparity codebook (sometimes referred to as the "positive" codebook) has the non-negative disparity indicated (in the third column from the left in Table 1).

Table 1 includes decimal representations of the input symbol. However, in typical implementations of the invention, binary versions of input symbols are encoded

using an NB/(N+1)B block code (e.g., the block code of Table 1), and the resulting binary code words are used in accordance with the invention.

With reference to Table 1, the complement of each code word of positive disparity codebook determines the code word of the negative disparity codebook to which the relevant input symbol maps. This determines the 408 code words of the negative disparity codebook (set forth in Table 1 in the fourth column from the left) to which the input symbols are mapped by the primary mapping. Each code word in the negative disparity codebook (sometimes referred to as the "negative" codebook) has the non-positive disparity indicated (in the second column from the right in Table 1).

A secondary mapping for the 9B/10B code of Table 1 determines those code words in each row of Table 1 in which there is no "Y" symbol in the right column. (The primary mapping for this code determines those code words in each row of Table 1 in which there is a "Y" symbol in the right column).

Each input symbol maps to both a code word in the positive disparity codebook and a code word in the negative disparity codebook. The choice of which code word is used to encode each input symbol (in a sequence of input symbols to be encoded) is determined by the cumulative disparity of the code words that have been used to encode the previous input symbols in the sequence. More specifically, the code word from the positive codebook is used if the cumulative disparity is less than zero, and the code word from the negative codebook is used if the cumulative disparity is greater than or equal to zero.

For example, if the first input symbol (in a sequence of input symbols to be encoded) is the symbol "0" (the binary word 000000000), this input symbol is mapped to the code word "1001000111" from the positive codebook. Because this code word is determined by the secondary mapping, a table lookup is typically used to generate the code word in response to the input symbol.

If the next input symbol (in the same sequence) is the symbol "65" (the binary word 001000001), this input symbol is mapped to the code word "1110111110" from the positive codebook. This code word is determined by the primary mapping, so that typically, logic circuitry (rather than table lookup circuitry) is used to generate the code word in response to the input symbol.

If the third input symbol (in the same sequence) is also the symbol "65" (the binary word 001000001), this input symbol is mapped to the code word "0001000001"

from the negative codebook (since the cumulative disparity of the two previously generated code words is a positive number, 6).

The code words of the 9B/10B code of Table 1 are selected so that each code word has disparity in the range of [-6, 6] (even values only), so that each sequence of the code words has a maximum run length of 7, a running digital sum variation of 10, a transition density of at least 30% (i.e. at least 3 transitions per code word), and so that only a relative small number of input symbols (i.e., 104 symbols of the total set of 512 symbols) do not have a successful primary mapping (i.e., each of the positive and negative codebooks has 104 symbols that are determined by the secondary mapping). The code of Table 1 has an average of 5.207 transitions per code word (over all legal code word pairs). Error magnification is minimized so that only 16% to 17% of single bit errors result in a burst error of 6, 7, 8, or 9 bits in the decoded symbol.

Table 2 sets forth examples of special characters ("out-of-band" or "OOB" characters) that can be inserted in a stream of code words generated in accordance with the 9B/10B code of Table 1 (or the 9B/10B code of Table 4 or Table 5, described below).

Table 2: 9B/10B Out-of-Band Codes

OOB Code	Positive		Negative	
	Preamble	**Discriminant**	**Preamble**	**Discriminant**
OOB00	1100000000	1111111001	0011111111	0000000110
OOB01	1100000000	1111110011	0011111111	0000001100
OOB02	1100000000	1111100111	0011111111	0000011000
OOB03	1100000000	1111111010	0011111111	0000000101
OOB04	1100000000	1111110101	0011111111	0000001010
OOB05	1100000000	1111101011	0011111111	0000010100
OOB06	1100000000	1111010111	0011111111	0000101000
OOB07	1100000000	1111110110	0011111111	0000001001
OOB08	1100000000	1111101101	0011111111	0000010010
OOB09	1100000000	1111011011	0011111111	0000100100
OOB10	1100000000	1110110111	0011111111	0001001000
OOB11	1100000000	1111101110	0011111111	0000010001

OOB Code	Positive		Negative	
	Preamble	Discriminant	Preamble	Discriminant
OOB12	1100000000	1111011101	0011111111	0000100010
OOB13	1100000000	1110111011	0011111111	0001000100
OOB14	1100000000	1101110111	0011111111	0010001000
OOB15	1100000000	1111011110	0011111111	0000100001
OOB16	1100000000	1110111101	0011111111	0001000010
OOB17	1100000000	1101111011	0011111111	0010000100
OOB18	1100000000	1011110111	0011111111	0100001000
OOB19	1100000000	1110111110	0011111111	0001000001
OOB20	1100000000	1101111101	0011111111	0010000010
OOB21	1100000000	1011111011	0011111111	0100000100
OOB22	1100000000	1101111110	0011111111	0010000001
OOB23	1100000000	1011111101	0011111111	0100000010
OOB24	1100000000	1011111110	0011111111	0100000001

In Table 2, each special character consists of a 10-bit preamble followed by a 10-bit discriminant pattern. Each special character is thus a sequence of two, 10-bit words. The preamble contains a run of eight 0s or 1s, which guarantees it never appears in a legal sequence of 9B/10B code words (assuming that the Table 1, Table 4, or Table 5 implementation of the 9B/10B code is employed). Thus, the preamble can be used to establish symbol alignment. The preamble is commonly referred to as the "comma," "comma character, " or "comma symbol."

The discriminant identifies the code type. Applications may assign logical meanings to the OOB codes as necessary. For example, one OOB code can be used as an "idle" character (of a type described elsewhere herein) for simplex or duplex flow control, another can be used as a "link training" character (of a type described elsewhere herein), and others can be used as "state exchange" characters ("Si") of a type described elsewhere herein. A particular application may choose to use a subset of the possible OOB values in order to increase the Hamming distance between allowable codes, thereby reducing the probability of missing errors in the transmitted characters.

Each OOB code has a "positive" and "negative" version. "Positive" OOB codes are used when the current running disparity is positive. "Negative" OOB codes are used when the current running disparity is negative. This ensures that the maximum digital sum variation does not grow too large. OOB code bits are transmitted MSB first, where the MSB is depicted on the left in Table 2. It is an error to transmit or receive a sequence with a run of eight (or more) identical bits that does not match an OOB code, and it is also an error to transmit or receive a positive OOB code when current running disparity is negative or a negative OOB code when current running disparity is positive.

Since all the OOB codes start with a run of length two and end with runs of length no more than three, they may be inserted between any pair of 9B/10B code words (assuming that the 9B/10B code words begin and end with runs of length no greater than four in all cases) without producing a run of length greater than seven (except for the run of length eight within the preamble).

We next describe the 7B/8B code whose code words are set forth as Table 3.

TABLE 3

Symbol	Positive Code	Positive Disparity	Negative Code	Negative Disparity	Primary Mapping?
0	11000011	0	00111100	0	
1	10001110	0	01110001	0	
2	10001101	0	01110010	0	
3	11100100	0	00011011	0	
4	10001011	0	01110100	0	
5	11101000	0	00010111	0	
6	11000101	0	00111010	0	
7	11000110	0	00111001	0	
8	10000111	0	01111000	0	
9	11001010	0	00110101	0	
10	11001001	0	00110110	0	
11	11010100	0	00101011	0	
12	10010011	0	01101100	0	
13	11011000	0	00100111	0	
14	10010101	0	01101010	0	
15	10011010	0	01100101	0	
16	11100001	0	00011110	0	

17	11101110	4	00010001	-4	Y
18	11101101	4	00010010	-4	Y
19	11101100	2	00010011	-2	Y
20	11101011	4	00010100	-4	Y
21	11101010	2	00010101	-2	Y
22	11101001	2	00010110	-2	Y
23	00010111	0	11101000	0	Y
24	11100111	4	00011000	-4	Y
25	11100110	2	00011001	-2	Y
26	11100101	2	00011010	-2	Y
27	00011011	0	11100100	0	Y
28	11100011	2	00011100	-2	Y
29	00011101	0	11100010	0	Y
30	00011110	0	11100001	0	Y
31	11100010	0	00011101	0	
32	11010001	0	00101110	0	
33	11011110	4	00100001	-4	Y
34	11011101	4	00100010	-4	Y
35	11011100	2	00100011	-2	Y
36	11011011	4	00100100	-4	Y
37	11011010	2	00100101	-2	Y
38	11011001	2	00100110	-2	Y
39	00100111	0	11011000	0	Y
40	11010111	4	00101000	-4	Y
41	11010110	2	00101001	-2	Y
42	11010101	2	00101010	-2	Y
43	00101011	0	11010100	0	Y
44	11010011	2	00101100	-2	Y
45	00101101	0	11010010	0	Y
46	00101110	0	11010001	0	Y
47	11010010	0	00101101	0	
48	10100011	0	01011100	0	
49	11001110	2	00110001	-2	Y
50	11001101	2	00110010	-2	Y
51	00110011	0	11001100	0	Y
52	11001011	2	00110100	-2	Y
53	00110101	0	11001010	0	Y
54	00110110	0	11001001	0	Y
55	00110111	2	11001000	-2	Y

56	11000111	2	00111000	-2	Y
57	00111001	0	11000110	0	Y
58	00111010	0	11000101	0	Y
59	00111011	2	11000100	-2	Y
60	00111100	0	11000011	0	Y
61	00111101	2	11000010	-2	Y
62	00111110	2	11000001	-2	Y
63	11001100	0	00110011	0	
64	10110001	0	01001110	0	
65	10111110	4	01000001	-4	Y
66	10111101	4	01000010	-4	Y
67	10111100	2	01000011	-2	Y
68	10111011	4	01000100	-4	Y
69	10111010	2	01000101	-2	Y
70	10111001	2	01000110	-2	Y
71	01000111	0	10111000	0	Y
72	10110111	4	01001000	-4	Y
73	10110110	2	01001001	-2	Y
74	10110101	2	01001010	-2	Y
75	01001011	0	10110100	0	Y
76	10110011	2	01001100	-2	Y
77	01001101	0	10110010	0	Y
78	01001110	0	10110001	0	Y
79	10110010	0	01001101	0	
80	10110100	0	01001011	0	
81	10101110	2	01010001	-2	Y
82	10101101	2	01010010	-2	Y
83	01010011	0	10101100	0	Y
84	10101011	2	01010100	-2	Y
85	01010101	0	10101010	0	Y
86	01010110	0	10101001	0	Y
87	01010111	2	10101000	-2	Y
88	10100111	2	01011000	-2	Y
89	01011001	0	10100110	0	Y
90	01011010	0	10100101	0	Y
91	01011011	2	10100100	-2	Y
92	01011100	0	10100011	0	Y
93	01011101	2	10100010	-2	Y
94	01011110	2	10100001	-2	Y

95	10101100	0	01010011	0	
96	10011001	0	01100110	0	
97	10011110	2	01100001	-2	Y
98	10011101	2	01100010	-2	Y
99	01100011	0	10011100	0	Y
100	10011011	2	01100100	-2	Y
101	01100101	0	10011010	0	Y
102	01100110	0	10011001	0	Y
103	01100111	2	10011000	-2	Y
104	10010111	2	01101000	-2	Y
105	01101001	0	10010110	0	Y
106	01101010	0	10010101	0	Y
107	01101011	2	10010100	-2	Y
108	01101100	0	10010011	0	Y
109	01101101	2	10010010	-2	Y
110	01101110	2	10010001	-2	Y
111	10011100	0	01100011	0	
112	10100101	0	01011010	0	
113	01110001	0	10001110	0	Y
114	01110010	0	10001101	0	Y
115	01110011	2	10001100	-2	Y
116	01110100	0	10001011	0	Y
117	01110101	2	10001010	-2	Y
118	01110110	2	10001001	-2	Y
119	01110111	4	10001000	-4	Y
120	01111000	0	10000111	0	Y
121	01111001	2	10000110	-2	Y
122	01111010	2	10000101	-2	Y
123	01111011	4	10000100	-4	Y
124	01111100	2	10000011	-2	Y
125	01111101	4	10000010	-4	Y
126	01111110	4	10000001	-4	Y
127	10010110	0	01101001	0	

The primary mapping for the 7B/8B code of Table 3 also prepends a 0 bit to the input symbol so that disparity of the resulting code word (the number of "one" bits thereof minus the number of "0" bits thereof) is less than the disparity of the input symbol, and complements the resulting code word if its disparity is negative. This

determines the 98 code words of the positive disparity codebook (set forth in Table 3 in the second column from the left) to which the input symbols are mapped by the primary mapping. Each code word in the positive disparity codebook (sometimes referred to as the "positive" codebook) has the non-negative disparity indicated (in the third column from the left in Table 3).

The complement of each code word of positive disparity codebook determines the code word of the negative disparity codebook to which the relevant input symbol maps. This determines the 98 code words of the negative disparity codebook (set forth in Table 3 in the fourth column from the left) to which the input symbols are mapped by the primary mapping. Each code word in the negative disparity codebook (sometimes referred to as the "negative" codebook) has the non-positive disparity indicated (in the second column from the right in Table 3).

The secondary mapping for the 7B/8B code of Table 3 determines those code words in each row of Table 3 in which there is no "Y" symbol in the right column. (The primary mapping for this code determines those code words in each row of Table 3 in which there is a "Y" symbol in the right column).

Each input symbol maps to both a code word in the positive disparity codebook and a code word in the negative disparity codebook. The choice of which code word is used to encode each input symbol (in a sequence of input symbols to be encoded) is determined by the cumulative disparity of the code words that have been used to encode the previous input symbols in the sequence. More specifically, the code word from the positive codebook is used if the cumulative disparity is less than zero, and the code word from the negative codebook is used if the cumulative disparity is greater than or equal to zero.

The code words of the 7B/8B code of Table 3 are selected so that each code word has disparity in the range of [-4, 4] (even values only), so that each sequence of the code words has a maximum run length of 6, a running digital sum range of 16, a minimum transition density of 25% (i.e. at least 2 transitions per code word), and an average transition density of 4.181 transitions per code word (over all legal code word pairs) so that only a relative small number of input symbols (i.e., 30 symbols of the total set of 128 symbols) do not have a successful primary mapping (i.e., each of the positive and negative codebooks has 30 symbols that are determined by the secondary mapping). The normalized DC offset is 4.75. Error magnification is minimized so that only 10% of single bit errors result in a burst error of 6 or 7 bits in the decoded symbol.

In variations on the code set forth in Table 3 (or Table 1), the positive and negative codebooks are not strictly complements of each other. Rather, the code words having nonzero disparity are identical to those of Table 3 (or 1), so that the code words of the negative codebook having nonzero disparity are complements of corresponding code words of the positive codebook, but the code words of the negative codebook that have zero disparity are identical to corresponding code words of the positive codebook. The code words having zero disparity can be either the zero-disparity code words of the positive codebook of Table 3 (or 1) or the zero-disparity code words of the negative codebook of Table 3 (or 1).

We next describe the 9B/10B code whose code words are set forth as Table 4.

TABLE 4

Symbol	Positive Code	Positive Disparity	Negative Code	Negative Disparity	Primary Mapping?
0	1100010011	0	0011101100	0	N
1	1000011110	0	0111100001	0	N
2	1000011101	0	0111100010	0	N
3	1110000110	0	0001111001	0	N
4	1000011011	0	0111100100	0	N
5	1110001010	0	0001110101	0	N
6	1110000101	0	0001111010	0	N
7	1110010010	0	0001101101	0	N
8	1000010111	0	0111101000	0	N
9	1110010100	0	0001101011	0	N
10	1110001001	0	0001110110	0	N
11	1100010110	0	0011101001	0	N
12	1100100011	0	0011011100	0	N
13	1100011010	0	0011100101	0	N
14	1110010001	0	0001101110	0	N
15	1100100110	0	0011011001	0	N
16	1101000011	0	0010111100	0	N
17	1100001110	0	0011110001	0	N
18	1100001101	0	0011110010	0	N
19	1100101010	0	0011010101	0	N
20	1100001011	0	0011110100	0	N
21	1100110010	0	0011001101	0	N
22	1100010101	0	0011101010	0	N
23	1101000110	0	0010111001	0	N

24	1100000111	0	0011111000	0	N
25	1101001010	0	0010110101	0	N
26	1100011001	0	0011100110	0	N
27	1101010010	0	0010101101	0	N
28	1000110011	0	0111001100	0	N
29	1101010100	0	0010101011	0	N
30	1100100101	0	0011011010	0	N
31	1001110010	0	0110001101	0	N
32	1001010011	0	0110101100	0	N
33	1000101110	0	0111010001	0	N
34	1000101101	0	0111010010	0	N
35	1111011100	4	0000100011	-4	Y
36	1000101011	0	0111010100	0	N
37	1111011010	4	0000100101	-4	Y
38	1111011001	4	0000100110	-4	Y
39	1111011000	2	0000100111	-2	Y
40	1000100111	0	0111011000	0	N
41	1111010110	4	0000101001	-4	Y
42	1111010101	4	0000101010	-4	Y
43	1111010100	2	0000101011	-2	Y
44	1111010011	4	0000101100	-4	Y
45	1111010010	2	0000101101	-2	Y
46	1111010001	2	0000101110	-2	Y
47	1010010110	0	0101101001	0	N
48	1001100011	0	0110011100	0	N
49	1111001110	4	0000110001	-4	Y
50	1111001101	4	0000110010	-4	Y
51	1111001100	2	0000110011	-2	Y
52	1111001011	4	0000110100	-4	Y
53	1111001010	2	0000110101	-2	Y
54	1111001001	2	0000110110	-2	Y
55	1010011010	0	0101100101	0	N
56	1111000111	4	0000111000	-4	Y
57	1111000110	2	0000111001	-2	Y
58	1111000101	2	0000111010	-2	Y
59	1010100110	0	0101011001	0	N
60	1111000011	2	0000111100	-2	Y
61	1010101010	0	0101010101	0	N
62	1100101001	0	0011010110	0	N
63	1010110010	0	0101001101	0	N

64	1110100001	0	0001011110	0	N
65	1001001110	0	0110110001	0	N
66	1001001101	0	0110110010	0	N
67	1110111100	4	0001000011	-4	Y
68	1110000011	0	0001111100	0	N
69	1110111010	4	0001000101	-4	Y
70	1110111001	4	0001000110	-4	Y
71	1110111000	2	0001000111	-2	Y
72	1001000111	0	0110111000	0	N
73	1110110110	4	0001001001	-4	Y
74	1110110101	4	0001001010	-4	Y
75	1110110100	2	0001001011	-2	Y
76	1110110011	4	0001001100	-4	Y
77	1110110010	2	0001001101	-2	Y
78	1110110001	2	0001001110	-2	Y
79	1110100010	0	0001011101	0	N
80	1110101000	0	0001010111	0	N
81	1110101110	4	0001010001	-4	Y
82	1110101101	4	0001010010	-4	Y
83	1110101100	2	0001010011	-2	Y
84	1110101011	4	0001010100	-4	Y
85	1110101010	2	0001010101	-2	Y
86	1110101001	2	0001010110	-2	Y
87	0001010111	0	1110101000	0	Y
88	1110100111	4	0001011000	-4	Y
89	1110100110	2	0001011001	-2	Y
90	1110100101	2	0001011010	-2	Y
91	0001011011	0	1110100100	0	Y
92	1110100011	2	0001011100	-2	Y
93	0001011101	0	1110100010	0	Y
94	0001011110	0	1110100001	0	Y
95	1110100100	0	0001011011	0	N
96	1010010011	0	0101101100	0	N
97	1110011110	4	0001100001	-4	Y
98	1110011101	4	0001100010	-4	Y
99	1110011100	2	0001100011	-2	Y
100	1110011011	4	0001100100	-4	Y
101	1110011010	2	0001100101	-2	Y
102	1110011001	2	0001100110	-2	Y
103	0001100111	0	1110011000	0	Y

104	1110010111	4	0001101000	-4	Y
105	1110010110	2	0001101001	-2	Y
106	1110010101	2	0001101010	-2	Y
107	0001101011	0	1110010100	0	Y
108	1110010011	2	0001101100	-2	Y
109	0001101101	0	1110010010	0	Y
110	0001101110	0	1110010001	0	Y
111	1110011000	0	0001100111	0	N
112	1010100011	0	0101011100	0	N
113	1110001110	2	0001110001	-2	Y
114	1110001101	2	0001110010	-2	Y
115	0001110011	0	1110001100	0	Y
116	1110001011	2	0001110100	-2	Y
117	0001110101	0	1110001010	0	Y
118	0001110110	0	1110001001	0	Y
119	0001110111	2	1110001000	-2	Y
120	1110000111	2	0001111000	-2	Y
121	0001111001	0	1110000110	0	Y
122	0001111010	0	1110000101	0	Y
123	0001111011	2	1110000100	-2	Y
124	0001111100	0	1110000011	0	Y
125	0001111101	2	1110000010	-2	Y
126	0001111110	2	1110000001	-2	Y
127	1110001100	0	0001110011	0	N
128	1101100001	0	0010011110	0	N
129	1010001110	0	0101110001	0	N
130	1010001101	0	0101110010	0	N
131	1101111100	4	0010000011	-4	Y
132	1001001011	0	0110110100	0	N
133	1101111010	4	0010000101	-4	Y
134	1101111001	4	0010000110	-4	Y
135	1101111000	2	0010000111	-2	Y
136	1010000111	0	0101111000	0	N
137	1101110110	4	0010001001	-4	Y
138	1101110101	4	0010001010	-4	Y
139	1101110100	2	0010001011	-2	Y
140	1101110011	4	0010001100	-4	Y
141	1101110010	2	0010001101	-2	Y
142	1101110001	2	0010001110	-2	Y
143	1101100010	0	0010011101	0	N

144	1101101000	0	0010010111	0	N
145	1101101110	4	0010010001	-4	Y
146	1101101101	4	0010010010	-4	Y
147	1101101100	2	0010010011	-2	Y
148	1101101011	4	0010010100	-4	Y
149	1101101010	2	0010010101	-2	Y
150	1101101001	2	0010010110	-2	Y
151	0010010111	0	1101101000	0	Y
152	1101100111	4	0010011000	-4	Y
153	1101100110	2	0010011001	-2	Y
154	1101100101	2	0010011010	-2	Y
155	0010011011	0	1101100100	0	Y
156	1101100011	2	0010011100	-2	Y
157	0010011101	0	1101100010	0	Y
158	0010011110	0	1101100001	0	Y
159	1101100100	0	0010011011	0	N
160	1011000011	0	0100111100	0	N
161	1101011110	4	0010100001	-4	Y
162	1101011101	4	0010100010	-4	Y
163	1101011100	2	0010100011	-2	Y
164	1101011011	4	0010100100	-4	Y
165	1101011010	2	0010100101	-2	Y
166	1101011001	2	0010100110	-2	Y
167	0010100111	0	1101011000	0	Y
168	1101010111	4	0010101000	-4	Y
169	1101010110	2	0010101001	-2	Y
170	1101010101	2	0010101010	-2	Y
171	0010101011	0	1101010100	0	Y
172	1101010011	2	0010101100	-2	Y
173	0010101101	0	1101010010	0	Y
174	0010101110	0	1101010001	0	Y
175	1101011000	0	0010100111	0	N
176	1100110001	0	0011001110	0	N
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178	1101001101	2	0010110010	-2	Y
179	0010110011	0	1101001100	0	Y
180	1101001011	2	0010110100	-2	Y
181	0010110101	0	1101001010	0	Y
182	0010110110	0	1101001001	0	Y
183	0010110111	2	1101001000	-2	Y

184	1101000111	2	0010111000	-2	Y
185	0010111001	0	1101000110	0	Y
186	0010111010	0	1101000101	0	Y
187	0010111011	2	1101000100	-2	Y
188	0010111100	0	1101000011	0	Y
189	0010111101	2	1101000010	-2	Y
190	0010111110	2	1101000001	-2	Y
191	1101001100	0	0010110011	0	N
192	1101000101	0	0010111010	0	N
193	1100111110	4	0011000001	-4	Y
194	1100111101	4	0011000010	-4	Y
195	1100111100	2	0011000011	-2	Y
196	1100111011	4	0011000100	-4	Y
197	1100111010	2	0011000101	-2	Y
198	1100111001	2	0011000110	-2	Y
199	0011000111	0	1100111000	0	Y
200	1100110111	4	0011001000	-4	Y
201	1100110110	2	0011001001	-2	Y
202	1100110101	2	0011001010	-2	Y
203	0011001011	0	1100110100	0	Y
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205	0011001101	0	1100110010	0	Y
206	0011001110	0	1100110001	0	Y
207	1100111000	0	0011000111	0	N
208	1101001001	0	0010110110	0	N
209	1100101110	2	0011010001	-2	Y
210	1100101101	2	0011010010	-2	Y
211	0011010011	0	1100101100	0	Y
212	1100101011	2	0011010100	-2	Y
213	0011010101	0	1100101010	0	Y
214	0011010110	0	1100101001	0	Y
215	0011010111	2	1100101000	-2	Y
216	1100100111	2	0011011000	-2	Y
217	0011011001	0	1100100110	0	Y
218	0011011010	0	1100100101	0	Y
219	0011011011	2	1100100100	-2	Y
220	0011011100	0	1100100011	0	Y
221	0011011101	2	1100100010	-2	Y
222	0011011110	2	1100100001	-2	Y
223	1100011100	0	0011100011	0	N

224	1101010001	0	0010101110	0	N
225	1100011110	2	0011100001	-2	Y
226	1100011101	2	0011100010	-2	Y
227	0011100011	0	1100011100	0	Y
228	1100011011	2	0011100100	-2	Y
229	0011100101	0	1100011010	0	Y
230	0011100110	0	1100011001	0	Y
231	0011100111	2	1100011000	-2	Y
232	1100010111	2	0011101000	-2	Y
233	0011101001	0	1100010110	0	Y
234	0011101010	0	1100010101	0	Y
235	0011101011	2	1100010100	-2	Y
236	0011101100	0	1100010011	0	Y
237	0011101101	2	1100010010	-2	Y
238	0011101110	2	1100010001	-2	Y
239	1100101100	0	0011010011	0	N
240	1000110101	0	0111001010	0	N
241	0011110001	0	1100001110	0	Y
242	0011110010	0	1100001101	0	Y
243	0011110011	2	1100001100	-2	Y
244	0011110100	0	1100001011	0	Y
245	0011110101	2	1100001010	-2	Y
246	0011110110	2	1100001001	-2	Y
247	0011110111	4	1100001000	-4	Y
248	0011111000	0	1100000111	0	Y
249	0011111001	2	1100000110	-2	Y
250	0011111010	2	1100000101	-2	Y
251	0011111011	4	1100000100	-4	Y
252	0011111100	2	1100000011	-2	Y
253	0011111101	4	1100000010	-4	Y
254	0011111110	4	1100000001	-4	Y
255	1100110100	0	0011001011	0	N
256	1011100001	0	0100011110	0	N
257	1011100010	0	0100011101	0	N
258	1011101000	0	0100010111	0	N
259	1011111100	4	0100000011	-4	Y
260	1010001011	0	0101110100	0	N
261	1011111010	4	0100000101	-4	Y
262	1011111001	4	0100000110	-4	Y
263	1011111000	2	0100000111	-2	Y

264	1001010101	0	0110101010	0	N
265	1011110110	4	0100001001	-4	Y
266	1011110101	4	0100001010	-4	Y
267	1011110100	2	0100001011	-2	Y
268	1011110011	4	0100001100	-4	Y
269	1011110010	2	0100001101	-2	Y
270	1011110001	2	0100001110	-2	Y
271	1011011000	0	0100100111	0	N
272	1001011001	0	0110100110	0	N
273	1011101110	4	0100010001	-4	Y
274	1011101101	4	0100010010	-4	Y
275	1011101100	2	0100010011	-2	Y
276	1011101011	4	0100010100	-4	Y
277	1011101010	2	0100010101	-2	Y
278	1011101001	2	0100010110	-2	Y
279	0100010111	0	1011101000	0	Y
280	1011100111	4	0100011000	-4	Y
281	1011100110	2	0100011001	-2	Y
282	1011100101	2	0100011010	-2	Y
283	0100011011	0	1011100100	0	Y
284	1011100011	2	0100011100	-2	Y
285	0100011101	0	1011100010	0	Y
286	0100011110	0	1011100001	0	Y
287	1011100100	0	0100011011	0	N
288	1001100101	0	0110011010	0	N
289	1011011110	4	0100100001	-4	Y
290	1011011101	4	0100100010	-4	Y
291	1011011100	2	0100100011	-2	Y
292	1011011011	4	0100100100	-4	Y
293	1011011010	2	0100100101	-2	Y
294	1011011001	2	0100100110	-2	Y
295	0100100111	0	1011011000	0	Y
296	1011010111	4	0100101000	-4	Y
297	1011010110	2	0100101001	-2	Y
298	1011010101	2	0100101010	-2	Y
299	0100101011	0	1011010100	0	Y
300	1011010011	2	0100101100	-2	Y
301	0100101101	0	1011010010	0	Y
302	0100101110	0	1011010001	0	Y
303	1010011100	0	0101100011	0	N

304	1001101001	0	0110010110	0	N
305	1011001110	2	0100110001	-2	Y
306	1011001101	2	0100110010	-2	Y
307	0100110011	0	1011001100	0	Y
308	1011001011	2	0100110100	-2	Y
309	0100110101	0	1011001010	0	Y
310	0100110110	0	1011001001	0	Y
311	0100110111	2	1011001000	-2	Y
312	1011000111	2	0100111000	-2	Y
313	0100111001	0	1011000110	0	Y
314	0100111010	0	1011000101	0	Y
315	0100111011	2	1011000100	-2	Y
316	0100111100	0	1011000011	0	Y
317	0100111101	2	1011000010	-2	Y
318	0100111110	2	1011000001	-2	Y
319	1010101100	0	0101010011	0	N
320	1001110001	0	0110001110	0	N
321	1010111110	4	0101000001	-4	Y
322	1010111101	4	0101000010	-4	Y
323	1010111100	2	0101000011	-2	Y
324	1010111011	4	0101000100	-4	Y
325	1010111010	2	0101000101	-2	Y
326	1010111001	2	0101000110	-2	Y
327	0101000111	0	1010111000	0	Y
328	1010110111	4	0101001000	-4	Y
329	1010110110	2	0101001001	-2	Y
330	1010110101	2	0101001010	-2	Y
331	0101001011	0	1010110100	0	Y
332	1010110011	2	0101001100	-2	Y
333	0101001101	0	1010110010	0	Y
334	0101001110	0	1010110001	0	Y
335	1010111000	0	0101000111	0	N
336	1010010101	0	0101101010	0	N
337	1010101110	2	0101010001	-2	Y
338	1010101101	2	0101010010	-2	Y
339	0101010011	0	1010101100	0	Y
340	1010101011	2	0101010100	-2	Y
341	0101010101	0	1010101010	0	Y
342	0101010110	0	1010101001	0	Y
343	0101010111	2	1010101000	-2	Y

344	1010100111	2	0101011000	-2	Y
345	0101011001	0	1010100110	0	Y
346	0101011010	0	1010100101	0	Y
347	0101011011	2	1010100100	-2	Y
348	0101011100	0	1010100011	0	Y
349	0101011101	2	1010100010	-2	Y
350	0101011110	2	1010100001	-2	Y
351	1010110100	0	0101001011	0	N
352	1010011001	0	0101100110	0	N
353	1010011110	2	0101100001	-2	Y
354	1010011101	2	0101100010	-2	Y
355	0101100011	0	1010011100	0	Y
356	1010011011	2	0101100100	-2	Y
357	0101100101	0	1010011010	0	Y
358	0101100110	0	1010011001	0	Y
359	0101100111	2	1010011000	-2	Y
360	1010010111	2	0101101000	-2	Y
361	0101101001	0	1010010110	0	Y
362	0101101010	0	1010010101	0	Y
363	0101101011	2	1010010100	-2	Y
364	0101101100	0	1010010011	0	Y
365	0101101101	2	1010010010	-2	Y
366	0101101110	2	1010010001	-2	Y
367	1011001100	0	0100110011	0	N
368	1010100101	0	0101011010	0	N
369	0101110001	0	1010001110	0	Y
370	0101110010	0	1010001101	0	Y
371	0101110011	2	1010001100	-2	Y
372	0101110100	0	1010001011	0	Y
373	0101110101	2	1010001010	-2	Y
374	0101110110	2	1010001001	-2	Y
375	0101110111	4	1010001000	-4	Y
376	0101111000	0	1010000111	0	Y
377	0101111001	2	1010000110	-2	Y
378	0101111010	2	1010000101	-2	Y
379	0101111011	4	1010000100	-4	Y
380	0101111100	2	1010000011	-2	Y
381	0101111101	4	1010000010	-4	Y
382	0101111110	4	1010000001	-4	Y
383	1011010100	0	0100101011	0	N

384	1010101001	0	0101010110	0	N
385	1001111110	4	0110000001	-4	Y
386	1001111101	4	0110000010	-4	Y
387	1001111100	2	0110000011	-2	Y
388	1001111011	4	0110000100	-4	Y
389	1001111010	2	0110000101	-2	Y
390	1001111001	2	0110000110	-2	Y
391	0110000111	0	1001111000	0	Y
392	1001110111	4	0110001000	-4	Y
393	1001110110	2	0110001001	-2	Y
394	1001110101	2	0110001010	-2	Y
395	0110001011	0	1001110100	0	Y
396	1001110011	2	0110001100	-2	Y
397	0110001101	0	1001110010	0	Y
398	0110001110	0	1001110001	0	Y
399	1001111000	0	0110000111	0	N
400	1010110001	0	0101001110	0	N
401	1001101110	2	0110010001	-2	Y
402	1001101101	2	0110010010	-2	Y
403	0110010011	0	1001101100	0	Y
404	1001101011	2	0110010100	-2	Y
405	0110010101	0	1001101010	0	Y
406	0110010110	0	1001101001	0	Y
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408	1001100111	2	0110011000	-2	Y
409	0110011001	0	1001100110	0	Y
410	0110011010	0	1001100101	0	Y
411	0110011011	2	1001100100	-2	Y
412	0110011100	0	1001100011	0	Y
413	0110011101	2	1001100010	-2	Y
414	0110011110	2	1001100001	-2	Y
415	1001011100	0	0110100011	0	N
416	1011000101	0	0100111010	0	N
417	1001011110	2	0110100001	-2	Y
418	1001011101	2	0110100010	-2	Y
419	0110100011	0	1001011100	0	Y
420	1001011011	2	0110100100	-2	Y
421	0110100101	0	1001011010	0	Y
422	0110100110	0	1001011001	0	Y
423	0110100111	2	1001011000	-2	Y

424	1001010111	2	0110101000	-2	Y
425	0110101001	0	1001010110	0	Y
426	0110101010	0	1001010101	0	Y
427	0110101011	2	1001010100	-2	Y
428	0110101100	0	1001010011	0	Y
429	0110101101	2	1001010010	-2	Y
430	0110101110	2	1001010001	-2	Y
431	1001101100	0	0110010011	0	N
432	1011001001	0	0100110110	0	N
433	0110110001	0	1001001110	0	Y
434	0110110010	0	1001001101	0	Y
435	0110110011	2	1001001100	-2	Y
436	0110110100	0	1001001011	0	Y
437	0110110101	2	1001001010	-2	Y
438	0110110110	2	1001001001	-2	Y
439	0110110111	4	1001001000	-4	Y
440	0110111000	0	1001000111	0	Y
441	0110111001	2	1001000110	-2	Y
442	0110111010	2	1001000101	-2	Y
443	0110111011	4	1001000100	-4	Y
444	0110111100	2	1001000011	-2	Y
445	0110111101	4	1001000010	-4	Y
446	0110111110	4	1001000001	-4	Y
447	1001110100	0	0110001011	0	N
448	1011010001	0	0100101110	0	N
449	1000111110	2	0111000001	-2	Y
450	1000111101	2	0111000010	-2	Y
451	0111000011	0	1000111100	0	Y
452	1000111011	2	0111000100	-2	Y
453	0111000101	0	1000111010	0	Y
454	0111000110	0	1000111001	0	Y
455	0111000111	2	1000111000	-2	Y
456	1000110111	2	0111001000	-2	Y
457	0111001001	0	1000110110	0	Y
458	0111001010	0	1000110101	0	Y
459	0111001011	2	1000110100	-2	Y
460	0111001100	0	1000110011	0	Y
461	0111001101	2	1000110010	-2	Y
462	0111001110	2	1000110001	-2	Y
463	1000110110	0	0111001001	0	N

464	1011000110	0	0100111001	0	N
465	0111010001	0	1000101110	0	Y
466	0111010010	0	1000101101	0	Y
467	0111010011	2	1000101100	-2	Y
468	0111010100	0	1000101011	0	Y
469	0111010101	2	1000101010	-2	Y
470	0111010110	2	1000101001	-2	Y
471	0111010111	4	1000101000	-4	Y
472	0111011000	0	1000100111	0	Y
473	0111011001	2	1000100110	-2	Y
474	0111011010	2	1000100101	-2	Y
475	0111011011	4	1000100100	-4	Y
476	0111011100	2	1000100011	-2	Y
477	0111011101	4	1000100010	-4	Y
478	0111011110	4	1000100001	-4	Y
479	1001010110	0	0110101001	0	N
480	1011001010	0	0100110101	0	N
481	0111100001	0	1000011110	0	Y
482	0111100010	0	1000011101	0	Y
483	0111100011	2	1000011100	-2	Y
484	0111100100	0	1000011011	0	Y
485	0111100101	2	1000011010	-2	Y
486	0111100110	2	1000011001	-2	Y
487	0111100111	4	1000011000	-4	Y
488	0111101000	0	1000010111	0	Y
489	0111101001	2	1000010110	-2	Y
490	0111101010	2	1000010101	-2	Y
491	0111101011	4	1000010100	-4	Y
492	0111101100	2	1000010011	-2	Y
493	0111101101	4	1000010010	-4	Y
494	0111101110	4	1000010001	-4	Y
495	1001011010	0	0110100101	0	N
496	1011010010	0	0100101101	0	N
497	0111110001	2	1000001110	-2	Y
498	0111110010	2	1000001101	-2	Y
499	0111110011	4	1000001100	-4	Y
500	0111110100	2	1000001011	-2	Y
501	0111110101	4	1000001010	-4	Y
502	0111110110	4	1000001001	-4	Y
503	1001100110	0	0110011001	0	N

504	0111111000	2	1000000111	-2	Y
505	0111111001	4	1000000110	-4	Y
506	0111111010	4	1000000101	-4	Y
507	1000111100	0	0111000011	0	N
508	0111111100	4	1000000011	-4	Y
509	1000111010	0	0111000101	0	N
510	1000111001	0	0111000110	0	N
511	1001101010	0	0110010101	0	N

In Table 4, the 512 code words set forth in the second column from the left determine the positive disparity codebook of the Table 4 code to which the input symbols map. Each code word in the positive disparity codebook (sometimes referred to as the "positive" codebook) has the non-negative disparity indicated (in the third column from the left in Table 4). The complement of each code word of positive disparity codebook determines the code word of the negative disparity codebook to which the relevant input symbol maps. This determines the 512 code words of the negative disparity codebook (set forth in Table 4 in the fourth column from the left) to which the input symbols map. Each code word in the negative disparity codebook (sometimes referred to as the "negative" codebook) has the non-positive disparity indicated (in the second column from the right in Table 4).

The secondary mapping for the 9B/10B code of Table 4 determines those code words in each row of Table 4 in which there is an "N" symbol in the right column. (The primary mapping for this code determines those code words in each row of Table 4 in which there is a "Y" symbol in the right column).

The Table 4 code favors lower digital sum variation over higher transition density with the goal of providing better EMI characteristics for transmission of long distances. The code space is defined as follows:

each code word having disparity 0 has a run of length three or less on either end, and includes no run of length greater than six away from its ends;

each code word having disparity 2, -2, 4, or -4 has a run of length four or less on the left, a run of length three or less on the right, and includes no run of length greater than seven away from its ends;

no code word has disparity greater than 4 or less than -4; and

no code word has less than 2 transitions.

The code set forth in Table 4 has a maximum run length of 7, a running digital sum variation of 16, an average of 5.248 transitions per code word (over all legal code word pairs), and a normalized DC offset of 4.9. Of the 512 code words in the positive codebook, only 116 are not determined by the primary mapping.

In variations on the code set forth in Table 4, the positive and negative codebooks are not strictly complements of each other. Rather, the code words having nonzero disparity are identical to those of Table 4 (the code words of the negative codebook having nonzero disparity are complements of corresponding code words of the positive codebook) but the code words of the negative codebook that have zero disparity are identical to corresponding code words of the positive codebook. The code words having zero disparity can be either the zero-disparity code words of the positive codebook of Table 4 or the zero-disparity code words of the negative codebook of Table 4.

We next describe the 9B/10B code whose code words are set forth as Table 5.

TABLE 5

Symbol	Positive Code	Positive Disparity	Negative Code	Negative Disparity	Primary Mapping?
0	1001000111	0	0110111000	0	N
1	1000011110	0	0111100001	0	N
2	1000011101	0	0111100010	0	N
3	1100010110	0	0011101001	0	N
4	1000011011	0	0111100100	0	N
5	1100011010	0	0011100101	0	N
6	1100010101	0	0011101010	0	N
7	1100100110	0	0011011001	0	N
8	1000010111	0	0111101000	0	N
9	1110000110	0	0001111001	0	N
10	1110000101	0	0001111010	0	N
11	1100101010	0	0011010101	0	N
12	1100100011	0	0011011100	0	N
13	1100101100	0	0011010011	0	N
14	1100100101	0	0011011010	0	N
15	1100110010	0	0011001101	0	N
16	1000101011	0	0111010100	0	N
17	1100001110	0	0011110001	0	N
18	1100001101	0	0011110010	0	N

19	1100110100	0	0011001011	0	N
20	1100001011	0	0011110100	0	N
21	1101010010	0	0010101101	0	N
22	1100101001	0	0011010110	0	N
23	1101010100	0	0010101011	0	N
24	1001001011	0	0110110100	0	N
25	1101011000	0	0010100111	0	N
26	1100110001	0	0011001110	0	N
27	1101100010	0	0010011101	0	N
28	1001010011	0	0110101100	0	N
29	1101101000	0	0010010111	0	N
30	1000101101	0	0111010010	0	N
31	1000101110	0	0111010001	0	N
32	1001100011	0	0110011100	0	N
33	1000110110	0	0111001001	0	N
34	1000110101	0	0111001010	0	N
35	1001001110	0	0110110001	0	N
36	1010001011	0	0101110100	0	N
37	1001010110	0	0110101001	0	N
38	1001001101	0	0110110010	0	N
39	1001011010	0	0110100101	0	N
40	1010010011	0	0101101100	0	N
41	1001100110	0	0110011001	0	N
42	1001010101	0	0110101010	0	N
43	1001101010	0	0110010101	0	N
44	1010100011	0	0101011100	0	N
45	1001110010	0	0110001101	0	N
46	1001011001	0	0110100110	0	N
47	1001110100	0	0110001011	0	N
48	1001100101	0	0110011010	0	N
49	1010001110	0	0101110001	0	N
50	1001101001	0	0110010110	0	N
51	1010010110	0	0101101001	0	N
52	1001110001	0	0110001110	0	N
53	1010011010	0	0101100101	0	N
54	1010001101	0	0101110010	0	N
55	1010100110	0	0101011001	0	N
56	1010010101	0	0101101010	0	N
57	1010101010	0	0101010101	0	N
58	1010011001	0	0101100110	0	N

59	1010101100	0	0101010011	0	N
60	1010100101	0	0101011010	0	N
61	1010110010	0	0101001101	0	N
62	1010101001	0	0101010110	0	N
63	1010110100	0	0101001011	0	N
64	1110100001	0	0001011110	0	N
65	1110111110	6	0001000001	-6	Y
66	1110111101	6	0001000010	-6	Y
67	1110111100	4	0001000011	-4	Y
68	1110111011	6	0001000100	-6	Y
69	1110111010	4	0001000101	-4	Y
70	1110111001	4	0001000110	-4	Y
71	1110111000	2	0001000111	-2	Y
72	1110110111	6	0001001000	-6	Y
73	1110110110	4	0001001001	-4	Y
74	1110110101	4	0001001010	-4	Y
75	1110110100	2	0001001011	-2	Y
76	1110110011	4	0001001100	-4	Y
77	1110110010	2	0001001101	-2	Y
78	1110110001	2	0001001110	-2	Y
79	1110100010	0	0001011101	0	N
80	1110101111	6	0001010000	-6	Y
81	1110101110	4	0001010001	-4	Y
82	1110101101	4	0001010010	-4	Y
83	1110101100	2	0001010011	-2	Y
84	1110101011	4	0001010100	-4	Y
85	1110101010	2	0001010101	-2	Y
86	1110101001	2	0001010110	-2	Y
87	0001010111	0	1110101000	0	Y
88	1110100111	4	0001011000	-4	Y
89	1110100110	2	0001011001	-2	Y
90	1110100101	2	0001011010	-2	Y
91	0001011011	0	1110100100	0	Y
92	1110100011	2	0001011100	-2	Y
93	0001011101	0	1110100010	0	Y
94	0001011110	0	1110100001	0	Y
95	1110100100	0	0001011011	0	N
96	1110010001	0	0001101110	0	N
97	1110011110	4	0001100001	-4	Y
98	1110011101	4	0001100010	-4	Y

99	1110011100	2	0001100011	-2	Y
100	1110011011	4	0001100100	-4	Y
101	1110011010	2	0001100101	-2	Y
102	1110011001	2	0001100110	-2	Y
103	0001100111	0	1110011000	0	Y
104	1110010111	4	0001101000	-4	Y
105	1110010110	2	0001101001	-2	Y
106	1110010101	2	0001101010	-2	Y
107	0001101011	0	1110010100	0	Y
108	1110010011	2	0001101100	-2	Y
109	0001101101	0	1110010010	0	Y
110	0001101110	0	1110010001	0	Y
111	1110010100	0	0001101011	0	N
112	1110101000	0	0001010111	0	N
113	1110001110	2	0001110001	-2	Y
114	1110001101	2	0001110010	-2	Y
115	0001110011	0	1110001100	0	Y
116	1110001011	2	0001110100	-2	Y
117	0001110101	0	1110001010	0	Y
118	0001110110	0	1110001001	0	Y
119	1110001100	0	0001110011	0	N
120	1010110001	0	0101001110	0	N
121	0001111001	0	1110000110	0	Y
122	0001111010	0	1110000101	0	Y
123	1110010010	0	0001101101	0	N
124	1011011000	0	0100100111	0	N
125	1110001010	0	0001110101	0	N
126	1110001001	0	0001110110	0	N
127	1110011000	0	0001100111	0	N
128	1101000011	0	0010111100	0	N
129	1101111110	6	0010000001	-6	Y
130	1101111101	6	0010000010	-6	Y
131	1101111100	4	0010000011	-4	Y
132	1101111011	6	0010000100	-6	Y
133	1101111010	4	0010000101	-4	Y
134	1101111001	4	0010000110	-4	Y
135	1101111000	2	0010000111	-2	Y
136	1101110111	6	0010001000	-6	Y
137	1101110110	4	0010001001	-4	Y
138	1101110101	4	0010001010	-4	Y

139	1101110100	2	0010001011	-2	Y
140	1101110011	4	0010001100	-4	Y
141	1101110010	2	0010001101	-2	Y
142	1101110001	2	0010001110	-2	Y
143	1101100001	0	0010011110	0	N
144	1101101111	6	0010010000	-6	Y
145	1101101110	4	0010010001	-4	Y
146	1101101101	4	0010010010	-4	Y
147	1101101100	2	0010010011	-2	Y
148	1101101011	4	0010010100	-4	Y
149	1101101010	2	0010010101	-2	Y
150	1101101001	2	0010010110	-2	Y
151	0010010111	0	1101101000	0	Y
152	1101100111	4	0010011000	-4	Y
153	1101100110	2	0010011001	-2	Y
154	1101100101	2	0010011010	-2	Y
155	0010011011	0	1101100100	0	Y
156	1101100011	2	0010011100	-2	Y
157	0010011101	0	1101100010	0	Y
158	0010011110	0	1101100001	0	Y
159	1101100100	0	0010011011	0	N
160	1101000101	0	0010111010	0	N
161	1101011110	4	0010100001	-4	Y
162	1101011101	4	0010100010	-4	Y
163	1101011100	2	0010100011	-2	Y
164	1101011011	4	0010100100	-4	Y
165	1101011010	2	0010100101	-2	Y
166	1101011001	2	0010100110	-2	Y
167	0010100111	0	1101011000	0	Y
168	1101010111	4	0010101000	-4	Y
169	1101010110	2	0010101001	-2	Y
170	1101010101	2	0010101010	-2	Y
171	0010101011	0	1101010100	0	Y
172	1101010011	2	0010101100	-2	Y
173	0010101101	0	1101010010	0	Y
174	0010101110	0	1101010001	0	Y
175	0010101111	2	1101010000	-2	Y
176	1101001111	4	0010110000	-4	Y
177	1101001110	2	0010110001	-2	Y
178	1101001101	2	0010110010	-2	Y

179	0010110011	0	1101001100	0	Y
180	1101001011	2	0010110100	-2	Y
181	0010110101	0	1101001010	0	Y
182	0010110110	0	1101001001	0	Y
183	0010110111	2	1101001000	-2	Y
184	1101000111	2	0010111000	-2	Y
185	0010111001	0	1101000110	0	Y
186	0010111010	0	1101000101	0	Y
187	0010111011	2	1101000100	-2	Y
188	0010111100	0	1101000011	0	Y
189	0010111101	2	1101000010	-2	Y
190	0010111110	2	1101000001	-2	Y
191	1101001100	0	0010110011	0	N
192	1101001001	0	0010110110	0	N
193	1100111110	4	0011000001	-4	Y
194	1100111101	4	0011000010	-4	Y
195	1100111100	2	0011000011	-2	Y
196	1100111011	4	0011000100	-4	Y
197	1100111010	2	0011000101	-2	Y
198	1100111001	2	0011000110	-2	Y
199	0011000111	0	1100111000	0	Y
200	1100110111	4	0011001000	-4	Y
201	1100110110	2	0011001001	-2	Y
202	1100110101	2	0011001010	-2	Y
203	0011001011	0	1100110100	0	Y
204	1100110011	2	0011001100	-2	Y
205	0011001101	0	1100110010	0	Y
206	0011001110	0	1100110001	0	Y
207	0011001111	2	1100110000	-2	Y
208	1100101111	4	0011010000	-4	Y
209	1100101110	2	0011010001	-2	Y
210	1100101101	2	0011010010	-2	Y
211	0011010011	0	1100101100	0	Y
212	1100101011	2	0011010100	-2	Y
213	0011010101	0	1100101010	0	Y
214	0011010110	0	1100101001	0	Y
215	0011010111	2	1100101000	-2	Y
216	1100100111	2	0011011000	-2	Y
217	0011011001	0	1100100110	0	Y
218	0011011010	0	1100100101	0	Y

219	0011011011	2	1100100100	-2	Y
220	0011011100	0	1100100011	0	Y
221	0011011101	2	1100100010	-2	Y
222	0011011110	2	1100100001	-2	Y
223	1100111000	0	0011000111	0	N
224	1101010001	0	0010101110	0	N
225	1100011110	2	0011100001	-2	Y
226	1100011101	2	0011100010	-2	Y
227	0011100011	0	1100011100	0	Y
228	1100011011	2	0011100100	-2	Y
229	0011100101	0	1100011010	0	Y
230	0011100110	0	1100011001	0	Y
231	0011100111	2	1100011000	-2	Y
232	1100010111	2	0011101000	-2	Y
233	0011101001	0	1100010110	0	Y
234	0011101010	0	1100010101	0	Y
235	0011101011	2	1100010100	-2	Y
236	0011101100	0	1100010011	0	Y
237	0011101101	2	1100010010	-2	Y
238	0011101110	2	1100010001	-2	Y
239	0011101111	4	1100010000	-4	Y
240	1101000110	0	0010111001	0	N
241	0011110001	0	1100001110	0	Y
242	0011110010	0	1100001101	0	Y
243	0011110011	2	1100001100	-2	Y
244	0011110100	0	1100001011	0	Y
245	0011110101	2	1100001010	-2	Y
246	0011110110	2	1100001001	-2	Y
247	0011110111	4	1100001000	-4	Y
248	1101001010	0	0010110101	0	N
249	0011111001	2	1100000110	-2	Y
250	0011111010	2	1100000101	-2	Y
251	0011111011	4	1100000100	-4	Y
252	1100010011	0	0011101100	0	N
253	0011111101	4	1100000010	-4	Y
254	1100011001	0	0011100110	0	N
255	1100011100	0	0011100011	0	N
256	1010000111	0	0101111000	0	N
257	1011100001	0	0100011110	0	N
258	1011111101	6	0100000010	-6	Y

259	1011111100	4	0100000011	-4	Y
260	1011111011	6	0100000100	-6	Y
261	1011111010	4	0100000101	-4	Y
262	1011111001	4	0100000110	-4	Y
263	1011111000	2	0100000111	-2	Y
264	1011110111	6	0100001000	-6	Y
265	1011110110	4	0100001001	-4	Y
266	1011110101	4	0100001010	-4	Y
267	1011110100	2	0100001011	-2	Y
268	1011110011	4	0100001100	-4	Y
269	1011110010	2	0100001101	-2	Y
270	1011110001	2	0100001110	-2	Y
271	1011100010	0	0100011101	0	N
272	1011101111	6	0100010000	-6	Y
273	1011101110	4	0100010001	-4	Y
274	1011101101	4	0100010010	-4	Y
275	1011101100	2	0100010011	-2	Y
276	1011101011	4	0100010100	-4	Y
277	1011101010	2	0100010101	-2	Y
278	1011101001	2	0100010110	-2	Y
279	0100010111	0	1011101000	0	Y
280	1011100111	4	0100011000	-4	Y
281	1011100110	2	0100011001	-2	Y
282	1011100101	2	0100011010	-2	Y
283	0100011011	0	1011100100	0	Y
284	1011100011	2	0100011100	-2	Y
285	0100011101	0	1011100010	0	Y
286	0100011110	0	1011100001	0	Y
287	1011100100	0	0100011011	0	N
288	1011000011	0	0100111100	0	N
289	1011011110	4	0100100001	-4	Y
290	1011011101	4	0100100010	-4	Y
291	1011011100	2	0100100011	-2	Y
292	1011011011	4	0100100100	-4	Y
293	1011011010	2	0100100101	-2	Y
294	1011011001	2	0100100110	-2	Y
295	0100100111	0	1011011000	0	Y
296	1011010111	4	0100101000	-4	Y
297	1011010110	2	0100101001	-2	Y
298	1011010101	2	0100101010	-2	Y

299	0100101011	0	1011010100	0	Y
300	1011010011	2	0100101100	-2	Y
301	0100101101	0	1011010010	0	Y
302	0100101110	0	1011010001	0	Y
303	0100101111	2	1011010000	-2	Y
304	1011001111	4	0100110000	-4	Y
305	1011001110	2	0100110001	-2	Y
306	1011001101	2	0100110010	-2	Y
307	0100110011	0	1011001100	0	Y
308	1011001011	2	0100110100	-2	Y
309	0100110101	0	1011001010	0	Y
310	0100110110	0	1011001001	0	Y
311	0100110111	2	1011001000	-2	Y
312	1011000111	2	0100111000	-2	Y
313	0100111001	0	1011000110	0	Y
314	0100111010	0	1011000101	0	Y
315	0100111011	2	1011000100	-2	Y
316	0100111100	0	1011000011	0	Y
317	0100111101	2	1011000010	-2	Y
318	0100111110	2	1011000001	-2	Y
319	1011001100	0	0100110011	0	N
320	1011000101	0	0100111010	0	N
321	1010111110	4	0101000001	-4	Y
322	1010111101	4	0101000010	-4	Y
323	1010111100	2	0101000011	-2	Y
324	1010111011	4	0101000100	-4	Y
325	1010111010	2	0101000101	-2	Y
326	1010111001	2	0101000110	-2	Y
327	0101000111	0	1010111000	0	Y
328	1010110111	4	0101001000	-4	Y
329	1010110110	2	0101001001	-2	Y
330	1010110101	2	0101001010	-2	Y
331	0101001011	0	1010110100	0	Y
332	1010110011	2	0101001100	-2	Y
333	0101001101	0	1010110010	0	Y
334	0101001110	0	1010110001	0	Y
335	0101001111	2	1010110000	-2	Y
336	1010101111	4	0101010000	-4	Y
337	1010101110	2	0101010001	-2	Y
338	1010101101	2	0101010010	-2	Y

339	0101010011	0	1010101100	0	Y
340	1010101011	2	0101010100	-2	Y
341	0101010101	0	1010101010	0	Y
342	0101010110	0	1010101001	0	Y
343	0101010111	2	1010101000	-2	Y
344	1010100111	2	0101011000	-2	Y
345	0101011001	0	1010100110	0	Y
346	0101011010	0	1010100101	0	Y
347	0101011011	2	1010100100	-2	Y
348	0101011100	0	1010100011	0	Y
349	0101011101	2	1010100010	-2	Y
350	0101011110	2	1010100001	-2	Y
351	1010111000	0	0101000111	0	N
352	1011001001	0	0100110110	0	N
353	1010011110	2	0101100001	-2	Y
354	1010011101	2	0101100010	-2	Y
355	0101100011	0	1010011100	0	Y
356	1010011011	2	0101100100	-2	Y
357	0101100101	0	1010011010	0	Y
358	0101100110	0	1010011001	0	Y
359	0101100111	2	1010011000	-2	Y
360	1010010111	2	0101101000	-2	Y
361	0101101001	0	1010010110	0	Y
362	0101101010	0	1010010101	0	Y
363	0101101011	2	1010010100	-2	Y
364	0101101100	0	1010010011	0	Y
365	0101101101	2	1010010010	-2	Y
366	0101101110	2	1010010001	-2	Y
367	0101101111	4	1010010000	-4	Y
368	1010001111	2	0101110000	-2	Y
369	0101110001	0	1010001110	0	Y
370	0101110010	0	1010001101	0	Y
371	0101110011	2	1010001100	-2	Y
372	0101110100	0	1010001011	0	Y
373	0101110101	2	1010001010	-2	Y
374	0101110110	2	1010001001	-2	Y
375	0101110111	4	1010001000	-4	Y
376	0101111000	0	1010000111	0	Y
377	0101111001	2	1010000110	-2	Y
378	0101111010	2	1010000101	-2	Y

379	0101111011	4	1010000100	-4	Y
380	0101111100	2	1010000011	-2	Y
381	0101111101	4	1010000010	-4	Y
382	0101111110	4	1010000001	-4	Y
383	1010011100	0	0101100011	0	N
384	1011010001	0	0100101110	0	N
385	1001111110	4	0110000001	-4	Y
386	1001111101	4	0110000010	-4	Y
387	1001111100	2	0110000011	-2	Y
388	1001111011	4	0110000100	-4	Y
389	1001111010	2	0110000101	-2	Y
390	1001111001	2	0110000110	-2	Y
391	0110000111	0	1001111000	0	Y
392	1001110111	4	0110001000	-4	Y
393	1001110110	2	0110001001	-2	Y
394	1001110101	2	0110001010	-2	Y
395	0110001011	0	1001110100	0	Y
396	1001110011	2	0110001100	-2	Y
397	0110001101	0	1001110010	0	Y
398	0110001110	0	1001110001	0	Y
399	0110001111	2	1001110000	-2	Y
400	1001101111	4	0110010000	-4	Y
401	1001101110	2	0110010001	-2	Y
402	1001101101	2	0110010010	-2	Y
403	0110010011	0	1001101100	0	Y
404	1001101011	2	0110010100	-2	Y
405	0110010101	0	1001101010	0	Y
406	0110010110	0	1001101001	0	Y
407	0110010111	2	1001101000	-2	Y
408	1001100111	2	0110011000	-2	Y
409	0110011001	0	1001100110	0	Y
410	0110011010	0	1001100101	0	Y
411	0110011011	2	1001100100	-2	Y
412	0110011100	0	1001100011	0	Y
413	0110011101	2	1001100010	-2	Y
414	0110011110	2	1001100001	-2	Y
415	1001111000	0	0110000111	0	N
416	1011000110	0	0100111001	0	N
417	1001011110	2	0110100001	-2	Y
418	1001011101	2	0110100010	-2	Y

419	0110100011	0	1001011100	0	Y
420	1001011011	2	0110100100	-2	Y
421	0110100101	0	1001011010	0	Y
422	0110100110	0	1001011001	0	Y
423	0110100111	2	1001011000	-2	Y
424	1001010111	2	0110101000	-2	Y
425	0110101001	0	1001010110	0	Y
426	0110101010	0	1001010101	0	Y
427	0110101011	2	1001010100	-2	Y
428	0110101100	0	1001010011	0	Y
429	0110101101	2	1001010010	-2	Y
430	0110101110	2	1001010001	-2	Y
431	0110101111	4	1001010000	-4	Y
432	1001001111	2	0110110000	-2	Y
433	0110110001	0	1001001110	0	Y
434	0110110010	0	1001001101	0	Y
435	0110110011	2	1001001100	-2	Y
436	0110110100	0	1001001011	0	Y
437	0110110101	2	1001001010	-2	Y
438	0110110110	2	1001001001	-2	Y
439	0110110111	4	1001001000	-4	Y
440	0110111000	0	1001000111	0	Y
441	0110111001	2	1001000110	-2	Y
442	0110111010	2	1001000101	-2	Y
443	0110111011	4	1001000100	-4	Y
444	0110111100	2	1001000011	-2	Y
445	0110111101	4	1001000010	-4	Y
446	0110111110	4	1001000001	-4	Y
447	1000111100	0	0111000011	0	N
448	1011001010	0	0100110101	0	N
449	1000111110	2	0111000001	-2	Y
450	1000111101	2	0111000010	-2	Y
451	0111000011	0	1000111100	0	Y
452	1000111011	2	0111000100	-2	Y
453	0111000101	0	1000111010	0	Y
454	0111000110	0	1000111001	0	Y
455	0111000111	2	1000111000	-2	Y
456	1000110111	2	0111001000	-2	Y
457	0111001001	0	1000110110	0	Y
458	0111001010	0	1000110101	0	Y

459	0111001011	2	1000110100	-2	Y
460	0111001100	0	1000110011	0	Y
461	0111001101	2	1000110010	-2	Y
462	0111001110	2	1000110001	-2	Y
463	0111001111	4	1000110000	-4	Y
464	1000101111	2	0111010000	-2	Y
465	0111010001	0	1000101110	0	Y
466	0111010010	0	1000101101	0	Y
467	0111010011	2	1000101100	-2	Y
468	0111010100	0	1000101011	0	Y
469	0111010101	2	1000101010	-2	Y
470	0111010110	2	1000101001	-2	Y
471	0111010111	4	1000101000	-4	Y
472	0111011000	0	1000100111	0	Y
473	0111011001	2	1000100110	-2	Y
474	0111011010	2	1000100101	-2	Y
475	0111011011	4	1000100100	-4	Y
476	0111011100	2	1000100011	-2	Y
477	0111011101	4	1000100010	-4	Y
478	0111011110	4	1000100001	-4	Y
479	1001011100	0	0110100011	0	N
480	1011010010	0	0100101101	0	N
481	0111100001	0	1000011110	0	Y
482	0111100010	0	1000011101	0	Y
483	0111100011	2	1000011100	-2	Y
484	0111100100	0	1000011011	0	Y
485	0111100101	2	1000011010	-2	Y
486	0111100110	2	1000011001	-2	Y
487	0111100111	4	1000011000	-4	Y
488	0111101000	0	1000010111	0	Y
489	0111101001	2	1000010110	-2	Y
490	0111101010	2	1000010101	-2	Y
491	0111101011	4	1000010100	-4	Y
492	0111101100	2	1000010011	-2	Y
493	0111101101	4	1000010010	-4	Y
494	0111101110	4	1000010001	-4	Y
495	0111101111	6	1000010000	-6	Y
496	1011010100	0	0100101011	0	N
497	0111110001	2	1000001110	-2	Y
498	0111110010	2	1000001101	-2	Y

499	0111110011	4	1000001100	-4	Y
500	0111110100	2	1000001011	-2	Y
501	0111110101	4	1000001010	-4	Y
502	0111110110	4	1000001001	-4	Y
503	0111110111	6	1000001000	-6	Y
504	1000100111	0	0111011000	0	N
505	0111111001	4	1000000110	-4	Y
506	0111111010	4	1000000101	-4	Y
507	0111111011	6	1000000100	-6	Y
508	1000110011	0	0111001100	0	N
509	1000111010	0	0111000101	0	N
510	1000111001	0	0111000110	0	N
511	1001101100	0	0110010011	0	N

In Table 5, the 512 code words set forth in the second column from the left determine the positive disparity codebook of the Table 5 code to which the input symbols map. Each code word in the positive disparity codebook (sometimes referred to as the "positive" codebook) has the non-negative disparity indicated (in the third column from the left in Table 5). The complement of each code word of positive disparity codebook determines the code word of the negative disparity codebook to which the relevant input symbol maps. This determines the 512 code words of the negative disparity codebook (set forth in Table 5 in the fourth column from the left) to which the input symbols map. Each code word in the negative disparity codebook (sometimes referred to as the "negative" codebook) has the non-positive disparity indicated (in the second column from the right in Table 5).

The secondary mapping for the 9B/10B code of Table 5 determines those code words in each row of Table 5 in which there is an "N" symbol in the right column. (The primary mapping for this code determines those code words in each row of Table 4 in which there is a "Y" symbol in the right column).

The Table 5 code favors higher transition density over lower digital sum variation with the goal of providing better clock data recovery performance for transmission over short distances. The code space is defined as follows:

each code word having disparity 0 has a run of length three or less on either end, and includes no run of length greater than six away from its ends;

each code word having disparity 2, -2, 4, -4, 6, or -6 that has a run of zeroes on the left has a run of zeroes of length two or less on the left;

each code word having disparity 2, -2, 4, -4, 6, or -6 that has a run of zeroes on the right has a run of zeroes of length three or less on the right;

each code word having disparity 2, -2, 4, -4, 6, or -6 that has a run of ones on the left has a run of ones of length three or less on the left;

each code word having disparity 2, -2, 4, -4, 6, or -6 that has a run of ones on the right has a run of ones of length four or less on the right;

no code word having disparity 2, -2, 4, -4, 6, or -6 has a run of zeroes of length greater than six away from its ends;

no code word having disparity 2, -2, 4, -4, 6, or -6 has a run of ones of length greater than seven away from its ends;

no code word has disparity greater than 6 or less than -6; and

no code word has less than 3 transitions.

These rules select 513 code words out of the 1024 possible 10-bit code words.

The code set forth in Table 5 has a maximum run length of 7, a running digital sum variation of 20, an average of 5.29 transitions per code word (over all legal code pairs), and a normalized DC offset of 6.9. Of the 512 code words in the positive codebook, only 113 are not determined by the primary mapping.

In variations on the code set forth in Table 5, the positive and negative codebooks are not strictly complements of each other. Rather, the code words having nonzero disparity are identical to those of Table 5 (the code words of the negative codebook having nonzero disparity are complements of corresponding code words of the positive codebook) but the code words of the negative codebook that have zero disparity are identical to corresponding code words of the positive codebook. The code words having zero disparity can be either the zero-disparity code words of the positive codebook of Table 5 or the zero-disparity code words of the negative codebook of Table 5.

For both the Table 4 code and the Table 5 code, the same prefixes for denoting control/out-of-band characters are used. In particular, when current running disparity is < 0, the prefix is 0011111111. The prefix is 1100000000 when current running disparity is > 0. A comma or control code contains a 10-bit code following this prefix so that the total disparity across the 20 bits is 0 and so that it does not end with a run of length greater than 3. This gives 25 possible combinations for each prefix, i.e. 25 possible 20-bit out-of-band characters. If one allows the OOB characters to be longer than 20 bits, one can have more possible values.

Other embodiments of the invention employ other spectral coding approaches which reduce channel coding overhead. For example, bits could be inserted to force transitions, a polarity bit can be used to ensure DC balance, and additional transitions can be guaranteed by controlling the use of parity bits for error control coding or by forcing transitions in other back channel fields.

Inclusion of control bits (with application data) in predetermined slots of input words (e.g., inclusion of control bits as the least significant bits, or most significant bits, of input words whose other bits are application data, as described with reference to Fig. 2), encoding the input words to generate code words, and transmitting sequences of the code words indicative of cells in accordance with the invention provides additional link layer and higher layer functionality as described herein. Use of a low overhead block code (e.g., a 9-bit-to-10-bit code) to generate the code words, rather than a higher overhead block code (e.g., a conventional 8-bit-to-10-bit code), provides such link layer and higher layer functionality without reducing the effective bandwidth of the serial link over which the code words are transmitted.

The special characters (e.g., "idle" characters used for simplex or duplex link flow control, and "link training" characters) transmitted in accordance with the invention are preferably chosen to be easily recognizable and distinguishable from the code words indicative of cells that are also transmitted. Typically, only a small number of special characters are used. Preferably, the set of code words employed to encode cells and the special characters are chosen such that no special character can unintentionally occur in a sequence of code words indicative of a cell (i.e., no special character matches any of the code words, and no sequence of bits from any possible sequence of consecutively transmitted code words matches any of the special characters). This allows intentional transmission of any special character at any time (including by interrupting transmission of a cell to transmit the special character), and allows the circuitry employed for receiving and decoding code words to be configured (e.g., to include simple logic configured) to recognize each transmitted special character regardless of whether transmission of the special character has or has not interrupted transmission of a cell.

In a system having the OSI seven-layer (or TCP/IP) architecture, the link layer is responsible for point-to-point communication. Point-to-point communication can be subdivided into duplex (which herein denotes both full duplex and dual simplex) communication and simplex communication. In such systems, transmission in

accordance with the invention of code word sequences (indicative of cells) and special characters (that are distinguishable from the bit sequences that can occur in such code word sequences) allows transmitters and receivers to provide improved link layer functionality. We next describe examples of this improved link layer functionality, including examples of improved framing, simplex link flow control, simplex link error detection and correction, and duplex link flow control.

"Framing" denotes the process of determining the boundaries of blocks of data utilized by higher-layer protocols. At the physical layer, these blocks are referred to as symbols or characters. Examples of characters are the 10-bit code words described with reference to Fig. 2. At the link layer, the blocks whose boundaries are determined are referred to as cells or frames. Examples of frames are ethernet frames and the 144-bit cells described with reference to Fig. 2. In preferred embodiments of the invention, the link layer frames are cells consisting of a fixed, predetermined number of physical layer symbols (i.e., cells consisting of a fixed number of code words). Preferred embodiments of the inventive system, that include two communication endpoints (e.g., transceivers) and a serial link between them, use at least one special character (e.g., a "link training" character and typically also a "state exchange" character) to perform framing both at the physical layer and link layer. Such a system enters a training state at startup (power on) or after detection of an uncorrectable error. Typically in the training state, a first endpoint begins transmitting a special character or set of special characters (e.g., a link training character, or link training and state exchange characters) to the second endpoint. The second endpoint responds by transmitting a special character or set of special characters to the first endpoint, and one or more additional cycles of special character transmission between the endpoints can also occur. Once a specific pattern of special characters has been received at both endpoints, both endpoints exit the training state and enter a normal operating state. In the normal operating state, each endpoint can reliably determine the proper symbol and cell framing for the stream of code bits (indicative of cells) that it receives over the link. Several examples of a link training operation (which accomplishes framing both at the physical layer and link layer) are described herein.

A transmitter (e.g., circuit 32 of transmitter 10) can insert a special idle character, I, between valid code words (each indicative of contents of a cell) for plesiosynchronous communication. In response to an idle character, the receiver enters

a wait state and resumes processing of a sequence of code words in response to receiving the first valid code word after an idle character.

We next describe how simplex link flow control can be accomplished at the link level in accordance with the invention. In typical systems that embody the invention, transmitters and receivers operate in different clock domains. To ensure that a transmitter does not overrun a receiver's input buffer, a plesiosynchronous communication technique can be employed. Based on maximum allowable clock skew between transmitter and receiver, the transmitter inserts special characters (referred to herein as "idle" characters) between cells at appropriate intervals. A slow receiver can drop (ignore) the idle characters to catch up to a faster transmitter. For example, circuit 43, in an implementation of receiver 20 (of Fig. 1) that operates in response to a slower clock than does transmitter 10, is configured to drop the idle characters that it receives over channel 51 (thereby allowing the decoding circuitry within circuit 43 to stay caught up with transmitter 10). In the example, circuit 32 of transmitter 10 inserts the idle characters in the bit stream transmitted over channel 51 at appropriate intervals, and the decision as to when to transmit idle characters is made at the link layer (e.g., by circuits 32, 33, 34, and/or 35 in transmitter 10; not by circuitry 30).

We next describe how simplex link error detection can be accomplished at the link level in accordance with the invention. Error code bits (e.g., parity bits, or the CRC bits discussed with reference to Fig. 2) are generated for the entire amount of data to be transmitted in a cell (or a fixed number of cells), and the error control bits are encoded with the other bits (application and control bits) of the cell or cells. The transmitted code words (indicative of the cell or cells) are thus indicative of the error control bits. In link layer circuitry in the receiver, the error control bits are extracted from decoded versions of the code words and used to detect errors in the cell (or across the fixed number of cells). For example, the receiver can perform a cyclic redundancy check using the error control bits. The number of error control bits and cell coverage can be determined based on the error detection performance and latency requirements of the communication environment, as well as the allowable overhead. When a receiver detects an error, application-specific actions can be applied. In preferred embodiments which incorporate transport layer functionality (as described below), a low latency re-transmission of the cell(s) can be requested.

Simplex link error correction can also be accomplished at the link level in accordance with the invention. The error control bits described in the previous

paragraph can be used by link layer circuitry in the receiver to implement error correction instead of (or in addition to) error detection. The number of error control bits and cell coverage can be determined based on the error correction performance and latency requirements of the communication environment, as well as the allowable overhead. In preferred embodiments which incorporate transport layer functionality (as described below), re-transmission of a cell or cells will not be necessary when detected errors are corrected by link layer circuitry in the receiver.

We next describe how duplex link flow control can be accomplished at the link level in accordance with the invention. When an embodiment of the inventive system treats pairs of simplex channels (e.g., channels 51 and 52 of Fig. 1) as a single bidirectional link, the coordination between the channels is most efficiently supported by the line code. In preferred embodiments, the inventive system employs an implicit credit-based scheme to synchronize flow control between the two simplex channels. At startup, an initial credit allocation (e.g., four credits) is assigned to each endpoint. The amount of the initial credit allocation will depend on link speed, logic clock rate, cell length, and typically also other factors. For each cell transmitted by the endpoint, the allocation is decremented by one by link layer circuitry. For each cell received by the endpoint, the allocation is incremented by one by link layer circuitry.

In one class of embodiments, each endpoint transmits idle characters when its credit allocation is exhausted. This ensures that rate mismatches between the channels are normalized to the slower channel, and serves to minimize buffering required to allow re-transmission of cells when necessary (e.g., a two-credit allocation implies four cell buffers). Some method should be employed to ensure that the idle character-receiving endpoint will increment its credit allocation appropriately even when it is not receiving cells from the other endpoint. For example, the endpoint that transmits idle characters can transmit additional special characters ("credit-incrementing" characters Ci) with the idle characters to cause the receiving endpoint to increment its credit allocation in response to each credit-incrementing character (Ci). Just as in the case of link training in which multiple symbols are used (e.g., the training character T and state exchange characters Si, each of which typically includes a common preamble pattern useful for physical framing, and a discriminant pattern for distinguishing itself from the other characters), each idle character I and each credit-incrementing character Ci used for duplex flow control can have the same preamble pattern, and each credit-incrementing character can include a distinctive credit-incrementing value. In response

to each credit-incrementing value, the receiving endpoint increments its credit allocation by a predetermined amount.

For example, in an implementation of transmitter 10 (of Fig. 1), circuit 32 is configured to decrement a credit allocation by one whenever it transmits a cell on channel 51, and to increment the allocation by one whenever a control signal (transmitted to it by circuit 34 or 35) indicates that circuit 35 has received a cell (or circuit 34 or 35 has received a credit-incrementing character Ci) that has propagated to transmitter 10 over channel 52. When the allocation drops to zero, circuit 32 would insert one or more idle characters (and credit characters Ci) in the bit stream it transmits over channel 51. Circuit 43 of receiver 20 would be configured to drop the idle characters that it receives over channel 51, and to increment its credit allocation in response to each credit character Ci.

In another class of embodiments, duplex flow control is implemented as follows. An endpoint whose credit allocation has dropped to zero transmits one or more empty cells (rather than idle and credit-incrementing characters as in the embodiments described above) when its credit allocation is exhausted. Each empty cell includes one or more of the above-mentioned "Valid" bits, each such "Valid" bit being set to indicate that the cell include no valid application data. The receiving endpoint increments its credit allocation in response to each such empty cell, just as it does in response to a non-empty cell.

In a third class of embodiments, duplex flow control is implemented as follows. An endpoint transmits special flow control characters (XON and XOFF characters) when a rate mismatch occurs between it and another endpoint. The XON and XOFF characters would not be exposed to application layer circuitry as are the above-described FLOW bits. Rather, the XON and XOFF characters can be used to implement a TCP window style flow control, whereas the FLOW bits are used by the application to implement end-to-end flow control across potentially multiple hops. To accomplish duplex flow control using XON/XOFF characters, a transmitter sends cells at will during normal operation. If the receiver does not consume the cells fast enough (i.e., if the receiver's buffers fill up before application layer circuitry in the receiver drains them), then the receiver sends an XOFF character back to the transmitter and the receiver drops any subsequently received cells. When physical (or link) layer circuitry in the transmitter notices the XOFF character, it ceases normal cell transmission and instead sends idle characters or empty cells. Once the receiver's buffers have drained a

sufficient amount, the receiver sends an XON character to the transmitter. In response to the XON character, physical (or link) layer circuitry in the transmitter causes the transmitter to resume normal cell transmission. The XON character should include embedded state information (or be accompanied by state information) so that the transmitter knows at which cell to begin re-transmission. This can be accomplished with multiple XONi characters (each identifying a different cell as the first cell to be re-transmitted) or by sending a state exchange character ("XONSi") with the XON character. Note that if the XONSi characters are identical to state exchange characters ("Si") used in a link training context, then the state machine must include extra states to disambiguate between an error condition (in which the transmitter should enter a link training state) and receipt of an XONSi character with an XON character (in which case normal cell transmission should simply be re-enabled). Preferably, the XONSi characters are distinguishable from (i.e., are different characters than) any state exchange characters ("Si") used in a link training context. Each XONSi character can be sent multiple times to guard against bit errors.

We next describe an example of improved network layer functionality that is provided by some embodiments of the invention. The point-to-point communication facilitated by the link layer can be extended by including addressing support within the line code employed in accordance with the invention, to enable routing of cells (by network layer circuitry) to appropriate addresses in a network of interconnected endpoints. For example, a control bit (e.g., the XTND bit discussed with reference to Fig. 2) in a non-extended cell can enable an enhanced mode of operation in which an address is appended to a code word sequence indicative of the non-extended cell, to form an extended version of the non-extended cell. In other words, the control bit can indicate whether the cell containing it has an address extension. For example, in an implementation of receiver 20 of Fig. 1, de-packetizing circuit 45 (which is an element of the link layer circuitry of receiver 20) can identify an XTND bit in each sequence of decoded words (indicative of a cell) that it receives from circuit 44. Such an implementation of circuit 45 would assert to circuitry 40 a control signal indicative of the XTND bit's value, and would also assert to circuitry 40 the decoded data bits comprising each address extension. In response, network layer circuitry within circuitry 40 would route (e.g., to other endpoint devices, not shown in Fig. 1, of a network that includes receiver 20) cells (including application data and typically also control bits) that are received by circuitry 40 from circuit 45 in the manner determined

by the address extensions of the cells. When only point-to-point communication (e.g., between transmitter 10 and receiver 20) is desired, the XTND bit would be forced (e.g., by circuit 32 of an implementation of transmitter 10) to a value indicating that no cell has an address extension, transmitter 10 would transmit cells without address extensions, and receiver 20 would not operate to route cells to devices determined by address extensions. Even when only point-to-point communication is desired, inclusion of a control bit (e.g., an XTND = 0 bit) in each cell is the only added overhead resulting from configuration of the link layer circuitry in accordance with the invention to be capable of supporting the network layer function of routing cells to appropriate addresses in a network of interconnected endpoints.

In variations on the implementation described in the previous paragraph, at least one control bit in a predetermined position within each cell is used by a transmitter or receiver to enable another enhanced mode of operation (i.e., an enhanced mode of operation other than the routing of cells, by network layer circuitry, to appropriate addresses in a network of interconnected endpoints).

We next describe an example of improved transport layer functionality provided by some embodiments of the invention. The hallmark of the transport layer is its ability to provide sequenced, reliable delivery of user data across a connection (e.g. a bidirectional channel), including by handling all error control, ordering, and flow control issues. At least some of these functions can be implemented using a line code in accordance with the invention as follows. As previously described, duplex link flow control and link training can be implemented in accordance with the invention in a manner in which link layer circuitry in each endpoint (e.g., circuits 32 and 35 of transmitter 10 and circuits 42 and 45 of receiver 20 in Fig. 1) is configured such that each endpoint keeps a running count of the cells transmitted and received thereby. In each direction of communication, the sequence in which cells are transmitted is never re-ordered. At the end of a link training operation, or when normal cell transmission resumes after an interruption for the purpose of duplex link flow control, the transmitting endpoint begins to transmit cells beginning with the first cell that was not received by the receiving endpoint. Thus, transport layer functionality in both endpoints is enhanced in the sense that the transport layer protocol does not require support for handling the re-ordering of cells, and thus the transport layer circuitry can be implemented more simply than if it had to be capable of handling the re-ordering of cells.

Several embodiments have been described in which the inventive line code allows the transmitting endpoint to begin to transmit cells beginning with the first cell that was not received by the receiving endpoint, at the end of a link training operation or when normal cell transmission resumes after an interruption for the purpose of duplex link flow control. For example, if an uncorrectable error is detected in a cell, link re-training is initiated and the endpoint that detects the error can send a link training character (as described above) to force the other endpoint to enter a training phase. By the end of the training phase, each endpoint has sent at least one state exchange character (e.g., a version of the "Si" characters described above) to the other endpoint. Embedded within each state exchange character is the sequence number of the last cell received by the endpoint that sends the state exchange character. Alternatively, a sequence of the state exchange characters can be indicative of the sequence number of the last cell received by the endpoint that sends the state exchange character sequence (e.g., if each state exchange character in the sequence is indicative of a binary "1" or "0" and the sequence consists of N characters, the sequence number of the cell can be an N-bit binary number determined by the N-character sequence). At the end of the training phase, normal transmission resumes with the first cell that was not received. This is a version of a go-back-N ARQ scheme, and requires the link-layer circuitry within each endpoint to buffer a sufficient number of cells to allow for re-transmission of the cells when necessary. In typical implementations of the inventive system that include two endpoints configured for point-to-point communication with each other via a serial link, no more than four cells must be buffered in each endpoint. For example, in an implementation of receiver 20 (of Fig. 1), circuit 45 is configured to increment a sequence number whenever it receives a cell on channel 51, and during a training phase, circuit 42 operates to send a state exchange character over channel 52 that is indicative of the current sequence number (in response to a control signal indicative of the sequence number received from circuit 45). Circuit 32 of transmitter 10 stores in a buffer memory the four cells most recently transmitted thereby, and a sequence number of each cell. At the end of the training phase, circuit 32 resumes normal transmission starting with the first cell that was not received by receiver 20.

We next describe examples of improved application layer functionality provided by some embodiments of the invention. Application-specific protocols can be efficiently implemented by embedding control signals within the line code employed in accordance with the invention.

One such application-specific protocol is end-to-end flow control. While link level flow control ensures that transmitters and receivers will not overflow their buffers, applications may not be able to consume data at the line rate. One or more control bits (e.g., the above-discussed FLOW bit or bits) can be included in each cell and exposed to application layer circuitry in the endpoint that receives the cell, to allow application layer circuitry in both endpoints to maintain end-to-end flow control.

For example, in an implementation of the Fig. 1 system, circuitry 40 of receiver 20 provides (to packetizing circuit 41) control data (generated by application layer circuitry within circuitry 40) that determine the FLOW bit of each cell to be transmitted over channel 52. In response to each such cell, circuit 35 of transmitter 10 asserts a control signal indicative of the value of the FLOW bit to circuitry 30. Application layer circuitry within circuitry 30 responds to the control signal by causing transmitter 10 to enter either a "data transmitting" state in which it sends code words indicative of cells to receiver 20 over channel 51, or a state in which it suspends transmission of such code words to receiver 20 over channel 51.

In a variation on this example, each cell includes two or more FLOW bits. Where there are N blocks of application data per cell, each block having a different priority, there can be (N-1) FLOW bits per cell (one FLOW bit for each block of application data except the block having the highest priority, since flow control is typically not allowed at the highest priority level). In this case, transmitter 10 responds to each FLOW bit by sending cells that include or do not include application data of each relevant priority level. Typically, flow control at one priority level would affect flow control at each lower priority level.

In other variations, "M" FLOW bits (where $M > 1$) are evenly distributed in each cell, and each FLOW bit applies to all priority levels of data. This provides M granularity for controlling flow (e.g., the flow control state for the next cell transmitted from the far side is the last interpreted incoming flow control value) and can reduce flow control latency, reduce receiver buffering, and provide faster response time at the receiver. For example, if receiver 20 wishes to assert a FLOW bit having the value XOFF, but can include only one FLOW bit in each cell and has just started to serialize another FLOW bit in a cell, it would need to wait an entire cell time before it can insert the FLOW bit that indicates XOFF. If receiver 20 could instead include multiple FLOW bits in each cell, response time can be greatly reduced, which in turn reduces buffering requirements. If each cell includes two evenly spaced FLOW bits (each

applying to all priority levels of application data), no more than half a cell time would be wasted on either endpoint when the value of the FLOW bit is to be changed, which would reduce system buffering requirements by one cell.

In variations on the embodiments described in the three previous paragraphs, a special flow control character (chosen such that its bit pattern cannot unintentionally occur in a sequence of code words indicative of a cell) is transmitted (e.g., between cells) for use in application level end-to-end flow control, rather than a flow control bit (e.g., a FLOW bit) within a cell. However, transmission of a flow control bit within a cell for this purpose will typically have greater reliability (e.g., when the cell also includes CRC bits or other error control coding that covers the flow control bit as well as application data within the cell) without compromising (or significantly compromising) available data bandwidth.

Another application-specific protocol is out-of-band signaling. Applications typically incorporate a control/command stream and a data stream that are logically separate (with one stream having higher priority than the other). Similarly, some application data may be considered out-of-band or otherwise at higher priority than other application data. In accordance with the invention, for each block of application data in a cell, a command bit (e.g., the "OOB" bits described with reference to Fig. 2) is included within the cell to indicate the priority level of the data (e.g., to indicate whether the data are in-band or out-of-band), or simply to create a different logical channel (all having the same priority level) for each block of application data. The granularity of the application data within each cell (e.g., the number of separate blocks of the application data) is chosen based on expected demands. The priority-level-indicating bit is exposed to application layer circuitry in the endpoint that receives the cell, to allow the application layer circuitry to determine the priority level of each block of application data in the cell.

For example, in an implementation of the Fig. 1 system, circuitry 30 of transmitter 10 provides (to packetizing circuit 31) control data (generated by application layer circuitry within circuitry 30) that determine the priority level of each block of application data to be included in each cell to be transmitted over channel 51. In response to such control data, circuit 31 includes in the cell an OOB bit for each block of application data. After transmission of the cell, circuit 45 in receiver 20 asserts to circuitry 40 not only the application data, but also at least one control signal indicative of the value of each OOB bit. Application layer circuitry within circuitry 40

responds to the control signal(s) by determining the priority level for the relevant block of application data.

Inclusion in a cell of one binary priority-level-indicating bit for each block of application data in the cell implements two priority levels for the data. At least one additional binary priority-level-indicating bit for each block of application data would allow the application data to be categorized into more than two priority levels. A transmitter that embodies the invention can be implemented to transmit higher priority traffic before lower priority traffic, and a receiver that embodies the invention can be implemented to pass or process higher priority traffic before lower priority traffic. This is important because it is often necessary to enable control traffic to pass data traffic to avoid deadlocks, enable command pipelining, and efficiently utilize link bandwidth.

In a class of embodiments, the invention is a method of encoding data, including the steps of generating M-bit input words, where the input words are indicative of application data and control bits; and encoding the input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein $N > M$, the code word sequence is indicative of at least one cell of the input words, the cell includes at least some of the application data and at least two of the control bits, and said at least two of the control bits have multiple levels of communication protocol functionality. In some such embodiments, the block code is specified by a line code, the line code also specifies special characters, and the method also includes the step of generating encoded data such that the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence. Preferably, each cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit. In preferred embodiments, $N = M + 1$.

In some embodiments of the inventive system, the serial link between two endpoints includes a single simplex (or half duplex) channel, or a single duplex channel (e.g., a pair of simplex channels which are used as a single bidirectional link). However, in other embodiments of the inventive system, the serial link between two endpoints includes any number of channels. For example, if one endpoint includes N transmitters (which work together) and the other endpoint includes M receivers (which work together), the serial link between the endpoints can include a channel between each transmitter-receiver pair (e.g., the serial link can include six channels, when $N = 2$

and M = 3). If one endpoint has N transmitters and the other endpoint has M receivers (and N is not equal to M), then either all N transmitters or all M receivers cannot be connected simultaneously to the other endpoint. In some embodiments, one endpoint has N transmitters and M receivers. In some embodiments, one endpoint has N transmitters and the other endpoint has M transmitters. As a more specific example, the serial link of an embodiment of the inventive system could have groups of one downstream and three upstream channels together in a DRAM architecture (e.g., one write/command channel for transmitting encoded data to a DRAM and three read channels for receiving encoded data from the DRAM).

It should be appreciated that in a class of embodiments the invention provides a reliable link embedded within a line code, in the sense that it allows physical and link layer circuitry to provide the abstraction of a communication channel that provides sequenced, reliable delivery of application data streams. For example, a system that implements an embodiment in this class can employ a lossy serial interface, rather than a standard parallel interface that is assumed to be 100% reliable, to provide the reliable link. Error detection functionality and re-transmission at the physical and link layer can be efficiently incorporated within the line code to allow a system implementing the invention to be assumed to be 100% reliable. To facilitate the creation of command/response protocols on top of the reliable link, the line code can implement virtual channels (e.g., using OOB bits indicative of the virtual channels) in accordance with the invention to distinguish commands from data, and can also implement flow control in accordance with the invention. If NB/(N+1)B block coding is employed, all this enhanced functionality can be fully encapsulated within the physical and link layer with no more overhead than that of typical conventional line codes (e.g., conventional line codes using a conventional 8B/10B block code).

The term "includes" as used in the claims denotes "consists of or includes."

It should be understood that while certain forms of the present invention are illustrated and described herein, the invention is defined by the claims and is not to be limited to the specific embodiments described and shown.

CLAIMS

What is claimed is:

1. A communication system, including:

a first endpoint;

a second endpoint, including physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and

wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data to recover application data and control bits, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

2. The system of claim 1, wherein the line code specifies a block code and special characters, the first endpoint is configured to encode M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, where $N > M$, the code word sequence is indicative of at least one cell of the input words, and the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

3. The system of claim 2, wherein the physical and link layer circuitry is configured to distinguish each of the special characters of the encoded data from each bit sequence of the code word sequence.

4. The system of claim 2, wherein said at least one of the special characters is a link training character, and the physical and link layer circuitry is configured to perform physical level framing and link level framing in response to the link training character.

5. The system of claim 2, wherein said at least one of the special characters is a state exchange character.

6. The system of claim 2, wherein said at least one of the special characters is an idle character.

7. The system of claim 6, wherein the physical and link layer circuitry is configured to perform simplex link flow control by inserting idle characters between subsequences of the code word sequence, where each of the subsequences is indicative of a different cell of the input words.

8. The system of claim 2, wherein said at least one of the special characters is a flow control character.

9. The system of claim 2, wherein the input words of each said cell are indicative of application data and control bits, and the control bits have multiple levels of communication protocol functionality.

10. The system of claim 9, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

11. The system of claim 9, wherein each said cell has a predetermined structure such that position of each bit within the cell determines whether the bit is an application data bit or a control bit, and position of each control bit within the cell determines a function of said control bit.

12. The system of claim 9, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

13. The system of claim 9, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an

extension, and the physical and link layer circuitry is configured to assert to the higher level circuitry an extension-indicating control signal indicative of the value of the extension-indicating bit.

14. The system of claim 13, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

15. The system of claim 9, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the code word sequence is indicative of at least one cell of the input words, and the input words of each said cell are indicative of application data and control bits, and wherein the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint, and

wherein the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits therefrom, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry of the first endpoint, and the higher level circuitry of the first endpoint is configured to perform at least one higher level function in response to the at least one control signal.

16. The system of claim 15, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry of the first endpoint is configured to assert, to the higher level circuitry of the first endpoint, at least one flow control signal indicative of at least one said end-to-end flow control bit recovered by the physical and link layer circuitry of the first endpoint, and the higher level circuitry

of the first endpoint includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

17. The system of claim 15, wherein the additional encoded data are a sequence of the code words of the code word sequence and at least one of the special characters specified by the line code, the special characters include at least one link training character, and the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data and at least one said link training character in the additional encoded data.

18. The system of claim 17, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the special characters include at least one state exchange character indicative of a received cell sequence number,

the physical and link layer circuitry of the first endpoint is configured to resume transmission of the encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the second endpoint during the training phase, and

the physical and link layer circuitry of the second endpoint is configured to resume transmission of the additional encoded data over the second channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the first endpoint during the training phase.

19. The system of claim 15, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and

configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, and the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, and the special characters include an idle character, and

wherein the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform duplex link flow control in which the physical and link layer circuitry of the first endpoint inserts idle characters between subsequences of the code word sequence of the encoded data and the physical and link layer circuitry of the second endpoint inserts idle characters between subsequences of the code word sequence of the additional encoded data, where each of the subsequences is indicative of a different cell of the input words.

20. The system of claim 15, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, and the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint,

wherein at least one of the control bits is a data-validity indicating bit, each said cell is indicative of at least one said data-validity indicating bit, and

the physical and link layer circuitry of the first endpoint is configured to cause each cell of the encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data and the physical and link layer circuitry of the second endpoint is configured to cause each cell of the additional encoded data to include at least one said data-indicating bit indicating that the cell includes no valid application data, at times sufficient to accomplish duplex link flow control.

21. The system of claim 9, wherein the control bits of each said cell include error control bits, and the physical and link layer circuitry of the second endpoint is configured to perform at least one of error detection and error correction, on the

application data and at least some of the control bits recovered from the encoded data, using the error control bits.

22. The system of claim 2, wherein N = M +1.

23. A communication system, including:

a first endpoint;

a second endpoint; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to encode M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where N > M, the code word sequence is indicative of at least one cell of the input words, the input words of each said cell are indicative of application data and control bits, the control bits have multiple levels of communication protocol functionality, and the first endpoint is configured to transmit encoded data including the code words of the code word sequence over the link to the second endpoint.

24. The system of claim 23, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

25. The system of claim 23, wherein the block code is specified by a line code that also specifies special characters, the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, and none of the special characters of the encoded data matches a bit sequence of the code word sequence.

26. The system of claim 25, wherein said at least one of the special characters is a link training character.

27. The system of claim 25, wherein said at least one of the special characters is a state exchange character.

28. The system of claim 25, wherein said at least one of the special characters is an idle character.

29. The system of claim 25, wherein said at least one of the special characters is a flow control character.

30. The system of claim 25, wherein the link has at least a first channel and a second channel, the first endpoint includes physical and link layer circuitry coupled and configured to transmit the encoded data over the first channel to the second endpoint, the second endpoint includes physical and link layer circuitry coupled and configured to transmit additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the additional encoded data include N-bit code words of a second code word sequence, and at least one of the special characters is an idle character, and

the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform duplex link flow control in which the physical and link layer circuitry of the first endpoint inserts idle characters between code words of the encoded data and the physical and link layer circuitry of the second endpoint inserts idle characters between code words of the additional encoded data.

31. The system of claim 23, wherein each of the first endpoint and the second endpoint is a transceiver, and the second endpoint is configured to generate additional encoded data in response to input words in accordance with the line code and to transmit the encoded data over the link to the first endpoint.

32. The system of claim 23, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

33. The system of claim 23, wherein $N = M + 1$.

34. The system of claim 23, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a

priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

35. The system of claim 23, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension, the second endpoint includes physical and link layer circuitry coupled to the link and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry is configured to identify each extension-indicating bit indicated by the encoded data and assert to the higher level circuitry an extension-indicating control signal indicative of the value of each said extension-indicating bit.

36. The system of claim 23, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry of the second endpoint includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

37. The system of claim 23, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the code word sequence is indicative of at least one cell of the input words, and the input words of each said cell are indicative of application data and control bits, and wherein the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint, and

wherein the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits therefrom, to perform at least one link level function in response to at least one of the control bits, and to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry of the first endpoint, and the

higher level circuitry of the first endpoint is configured to perform at least one higher level function in response to the at least one control signal.

38. The system of claim 37, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry of the first endpoint is configured to assert, to the higher level circuitry of the first endpoint, at least one flow control signal indicative of at least one said end-to-end flow control bit recovered by the physical and link layer circuitry of the first endpoint, and the higher level circuitry of the first endpoint includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

39. The system of claim 23, wherein the link has at least a first channel and a second channel, the first endpoint includes physical and link layer circuitry coupled and configured to transmit the encoded data over the first channel, the second endpoint includes physical and link layer circuitry coupled and configured to transmit additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the additional encoded data include N-bit code words of a second code word sequence, the second code word sequence is indicative of at least one cell of M-bit input words, at least one of the control bits is a data-validity indicating bit, each said cell is indicative of at least one said data-validity indicating bit, and

the physical and link layer circuitry of the first endpoint is configured to cause each cell of the encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data and the physical and link layer circuitry of the second endpoint is configured to cause each cell of the additional encoded data to include at least one said data-validity indicating bit indicating that the cell includes no valid application data, at times sufficient to accomplish duplex link flow control.

40. The system of claim 23, wherein the control bits of each said cell include error control bits, the second endpoint includes physical and link layer circuitry coupled to the link and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry is configured is configured to perform at least one of error detection and error correction, on the application data and at least some of the control bits recovered from the encoded data, using the error control bits.

41. A communication system, including:

a first endpoint;

a second endpoint; and

a serial link between the first endpoint and the second endpoint, wherein the first endpoint is configured to generate encoded data, including by encoding M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein N > M, the input words are indicative of application data and control bits, the code word sequence is indicative of at least one cell of the input words, the cell includes at least one block of the application data and at least one of the control bits, the block code is specified by a line code that also specifies special characters, the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, and the first endpoint is configured to transmit the encoded data over the link to the second endpoint, wherein the control bits indicated by the encoded data, with said at least one of the special characters of the encoded data, have multiple levels of communication protocol functionality.

42. The system of claim 41, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

43. The system of claim 41, wherein said at least one of the special characters is a link training character.

44. The system of claim 41, wherein said at least one of the special characters is a state exchange character.

45. The system of claim 41, wherein said at least one of the special characters is an idle character.

46. The system of claim 41, wherein said at least one of the special characters is a flow control character.

47. The system of claim 41, wherein each of the first endpoint and the second endpoint is a transceiver, and the second endpoint is configured to generate additional

encoded data in response to input words in accordance with the line code and to transmit the additional encoded data over the link to the first endpoint.

48. The system of claim 41, wherein each said cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

49. The system of claim 41, wherein N = M +1.

50. The system of claim 41, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

51. The system of claim 41, wherein each of the first endpoint and the second endpoint is a transceiver, the second endpoint is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, the input words are indicative of application data and control bits, the code word sequence is indicative of at least one cell of the input words, each said cell includes at least one block of the application data and at least one of the control bits, the additional encoded data are a sequence of the code words of the code word sequence and at least one of the special characters, the second endpoint is configured to transmit the additional encoded data over the link to the first endpoint,

the first endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry of the first endpoint is coupled to the link and configured to decode the additional encoded data transmitted by the second endpoint to recover application data and control bits therefrom, and

the second endpoint includes physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry, and the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the

encoded data transmitted by the first endpoint to recover application data and control bits therefrom,

wherein the special characters include at least one link training character, and the physical and link layer circuitry of the first endpoint and the physical and link layer circuitry of the second endpoint are configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data and at least one said link training character in the additional encoded data.

52. The system of claim 51, wherein the link has at least a first channel and a second channel, the physical and link layer circuitry of the first endpoint is coupled and configured to transmit the encoded data over the first channel to the physical and link layer circuitry of the second endpoint, the physical and link layer circuitry of the second endpoint is coupled and configured to transmit the additional encoded data over the second channel to the physical and link layer circuitry of the first endpoint, the special characters include at least one state exchange character indicative of a received cell sequence number,

the physical and link layer circuitry of the first endpoint is configured to resume transmission of the encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the second endpoint during the training phase, and

the physical and link layer circuitry of the second endpoint is configured to resume transmission of the additional encoded data over the second channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received from the first endpoint during the training phase.

53. A receiver for receiving encoded data that have propagated over a serial link, the encoded data having been generated in accordance with a line code, said receiver including:

physical and link layer circuitry, coupled and configured to receive and decode the encoded data to recover application data and control bits, to perform at least one link level function in response to at least one of the control bits; and

higher level circuitry coupled to the physical and link layer circuitry, wherein the physical and link layer circuitry is coupled and configured to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

54. The receiver of claim 53, wherein the line code specifies a block code and special characters, the encoded data are a sequence of at least one of the special characters and N-bit code words of a code word sequence, where each of the code words has been generated by encoding an M-bit input word in accordance with the block code, wherein N > M, the code word sequence is indicative of at least one cell of the input words, and the physical and link layer circuitry is configured to distinguish each of the special characters of the encoded data from each bit sequence of the code word sequence.

55. The receiver of claim 54, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension, and the physical and link layer circuitry is configured to assert to the higher level circuitry an extension-indicating control signal indicative of the value of the extension-indicating bit.

56. The receiver of claim 55, wherein at least one said cell also includes an address extension, the value of the extension-indicating bit in said cell indicates that said cell includes the address extension, and the higher level circuitry includes network layer circuitry configured to perform at least one network level function in response to the extension-indicating control signal.

57. The receiver of claim 54, wherein the control bits of each said cell include an end-to-end flow control bit, the physical and link layer circuitry is configured to assert to the higher level circuitry at least one flow control signal indicative of at least

one said end-to-end flow control bit recovered by the physical and link layer circuitry, and the higher level circuitry includes application layer circuitry configured to perform at least one flow control operation in response to the at least one flow control signal.

58. The receiver of claim 54, wherein the special characters include at least one link training character, and the physical and link layer circuitry is configured to perform physical level and link level framing during a training phase in response to at least one said link training character in the encoded data.

59. The receiver of claim 54, wherein the control bits of each said cell include error control bits, and the physical and link layer circuitry is configured to perform at least one of error detection and error correction, on the application data and at least some of the control bits recovered from the encoded data, using the error control bits.

60. The receiver of claim 54, wherein the special characters include at least one flow control character.

61. The receiver of claim 53, wherein the receiver is a transceiver, the transceiver is configured to generate additional encoded data in accordance with the line code including by encoding M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where $N > M$, the code word sequence is indicative of at least one cell of the input words, the input words are indicative of application data and control bits, each said cell includes at least one block of the application data and at least one of the control bits, and the transceiver is configured to transmit the additional encoded data over the link,

wherein the line code also specifies special characters, the additional encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

62. The receiver of claim 61, wherein said at least one of the special characters is an idle character, and the physical and link layer circuitry is configured to perform link flow control by inserting idle characters between subsequences of the code word sequence of the additional encoded data, where each of the subsequences is indicative of a different cell of the input words.

63. The receiver of claim 61, wherein each cell of the code word sequence of the additional encoded data has a predetermined structure such that position of each bit within the cell determines whether the bit is an application data bit or a control bit, and position of each control bit within the cell determines a function of said control bit.

64. The receiver of claim 61, wherein each cell of the code word sequence of the additional encoded data includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

65. The receiver of claim 61, wherein the special characters include at least one link training character, the physical and link layer circuitry is configured to cease transmission of the additional encoded data and enter a training phase in response to at least one said link training character in the encoded data, and the physical and link layer circuitry is configured to perform physical level and link level framing during the training phase.

66. The receiver of claim 65, wherein the special characters include at least one state exchange character indicative of a received cell sequence number, and the physical and link layer circuitry is configured to resume transmission of the additional encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by the received cell sequence number indicated by at least one said state exchange character received over the link during the training phase.

67. The receiver of claim 65, wherein the physical and link layer circuitry is configured to resume transmission of the additional encoded data over the first channel after the training phase by transmitting a sequence of the code words indicative of a cell whose sequence number is determined by a cell sequence number indicated by data received over the link during the training phase.

68. A transmitter including physical and link layer circuitry, wherein the physical and link layer circuitry include:

packetizing circuitry configured to generate M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding and transmission circuitry coupled to the packetizing circuitry and configured to encode the input words in accordance with a block code to generate a code word sequence of N-bit code words, where N > M, the code word sequence is indicative of at least one cell of the input words, the cell includes at least two of the control bits, and said at least two of the control bits have multiple levels of communication protocol functionality, wherein the encoding and transmission circuitry is configured to be coupled to a serial link and to transmit encoded data over the serial link, said encoded data including the code words of the code word sequence.

69. The transmitter of claim 68, wherein each of the input words is indicative of at least some of the application data and at least one of the control bits.

70. The transmitter of claim 68, wherein the block code is specified by a line code, the line code also specifies special characters, and the encoding and transmission circuitry is configured to generate the encoded data such that said encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

71. The transmitter of claim 70, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

72. The transmitter of claim 70, wherein said at least one of the special characters is a link training character.

73. The transmitter of claim 70, wherein said at least one of the special characters is a state exchange character.

74. The transmitter of claim 70, wherein said at least one of the special characters is an idle character.

75. The transmitter of claim 70, wherein said at least one of the special characters is a flow control character.

76. The transmitter of claim 68, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

77. The transmitter of claim 68, wherein N = M +1.

78. The transmitter of claim 68, wherein at least one of the control bits of each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

79. The transmitter of claim 68, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension.

80. The transmitter of claim 79, wherein at least one said cell also includes an address extension, and the value of the extension-indicating bit in said cell indicates that said cell includes the address extension.

81. The transmitter of claim 68, wherein the control bits of each said cell include an end-to-end flow control bit.

82. The transmitter of claim 68, wherein the control bits of each said cell include error control bits.

83. The transmitter of claim 68, wherein the transmitter is a transceiver and the transmitter also includes:

higher level circuitry coupled to the physical and link layer circuitry, and wherein the physical and link layer circuitry also includes:

receiving and decoding circuitry configured to be coupled to the serial link and configured to receive and decode additional encoded data that have been generated in

accordance with the line code and propagated over the serial link, thereby recovering application data and control bits from the additional encoded data, wherein the receiving and decoding circuitry is coupled and configured to perform at least one link level function in response to at least one of the control bits recovered from the additional encoded data, and to assert at least one control signal indicative of at least another one of the control bits recovered from the additional encoded data to the higher level circuitry, wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.

84. A method of encoding data, including the steps of:

generating M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding the input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein N > M, the code word sequence is indicative of at least one cell of the input words, the cell includes at least some of the application data and at least two of the control bits, and said at least two of the control bits have multiple levels of communication protocol functionality.

85. The method of claim 84, wherein the block code is specified by a line code, the line code also specifies special characters, said method also including the step of:

generating encoded data such that the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.

86. The method of claim 85, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.

87. The method of claim 85, wherein said at least one of the special characters is a link training character.

88. The method of claim 85, wherein said at least one of the special characters is a state exchange character.

89. The method of claim 85, wherein said at least one of the special characters is an idle character.

90. The method of claim 84, also including the step of transmitting the encoded data over a serial link.

91. The method of claim 84, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

92. The method of claim 84, wherein N = M +1.

93. The method of claim 84, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

94. The method of claim 84, wherein each said cell includes a base portion, the control bits of the cell include an extension-indicating bit in the base portion, the extension-indicating bit has a value indicative of whether the cell also includes an extension.

95. The method of claim 84, wherein at least one said cell also includes an address extension, and the value of the extension-indicating bit in said cell indicates that said cell includes the address extension.

96. The method of claim 84, wherein the control bits of each said cell include an end-to-end flow control bit.

97. The method of claim 84, wherein the control bits of each said cell include error control bits.

98. The method of claim 84, wherein the code words of each said cell belong to a virtual control channel, each said cell includes at least one block of the application data, and each said block belongs to different virtual data channel.

99. The method of claim 84, wherein the levels of communication protocol functionality include at least one level of communication protocol functionality higher than link level functionality.

100. A method for encoding data, including the steps of:

generating M-bit input words, wherein the input words are indicative of application data and control bits; and

encoding the input words in accordance with a block code to generate a code word sequence of N-bit code words, wherein N > M, the code word sequence is indicative of at least one cell of the input words, the cell includes at least some of the application data and at least one of the control bits, and the block code is specified by a line code that also specifies special characters; and

generating encoded data, such that the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence, wherein the control bits indicated by the encoded data, with said at least one of the special characters of the encoded data, have multiple levels of communication protocol functionality.

101. The method of claim 100, wherein said at least one of the special characters is a link training character.

102. The method of claim 100, wherein said at least one of the special characters is a state exchange character.

103. The method of claim 100, wherein said at least one of the special characters is an idle character.

104. The method of claim 100, wherein said at least one of the special characters is a flow control character.

105. The method of claim 100, wherein the cell has a predetermined structure such that the position of a bit within the cell determines whether the bit is an

application data bit or a control bit, and the position of each control bit within the cell determines a function of said control bit.

106. The method of claim 100, wherein N = M +1.

107. The method of claim 100, wherein each said cell includes at least one block of the application data, and the control bits of each said cell include at least one of a priority-level-indicating bit, and a virtual-channel-identifying bit, for each said block of application data.

108. The method of claim 100, wherein the control bits of each said cell include an end-to-end flow control bit.

109. The method of claim 100, wherein the levels of communication protocol functionality include at least one level of communication protocol functionality higher than link level functionality.

ABSTRACT OF THE DISCLOSURE

A communication system including two endpoints (transceivers or a transmitter and receiver) and a serial link between them. At least one endpoint is configured to generate encoded data in accordance with a line code and to transmit the encoded data over the link. The line code specifies a block code for encoding cells of application data and control bits, and typically also special characters that do not match bit sequences of encoded cells. Other aspects of the invention are methods for generating (and endpoint devices configured to generate and transmit, or receive and process) such encoded data, and methods for performing functions of multiple layers of a communication protocol in response to such encoded data. In accordance with the invention, multiple levels of communication protocol functionality can be efficiently incorporated within a line code.

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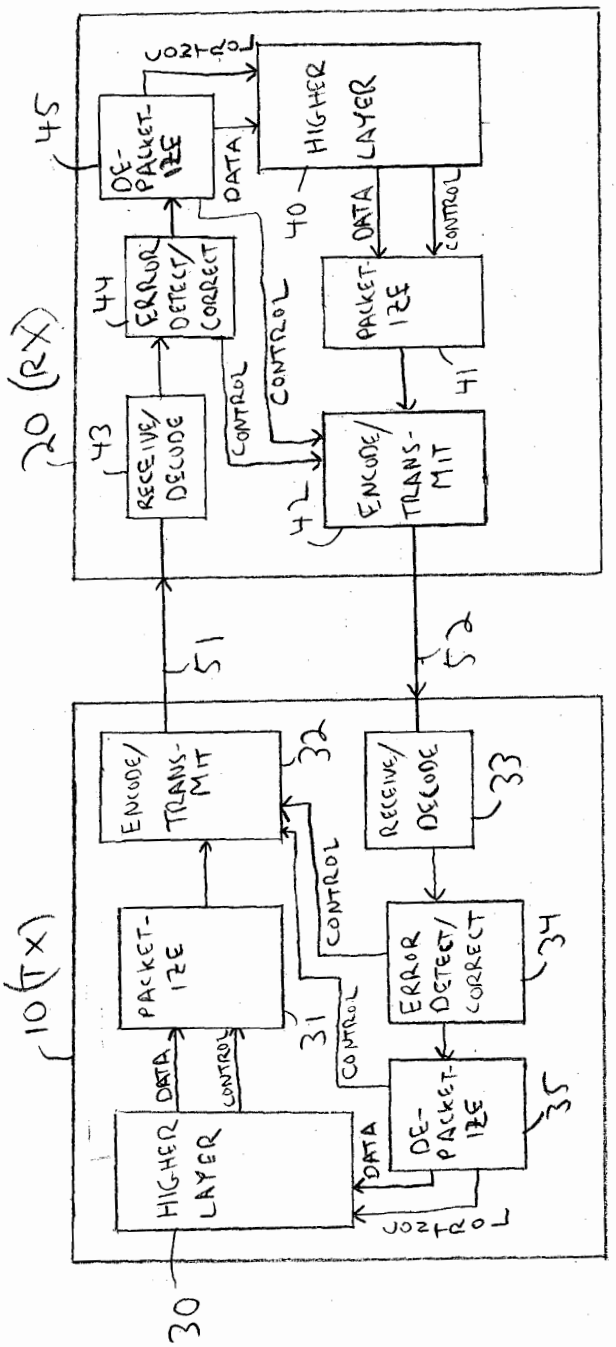


FIG. 1

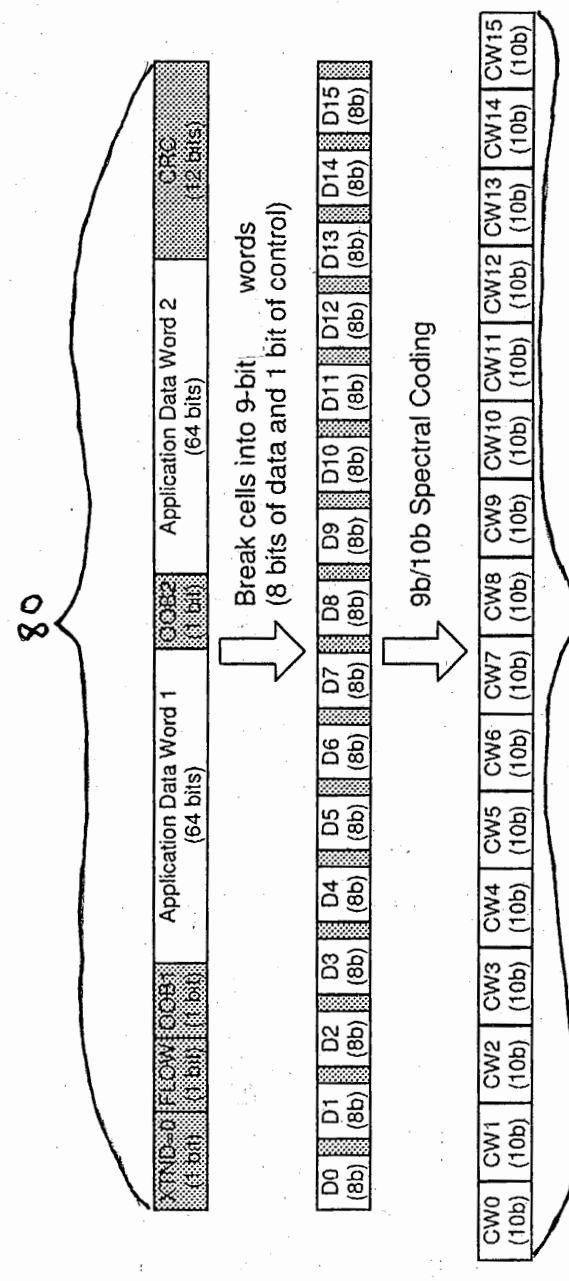

80
XTND=0 (1 bit)
FLOW (1 bit)
OOB3 (1 bit)
Application Data Word 1 (64 bits)
OOB2 (1 bit)
Application Data Word 2 (64 bits)
CRC (12 bits)
Break cells into 9-bit words
(8 bits of data and 1 bit of control)
D0 (8b)
D1 (8b)
D2 (8b)
D3 (8b)
D4 (8b)
D5 (8b)
D6 (8b)
D7 (8b)
D8 (8b)
D9 (8b)
D10 (8b)
D11 (8b)
D12 (8b)
D13 (8b)
D14 (8b)
D15 (8b)
9b/10b Spectral Coding
CW0 (10b)
CW1 (10b)
CW2 (10b)
CW3 (10b)
CW4 (10b)
CW5 (10b)
CW6 (10b)
CW7 (10b)
CW8 (10b)
CW9 (10b)
CW10 (10b)
CW11 (10b)
CW12 (10b)
CW13 (10b)
CW14 (10b)
CW15 (10b)
81

FIG. 2

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Express Mail Number EV 322540235 US

Atty Docket No. SII-3000 [SIMG0158]

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES

the specification of which (check one) X is attached hereto or __ was filed on __ as Application No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed Yes	No
Number	Country	Day/Month/Year Filed	___	___
Number	Country	Day/Month/Year Filed	___	___

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status: Patented, Pending, Abandoned
Application Number	Filing Date	Status: Patented, Pending, Abandoned

IPR2024-001429
HP – EX1002, Page 347 of 357

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first joint inventor, if any, BRIAN K. SCHMIDT

Inventor's signature Brian K. Schmidt 6/11/03
Date

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Citizenship USA

Post Office Address ~~247 Andsbury Avenue, Mountain View, California 94043~~ Apt D

Full name of second joint inventor, if any, JAMES G. HANKO

Inventor's signature James G. Hanko 6/11/2003
Date

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Citizenship USA

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Full name of third joint inventor, if any, J. DUANE NORTHCUTT

Inventor's signature 11 Jun 03
Date

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Citizenship USA

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Inventor's signature 6/11/03
Date

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Citizenship USA

Post Office Address ~~274 Andsbury Avenue, Mountain View, California 94043~~ 1009 Almanor Ave, Menlo Park CA 94025 CATR

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/16/2003 AADOF01 00000004 10459989

01 FC:1001	750.00	OP
02 FC:1201	336.00	OP
03 FC:1202	1602.00	OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

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PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: S11 - 3000

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	109	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	109 minus 20=	* 89
INDEPENDENT CLAIMS	7 minus 3 =	* 4
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	1602
X42=		OR	X84=	336
+140=		OR	+280=	
TOTAL		OR	TOTAL	2688

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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CLAIMS ONLY

SERIAL NO. | FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT	
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TOTAL DEP.	102					
TOTAL CLAIMS	109					

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TOTAL CLAIMS						

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CLAIMS ONLY

SERIAL | FILING DATE

APPLICANT(S)

CLAIMS

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TOTAL DEP.						
TOTAL CLAIMS						

PTO-2202 (Replaces ...)(11-97)

#2

Express Mail Number EV 322540235 US PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

BRIAN K. SCHMIDT, et al.

Application No. NEW

Filed: Herewith

For: **METHOD AND SYSTEM FOR ENCAPSULATION OF MULTIPLE LEVELS OF COMMUNICATION PROTOCOL FUNCTIONALITY WITHIN LINE CODES**

Group Art Unit: Unknown

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT

400 Montgomery Street
Suite 1110
San Francisco, CA 94104
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16235 U.S. PTO 10/459989 06/12/03

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants submit herewith patents, publications or other information [attached hereto and listed on the attached Form PTO-1449 (modified)] of which they are aware, which they believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

(a) [X] accompanies the new patent application submitted herewith. 37 CFR § 1.97(a).

(b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.

(c) [] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) [] is filed after the first office action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned, prior to the mailing date of either a final rejection or a notice of allowance, whichever occurs first, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) **or** a certification as specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and the Issue Fee has not been paid, and is accompanied by the fee ($130) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

(f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

(g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publication(s) is set forth on the attached Form PTO-1449 (Modified).

A copy of the items on PTO-1449 (Modified) is supplied herewith:

(h) [X] each (i) [] none (j) [] only those listed below:

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they were previously cited by or submitted to the Office in a prior application

no. , filed and relied upon in this application for an earlier filing date under 35 U.S.C. § 120.

A concise explanation of relevance of the items listed on form PTO-1449 (Modified) is:

(k) [X] not given

(l) [] given for each listed item

(m) [] given for only non-English language listed item(s) [Required]

(n) [] is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references [copy attached].

The Examiner is reminded that a "concise explanation of the relevance" of the submitted items "may be nothing more than identification of the particular figure or paragraph of the patent or publication which has some relation to the claimed invention," MPEP § 609.

While the information and references disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the listed references.

[] The Commissioner is hereby authorized to charge our Deposit Account No. **50-1697** for any fees required in connection with the filing of this Information Disclosure Statement. **A duplicate copy of this Notice is enclosed for this purpose.**

Respectfully submitted,

Dated: 6/12/03 By Alfred A. Equitz

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Registration No. 30,922
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Our File: SII-3000 [SIMG0158]

FORM PTO-1449 (Modified) U.S Dept. of Commerce (Rev. 7-80) Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Atty Docket No. SII-3000 [SIMG0158]	Appln. No. NEW
	Applicant(s) BRIAN K. SCHMIDT, et al.	
	Filing Date Herewith	Group Unknown

16235 U.S. PTO 10/459989 06/12/03

U.S. PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date
	AA	4,486,739	12/04/84	FRANASZEK et al.	340	347	06/30/82
	AB	5,144,304	09/01/92	McMAHON et al.	341	58	09/10/91
	AC	5,740,186	04/14/98	WIDMER	371	37.1	06/13/96
	AD	6,198,413 B1	03/06/01	WIDMER	341	59	07/01/99
	AE						

FOREIGN PATENT DOCUMENTS

*Examiner Initials		Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO
	AF							

OTHER DOCUMENTS

	AG	Widmer, Albert X., *"Partitioned DC-Balanced (0,6) 16B/18B Transmission Code"*, downloaded from the Internet on December 16, 2002 from http://www.grouper.ieee.org/groups/802/3/10G_study/public/july99/widmer_2_0799.pdf, cover sheet and pages 1-8.
	AH	Zhou, Tao, *"ISO/OSI, IEE 82.02, and TCP/IP, InstantDoc #22"*, dated May 1997, downloaded from the Internet on May 21, 2003 from http://www.winnetmag.com/Articles/Print.cfm?ArticleID=22, two pages.
	AI	

Examiner	Date Considered

* Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.