

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HP INC., DELL TECHNOLOGIES INC., DELL INC., AND
LENOVO (UNITED STATES) INC.,

Petitioners,

v.

UNIVERSAL CONNECTIVITY TECHNOLOGIES INC.,

Patent Owner.

Case IPR2024-01429
U.S. Patent No. 7,187,307

**PATENT OWNER'S PRELIMINARY RESPONSE
TO THE PETITION**

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Exhibit No.	Description
2001	Declaration of Dr. William H. Mangione-Smith In Support of Patent Owner’s Preliminary Response
2002	Docket Control Order, <i>Universal Connectivity Technologies Inc. v. Lenovo Group Limited</i> , No. 2:23-cv-00449-JRG (E.D. Tex. June 12, 2024)
2003	Civil Minutes, <i>Universal Connectivity Technologies Inc. v. HP Inc.</i> , No. 4:24-cv-04097-YGR (N.D. Cal. Nov. 4, 2024)
2004	Order, <i>Universal Connectivity Technologies Inc. v. Dell Inc.</i> , No. 1:23-cv-01506-RP (W.D. Tex. Dec. 12, 2024)
2005	Defendant’s Invalidity and Eligibility Contentions, <i>Universal Connectivity Technologies Inc. v. Lenovo Group Limited</i> , No. 2:23-cv-00449-JRG (E.D. Tex. July 24, 2024)
2006	Defendants Dell Technologies Inc. and Dell Inc.’s Preliminary Invalidity Contentions, <i>Universal Connectivity Technologies Inc. v. Dell Inc.</i> , No. 1:23-cv-01506-RP (W.D. Tex. July 24, 2024)
2007	HP’s Invalidity Contentions, <i>Universal Connectivity Technologies Inc. v. HP Inc.</i> , No. 4:24-cv-04097-YGR (N.D. Cal. Dec. 5, 2024)
2008	U.S. District Courts—Federal Court Management Statistics—Profiles—During the 12-Month Periods Ending September 30, 2019 through 2024
2009	Memorandum Opinion and Order, <i>Universal Connectivity Technologies Inc. v. Lenovo Group Limited</i> , No. 2:23-cv-00449-JRG (E.D. Tex. Oct. 17, 2024)
2010	Order, <i>Universal Connectivity Technologies Inc. v. Lenovo Group Limited</i> , No. 2:23-cv-00449-JRG (E.D. Tex. Oct. 2, 2024)

I. INTRODUCTION

Petitioners have failed to show a reasonable likelihood of success in demonstrating that any of the challenged claims of U.S. Patent Number 7,187,307 are anticipated or obvious over the cited prior art. As an initial matter, the Board should exercise its discretion to deny institution under *Fintiv*. No stay has been requested in the underlying Eastern District of Texas litigation (the “LGL Case”) and trial is set to begin in early November 2025—nearly five months before the Board will enter its final written decision. Petitioners will have their day in court to make these same invalidity arguments to the jury. To conserve time and resources, the Board should exercise its discretion and deny institution under *Fintiv*.

In the alternative, the Board should deny institution on the merits because the Petitioners have not demonstrated a reasonable likelihood that they will prevail with respect to at least one of the claims challenged in the Petition. The Petition relies on two prior art references—“Shin” (EX1004 – all Grounds) and “Yusairi” (EX1005 – Ground 3 only). Neither Shin alone (Grounds 1 and 2) nor Yusairi in view of Shin (Ground 3) meet all the limitations of the challenged claims. In particular, neither

reference teaches (1) encoding *both* application data *and* control bits together to generate encoded data or (2) decoding encoded data to recover *both* application data *and* control bits as required by the independent challenged claims. Accordingly, the Board should deny institution of the '307 Petition.

II. OVERVIEW

A. The '307 Patent

The '307 patent describes a communication system with a serial link between two endpoints, such as a transmitter and a receiver, wherein the transmitter portion includes higher layer, packetizing and encoding/transmitting circuitry and the receiver portion includes receiving/decoding, error detecting and depacketizing circuitry. *See* EX1001, Fig. 1, 9:56-10:45. These aspects of the invention are depicted in exemplary Figure 1:

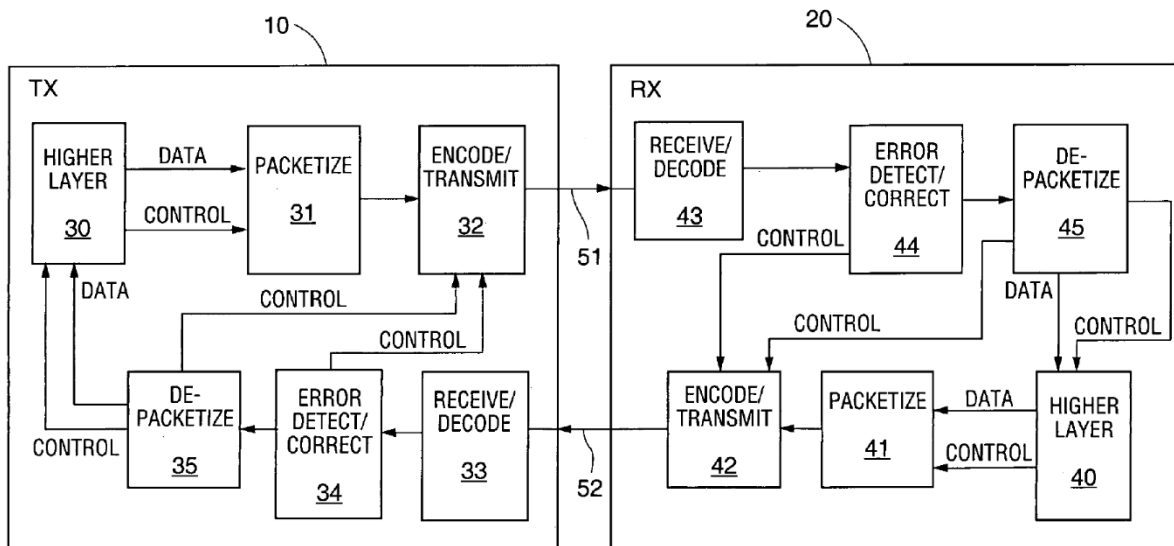


FIG. 1

EX1001, Fig. 1; EX2001 at ¶¶19-22. The packetizing circuitry at the transmitter generates sequences of input words indicative of application data and control bits. EX 1001, Figs 1 and 2, 10:20-39, 10:46-49; EX2001 at ¶22. The encoding circuitry at the transmitter encodes the input words into a sequence of code words according to a block code specified by a line code. EX 1001, Fig. 2, 11:45-47, 11:66-12:2; EX2001 at ¶22. The line code also specifies certain special characters which are distinguished from the code words. EX1001, 10: 46-51; EX2001 at ¶22. These special characters are also transmitted over the link, but they are not encoded with the codewords. EX2001 at ¶22.

Once the codewords are generated and combined with the special characters, the entire sequence is transmitted to the receiver. EX1001, Fig. 1, 5:15-28, 10:46-62; EX2001 at ¶23. Receiving/decoding circuitry receives the sequence, recognizing and separating the special characters and decoding the codewords to generate a stream of decoded words which are the original input words. EX1001, Figs 1 and 2, 13:37-41; *see also id.* at 10:62-11:4; EX2001 at ¶23. Depacketizing circuitry then determines which of the input words are application data and which are control bits. EX2001 at ¶23. The control bits are then sent to higher layer circuitry for processing. EX1001, 13:48-56; EX2001 at ¶24.

“The control bits in each cell typically have multiple levels of communication protocol functionality.” EX1001 at 4:66-5:1; EX2001 at ¶24. “Link layer circuitry in the receiver recognizes the cells in response to the M-bit decoded words..., performs link level functions in responses to appropriate ones of the controls bits, and asserts the decoded application data bits and appropriate ones of the decoded control bits to higher-level circuitry (circuitry that operates at least one level of communication protocol functionality higher than the link level).” EX1001 at 5:1-10; EX2001 at ¶24. “The decoded control bits are used by

the higher-level circuitry (which can be network layer circuitry and/or application layer circuitry, for example) to implement communication protocol functions at least one level higher than the link level.” EX1001 at 5:10-14; EX2001 at ¶24.

B. Claim Construction

For purposes of *inter partes* review, disputed claim terms are construed to give them “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *See* 83 Fed. Reg. 51341 (Oct. 11, 2018) (adopting the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005)). The proper construction is considered in the context of, and must be consistent with, the specification—and the claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *See, e.g., Phillips*, 415 F.3d at 1313.

Petitioners have proposed that no terms require construction. At this time, Patent Owner submits that the Board need not construe any claim terms in determining whether or not to institute *inter partes* review.

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art of the subject matter of the '307 patent would have the equivalent of a bachelor's degree in electrical engineering, computer engineering, computer science, or equivalent training and three years of work experience with data communications systems or interfaces, including at least some experience with serial or display data communications systems or interfaces. EX2001 at ¶15. Additional education may compensate for lesser work experience, and vice versa. *Id.*

D. Prior Art

1. Shin (EX1004)

Petitioners rely on Shin (EX1004) for all three presented Grounds. Shin is a U.S. Patent Application that was filed on November 7, 2001 and published on October 31, 2002 under Publication No. 2002/0159450. Shin is titled "Method and System for Asymmetric Packet Ordering Between Communications Devices." EX1004; EX2001 at ¶25.

Shin describes "[a] serial communications architecture for communicating between hosts and data store devices." EX1004 at Abstract; EX2001 at ¶26. Shin's architecture is depicted in Figure 1

which shows hosts [110] interconnected with data store devices [120] via a switching network [130]. EX1004 at Fig. 1. Each of the hosts, data store devices, and switching network include a transport layer, a link layer, and a physical layer. *Id.*

“The link layer encodes the codes to be transmitted via its communications link into symbols and decodes symbols received via its communications link into codes. The link layer receives codes to be transmitted from the transport layer, encodes those codes into symbols, and provides those symbols to the physical layer.” EX1004 at [0077]; EX2001 at ¶27.

The components of the transmit and receive portions of each layer are show in more detail in Figure 2 of Shin reproduced and annotated below:

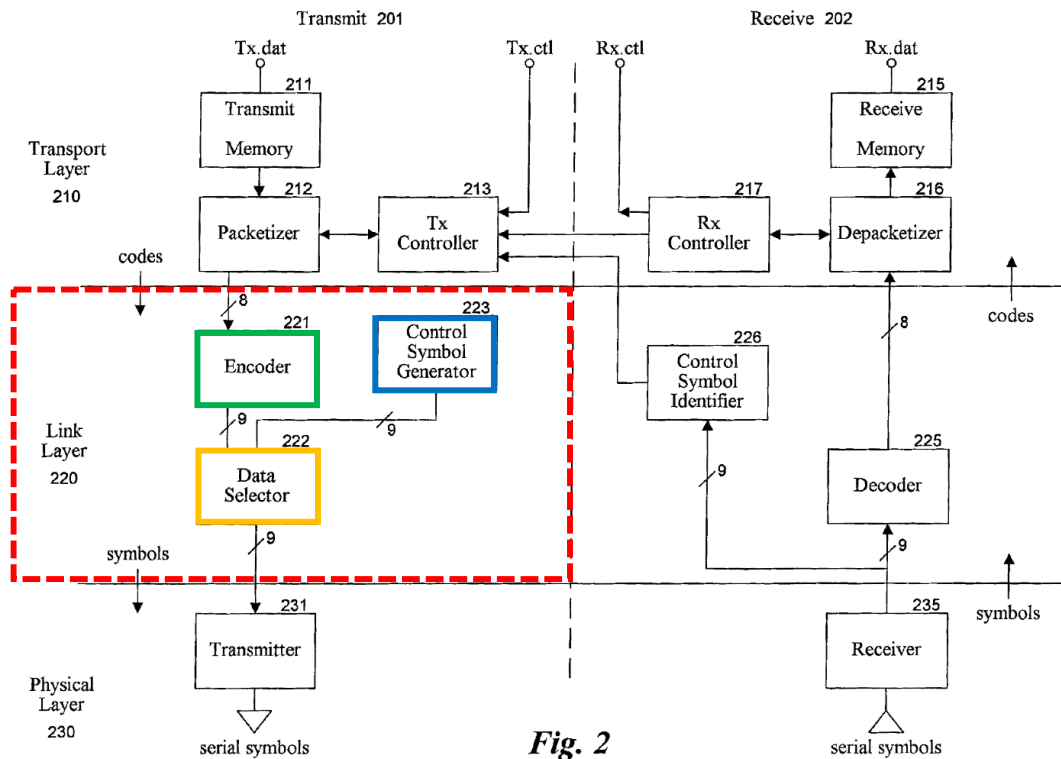


Fig. 2

Id. at Fig. 2 (annotated); EX2001 at ¶26.

Shown in **red** in annotated Figure 2 above is the link layer of a transmitter. EX2001 at ¶27. As Shin explains “[t]he link layer includes transmit components, such as an encoder **221**, a data selector **222**, and a control symbol generator **223**.” EX1004 at [0079]; EX2001 at ¶27. The Encoder (**green**) receives packetized data (i.e., application data) from the transport layer and encodes it into symbols for transmission. *Id.* at [0077]; EX2001 at ¶27. The Control Symbol Generator (**blue**) generates control symbols (such as primitives). EX1004 at [0079]; EX2001 at ¶27.

The Data Selector (**orange**) “selects symbols encoded from codes provided by the transport layer or symbols generated by the control symbol generator” and “effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be transmitted.” EX1004 at [0079]; EX2001 at ¶27.

The receive portion of the link layer includes a data decoder [225] and a control symbol identifier [226]. EX2001 at ¶28. “The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer.” EX1004 at [0079]; EX2001 at ¶28. “The control symbol identifier identifies control symbols and signals the transport layer as appropriate.” EX1004 at [0079]; EX2001 at ¶28.

2. Yusairi (EX1005)

Petitioners rely on Yusairi (EX1005) as their primary reference for obviousness under Ground 3. Yusairi is an article dated March 4, 2003 and titled “Hardware Design and Implementation of IP-over1394 Protocol Stack and Its Evaluation,” by Mohd Yusairi et al. EX2001 at ¶32.

Yusairi describes “a hardware design of a subset of the Internet protocol IP over IEEE1394 interface (IP over 1394) and its

implementation on an FPGA.” EX1005 at 5; EX2001 at ¶33. Yusairi utilizes a layered protocol stack together with data encapsulation and decapsulation as shown below in Figure 4:

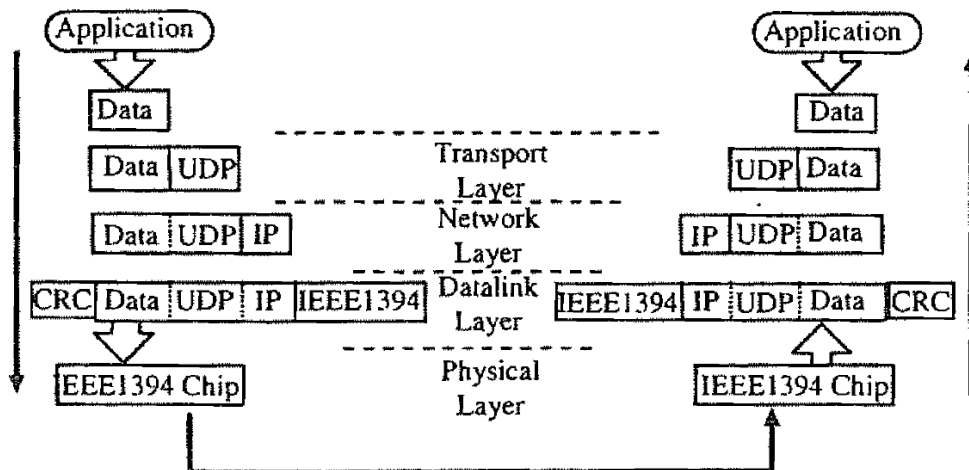


Fig. 4 UDP/IP protocol suite.

EX1005 at Fig. 4; EX2001 at ¶33.

III. THE *FINTIV* FACTORS WEIGH AGAINST INSTITUTION

The Board has discretion under 35 U.S.C. § 314(a) to deny institution of the requested *inter partes* review due to the advanced state of parallel district court litigation regarding the same issues. *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential, designated May 7, 2019). The Board has set forth six factors (known as the “Fintiv factors”) for determining whether discretionary denial is appropriate:

- whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
- proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
- investment in the parallel proceeding by the court and the parties;
- overlap between issues raised in the petition and in the parallel proceeding;
- whether the petitioner and the defendant in the parallel proceeding are the same party; and
- other circumstances that impact the Board’s exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential, designated May 5, 2020) (“*Fintiv I*”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 7-8 (PTAB May 13, 2020) (decision denying institution of inter partes review) (“*Fintiv II*”). “These factors relate to whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding.” *Fintiv I* at 6. In evaluating the factors, “the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.*

As set forth below, all of the *Fintiv* factors weigh against institution. To avoid duplication of efforts, wasting resources, and potentially inconsistent decisions, the Board should deny institution.

A. Factor 1: No stay has been entered in the LGL Case and there is no evidence that a stay will be granted

There are presently four district court cases involving the '307 patent: one pending in the Eastern District of Texas (*Universal Connectivity Technologies Inc. v. Lenovo Group Limited*, No. 2:23-cv-00449-JRG (the “LGL Case”)); one pending in Delaware (*Lenovo (United States) Inc. v. Universal Connectivity Technologies Inc.*, No. 1:24-cv-01126-RGA (the “Lenovo US Case”))¹; one pending in the Northern District of California (*Universal Connectivity Technologies Inc. v. HP Inc.*, No. 4:24-cv-04097-YGR (the “HP Case”))²; and one pending in the Western District of Texas (*Universal Connectivity Technologies Inc. v. Dell Inc.*, No. 1:23-cv-01506-RP (the “Dell Case”))³. Lenovo Group

¹ Lenovo US case is a declaratory judgment action filed by LGL’s wholly-owned, U.S.-based subsidiary Lenovo (United States) Inc., over a year after the LGL Case was filed. On December 2, 2024, UCT filed a Motion to Dismiss the Lenovo US Delaware action based on the first-to-file rule. See Case No. 1:24-cv-01126-RGA, Dkt. 10. Lenovo US filed its response on January 6, 2025, and UCT filed its reply on January 20, 2025.

² HP filed a motion to stay in the HP Case which was denied. See EX2003, Civil Minutes, HP Case, Dkt. No. 92.

³ Dell filed a motion to stay in the Dell Case which was granted. See EX2004, Order, Dell Case, Dkt. No. 69.

Limited (“LGL”), while not a Petitioner in the instant *inter partes* review request, is the parent of Petitioner Lenovo (United States) Inc. (“Lenovo US”) and has been identified as a real party-in-interest. *See* Petition at 1. The LGL Case is proceeding ahead of the other three cases, with a jury trial set to begin in November 2025. LGL has not filed a motion to stay in the LGL Case, nor is there any evidence to suggest a stay would be granted if such a motion was filed.

The LGL Case is not in its early stages. Jury selection is scheduled for later this year, on November 3, 2025. *See* EX2002, Docket Control Order, LGL Case, Dkt. 27 (June 12, 2024), at 1. This is “a deadline that cannot be changed without an acceptable showing of good cause. Good cause is not shown merely by indicating that the parties agree that the deadline should be changed.” *Id.* at 5. Fact discovery—including extensive third-party discovery—is ongoing. An institution decision on the ’307 IPR Petition is not due until April 2025. By that date, the parties will have substantially completed the claim construction process, with the *Markman* hearing scheduled for May 12, 2025. *See id.* at 4. A Final Written Decision would not be due until April 2026, five (5) months after trial is scheduled to begin. *See id.* at 1.

It is unlikely that a stay would be granted in the LGL Case at this time. *Trover Group, Inc. v. Dedicated Micros USA*, No. 2:13-cv-1047-WCB, 2015 WL 1069179, at *6 (E.D. Tex. Mar. 11, 2015) (Bryson, J.) (“This Court’s survey of cases from the Eastern District of Texas shows that when the PTAB has not yet acted on a petition for inter partes review, the courts have uniformly denied motions for a stay.”); *see also Samsung Elecs. Co. Ltd. v. Evolved Wireless LLC*, IPR2021-00950, Paper 10 at 10-11 (PTAB Nov. 29, 2021) (“*Evolved*”) (finding this factor weighed in favor of denial and denying institution where patent owner showed a stay was unlikely based on the advanced stage of the case and the court’s past decisions denying stays); *Samsung Elecs. Co. Ltd. v. Clear Imaging Research, LLC*, IPR2020-0152, Paper 12 at 12-13 (PTAB Mar. 3, 2021) (denying institution because, in part, Judge Gilstrap deemed unlikely to stay a case in similar circumstances).

The Eastern District of Texas is likely to find that a stay in this situation would unduly prejudice UCT, disfavoring a stay. *See, e.g., MyPort, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 2:22-cv-00114-JRG, Dkt. No. 73 (E.D. Tex. June 12, 2023) at 4 (Noting that patent owner has an interest in the timely enforcement of its patent rights and that

granting a stay could delay the case by nearly two years where the PTAB decision is not due until over two months after jury trial is set to begin.). The district court is also likely to find that the stage of litigation disfavors a stay. As noted above, by the date an institution decision is due in this proceeding, the parties will have substantially completed claim construction in the district court litigation and, as further evidenced by the docket sheet, a substantial amount of work and financial resources have been invested in the district court case. Under similar circumstances, the district court has found that the stage of litigation disfavors a stay. *Id.* at 5.

Moreover, because LGL has asserted multiple invalidity theories and there are other defendants who are asserting invalidity defenses, a stay in the district court would be unlikely to simplify the issues. As district courts have recognized, when a party has raised multiple invalidity theories that will not go before the PTAB, a stay would leave in limbo these invalidity theories that will not go before the Board, weighing against a stay. *Id.* at 5-6.

As explained by the Board, a stay of the district court litigation pending resolution of the PTAB proceedings “allays concerns about

inefficiency and duplication of efforts.” *Fintiv I* at 6; *Fintiv II* at 12. But here, the district court in the LGL case has not stayed the pending litigation, nor is there any evidence that a stay will be granted. Allowing this IPR to proceed simultaneously with the district court litigation in the LGL case would be wasteful and inefficient.⁴ This factor weighs against institution.

B. Factor 2: The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.

“If a district court’s trial date is earlier than the Board’s projected statutory deadline for a final written decision, the Board generally has weighed this fact in favor of exercising discretion to deny institution.” *T-Mobile USA, Inc., et al., v. Wireless Alliance*, IPR2024-00608, Paper 16 (PTAB Sept. 3, 2024) (exercising discretion to deny institution of *inter partes* review). The ’307 Petition was filed on October 2, 2024, a decision

⁴ While the HP case and the Dell case do not have a matching schedule to the LGL case, the resources expended in the LGL case are nonetheless wasteful and inefficient as all the Petitioners have taken a predominantly common approach with respect to prior art invalidity in their respective invalidity contentions for the ’307 Patent. *Compare* EX2005, Invalidity Contentions, LGL Case, at pp. 28-29, *with* EX2006, Invalidity Contentions, Dell Case, at pp. 27-28, *with* EX2007, Invalidity Contentions, HP Case, at 25-26.

whether to institute is expected approximately on April 30, 2025, and, if instituted, the statutory deadline for a final written decision is April 30, 2026, which can be extended to October 30, 2026, for good cause or in the case of joinder. 37 C.F.R. § 42.100.

Jury selection in the LGL Case is scheduled to begin on November 3, 2025. *See* EX2002 at 1. This is “a deadline that cannot be changed without an acceptable showing of good cause. Good cause is not shown merely by indicating that the parties agree that the deadline should be changed.” *Id.* at 5.

Even if the Board disregards the scheduled trial date, an analysis of the current median time-to-trial statistics still weighs against institution.⁵ *See* EX2008, U.S. District Courts—Federal Court Management Statistics—Profiles—During the 12-Month Periods Ending September 30, 2019 through 2024. The most recent statistics, for a 12-month period ending September 30, 2024, show a median time-to-trial in

⁵ “The Guidance Memo provides that the parties may also present the most recent statistics on median time-to-trial for civil actions in the relevant district court.” *T-Mobile*, IPR2024-00608, Paper 16 at 13 (citing the June 21, 2022 Memorandum “Interim Procedure for Discretionary Denials in AIA Post Grant Proceedings with Parallel District Court Litigation”).

the Eastern District of Texas of 21.9 months. *Id.* at 35. Accordingly, the projected trial date for purposes of *Fintiv* in accordance with Director’s June 21, 2022 Memorandum on Discretionary Denials would be around July 2025—close to the scheduled trial date and more than nine months before the expected timing of a Final Written Decision if proceedings are instituted. The Board recently found that this weighed in favor of exercising discretionary denial where the underlying litigation was also in the Eastern District of Texas and the projected trial date was prior to the date when the final written decision would be due. *See, e.g., T-Mobile*, IPR2024-00608, Paper 16 at 13 (“Because the district court would address issues relating to the validity of the ’662 patent in a trial that, by any measure, would occur many months before we would issue a final written decision, we weigh the second *Fintiv* factor as favoring discretionary denial.”).

Accordingly, this factor weighs against institution.

C. Factor 3: The parties and the courts have made a substantial investment in the parallel proceeding.

This factor relates to the “amount and type of work already completed in the parallel litigation by the court and the parties at the

time of the institution decision.” *Fintiv I* at 9 (emphasis added). For example, “if, at the time of the institution decision, the district court has issued substantive orders related to the patent at issue in the petition,” this factor favors denial. *Id.* at 9-10. Claim construction orders entered by the district court likewise “indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.” *Id.* at 10.

As discussed above, fact discovery between the parties is ongoing in the LGL Case. In addition, UCT has conducted extensive third-party discovery from LGL’s suppliers. By the date the institution decision is due, the parties will have substantially completed the claim construction process with the *Markman* hearing scheduled for May 12, 2025. *See* EX2002 at 4. As shown in the district court docket sheet, the courts and the parties have made a substantial investment in the LGL Case to date: the parties have already briefed, and the Court has denied, LGL’s Motion to Dismiss (*see* EX2009 Memorandum Opinion and Order, LGL Case, Dkt. No. 47) and the parties have already briefed, and the Court has granted, UCT’s Motion to Compel (*see* EX2010, Order, LGL Case, Dkt. No. 44).

Thus, the parties and the district court will have invested significant time and resources in the litigation by the time the Board reaches an institution decision in this matter. This favors discretionary denial. *Fintiv I* at 10; *Fintiv II* at 13-14 (finding that “the level of investment and effort already expended on claim construction and invalidity contentions” favored denial).

D. Factor 4: There is complete overlap between this IPR and the LGL Case

This factor looks at “whether all or some of the claims challenged in the petition are also at issue in district court,” and whether the “petition includes the same or substantially the same claims, grounds, arguments, and evidence” as the parallel district court case. *Fintiv I* at 12-13.

Here, Petitioners have challenged all of the asserted claims of the ’307 patent. And, LGL’s Preliminary Invalidity Contentions in the district court case identify the same Shin reference asserted in the Petition as prior art that either anticipates (Ground 1) or renders obvious (Grounds 2 and 3) the challenged claims. *See* EX2005 Invalidity Contentions, LGL Case, at 28-29. Likewise, HP and Dell also identified the same Shin reference in their invalidity contentions. *See* EX2006

Invalidity Contentions, Dell Case, at 27-28; EX2007 Invalidity Contentions, HP Case, at 25-26.

Thus, there is complete overlap with respect to the arguments and evidence presented here and in the district court litigation for Grounds 1 and 2, and substantial overlap for Ground 3 as it relates to Shin. That the district court case involves additional prior art references not asserted in this IPR is “not relevant to the question of the degree of overlap for this factor.” *Fintiv II* at 15. The fact that the Petition challenges additional claims does not warrant institution. *See, e.g., Next Caller Inc. v. TRUSTID, Inc.*, IPR2019- 00961, Paper 10 at 14 (PTAB Oct. 16, 2019) (denying institution where the district court case involved only a subset of the challenged claims).

Notably, none of the Petitioners have stipulated to not pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition (*i.e.*, a Sotera stipulation). Had the Petitioners done so, that could mitigate concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 18-19 (PTAB Dec. 1, 2020)

(precedential as to § II.A). Those concerns are particularly relevant when, as here, the Petitioners are asserting the same prior art in the district court and the PTAB, guaranteeing duplicative efforts between the district court and the PTAB and potentially conflicting decisions.

In sum, this IPR and the district court case involve the same claims—which will be construed under the same *Phillips* standard—and nearly the same prior art (and, as discussed below, the same parties), which raises substantial “concerns of inefficiency and the possibility of conflicting decisions.” *Fintiv I* at 12. This factor thus weighs in favor of a discretionary denial. *See Fintiv II* at 15; *NHK Spring* at 19–20.

E. Factor 5: The Petitioners and Real Parties-in-Interest are parties to the District Court Cases

There is no dispute that real party-in-interest LGL, parent of Lenovo US, is the defendant in the LGL Case. There is also no dispute that Lenovo US is the plaintiff in the Lenovo US Case, or that Dell and HP are defendants in the Dell Case and HP Case, respectively. “Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.” *Fintiv II* at 15.

F. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.

The Board may consider other circumstances in the exercise of its discretion, including the merits of the case. *Fintiv I* at 14. However, “a full analysis of the merits is not necessary to evaluate this factor.” *Fintiv II* at 17. And, it is important to note that the compelling merits standard is a higher standard than the standard for institution set by statute. “A challenge can only ‘plainly lead to a conclusion that one or more claims are unpatentable’ if it is highly likely that the petitioner would prevail with respect to at least one challenged claim.” *OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021-01064, Paper 102, 49 (PTAB Oct. 4, 2022) (precedential). Petitioners have not done so here, and, when considered together with the five other *Fintiv* factors discussed above, this factor also favors discretionary denial.

As discussed in detail below, the Petition does not present even a reasonable likelihood of unpatentability of any challenged claim, let alone compelling evidence of unpatentability, and factor 6 weighs against institution.⁶ All six *Fintiv* factors strongly favor discretionary denial, and

⁶ The Petition is defective for other reasons as well, but a full discussion of the merits is not required in the Patent Owner’s Preliminary Response.

the Petition should be denied on this basis alone.

IV. GROUND 1: CLAIMS 1, 2, 6, 7, AND 53 ARE NOT ANTICIPATED BY SHIN (EX1004)

Petitioners rely exclusively on Shin for Ground 1. As explained in more detail below, however, Shin does not disclose encoding *both* application data bits *and* controls bits to create “encoded data” that is decoded to recover *both* application data bits *and* controls bits. Petitioners rely on Shin’s disclosure of primitives as the recited “control bits” of the claims. The primitives in Shin, however, are not and cannot be the recited control bits of independent claims 1 and 53 at least because they are never encoded prior to transmission and they are never decoded upon receipt.

A. The ’307 Patent Discloses Encoding and Decoding Application Data Bits *and* Control Bits to Generate “Encoded Data”

The ’307 Patent describes generating encoded data (i.e., encoding application data bits and control bits into codewords) at the transmitter and then decoding that encoded data to recover the original application data bits and control bits at the receiver. With respect to the transmitter end of the communication system, the ’307 Patent explains that “application data and control bits are encoded in accordance with a line

code to generate sequences of code words that, when decoded, are indicative (at a 'link' level of communication protocol functionality) of cells of the application data and control bits." EX1001 at 4:33-38; EX2001 at ¶20. For example, M-bit input words comprising application data bits and control bits are encoded to generate N-bit codewords, where $M < N$. EX1001 at 4:53-56; *id.* at 4:59-63 ("At a 'link' level of communication protocol functionality... a sequence of a predetermined number of M-bit decoded words is indicative of a cell of the application data and control bits."). The '307 Patent explains that the line code "also specifies special characters that are distinguishable from bits of the encoded cell." EX1001, 8:48-59; *id.* at 5:15-19 ("the line code employed to transmit encoded data over a serial link specifies not only a block code (for encoding cells) but also special characters that are typically transmitted between cells."); *id.* at 8:60-67; *id.* at 10:46-11:4; EX2001 at ¶22.

With respect to the receiver end of the communication system, the '307 Patent teaches that the "[r]eceiving and decoding circuit 43 (of receiver 40) decodes code words received sequentially on channel 51 to generate a stream of decoded words (e.g., 9-bit words as shown in FIG. 2, each comprising eight application data bits and one control bit)."

EX1001, 13:37-41; *id.* at 10:62-11:4 (“recognize each transmitted special character, regardless of whether transmission of the special character has or has not interrupted transmission of a cell”). “De-packetizing circuit 45 then determines which of the bits of the corrected, decoded words are application data bits and which are control data bits, and asserts the application data, and appropriate ones of the control bits (separately from the application data) to higher layer circuitry 40 for processing.” EX1001, 13:48-56. The steps of encoding application data and control bits into encoded data that is later decoded to recover the application data and control bits is also illustrated in Figure 1 of the ’307 Patent.

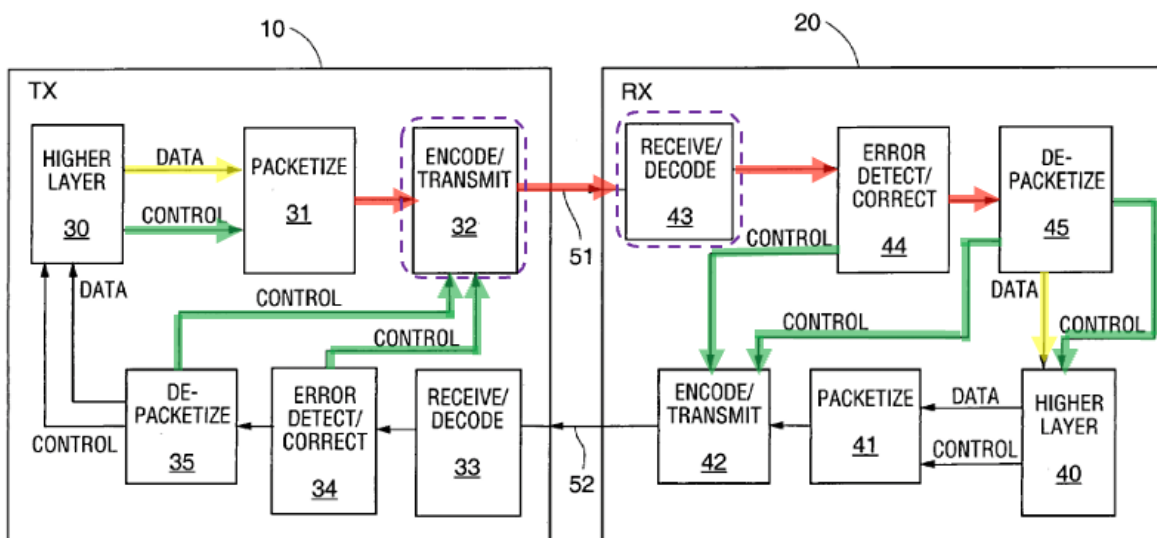


FIG. 1

EX1001, Fig. 1 (annotations added).

This is directly reflected in the independent claims. For example, independent claim 1 recites, in relevant part, “[a] communication system, including: a first endpoint [and] a second endpoint... wherein the first endpoint is ***configured to generate encoded data...*** and to transmit the encoded data... and wherein the physical and link layer circuitry of the second endpoint is coupled to the link and ***configured to decode the encoded data to recover application data and control bits...***” EX1001 at cl. 1 (emphasis added). Similarly, independent claim 53 recites, in relevant part, “[a] receiver for ***receiving encoded data...*** including physical and link layer circuitry, coupled and configured to ***receive and decode the encoded data to recover application data and control bits...***”. EX1001 at cl. 53.

Independent claims 1 and 53 each recites a second endpoint (i.e., a receiver) that can decode the encoded data received from the transmitter to recover both the application data bits and control bits. Accordingly, the recited “encoded data” of the claims must include both application data *and* control bits.

**B. Petitioners Fail to Demonstrate that Shin Discloses
“decod[ing] the encoded data to recover... control bits”
as recited in claims 1 and 53**

Independent claims 1 and 53 each recites, in relevant part,
“decod[ing] the encoded data to recover application data *and* control bits.”
EX1001 at cls. 1 and 53 (emphasis added).

For claim 1, Petitioners analyze this portion of the claim piecemeal,
separating the decoding portion from the recovery portion:

*1[e] wherein the physical and link layer circuitry of the second
endpoint is coupled to the link and **configured to decode the
encoded data***

*1[f] **to recover application data and control bits;***

Petition at 17 (emphasis added). Petitioners similarly separate out the
claim language in its analysis of claim 53. *See* Petition at 36 (analyzing
claim elements 53[a] and 53[b] and relying, in relevant part, on its
analysis for claim elements 1[e] and 1[f]).

For its analysis of claim element 1[f] (i.e., the “to recover” step),
Petitioners rely on an annotated version of Figure 9C of Shin, reproduced
(and further annotated) below:

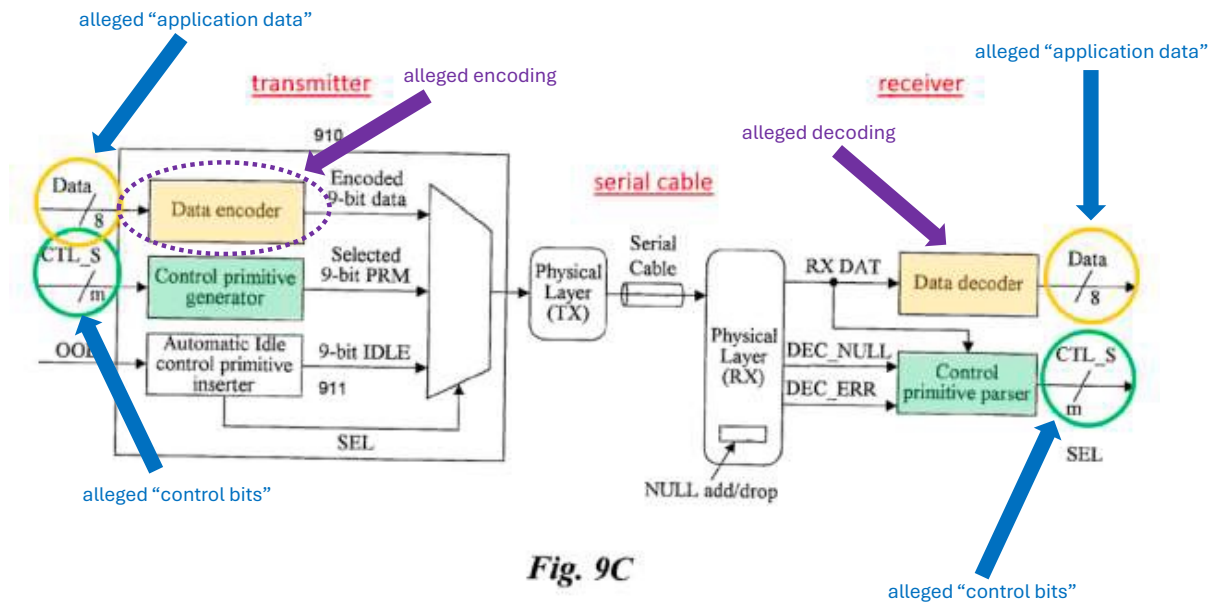


Fig. 9C

Petition at 19. Petitioners state “after receipt, the receiver data (RX DAT) that includes the encoded data is decoded by the data decoder (**orange**) to recover bits of data (e.g., 8 bits), while the primitives of the receiver data (RX DAT) are parsed by the control primitive parser (**green**) to recover ‘m’ control bits.” Petition at 19. Petitioners conclude that the “decoded ‘Data’ that is transmitted via ‘data packets’ (**orange**) constitutes *recover[ed] application data*, and the ‘m’ control bits recovered from parsing control primitives (‘CTL_S’) (**green**), such as preempt primitives, as well as the ‘control bit[s]’ recovered from synchronization primitives, constitute *recover[ed] control bits*.” Petition at 20.

But neither the “m” control bits recovered from parsing control primitives nor the control bits recovered from synchronization primitives of Shin constitute the recovered “control bits” of the claims because those bits are neither encoded at the transmitter (to form encoded data) nor recovered at the receiver by decoding the encoded data. EX2001 at ¶30. This is evident in Figure 9C relied on by Petitioners. EX1004 at [0105] (“FIG. 9C is a block diagram illustrating a component of a link layer for inserting a synchronization symbol into a stream of symbols.”); *see also id.* at [0022] (describing Figure 9C as “a block diagram illustrating a component of a link layer for inserting a synchronization symbol into a stream of symbols.”). For example, Shin explains that “[t]he link layer 910 is provided with the bits of the code (“Data”) to be transmitted and with an indication of a control primitive (“CTL-S”) to transmit.” *Id.* at [0105]. That is, the “Data” (circled in orange)—which Petitioners rely on as the recited “application data”—is provided by the transport layer and moves through the “Data encoder” (colored orange) at the link layer to create symbols for transmission (referenced as the “Encoded 9-bit data” in Fig. 9C). EX2001 at ¶30. The primitives (referenced as “CTL_S” in Fig. 9C circled in green) **do not** travel through the Data encoder as

input words to be encoded. Instead, they travel through the “Control primitive generator.” EX2001 at ¶30. It is only **after** the Encoded 9-bit data is created, that control symbols such as primitives are added into the sequence of symbols for transmission. EX2001 at ¶30. Likewise, at the receiver side of the communication link, the primitives do not travel through the “Data decoder.” EX2001 at ¶30. Instead, they are separated from the Encoded 9-bit data **prior to decoding** and travel through the “Control primitive parser.” EX2001 at ¶30. This makes sense because the primitives were never encoded by the Data Encoder in the first place and, thus, need not be decoded by the Data decoder at the receiver.

This understanding of Shin is further confirmed by Figure 2 reproduced and annotated below:

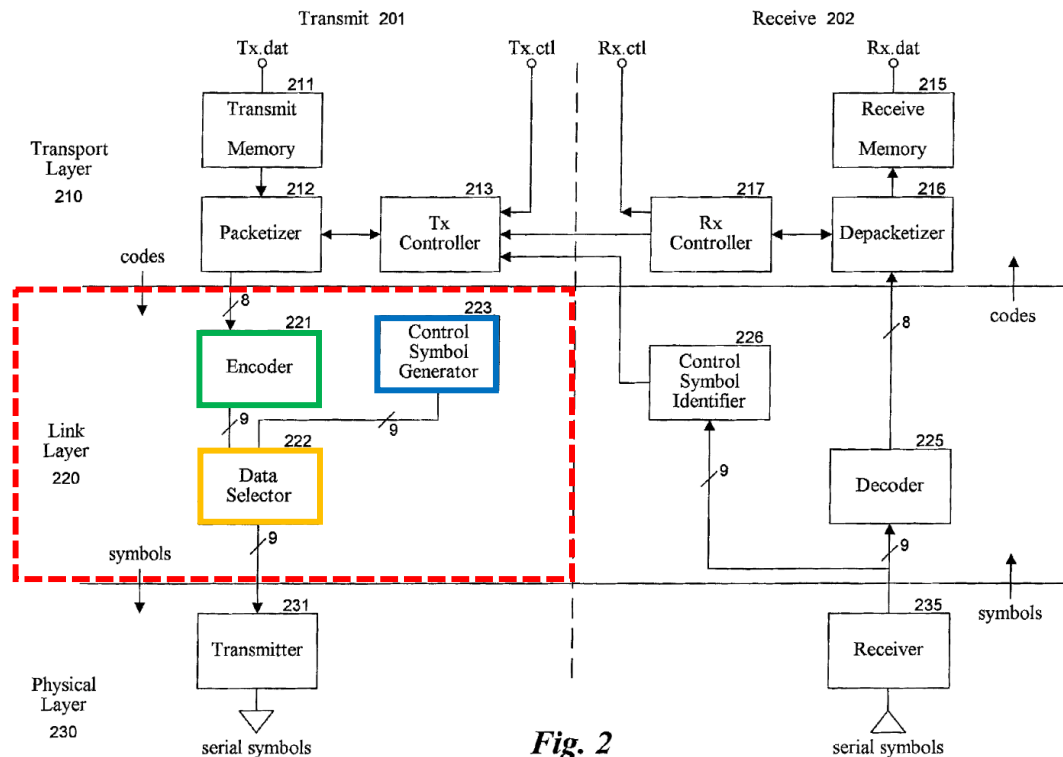


Fig. 2

EX1004 at Figure 2 (annotated). As Shin explains, the “Encoder” (**green**) receives packetized data (the alleged “application data”) from the transmit layer and encodes it into symbols for transmission. EX1004 at [0077]; EX2001 at ¶27. The “Control Symbol Generator” (**blue**) generates the control symbols (the alleged “control bits”). EX1004 at [0079]; EX2001 at ¶27. The “Data Selector” (**orange**) “selects symbols encoded from codes provided by the transport layer or symbols generated by the control symbol generator” and “effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be

transmitted.” EX1004 at [0079]; EX2001 at ¶27. In Shin, only the packetized data received from the transport layer is encoded; the control symbols and synchronization symbols are inserted in the sequence *after* the packetized data has been encoded. EX2001 at ¶30.

Shin is fundamentally different from the '307 patent. As explained above, the recited ***encoded data*** of claims 1 and 53 of the '307 patent must include both application data and control bits. That is made clear by the language in the latter portion of claims 1 and 53, which recites “the second endpoint... configured to ***decode the encoded data to recover*** application data and control bits.” Accordingly, the “encoded data” must include both application data *and* control bits, and the decoding process must recover both application data *and* control bits. Put simply, the primitives in Shin relied on by Petitioners as the recited “control bits” are never encoded at the transmitter side by the encoder nor decoded at the receiver side by the decoder. EX2001 at ¶30. Accordingly, they cannot be the recited “control bits” of the claims.

Petitioners’ reliance on Shin’s primitives as the recited “control bits” of claims 1 and 53 is wrong because Shin’s primitives are not encoded as part of the alleged encoded data and are not recovered at the

receiver. EX2001 at ¶30. In Shin, the primitives are separated out from the application data prior to decoding. *Id.* Thus, Shin is not “configured to decode the ***encoded data*** to recover application data and control bits” as recited in claims 1 and 53. EX2001 at ¶31.

C. Claims 2, 6, and 7 Are Not Anticipated by Shin

Shin does not anticipate dependent claims 2, 6, and 7 because, at a minimum, they each depend from independent claim 1, which is not anticipated by Shin for all of the reasons set forth above. Because Petitioners have not shown a reasonable likelihood that independent claim 1 is anticipated, each dependent claim is likewise not anticipated.

V. GROUND 2: CLAIMS 1, 2, 6, 7, AND 53 ARE NOT OBVIOUS OVER SHIN (EX1004)

A. Independent Claims 1 and 53 Are Not Obvious Over Shin

Petitioners combine their analysis for Grounds 1 (anticipation by Shin) and 2 (obviousness over Shin) together. Petition at 7. With respect to claim 1, the only element that Petitioners purport is rendered obvious by Shin (versus just being “disclosed” by Shin) is claim element 1[h]. Claim element 1[h] recites: “to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry...”

EX1001 at cl. 1. The entirety of Petitioners’ obviousness analysis for claim element 1[h] is found at pages 23-25 of the Petition. Petitioners’ obviousness analysis for claim 1—which is limited to claim element 1[h]—does not overcome the deficiencies described *supra* with respect to claim elements 1[d-f]. Accordingly, Petitioners have failed to show that Shin renders obvious claim 1.

With respect to claim 53, the only element that Petitioners purport is rendered obvious by Shin (versus just being “disclosed” by Shin) is claim element 53[d]. Claim element 53[d] recites: “higher level circuitry coupled to the physical and link layer circuitry, wherein the physical and link layer circuitry is coupled and configured to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry[.]” EX1001 at cl. 53. The entirety of Petitioners’ obviousness analysis for claim element 53[d] is found at page 36 of the Petition. Petitioners’ obviousness analysis for claim 53—which is limited to claim element 53[d]—does not overcome the deficiencies described *supra* with respect to claim elements 53[a-b]. Accordingly, Petitioners have failed to show that Shin renders obvious claim 53.

B. Dependent Claims 2, 6, and 7 Are Not Obvious Over Shin

Shin does not render obvious dependent claims 2, 6, and 7 because, at a minimum, they each depend from independent claim 1, which is not rendered obvious by Shin for all of the reasons set forth above. Because Petitioners have not shown a reasonable likelihood that independent claim 1 is rendered obvious, each dependent claim is likewise not obvious.

VI. GROUND 3: CLAIMS 1, 2, 6, 7, 23, 25, 31, 53, 68, 70, 71, 72, 74, AND 75 ARE NOT OBVIOUS OVER YUSAIRI (EX1005) IN VIEW OF SHIN (EX1004)

As explained *supra*, the '307 Patent describes encoding application data bits *and* control bits into “encoded data” at the transmitter and then decoding the “encoded data” at the receiver to recover the application data bits and control bits. Encoding and/or decoding of application data and controls bits is recited in every independent claim. Like Shin, Yusairi fails to disclose encoding both application data bits and control bits to create encoded data for transmission and fails to disclose decoding the encoded data to recover application data bits and controls bits.

For independent claims 1 and 53, Petitioners rely solely on Yusairi. Petition at 38-50, 60-61. Yusairi fails to disclose encoding (and decoding) control bits. Accordingly, Petitioners fail to demonstrate that Yusairi

discloses “generat[ing] encoded data” and “decod[ing] the encoded data to recover application data *and* control bits” as recited in claims 1 and 53.

For independent claims 23 and 68, Petitioners rely on the combination of Yusairi and Shin arguing, in relevant part, that a POSITA would use Shin’s encoding scheme with Yusairi’s link-layer circuitry to arrive at the claimed invention. Petition at 53-54, 63-64. That combination, however, fails to meet the claim limitations at least because the encoding method disclosed in Shin only encodes data, not control bits. Accordingly, using Shin’s encoding method with Yusairi’s link-layer circuitry as Petitioners suggest would not result in encoding both application data and control bits. Accordingly, Yusairi in view of Shin does not and cannot render obvious any of the challenged claims.

A. Petitioners Fail to Demonstrate that Yusairi Discloses “encoded data” and “decod[ing] the encoded data to recover... control bits” as recited in claims 1 and 53

With respect to independent claim 1, Petitioners contend that Yusairi discloses every claim element. Petition at 38-50. In the alternative, Petitioners also contend that Yusairi renders obvious claim element 1[i]. Petition at 50. Petitioners do not rely on obviousness for

any other element of claim 1 under Ground 3. In addition, Petitioners do not rely on Shin for any elements of claim 1 under Ground 3.

Independent claim 1 recites, in relevant part, “configured to generate encoded data” and “configured to decode the encoded data to recover application data *and* control bits.” EX1001 at cls. 1. Claim 53 recites, in relevant part, “[a] receiver for receiving encoded data... the encoded data having been generated in accordance with a line code” and “configured to receive and decode the encoded data...” *Id.* at cl. 53 (emphasis added).

For claim 1, Petitioners analyze this element of the claim piecemeal, separating the decoding portion from the recovery portion:

*1[d] wherein the first endpoint is **configured to generate encoded data** in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and*

*1[e] wherein the physical and link layer circuitry of the second endpoint is coupled to the link and **configured to decode the encoded data***

*1[f] to recover **application data and control bits**;*

Petition at 17 (emphasis added). Thus, Petitioners attempt to show the that limitations 1[d], 1[e] and 1[f] are separately satisfied and ignore that the “encoded data” is the same data that is then “decode[d]” “to recover application data and control bits.”

As to the alleged “encoded data” of claim element 1[d], Petitioners state that “Yusairi is encoding data by encapsulating it at SOPC Board A.” Petition at 43 (citing EX1003 at ¶¶151-152). Encapsulation as disclosed in Yusairi, however, is not encoding as disclosed in claim 1. EX2001 at ¶35. Figure 4 of Yusairi shows the encapsulation process:

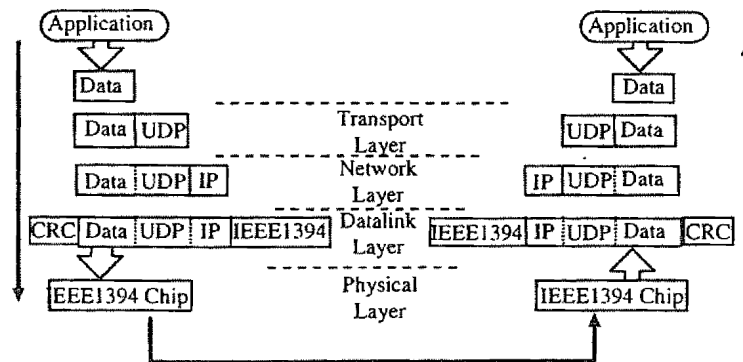


Fig. 4 UDP/IP protocol suite.

EX1005 at Sec. 4 (“The protocol stack we are going to implement is shown in Fig. 4 together with data encapsulation and decapsulation....”). Encapsulation does not change the underlying bits in anyway; instead, encapsulation merely repackages the data. EX2001 at ¶35. This is confirmed by EX1023 cited by Petitioners which states that “[e]ncapsulation is the computer-networking process of concatenating layer-specific headers or trailers with a service data unit (i.e. payload) for

transmitting information over computer networks.” EX1023 at 1. Encoding, on the other hand, changes the underlying bits by, for example, adding additional bits. This is confirmed by EX1020 cited by Petitioners which states “8b/10b in a line code that maps 8-bit words to 10-bit symbols....” EX1023 at 1. Accordingly, Yusairi does not disclose that the first endpoint is “configured to generate encoded data” as recited in claim 1. Likewise, Yusairi does not disclose a “receiver for receiving encoded data... the encoded data having been generated in accordance with a line code...” as recited in claim 53.

As to the alleged “decoding” step (limitation 1[e]), Petitioners identify a decapsulation process disclosed in Yusairi, stating that “[a] POSITA would have also understood that the encoded data is decoded by *the physical and link layer circuitry of SOPC Board B*” because “the ‘PHY [physical layer] hands a received packet to the module rec’ and the ‘rec module then puts the packet into a fifo.’” Petition at 45-46. Furthermore, Petitioners state that “[a]t the link layer, ‘stream_rec takes the data from the fifo and checks the link head’ to ‘start the header check process.’” *Id.* As to the “application data and control bits” (limitation 1[f]), Petitioners identify the “IP data” as the claimed “application data” and to the bits in

the “transaction code” and “type field” in the link header as the claimed “control bits.” Petition at 46.

Petitioners have not shown that the “transaction code” and “type field” values in the link header are the recited “control bits” of the claim at least because Yusairi indicates that those values are to remain as whole values and therefore, would not be encoded. The “transaction code” and the “type field” are used to specify that the IP data packet format is compliant with GASP format for the IP over IEEE 1394 standard. *See* EX1005, Sec. 5.2, pg. 9 (transaction code value equal to 0xA indicative of GASP type); *see* EX1005, Sec. 5.2, pg. 10 (type field value equal to 0x0800 indicative of IPv4); *see* EX1005, Sec. 4.3 (stating that “[t]he asynchronous stream packets must confirm to the GASP format”). According to Yusairi, the “transaction code” and the “type field” values are checked as whole values (0xA and 0x0080 respectively) to confirm the GASP packet meaning that any change to their format could result in them being ignored. *See* EX1005, Sec. 5.2 (“stream_rec: On detecting the signal from rec, stream_rec takes the data from the fifo and checks the link header. If the transaction code is equal to 0xA of the GASP type, stream_rec will start the header check process. **Otherwise, the packet will be**

ignored. The header check process checks header and data CRCs and the type field value. If both of the CRCs are correct and the type field equals to 0x0800 (IPv4) the packet is accepted and handed to the ip_rec. Otherwise, the packet is discarded and stream_rec clears the fifo in rec.”) (emphasis added); *see id.*, Sec. 3.1.2 (Global Asynchronous Stream Packet, GASP); *see also id.*, Sec. 4.3 “The asynchronous stream packets must conform to the GASP format. IP datagrams are prefixed by an encapsulation header containing type field identifying datagrams IPv4, ARP, etc. ”). Petitioners have not explained how the “transaction code” and “type field” values could be encoded without causing them to change format and be ignored. Accordingly, the “transaction code” and “type field” values of the link layer cannot be the “control bits” of claims 1 and 53 that are recovered by “decod[ing] the encoded data.”

Ultimately, Petitioners’ argument on claim elements 1[d]/1[e]/1[f] fails because Yusairi does not disclose encoding or decoding to recover *both* application data and control bits at the receiver as recited in claim 1.

Petitioners similarly separate out the claim language in its analysis of claim 53. *See* Petition at 60-61. Petitioners’ analysis of claim 53 relies

entirely on Petitioners' analysis of claim 1 and fails for the same reasons described above for claim 1.

B. Petitioners Fail to Demonstrate that Yusairi in View of Shin Discloses “encod[ing]... input words... [that are] indicative of application data and control bits” as Recited in Claim 23

Claim 23 recites:

[pre]⁷ A communication system, including:

[a] a first endpoint;

[b] a second endpoint; and

[c] a serial link between the first endpoint and the second endpoint,

[d] *wherein the first endpoint is configured to encode M-bit input words in accordance with a block code to generate a code word sequence* of N-bit code words, where $N > M$,

[e] *the code word sequence is indicative of at least one cell of the input words, the input words of each said cell are indicative of application data and control bits,*

[f] the control bits have multiple levels of communication protocol functionality, and

[g] the first endpoint is configured to transmit encoded data including the code words of the code word sequence over the link to the second endpoint.

⁷ This labeling follows how the Petitioners broke down the claim elements.

EX1001 at cl. 23 (emphasis added).

Petitioners fail to demonstrate that Yusairi in view of Shin renders obvious “encoding... input words... indicative of **application data and control bits**” because the combination of Yusairi and Shin does not disclose encoding input words that include both **application data and control bits** as recited in claim 23.

For claim element 23[d], Petitioners rely on the combination of Yusairi and Shin and refer back to their analysis of claim 2. Petition at 54 (“[a] POSITA would have been motivated to modify Yusairi with Shin’s encoding methods for the reasons discussed at limitation [2].”). For claim element 23[e], Petitioners rely on the combination of Yusairi and Shin and states that “Shin discloses that a packet (*cell*) can be formed into codes (*input words*) that are encoded by block encoding into symbols (*code words*). A POSITA would have understood that when Yusairi’s packet having application data (IP data) and control bits (transaction code and type field) are encoded using Shin’s block code, the application data and control bits from the packet (*cell*) would have been placed into codes (*input words*) before being encoded into symbols (code words). [] Thus, by applying Shin’s block encoding to Yusairi’s packets, the codes (*input*

words) of each packet (*cell*) would be indicative of application data and control bits.” Petition at 54-55.

There are several problems with Petitioners’ argument. First, as explained *supra* in Ground 1, Shin does not encode or decode control bits (i.e., “control symbols” in Shin). *See supra* at Section IV.B. Rather, Shin teaches encoding ***data*** at the link layer—not the alleged “control bits” (i.e., “control symbols” in Shin). *Id.* In fact, Shin is clear that the control symbols are not encoded at the link layer, but rather, are added to the sequence of codewords *after* the data is encoded. *Id.* This is clearly shown in Figure 2 of Shin reproduced and annotated below:

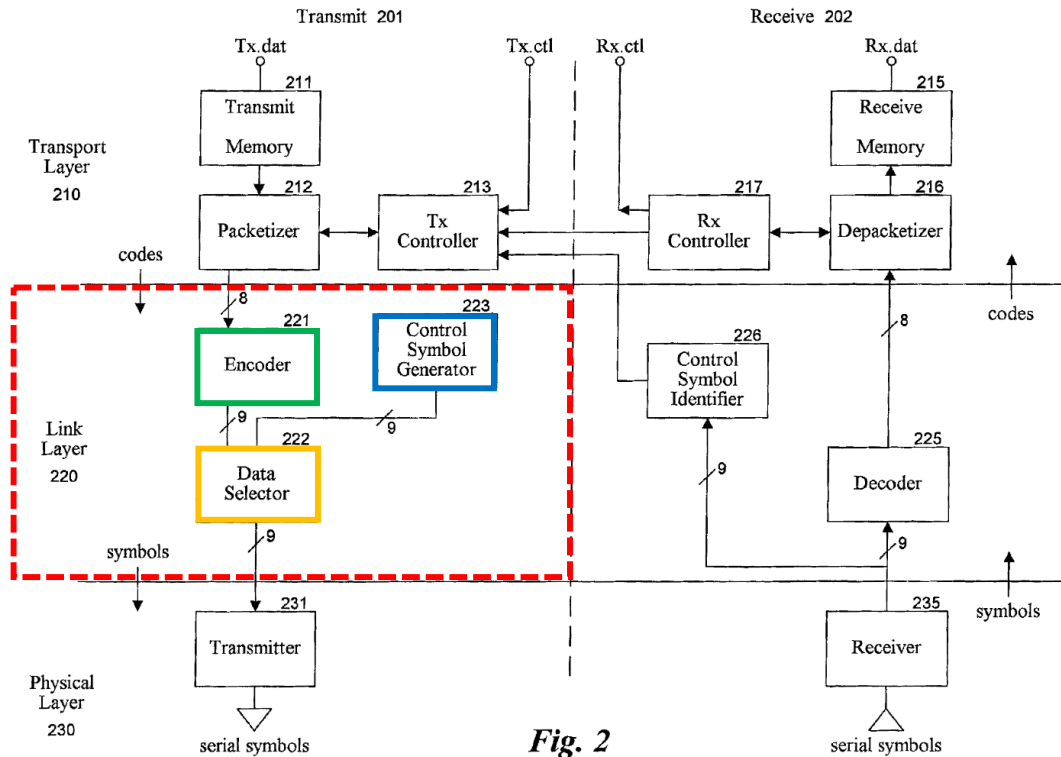


Fig. 2

Id. at Fig. 2 (annotated).

The Packetizer **212** of the Transport Layer provides the codes (i.e., packetized data) to the Encoder **221** of the Link Layer. EX1004 at Fig. 2; EX2001 at ¶27. The packetized data that enters the Encoder **221** does not include the control symbols which are instead generated by the Control Symbol Generator **223**. EX2001 at ¶27. Encoder **221** encodes those codes into symbols and provides those encoded codes to the Data Selector **222**. EX1004 at [0077] (“[t]he link layer receives codes to be transmitted from the transport layer, encodes those codes into symbols,

and provides those symbols to the physical layer.”); EX2001 at ¶27. The Data Selector **222** “selects symbols encoded from codes provided by the transport layer or symbols generated by the control symbol generator” and “effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be transmitted.” EX1004 at [0077] (emphasis added); EX2001 at ¶27. That is, the Data Selector creates a sequence of symbols for transmission by interlacing the control symbols provided by Control Symbol Generator **223** within the sequence of symbols of encoded data output from the Encoder **221**. Accordingly, Shin’s encoding scheme is only applied to the codes (i.e., the alleged “application data”) provided by the Transport Layer—*not* to control symbols (i.e., the alleged “control bits”); EX2001 at ¶¶26-31, 38-39. Thus, adding Shin’s encoding scheme to Yusairi would likewise result in the scheme only being applied to the *data* in Yusairi, not the alleged “control bits.” *Id.* Importantly, Petitioners do not adequately explain why a POSITA would apply Shin’s encoding to the alleged “control bits” in Yusairi when Shin expressly teaches that control symbols are added to the transmission sequence *after* encoding. *See* EX2001 at ¶¶38-39; *Globus Med., Inc. v. Moskowitz Fam. LLC*, IPR2020-01310, Paper 7 at 14

(P.T.A.B. Feb. 4, 2021) (“The Petition, however, does not assert with any clarity or particularity that it would have been obvious to modify Gutlin’s implant parts 5, 2 to expand laterally like Barber’s brackets 45 or provide any sufficient rational underpinning that such a modification would have been obvious.”).

Second, as explained *supra* with respect to claims 1 and 53 under Ground 3, Yusairi explains that the “transaction code” and the “type filed” values are checked as whole values (0xA and 0x0080 respectively) to confirm the GASP packet meaning that they cannot be divided into individual bits or else they would lose the format confirmation resulting in the IP datagram being either ignored and discarded. *See* EX1005, Sec. 5.2 (“stream_rec: On detecting the signal from rec, stream_rec takes the data from the fifo and checks the link header. If the transaction code is equal to 0xA of the GASP type, stream_rec will start the header check process. **Otherwise, the packet will be ignored.**”). If Shin’s encoding scheme were applied to the “transaction code” and “field type” values, then they would no longer be 0xA and 0x0080 respectively. This is confirmed by the language in claim 23 which recites “wherein the first endpoint is configured to encode M-bit input words in accordance with a

block code to generate a code word sequence of N-bit code words, where $N > M$...” EX1001 at cl. 23. That is, applying a block code increases the number of bits. For this reason, Shin’s encoding scheme would not be applied to Yusairi’s alleged “control bits” because it would result in the “transaction code” and “type field” values being ignored.

Lastly, Petitioners alleged motivation to combine does not address why a POSITA would add Shin’s encoding scheme to the “transaction code” and “field type” values in Yusairi when neither Shin nor Yusairi ever contemplate encoding “control bits.” Instead, Petitioners state that “[a] POSITA would have been motivated to use Shin’s block encoding methods to encode Yusairi’s packets because Shin’s block encoding methods... would have provided Yusairi with known communication protocols having a neutral DC component to help ensure signal is accurately received and decoded by synchronizing the SOPC Board B receiver with the SOPC Board A transmitter.” Petition at 51. But that alleged motivation is related to the benefit of Shin’s block encoding scheme generally. EX2001 at ¶40. It has nothing to do with why a POSITA would be motivated to use Shin’s encoding scheme on the alleged control bits of Yusairi when Shin *expressly teaches* that control bits are

not encoded and instead, are added to the transmission sequence *after* encoding. Accordingly, a POSITA would not be motivated to combine Yusairi and Shin as described by Petitioners. EX2001 at ¶¶37-40.

Accordingly, Yusairi in view of Shin does not render obvious claim 23.

C. Petitioners Fail to Demonstrate that Yusairi in view of Shin Discloses “generat[ing]... input words, wherein the input words are indicative of application data and control bits...[and] encod[ing] the input words...” as Recited in Claim 68

Petitioners’ analysis of claim 68 fails for the same reasons as discussed *supra* for claim 23. For the portion of claim 68 that recites “configured to generate M-bit input words[,]” Petitioners assert, as it did for claim 23, that “Shin’s packet (cell) can be formed into codes (M-bit input words) that are encoded by block encoding into symbols (code words)” and that “[a] POSITA would have been motivated to use Shin’s block encoding methods, which generate M-bit input words, with Yusairi’s link-layer packetizing circuitry in generating packets for transmission.” Petition at 63. For the portion of claim 68 that recites “wherein the input words are indicative of application data and control bits[,]” Petitioners rely exclusively on its analysis of claim element 23[e].

Petition at 64. For the portion of claim 68 that recites “configured to encode the input words...” Petitioners again rely on the combination of Shin’s encoding with Yusairi’s packetizing circuitry. Petition at 65-66.

Accordingly, for the reasons discussed above with respect to claim 23, the combination of Yusairi and Shin does not render obvious claim 68.

**D. Dependent Claims 2, 6, 7, 25, 31, 70, 71, 72, 74, and 75
Are Not Obvious Over Yusairi in view of Shin**

Yusairi in view of Shin does not render obvious dependent claims 2, 6, 7, 25, 31, 70, 71, 72, 74, and 75 because, at a minimum, they each depend from the independent claims that—for all the reasons set forth above—are not rendered obvious by the combination of Yusairi and Shin. Because Petitioners have not shown a reasonable likelihood that the independent claims are rendered obvious, each dependent claim is likewise not obvious.

VII. CONCLUSION

As discussed *supra*, all of the *Fintiv* factors strongly favor discretionary denial, and the Petition should be denied for this reason alone. Alternatively, the Board should deny institution on the merits because the Petitioners have not demonstrated any reasonable likelihood

of prevailing with respect to at least one of the claims challenged in the
Petition.

Date: January 31, 2025

Respectfully submitted,

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that there are no more than 9,366 words in the paper excluding the portions exempted under 37 C.F.R. § 42.24(a)(1).

Dated: January 31, 2025

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on January 31, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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