

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inter Partes Review

HP Inc., Dell Technologies Inc., Dell Inc., AND
Lenovo (United States) Inc.,
Petitioners,
v.

Universal Connectivity Technologies Inc.,
Patent Owner.

IPR2024-01429
U.S. Patent No. 7,187,307

**DECLARATION OF DR. WILLIAM H. MANGIONE-SMITH
IN SUPPORT OF PATENT OWNER'S
PRELIMINARY RESPONSE**

I, William Mangione-Smith, of Kirkland WA, declare that:

I. INTRODUCTION

1. Universal Connectivity Technologies Inc. (“UCT”) has retained me as an independent expert in connection with IPR2024-01429 to provide testimony regarding the technology involved in U.S. Patent No. 7,187,307 (the “’307 Patent,” or the “Challenged Patent”) and how the inventions described and claimed therein compare with the asserted prior art. I have been asked to provide my technical review, analysis, insights, and opinions regarding the references set forth in the above-referenced IPR.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation is not dependent on the outcome of the case and does not affect the substance of my statements in this Declaration. I have no financial interest in the matter or the patent at issue.

3. I have reviewed the specification and the claims of the ’307 patent, as well as the prosecution history for the patent. I am familiar with the technology involved therein, having practical, hands-on experience in the field for over 30 years. I have also reviewed each of the alleged prior art references cited herein as well as the declaration of Petitioners’ expert, Dr. Wolfe (Exhibit 1003).

II. QUALIFICATIONS

4. My technical background and experience covers most aspects of computer system design, including low level circuitry, computer architecture, computer networking, graphics, application software, client-server application, Web technology, and system software (e.g., operating systems and compilers). I am a member of the Institute of Electrical and Electronics Engineers and the Association for Computing Machinery, which are the two most significant professional organizations in my profession. I have been employed as a design engineer, research engineer, professor and technical expert. Over my professional career, I have been an active inventor with 112 issued U.S. patents, 200 published and pending U.S. patent applications and many unpublished U.S. patent applications.

5. From 1984 until 1991 I attended the University of Michigan in Ann Arbor, Michigan, where I was awarded the degrees of Bachelor of Science and Engineering, Master of Science and Engineering, and Doctorate of Philosophy. My doctoral research focused on high performance computing systems including computer architecture, applications and operating system software, and compiler technology. One of my responsibilities during my graduate studies included teaching senior undergraduate students who were about to enter the profession.

6. After graduating from the University of Michigan I was employed by Motorola in Schaumburg, Illinois. While at Motorola, I was part of a team designing and manufacturing the first commercial battery-powered product capable of delivering Internet email over a wireless (i.e., radio frequency) link and one of the first personal digital assistants. I also served as the lead architect on the second-generation of this device with control over the entire system design including the memory subsystem architecture, embedded processor, ASIC, power system, and analog circuitry. Part of my responsibilities at Motorola involved the specification, design, and testing of system control Application-Specific Integrated Circuits (“ASICs”). I conducted the initial research and advanced design that resulted in the Motorola M*Core embedded microprocessor. M*Core was designed to provide the high performance of desktop microprocessors with the low power of contemporaneous embedded processors. The M*Core received widespread use in many communications products including various cellular handsets, advanced pagers, and embedded infrastructure. While at Motorola I was the sole inventor on one U.S. patent.

7. From 1995 until 2005 I was employed by the University of California at Los Angeles (“UCLA”) as a professor of Electrical Engineering. I was the director of the laboratory for Compiler and Architecture Research in Embedded Systems

(“CARES”) and served as the field chair for Embedded Computing Systems. The CARES research team focused on research, engineering and design challenges in the context of battery-powered and multi-media mobile computing devices. One of the key developments of my lab was the Mediabench software tool, which is widely used to design and evaluate multi-media embedded devices. Key elements of Mediabench include software that is essential for modern digital wireless communications. My primary responsibility, in addition to classroom teaching, involved directing the research and training of graduate students. I was a tenured member of the faculty, and had responsibilities for teaching as well as scholarly research. While at UCLA I was a named inventor on three U.S. patent applications, one of which issued as a patent. My colleagues at UCLA were some of the leading scientists and engineers in the world with a long list of innovations from computer network security devices to the nicotine patch. The graduate student researchers in my laboratory came from a diverse set of backgrounds, all with undergraduate degrees in computer engineering, electrical engineering or computer science, many with multiple years of experience working as professional engineers in areas such as software development, computer system design and ASIC circuit design.

8. From 2005 until 2009, I was employed at Intellectual Ventures in Bellevue, Washington. My responsibilities at Intellectual Ventures included

business development, technology assessment, market forecasting, university outreach, collaborative inventing, intellectual property licensing support, and intellectual property asset pricing. My colleagues and co-inventors at Intellectual Ventures included the former lead intellectual property strategist at Intel, Intel's former lead IP council, Microsoft's former chief software architect, the founder of Microsoft research, the designer of the Mach operating system, the architect of the U.S. Defense Department's Strategic Defense Initiative, the founder of Thinking Machines (a seminal parallel processing computer system), and Bill Gates. I had responsibility for hiring and managing over 15 staff members including multiple Ph.Ds. with degrees in electrical engineering and decades of experience in product design and engineering.

9. A summary of some of my qualifications for forming the opinions in this declaration are as follows: I have more than 30 years of experience as a computer architect, computer system designer, educator, and as an executive in the PC and electronics business. I am also a member of several professional associations, such as the ACM, IEEE and have been intimately involved in professional research through the International Symposium on Microarchitecture (Program Chair for 26th and General Chair for 36th), IEEE Transactions on Computers (Associate Editor), ACM Transactions on Embedded Computing Systems (Associate Editor), and IEEE

Computer (Associate Editor). I also have been on the program committees for ISCA, MICRO, ISLPED, Network Processors Workshop, FPL, Complexity-Effective Design, RAW, Workshop on Mediaprocessors, and DSP, FPT, and INTERACT.

10. For further details regarding my employment and academic history, please refer to my curriculum vitae attached as Appendix A to this report.

III. SCOPE OF WORK

11. I have been asked to consider and provide my opinions on the claims of the Challenged Patent, including the technical subject matter and the application of various references that predate the priority date of the Challenged Patent. In particular, I have been asked to consider what one of ordinary skill in the art would have understood from the claims and specification of the Challenged Patent, and whether certain references would have disclosed or suggested the features recited in the claims of the Challenged Patent to a person of ordinary skill in the art at the time of filing of the Challenged Patent.

12. My opinions set forth below are based on my education, training, experience, and the content of the references considered.

IV. LEVEL OF ORDINARY SKILL IN THE ART

13. My opinions are provided based on what a person of ordinary skill in the art in the technical field of the inventions of the Challenged Patent would have understood at the time of filing of the Challenged Patent.

14. I have been informed and understand that the content of a patent and prior art should be interpreted the way a person of ordinary skill in the art would have interpreted those references at the time of filing of the patent. I understand that the person of ordinary skill is a hypothetical concept referring to one who understands the technology and associated conventional wisdom at the time.

15. I was asked to provide an opinion as to the level of one of ordinary skill in the art pertinent to the subject matter set forth in the Challenged Patent at the time of the priority date. It is my opinion that a person of ordinary skill in the art in the field of the Challenged Patent would have the equivalent of a bachelor's degree in electrical engineering, computer engineering, computer science, or equivalent training and three years of work experience with data communications systems or interfaces, including at least some experience with serial or display data communications systems or interfaces. I understand that Dr. Wolfe offered a slightly different opinion as to the level of skill in the art. Exhibit 1003 at ¶29. My opinions

regarding patentability of the Challenged Patent would not change if Dr. Wolfe's opinion as to the level of skill in the art were applied.

16. Throughout this declaration, I use the term "POSITA" to refer to a person with these or similar qualifications. To have similar qualifications, an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional education or experience compensates for a deficit in one of the other aspects of the requirements stated above.

17. The basis for my familiarity with the level of ordinary skill is my interaction with large numbers of workers in the relevant field who were at this level of skill. In reaching this opinion as to the hypothetical person of ordinary skill in the art, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field. I further note that, as of June 12, 2003, the filing date of the Challenged Patent, I was at least at this level of skill.

V. OVERVIEW OF THE CHALLENGED PATENT

A. Assumed Effective Filing and Invention Dates

18. The '307 Patent is titled "Method and System for Encapsulation of Multiple Levels of Communication Protocol Functionality within Line Codes" and

was filed on June 12, 2003. *See* Ex. 1001. I assume the priority date for the Challenged Patent is the filing date of the patent application, June 12, 2003.

B. The Challenged Patent

19. As noted in the Background of the Invention section of the Challenged Patent, “[l]ine coding techniques are often employed in serial, digital transmission (at the physical layer) to transform the frequency spectrum of the transmitted data stream to adapt to channel characteristics and facilitate clock/data recovery by receiver systems. This is typically accomplished using a block code which encodes a number of user data bits as a larger number of bits, according to some pre-determined table or function.” Ex. 1001, 1:34-42.

20. As explained in the Summary of the Invention section of the Challenged Patent, “[i]n a class of embodiments of the invention, application data and control bits are encoded in accordance with a line code to generate sequences of code words that, when decoded, are indicative (at a ‘link’ level of communication protocol functionality) of cells of the application data and control bits. The line code provides packet-based (cell-based) communication with multiple logical communication paths (virtual channels). The virtual channels include a virtual channel (a ‘control’ channel) for the control bits (or a control channel for each of two or more subsets of the control bits in each cell) and at least one virtual channel (a ‘data’ channel) for

the application data (e.g., a data channel for each of two or more blocks of application data in each cell).” *Id.*, 4:33-46.

21. The Challenged Patent discloses an exemplary communication system in Figure 1:

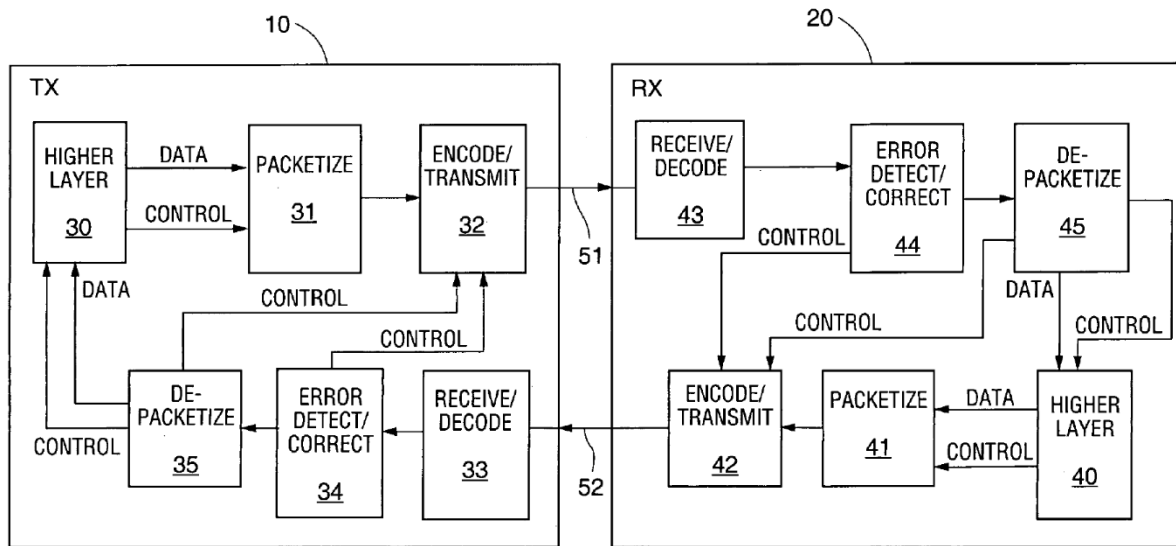


FIG. 1

Ex. 1001, Fig. 1.

22. In typical implementations, the packetizing circuitry at the transmitter generates sequences of input words indicative of application data and control bits. Ex. 1001, Figs 1 and 2, 10:20-39, 10:46-49. The encoding circuitry encodes the input words into a sequence of code words according to a block code specified by a line code. Ex. 1001, Fig. 2, 11:45-47, 11:66-12:2. The line code also specifies certain special characters which are distinguished from the code words. Ex. 1001,

10:46-51. These special characters are also transmitted over the link, but they are not encoded with the codewords.

23. Once the codewords are generated and combined with the special characters, the entire sequence is transmitted to the receiver. Ex. 1001, Fig. 1, 5:15-28, 10:46-62. Receiving/decoding circuitry receives the sequence, recognizing and separating the special characters and decoding the codewords to generate a stream of decoded words which are the original input words. Ex. 1001, Figs 1 and 2, 13: 37-41; Ex. 1001, 10:62-11:4. Depacketizing circuitry then determines which of the input words are application data and which are control bits. The control bits are then sent to higher layer circuitry for processing. Ex. 1001, 13:48-56.

24. “The control bits in each cell typically have multiple levels of communication protocol functionality.” Ex. 1001 at 4:66-5:1. “Link layer circuitry in the receiver recognizes the cells in response to the M-bit decoded words..., performs link level functions in responses to appropriate ones of the controls bits, and asserts the decoded application data bits and appropriate ones of the decoded control bits to higher-level circuitry (circuitry that operates at least one level of communication protocol functionality higher than the link level).” Ex. 1001 at 5:1-10. “The decoded control bits are used by the higher-level circuitry (which can be network layer circuitry and/or application layer circuitry, for example) to implement

communication protocol functions at least one level higher than the link level.” Ex. 1001 at 5:10-14.

VI. WHY THE CHALLENGED CLAIMS ARE NOT INVALID

A. Grounds 1 and 2: Shin Does Not Disclose or Render Obvious “decod[ing] the encoded data to recover application data and control bits.”

25. For Grounds 1 and 2, Petitioners rely only on the Shin reference (Ex. 1004). Shin is a U.S. Patent Application that was filed on November 7, 2001 and published on October 31, 2002 under Publication No. 2002/0159450. Shin is titled “Method and System for Asymmetric Packet Ordering Between Communications Devices.”

26. Shin describes “[a] serial communications architecture for communicating between hosts and data store devices.” Ex. 1004 at Abstract. Shin’s architecture is depicted in the annotated version of Figure 2 shown below:

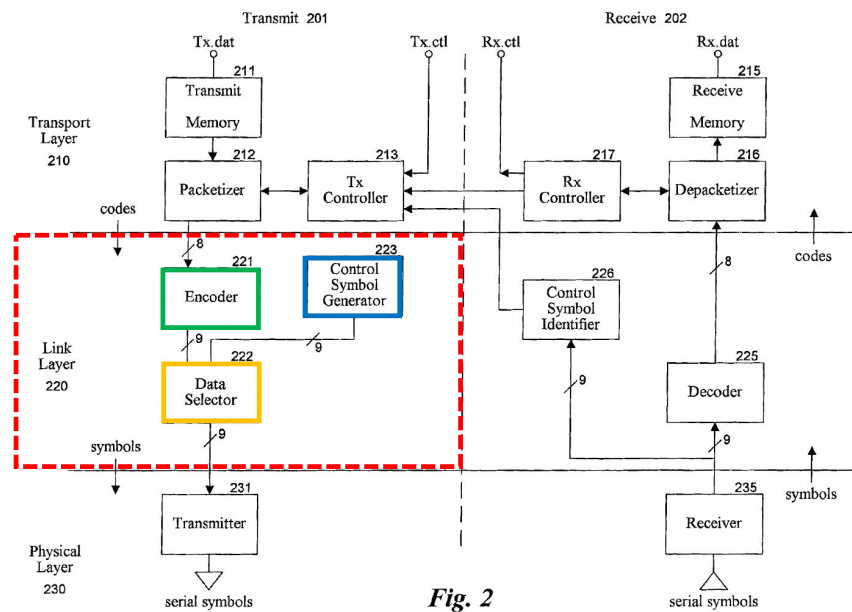


Fig. 2

27. The Link Layer is shown in red. “The link layer includes transmit components, such as an encoder 221, a data selector 222, and a control symbol generator 223.” Ex. 1004 at [0079]. The Encoder (shown above in green) receives packetized data (i.e., application data) from the transport layer and encodes it into symbols for transmission. *Id.* at [0077]. The Control Symbol Generator (shown above in blue) generates control symbols (such as primitives). *Id.* at [0079]. The Data Selector (shown above in orange) “selects symbols encoded from codes provided by the transport layer or symbols generated by the control symbol generator” and “effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be transmitted.” *Id.*

28. The receive portion of the link layer includes a data decoder [225] and a control symbol identifier [226]. “The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer.” Ex. 1004 at [0079]. “The control symbol identifier identifies control symbols and signals the transport layer as appropriate.” *Id.*

29. Independent claims 1 and 53 both recite, in relevant part, “decod[ing] the encoded data to recover application data and control bits.” Ex. 1001 at cls. 1 and 53 (emphasis added). Petitioners and Dr. Wolfe state that Shin discloses this claim element. Petition at 17, 36; Exhibit 1003 at ¶¶ 76-80, 122-126. That is, Petitioners and Dr. Wolfe do not rely on obviousness for this claim element. Shin does not disclose “decod[ing] the encoded data to recover... control bits.”

30. For the “control bits” portion of independent claims 1 and 53, Petitioners and Dr. Wolfe rely on the “m” control bits recovered from parsing control primitives (“CTL_S”), such as preempt primitives, as well as those recovered from synchronization primitives. Petition at 20; Exhibit 1003 at ¶ 81. However, Petitioners and Dr. Wolfe fail to recognize that neither the “m” control bits recovered from parsing control primitives nor the control bits recovered from synchronization primitives of Shin constitute the recovered control bits of the claims at least because they are not encoded at the transmitter or decoded at the receiver. This can be seen

from Petitioners' annotated Figure 9C which shows that only the "Data" moves through the "Data encoder" at the Link Layer to create symbols for transmission.

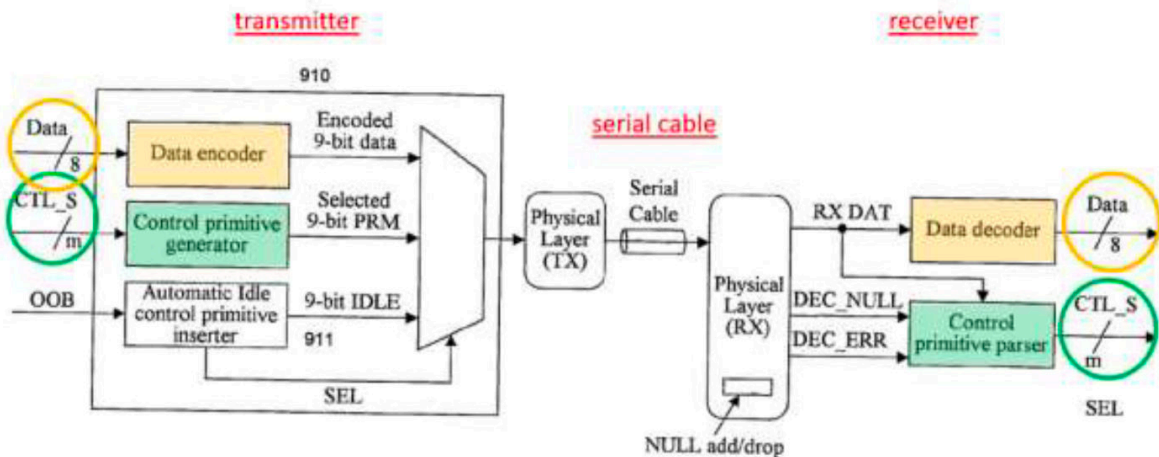


Fig. 9C

Pet. 19 (citing Ex. 1004 at Fig. 9C) (annotations in Petition); *see also* Exhibit 1003 ¶ 36. The primitives ("CTL_S") do not travel through the "Data encoder" as input words to be encoded. Rather, they move through the "Control primitive generator" and are added to the sequence of symbols *after* the "Data" is encoded. On the receiver side, the primitives likewise do not move through the "Data decoder." Instead, they are separated out from the Encoded 9-bit data prior to the decoding process and travel through the "Control primitive parser." Shin only discloses that the packetized data received from the transport later is encoded, not the control symbols.

31. Accordingly, the primitives in Shin cannot be the recited “control bits” of independent claims 1 and 53 because they are never encoded at the transmitter side by the encoder and they are never decoded at the receiver side by the data decoder. Therefore, I disagree with Petitioners and Dr. Wolfe that Shin anticipates or renders obvious these claims.

B. Ground 3: Yusairi in view of Shin Does Not Render Obvious the Independent Claims

32. For Ground 3, Petitioners and Dr. Wolfe rely on the combination of the Yusairi reference (Ex. 1005) and the Shin reference (Ex. 1004). Petition at 37; *see, e.g.*, Exhibit 1003 at ¶ 138-174. Yusairi is an article dated March 4, 2003 and titled “Hardware Design and Implementation of IP-over1394 Protocol Stack and Its Evaluation,” by Mohd Yusairi et al.

33. Yusairi describes “a hardware design of a subset of the Internet protocol IP over IEEE1394 interface (IP over 1394) and its implementation on an FPGA.” Ex. 1005 at 5. Yusairi utilizes a layered protocol stack together with data encapsulation and decapsulation as shown below in Figure 4:

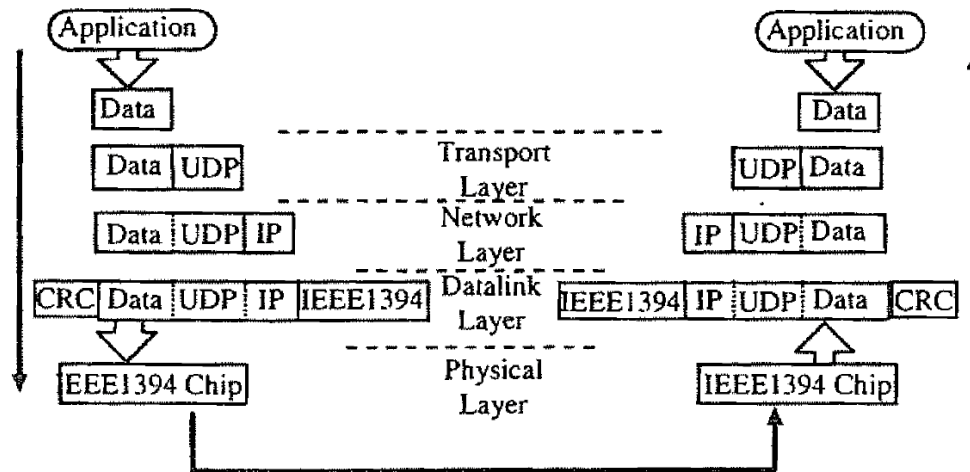


Fig. 4 UDP/IP protocol suite.

Ex. 1005 at Fig. 4.

34. Independent claims 1 and 53 both recite, in relevant part, “... the first endpoint is configured to *generate encoded data*,” and “configured to *decode the encoded data to recover application data and control bits*.” Ex. 1001 at cls. 1 and 53 (emphasis added). For independent claims 1 and 53 in Ground 3, Petitioners rely solely on Yusairi. Petition at 38-50. Yusairi does not disclose “encoded data” or “decod[ing] the encoded data to recover... control bits.”

35. Yusairi does not disclose encoding (or decoding). Petitioners state that “Yusairi is encoding data by encapsulating it at SOPC Board A.” Petition at 43 (citing EX1003 at ¶¶151-152). But encapsulation as disclosed in Yusairi, is not encoding as disclosed in claim 1. Figure 4 of Yusairi (depicted above) shows the encapsulation and decapsulation process. See Ex. 1005 at Sec. 4 (“The protocol

stack we are going to implement is shown in Fig. 4 together with data encapsulation and decapsulation....”). Unlike encoding, encapsulation does not change the underlying bits. Rather, encapsulation repackages the data bits. This is confirmed by Ex. 1023 cited by Petitioners and Dr. Wolfe which states that “[e]ncapsulation is the computer-networking process of concatenating layer-specific headers or trailers with a service data unit (i.e. payload) for transmitting information over computer networks.” Ex. 1023 at 1. Encoding, on the other hand, changes the underlying bits by, for example, adding additional bits. This is confirmed by Ex. 1020 cited by Petitioners and Dr. Wolfe which states “8b/10b in a line code that maps 8-bit words to 10-bit symbols....” Ex. 1023 at 1. Accordingly Yusairi does not disclose that the first endpoint is “configured to generate encoded data” as recited in claim 1.¹

36. Claim 23 recites, in relevant part, “*encod[ing]... input words... [that are] indicative of application data and control bits*” and claim 68 recites, in relevant part, “*generat[ing]... input words, wherein the input words are indicative of application data and control bits...[and] encod[ing] the input words....*” Ex. 1001 at cls. 23 and 68. The combination of Yusairi and Shin does not disclose encoding

¹ Petitioners similarly separate out the claim language in its analysis of claim 53. Petition at 60-61. My analysis of claim 1 equally applies to claim 53.

or generating input words that include both application data and control bits as recited in claim 23 and claim 68.

37. Petitioners combine Yusairi and Shin as follows:

Shin discloses that a packet (cell) can be formed into codes (input words) that are encoded by block encoding into symbols (code words). A POSITA would have understood that when Yusairi's packet having application data (IP data) and control bits (transaction code and type field) are encoded using Shin's block code, the application data and control bits from the packet (cell) would have been placed into codes (input words) before being encoded into symbols (code words). [] Thus, by applying Shin's block encoding to Yusairi's packets, the codes (input words) of each packet (cell) would be indicative of application data and control bits.

Petition at 54-55.

38. As explained above, however, Shin teaches encoding data at the link layer—Shin does not teach encoding control bits (i.e., control symbols). A POSITA would readily understand that the control symbols in Shin are added to the sequence of codewords after the data is encoded. *See* Ex. 1004 at Fig. 2; *id.* at [0077] (“selects symbols encoded from codes provided by the transport layer **or** symbols generated by the control symbol generator” and “effectively inserts control symbols and synchronization symbols into the sequence of symbols that are to be transmitted.”) (emphasis added). Accordingly, Shin's encoding scheme is only applied to the data, not to the control symbols. Therefore I disagree with Petitioners and Dr. Wolfe that

Shin discloses or renders obvious the “encoding” limitations of claims 23 and 68. Exhibit 1003 at ¶¶ 187-188.

39. If Shin’s encoding scheme were applied to Yusairi, a POSITA would recognize that the same conclusion would result. Shin’s encoding scheme would be applied to the “Data” of Yusairi at the link layer, encoding only data, not control bits. Therefore, the combination of Yusairi and Shin does not result in encoding or generating input words that include both application data and control bits as required in claims 23 and 68.

40. Petitioners’ and Dr. Wolfe argue that “[a] POSITA would have been motivated to use Shin’s block encoding methods to encode Yusairi’s packets because Shin’s block encoding methods... would have provided Yusairi with known communication protocols having a neutral DC component to help ensure signal is accurately received and decoded by synchronizing the SOPC Board B receiver with the SOPC Board A transmitter.” Petition at 51; Ex. 1003 at ¶ 177. But that is just a benefit of Shin’s block encoding scheme generally and has nothing to do with encoding control bits. It also does not address how or why a POSITA would apply Shin’s encoding scheme to control bits when Shin expressly teaches that control bits are not encoded. As I explained above, Shin teaches that control symbols are added

Declaration of William Mangione-Smith
Inter Partes Review IPR2024-01429
U.S. Patent No. 7,187,307

to the transmission sequence *after* the data is encoded. Accordingly, a POSITA would not utilize Shin's block encoding method to encode control bits.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, undersection 1001 of Title 18 of the United States Code.

Date: January 31, 2025

A handwritten signature in black ink, appearing to read "William H. Mangione-Smith", with a long horizontal flourish extending to the right.

Dr. William Mangione-Smith