UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

UNIVERSAL CONNECTIVITY TECHNOLOGIES INC., Plaintiff, v. LENOVO GROUP LIMITED, Defendant.	Case No. 2:23-cv-00449-JRG

DEFENDANT'S INVALIDITY AND ELIGIBILITY CONTENTIONS

Pursuant to the Court's Patent Rules, Standing Order Regarding Subject Matter Eligibility Contentions, and Docket Control Order (Dkt. No. 27), Defendant Lenovo Group Limited respectfully submits these invalidity and eligibility contentions with respect to the asserted claims of U.S. Patent Nos. 7,154,905 ("the '905 Patent"), 7,187,307 ("the '307 Patent"), 7,746,798 ("the '798 Patent"), 9,232,265 ("the '265 Patent"), 8,680,712 ("the '712 Patent"), 7,856,520 ("the '520 Patent"), 7,921,231 ("the '231 Patent"), and 9,852,103 ("the '103 Patent") (collectively, the "Asserted Patents") identified by Plaintiff Universal Connectivity Technologies Inc., ("UCT" or "Plaintiff") in its May 15, 2024 Patent Rule 3-1 Disclosures and July 3, 2024 Notice Regarding Claim Reduction (together, "Infringement Contentions").

The currently Asserted Claims, as reflected in Plaintiff's Infringement Contentions, are:

- '905 Patent: Claims 1, 8, 12, 15, 16, 17, 21, 22, 23, 26
- '307 Patent: Claims 1, 7, 23, 31, 53, 68, 71, 72, 74, 75
- '798 Patent: Claims 11, 19, 20, 21, 22, 23, 24, 25, 26, 28

- ’265 Patent: Claims 1, 8, 11, 14, 16
- ’712 Patent: Claims 1, 2, 5, 7, 9
- ’520 Patent: Claims 1, 4, 8, 9, 12, 13, 15, 18, 19, 25
- ’231 Patent: Claims 1, 2, 10, 11, 12, 13, 14, 16, 17, 18
- ’103 Patent: Claims 1, 2, 3, 11, 12, 13, 17, 20, 21, 22

As detailed further below, the asserted claims of each Asserted Patent are anticipated by and/or obvious in view of one more of the prior art references being produced concurrently pursuant to 35 U.S.C. § 102 and/or § 103, are directed to ineligible subject matter under 35 U.S.C. § 101, and are otherwise invalid under 35 U.S.C. § 112.

I. PRELIMINARY STATEMENT

These invalidity contentions and eligibility contentions are based on Defendant’s current knowledge, understanding, and belief of the Asserted Patents and prior art, of Plaintiff’s infringement theories (inasmuch as they can be inferred from its Infringement Contentions), and of the facts and other information available as of the date of these contentions. Defendant’s investigation, discovery, and analysis of information related to this action is ongoing. Additional discovery, elucidation of Plaintiff’s impermissibly vague infringement contentions, Plaintiff’s expert report(s) regarding infringement, and/or orders of the Court may require Defendant to amend or supplement these invalidity contentions and eligibility contentions, and Defendant expressly reserves the right to do so, subject to the Court’s procedures, as the case proceeds. These contentions represent Defendant’s good-faith effort to provide a comprehensive identification of prior art relevant to this case, but Defendant reserves the right to modify or supplement its prior art list and invalidity contentions and eligibility contentions at a later time with, or based upon, pertinent information that may be subsequently discovered.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 2

In addition to the prior art that charted in the attached exhibits, additional background references are discussed herein and/or included in the document production accompanying these Invalidity and Eligibility Contentions. Defendant reserves the right to rely on these background references for any purpose including, for example, to demonstrate the knowledge of a POSITA at the relevant time.

To the extent UCT believes anything in these contentions (including the attached claim chart exhibits and accompanying document production) are insufficient, Defendant invites UCT to bring such issues to its attention as soon as reasonably possible.

A. No Waiver

Nothing in these contentions is intended, nor should be construed, as a waiver of any non-infringement position or argument under 35 U.S.C. §§ 101 or 112. To the contrary, as set forth herein, Defendant contends that all Asserted Claims are invalid pursuant to 35 U.S.C. §§ 101 and/or 112. Defendant's statements herein (including the accompanying claim charts) reflect Defendant's present understanding of the purported scope of the claims as alleged by Plaintiff in its Infringement Contentions (as best those contentions can be understood in light of their present deficiencies).

The patent claims have yet to be construed. As a result, Defendant has based these contentions upon its knowledge and understanding of the potential scope of the Asserted Claims at this time, and, in part, upon the apparent interpretations of the Asserted Claims advanced by Plaintiff in its Infringement Contentions. Defendant may disagree with Plaintiff's interpretation of the meaning of many terms and phrases in the Asserted Claims. Defendant has provided these contentions based in part on its present understanding of Plaintiff's apparent constructions and interpretations of the Asserted Claims. These contentions do not represent Defendant's agreement or view as to the proper interpretation of any claim term contained therein. Any similarity between

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 3

any apparent claim interpretation in any of Defendant's charts of prior art references and Plaintiff's contentions is not an admission or agreement with Plaintiff about the meaning of any claim term, but rather a reflection of the fact that the subject matter Plaintiff believes is claimed is present in the prior art, or that the claims are otherwise invalid. These contentions are made in the alternative, and should not be interpreted to rely upon, or in any way affect, the non-infringement arguments Defendant may assert in this case. Defendant reserves the right to amend, supplement, or materially modify these contentions as the case proceeds, including to identify additional prior art and/or additional bases for invalidity under 35 U.S.C. §§ 101 and/or 112. Defendant also reserves the right to amend, supplement, or materially modify its contentions based on any infringement and/or additional claim construction positions that Plaintiff may take in this case.

Defendant also reserves the right to amend, supplement, or materially modify its contentions in response to any claim construction or interpretation positions that Plaintiff may take or based on any claim construction the Court may further adopt in this case. Defendant also reserves the right to assert that a claim is indefinite, not enabled, or fails to meet the written description requirement of 35 U.S.C. § 112 based on any claim construction or interpretation position Plaintiff may take in this case or based on any claim construction the Court may further adopt in this case.

B. No Admission

Nothing disclosed herein is an admission or acknowledgement that any product accused of infringement by Plaintiff in its Infringement Contentions (the "Accused Products"), or any of Defendant's other products or services, infringes any of the Asserted Claims.

Defendant further notes that Plaintiff appears to rely upon overly broad interpretations of the Asserted Claims. At the same time, Plaintiff's Infringement Contentions are in most places too general and vague to discern Plaintiff's infringement theories and how exactly Plaintiff

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 4

contends each Accused Product meets or practices each element of the Asserted Claims. As a result, Defendant has been prejudiced in its ability to prepare these contentions. In addition, Plaintiff's Infringement Contentions, in many cases, continue to fail to put Defendant on notice of Plaintiff's interpretation of the Asserted Claims, further prejudicing Defendant's ability to identify relevant prior art.

Patent Rule 3-1(d) required Plaintiff to identify "each element of each asserted claim" that is alleged to be present under the doctrine of equivalents. In its Contentions, Plaintiff identified no specific claim elements as allegedly being present under the doctrine of equivalents. In preparing these invalidity and eligibility contentions, Defendant has relied on Plaintiff's representation that it has no doctrine of equivalents theories for any specific claim element, and any attempt by Plaintiff to present an untimely doctrine of equivalents argument or allegation would be severely prejudicial to Defendant. To the extent Plaintiff attempts to or is later permitted by the Court to amend its contentions to pursue any currently undisclosed doctrine of equivalents theories for additional claim elements, Defendant expressly reserves the right to supplement or amend these contentions to account for such amendments.

To the extent that any of the prior art references discloses the same functionality or feature of any of the Accused Products, Defendant reserves the right to argue that said feature or functionality does not practice any element of any of the Asserted Claims, and to argue, in the alternative, that if said feature or functionality is found to practice any element of any of the Asserted Claims, then the prior art reference demonstrates that the element is not novel, is obvious, and/or is otherwise not patentable.

Attached hereto are representative claim charts that identify examples of where the elements of the Asserted Claims may be found in the prior art and further identifying why those

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 5

claims are not novel or non-obvious. Defendant's claim charts cite particular teachings and disclosures of the prior art as applied to features of the Asserted Claims. Providing citations to portions of the prior art references should not be construed to mean that other portions of the prior art references are not also relevant to the validity of the claims. Other passages of the identified prior art may additionally disclose, either expressly or inherently, information relevant to the validity of one or more elements of the Asserted Claims. And, persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, Defendant reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony to establish the state of the art and to aid in understanding and interpreting the cited portions, as providing context thereto, showing reasons to combine references and as additional evidence that the prior art discloses a claim limitation. Defendant further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish bases for combinations of certain cited references that render the asserted claims obvious. Defendant also reserves the right to rely on uncited portions of the prior art references that describe substantially the same functionality or features that are described in cited portions. Further, for any combination, Defendant reserves the right to rely on information generally known to those skilled in the art and/or common sense.

Where Defendant cites a particular drawing or figure in the accompanying charts, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not itself expressly cited). Similarly, where Defendant cites particular text concerning a drawing or figure in the accompanying charts, the citation encompasses that drawing or figure (even if the associated drawing or figure is not expressly cited).

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 6

The references cited in the attached claim charts may disclose the limitations of the Asserted Claims expressly and/or inherently. Defendant may rely on inherency to demonstrate the invalidity of the Asserted Claims. Moreover, certain prior art references and solutions may inherently anticipate certain features of the asserted claims as construed by Plaintiff. Defendant may rely on cited or uncited portions of the prior art, other documents, and expert testimony to establish the inherency of certain features of the prior art to invalidate the Asserted Claims. Defendant also may rely on any reference identified in these contentions or any other reference to prove that the references are enabling, to provide a reason to combine the references, as an indication of the state of the art, or to explain the meaning of a term used in any reference.

The suggested obviousness combinations may be presented in conjunction with or in the alternative to Defendant's contentions regarding anticipation. These obviousness combinations should not be construed to suggest that any reference included in any combination is not anticipatory in its own right. Further, to the extent that Plaintiff contends that any of the references identified does not constitute prior art under 35 U.S.C. § 102, Defendant reserves the right to rely upon other prior art references in the same patent family with substantially identical disclosures as evidence of invalidity based on the same theories as those disclosed below.

Throughout the charts, Defendant provides exemplary citations indicating where the cited references disclose subject matter recited in the preambles of the claims, without regard to whether the preambles are limitations of the claims. Defendant does not take any position at this time regarding whether or not the preambles of the Asserted Claims are limitations, and will address this topic, if necessary, during the scheduled claim construction process.

With regard to the prior art that Defendant identifies as rendering the Asserted Claims obvious, non-limiting examples of the reasons why the prior art renders the Asserted Claims

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 7

obvious, including exemplary identification of combinations of prior art showing obviousness, are provided below. Generally, for all prior art combinations addressed herein, a reason or motivation to combine the prior art includes that each prior art reference is relevant to data communications and/or power distribution between devices, and one of ordinary skill in the art tasked with implementing such a system would have been motivated to investigate the various existing systems, patents, and other publications, including those identified herein, to address his or her particular needs. The combinations and modifications of the prior art to invalidate the Asserted Claims would have arisen from ordinary innovation, ordinary skill, or common sense and/or would have been obvious to try or otherwise predictable in the field of data communications and/or power distribution between devices.

A person having ordinary skill in the art would have had a reason to combine the prior art based on the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons having ordinary skill in the art. For example, each of the prior art references is relevant to data communications and/or power distribution between devices, including addressing problems such as symbol alignment, device and signal negotiation, and power provision. In addressing these problems, one of ordinary skill in the art would have been motivated to combine the teachings of research in the field.

Additionally, some prior art references cite or discuss other prior art references, illustrating the close technical relationship among the prior art. To the extent that any prior art reference refers to or discusses another prior art reference, either expressly or inherently, it would have been obvious to combine those references for at least that reason.

As shown in the accompanying claim charts, numerous books and research papers show that methods were being used to streamline packetized data transmission and power distribution

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 8

across device-to-device connections. Design incentives and other market forces would have prompted combinations and modifications of the prior art. Design needs and market pressures provide ample reason to combine prior art elements in the manner combined. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007). Defendant reserves the right to supplement these discloses if such evidence of design needs and/or market pressures become apparent through discovery in this case.

Moreover, the Asserted Claims are also obvious because they merely arrange old elements, with each performing the same function that had been known, to perform and yield no more than what one having ordinary skill in the art would expect from such an arrangement.

Because there were a finite number of predictable solutions in the art of packetized data transmission and power distribution across device-to-device connections with regard to any claimed feature, it would have been obvious to a person of ordinary skill in the art to pursue the known options. A person skilled in this art would have been familiar with all the claim elements that the patentees used to distinguish the prior art during prosecution. The identified prior art references merely use those familiar elements for their primary or well-known purposes and in a manner well within the ordinary level of skill in the art. Accordingly, common sense and the knowledge of one having ordinary skill in the art render the Asserted Claims invalid.

C. Reservation of Rights

Prior art not currently included in this disclosure may become relevant. Defendant is currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Defendant or contend that prior art identified by Defendant does not qualify as prior art. Defendant reserves the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device or method obvious or show that the allegedly missing limitation would have been known

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 9

or readily apparent to one of ordinary skill in the art at the time of the invention in light of the disclosure of the prior art at issue or other prior art. Defendant further reserves the right to rely on any of the references produced concurrently with these contentions in order to demonstrate the state of art at the alleged times of invention and as evidence of the knowledge of one of ordinary skill in the art[1] in support of any motivations to modify or combine the charted prior art references with other references or knowledge.

To the extent that Defendant charted a published patent application that later issued as a patent that includes substantially the same disclosure, Defendant contends that the issued patent discloses the claims for at least the same reasons explained in connection with the published application and Defendant reserves its rights to rely on the issued patent to establish invalidity. Similarly, to the extent that Defendant charted an issued patent the application for which was previously published (and which contains substantially the same disclosure), Defendant contends that the published application discloses the claims for at least the same reasons explained in connection with the issued patent and Defendant reserves the right to rely on the published application to establish invalidity (including to establish an earlier prior art date).

Consistent with the Patent Rules and Docket Control Order (Dkt. No. 27), and in view of the following, Defendant reserves the right to supplement or otherwise amend these Invalidity and Eligibility Contentions. This is particularly true for all claims for which Plaintiff has not provided adequate infringement contentions.

Plaintiff may also be aware of additional prior art that is not known to Defendant. To the extent Plaintiff produces additional prior art responsive to Defendant's discovery requests after

[1] For purposes of these Invalidity and Eligibility Contentions, the term "general knowledge" includes the common knowledge and common sense of a POSITA as well as the general knowledge of POSITAs in the field.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 10

these contentions are served, Defendant may supplement its Invalidity and Eligibility Contentions with prior art contained in such production once it has had a fair opportunity to review, analyze, and chart such prior art. Defendant reserves the right to amend its Invalidity and Eligibility Contentions with any additional potential prior art known by Plaintiff but not yet disclosed to Defendant.

Defendant provides these Invalidity and Eligibility Contentions only for the claims that are asserted by Plaintiff, but reserves the right to seek invalidation of all claims in each of the Asserted Patents.

In addition to the prior art that is set forth in the charts, additional prior art references are being produced concurrently with these contentions. This additional art may be relevant to the validity of the Asserted Claims depending on the positions taken by Plaintiff, and in any event may be referenced to show the state and evolution of technology in these fields. Accordingly, for the foregoing reasons, Defendant reserves the right to supplement these Invalidity and Eligibility Contentions with specific claim charts and obviousness combinations with the additional references based on the allegations and contentions asserted by Plaintiff as these allegations and corresponding constructions of the claims become clear.

D. Ongoing Investigation

Defendant's investigation is ongoing, and Defendant expressly reserves the right to amend its disclosures and document production to account for evidence uncovered as its investigation continues. Such amendments include identifying and relying on additional references that may result from Defendant's further search and analysis. Defendant reserves the right to supplement these contentions in light of any additional prior art of which Plaintiff is aware and has not disclosed to Defendant in discovery, or that might be subsequently disclosed by Plaintiff in response to Defendant's discovery requests. An example of such prior art may include products

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 11

sold and offered for sale by Silicon Image and/or Lattice Semiconductor. Such products may have been offered for sale or publicly shown in a manner that renders them prior art under 35 U.S.C. §§ 102 and 103. Defendant reserves the right to supplement these contentions to rely on those and other products from Plaintiff. Defendant's investigation into prior art systems and products is ongoing, and Defendant reserves the right to amend these contentions to reflect the identification of and information about such systems and products learned through discovery.

Defendant anticipates issuing subpoenas to third parties believed to have knowledge, documentation and/or corroborating evidence concerning some of the prior art listed herein and/or additional prior art. These third parties include, but are not limited to, the authors, employers of authors, inventors, assignees, or former or current employees of assignees or previous assignees, of the references identified in these Invalidity and Eligibility Contentions. For example, Defendant anticipates issuing subpoenas to potential prior artists including but not limited to individuals and entities responsible for the development of prior art systems identified in these Invalidity and Eligibility Contentions. Defendant reserves the right to supplement these contentions in light of any newly discovered information produced by these or other companies from which Defendant may seek discovery.

E. Incorporation by Reference

Defendant hereby incorporates by reference all arguments made in all IPR petitions filed by any party or third party (and all Institution Decisions instituting IPR relating to such petitions) challenging any Asserted Claim, including any IPR petition or decision instituting IPR that is filed after the date of these contentions. Defendant further incorporates by reference the file history of each Asserted Patent and the prior art cited therein.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 12

II. PRIORITY DATE OF THE ASSERTED PATENT CLAIMS

Plaintiff asserted the following priority dates for the Asserted Claims in its Infringement Contentions:

Asserted Patent	"Priority Date"
'905 Patent	"at least a priority date of November 22, 2000"
'307 Patent	"at least a priority date of June 12, 2003"
'798 Patent	"at least a priority date of November 22, 2000"
'265 Patent	"at least a priority date of March 31, 2011"
'712 Patent	"at least a priority date of December 11, 2008"
'520 Patent	"at least a priority date of January 4, 2008"
'231 Patent	"at least a priority date of January 4, 2008"
'103 Patent	"at least a priority date of April 14, 2014"

It is Plaintiff's burden to show entitlement to its asserted priority dates, and Defendant asserts that Plaintiff has failed to meet that burden, at least because it discloses ambiguous "priority dates" qualified with the phrase "at least as early as." To the extent Plaintiff attempts to rely on a different date from the specifically enumerated "Priority Dates" listed above (i.e., under the "at least" language), Defendant reserves the right to supplement these contentions. Moreover, because discovery has not yet been completed, Defendant has relied on Plaintiff's assertions for the purposes of identifying relevant prior art in these Invalidity and Eligibility Contentions, but Defendant does not concede that those priority dates are accurate. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions should discovery reveal that Plaintiff is not entitled to the asserted priority date. In addition, Defendant also reserves the right to supplement these contentions should Plaintiff subsequently attempt to amend its infringement

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 13

contentions in any way, or to otherwise modify its infringement allegations or seek to establish an earlier date of invention.

III. THE ASSERTED CLAIMS OF THE '905 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits A-1 through A-6, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '905 Patent.

1. The '905 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '905 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit A-1 through A-6 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art ("POSITA").

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '905 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '905 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 14

a) Prior Art Patents and Applications[2]

Number	Published/Issued Date	Short Name	Exhibit Number
UK Patent App. No. GB 2344029	May 24, 2000	Banes	A-1
U.S. Patent No. 4,542,380	September 17, 1985	Beckner	A-2
U.S. Patent No. 5,557,608	September 17, 1996	Calvignac	A-3
U.S. Patent No. 5,845,085	December 1, 1998	Gulick	A-4
U.S. Patent No. 5,574,934	November 12, 1996	Mirashrafi	A-5
U.S. Patent No. 5,974,464	October 26, 1999	Shin	A-6

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '905 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not

[2] Where the accompanying charts cite a particular drawing or figure, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not by itself expressly cited). Similarly, where the accompanying charts cite particular text concerning a drawing or figure, the citation also encompasses that drawing or figure (even if the associated drawing or figure is not expressly cited).

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 15

specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

b) Prior Art Systems

On information and belief, the systems identified below were in public use, on sale, or otherwise available to the public before the priority date of the '905 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- G-Link chipset by HP (*e.g.*, HIPPI-6400, HIPPI-6400-SC, HIPPI-800).
- Alterra chipset ED8B10B
- Fast Ethernet devices, including those using 100-BASE chipsets employing IEEE 802.3u (*e.g.*, 100-BASE-TX, 100-BASE-FX, 100-BASE-T4)
- Fast Ethernet devices, including those using 100-BASE Chipset employing IEEE 802.z, or IEEE 802.ae. (*e.g.*, 1000-BASE-T, 1000-BASE-LX, 1000-BASE-CX, 1000-BASE-SX)
- Fibre Channel networks and devices
- Infiniband networks and devices
- 10GFC networks and devices
- Xaui

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 16

above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '905 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The '905 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '905 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits A-1 through A-6, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits A-1 through A-6 with each other, at least because these prior art references relate to data transmission methods and devices utilizing certain transmission schemes in the same field of endeavor and to solve similar problems. For example, the transmission schemes disclosed by the prior art include packet ordering, such as pausing, interrupting, prioritizing, and/or resuming paused transmissions of packetized data designed to solve a number of problems that were known in the art. *See, e.g.*,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 17

’905 Patent, 2:59-66 (“[e]xisting memory devices that are designed to support access patterns with a high temporal and spatial relationship may not be appropriate for uses having access patterns with a lower spatial relationship.”); 3:15-19 (“existing memory devices are not particularly suitable for many uses because the memory devices typically allow access by only one accessing device at a time and because the memory devices typically operate at different clock rates than the accessing devices.”); and 3:34-36 (“[e]xisting communications protocols, such as Fibre Channel, may have an unacceptable overhead for communicating with memory devices.”). Therefore, these references provide interrelated teachings and one of ordinary skill would have looked to the concepts in any of these references when attempting to solve the problems purportedly solved by the ’905 Patent, among other asserted patents.

Turning to the prior art, U.S. Patent No. 5,574,934 to Mirashrafi et. al (“Mirashrafi ’934”), issued on November 12, 1996, discloses a system for priority-based transmission of signals. Mirashrafi ’934 at Abstract. For instance, transmission of lower priority signals may be interrupted while signals of higher priority are transmitted before resumption of the lower priority signal transmission. *Id.* at 1:46-58. Signals may be transmitted in data packets over a communication link such as an ISDN channel. *Id.* at 71:11-23.

U.S. Patent No. 5,845,085 to Dale E. Gulick (“Gulick ’085”), issued on December 1, 1998, discloses a data-link controller for receiving and transmitting frames of serialized data over a data-link. Gulick ’085 at Abstract. Gulick ’085 specifically describes that data may often be transmitted or received in “packets” or “frames” of information. *Id.* at 1:17-25. Gulick ’085 further discusses the use of flag signals to mark states or conditions for the link controller transmitter or receiver. *Id.* at 2:18-44.

U.S. Patent No. 4,542,380 to Beckner, *et. al* ("Beckner '380"), issued September 17, 1985, discloses a method and apparatus for graceful preemption on a digital communications link. Beckner '380 at Abstract. A link controller is configured on a respective transmitting or receiving end of a communications link to interrupt and resume communications according to signals such as a "preemption signal" or "end preemption signal". *Id.* at 2:10-42.

U.S. Patent No. 5,974,464 to Shin, *et. al* ("Shin '464"), issued October 26, 1999, discloses a high speed digital interface for transmitting information (*e.g.*, video) over various transmission media. Shin '464 at Abstract. In particular, Shin '464 discloses an encoder and deserializer configured to distinguish encoded characters based on a number of logical transitions. *Id.* at 3:55-4:5. Shin '464 further discloses encoding and transmission of in-band and out-of-band characters such as control characters which can be distinguished from characters within the transmitted data stream. *Id.* at 9:49-10:8.

UK Patent Application No. GB 2,344,029 to David Banes ("Banes '029"), published on May 24, 2000, discloses a data communication network technique involving interruption of lower priority data packets such that higher priority packets can be transmitted. Banes '029 at Abstract. Banes '029 specifically discloses the use of priority flags, interrupt codes, and resumption codes in order to facilitate preemption and resumption of lower priority transmissions until higher priority packets are sent. *Id.* at 11:18-12:18.

U.S. Patent No. 5,557,608 to Calvignac et. al ("Calvignac '608"), issued September 17, 1996, discloses a method and apparatus for preempting low-priority traffic in favor of high-priority traffic transmission. Calvignac '608 at 2:25-38. Calvignac '608 discloses transmission of pieces of data in packets with headers used by each node of a packet switching network to send packets

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 19

toward their destination. *Id.* at 3:13-27. Calvignac '608 further discloses the use of byte aligned flags to signify starting and ending preemption. *Id.* at 4:44-49.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

To the extent that it is determined that any of the above references do not disclose a particular claim element, a person skilled in the art would have been motivated to combine any of the above references (as documented in the claim charts attached as Exhibits A-1 through A-6). In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to data transmission methods and devices utilizing certain transmission schemes.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 20

problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards data transmission methods and devices utilizing certain transmission schemes, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

For example, to the extent that it is determined that any of the above references do not disclose the general concept of preempting and resuming data transmission as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934, Beckner '380, Calvignac '608, and Banes '029. As demonstrated in the attached claim charts for these references, each discloses preemption of data transmission on the basis of, *e.g.*, priority as was well known in the art at the time of the '905 filing. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose transmitting or receiving "packets" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934, Gulick '085, Calvignac '608, and Banes '029. As demonstrated in the attached claim charts for these references, each discloses transmission of data in various container formats including packets. For instance, Gulick '085 describes common data-link transmission in

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 21

"packets" or "frames" of information. Gulick '085 at 1:17-25. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose transmitting or receiving indicators such as a "preempt indicator" or "continue indicator" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Beckner '380, Banes '029, Calvignac '608, and Gulick '085. As demonstrated in the attached claim charts for these references, each discloses transmission of symbols or flags signifying preemption or resumption of data transmission. For instance, Beckner '380 describes a link controller for graceful preemption of data using characters such as "PREEMP", represented in binary as "111111110." Beckner '380 at 4:18-52. Similarly, Banes '029 discusses a priority detector and interrupt device to facilitate packet interruption and resumption using an "interrupt code" and "resume code," respectively. Banes '029 at 11:18-12:18. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "in-band symbols" and "out-of-band symbols" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Shin '464, Beckner '380, Calvignac '608, Banes '029, and Gulick '085. As demonstrated in the attached claim charts for these references, each discloses symbols or characters including those that are in-band and out-of-band. For instance, Shin '464 describes "selected out-of-band characters easily distinguishable from in-band characters." Shin '464 at 14:37-62. Similarly, Beckner '380 describes a link controller for graceful preemption of data using characters such as

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 22

"PREEMP," represented in binary as "111111110." Beckner '380 at 4:18-52. As discussed in the '905 Patent, in-band and out-of-band symbols may be distinguished by the number of bit transitions occurring in their binary representation. '905 Patent at 24:33-46. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "primitives" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Mirashrafi '934 and Shin '464. As demonstrated in the attached claim charts for these references, each discloses symbols or characters including in-band and out-of-band. For instance, Mirashrafi '934 describes a "set of primitives" such as "comm primitives" implemented for API calls. Mirashrafi '934 at 28:61-65. In addition, transmitting primitives for the purpose of communication and synchronization between networked components was well known in the art at the time of the '905 filing. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose a "header that is transmitted only once" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Calvignac '608, Mirashrafi '934, and Banes '029. As demonstrated in the attached claim charts for these references, each at least inherently discloses a header that is initially transmitted and is not repeated upon continuation of the packet transmission. For instance, Calvignac '608 at Fig. 5 depicts a first packet of data with a packet header, a second packet with a packet header, and the continuation of the first packet data without repeating the header. As discussed in the '905

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 23

specification, merging segmented packets of the same transaction would have been appreciated by a POSITA as a way to efficiently transmit packet switched data. '905 Patent at 13:18-39. Additionally, Mirashrafi '934 noted that it would be desirable for a computing system to avoid "being inundated with subsequent signal packets it may not be able to handle." *See* Mirashrafi '934, 78:9-15. To address this issue, Calvignac '608 provides a first packet of data with a packet header, a second packet with a packet header, and the continuation of the first packet data without repeating the header, to achieve the technological improvements contemplated by the existing prior art and the '905 Patent. Therefore, a POSITA would be motivated to make such a modification and/or combination.

In addition, one of ordinary skill in the art would have been motivated to combine the prior art references. One of skill in the art would have would have been motivated to combine these references: (1) by their education, knowledge, and experience; (2) by the state of the prior art as a whole; (3) by the nature of the problem to be solved; (4) by common sense and ordinary ingenuity; and (5) by a desire to create a device, system, and method of controlling communication of computer data. Moreover, one of ordinary skill in the art would have been well-equipped with sufficient education, knowledge, and training to make the specific combinations with a reasonable expectation of success given the simplicity of the electrical components to one of ordinary skill in the art, the predictability of the arts, and the minimal level of experimentation needed to combine the various teachings.

One of skill in the art, seeking to solve these problems, would have looked to analogous art to identify ways to solve the problem. Indeed, the solution identified by the patentee had already been identified by others in the field, and one of ordinary skill in the art would have been motivated to combine such analogous teachings in the same manner proposed by the patentee. Additionally,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 24

one of skill in the art would have had a reasonable expectation of success because the references contained analogous teachings to those proposed by the patentee, the references describe relatively simple electrical technologies in predictable fields, and the modifications and combinations would not require undue experimentation. As such, one of skill would have been motivated to combine the references.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the ’905 Patent:

- Mirashrafi ’934 alone or in combination with Beckner ’380
- Mirashrafi ’934 alone or in combination with Shin ’464
- Calvignac ’608 alone or in combination with Beckner ’380
- Calvignac ’608 alone or in combination with Shin ’464
- Banes ’029 alone or in combination with Shin ’464

B. Invalidity of the ’905 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’905 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that the Asserted Claims of the ’905 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- “the out-of-band symbols are not transition optimized.” (claim 3, 10, 17, and 23)
- “signals the transmission component to continue transmitting the first packet” (claim 21)

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 25

not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

C. Invalidity of the '905 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '905 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '905 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- "the indicators include one or more out-of-band symbols" (claims 1, 8, 15, and 21)
- "[the] packets include [one or more] in-band symbols" (claims 1, 15, and 21)
- "transition optimized." (claim 3, 10, 17, and 23)
- "the symbols of the packets include in-band symbols" (claim 8)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with or broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, at least claim 21 (and its dependent claims) of the '905 Patent recites functions without sufficient structure for performing the function, thus invoking 35 U.S.C. § 112,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 26

¶ 6. Because the specification of the '905 Patent also does not recite structure for performing the function, the following terms are invalid as indefinite under 35 U.S.C. §§ 112, ¶ 2:

- "a transmission component that transmits a first packet" (claim 21)
- "a preemption component that signals the transmission component to stop transmitting the first packet, transmits a preempt indicator indicating that a second packet is to be transmitted, transmits the second packet, and signals the transmission component to continue transmitting the first packet" (claim 21)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

IV. THE ASSERTED CLAIMS OF THE '307 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits B-1 through B-8, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '307 Patent.

1. The '307 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '307 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit B-1 through B-9, or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 27

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '307 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '307 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications[3]

Number	Published/Issued Date	Short Name	Exhibit Number
WO1992/09162	May 29, 1992	Hornak	B-1
U.S. Patent Appln. No. 2002/0114348	August 22, 2002	McCrosky	B-2
U.S. Patent No. 5,313,458	May 17, 1994	Suzuki	B-3
U.S. Patent No. 6,584,535	June 24, 2003	Ouellet	B-4
International Pub. No. WO 01/58107	January 24, 2002	Azizoglu	B-5
U.S. Patent No. 4,486,739	December 4, 1984	Franaszek	B-6
European Patent No. EP 0,938,211	August 25, 1999	Blanc	B-6
U.S. Patent Appln. No. 2002/0159450	October 31, 2002	Shin '450	B-7

[3] Where the accompanying charts cite a particular drawing or figure, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not by itself expressly cited). Similarly, where the accompanying charts cite particular text concerning a drawing or figure, the citation also encompasses that drawing or figure (even if the associated drawing or figure is not expressly cited).

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 28

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
PCI-SIG	PCI Express Base Specification Revision 1.0	April 29, 2002	PCI 1.0	B-8
IEEE	802.3z Specification	March 8, 2002	802.3z	B-9

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '307 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

c) Prior Art Systems

On information and belief, the systems identified below were in public use, on sale, or otherwise available to the public before the priority date of the '307 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 29

right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- G-Link chipset by HP (*e.g.*, HIPPI-6400, HIPPI-6400-SC, HIPPI-800).
- Alterra chipset ED8B10B
- Fast Ethernet devices, including those using 100-BASE chipsets employing IEEE 802.3u (*e.g.*, 100-BASE-TX, 100-BASE-FX, 100-BASE-T4)
- Fast Ethernet devices, including those using 1000-BASE Chipset employing IEEE 802.3z, IEEE 802.3ab, or IEEE 802.3ae. (*e.g.*, 1000-BASE-T, 1000-BASE-LX, 1000-BASE-CX, 1000-BASE-SX)
- Fibre Channel networks and devices
- Infiniband networks and devices
- 10GFC networks and devices
- Xaui
- The Firewire IEEE 1394b switches (Ex. H-FWS).
- PCI Express 1.0 devices (Ex. H-PCI).

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the ’307 Patent, Defendant contends that any

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 30

difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The ’307 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the ’307 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits B-1 through B-9, or discussed in the incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits B-1 through B-9 with each other, at least because these prior art references relate to data transmission methods and digital communication devices and attempt to solve a common problem of improving data transmission and control. Moreover, one of ordinary skill in the art would have been well-equipped with sufficient education, knowledge, and training to make the specific combinations with a reasonable expectation of success given the simplicity of the electrical components to one of ordinary skill in the art, the predictability of the arts, and the minimal level of experimentation needed to combine the various teachings. Indeed, the patentee conceded the simplicity and conventional nature of the arts by providing that “[v]arious serial links for transmitting data and clock signals over various media . . . are well known.” *See, e.g.*, ’307 Patent, 1:47-50. Therefore, these references provide interrelated teachings and one of ordinary skill would have looked to the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 31

concepts in any of these references when attempting to solve the problems in the simple technical field described by the ’905 Patent, among other asserted patents.

As one example of a prior art reference used to address these problems, U.S. Patent application 2002/0159450 to Shin et al. (Application ’450), published October 31, 2002, discloses a serial communications architecture for communicating between devices. Application ’450 at Abstract. The communications on physical layer, link layer, and transport layer are disclosed in the network architecture. *Id.* at [0075-0081], Figs. 1, 2, 38A. Together with data signal, control signals are encoded, transferred, and decoded to perform control functions on multiple levels. *Id.* at [0128-0140], Fig. 2.

International Patent Application Pub. No. WO 92/09162 to Hornak et al. (“Hornak ’162”), published on May 29, 1992, discloses a method of data communication that involves adding additional bits to a data word that include an encoded master transition, data status indication, and a phantom bit indication. Hornak ’162 at Abstract and at p. 9 ll. 17-31. Hornak ’162 discloses that the phantom bit may be “a user definable bit, such as an additional data bit or some type of control or indicator bit desired by the user.” Hornak ’162 at p. 9 ll. 17-31, and that control “signals may convey additional information or they may be used to regulate the operation of the receiver itself.” Hornak ’162 at p. 2 ll. 21-23. Hornak ’162 incorporates by reference U.S. patent 5,022,051 (the ’051 patent) issued 1/4/1991 and U.S. Patent 4,926,447 (the ’447 patent) issued 5/15/1990.

U.S. Patent No. 5,313,458 to Hiroyuki Suzuki (“Suzuki ’458”), issued May 17, 1994, discloses a traffic control system 4 that connects to other traffic control systems that each connect to a subscriber system 2. Suzuki ’458 at Abstract and Fig. 1b. Suzuki ’458 discloses a traffic control system 4 operating on a frame consisting of a header and payload within the traffic control system 4 to perform a network level function of discarding packets when a C2 bit in the header is set.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 32

Suzuki ’458 at Abstract and at 6:9-32. Suzuki ’458 discloses the use of the C2 bit at the link layer function of allowing constant high rate communication between subscriber 2 and traffic control unit 4 by indicating empty frames with the C2 bit. Suzuki ’458 at 1:18-30.

U.S. Patent Application Pub. No. 2002/0114348 to McCrosky et. al (“McCrosky ’348”), published on August 22, 2002, discloses a system for receiving and transmitting from a switch to various endpoints using a link interface that uses an improved standard 8B/10B transmission code. McCrosky ’348 at [0118-119]. McCrosky ’348 discloses a J0 link level synchronization character that signals the switch to write the J0 Character into a FIFO and to use a set of counters to perform a synchronization operation for multiple endpoints within the switch. McCrosky ’348 at [0116-117]. McCrosky ’348 discloses the use of a J0 character to synchronize both at the character level and at the frame or link level. McCrosky ’348 at [0092-93].

U.S. Patent No. 6,584,535 to Ouellet, et. al (Ouellet ’535), issued June 24, 2003, discloses a configurable interconnect for use with high-speed electronic system components. Ouellet ’535 at Abstract. Physical layer, MAC layer, and L3 packet layer are included in the network. *Id.* at 1:52-61, 2:23-26, 5:21-28. The 8B/10B encoding method is used to encode control information into the data stream, controlling events of multiple levels. *Id.* at 6:30-12:18.

PCI Express Base Specification Revision 1.0 (PCIe v1), published April 29, 2002, discloses the PCI Express architecture in terms of three discrete logical layers: the Transaction Layer, the Data Link Layer, and the Physical Layer. PCIe v1 on p35-36. PCI Express uses the 8B/10B transmission code system to encode and transfer special symbols for framing and link management. *Id.* at p. 150-56.

802.3z Specification (802.3z), published March 8, 2002 by the IEEE, discloses the 802.3z architecture in terms of three discrete logical layers: the MAC client (Network, Transport, session,

presentation, and/or application layers), the Data Link Layer, and the Physical Layer. 802.3z, Section 3 at 33-34, Section 1 at 35. 802.3z uses the 8B/10B transmission code system to encode and transfer special symbols for idle and packet management. 802.3z, Section 3 at 45, 36.

International Patent Application Pub. No. WO 01/58107 to Azizoglu et al. ("Azizoglu '107"), published on August 9, 2001, discloses a method of encoding signaling information using Gigabit Ethernet, *e.g.* using 8B10B encoding. Azizoglu at Abstract and p. 2 ll. 18-24.

European Patent No. EP 0,938,211 to Blanc et al., ("Blanc '211"), Published October 25, 1999, discloses a switching architecture that uses 8b/10b coding. Blanc '211 at [0001]. Blanc '211 specifically describes the use of one of a set of three comma characters for the purposes of flow control. Blanc '211 at [0017].

U.S. Patent No. 4,486,739 to Franaszek et al. ("Franaszek '739"), issued on December 4, 1984, discloses a binary DC balanced code and an encoder circuit that forms an 8B/10B code. Franaszek '739 at ABSTRACT. Franaszek '739 discloses a control character such as 28.1, 28.5, or 28.7 that is singular, that is, has a COMMA property that it does not appear in data characters neither in individual characters nor in overlap between adjacent characters. Franaszek '739 at 9:2-14.

To the extent that it is determined that any of the above references do not disclose a particular claim element, a person skilled in the art would have been motivated to combine any of the above references (as documented in the claim charts attached as Exhibits B-1 through B-9). In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 34

known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to data transmission methods and digital communication devices.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards data transmission methods and digital communication devices, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Additionally, Hornak '162 describes a motivation of saving bits so that they are not required at a higher layers, by providing bits in the link layer header for an arbitrary higher level,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 35

or user level purpose. Hornak ’162 at p. 9 ll. 17-31. Since Shin ’450 discloses an indication of flow control such as flow control off (XOFF), Shin ’450 at [0069], it would have been obvious to combine Hornak ’162 with Shin ’450. Likewise, since McCrosky ’348 discloses the higher layer function of indicating payload type, McCrosky ’348 at [0002], it would have been obvious to indicate one of two payload types using the “phantom bit” of Hornak ’162. Furthermore, Suzuki ’458 discloses discarding bits at the Traffic Control System 4. Suzuki ’458 at 6:9-32. Additionally, since PCIe V1 discloses the higher level function of virtual channel indication for independent flow control, PCIe V1 at p. 282, it would have been obvious to indicate one of two virtual channels using the “phantom bit” of Hornak ’162. Ouellet discloses the higher layer function of indicating a flow control signal such as XON or XOFF. Ouellet ’535 at 6:30-12:18. Therefore, it would have been obvious to indicate XON or XOFF of Ouellet ’535 using the “phantom bit” of Hornak ’162. Blanc ’211 discloses the higher level function of a flow control indication by virtue of a COMMA character. Blanc ’211 at [0017]. Hence it would have been obvious to indicate a flow control indication using the “phantom bit” of Hornak ’162, since Blanc ’211 suggests signaling flow control. Azizoglu ’107 discloses flow control. Hence it would have been obvious to indicate a flow control indication using the “phantom bit” of Hornak ’162 since Azizoglu ’107 describes the signaling of flow control. 802.3z discloses flow control. 802.3z, Section 2 at 571. Hence it would have been obvious to indicate a flow control indication using the “phantom bit” of Hornak ’162.

Furthermore, Shin ’450 provides a motivation to combine Hornak ’162, or Shin ’450 with any functions which are performed by higher layer control signaling. Shin ’450 explains that doing so makes higher layer processing more time efficient by starting it earlier when the link layer header is received, and also makes the system more information efficient by not requiring that this information even be sent at a higher layer. Shin ’450 at [0096]. Hence, for the reasons stated above,

a POSITA would have been motivated to combine Hornak '162 with Shin '450, McCrosky '348, Suzuki '458, PCIe v1, Ouellet '535, Blanc '211, Azizoglu '107, or 802.3z. Similarly, a POSITA would have been motivated to combine Shin '450 with McCrosky '348, Suzuki '458, PCIe v1, Ouellet '535, Blanc '211, Azizoglu '107, or 802.3z.

Additionally, McCrosky '348 discloses a motivation to combine a reference that discloses 8B/10B coding with a reference which does not disclose 8B/10B encoding, in order to maintain DC balance on a serial link. McCrosky '348 at [0118-119]. Thus it would have been obvious to combine either Suzuki '458 or Hornak '162 with one or more of the references that disclose 8B/10B encoding, such as McCrosky '348, Shin '450, Blanc '211, PCIe V1, Ouellet '535 Franaszek '739, or Azizoglu '107.

Thus, to the extent that it is determined that any of the above references do not disclose a particular claim element, it would have been obvious to modify the teachings of that reference to include such element as taught in any other of the above references that discloses such element (as documented in the claim charts attached as Exhibits B-1 through B-9).

For example, to the extent it is determined that any of the above references do not disclose the general concept of generating encoded data in accordance with a line code, and transmitting the encoded data over the link to the second endpoint and/or encode M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where N>M/ transmit encoded data including the code words of the code word sequence over the link, it would have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Shin '450, McCrosky '348, Ouellet '535, PCIe v1, Blanc '211, Franaszek '739, 802.3z, and Azizoglu '107. As demonstrated in the attached claim charts for these references, each

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 37

discloses the use of a DC balancing using 8B/10B code words. Therefore, a POSITA would be motivated to make such a modification and/or combination to payload or application data.

As an additional example, to the extent it is determined that any of the above references do not disclose asserting a control signal indicative of at least another one of the control bits to higher level circuitry/performing at least one higher level function in response to the at least one control signal, it would have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Shin '450, Suzuki '458, 802.3z, and McCrosky '348. As demonstrated in the attached claim charts for these references, each discloses asserting a control signal indicative of at least another one of the control bits to higher level circuitry and performing at least one higher level function in response to the at least one control signal. For instance, Shin '450 describes at Shin '450 [0079] indicating to the transport layer when control symbols are received and thus identifying a packet type or performing flow control at the transport layer in response Shin '450 at [0097] and [0090]. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent it is determined that any of the above references do not disclose "control bits" have "multiple levels of communication protocol functionality" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Hornak '162, McCrosky '348, Shin '450, Suzuki '458, and Blanc '211. As demonstrated in the attached claim charts for these references, each discloses a link layer symbol with a function at a link layer and also a function that is performed at a layer above link layer. For instance, Suzuki '458 discloses a link layer C2 bit that results in frames being

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 38

discarded by the traffic control system 4. Suzuki ’458 at Abstract and at 6:9-32. Similarly Hornak ’162 discloses a phantom bit which performs the link layer function of defining a master transition, and which is provided to a user level to perform a user-definable function. Hornak ’162 at Hornak ’162 at p. 9 ll. 17-31, and at p. 2 ll. 21-23. Additionally Blanc ’211 discloses a set of three comma characters for the purposes of flow control. Blanc ’211 at [0017]. Therefore, a POSITA would be motivated to make such a modification and/or combination.

As an additional example, to the extent it is determined that any of the above references do not explicitly disclose “special characters, … none of the special characters of the encoded data matches a bit sequence of the code word sequence”/“none of the special characters of the encoded data matches a bit sequence of the code word sequence” as claimed, it would have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Franaszek ’739 at 9:2-14, McCrosky ’348, Ouellet ’535, PCIe v1, 802.3z, and Azizoglu ’107. As demonstrated in the attached claim charts for these references, each reference at least inherently discloses a header that is initially transmitted and is not repeated upon continuation of the packet transmission. For instance, McCrosky ’348 discloses a comma K28.5 character at Fig. 2 and [0075]. Likewise, Ouellet ’535 discloses the K28.5 character. Ouellet ’535 at [0011]. Furthermore, PCIe v1 discloses the K28.5 symbol. Azizoglu ’107 likewise teaches the use of a K-character. Azizoglu ’107 at p. 16, ll. 23-25. Similarly 802.3z discloses a K28.5 character. 802.3z, Section 3 at 45.

One of skill in the art, seeking to solve these problems, would have looked to analogous art to identify ways to solve the problem. Indeed, the solution identified by the patentee had already been identified by others in the field, and one of ordinary skill in the art would have been motivated

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 39

to combine such analogous teachings in the same manner proposed by the patentee. Additionally, one of skill in the art would have had a reasonable expectation of success because the references contained analogous teachings to those proposed by the patentee, the references describe relatively simple electrical technologies in predictable fields, and the modifications and combinations would not require undue experimentation. As such, one of skill would have been motivated to combine the references.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the ’307 Patent:

- Hornak alone or in combination with Suzuki ’458
- Hornak alone or in combination with McCrosky
- Hornak alone or in combination with PCI 1.0
- Hornak alone or in combination with Ouellet
- PCI 1.0 alone or in combination with Suzuki ’458
- Ouellet alone or in combination with Suzuki ’458
- Suzuki ’458 alone or in combination with McCrosky
- Shin ’450 alone or in combination with Hornak
- Shin ’450 alone or in combination with Suzuki
- Hornak, McCrosky, Suzuki ’458, Ouellet, Azizoglu, or Shin ’450 in combination with Franaszek
- Hornak, McCrosky, Suzuki ’458, Ouellet, Azizoglu, or Shin ’450 in combination with Franaszek, in further view of Blanc

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 40

B. Invalidity of the ’307 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’307 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, the Asserted Claims of the ’307 Patent are invalid at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. At least the following claim language is indefinite:

- “Multiple levels of communication protocol functionality” (claims 23 and 68)
- “Indicative of” (all asserted claims)

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

C. Invalidity of the ’307 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’307 Patent, to the extent such positions can be understood from Plaintiff’s Infringement

Contentions, Defendant asserts that the Asserted Claims of the ’307 Patent are invalid for reciting at least the following claim term:

- “Multiple levels of communication protocol functionality” (claims 23 and 68)
- “Indictive of” (all asserted claims)

These claim terms, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions, at least these claim terms are indefinite because they are inconsistent with and/or broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff’s apparent constructions of the claims, a POSITA at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

V. THE ASSERTED CLAIMS OF THE ’798 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits C-1 through C-8, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the ’798 Patent.

1. The ’798 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the ’798 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit C-1 through C-8 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 42

identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '798 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '798 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date	Short Name	Exhibit Number
U.S. Patent No. 5,592,487	Filed: Mar. 20, 1995 Issued: Jan. 7, 1997	Knecht	C-1
U.S. Patent No. 5,686,965	Filed: Sep. 18, 1995 Issued: Nov. 11, 1997	Auld	C-2
European Patent Application No. 1,137,278	Filed: Mar. 20, 2001 Pub'd: Sep. 26, 2001	Kotani	C-3
U.S. Patent No. 5,790,607	Filed: Nov. 28, 1995 Issued: Aug. 4, 1998	Burke	C-4
U.S. Patent No. 6,609,167	Filed: Mar. 15, 2000 Issued: Aug. 19, 2003	Bastiani	C-5
U.S. Patent No. 7,251,256	Filed: May 18, 2000 Issued: July 31, 2007	Barry	C-6
WIPO Patent Pub. No. 1999/023776	Filed: Oct. 31, 1997 Pub'd: May 14, 1999	Hui	C-7
U.S. Patent No. 5,917,830 U.S. Patent No. 6,430,230	Filed: Oct. 18, 1996 Issued: June 29, 1999 Filed: June 30, 1999 Issued: Aug. 6, 2002	Chen Cunningham	C-8

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 43

U.S. Patent No. 5,801,781	Filed: June 19, 1996 Issued: Sep. 1, 1998	Hiroshima	
WIPO Patent Pub. No. 2000/011831	Filed: Aug. 17, 1999 Pub'd: Mar. 2, 2000	Haartsen	
U.S. Patent No. 5,974,464	Filed: Sep. 30, 1996 Issued: Oct. 26, 1999	Shin	
U.S. Patent No. 6,498,568	Filed. Sep. 24, 1997 Issued: Dec. 24, 2002	Austin	

b) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '798 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- MPEG-2 Transport Stream
- Lightweight Medium Access Protocol ("LMAC")

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 44

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '798 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The '798 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '798 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits C-1 through C-8, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits C-1 through C-8 with each other, at least because all of these references relate to communication of packets between a transmitting device and a receiving device, and synchronization of such communication.

For example, U.S. Patent No. 5,592,487 ("Knecht") teaches that "[a] communications protocol is established with data packets, control packets, checksum packets, and synchronization symbols. One of the control packets is transmitted after a synchronization symbol is transmitted. One of the synchronization symbols, data packets, or checksum packets is transmitted after one of the control packets is transmitted. One of the synchronization symbols is transmitted after one of the checksum packets is transmitted, and one of the synchronization symbols or another of the data

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 45

packets is transmitted after one of the data packets is transmitted." Knecht, 2:3–13. Knecht further teaches that the "[c]ommunication protocol is established and maintained with four signals, namely: sync symbol, data packet, control packet, and checksum packet. In the preferred embodiment, control, data and checksum packets comprise 16 bits of information before encoding and 20 bits after encoding." *Id.* at 3:28–32.

Furthermore, U.S. Patent No. 5,686,965 ("Auld") teaches that "[a]n MPEG ISO system bitstream typically includes a sequence of packs 90. A typical pack 90, in turn, includes a sequence pack layer headers 92, a system header packet 94, a sequence of packets 96, 98, and 100, and an end code 102. The pack layer header 92 contains a pack start code, or sync code, used for synchronization purposes, and a system clock value. The system header packet 94 contains a variety of information commonly referred to as system housekeeping data, and a system stream ID which is used to differentiate among multiple system streams. A sequence of one or more packets typically contains either encoded audio or encoded video stream data. The final element of a pack 90 is an end code 102. It should be noted that any one packet 96, 98, 100 may carry either audio or video data, but not both simultaneously. With respect to a packet containing video data, typically a video packet header and one or more video frames is contained within the packet." Auld, 10:20–36.

Furthermore, European Patent Application No. 1,137,278 ("Kotani") teaches "the structure of a packet generated by a VCR. A sync pattern of about 2 bytes, which indicates the head of the packet, and an ID of about 3 bytes, which includes address information on data, are added to the packet." Kotani, ¶ 4. Kotani further teaches that "packets for commercialized household digital VCRs can be classified into two types, i.e., a 12-byte sub-code packet including a 2-byte sync pattern, and a 90-byte AV data packet including a 2-byte sync pattern." *Id.* ¶ 5. Kotani further

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 46

teaches that "[w]hen there are two types of time-division multiplexed HD data (for example, when there are a sub-code and AV data), it is necessary to add different sync patterns to the two types of data in order to discriminate between each type of data." *Id.* ¶ 35.

Furthermore, U.S. Patent No. 5,790,607 ("Burke") teaches that "for asynchronous data transmission and reception, it is highly desireable to organize the data into predetermined formats or packets for accurate and reliable data reception. In addition to providing the actual data, which is highly variable and essentially random, the data packet should also provide appropriate timing and synchronizing information needed for accurate data reception, without creating excessive overhead and without decreasing data throughput. In addition, for asynchronous data transmission and reception, an apparatus and method is also necessary to quickly, reliably and accurately detect such timing and synchronizing information prior to the reception of any actual data, without excessive or unnecessary processor complexity, speed, and cost." Burke, 2:38–51.

Furthermore, U.S. Patent No. 6,609,167 ("Bastiani") teaches that "a method for communicating serial data between a host computer and a peripheral device is disclosed. The packet for communication between the host computer and the peripheral device includes: (a) a synchronization field; (b) a packet type (PT) field following the synchronization field, the packet type field defining an error correction type for the packet; (c) a byte count (BC) field for defining a length of data for the packet; (d) a data type (DT) field for defining whether the data is one of link control, device control, and device data; (e) a data field; and (f) a CRC field for error checking the data in the data field." Bastiani, 2:29–39.

Furthermore, U.S. Patent No. 7,251,256 ("Barry") teaches that "[a]n LMAC-compatible link has the following characteristics: (a) the two devices at the endpoints of the link are not synchronized, e.g. the link is asynchronous; (b) the data transported on the link is in the form of

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 47

packets, cells, or frames; and (c) the MAC layer encoding of the data is such that devices called LMACs can insert synchronization symbols anywhere into the data stream at the ingress end of the link and remove them at the egress end so that the synchronization symbols are not visible to higher-layer components that process data packets." Barry, 3:61–4:3. Barry further teaches that "[i]n the LMAC protocol, the MAC layer encoding of the data is such that devices called LMACs can insert synchronization symbols anywhere into the data stream at the ingress end of an LMAC-compatible link and remove them at the egress end so that the synchronization symbols are not visible to higher-layer components that process data packets." Barry, 4:65–5:4.

Furthermore, WIPO Patent Publication No. 1999/023776 ("Hui") teaches that "[i]n data retrieval or communication systems, digital data or digitized multimedia information which can be, potentially, large or variable in size is normally packetized before storage or transmission. This process breaks the data into smaller packets where each packet contains one or more detectable synchronization patterns called sync-word, necessary information about the packet, and a payload of a smaller partition of the original data. The information about the packet may consist of a packet identification (ID), size of the payload contained in the current packet, timing information, and any necessary side information." Hui, 1:13–19.

Furthermore, U.S. Patent No. 5,917,830 ("Chen") teaches "the insertion of digital video messages such as commercials into a pre-existing compressed packetized data stream." Chen, 1:7–9. Chen further teaches that "a transport stream, or transport multiplex is made up of a contiguous set of fixed length packets. Each packet is 188 total bytes in length, with the first four of those bytes being defined as the packet header." *Id.* at 14:47–50. Chen further discloses that "[v]arious timing and identification information is provided in different portions of the transport stream. These include a packet identifier (PID) found in the transport header of each transport

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 48

packet" and "a program clock reference (PCR) which effectively represents a sample of the system time clock (STC) time base that underlies the service composed of the PIDs referenced in the service map." *Id.* at 14:57–59, 15:5–8.

Furthermore, U.S. Patent No. 6,430,230 ("Cunningham") teaches "a method of encoding payload bits for transmission over a communications link such that the running disparity of the transmitted symbol stream is constrained within a predetermined limit, and said payload bits comprising either data or control information." Cunningham, 1:58–63. Cunningham further teaches that "a data frame intended to be communicated over an optical fibre channel 20 typically comprises a binary digital message (payload) to be transferred between stations on the network; this message may comprise user data, or control information for managing operation of the network and its components." *Id.* at 2:65–3:3. Cunningham further teaches that "[c]ontrol information is conveyed by using selected n-bit data block values, together with a distinctive value of 10 for the pair of label bits a and b to indicate that the associated data block represents control information rather than actual data." *Id.* at 4:23–27.

Furthermore, U.S. Patent No. 5,801,781 ("Hiroshima") teaches "the details of the MPEG2-TS. Each packet of the MPEG2-TS has a prefix length of 188 bytes. The header 194 consists of four bytes and the payload 196 consists of 184 bytes. The header 194 is constructed by sync bytes 198, an error indicator 200, a unit start indicator 202, a transport priority 204, a packet ID 206, a scramble control 208, an adaptation field control 210, a continuity counter 212, and an adaptation field 214." Hiroshima, 10:51–58. Hiroshima further teaches "a process for forming the MPEG2-TS from the PES packet 82 by a multiplexing process." *Id.* at 11:13–14.

Furthermore, WIPO Patent Publication No. 2000/011831 ("Haartsen") teaches "a multi-part digital preamble for use in transmitting digital data packets. Advantageously, a preamble

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 49

according to the invention substantially reduces the overall length of DC-free sequences that are transmitted with each data packet in a digital FM system." Haartsen, 5:3–6. More specifically, Haartsen teaches that "a digital preamble can be strategically divided into three or more parts so that synchronization and other information can be included within the preamble while still enabling accurate DC estimation." *Id.* at 12:13–16.

Furthermore, U.S. Patent No. 5,974,464 ("Shin") teaches "a high-speed digital video signal transmission system in which high-speed video transmission is effected between a host computer system and a system display." Shin, 4:56–59. Shin further teaches that "various synchronization and other special characters are defined using the high-transition and low-transition sets of out-of-band characters. . . . The difference in the number of transitions between in-band and out-of-band characters allows selected out-of-band characters to serve as control characters, and to be readily distinguished from in-band characters within the transmitted data stream." *Id.* at 9:64–10:8.

Furthermore, U.S. Patent No. 6,498,568 ("Austin") teaches a "system [that] uses up to 5 pre-defined data packet sizes and up to 16 user defined data message types within each packet. Each packet has Forward Error Connection (FEC) and bit interleaving applied to it on transmission. Error checking is performed using a standard CRC. The system uses standard run in and byte synchronisation techniques. The byte synchronisation word used is 32 bits long and there are 5 different words used, one to identify each of the different packet types." Austin, 4:37–45.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 50

skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

For example, to the extent that it is determined that any of the above references do not disclose a "different synchronization symbol" for each "packet type," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Auld, 10:53–61 ("The packet data field of the packet layer 96 may contain emulations of the sync codes of other bitstream data, such as those comprising audio packets. The system synchronizer 62, however, analyzes the bitstream to determine whether a legitimate video packet sync code has been located, as at 126. If either the video sync code has not been located or a sync code emulation is located, the system synchronizer 62 will continue to predict the occurrence of a legitimate video sync code in the bitstream."); Kotani, ¶ 35 ("When there are two types of time-division multiplexed HD data (for example, when there are a sub-code and AV data), it is necessary to add different sync patterns to the two types of data in order to discriminate between each type of data."); Bastiani, 24:58–63 ("A packet type (PT) immediately follows the SYNC field of every ASP packet. A PT consists of a four bit packet type field followed by a four-bit check field as shown in FIG. 18. The PT indicates the type of packet and, by inference, the format of the packet and the type of error detection applied to the packet."); Hui, 13:6–7 ("The sync-word is defined based on applications or packet types, and is normally a digital pattern not easily found within the payload."); Chen, 14:56–15:3 ("Various timing and identification information is provided in different portions of the transport stream. These include a packet identifier (PID) found in the transport header of each transport packet to provide a reference number for identifying the transport packets carrying a specific service component. . . . Each type of packet will have a different PID identifying the packet type."); Cunningham, 4:23–27 ("Control

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 51

information is conveyed by using selected n-bit data block values, together with a distinctive value of 10 for the pair of label bits a and b to indicate that the associated data block represents control information rather than actual data."); Hiroshima, 11:16–22 ("The TS header 194 is formed in a manner such that the parameters such as error indicator 200 indicative of the presence or absence of the bit error in the packet, unit start indicator 202 indicating whether a new PES packet appears in the TS payload or not, packet ID 206 indicating whether the packet in the payload is video or audio . . . ."); Haartsen, 12:19–13:2 ("Thereafter, a synchronization part of the preamble, which is not necessarily DC free, but which is protected by code to prevent detection errors, can be used not only to synchronize detection of a data packet, but also to carry timing and/or other useful information (e.g., channel identification, destination address, time of day, user identification, etc.)."); Austin, 4:42–45 ("The byte synchronisation word used is 32 _bits long and there are 5_different words used, one to identify each of the different packet types."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Additionally, to the extent that it is determined that any of the above references do not disclose "synchronization information," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Burke, 3:41–48 ("In the preferred embodiment of the invention, data for transmission is organized into packets beginning with a 'preamble' 101 comprising a known, predetermined bit sequence, followed by a transition 102 comprising an indicator that data will follow, such as synchronizing information (a SYNC word preferrably having a high autocorrelation), followed by a data stream 103 having a variable length . . . ."); Hui, 13:6–9 ("The sync-word is defined based on applications or packet types, and is normally a digital pattern not easily found within the payload. After detection of the sync-word, the process checks at step 503 for the correct packet ID which may be

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 52

used to differentiate packets from different data sources, types, or versions."); Haartsen, 13:16–19 ("The synchronization word 520, which can include timing and/or other information and which is coded to protect against detection errors, is in turn followed by a trailing DC-free sequence 530."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Additionally, to the extent that it is determined that any of the above references do not disclose packets containing "in-band symbols" that are "transition optimized" and synchronization symbols that are "out-of-band symbols" and "not transition optimized," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Auld, 11:14–19 ("A typical sync word may be represented by a 24-bit or 32-bit word made up of consecutive zeros and ending with a '1' bit. Alignment involves the recognition of word or byte boundaries within a system bitstream in accordance with the syntax of the selected compression algorithm."); Knecht, 4:46–49 ("The 5-bit codes, with the exception of the sync symbol, are formatted in a 40/60 percent ratio of 0 and 1 bits, with either end of the 5-bit code being made up of no more than two logical '0' or '1' bits."), 5:37–38 ("Two representations of sync symbols namely 00000 and 11111 are necessary."); Kotani, ¶ 6 ("Ten l's or ten 0's are repeated in the respective [sync] patterns. In this way, erroneous detection of data bits and sync patterns is prevented since the number of consecutive 0's is restricted in the data bits."); Shin, 9:66–10:8 ("Each character corresponding to one of these 'out-of-band' characters associated with the high-transition set includes less than four logical transitions, and each of the out-of-band characters associated with the low-transition set of code characters includes more than four logical transitions. The difference in the number of transitions between in-band and out-of-band characters allows selected out-of-band characters to serve as control characters, and to be readily

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 53

distinguished from in-band characters within the transmitted data stream."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Additionally, to the extent that it is determined that any of the above references do not disclose packet types that include a "control packet," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Knecht, 3:28–32 ("Communication protocol is established and maintained with four signals, namely: sync symbol, data packet, control packet, and checksum packet. In the preferred embodiment, control, data and checksum packets comprise 16 bits of information before encoding and 20 bits after encoding."); Kotani, ¶ 5 ("For example, packets for commercialized household digital VCRs can be classified into two types, i.e., a 12-byte sub-code packet including a 2-byte sync pattern, and a 90-byte AV data packet including a 2-byte sync pattern."); Bastiani, 26:48–50 ("Data type 1 will be used for control and status of the device, and Data type 2 will be used to transfer data to the device."); Chen, 14:65–15:3 ("In the case of video, audio or isochronous control data, the stream of packets labeled with a single PID represents a single video, audio or isochronous data service elementary stream, respectively. Each type of packet will have a different PID identifying the packet type."); Cunningham, 4:23–27 ("Control information is conveyed by using selected n-bit data block values, together with a distinctive value of 10 for the pair of label bits a and b to indicate that the associated data block represents control information rather than actual data."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Additionally, to the extent that it is determined that any of the above references do not disclose transmitting symbols to a "switch network," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 54

Burke, 1:31–36 ("[D]igital data may be transmitted both in the downstream direction, from the head end (connected to a network) to the individual user (subscriber access unit), and in the upstream direction, from the individual user to the head end (and to the network)."); Bastiani, 6:3–6 ("ASP is a star network that supports data exchange between a host computer and storage devices such as disks, tapes and CD's. The attached peripherals share ASP bandwidth through a host scheduled polling based protocol."), 6:20–23 ("In this example, the host adapter 104 is configured to include ASP circuitry 104 a for processing ASP packet data and communicating between the host computer 102 and the ASP device 106."); Barry, 12:17–23 ("The output of packet processor 54 enters the switch fabric 50. One suitable packet switch is the MMC Networks model nP5400 Packet Switch Module. In one embodiment, four such switches are connected in each switching card for faster throughput. This embodiment is used on the switching card. The capabilities of this switch are not critical to this specification."); Chen, 4:63–67 ("A compressed digital packetized data stream which includes the inserted message combined with the main program is output from the DAIM 130 to an ATM transmitter (Tx) interface 126, and then provided to an access network (e.g., cable system headend) 140."); Cunningham, 2:65–3:1 ("Referring to FIG. 1, a data frame intended to be communicated over an optical fibre channel 20 typically comprises a binary digital message (payload) to be transferred between stations on the network. . . ."); Hiroshima, 5:40–43 ("The video-on-demand system corresponds to MPEG2 having a transmission rate of 6.144 Mbps and transmits data by a prefix bit rate of the MPEG2-TS through the network 22."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Additionally, to the extent that it is determined that any of the above references do not disclose a "synchronization primitive" made up of "a sequence of bit-string synchronization

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 55

symbols," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Bastiani, 24:43–46 ("A minimum of two and maximum of four SYNC characters must be sent to assure byte synchronization. It is used by the receive circuitry to align incoming data bytes and is defined to be eight bits in length."); Cunningham, 7:5–8 ("There are many potential ways to achieve code block synchronization (i.e. correct alignment in the receiver of the label and payload fields). For example, one technique would be to transmit a 'comma sequence' during start-up."); Shin, 15:20–26 ("During each preambling period, three repetitions of the same synchronization character are produced by the encoder 18. As is described herein, by processing the 21 bits most recently produced by the encoder 14, synchronization module 114 is able to detect at least one of the three repetitions of the synchronization character transmitted during a given preambling period."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable resIs; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 56

all pertain to serial communication between a transmitting device and a receiving device using packets.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards communication between a transmitting device and a receiving device using packets, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

For example, a person skilled in the art would have been motivated to combine Auld with Haartsen, Kotani, Shin, and/or additional references discussed above and disclosed in Exhibits C-1 through C-8 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed to serial transmission of data using packets. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, a simple substitution of Haartsen's digital preamble for Auld's sync code would achieve the predictable result of incorporating synchronization information into a synchronization symbol. As another example, a person of ordinary skill in the art would have been motivated to implement Kotani's disclosure of a unique synchronization code for subcode (i.e., control) packets into Auld, which discloses a need to distinguish between packet types. Additionally, the straightforward addition of Shin's preambling

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 57

sequence to Auld would enhance the capability of Auld's system to synchronize and align the transmitted data packets.

Furthermore, a person skilled in the art would have been motivated to combine Bastiani with Haartsen, Kotani, Knecht, Shin, and/or additional references discussed above and disclosed in Exhibits C-1 through C-8 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed to serial transmission of data using packets. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, a simple substitution of Haartsen's digital preamble for the non-data fields of the packets in Bastiani would achieve the predictable result of incorporating synchronization information into a synchronization symbol. As another example, a person of ordinary skill in the art would have been motivated to implement the out-of-band synchronization symbols in Kotani and Knecht in order to avoid the erroneous detection of packets and synchronization symbols. Additionally, the straightforward addition of Shin's preambling sequence to Bastiani would enhance the capability of Bastiani's system to synchronize and align the transmitted data packets.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the '798 Patent:

- Auld in view of Haartsen
- Auld in view of Haartsen and Shin
- Auld in view of Haartsen and Kotani
- Bastiani in view of Haartsen
- Bastiani in view of Haartsen and Kotani
- Bastiani in view of Haartsen and Knecht

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 58

- Bastiani in view of Haartsen and Shin

B. Invalidity of the '798 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '798 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '798 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- "the out-of-band symbols are not transition optimized." (claims 3, 13, 21)
- "synchronization information" (claim 19)
- "bit-string synchronization symbols" (claim 28)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

C. Invalidity of the '798 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '798 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, the Asserted Claims of the '798 Patent are invalid at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. At least the following claim language is indefinite:

- "the synchronization symbols are out-of-band symbols" (claims 2, 12, 20)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 59

- "the symbols of the packets include in-band symbols" (claims 2, 12, 20)
- "the synchronization symbol permitting properly alignment upon receiving with a synchronization primitive to be correctly aligned on a symbol boundary (claim 11)
- "synchronization information" (claim 19)
- "the transmitted synchronization symbol . . . permitting an external receiving node to properly align with a synchronization primitive to be correctly aligned on a symbol boundary" (claim 19)
- "transition optimized" (claim 21)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, at least claim 19 (and its dependent claims) of the '798 Patent recites functions without sufficient structure for performing the function, thus invoking 35 U.S.C. § 112, ¶ 6. Because the specification of the '798 Patent also does not recite structure for performing the function, the following terms are invalid as indefinite under 35 U.S.C. §§ 112, ¶ 2:

- "an identification component that identifies a packet type of a packet of symbols" (claim 19)
- "a transmission component that transmits a synchronization symbol that corresponds to the identified packet type . . . and that transmits the symbols of the packet" (claim 19)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 60

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

VI. THE ASSERTED CLAIMS OF THE '265 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits D-1 through D-8, discussed in any incorporated IPR petitions and institution decisions, discussed or cited in the prosecution history and/or any reexamination proceedings, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '265 Patent.

1. The '265 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '265 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit D-1 through D-8 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '265 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '265 Patent. Further, Defendant contends that any prior art

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 61

reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date	Short Name	Exhibit Number
JP 2009060204 A	Filed: Aug. 30, 2007 Pub'd: Mar. 19, 2009	Iwamoto	D-1
U.S. Patent Publ. No. 2009/0046690 A1	Filed: Aug. 16, 2007 Pub'd: Feb. 19, 2009	Hsieh	D-2
U.S. Patent Publ. No. 2008/0028237 A1	Filed: Jul. 26, 2006 Pub'd: Jan. 31, 2008	Knight	D-3

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Hitachi, Ltd. Panasonic Corporation Philips Consumer Electronics, International B.V. Silicon Image, Inc. Sony Corporation Thomson Inc. Toshiba Corporation	High-Definition Multimedia Interface Specification Version 1.4	Jun. 5, 2009	HDMI 1.4	D-4

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '265 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 62

Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- High-Definition Multimedia Interface (HDMI) (*e.g.,* HDMI 1.4, Ex. D-4)
- USB OTG
- USB 2.0
- IEEE 802.3af (PoE)
- IEEE 1394 (Firewire)

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the ’265 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

d) Other Relevant References

Defendant reserves the right to rely on the prior art references identified in connection with one of the other Asserted Patents in connection with the ’265 patent. In addition, Defendant hereby cites the following additional references as being relevant to the subject matter claimed in the ’265

patent. Defendant is producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendant reserves the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Plaintiff may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendant reserves the right to revise these contentions and to rely on these references to prove the invalidity of the '265 patent in a manner consistent with this Court's Rules and with the Federal Rules of Civil Procedure.

(1) Prior Art Patents and Applications

Number	Published/Issued Date
U.S. Pat. No. 7,480,758	Filed: Mar. 7, 2007 Pub'd: Sep. 11, 2008 Issued: Jan. 20, 2009
WO 2010067243 A1	Filed: Nov. 24, 2009 Pub'd: Jun. 17, 2010
U.S. Patent Publ. No. 2003/0229749 A1	Filed: Mar. 4, 2003 Pub'd: Dec. 11, 2003
U.S. Pat. No. 9,274,739	PCT Filed: Apr. 17, 2009 PCT Pub'd: Oct. 21, 2010 Filed: Dec. 16, 2011 Issued: Mar. 1, 2016
U.S. Patent Publ. No. 2007/0242062 A1	Filed: Apr. 18, 2006 Pub'd: Oct. 18, 2007
U.S. Patent Publ. No. 2009/0179883 A1	Prov.: Jan. 15, 2008 Filed: Apr. 21. 2008 Pub'd: Jul. 16, 2009
U.S. Patent Publ. No. 2010/0183004 A1	Prov.: Jan. 16, 2009, Apr. 23, 2009, May 13, 2009

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 64

	Filed: Jun. 15, 2009 Pub'd: Jul. 22, 2010
U.S. Patent Publ. No. 2014/0092305 A1	Priority: Dec. 17, 2007 Filed: Dec. 4, 2013 Pub'd: Apr. 3, 2014
JP 1992368666 A	Filed: Jun. 18, 1991 Pub'd: Dec. 21, 1992
JP 2001086416 A	Filed: Sep. 13, 1999 Pub'd: Mar. 30, 2001
U.S. Pat. No. 8,185,669	Filed: Jul. 10, 2007 Pub'd: May 1, 2008 Issued: May 22, 2012
U.S. Pat. No. 8,841,886	Filed: Sep. 9, 2010 Pub'd: Mar. 24, 2011 Issued: Sep. 23, 2014
U.S. Pat. No. 9,124,853	Filed: Nov. 30, 2010 Pub'd: May 31, 2012 Issued: Sep. 1, 2015
U.S. Pat. No. 9,900,653	Priority: Mar. 5, 2009 Filed: Nov. 8, 2016 Pub'd: Feb. 23, 2017 Issued: Feb. 20, 2018
U.S. Patent Publ. No. 2008/0126591 A1	Filed: Nov. 13, 2007 Pub'd: May 29, 2008
U.S. Patent Publ. No. 2009/0177818 A1	Filed: Jan. 4, 2008 Pub'd: Jul. 9, 2009
U.S. Patent Publ. No. 2011/0063501 A1	Filed: Sep. 14, 2009 Pub'd: Mar. 17, 2011

(2) Prior Art Publications

Author or Publisher	Title	Publication/Use Date
USB Implementers Forum, Inc.	On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a	Jun. 24, 2003
Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation,	Universal Serial Bus Specification, Revision 2.0	Apr. 27, 2000

NEC Corporation, Koninklijke Philips Electronics N.V.		
IEEE Computer Society	802.3af IEEE Standard for Information Technology	Jun. 18, 2003
IEEE Computer Society	1394b IEEE Standard for High-Performance Serial Bus-Amendment 2	Dec. 14, 2002

2. The '265 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '265 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits D-1 through D-8, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits D-1 through D-8 with each other, at least because all of these references relate to methods and apparatuses for communicating audio/visual data between a source and a sink, and/or methods and apparatuses for communicating audio/visual data using a source/sink dual purpose device. The charted references may further disclose methods for a source/sink dual purpose device to transition between source and sink modes.

For example, JP 2009060204 A to Iwamoto ("Iwamoto") teaches a "source/sink dual-purpose device conforming to the HDMI standard" that can function as a source device or a sink device. Iwamoto at [0016]-[0017]. The dual-purpose device includes a first voltage level monitor

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 66

for detecting the voltage level of the power line of an HDMI cable (V1), and a second voltage level monitor for detecting the voltage level of a TMDS_CLK line of the HDMI cable (V2). Iwamoto at [0016]. Iwamoto teaches that the dual-purpose device uses these measurements to determine whether a connected device is a source or a sink, and to "automatically switch[] its own functions" accordingly. *Id.* at [0016], [0026]. More specifically, Iwamoto teaches that the dual-purpose device has several modes depending on the two voltage levels. When V1 and V2 are low, the dual-purpose device determines that it is not connected to a second device and operates in standby mode. *Id.* at [0043]-[0044], [0072]-[0073], Fig. 3. When V1 is high and V2 is low, the dual-purpose device determines that the connected device is a source and operates in sink mode. *Id.* at [0043]-[0045], [0075], [0076], Fig. 3. When V1 is low and V2 is high, the dual-purpose device determines that the connected device is a sink and operates in source mode. *Id.* Thus, "the source/sink dual-purpose device can function as the source device or the sink device according to…whether [the connected device] is the sink device or the source device, without a switching operation of the user." Iwamoto at [0027].

U.S. Patent App. Pub. No. 2009/0046690 A1 to Hsieh ("Hsieh) similarly discloses a bi-directional high speed digital interface ("HSDI") transceiver and "a method for supplying a bi-directional communication process on a HSDI device." Hsieh at [0001]-[0004]. Hsieh explains that the "HSDI transceiver with bi-directional functionality can switch its function to make itself compatible to a typical HSDI source device/HSDI sink device, or form a bi-directional HSDI structure coupled with another HSDI transceiver with bi-directional functionality." *Id.* at [0035]. In other words, "the first HSDI transceiver acts as a source device if the interface is coupled to [a sink], and the first HSDI transceiver acts as a sink device if the interface is coupled to [a source]." *Id.* at [0006]. Hsieh further teaches that "the first HSDI transceiver is pre-set to be either the source

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 67

device or the sink device prior [to] receiving or generating a first control switching command." *Id.* at [0006], [0106]. Accordingly, "the settings of the power pin 114 and the hot plug detect pin 118, and the connection relationships of the first multiplexer 106 and the second multiplexer 112 of the HSDI transceiver 100 are pre-set…[according to] the standard for HSDI device, such as HDMI specification," depending on the pre-set default function. *Id.* at [0106]. For example, when the HSDI transceiver is a DVD recorder (typically a source), "the default setting of the first multiplexer 106 is to couple to the transmitter 102, the default setting of the second multiplexer 112 is to couple to the controller 108, the controller 108 controls the third multiplexer 116 to set the power pin 114 to supply power, and controls the fourth multiplexer 120 to set the hot plug detect pin 118 to become an input node." *Id.* at [0106].

Hsieh explains that the HSDI transceiver first determines whether an HSDI device is connected and whether it supports bi-directional functionalities. *Id.* at [0017]-[0018], Fig. 3. The HSDI transceiver is initially set to its default function, but if the attached device has the same function, the HSDI transceiver may toggle its function to "act as the source device and the sink device alternately" in order to connect to the attached device. *Id.* at [0017], [0020]. The HSDI transceiver then determines whether the connected device has bi-directional functionality (i.e., can also swap between source and sink). *Id.* at [0018]. If the connected device is bi-directional, the HSDI transceiver may ask the device to switch functions via switching commands. *Id.* at [0020]-[0022].

U.S. Patent App. Pub. No. 2008/0028237 A1 to Knight ("Knight") also discloses a device "capable of communicating power and data through a single connector to another device," where the device may be configured as a source or sink. Knight at [0024], [0039]-[0040]. The device may be, for example, "a dedicated network connection device…, [or] a portion of a computer, robot,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 68

[or] network appliance." *Id.* at [0031]. Knight teaches that the device may connect to multiple other devices and enable communication between them according to PoE, Firewire, USB, or similar communication protocols. *Id.* at [0031]-[0032], [0001], [0024].

Knight further explains that, when a connection is made, the device may "first attempt[] to connect as a power source, then attempt[] to connect as a power sink if the power source attempt fails." *Id.* at [0048]. Alternatively, the device "may be configured to attempt to connect as a power sink initially, then attempts as a power source secondarily." *Id.* The sink/source negotiation process "may be through sensing status and communicating through the power connections." *Id.* at [0047]. "One example of such communication may be for a device to configure a specific resistance along the power connections to indicate that it may sink power," in which case "the connecting device may sense the resistance and then begin supplying power to the first device." *Id.*

Lastly, the High-Definition Multimedia Interface Specification Version 1.4 ("HDMI 1.4") discloses an interface for "transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays." HDMI 1.4 at 1. The specification describes the "[m]echanical, electrical, behavioral and protocol requirements necessary for compliance…for sources, sinks and cables." *Id.* HDMI 1.4 explains that the "HDMI system architecture is defined to consist of Sources and Sinks," where "[e]ach HDMI input…shall follow all of the rules for an HDMI Sink and each HDMI output shall follow all of the rules for an HDMI Source." *Id.* at 9. The specification further teaches that "[t]he HDMI connector provides a pin allowing the Source to supply +5.0 Volts to the cable and Sink," where "[a] Sink shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that a Source is connected and applying power to the +5V Power signal." *Id.* at 71. Once a sink detects the +5V power line, it may assert the hot plug detect pin. *Id.* at 153. "A Source shall

assume that any voltage [on the hot plug detect pin] within the range specified for High voltage level in Table 4-39 indicates that a Sink is connected." *Id.* at 153. The HDMI 1.4 specification further teaches that HDMI sources and sinks, "upon power-up, reset, or detection of a new [] device," shall assume that the connected device is not HDMI-capable. *Id.* at 166-167. Once it is determined that the connected device is HDMI-capable, the HDMI sink or source follows all HDMI requirements in the specification. *Id.*

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Furthermore, to the extent that it is determined that any of the above references do not disclose a particular claim element, it would have been obvious to modify the teachings of that reference to include such element as taught in any other of the above references that discloses such element (as documented in the claim charts attached as D-1 through D-8).

For example, to the extent that it is determined that any of the above references do not disclose "initializing a first audio/video (AV) device to operate in a default AV sink operation mode in response to a power-on-reset or powering up" and/or "the AV sink operation mode being a default mode of operation for the AV device," as recited in claim 1 and in similar form in claims 8 and 14, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Iwamoto, Hsieh, Knight, and/or HDMI 1.4. More particularly, Iwamoto teaches a dual-purpose source/sink device

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 70

that is in a "standby" mode when disconnected. Iwamoto at [0052]. Hsieh similarly discloses an HDMI device that can switch between source and sink mode which is "pre-set" to either the source or sink mode. Hsieh at [0006] and [0016]. Knight also teaches an AV device that may first attempt to connect as a sink, then attempt to connect as a source. Knight at [0048]. Moreover, the HDMI 1.4 specification explains that HDMI sources and sinks default to particular settings upon power-up, reset or detection of a new [] device." HDMI 1.4 at 166-167. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "determining whether a first supply voltage is provided at a channel of a connector;" "in response to determining that the first supply voltage is provided at the channel of the connector, configuring communication logic of the first AV device to continue operating the first AV device in the AV sink operation mode;" and/or "in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV source operation mode;" as recited in claim 1 and in similar form in claims 8 and 14, it would further have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Iwamoto and HDMI 1.4.

As outlined in further detail below, Iwamoto teaches a "source/sink dual-purpose device conforming to the HDMI standard" that determines whether a connected device is a source or a sink based on the voltage levels on the power line and the TMDS_CLK line. Iwamoto at [0016], [0026]. When V1 is high and V2 is low, the dual-purpose device determines that the connected device is a source and operates in sink mode. *Id.* at [0043]-[0045], [0075], [0076], Fig. 3. When V1 is low and V2 is high, the dual-purpose device determines that the connected device is a sink

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 71

and operates in source mode. *Id.* The HDMI 1.4 specification also explains that sources are configured to "supply +5.0 Volts to the cable and Sink," where "[a] Sink shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that a Source is connected and applying power to the +5V Power signal." *Id.* at 71. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to methods and apparatuses for communicating audio/visual data between a source and a sink, and/or methods and apparatuses for communicating audio/visual data using a source/sink dual purpose device.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards communicating audio/visual data between a source and a sink and/or a

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 72

source/sink dual purpose device, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

As illustrated in the claim charts attached as Exhibits D-1, D-5, and D-6, Iwamoto, alone or in combination with HDMI 1.4 and Hsieh or Knight, discloses or renders obvious all elements of the '265 Asserted Claims. Iwamoto teaches a "source/sink dual-purpose device conforming to the HDMI standard" that can function as a source device or a sink device. Iwamoto at [0016]-[0017]. Iwamoto teaches that the dual-purpose device measures the voltage level of the power line of an HDMI cable (V1), and the voltage level of a TMDS_CLK line of the HDMI cable (V2) to determine whether a connected device is a source or a sink, and to "automatically switch[] its own functions" accordingly. *Id.* at [0016], [0026]. More specifically, Iwamoto teaches that the dual-purpose device has several modes depending on these values, as illustrated in the negotiation process of Fig. 3. When V1 and V2 are low, the dual-purpose device determines that it is not connected to a second device and operates in standby mode. *Id.* at [0043]-[0044], [0072]-[0073], Fig. 3. When V1 is high and V2 is low, the dual-purpose device determines that the connected device is a source and operates in sink mode. *Id.* at [0043]-[0045], [0075], [0076], Fig. 3. When V1 is low and V2 is high, the dual-purpose device determines that the connected device is a sink and operates in source mode. *Id.* When the devices are disconnected, the dual-purpose device goes into standby mode and restarts the process of Fig. 3. *Id.* at [0065]. Iwamoto does not explicitly address how its dual-purpose device would negotiate source/sink mode when connected to another dual-purpose device, rather than a standard HDMI source or sink.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 73

Hsieh discloses a bi-directional high speed digital interface transceiver that may also conform to the HDMI specification. Hsieh at [0002]. Like the device of Iwamoto, Hsieh's transceiver can also switch between source and sink mode to "make itself compatible to a typical HSDI source device/HSDI sink device, or form a bi-directional HSDI structure coupled with another HSDI transceiver with bi-directional functionality." *Id.* at [0035]. Hsieh further teaches that "the first HSDI transceiver is pre-set to be either the source device or the sink device." *Id.* at [0006], [0106]. For example, a device that is typically used as a source—such as a DVD recorder—can be pre-set to operate as a source device. *Id.* at [0002], [0016] (explaining that a DVD recorder, which is generally a video source device, would default to source mode).

Hsieh further contemplates that a first bidirectional source/sink device may be connected to a second bidirectional source/sink device, rather than a standard source or sink. Hsieh at [0018], [0020]. When two such dual-purpose devices are connected, they default to either source or sink to begin the connection and source/sink negotiation process. *Id.* If the devices start with the same default setting, the bidirectional source/sink device will alternate between source and sink until the devices connect and can communicate. *Id.* at [0017]. If the devices need to swap modes after the connection is established, they can communicate via switching commands. *Id.* at [0020]-[0022].

Like Hsieh, Knight also teaches an AV device that may first attempt to connect as a sink, then attempt to connect as a source. Knight at [0048]. Moreover, the HDMI specification—which Hsieh and Iwamoto each follow—explains that HDMI sources and sinks default to particular settings upon power-up, reset or detection of a new [] device." HDMI 1.4 at 166-167.

Both Iwamoto and Hsieh relate to HDMI devices that can function as either a source or a sink, depending on the function of the connected device. While Iwamoto explains that its dual-purpose source/sink device changes modes according to whether a dedicated source or dedicated

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 74

sink is attached, Iwamoto does not explicitly address how two dual-purpose source/sink devices would negotiate the source/sink swapping process if connected together. Because Iwamoto's dual-purpose source/sink device does not set the power supply, hot plug, DDC, or TMDS when disconnected and in standby (see Iwamoto at Fig. 2), it is unclear whether the device would be registered as a source, sink, or neither by another dual-purpose source/sink device during the source/sink negotiation process in Fig. 3. However, as explained above, Hsieh does address the connection of two bi-directional source/sink devices, which begin the connection process in either a default source or default sink mode. Hsieh further explains that, when in the default source or sink mode, the power pin, hot plug detect pin, and other connection settings are also pre-set to conform to the HDMI specification. *Id.* at [0016].

Accordingly, a person skilled in the art would have been motivated to combine Iwamoto and Hsieh or Knight to set the dual-purpose source/sink device into either a default source or default sink mode, in order to provide for the situation when two dual-purpose source/sink devices attempt to connect. Furthermore, a person skilled in the art would have understood that the dual-purpose device would default to this mode upon power-up, reset, or connection of a new device, in view of the HDMI 1.4 standard, which is explicitly followed by Iwamoto and Hsieh. This combination reflects no more than a simple substitution of a known element—default sink or source—for another—default standby—to obtain predictable results.

Moreover, as illustrated in the claim charts attached as D-2 and D-7, Hsieh, alone or in combination with Iwamoto and/or HDMI 1.4, discloses or renders obvious all elements of the '265 Asserted Claims. Specifically, Hsieh teaches a bi-directional HDMI transceiver that "can switch its function to make itself compatible to a typical HSDI source device/HSDI sink device, or form a bi-directional HSDI structure coupled with another HSDI transceiver with bi-directional

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 75

functionality." Hsieh at [0035]. In other words, "the first HSDI transceiver acts as a source device if the interface is coupled to [a sink], and the first HSDI transceiver acts as a sink device if the interface is coupled to [a source]." *Id.* at [0006].

Hsieh explains that, when a device is connected to the transceiver, it undergoes a detection process according to the HDMI specification. *Id.* at [0017] ("When the HSDI transceiver 100 is connected to a specific HSDI device, it will trigger the detection process to determine whether the specific HSDI device is plugged in according to a communication procedure specified in the specification for a variety of HSDI devices, such as HDMI."). Hsieh further teaches that "the first HSDI transceiver is pre-set to be either the source device or the sink device prior [to] receiving or generating a first control switching command." *Id.* at [0006], [0106]. If the transceiver and an attached device have the same function, the HSDI transceiver may toggle its function to "act as the source device and the sink device alternately" in order to connect to the attached device. *Id.* at [0017], [0020]. The HSDI transceiver then determines whether the connected device has bi-directional functionality (i.e., can also swap between source and sink). *Id.* at [0018]. If the connected device is bi-directional, the HSDI transceiver may ask the device to switch functions via switching commands. *Id.* at [0020]-[0022].

As explained above, Iwamoto discloses a similar system where a dual-purpose HDMI device can operate as a source or a sink depending on whether the device is connected to a source or a sink. Iwamoto determines whether a source or sink is attached based, in part, on the voltage level of the power line. Iwamoto at [0043]-[0045], [0072]-[0076], Fig. 3. For example, when the voltage on the power line is high and the voltage on the TMDS_CLK line is low, the dual-purpose device determines that a source is connected, and the dual-purpose device operates as a sink. When the voltage on the power line is not high, the dual-purpose device stops operating as a sink. *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 76

This comports with the HDMI standard, which explains that "[t]he HDMI connector provides a pin allowing the Source to supply +5.0 Volts to the cable and Sink," where "[a] Sink shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that a Source is connected and applying power to the +5V Power signal." HDMI 1.4 at 71.

As previously explained, both Hsieh and Iwamoto relate to HDMI devices that can function as either a source or a sink, depending on the function of the connected device. Additionally, Hsieh states that the transceiver detects the connected device according to the HDMI specification, which explains that "[a] Sink shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that a Source is connected and applying power to the +5V Power signal." HDMI 1.4 at 71. Iwamoto operates in accordance with the HDMI specification, in that it determines that a source is attached, in part, based on whether the +5V power signal is applied to the power line. Iwamoto at [0043]-[0045], [0072]-[0076], Fig. 3. Accordingly, a person skilled in the art would have been motivated to combine Hsieh with Iwamoto and/or HDMI 1.4 such that the bi-directional transceiver taught by Hsieh can determine whether it is attached to a source or a sink based, at least in part, on whether the +5V power signal is applied to the power line, and switch its mode accordingly. This configuration comports with the HDMI 1.4 standard and relies on power characteristics that are common to all HDMI devices that comply with the specification. This combination reflects no more than the use of a known technique—determining that a source is connected based on the power line—to a known device to yield predictable results.

Additionally, as illustrated in the claim charts attached as D-3 and D-8, Knight, alone or in combination with Iwamoto and/or HDMI 1.4, discloses or renders obvious all elements of the '265 Asserted Claims. Specifically, Knight teaches a device "capable of communicating power and data through a single connector to another device," where the device may be configured as a source or

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 77

sink. Knight at [0024], [0039]-[0040]. Knight teaches that the device may connect to multiple other devices and enable communication between them according to PoE, Firewire, USB, or similar communication protocols. *Id.* at [0031]-[0032], [0001], [0024]. A POSITA would understand that the HDMI protocol is similar to PoE, Firewire, and USB, as it enables communication of power and data through a single connector. Knight further explains that, when a connection is made, the device may "attempt to connect as a power sink initially, then attempt[] as a power source secondarily." *Id.* at [0048]. The sink/source negotiation process "may be through sensing status and communicating through the power connections." *Id.* at [0047].

As explained above, Iwamoto teaches a similar source/sink device that uses power connections during the source/sink negotiation process. Specifically, Iwamoto teaches a dual-purpose HDMI device that can operate as a source or a sink depending on whether it is connected to a source or a sink. Iwamoto determines whether a source or sink is attached based, in part, on the voltage level of the power line—i.e., "power connections." Iwamoto at [0043]-[0045], [0072]-[0076], Fig. 3. This follows the HDMI standard, which explains that "[t]he HDMI connector provides a pin allowing the Source to supply +5.0 Volts to the cable and Sink," where "[a] Sink shall assume that any voltage within the range specified for TP2 voltage in Table 4-34 indicates that a Source is connected and applying power to the +5V Power signal." HDMI 1.4 at 71.

Both Knight and Iwamoto relate to devices that can function as either a source or a sink. Additionally, Knight states that the device may follow PoE, Firewire, USB, or similar communication protocols, and can determine whether it should be set as a source or a sink based on sensing the "power connections" between the devices. *Id.* at [0031]-[0032], [0001], [0024], [0047]. Iwamoto teaches how a device complying with the HDMI standard—which a POSA would find similar to PoE, Firewire, and USB—senses power connections to switch between source and

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 78

sink during the negotiation process. Accordingly, a person skilled in the art would have been motivated to combine Knight with Iwamoto and/or HDMI 1.4, such that the device taught by Knight can determine whether it is attached to a source or a sink based, at least in part, on whether the +5V power signal is applied to the power line, and switch its mode accordingly. This configuration comports with the HDMI 1.4 standard and relies on power characteristics that are common to all HDMI devices that comply with the specification. This combination reflects no more than the use of a known technique—determining that a source is connected based on the power line—to a known device to yield predictable results.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the '265 Patent:

- Iwamoto in view of Hsieh.
- Iwamoto in view of Hsieh and HDMI 1.4.
- Iwamoto in view of Knight.
- Iwamoto in view of Knight and HDMI 1.4.
- Hsieh in view of Iwamoto.
- Hsieh in view of Iwamoto and HDMI 1.4.
- Knight in view of Iwamoto.
- Knight in view of Iwamoto and HDMI 1.4.

B. Invalidity of the '265 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '265 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '265 Patent are invalid for failure

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 79

to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- "in response to determining that the first supply voltage is not provided at the channel of the connector, configuring the communication logic of the first AV device to transition the first AV device from the AV sink operation mode to an AV source operation mode" (claim 1)
- "to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector" (claim 8)
- "to configure the communication logic to transition the AV device from the AV sink operation mode to the AV source operation mode in response to determining that the first supply voltage is not provided at the channel of the connector" (claim 14)
- "wherein the detector logic is further configured to detect a change to the connectivity after the AV data exchange, wherein, in response to the detected change to the connectivity, the control logic further configured to place the communication logic into the AV sink operation mode" (claim 16)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

The written description and enablement issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

C. Invalidity of the '265 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '265 Patent, to the extent such positions can be understood from Plaintiff's Infringement

Contentions, Defendant asserts that one or more of the Asserted Claims of the '265 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- "a default AV sink operation mode" (claim 1)
- "the AV sink operation mode" (claim 1)
- "the AV sink operation mode being a default mode of operation" (claim 8)
- "the AV sink operation mode" (claim 8)
- "the default AV sink operation mode" (claim 8)
- "the default operation mode" (claim 11)
- "the AV sink operation mode" (claim 14)
- "the AV sink operation mode being a default mode of operation" (claim 14)
- "the default AV sink operation mode" (claim 14)
- "the default operation mode" (claim 15)
- "the AV sink operation mode" (claim 16)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 81

Additionally, Claims 8, 11, 14, 15, and 16 of the '265 Patent are invalid under 35 U.S.C. §§ 112 ¶ 6 because the '265 Patent does not disclose sufficient structure corresponding to the function recited in at least the following means-plus-function claim limitations:

- "communication logic to couple to a connector…" (claim 8)
- "circuitry configured to implement…" (claim 8)
- "control logic including circuitry to configure the communication logic…" (claim 8)
- "detector logic to detect…" (claim 11)
- "communication logic" (claim 14)
- "circuitry configured to implement…" (claim 14)
- "control logic including circuitry to configure the communication logic…" (claim 14)
- "detector logic to detect…" (claim 15)
- "detector logic is further configured to detect…" (claim 16)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

VII. THE ASSERTED CLAIMS OF THE '712 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits E-1 through E-19, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '712 Patent.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 82

1. The ’712 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the ’712 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit E-1 through E-19 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the ’712 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the ’712 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date	Short Name	Exhibit Number
U.S. Pat. App. Pub. No. 2006/0089230 A1	Filed: Oct. 7, 2004 Pub’d: Apr. 27, 2006	Biederman	E-1
U.S. Pat. App. Pub. No. 2006/0100799 A1	Filed: Nov. 5, 2004 Pub’d: May 11, 2006	Karam ’799	E-2
U.S. Pat. App. Pub. No. 2008/0168283 A1	Filed: Jan. 5, 2007 Pub’d: Jul. 10. 2008	Penning	E-3

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 83

U.S. Pat. App. Pub. No. 2006/0273661 A1	Filed: Jun. 2, 2005 Pub'd: Dec. 7, 2006	Toebes	E-4
U.S. Patent App. Pub. No. 2008/0028237 A1	Filed: Jul. 26, 2006 Pub'd: Jan. 31, 2008	Knight	E-5
U.S. Pat. App. Pub. No. 2005/0268120 A1	Filed: May 13, 2004 Pub'd: Dec. 1, 2005	Schindler	E-6
U.S. Pat. App. Pub. No. 2006/0210057 A1	Filed: Jan. 23, 2006 Pub'd: Sep. 21, 2006	Stanford	E-7
U.S. Pat. App. Pub. No. 2006/0218420 A1	Prov.: Mar. 28, 2005 Filed: Nov. 23, 2005 Pub'd: Sep. 28, 2006	Camagna	E-8
U.S. Pat. App. Pub. No. 2008/0250255 A1	Filed: Apr. 6, 2007 Pub'd: Oct. 9, 2008	Diab '255	E-9
U.S. Pat. App. Pub. No. 2008/0016263 A1	Prov.: Jun. 28, 2006 Filed: Jun. 26, 2007 Pub'd: Jan. 17, 2008	Diab '263	E-10
U.S. Pat. App. Pub. No. 2006/0168459 A1	Filed: Nov. 15, 2005 Pub'd: Jul. 27, 2006	Dwelley	E-11
U.S. Pat. App. Pub. No. 2008/0235523 A1	Prov. Mar. 20, 2007 Filed: Mar. 20, 2008 Pub'd: Sep. 25, 2008	Hussain	E-12
U.S. Pat. App. Pub. No. 2007/0220280 A1	Filed: Mar. 14, 2006 Pub'd: Sep. 20, 2007	Karam '280	E-13
U.S. Pat. App. Pub. No. 2008/0005598 A1	Filed: Jun. 30, 2006 Pub'd: Jan. 3, 2008	Landry	E-14
U.S. Pat. App. Pub. No. 2005/0044431 A1	Filed: May 24, 2004 Pub'd: Feb. 24, 2005	Lang	E-15
U.S. Pat. App. Pub. No. 2007/0278857 A1	Filed: Oct. 6, 2006 Pub'd: Dec. 6, 2007	Robbins	E-16

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
IEEE Computer Society	802.3af-2003 IEEE Standard for Information Technology	Jun. 18, 2003	IEEE 802.3af	E-17

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Maxim Integrated Products	+48V, Single-Port Network Power Switch For Power-Over-LAN	Apr. 2003	MAX5922	E-18
Texas Instruments	IEEE 802.3af Power Interface Switch For Power Over Ethernet (PoE) Powered Devices	Mar. 2004	TPS2370	E-19

c) Prior Art Systems

On information and belief, the systems identified below and the systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '712 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- MAX5922 and similar products
- TPS2370 and similar products
- IEEE 802.3af (PoE)
- USB 2.0
- IEEE 1394 (Firewire)

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 85

above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '712 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

d) Other Relevant References

Defendant reserves the right to rely on the prior art references identified in connection with one of the other Asserted Patents in connection with the '712 patent. In addition, Defendant hereby cites the following additional references as being relevant to the subject matter claimed in the '712 patent. In addition to these references, Defendant is producing concurrent herewith a number of other references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendant reserves the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Plaintiff may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendant reserves the right to revise these contentions and to rely on these references to

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 86

prove the invalidity of the ’712 patent in a manner consistent with this Court’s Rules and with the Federal Rules of Civil Procedure.

(1) Prior Art Patents and Applications

Number	Published/Issued Date
U.S. Pat. App. Pub. No. 2009/0222678	Filed: Feb. 29, 2008 Pub’d: Sep. 3, 2009
WO 2006/126160 A1	Filed May 22, 2006 Pub’d: Nov. 30, 2006
U.S. Patent No. 6,496,103	Filed: Feb. 4, 2000 Issued: Dec. 17, 2002
U.S. Patent No. 6,535,983	Filed: Nov. 8, 1999 Issued: Mar. 18, 2003

(2) Prior Art Publications

Author or Publisher	Title	Publication/Use Date
Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V.	Universal Serial Bus Specification, Revision 2.0	Apr. 27, 2000
IEEE Computer Society	1394b IEEE Standard for High-Performance Serial Bus-Amendment 2	Dec. 14, 2002
Roger Karam	Power Classification for the PD	Sep. 29, 2003
Maxim Integrated Products	IEEE 802.3af PD Interface Controller for Power-Over-Ethernet	Feb. 2006
Maxim Integrated Products	Quad Network Power Controller for Power-Over-LAN	Sep. 2005

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 87

Galit Mendelson	All You Need to Know About Power over Ethernet (PoE) and the IEEE 802.3af Standard	Jun. 2004

2. The '712 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the '712 Patent is not explicitly disclosed by an item of prior art identified above, in Exhibits E-1 through E-19, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits E-1 through E-19 with each other, at least because all of these references relate to systems and methods for delivering power to devices connected in a network via Power over Ethernet ("PoE"), including means for detecting connected devices and determining their power requirements. Furthermore, several of these references are specifically directed to the provision of power to devices connected in a daisy-chain configuration.

a) The PoE Standard

PoE is governed by the 802.3af-2003 IEEE Standard for Information Technology ("IEEE 802.3af"). The IEEE 802.3af standard "defines the functional and electrical characteristics of…a Powered Device (PD) and Power Sourcing Equipment (PSE)," which "allow devices to supply/draw power using the same generic cabling as is used for data transmission." IEEE 802.3af at 27. The standard provides "[a] protocol allowing the detection of a device that requires power,"

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 88

"a method to classify devices based on their power needs," and "[a] method for scaling supplied power back to the detect level when power is no longer requested or required." *Id.* The PSE's "main functions are to search the link section for a PD, optionally classify the PD, supply power to the link section (only if a PD is detected), monitor the power on the link section, and scale power back to the detect level when power is no longer requested or required." *Id.* at 29. One example of when power is no longer required is "[a]n unplugged link section." *Id.* A PSE may also detect a PD but opt not to power it. *Id.* at 37. A PD "is a device that is either drawing power or requesting power by participating in the PD detection algorithm." *Id.* at 49. A PD may be able to draw power from an alternate source, in which case the PD may not require power from the PSE. *Id.*

During the detection process, the PSE checks for a valid signature resistance in the PD. *Id.* at 38-39. The PD "shall present a valid detection signature…while it is in a state where it will accept power" from the PSE. *Id* at 51. The PD will present a non-valid signature "while it is in a state where it will not accept power" from the PSE. *Id.* A valid PD detection signature is between 23.75KΩ and 26.25 KΩ. *Id.* at 52, Table 33-8. IEEE 802.3af provides the Thevenin equivalent of the detection circuit, stating that "PSE requirements are stated for a Thevenin circuit only; they may be transformed via circuit theory into other circuit parameters in specific implementations." *Id.* at 38, Fig. 33-8. The PSE may detect the signature via "voltage or current measurement." *See Id.* at 39. The IEEE 802.3af standard explains that this detection process is vital and "should not be overlooked" because, [g]iven the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected…and the possible consequences of powering such devices, the protocol to distinguish compatible devices and noncompatible devices is important to prevent damage to non-compatible devices." *Id.* at 27.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 89

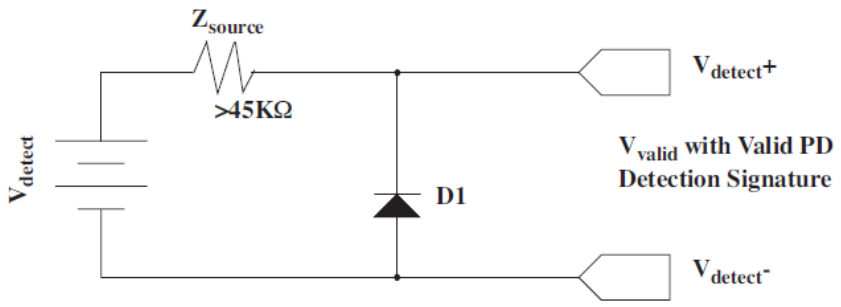


Figure 33–8—PSE detection source

After detection, the PSE may classify the maximum power required by the PD during operation. *Id.* at 53. The PSE performs classification of a PD by "applying voltage and measuring current." *Id.* at 40. "The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–4," which defines classes 0 through 4 based on current ranges. *Id.* at 40, 53. IEEE 802.3af further defines the power requirements for each class in Table 33-10; as one example, default class O requires .44 to 12.95 Watts. *Id.* at 53, Table 33-10.

b) Daisy Chained PoE Devices

U.S. Pat. App. Pub. No. 2006/0089230 A1 to Biederman et al. ("Biederman"), U.S. Pat. App. Pub. No. 2006/0100799 A1 to Karam ("Karam '799"), U.S. Pat. App. Pub. No. 2007/0220280 A1 to Karam et al. ("Karam '280"), U.S. Pat. App. Pub. No. 2008/0168283 A1 to Penning ("Penning"), U.S. Pat. App. Pub. No. 2006/0273661 A1 to Toebes et al. ("Toebes"), and U.S. Pat. App. Pub. No. 2007/0278857 A1 to Robbins ("Robbins") are each directed to the provision of power to devices in a daisy chain configuration via PoE. Each reference refers to the IEEE 802.3af standard, and Penning and Robbins explicitly incorporate it by reference.

(1) Biederman

Biederman teaches a networked device that "may operate as a powered device (PD) under certain circumstances, may be off for power purposes under other circumstances and may operate

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 90

as a power Sourcing equipment (PSE) under yet other circumstances." Biederman at [0033]. In Fig. 2, Biederman illustrates media dependent interfaces ("MDI") 14a and 14b, each with a PD functional block and a PSE functional block. *Id.* at [0034]. The MDI connected to the PSE has the PD block activated, while the MDI connected to the PD has the PSE block activated. *Id.* Biederman teaches that the PSE portion of the device includes a 48-volt power supply 70 to power a connected PD, and that the device includes a controller for selectively activating the PD block, the PSE block, neither, or both via switching circuitry which may include "diodes, transistors, relays, and the like." *Id.* at fig. 5, [0038].

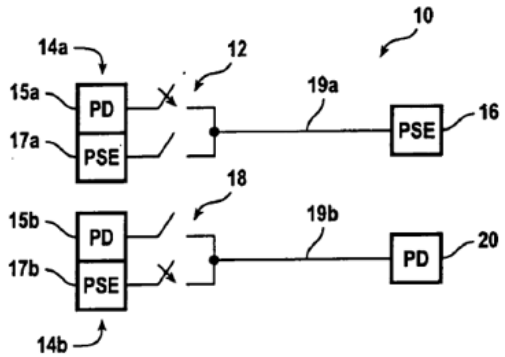


FIG. 2

Biederman at Fig. 2.

Biederman also teaches that "the power requirements of a PD may change from time to time depending upon how it is used," so "it would be desirable to adjust the power delivered to the PD from time to time to meet these new requirements, either by increasing the power delivered or decreasing it, as appropriate." *Id.* at [0042]. Biederman explains that "[a] number of mechanisms are provided by the present invention to accomplish this," and that "[t]hose of ordinary skill in the art will [] realize that other equivalent mechanisms are available to periodically revise the amount of power made available by the PSE to the PD." *Id.* at [0042]. As

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 91

one example, Biederman notes that "[t]here are mechanisms within the IEEE 802.3af standard to allocate a requested amount of power." *Id.* at [0014].

Finally, Biederman teaches that the combination PD/PSE units may be arranged in a daisy chain configuration to provide redundant data and inline power so that data or power interruption does not occur if the cabling is cut. *Id.* at [0043]-[0045]. In the below example, port 100 of device 88 is configured as a PD to receive power from PSE 826, and port 102 of device 88 is configured as a PSE to send power to device 90. *Id.* at [0044]. When a cable in the chain is cut, the adjacent devices reconfigure themselves—as illustrated below, when devices 88 and 90 are disconnected, port 104 of device 90 is turned off and port 108 of device 92 is turned on and configured to operate as a PSE. *Id.* at [0045].

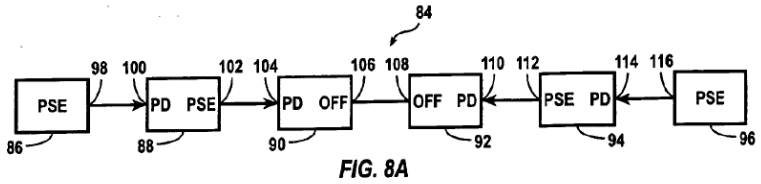


FIG. 8A

Biederman at Fig. 8A.

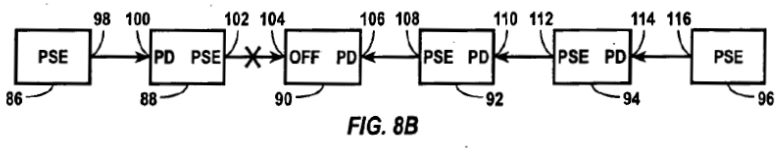


FIG. 8B

Biederman at Fig. 8B.

(2) Karam '799

Karam '799 teaches "a method and apparatus for managing an Inline Power relationship between a network device and a Powered Device (PD) where the network device is acting as power sourcing equipment (PSE) to provide Inline Power to a first PD (PD1) which is, in turn, powering another PD (PD2)." Karam '799 at [0039], Fig. 2A. The PSE may also provide power to a longer

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 92

daisy chain of PD devices. *Id.* at [0046] and Fig. 2D ("In FIG. 2D an arrangement is shown where a PSE provides power and data to three PDs: PD1, PD2 and PD3. This is again accomplished over a series of single 8 conductor (4 pair) cables daisy-chained between the various devices."). The first PD, PD1, receives power from a voltage source in the PSE. *Id.* at [0044].

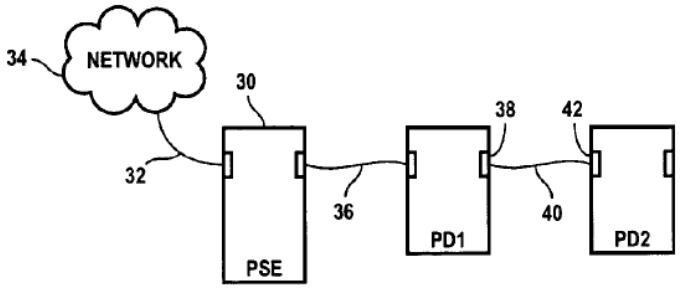


FIG. 2A

Karam '799 at Fig. 2A.

Karam '799 explains that "[i]n order to provide regular Inline Power to a PD from a PSE it is a general requirement that two processes first be accomplished. First, a 'discovery' process must be accomplished to verify that the candidate PD is, in fact, adapted to receive Inline Power. Second, a 'classification' process must be accomplished to determine an amount of Inline Power to allocate to the PD, the PSE having a finite amount of Inline Power resources available for allocation to coupled PDs." *Id.* at [0018]. Referencing the IEEE 802.3af standard, Karam '799 explains that the discovery process looks for an "identity network" in the PD, which is a 25,000Ω resistor. *Id.* at [0019]. To detect the identity network, the PSE applies voltage discovery signals, measures the "return currents responsive to application of the discovery signals," and calculates the resistance. *Id.* at [0020]. If the resistance is the proper value, classification may begin. *Id.* Again referencing the IEEE 802.3af standard, Karam '799 explains that the classification process involves applying a voltage to the PD, which responds by sending a classification current back to

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 93

the PSE. *Id.* at [0021]. This current corresponds to a "class," which represents a device's power requirements. *Id.* at [0021], Table I.

Karam '799 teaches that the first PD 50 in the chain includes a connector 52 to connect to the PSE, a second connector 54 which may be coupled to another device, and a third connector 56 for providing power to another device, such as a cell phone. *Id.* at [0051], Fig. 4A. Karam '799 explains that, in order to supply power to device 50, "the PSE port must see the proper identity network characteristics," which, "in accordance with the IEEE 802.3af standard," is a 25,000Ω resistance in response to "certain discovery voltage signals." *Id.* Accordingly, the controller 58 of the device 50 provides the identity network signal back to the PSE so that inline power may be provided. *Id.* at [0052]. The device 50 is also adapted to "act as a PSE device to determine if an attached device at a second connector 54 has an appropriate identity network so that inline power may be provided to it." *Id.* The device 50 senses the identify network via current sensor R2SENSE. *Id.* at Fig. 4A, [0058]. If the device 50 does not verify that the attached device can receive power, it may leave switches S1-S4 open, cutting off data and power to second connector 54. *Id.* Karam '799 further explains that the controller 58 may keep switch S5 to third connector 56 closed "only when current [is] being drawn from third connector 56 so that if the device were unplugged from third connector 56 the power would turn off." *Id.* at [0051].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 94

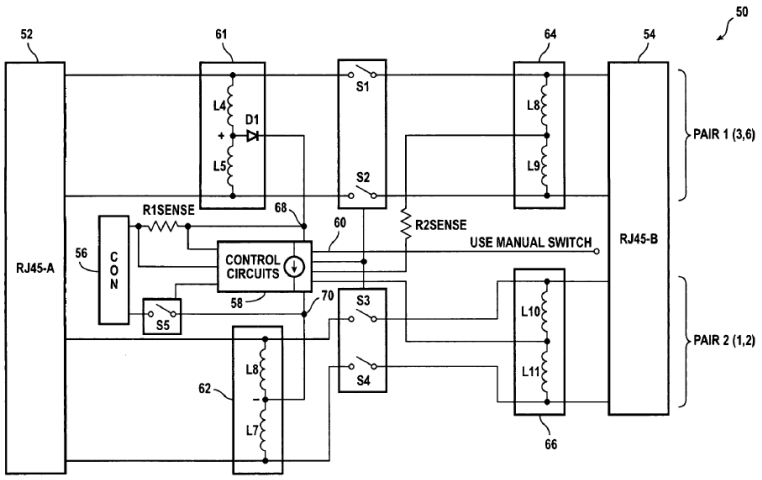


FIG. 4A

Karam '799 at Fig. 4A.

In another, similar embodiment, Karam '799 teaches that the PD 70 will measure power used by third port 76 using current sensor 81. *Id.* at [0058], Fig. 5. Switch 88, under control of control circuitry 78, provides power to the third port to power an accessory device such as a cell phone. *Id.* Similarly, current sensor 92 measures the power used by second port 74. *Id.* If power is being applied to port 74, and the current sensor 92 detects that the current has gone to zero—i.e., "device at second port 74 is off or disconnected"—control circuitry 78 forces switch 90 closed to "mak[e] sure that a 'hot cable' situation is not created at second port 74 by removing the inline power to second port 74." *Id.* To begin providing power again, the control circuitry 78 must identify the appropriate identify network, which may be achieved "by control circuitry 78 reducing the applied voltage and closing switch 90 to carry out a conventional inline power discovery process which may also be followed up by a classification process, if desired in the particular application." *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 95

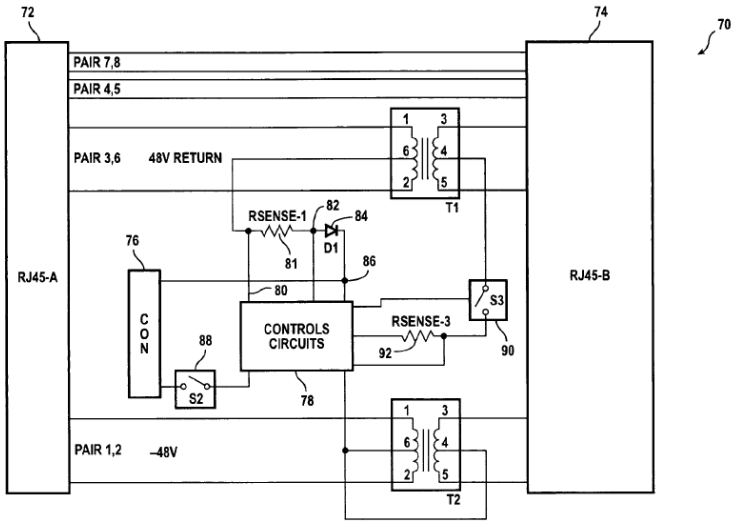


FIG. 5

Karam '799 at Fig. 5.

(3) Penning

Penning teaches a system for powering multiple devices connected over a network that may employ PoE network connections. Penning at [0028]-[0030]. The system includes a data distribution device 105, an independent power supply 115, a remote data distribution device 110, network devices 125-1 to 125-N, and externally powered network devices 120-1 to 120-N. *Id.* at [0029], Fig. 1. Remote data distribution device 110 acts as a PSE providing data and power to data distribution device 105, which can then provide data and power to network devices 125-1 through 125-N. *Id.* "Data distribution device 105 may sense the amount of power required by one or more network devices 125-1-125-N, and provide power accordingly." *Id.* Network devices 125-1 through 125-N may also be powered by a local AC/DC wall adapter, instead of data distribution device 105. *Id.* at [0039]-[0040].

Data distribution device 105 may power itself and network devices 125-1 through 125-N from one of several power sources, including remote data distribution device 110 and independent power supply 115. *Id.* at [0032]. The device 105 switches between power supplies using "relays,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 96

transistors, or any other known switching device." *Id.* More specifically, as illustrated in Fig. 3, power detectors 350 and 355 of the exemplary data distribution device 205, which may be "voltage or current detectors…of any appropriate type known to one of ordinary skill in the art," indicate whether power is available from independent power supply 115 or uplink port 350, respectively, by sending a signal to process controller 340. *Id.* at [0049], [0056], Fig. 3. After process controller 340 determines which power supply to use, it sends a command signal to switch 380, "which may be a relay, one or more transistors, or any other type of switch which may be controlled by an electronic signal." *Id.* at [0051], [0047]. If the data distribution device is powered locally by the independent power supply, process controller 340 signals PoE controller 360 to set a signature resistance on uplink port 320 in accordance with IEEE 802.3af to inform closet gigabit switch 210 that device 205 does not require power. *Id.* at [0056].

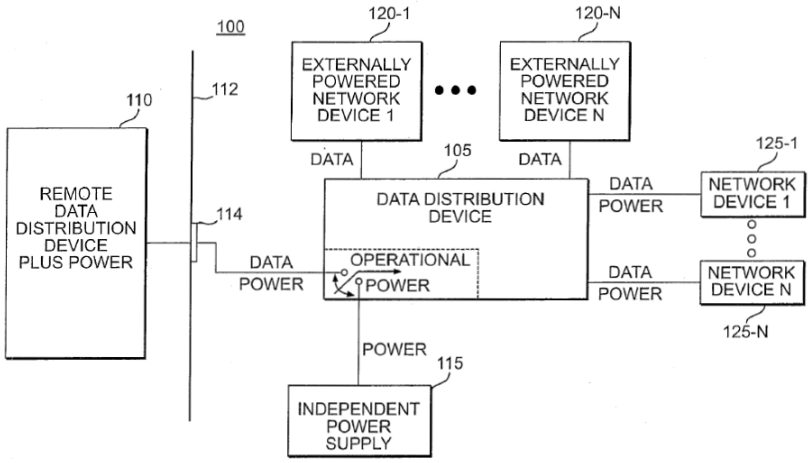


FIG. 1

Penning at Fig. 1.

Penning further teaches that the "[p]rocess controller 340 may provide a signal to PoE controller 360 in order to provide feedback to closet gigabit switch 210 regarding how much power to allocate and supply" to data distribution device 205. *Id.* at [0052]. PoE controller 360 may in

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 97

turn "set up a signature resistance in accordance with IEEE 802.3af, to signal a class 0, 1, 2, and/or 3 power signatures." *Id.* The closet gigabit switch 210 senses the resistance during initialization to provide the appropriate amount of power. *Id.* Process controller 340 may also "provide control signals to [PSE controller and power controller] PCPC 370 which may include instructions for providing the appropriate amount of power to VOIP telephone 215" according to the 802.3af standard. *Id.* at [0053], Fig. 3; *see also* [0063] ("the VOIP phone may include…a power controller 43 for…designating a power signature for the VOIP phone"); [0068] ("The network device may be provided with hardware circuitry, such as the power controller 435, which designates the power signature of the VoIP phone 400 and all of the associated auxiliary devices" connected to VOIP phone 400."). After requesting the power signature from VOIP phone 215, which may be class 0, 1, 2, or 3, the process controller may instruct the power controller in PCPC 370 to provide port 315 with the appropriate amount of power for use by VOIP telephone 215." *Id.* The PSE controller 370 may also collect the classification information from the VOIP telephone to send to process controller 340 to report back to the closet switch 210 for powering data distribution device 205. *Id.*

VOIP telephone may also include a USB port for connecting peripheral devices, as shown in Fig. 4. *Id.* at [0065]. The VOIP phone may include a current sensor to detect the power draw at USB port 415, which is used by process controller 435 to determine the total power consumption for the VOIP phone and any connected peripheral devices. *Id.* at [0065]-[0066]. Each time a peripheral device is connected to or disconnected from VOIP phone 400 and each time the VOIP phone is reset, the controller recalculates the total power available to the VOIP phone and the total power consumption of the VOIP phone and any peripheral devices. *Id.* at [0066], [0067], Fig. 5; *see also* [0085] ("[T]he power controller 435 may be configured to scan the auxiliary devices

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 98

periodically, e.g., every 3 seconds, to recognize each time an auxiliary device has been disconnected from the phone."). If the total required power is more than the total available power, the user may be prompted to remove the peripheral device. *Id.* The power management process terminates when the power consumption is adequately lowered—i.e., when the user removes the peripheral device. *Id.*

(4) Toebes

Toebes discloses "methods and apparatuses for providing inline power to multiple daisy chained devices in a wired data telecommunications network." Toebes at [0036]. Toebes explains that "inline power," also known as PoE, is a "technology for providing electrical power over a wired telecommunications network from power source equipment (PSE) to a powered device (PD) over a link section." *Id.* at [0015]. In accordance with the IEEE 802.3af standard, Toebes teaches that two processes must be accomplished in order to provide inline power: a discovery process to verify that the PD can receive inline power, and a classification process to determine an amount of power to provide to the PD. *Id.* at [0020].

The discovery process looks for an "identity network" at the PD, which "is one or more electrical components which respond in certain predetermined ways when probed by a signal from the PSE." *Id.* at [0021]. A simple identity network is a resistor, such as the 25,000Ω resistor called for by the IEEE 802.3af standard. *Id.* Toebes further explains that, in order to detect the resistor, the PSE applies some reduced inline power, measures the "return currents responsive to application of the discovery signals," and calculates the resistance. *Id.* at [0022]. If the identity network resistance is sensed, then the classification process may begin. *Id.* During classification, the PSE applies a classification-level voltage to the PD, which sends a classification current signal back to the PSE. *Id.* at [0023]. The PSE measures this current, which corresponds to a power "class" of the PD. *Id.* The discovery process prevents full inline power from being provided to

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 99

"legacy" devices—which are not adapted to receive inline power—and the classification process allows power to be efficiently allocated. *Id.* at [0024]-[0025].

In a basic exemplary configuration taught by Toebes, a POE enabled switch 102 with a PSE port 104 is coupled to a "first PSE-PD combination unit 108," which includes a first port 110 configured as a powered device (PD) and a second port 112 configured as power sourcing equipment (PSE). *Id.* at [0040], Fig. 2. Port 112 is connected to first port 116 of a second PSE-PD combination unit 18. *Id.* The second port 120 of the second unit is available for connecting to additional devices in the daisy chain. *Id.* As Toebes further explains, the three primary functional blocks of the PSE-PD device are: (1) "[t]he PD component 124 which acts as a PD power request unit to request power from a coupled PSE based on predefined current limits drawn by the PD in the power classification stage;" (2) "the summation unit 134 which sums power values from the PSE 126 with the power consumed;" and (3) the "PSE manager unit 140 which grants (or rejects) PD power requests from PDs coupled to PSE port 136." *Id.* at [0047].

When the PSE-PD combination unit is first connected to a PSE, it presents a first identity network such as "electrical resistors with certain resistance values corresponding to certain power classes" to the PSE. *Id.* at [0041]. The PD component uses the resistors to request maximum power from the PSE, and the PSE can grant or reject the request. *Id.* If the request is denied, the PD continues requesting less and less power, until the request is granted. *Id.* The granted power value is then presented to summation unit 134 in the PSE-PD combination device, which subtracts the measured or assumed value of the power consumed by the PSE-PD combination device from the granted power. *Id.*at [0044]. The summation unit calculates any leftover power and provides that value to the PSE component 136 of the PSE-PD combination device so that it can be made

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 100

available to a daisy chained PD unit, such as the second PSE-PD combination unit 138. *Id.* at [0044], Fig. 3.

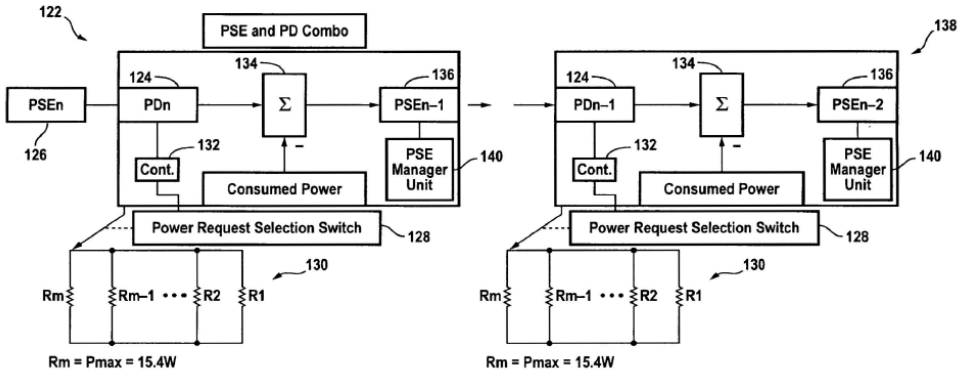


FIG. 3

Toebes at Fig. 3.

The operation continues with the second PSE-PD combination unit, which has its PD component 124 coupled to PSE component 136 of the first PSE-PD unit. *Id.* at [0049]. PRSS 128 of the second PSE-PD combination unit is set by default to select a resistor that requests maximum power from the first PSE-PD combination unit. *Id.* Once the power request is accepted (potentially after several failed requests), the first PSE-PD unit provides inline power to the second PSE-PD unit. *Id.* A new power classification cycle is triggered when the device is rebooted or when there is an interruption in connectivity to the PSE. *Id.* at [0047].

(5) Robbins

Robbins is directed to an "inexpensive means to power two PD's over a single network cable" which "overcome[s] a major disadvantage of conventional PoE systems." Robbins at [0007]. More particularly, Robbins teaches a PoE system with an endspan PSE 21, a midspan PSE 22, a mid-link PD 24, and a standard PD 25. *Id.* at [0023], Fig. 2. The mid-link PD uses power from one of the PSEs and conveys power from the other PSE to another PD in the link—which

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 101

may be a standard PD or another mid-link PD. *Id.* at [0024]. The advantage of this arrangement is that both PDs can be powered without laying a second network cable. *Id.* at [0025].

Rather than explicitly describing the basic components of a IEEE 802.3af compliant device, Robbins explains that "the complex circuitry inside the PSE ports that handles all the functions defined in the IEEE standard (detection, classification, current limiting, PD-disconnect sensing, etc.) are depicted in Fig. 3 as simple voltage source symbols 37 and 41" in mid-link PD 24. *Id.* at [0028]. Similarly, Robbins notes that "[t]he PD controller 39 [in mid-link PD 24] handles all the PD functions defined by the IEEE standard (detection, classification, in-rush current limiting, etc.)." *Id.* at [0029].

The exemplary mid-link PD illustrated in Fig. 7 includes a first PD controller 60 that outputs a signal 62 to second PD controller 61. *Id.* at [0039], Fig. 7. If the endspan PSE applies power to the mid-link PD, the first PD controller 60 disables second PD controller 61, which causes the controller 61 to disable detection and classification functions, stop conducting current to power supply 40, and appear high-impedance to the midspan PSE. *Id.* If the midspan PSE had been providing power to the mid-link PD, the disabled controller 61 will appear to the midspan PSE as an open circuit, and the midspan PSE will discontinue power. When voltage at controller 61 falls to a certain level, the control circuitry closes switch 63—which may be a mechanical or solid-state relay—allowing midspan PSE to detect and power the end-PD. *Id.* at [0039], [0036].

(6) Karam '280

Karam '280 is directed to "a method and apparatus for changing power class for a powered device, before or after the device power increases." Karam '280 at [0006]. "During operation, a first powered device, such as an IP telephone, receives power from a power source via a PoE device." *Id.* If a second powered device is connected to the first powered device, "the first powered device transmits a classification signal to the power source." *Id.* The power source then "performs

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 102

a powered device classification procedure to reclassify the first powered device, such as according to an IEEE 802.3af standard, and provide an increase amount of power to the first powered device." *Id.* The first powered device then provides some of that power to the second powered device. *Id.* This configuration is advantageous, as the second powered device "does not require additional equipment in order to operate," such as "a bulky power cube and cord." *Id.* at [0006], [0030]. The second device also does not need to be located near an external power supply, such as a wall outlet. *Id.* at [0030].

Karam '280 explains that an exemplary network system includes a power source 12, a first powered device 14, and a second powered device 16. *Id.* at [0020], Fig. 1. The network may provide power to the devices via PoE. *Id.* For example, "the power source 12 exchanges data signals with the first and second powered devices 14, 16 and transmits power signals to the first powered device 14 and also to the second powered device 16 via the first powered device 14." *Id.* The first powered device includes classification circuitry 20 with, by way of example, an operational amplifier 30 to convert voltage to current, a voltage divider, a first classification resistor RCLASS1 38, and a FET gate 40. *Id.* at [0033], Fig. 3. The second powered device includes connection circuitry 24, including a voltage divider, a FET gate 44, a second classification resistor RCLASS2 46, and a switch 48. *Id.*

When the first powered device is activated, RCLASS1 is placed in parallel with RCLASS2, such that the amount of current flowing through FET 40 = Vref/RCLASS1 + Vref/RCLASS2). *Id.* at [0035]. In other words, RCLASS2 in the second powered device increases the current 52 drawn through gate 40 during the classification process, and this increased current is provided to power source 12 as the classification signal 23. *Id.* This causes the power source to classify the first powered device 14 higher than it would be classified on its own, and provide additional power. *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 103

Control element 64 in the first powered device 14 controls gate 62 in response to current passing through node 50, such that the gate is open when a small amount of current passes through the node and remains closed when a large amount of current passes through the node. *Id.* at [0058]. When the gate is closed, current flows through the node 50 and through detection resistor RDETECT 66 in the second powered device. *Id.* at [0060]. The current measuring circuit 60 measures the current at node 50 and transmits the current value to detection circuitry 68, which detects the presence or absence of the second powered device 16. *Id.* at [0058]. The first powered device 14 can also detect decoupling of the second powered device 16. *Id.* at [0063].

(7) Diab '255

Lastly, Diab '255 is directed to a PoE system for providing power to a PD with unpredictable or variable levels of power draw. Diab '255 at [0014], [0019]. As with the previous references, the system taught by Diab '255 includes a PSE that transmits power to a PD, where the PD includes a PoE module which enables the PD to communicate with the PSE according to IEEE 802.3af. *Id.* at [0014]. The system may include multiple PDs (*Id.* at [0016]), and the PD includes a power module and a power FET for producing output PoE power based on power provided by the PSE. *Id.* at [0017], Fig. 2. Diab '255 teaches that where the PD has variable power draw—as is the case with a laptop computer, for example—the PSE may indirectly provide power to a rechargeable battery within the PD, instead of directly powering the PD, because a battery has a more stable power profile. *Id.* at [0023]. Under this arrangement, the PSE does not need to account for "wide fluctuations in power draw based on changes in use." *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 104

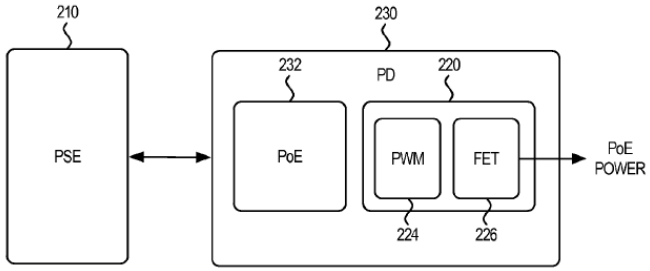


FIG. 2

Diab ’255 at Fig. 2.

An exemplary PD, illustrated in Fig. 3, includes regulation circuitry 330 for guiding power from an AC outlet to either the PD’s electronic circuitry 370 for use, or to the battery charging circuity 350 to charge battery 360. *Id.* at [0025], Fig. 3. The PD further includes switch 340 for powering electronic circuitry 370 from either the AC outlet or the battery 360. *Id.* In a second example illustrated in Fig. 4, the delivery of power from AC outlet 410 to electronic circuitry 480 and battery 470 is under control of a power management unit (PMU) 450. *Id. a*t [0028], Fig. 4. The PMU can monitor the current used to charge the battery using current control module 460 and adjust the battery charging if the current requirements of electronic circuitry 480 increase. PMU 450 includes a switch 450 to control provision of charging to the battery, which allows the device to cut-off charging current if the battery is fully charged. *Id.*

The process begins at step 502 in Fig. 5, where the PSE detects the PD by detecting the signature resistance, 25,000Ω, in the PD. *Id.* at [0034], Fig. 5. Then, the PSE identifies the class of the PD by measuring current drawn when voltage is applied to the PD at a classification range. *Id.* at [0035]. The resulting current measurement is used to classify the PD according to the IEEE 802.3af standard. *Id.* Based on the classification, the PSE provides power to the PD. *Id.* At step 508, power received from the PSE is routed to the battery charging circuit of the PD, and power from the battery is then used to power the PD. *Id.* at [0036].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 105

c) PoE Devices

U.S. Pat. App. Pub. No. 2005/0268120 A1 to Schindler et al. ("Schindler"), U.S. Pat. App. Pub. No. 2008/0235523 A1 to Hussain ("Hussain"), U.S. Pat. App. Pub. No. 2005/0044431 A1 to Lang et al. ("Lang"), U.S. Pat. App. Pub. No. 2006/0218420 A1 to Camagna et al. ("Camagna"), U.S. Pat. App. Pub. No. 2008/0016263 A1 to Diab et al. ("Diab '263"), U.S. Pat. App. Pub. No. 2006/0168459 A1 to Dwelley et al. ("Dwelley"), U.S. Pat. App. Pub. No. 2008/0005598 A1 to Landry et al. ("Landry"), U.S. Pat. App. Pub. No. 2006/0210057 A1 to Stanford ("Stanford"), MAX5922, and TPS2370 are each generally directed to the provision of power via PoE. While each of these references refers to PoE or the IEEE 802.3af standard, Hussain and Diab '263 explicitly incorporate IEEE 802.3af by reference.

(1) Schindler

Schindler is directed to a method for power delivery that includes coupling an ethernet cable with four wire pairs to a power delivery system and providing power to a PD on all four wire pairs. Schindler at [0003]. The system allows more power to be delivered to the PD and allows the PSE to provide variable power levels to a PD based on its changing power demands. *Id.* at [0006], [0016]. Schindler explains that one advantage of the system is "adaptability to multiport devices." *Id.* at [0025]. For example, a docking station could be coupled to an Ethernet jack, where the amount of power provided by the jack could be adjusted based on the number of devices attached to the docking station. *Id.*

Schindler teaches that the PSE 100 includes a controller 120, which controls switches 122 coupled to connectors 118A-D. *Id.* at [0019], Fig. 1. Schindler explains that switches 112, which are used to convey power from power source 124 to the connectors, may be diodes or "any components for regulating the power delivered to ports 118, such as mechanical, magnetic, or electrical relays." *Id.* at [0019]. Schindler further teaches that the PSE 100 may determine power

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 106

characteristics of the PD by monitoring the response of PD 102 to voltage and current values on ports 118. *Id.* at [0022]. For example, after detecting the power need of PD 102, the PSE may initially transmit power on all four ports 188, and reduce the number of ports after determining that the PD is not using all the power. *Id.* In another embodiment, the PSE and PD may exchange power information using IEEE 802.3af classification. *Id.* at [0024].

In operation, the PSE detects that a PD has been connected by providing power at a predetermined level and monitoring the response of the PD 102. *Id.* at [0027]. The PSE then determines a power level for the PD, and controller 120 applies power to the ports 118 based on the power requirements of the PD. *Id.* The PSE monitors PD power usage for changes; if there is a change, PSE determines whether the PD has been "powered off or disconnected from the network." *Id.* at [0028]. If the device has been powered off, the system returns to search for a PD, and the process ends. *Id.* If there has been a change caused by something other than the PD disconnecting or being powered off, the PSE determines a new power level for the PD and changes power accordingly. *Id.* at [0029].

(2) Hussain

Hussain is also directed to a PoE system comprising a PSE and a PD. Hussain teaches that the PSE includes a controller 218 that "detects and validates a compatible PD, determines a power classification signature for the validated PD, supplies power to the PD, monitors the power, and reduces or removes the power from the PD when the power is no longer requested or required." Hussain at [0026]. If the PSE determines that the PD is not compatible during the detection process, "the PSE can prevent the application of power to that PD device, protecting the PD from possible damage." *Id.* Hussain explains that "[t]he IEEE has imposed standards on the detection, power classification, and monitoring of a PD by a PSE in the IEEE 802.3af standard, which is incorporated herein by reference." Hussain at [0026].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 107

Hussain further teaches that, "[i]n order to conduct its management and control of PD 106, PSE 102 analyzes certain characteristics of PD 106, and the system as a whole, based on measurements taken at PD 106." *Id.* at [0032]. Example attributes determined by PSE 102 include "valid device detection, power classification, AC disconnect information, short circuit detection, PD load variations, various current measurements, overload conditions, and inrush conditions." *Id.* The PSE is designed to manage power based on the dynamic needs of the PD. *Id.* at [0025]. To that end, the PSE measures the voltage, current, and temperature of the PD so as to characterize its power requirements and implement management functions. *Id.*

More specifically, during initialization, the PD controller provides impedance signatures so that the PSE can recognize the PD as a valid PoE device. *Id.* at [0029]. A signature resistor is used to validate the PD, while a classification resistor is used to classify the PD. *Id.* During the detection process, the PSE probes the current and voltage drop at the PD to calculate the resistive signature of the PD. *Id.* at [0036]. If the signature is approximately 25KΩ, the PD is determined to have a valid signature. If the PD is deemed non-compatible, power will not be supplied. *Id.* After detection, the PSE uses power classification to determine the range of maximum power to be provided to the PD. *Id.* at [0037]. To classify the device, the PSE applies a voltage at the PD and measures the current through the PD's classification resistor. *Id.* Hussain teaches that detecting a PD before a normal level of power is supplied is important due to safety reasons, because legacy devices are not designed to accept inline power. *Id.* at [0053].

(3) Lang

Lang is directed to power delivery over a data wiring system with a power source, powered device, and cable for delivering both power and data. Lang at [0019]. Lang teaches that the power source includes a plurality of switches, which "may be electromechanical, or alternatively,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 108

configured as metal-oxide semiconductor field-effect transistors (MOSFET), bipolar junction transistors, equivalent circuitry, or any combination thereof," which form a programmable current limiting system. *Id.* at [0024]. Lang further teaches that the powered device has multiple signature resistors used for detection, and for signaling high and low power modes to the power source. *Id.* at [0032], [0037]. In operation, the power source senses the current through the signature resistors to detect a valid powered device and determine whether the device is requesting a high-powered mode. *Id.*

(4) Camagna

Camagna is directed to "a system and method operable to provide a power feed on differential cable pairs to network attached powered devices (PD)." Camagna at [0009]. Camagna teaches that the system follows the detection scheme set forth in the IEEE 802.3af standard, which allows the system "to be backward compatible with non-powered systems," because "the DC voltage applied [during detection] will begin at a very low voltage and only begin to deliver power after confirmation that a POE device is present." *Id.* at [0073]. The system also follows the classification procedure to determine the amount of power needed by the powered device. *Id.* at [0072]. Specifically, the PSE applies a voltage to the PD and "measures the current to determine the power class of the device." *Id.* at [0073].

(5) Diab '263

Diab '263 similarly describes a PoE system that implements the detection and classification schemes outlined in IEEE 802.3af. Diab '263 is directed to a PoE system with a PSE that controls its voltage supply based on the dynamic needs of the PD. Diab '263 at [0027]. "More specifically, the PSE controller 218 measures the voltage, current, and temperature of the outgoing and incoming DC supply lines so as to characterize the power requirements of the PD 106." *Id.* The PSE controller also "detects and validates a compatible PD, determines a power classification

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 109

signature for the validated PD, supplies power to the PD, monitors the power, and reduces or removes the power from the PD when the power is no longer requested or required." *Id.* at [0028]. Diab '263 explains that "IEEE has imposed standards on the detection, power classification, and monitoring of a PD by a PSE in the IEEE 802.3af standard and the IEEE 802.3 standard." *Id.* at [0028].

(6) Dwelley

Dwelley is directed to a PoE system that implements the detection and classification schemes outlined in IEEE 802.3af, and provides for a third signature that is not described in the standard for communicating additional information about the PD. Specifically, Dwelley discloses a PoE system where "[t]he PSE 12 may interact with each PD in accordance with the IEEE 802.3af standard." Dwelley at [0038]. This means that "the PSE 12 and the PD participate in the PD detection procedure, during which the PSE 12 probes a link to detect the PD" and determine whether "the PD detection signature… is valid or non-valid." *Id.* "While the valid PD detection signature indicates that the PD is in a state where it will accept power, the non-valid PD detection signature indicates that the PD is in a state where it will not accept power." *Id.* If the PD is valid, the PD may optionally present "a classification signature to the PSE to indicate how much power it will draw when powered up." *Id.* at [0039]. Then, "[b]ased on the determined class of the PD, the PSE applies the required power to the PD." Dwelley at [0039]. Dwelley additionally teaches that the PD may present a *third signature* to communicate additional information, such as "a special operating power level different from the standard IEEE 802.3af levels, or [] a system serial number that uniquely identifies the PD." *Id.* at [0044]. The third signature may be provided before power is applied to the PD or after power is provided. *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 110

(7) Landry

Landry is directed to a PoE system with a PD having an adjustable current limiter. Landry at [0016]. Landry teaches that the PD also includes PoE protocol circuitry, which incorporates a PoE detection and classification circuit that follows the IEEE 802.3af standard. *Id.* at [0017]. Landry further explains that, while only a single PD is shown, the PSE "may be coupled to multiple powered devices and may provide power and data to each of the multiple powered devices," which may have different power requirements. *Id.* at [0018].

During the detection process, the PCE of Landry's system applies a voltage to the PD and "monitors a received current" or "a received voltage" to detect a resistance within the expected range. *Id.* at [0003]. If a valid device is detected, the PSE may optionally classify the device by applying a classification voltage to the PD and measuring the resulting current, which is associated with a power class. *Id.* at [0004]-[0006].

(8) Stanford

Stanford is directed to a PoE system with a PSE configured to provide power to a high-power PD over all four pairs of conductors in an Ethernet link. Stanford at [0003], [0011]. Stanford explains that, according to the IEEE 802.3af standard, "[t]he main functions of the PSE are to search the link for a PD requesting power, optionally classify the PD, supply power to the link if a PD is detected, monitor the power on the link, and disconnect power when it is no longer requested or required." *Id.* at [0007]. The PD participates in the detection procedure "by presenting a PoE detection signature defined by the IEEE 802.3af standard." *Id.* Stanford further teaches that, "[i]f the detection signature is valid, the PD has an option of presenting a classification signature to the PSE to indicate how much power it will draw when powered up." *Id.* at [0008]. Based on the class, "the PSE applies the required power to the PD over the data pairs." *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 111

(9) MAX5922

MAX5922 is a single port network power switch for Power-Over-LAN that complies with the IEEE 802.3af standard. MAX5922 at 1. The device is "specifically designed for power-sourcing equipment (PSE)" and "provides power devices (PD) discovery, classification, current limit, and other necessary functions for an IEEE 802.3af compliant PSE." *Id.* The MAX5922 operates in three modes: "PD detection mode, PD classification mode, and power mode." *Id.* at 12. The MAX5922 performs PD detection by forcing a probe voltage and sensing the resulting current. *Id.* The MAX5922 uses the current measurement to check for a valid PD resistive signature. *Id.* After detection, the MAX5922 enters classification mode. *Id.* at 15. Again, the MAX5922 forces a voltage and measures the current, which corresponds with the class of the PD. *Id.* The MAX5922 also has a "zero-current detection function," which "monitors the output for an undercurrent condition and eventually turns off the power to the output if the PD is disconnected." *Id.* at 16.

(10) TPS2370

TPS2370 is an IEEE 802.3af compliant power interface switch for PDs. TPS2370 at 1. The TPS2370 acts "as an interface between the power sourcing equipment (PSE) and the powered device (PD)" and "performs all detection, classification, inrush current limiting, and switch FET control that is necessary for compliance with the IEEE 802.3af Standard." *Id.* at 1. The TPS2370 datasheet explains that "[a] powered device (PD) draws power or requests power by participating in a PD detection algorithm," which "requires the power sourcing equipment (PSE) to probe the link looking for a valid PD." *Id.* at 7. The PSE probes the link by sending out a voltage, and a valid PD detects this voltage and places a resistance of between 23.75 kΩ and 26.25 kΩ across the power lines. *Id.* "On detecting this current, the PSE concludes that a valid PD is connected at the end of the ethernet cable and is requesting power." *Id.* The PSE can then

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 112

optionally initiate a classification procedure, which "is used by the PSE to determine the maximum power required by the PD during normal operation." *Id.* To determine the PD's power class, the PSE increases the voltage across the power lines, and the amount of current drawn by the PD determines the classification according to the IEEE 802.3af standard.

d) Dual-Role PoE Device

Biederman, discussed above along with other daisy chain PoE devices, also discloses a dual-role combination PD/PSE device that can swap between PD and PSE functions depending on the connected device. *See, e.g.,* Biederman at [0034], Fig. 2.

U.S. Patent App. Pub. No. 2008/0028237 A1 to Knight ("Knight") is similarly directed to a device "capable of communicating power and data through a single connector to another device," where the device may source or sink power. Knight at [0024], [0039]-[0040]. The device may be, for example, "a dedicated network connection device…, [or] a portion of a computer, robot, [or] network appliance." *Id.* at [0031]. Knight teaches that the device may connect to multiple other devices and enable communication between them according to PoE, Firewire, USB, or similar communication protocols. *Id.* at [0031]-[0032], [0001], [0024].

Knight further explains that, when a connection is made, the device may "first attempt[] to connect as a power source, then attempt[] to connect as a power sink if the power source attempt fails." *Id.* at [0048]. Alternatively, the device "may be configured to attempt to connect as a power sink initially, then attempts as a power source secondarily." *Id.* The sink/source negotiation process "may be through sensing status and communicating through the power connections." *Id.* at [0047]. "One example of such communication may be for a device to configure a specific resistance along the power connections to indicate that it may sink power," in which case "the connecting device may sense the resistance and then begin supplying power to the first device." *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 113

Knight teaches that the device 102 with the power management system 124 may include connector interfaces 104, 106, 108, and 110 for connecting to devices 138, 140, 142, and 144, as well as a battery bank voltage source 126 which "may be used to store power during certain times and discharge power during other times." *Id.* at [0025]-[0026]. For example, in a robotic application where the device 102 may be mounted in a charging base, "the battery bank 126 may be charged through the outside power source 136 or through power supplied through one of the connector interfaces 104, 106, 108, and 110" during a charging phase, and "[w]hen the robot is mobile, the charging source may be disconnected and the battery bank 126 may supply power to the device 102 and other connected devices." *Id.* at [0025]. More particularly, "[a]ny or all of the devices 138, 140, 142, or 144 may be able to supply power through the respective connector interfaces to charge the battery bank 126," and "any of the devices 138, 140, 142, and 144 may draw power through the connector interfaces that would discharge the battery bank 126." *Id.* at [0029]. "In some cases, the power management system 124 may receive power from one or more of the remote devices, distribute power to other remote devices, and charge or discharge the battery bank 126 as appropriate….if the power source is greater than the total power drain for external devices….If the power source is less than the total power drain, the battery bank 126 may be discharged to supplement the power source." *Id.*

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 114

Furthermore, to the extent that it is determined that any of the above references do not disclose a particular claim element, it would have been obvious to modify the teachings of that reference to include such element as taught in any other of the above references that discloses such element (as documented in the claim charts attached as E-1 through E-19).

For example, to the extent that it is determined that any of the above references do not disclose a "power delivery circuit comprising…a voltage source configured to generate a voltage," as recited in claim 1, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Biederman, Knight, or Diab '255. Biederman teaches a combination PD/PSE unit that can swap between PD and PSE functions depending on the connected device. *See, e.g.,* Biederman at [0034], Fig. 2. Biederman discloses that the PSE portion of the unit contains its own 48 Volt power supply. *Id.* at Fig. 5 (supply 70), Fig. 6 (supply 80), [0038]-[0039]. Power supply block 70/80 may be a "conventional grid-powered or battery-powered power supply." *Id.* at [0039]. Providing the combination PD/PSE device with its own PSE power supply allows the device to power itself (in PSE+PD mode) or immediately adjacent devices in a daisy chain in certain emergency situations when connections to other devices in the chain that had previously been providing power are cut. *Id.* at [0041], [0044]-[0046]. This would allow "the normal effects (e.g., data interruption, power interruption) of a cut in the cabling coupling the devices together [to] be avoided." *Id.* at [0044]. Thus, it would have been obvious to a POSITA to modify any of the PoE references to provide a combination PD/PSE device with its own power supply block, in order to minimize power interruptions in the event of cable cuts and provide power redundancy.

Knight teaches a dual-role PoE device with a battery 126 and power management system 124 that can be used to store energy in battery 126 during certain times and discharge power from

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 115

the battery during other times. Knight at [0025]-[0026]. More specifically, any of the devices 138, 140, 142, or 144 connected to the dual-role device 102 "may be able to supply power through the respective connector interfaces to charge the battery bank 126," and "any of the devices 138, 140, 142, and 144 may draw power through the connector interfaces that would discharge the battery bank 126." *Id.* at [0029]. Knight explains that this arrangement is useful for mobile robotic applications, in which the device 102 may be in a charging phase when mounted in a charging base, and in a power supplying phase when mobile. *Id.* at [0025]-[0026], [0029]. Accordingly, it would have been obvious to a POSITA to modify any of the above references to provide for a dual-role rechargeable device in certain mobile applications, where it is desirable for the device to recharge when at rest and provide power to auxiliary devices when on the move. *Id.*

Diab '255 similarly discloses a PoE system with a PSE that can provide power directly to a PD, or indirectly to a rechargeable battery voltage source within the PD, which has a more stable power use profile. Diab '255 at [0023]. Diab '255 explains that such an arrangement is advantageous when a PSE is connected to a PD with variable and unpredictable power usage, because a rechargeable battery tends to have a more stable power profile that does not need to be accounted for by the PSE. *Id.* Thus, it would have been obvious to a POSITA to modify any of the PoE references in view of Diab '255 to provide for the provision of power to a PD that has variable power requirements—such as a laptop—so that the PSE does not need to account for "wide fluctuations in power draw based on changes in use." *Id.* Such a combination reflects no more than the use of a known technique—charging a battery—to improve similar PoE devices in the same way.

As an additional example, to the extent that it is determined that any of the above references do not disclose "a power relay switch configured to relay, when closed, the voltage generated by

the voltage source," as recited in claim 1, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Schindler, Biederman, Penning, Robbins, and Lang, which disclose a variety of switches for relaying voltage from a PSE to a PD, including relay switches. *See, e.g.,* Schindler at [0019] ("In one embodiment, diodes 112 may be used as a switch, and may be substituted with any components for regulating the power delivered to ports 118, such as mechanical, magnetic, or electrical relays."); Biederman at [0038] ("Switches (or other equivalent Switching equipment Such as diodes, transistors, relays and the like as will now be apparent to those of ordinary skill in the art) are provided to enable either the PD or the PSE (or neither or both) modes at port 61."); Penning at [0032] ("The switching of power supplies for the data distribution device may be performed using relays, transistors, or any other known switching devices."); Robbins at [0036] ("In another embodiment, the power switch 52 shown in FIG. 6 is a relay (either mechanical or solid-state) that is controlled by circuitry."); Lang at [0024] ("The switches 270 may be electromechanical, or alternatively, configured as metal-oxide semiconductor field-effect transistors (MOSFET), bipolar junction transistors, equivalent circuitry, or any combination thereof."). Such switches are well known in the art, and any suitable type of power switch could be selected by a POSITA as a matter of routine design choice. At a minimum, such a combination reflects a simple substitution of one known element—a relay—for another switching mechanism to obtain predictable results.

As an additional example, to the extent that it is determined that any of the above references do not disclose "a signature resistor," as recited in claim 1, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least IEEE 802.3af, Karam '799, Diab '255, Toebes, Hussain, Lang,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 117

Camagna, Diab ’263, Dwelley, Landry, MAX5922, TPS2370, and Stanford, which disclose the basic components of a PoE system under the IEEE 803.2af standard, including the signature resistor for PD detection. Given that the above references explicitly refer to the IEEE 802.3af standard, such a combination would have been obvious to a POSITA.

It also would have been obvious to modify the teachings of any of the above references to include the “signature resistor” feature in view of the knowledge of a POSITA and the teachings of at least Penning and Karam ’799. Specifically, Penning teaches a PoE device 205 with power detectors 355 and 350 for determining whether power is available from connected devices 115 and 210. Penning at Fig. 3, [0049], [0056]. Penning teaches that the detectors may be “either voltage or current detectors…of any appropriate type known to one of ordinary skill in the art.” *Id.* at [0049]. The detectors send signals to process controller 340, which determines which power supply to use and sends a command signal to switch 380 to switch between the sources. *Id.* at [0049], [0051], [0056], [0047]. Karam ’799 teaches that one type of current sensor is a “current sense resistor.” Karam ’799 at [0058], Fig. 5. It would have been obvious to a POSITA to provide such power detectors in a device that may be able to receive power from multiple sources, in order to switch between the sources. Such a combination would merely reflect the use of a known technique to improve similar devices in the same way.

As an additional example, to the extent that it is determined that any of the above references do not disclose “a load detector connected to the switch and configured to read a load current flowing therethrough so as to detect a load in one of the connected devices, and to extract information about the connected device based on the load current,” as recited in claim 1 and in similar form in claim 7, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least IEEE

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 118

802.3af, Karam ’799, Diab ’255, Toebes, Hussain, Lang, Camagna, Diab ’263, Dwelley, Landry, MAX5922, TPS2370, and Stanford, which disclose the basic components of a PoE system under the IEEE 803.2af standard, including the means by which the PSE detects a valid PD and classifies its power requirements using current measurements. Given that the above references explicitly refer to the IEEE 802.3af standard, such a combination would have been obvious to a POSITA.

As an additional example, to the extent that it is determined that any of the above references do not disclose “wherein the information extracted by the load detector comprises information regarding whether the connected device is powered on or powered off,” as recited in claim 1 and in similar form in claim 7, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Karam ’799, Penning, and Schindler, which each teach a PoE system in which a first device detects whether a connected device is powered off for the purpose of discontinuing power. *See, e.g.*, Karam ’799 at [0058] (“If the control circuitry 78 sees that power is applied and then the current in current sensor 92 goes to zero (device at second port 74 is off or disconnected) while current is still being used by third port 76 then it forces normally closed switch 90 to open making sure that a ‘hot cable’ situation is not created at second port 74 by removing the inline power to second port 74.”); Penning at [0067] (“The power management process 500 is terminated upon…powering down the VoIP phone 400.”); Schindler at [0028] (“If there is a change in the power usage of device 102, power delivery system 100 determines whether the device has been powered off or disconnected from the network at step 210. If device 102 has been powered off, then system 100 returns to a search for a powered device, and the method is at an end.”). It would have been obvious to a POSITA to modify any of the above references in view of Karam ’799, Penning, or Schindler to preserve power and avoid a “hot cable” situation when a connected device is powered off.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 119

Moreover, any such combination would merely reflect the use of known technique to improve similar devices or methods in the same way.

As an additional example, to the extent that it is determined that any of the above references do not disclose "wherein the load detector is further configured to detect removal of one of the plurality of devices from the network," as recited in claim 5 and in similar form in claim 9, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least IEEE 802.3af, Karam '799, Karam '280, Penning, MAX5922, and Schindler. As one example, Karam '799 discloses that the power switch S5 is "closed only while current [i]s being drawn from third connector 56 so that if the device were unplugged from third connector 56 the power would turn off." Karam '799 at [0051]. The above references refer to the IEEE 802.3af standard, which provides that one of the "PSE's main functions [is] to…scale power back to the detect level when power is no longer requested or required," where "an unplugged link section is one instance when power is no longer required." IEEE 802.3AF at 29. Accordingly, it would have been obvious to a POSITA that the PSE should be able to detect when a device is unplugged, so that the PSE can stop providing power. This would conserve power and prevent a legacy device from accidentally being powered when it is plugged in immediately after a valid PD device. *See, e.g.,* Mendelsen, All You Need to Know About Power over Ethernet (PoE) and the IEEE 802.3af Standard, at 18 ("When a PD is disconnected, there is a danger that it will be replaced by a non-PoE-ready device while power is still on. Imagine disconnecting a powered IP phone utilizing 48 Vdc, then inadvertently plugging the powered Ethernet cable into a non-PoE notebook computer. What's sure to follow is not a pretty picture. The standard defines two means of disconnection, DC Disconnect and AC Disconnect, both of which provide the same functionality - the PSE shutdowns power to a disconnected port within

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 120

300 to 400ms. The upper boundary is a physical human limit for disconnecting one PD and reconnecting another."). Accordingly, it would have been obvious to a POSITA to modify any of the above references to detect removal of a PD in order to shut down power. Such a combination would merely reflect the use of known technique to improve similar PoE devices or methods in the same way.

As an additional example, to the extent that it is determined that any of the above references do not disclose "[a] method of delivering power to one of a plurality of devices connected in a daisy chain," as recited in claim 7, it would have been obvious to modify the teachings of that reference to include these features in view of the knowledge of a POSITA and the teachings of at least Biederman, Karam '799, Karam '280, Diab '255, Penning, Toebes, and Robbins, which each disclose the provision of power via PoE to multiple devices arranged in a daisy chain. Karam '799, Karam '280, and Robbins further explain why daisy chaining devices in a PoE system is advantageous. *See, e.g.,* Karam '799 at [0054] ("A device such as that just described would be helpful to people who have a need to charge cellular phones or power other low-power equipment from the inline power available on network cabling. It would also be useful in situations where low-power sensors (such as IP television cameras) need to be wired in a daisy chain configuration and powered from a wired network using inline power."); Karam '280 at [0030] ("[T]he modular powered device 16 receives power directly from the first powered device 14 for operation. As a result, the modular powered device 16 does not require additional equipment, such as a bulky power cube and cord, in order to operate. Additionally, the modular powered device 16 does not need to be located in the vicinity of an external power supply, such as a wall outlet, in order to operate."); Robbins at [0025] ("An advantage of the mid-link PD 24 is that it can be installed without laying in a second network cable….No new network cable must be routed through the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 121

infrastructure of the building."). In view of the above, it would have been obvious to a POSITA to modify any of the above PoE references to have daisy chain functionality, in order to provide power to devices without requiring extra equipment or a local power supply.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to systems and methods for delivering power to devices connected in a network via PoE, including means for detecting connected devices and determining their power requirements. Furthermore, several of these references are specifically directed to the provision of power to devices connected in a daisy-chain configuration.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards systems and methods for delivering power to devices connected in a network via PoE, and (5) the predictable results obtained in combining the different elements of the prior art.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 122

The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

a) Exemplary Combinations and Modifications

As illustrated in the claim chart attached as Exhibit E-2, Karam '799, alone or in combination with Schindler, Biederman, Penning, Robbins, or Lang (as shown in their respective claim charts), discloses or renders obvious all elements of the '712 Asserted Claims.

Similarly, as illustrated in Exhibit E-1, Biederman, alone or in combination with (a) IEEE 802.3af, Karam '799, Diab '255, Toebes, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry, MAX5922, TPS2370, or Stanford (as shown in their respective claim charts); and (b) Karam '799, Penning, or Schindler (as shown in their respective claim charts), discloses or renders obvious all elements of the '712 Asserted Claims.

Furthermore, as illustrated in Exhibit E-5, Knight, alone or in combination with (a) IEEE 802.3af, Karam '799, Diab '255, Toebes, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry, MAX5922, TPS2370, or Stanford (as shown in their respective claim charts); (b) Karam '799, Penning, or Schindler (as shown in their respective claim charts); and (c) Schindler, Biederman, Penning, Robbins, or Lang (as shown in their respective claim charts), discloses or renders obvious all elements of the '712 Asserted Claims.

As illustrated in Exhibit E-3, Penning, alone or in combination with (a) IEEE 802.3af, Karam '799, Diab '255, Toebes, Hussain, Lang, Camagna, Diab '263, Dwelley, Landry, MAX5922, TPS2370, or Stanford (as shown in their respective claim charts); and (b) Karam '799 or Schindler (as shown in their respective claim charts), discloses or renders obvious all elements of the '712 Asserted Claims.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 123

As illustrated in Exhibit E-4, Toebes, alone or in combination with (a) Karam ’799, Penning, or Schindler (as shown in their respective claim charts); and (b) Schindler, Biederman, Penning, Robbins, or Lang (as shown in their respective claim charts), discloses or renders obvious all elements of the ’712 Asserted Claims.

As illustrated in Exhibits E-6 through E-15, E-18, and E-19, the general PoE references, alone or in combination with (a) any of the daisy chained PoE references, including Karam ’799, Karam ’280, Penning, or Toebes (as shown in their respective claim charts); and (b) Karam ’799, Penning, or Schindler (as shown in their respective claim charts), discloses or renders obvious all elements of the ’712 Asserted Claims.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the ’712 Patent:

- Knight in view of IEEE 802.3af.
- Knight in view of Karam ’799.
- Knight in view of IEEE 802.3af and Schindler.
- Knight in view of Karam ’799 and Schindler.
- Knight in view of Karam ’799 and Penning.
- Biederman in view of IEEE 802.3af.
- Biederman in view of Karam ’799.
- Biederman in view of Karam ’799 and Penning.
- Karam ’799 in view of Penning.
- Penning in view of IEEE 802.3af.
- Penning in view of Karam ’799.
- Penning in view of Schindler.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 124

- Toebes in view of Schindler.
- Toebes in view of Schindler, Karam '799, and Penning.

B. Invalidity of the '712 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '712 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '712 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- "a load detector connected to the switch and configured to read a load current flowing therethrough so as to detect a load in one of the connected devices, and to extract information about the connected device based on the load current" (claim 1)
- "a signature resistor connected to the switch and configured to detect a power source from one or more of the connected devices;" (claim 1)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

The written description and enablement issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

C. Invalidity of the '712 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '712 Patent, to the extent such positions can be understood from Plaintiff's Infringement

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 125

Contentions, Defendant asserts that the Asserted Claims of the ’712 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- “a load detector connected to the switch and configured to read a load current flowing therethrough so as to detect a load in one of the connected devices, and to extract information about the connected device based on the load current” (claim 1)
- “a signature resistor connected to the switch and configured to detect a power source from one or more of the connected devices;” (claim 1)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff’s apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

VIII. THE ASSERTED CLAIMS OF THE ’520 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits F-1 through F-9, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the ’520 Patent.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 126

1. The ’520 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the ’520 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit F-1 through F-9 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the ’520 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the ’520 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date	Short Name	Exhibit Number
U.S. Patent Pub. No. 2008/0084834	Filed: Oct. 9, 2006 Pub’d: April 10, 2008	Stanek	F-1
U.S. Patent Pub. No. 2006/0095596	Filed: Nov. 3, 2004 Pub’d: May 4, 2006	Yung	F-2
WIPO Patent Pub. No. 2008/117234	Filed: Mar. 25, 2007 Pub’d: Oct. 2, 2008	Van Willigen	F-3
U.S. Patent Pub. No. 2008/0247544	Filed: April 2, 2007 Pub’d: Oct. 9, 2008	Candelore	F-4
U.S. Patent Pub. No. 2006/0076977	Filed: Sep. 20, 2004 Pub’d: Apr. 23, 2006	Zhu	F-5

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 127

U.S. Patent No. 6,574,233	Filed: Apr. 9, 1999 Pub'd: June 3, 2003	Fuller	F-6
U.S. Patent No. 7,639,765	Filed: July 14, 2006 Pub'd: Dec. 29, 2009	Suzuki	F-8
U.S. Patent Pub. No. 2007/0200859 U.S. Patent No. 5,928,345 U.S. Patent Pub. No. 2005/0021892 WIPO Patent Pub. No. 2007/074611 U.S. Patent Pub. No. 2006/0104396 U.S. Patent No. 10,033,553	Filed: Jan. 31, 2007 Pub'd: Aug. 30, 2007 Filed: Sep. 30, 1996 Pub'd: July 27, 1999 Filed: July 22, 2004 Pub'd: Jan. 27, 2005 Filed: Dec. 5, 2006 Pub'd: July 5, 2007 Filed: Oct. 18, 2005 Pub'd: May 18, 2006 Filed: Nov. 22, 2007 Pub'd: July 24, 2018	Banks Tetzlaff Kim Takatsuji Soriano Ichimura	F-9

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Philips Semiconductors	The I²C-Bus Specification	Dec. 1998	I2C Specification	F-7
Srikanth Mujiga & Srihari Sukumaran	Modeling and Test Generation Using SAL for Interoperability Testing in Consumer Electronics	Nov. 6, 2007	Mujiga	F-9
HDMI Licensing, LLC	High-Definition Multimedia Interface Specification, Version 1.3a	Nov. 10, 2006	HDMI 1.3a Specification	
HDMI Licensing, LLC	High-Definition Multimedia Interface Specification, Version 1.3a, Supplement 1 – Consumer Electronics Control (CEC)	Nov. 10, 2006	HDMI-CEC Supplement	
Raida Al-Alawi & A. J. Al-Sammak			Al-Alawi	

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 128

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
	Design of a Multicode Bi-Phase Encoder for Data Transmission	February 2006		

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '520 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- HDMI Version 1.3a or earlier and the HDMI-CEC Supplement
- USB 2.0 or earlier and/or USB On-The-Go Revision 1.0a
- I^2C Bus, Version 2.0 or earlier

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '520 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 129

inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The ’520 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the ’520 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits F-1 through F-9, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits F-1 through F-9 with each other, at least because all of these references relate to transmission of information from a transmitting device to a receiving device over a control bus, and determining which device has control of the bus.

For example, U.S. Patent Publication No. 2008/0084834 (“Stanek”) teaches “[s]ystems and methods for serial data transmission having at least two different operating modes dependent on the connected signaling device.” Stanek, Abstract. Stanek further discloses that “[f]or HDMI compatible devices, a control channel is formed of three lines (SCL, SDA and DDC/CEC ground). Control signals are transmitted on this channel in accordance with the I2C bus protocol. The device may be able to detect and analyze these control signals and thus conclude the presence of a HDMI device when the correct signal sequence is detected.” *Id.* ¶ 46.

Furthermore, U.S. Patent Publication No. 2006/0095596 (“Yung”) teaches “a method and a device for a host control unit to communicate over a protocol compliant bus via the introduction

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 130

of an auxiliary control unit that handles communications to and from the protocol compliant bus." Yung, ¶ 7. Yung further teaches that "[w]hen acting as an initiator, the command control unit is adapted to receive a high-level command from a host control unit, and convert and transmit the high-level command to a remote command control unit via a bi-directional link in a format of frame. When acting as a follower, the command control unit is adapted to receive high-level commands from the bi-directional link as frames, and convert and send the frames to the host control unit as high-level commands." *Id.* ¶ 10.

Furthermore, WIPO Patent Publication No. 2008/117234 ("Van Willigen") teaches "a method of distributing audio-visual data between a first audio-visual device and a second audio-visual device using a digital display interface defined by an industry standard, the interface comprising a set of lines, the interface comprising a first transport channel for carrying video data in uncompressed form, the method comprising, at the first audio-visual device: sending or receiving audio-visual data in a compressed form using a second transport channel of the interface, wherein the second transport channel uses a subset of lines of the interface which are reserved in the standard for a different use." Van Willigen, 4:8–15.

Furthermore, U.S. Patent Publication No. 2008/0247544 ("Candelore") teaches "a method and apparatus for authentication of communications in digital communication systems having multiple input devices employing multiple interfaces." Candelore, ¶ 3. Candelore further teaches that "the HDMI-compatible device that is transmitting information may be referred to as a HDMI source device, while the HDMI-compatible device receiving the transmitted information is referred to as a HDMI sink device. It can be seen that audio, visual, control, status and CEC control information may be transmitted via one cable in the system. Of course, in a bidirectional system in which information is flowing both directions between various HDMI-compatible devices, such

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 131

as between a TV and a module, like a STB or SBB, each device will have an HDMI transmitter and HDMI receiver and may be referred to as a source or sink device depending upon whether it is transmitting or receiving information." *Id.* ¶ 50.

Furthermore, U.S. Patent Publication No. 2006/0076977 ("Zhu") teaches a "modified USB 1.1 system 200 including a microcontroller 205, an USB 1.1 device 201 and an USB 1.1 host 202 and the mixed signal interface circuit 208 to communicate seamlessly with an USB 2.0 OTG device 209. The full interface uses both software programming of the microcontroller device 205 and the hardware interface 208. The USB 2.0 OTG device 209, which may be either single role (slave) or dual-role (host/slave), is connected to the USB 1.1 system 200 through USB connectors 207 and 212 and USB cable 210." Zhu, ¶ 58.

Furthermore, U.S. Patent No. 6,574,233 ("Fuller") teaches a "connection is a communications bus that has a plurality of signal lines for conducting a first set of signals (a first protocol), including critical control signal lines for conducting critical control signals of the first set of signals. The first device transmits or receives the first set of signals on the signal lines, including transmitting and receiving the control signals on the control signal lines. The first device also transmits or receives a second set of signals (a second protocol) including control signals, on the signal lines other than the critical control signal lines for the first protocol." Fuller, 2:8–18. Fuller further teaches that "[a]t the beginning of a bus 100 transaction cycle, a bus 100 interface circuit 110 of each device 104-105 checks whether its device is the bus master, at steps 300 and 350. (A device becomes bus master by winning bus access contention, for example. Alternatively, the state of the system (active, standby) determines who is bus master.)" Fuller, 3:35–40.

Furthermore, U.S. Patent No. 7,639,765 ("Suzuki") teaches "an apparatus and a system which achieve bidirectional communication over a single line." Suzuki, 1:15-17. Suzuki further

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 132

teaches that "[s]ince CEC communication is bidirectional communication, a plurality of transmitters may perform transmission simultaneously. Therefore, during transmission, bus arbitration needs to be performed for a period of time defined by the standard, and the arbitration period gate pulse signal S109 c indicating the arbitration period is output." *Id.* at 9:11-17.

Furthermore, Philips Semiconductors, *The I2C-Bus Specification* ("I2C Specification") teaches that "[t]wo wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus." I2C Specification at 6. I2C Specification further teaches that "[t]he possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus." *Id.* at 7.

Furthermore, Srikanth Mujiga & Srihari Sukumaran, *Modeling and Test Generation Using SAL for Interoperability Testing in Consumer Electronics* ("Mujiga") teaches that "The High-Definition Multimedia Interface (HDMI) [1] is used to transmit digital audio-visual signals from source devices like DVD players, set-top boxes, etc., to sink devices like television sets, projectors and other displays. HDMI is capable of carrying high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI includes three separate communication channels, TMDS channel for carrying all audio and video data as well as auxiliary data, the DDC channel, which is used by an HDMI source to determine the capabilities and characteristics of the sink and the CEC channel which is used for high-level user functions such as automatic setup tasks or tasks typically associated with infrared remote control usage." Mujiga at 33. Mujiga further teaches that ""CEC is based on a bus system and all the transactions on the CEC bus consist of an initiator and one or more followers. The initiator sends the CEC frame (CEC

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 133

message and data) and the followers respond to the CEC message. There can be only one CEC frame at any time on the CEC channel. The CEC bus arbitration ensures collisions are spotted and reliable messaging can be achieved. It does this in a completely static priority-based manner based on the device's logical address." *Id.* at 34.

Furthermore, HDMI Licensing, LLC, *High-Definition Multimedia Interface Specification, Version 1.3a* ("HDMI 1.3a Specification") and HDMI Licensing, LLC, *High-Definition Multimedia Interface Specification, Version 1.3a, Supplement 1 – Consumer Electronics Control (CEC)* ("HDMI-CEC Supplement") together teach an interface "for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available. HDMI can also carry control and status information in both directions." HDMI 1.3a Specification at 1. The HDMI-CEC Supplement further discloses that "[t]he initiator provides bit timing and bit leading edges. Only one initiator is allowed at any one time. A control signal line arbitration mechanism avoids conflict when more than one initiator begins transmitting at the same time." HDMI-CEC Supplement at CEC-8.

Furthermore, U.S. Patent Publication No. 2007/0200859 ("Banks") teaches "a system video and audio source device that is coupled to a system video and audio sink through a serial link in a cable." Banks, ¶ 10. Banks further teaches that "a parallel HDMI bus transports control signals during control periods 402 and 406 and transports data signals during data periods 404 and 408." *Id.* ¶ 42. Banks further teaches that "specific control and data signals can be transported over any of the ports shown and during any appropriate interval." *Id.* ¶ 44.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 134

Furthermore, U.S. Patent No. 5,928,345 ("Tetzlaff") teaches a "a new data bus system and protocol for communication between master control nodes and peripheral devices." Tetzlaff, 1:6–7. Tetzlaff further discloses that "[d]ata bus 220 also includes a single CS line coupled to the CS output of master node microprocessor 200 and to the CS inputs of each of the slave nodes. The CS signal on the CS data bus line is generated by one of the master nodes and indicates that the data bus is active. It can be used as a delimiter between messages or to indicate which data bus is active if the master node is controlling multiple data buses." *Id.* at 4:49–55.

Furthermore, U.S. Patent Publication No. 2005/0021892 ("Kim") teaches "a system for transferring data between a mobile terminal and computer" and "[a] data transfer process between the terminal and computer." Kim, ¶¶ 5–6. Such data transfer, Kim discloses, "is accomplished when the terminal transmits a control signal to the computer through a control line of a USB cable based on a value stored in a terminal register unit." *Id.* at Abstract. Kim further discloses that "[a] computer register unit 31 includes a line control register 32 for receiving a control signal through the control line of the USB cable, and a status register 33 for indicating a data reception status from the terminal. The terminal register unit and computer register unit are connected to the control line of the USB cable." *Id.* ¶ 22.

Furthermore, WIPO Patent Publication No. 2007/074611 ("Takatsuji") teaches that "by transmitting control signals bidirectionally between TV, AV amplifier and DVD player, it is possible to operate the entire home theater with one remote control." Takatsuji, ¶ 2. Takatsuji further teaches "using a CEC bus which is a bidirectional connection, in order to control by bidirectional communication among the respective devices." *Id.* ¶ 22. Takatsuji further discloses that "[a] CEC message has a basic frame structure called 'block' and consists of one or more

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 135

blocks. Each 1-bit EOM and ACK field always exists every l block, and every block is used in the same manner." *Id.* ¶ 13.

Furthermore, U.S. Patent Publication No. 2006/0104396 ("Soriano") teaches that "[a] serial bus system for data communication between devices according to a master-slave protocol has a data bus connecting master and slave devices and a shared clock system arranged to provide a shared-clock signal to the master and slave devices." Soriano, Abstract. Soriano further teaches that "[t]he described embodiments of the bus system are arranged for data exchange between electronic devices, such as microprocessors, memory, I/O chips, controllers, sensors, etc. The data exchanged may be control data to control the devices connected to the bus; a bus of this kind is sometimes called a "control bus" (of course, a control bus may also exchange "content data")." *Id.* ¶ 26.

Furthermore, U.S. Patent No. 10,033,553 ("Ichimura") teaches that "[a] video signal and an audio signal are TMDS transmitted from a source device to a sink device. Through a reserved line and a HPD line provided separately from a TMDS transmission line, an Ethernet™ signal is bidirectionally transmitted, and also, a SPDIF signal is transmitted from the sink device to the source device." Ichimura, Abstract. Ichimura further teaches that "with respect to HDMI standards, a consumer electronics control (CEC) line 361, a reserved line 362, a hot plug detect (HPD) line 363, and the like, are provided. The CEC line 361 is a line for a bidirectional communication of device control signals. Whereas the display data channel 350 connects devices in a one-to-one manner, the CEC line directly connects all devices connected to HDMI." *Id.* at 5:51-57.

Furthermore, Raida Al-Alawi & A. J. Al-Sammak, *Design of a Multicode Bi-Phase Encoder for Data Transmission* ("Al-Alawi"), teaches that "[a]dvances in data transmission and

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 136

various digital communications network architectures have resulted in an increased demand to multimedia applications where data, voice, images and video signals are to be transmitted. These networks are becoming very large, and often their nodes have several different connections between them utilizing more than one protocol. Different protocols normally employ different line (modulation) codes, and hence, it is important to develop a controller in the physical layer that can cope with multiple protocols." Al-Alawi at 2.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Furthermore, to the extent that it is determined that any of the above references do not disclose a control bus that is "bi-directional" and "single-line," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 27 ("The CEC bus preferably consists of a single, bi-directional line. Each node is connected via the bi-directional CEC bus, thus allowing any CEC node to create a map of the network."); Van Willigen, 8:22–24 ("Line 13 is used for a Consumer Electronics Control (CEC) Channel which is optional to implement, but mandatory to wire. This is a one-wire bidirectional bus which is generally used for AV Link remote control signaling."); Candelore, ¶ 50 ("FIG. 3 references an exemplary HDMI System Block Diagram, said system transmitting CEC commands over a single cable."); Zhu, ¶ 59 ("USB cabling consists of D+ and D− data lines, 316 and 317 respectively, Vbus (power supply) line 318, GND 319 and USB ID detect line 320."); I2C

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 137

Specification at 6 (“Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus.”), 8 (“Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a current-source or pull-up resistor (see Fig.3).”); Suzuki, 7:44-48 (“An N-channel MOS transistor open drain terminal (TR) 113 receives and outputs the CEC signal S113 a which is connected to a communication party on the other end. The CEC signal S113 a is on a single signal line where a pull-up resistance is provided.”); Mujiga at 34 (“CEC is based on a bus system and all the transactions on the CEC bus consist of an initiator and one or more followers. The initiator sends the CEC frame (CEC message and data) and the followers respond to the CEC message.”); HDMI 1.3a Specification at 112 (“The CEC channel is optionally used for higher-level user functions such as automatic setup tasks or tasks typically associated with infrared remote control usage.”); Tetzlaff, 4:49–53 (“Data bus 220 also includes a single CS line coupled to the CS output of master node microprocessor 200 and to the CS inputs of each of the slave nodes. The CS signal on the CS data bus line is generated by one of the master nodes and indicates that the data bus is active.”); Kim, ¶ 19 (“The data transfer system includes a USB cable 20 having a control line, a terminal 10 provided with a data port (not shown) and a terminal register unit 11, and a computer 30 provided with a USB port (not shown) and a computer register unit 31.”); Takatsuji, ¶ 2 (“In addition, the HDMI standard specifies a protocol CEC (Consumer Electronics Control) for bidirectionally transmitting a control signal.”); Soriano, ¶ 5 (“The I2C-bus is a multi-master bus which means that the role of the master may be taken by different devices. The bus has two lines, a serial data line (SDA) and a serial clock line (SCL). The serial data line carries the data between the devices connected to the bus.”); Ichimura, 5:51-57 (“In addition, with respect to HDMI standards, a consumer electronics control (CEC) line 361, a reserved line 362, a hot plug detect (HPD) line 363, and the like, are provided. The CEC line 361

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 138

is a line for a bidirectional communication of device control signals. Whereas the display data channel 350 connects devices in a one-to-one manner, the CEC line directly connects all devices connected to HDMI."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a process for conducting "arbitration" of the control bus, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 38 ("If there is any other device sending the same simultaneously, the arbitration process is conducted (block 125). The arbitration process determines which device has higher priority to have control of the command bus."); Fuller, 3:35–40 ("At the beginning of a bus 100 transaction cycle, a bus 100 interface circuit 110 of each device 104-105 checks whether its device is the bus master, at steps 300 and 350. (A device becomes bus master by winning bus access contention, for example. Alternatively, the state of the system (active, standby) determines who is bus master.)"); I2C Specification at 7 ("The possibility of connecting more than one microcontroller to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed."); Mujiga at 34 ("The CEC bus arbitration ensures collisions are spotted and reliable messaging can be achieved. It does this in a completely static priority-based manner based on the device's logical address."); HDMI-CEC Supplement at CEC-15 ("Arbitration for the CEC line ensures collisions are spotted and a reliable message layer can be achieved."); Tetzlaff, 5:35–37 ("The above described arbitration method also aids in facilitating bi-directional communications."); Soriano, ¶ 30 ("In such protocols, typically an arbitration procedure is defined

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 139

which governs access to the bus in the case of bus-access conflicts."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a "transmitting device" that is a "mobile device," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Zhu, ¶ 14 ("USB On-the-Go (OTG) is a new USB communication protocol specified in the USB 2.0 specification. USB OTG allows peer-to-peer communications between two USB OTG devices enabling, for example, a digital camera to directly communicate with a printer without the need of a PC as a host."); I2C Specification at 4 ("In consumer electronics, telecommunications and industrial electronics, there are often many similarities between seemingly unrelated designs. For example, nearly every system includes . . . [a]pplication-oriented circuits such as digital tuning and signal processing circuits for radio and video systems, or DTMF generators for telephones with tone dialling."); HDMI 1.3a Specification at 10 ("A device's external HDMI connection shall be presented via one of the three specified HDMI connectors, Type A, Type B or Type C. . . . The Type C connector carries the same signals as the Type A but is more compact and intended for mobile applications."); Tetzlaff, 1:34–38 ("Frequently, the master node in a process control instrument is a Motorola or compatible microprocessor or microcontroller. For example, the Motorola 68HC05 and 68HC11 microcontrollers are commonly used as the master node in process control instruments."); Kim, Fig. 2. Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a "modified protocol," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 27 ("The

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 140

optional CEC protocol provides high-level control functions between all of the CEC compliant nodes in the CEC network."); Van Willigen, 8:30–32 ("In a preferred embodiment of the invention, lines 13 and 14 of a Type A connector are not used in the way specified by the HDMI standard (at least as defined by HDMI 1.0-1.3) but are used as a bi-directional channel for carrying compressed AV content."); Candelore, ¶ 56 ("Interface 1 may be considered the normal HDMI CEC signal path that is unacceptably slow while Interface 2 is the enhanced, faster data transmission path. As will be described, Interface 2 may rely upon a faster signal path through the HDMI connector, as illustrated in FIG. 6 or it may be based upon another protocol entirely such as USB, as shown in FIG. 7. Moreover, Interface 2 may be used instead of, or in addition to, the original HDMI CEC Interface 1. "); Zhu, ¶ 14 ("USB On-the-Go (OTG) is a new USB communication protocol specified in the USB 2.0 specification. USB OTG allows peer-to-peer communications between two USB OTG devices enabling, for example, a digital camera to directly communicate with a printer without the need of a PC as a host."); Fuller, 1:45–52 ("The second device presents a first interface (e.g., uses a first protocol) over the connection, while the third device presents a second interface (e.g., uses a second protocol) different from the first interface over the connection. The second interface provides capabilities different from (e.g., additional to, or that cannot be provided by) those provided by the first interface."); Kim, ¶ 19 ("The data transfer system includes a USB cable 20 having a control line, a terminal 10 provided with a data port (not shown) and a terminal register unit 11, and a computer 30 provided with a USB port (not shown) and a computer register unit 31."); Ichimura, 6:35-38 ("As described above, the reserved line 362 is, a line not utilized in HDMI standards. However, in the present case, the reserved line 362 is being used to detect the type of a device that is connected for the sake of efficient use of a pin."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 141

Furthermore, to the extent that it is determined that any of the above references do not disclose a data packet followed by an "acknowledge (ACK) message," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 38 ("At block 128, each byte of the command received from the host control unit is converted to a 10-bit command block by adding an "end of message" (EOM) bit, and an acknowledgement (ACK) bit."), ¶ 39 ("The follower receives each bit, combines bits into bytes and sends an acknowledgement for each byte."); I2C Specification at 10 ("If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. . . . Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address (see Section 10.1.3)."); HDMI-CEC Supplement at CEC-12 ("The ACK bit is used by follower(s) to acknowledge the data or header block. It is always set to 1 by the initiator."); Takatsuji, ¶¶ 18–19. Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose "bi-phase mark encoding," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Yung, ¶ 38 ("The 10-bit command block is converted to command signaling by converting 0s into logical 0s, and 1s into logical 1s (block 128). The implementation of logical 0s and logical 1s can be defined by the designers, providing the implementation is recognizable by both initiators and followers. The preferred implementation is provided in the CEC protocol, which use the durations of high and low Voltages to distinguish logical 0s and logical 1s."); Soriano, ¶ 28 ("The binary data may

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 142

be coded by the electrical signals in various ways, e.g. by the NRZ Code, the RZ Code, the AMI Code, the Manchester Code, the differential Manchester Code, etc."); Ichimura, 2:10-15 ("Furthermore, according to the first aspect, the second signal may be a signal including a clock component. Thereby, an effect that the clock component is transmitted to the external device is achieved. Here, as an example, the second signal may include a biphase-mark modulated signal."); Al-Alawi at 3 ("Several line coding techniques suitable for data transmission have been devised. Among these codes are Bi-Phase-Level (Bi-Φ-L), Bi-Phase-Mark (Bi-Φ-M), Bi-Phase-Space (Bi-Φ-S), Differential Manchester (DM) and Inverse Differential Manchester (IDM) codes. These widely used codes belong to the Bi-Phase code family which is characterized by having at least one transition per bit time."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a "switchable pull-up circuit" on the control bus, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Zhu, ¶ 74 ("B-device 327 detects in block 310 that bus is idle for more than 3 mS and begins (HNP) by turning off pull-up on D+. This pull-up is contained within block 312. This allows the bus to discharge to the session end zero SEO state."); I2C Specification at 22 ("After each acknowledge bit (A) or not-acknowledge bit (A) the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the LOW period of the SCLH signal. The active master re-enables its current-source pull-up circuit again when all devices have released and the SCLH signal reaches a HIGH level, and so speeds up the last part of the SCLH signal's rise time."); HDMI-CEC Supplement at 7 ("For example, this can be implemented by connecting an isolating diode between the CEC input pin and the internal pull-up

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 143

circuit, such that diode is reverse-biased in the off state with an external device pulling-up the CEC line."); Ichimura, 9:64-10:1 ("Similarly, when the source device 100 is of a specific type, pull-up is performed by the resistor 111 and the potential of the reserved line 362 becomes 2.5V, and when the source device 100 is not of a specific type, the potential becomes 0V."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose allowing "the transmitting device to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Fuller, 3:35–40 ("At the beginning of a bus 100 transaction cycle, a bus 100 interface circuit 110 of each device 104-105 checks whether its device is the bus master, at steps 300 and 350. (A device becomes bus master by winning bus access contention, for example. Alternatively, the state of the system (active, standby) determines who is bus master.)"); HDMI-CEC Supplement at CEC-15 ("It should be noted that this process gives priority to the logical address with the most leading zeros and, ultimately, the TV.") Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 144

use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to transmission of information from a transmitting device to a receiving device over a control bus.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards signal processing in microphone array systems, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

For example, a person skilled in the art would have been motivated to combine Stanek with Yung, Zhu, Candelore, Kim, and/or additional references discussed above and disclosed in Exhibits F-1 through F-9 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed communication between computing devices over a control bus. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, a simple addition of Yung's arbitration process and bi-phase mark encoding to the system disclosed in Stanek would yield a predictable result. As another example, a person of ordinary skill in the art would have been motivated to implement Zhu's switchable pull up circuit on a control bus of the HDMI

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 145

connection in Stanek. Indeed, Candelore discloses that the CEC control bus of the HDMI standard can be modified to enhance the speed of any communications. Additionally, a skilled artisan could easily incorporate Kim's teachings that communication can occur over a control bus to make Stanek compatible with mobile devices.

Furthermore, a person skilled in the art would have been motivated to combine Stanek, Yung, Van Willigen, Candelore, and/or Suzuki with Mujiga, the HDMI 1.3a Specification, the HDMI-CEC Supplement, Takatsuji, and/or additional references discussed above and disclosed in Exhibits F-1 through F-9 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed communication between computing devices over a control bus. The Stanek, Yung, Van Willigen, and Candelore references all disclose communication using the HDMI standard and, specifically, the CEC line of that standard. A person of ordinary skill in the art would have easily combined those references with the teachings of Mujiga, the HDMI 1.3a Specification, the HDMI-CEC Supplement, Takatsuji, and other references to implement the HDMI standard and the CEC bus. For example, to the extent such features are not inherent in the references, a skilled artisan would be aware of and could easily incorporate the HDMI-CEC Supplement's arbitration process and/or switchable pull up circuit into the system disclosed in any reference incorporating the HDMI standard, due to those references' express reliance on the HDMI standard.

Furthermore, a person skilled in the art would have been motivated to combine Stanek, Yung, Van Willigen, Candelore, and/or Suzuki with Soriano, Ichimura, Al-Alawi and/or additional references discussed above and disclosed in Exhibits F-1 through F-9 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed to communication between computing devices over a control bus. The concept of bi-

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 146

phase mark coding (also known as ”Manchester” coding) was well-known in the art as of the time of the ’520 patent, as demonstrated by the Soriano, Ichimura, and Al-Alawi references. Because the above references all relate to communication between devices over a control bus, a skilled artisan would have been capable of simply substituting bi-phase mark coding for the coding approaches used in Stanek, Yung, Van Willigen, Candelore, and/or Suzuki.

Furthermore, a person skilled in the art would have been motivated to combine Yung with Van Willigen and/or additional references discussed above and disclosed in Exhibits F-1 through F-9 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed communication between computing devices over a control bus. For example, a person of ordinary skill in the art would have been capable of making the simple substitution of Van Willigen’s modified HDMI protocol for the standard HDMI protocol disclosed in Yung.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the ’520 Patent:

- Stanek in view of Yung
- Stanek in view of Mujiga
- Stanek in view of the HDMI 1.3a Specification and the HDMI-CEC Supplement
- Stanek in view of the HDMI-CEC Supplement and Zhu
- Stanek in view of the HDMI-CEC Supplement and Candelore
- Stanek in view of the HDMI-CEC Supplement and Kim
- Stanek in view of the HDMI-CEC Supplement and Soriano
- Stanek in view of the HDMI-CEC Supplement and Al-Alawi
- Stanek in view of the HDMI-CEC Supplement and Ichimura

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 147

- Yung in view of Van Willigen
- Yung in view of the HDMI 1.3a Specification and the HDMI-CEC Supplement
- Yung in view of the HDMI-CEC Supplement and Kim
- Yung in view of the HDMI-CEC Supplement and Soriano
- Yung in view of the HDMI-CEC Supplement and Al-Alawi
- Yung in view of the HDMI-CEC Supplement and Ichimura

B. Invalidity of the '520 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '520 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, Defendant asserts that the Asserted Claims of the '520 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- "plurality of different control buses" (claim 8)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

The written description and enablement issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 148

C. Invalidity of the '520 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant's present understanding of Plaintiff's asserted scope of the claims of the '520 Patent, to the extent such positions can be understood from Plaintiff's Infringement Contentions, the Asserted Claims of the '520 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- "the transmitting device is operable for coupling with a receiving device via the first control bus" (claim 12)
- "the receiving device is a device utilizing the standard protocol" (claim 12)
- "the transmitting device is a mobile device utilizing a modified protocol" (claim 12)
- "the receiving device is operable for coupling with a transmitting device via the first control bus" (claim 19)
- "the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol" (claim 19)
- "the generated data packets" (claim 1)
- "the initiating device" (claim 9)
- "the following device" (claim 9)
- "the modified protocol being a modification of the standard protocol that is not included in the standard protocol" (claims 12 and 19)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

At least claims 12 and 19 (and their dependent claims) of the '520 Patent are invalid under 35 U.S.C. § 112(2) because they are mixed method-apparatus claims under the doctrine of *IPXL Holdings L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). In particular, at least the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 149

following claim terms and phrases improperly recite a method of using the entire claimed apparatus and/or functionality not tied to the capability of any recited structural element:

- "the transmitting device is operable for coupling with a receiving device via the first control bus" (claim 12)
- "the receiving device is a device utilizing the standard protocol and the transmitting device is a mobile device utilizing a modified protocol" (claim 19)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, at least Claims 12 and 19 (and their dependent claims) of the '520 Patent are invalid under 35 U.S.C. §§ 112(2) and (6) because the '520 Patent does not disclose sufficient structure corresponding to the function recited in at least the following means-plus-function claim limitations:

- "logic to convert each of one or more control signals into a data packet each of the one or more control signals being one of a plurality of different types of control signals for a standard protocol, each data packet including a plurality of bits to be transmitted" (claim 12)
- "logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to: determine whether the control bus is in use by the receiving device, and if the first control bus is not in use by the receiving device, conduct arbitration for control of the first control bus" (claim 12)
- "the logic to arbitrate use of the first control bus is further operable to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time" (claim 18)
- "logic to convert each of the one or more data packets into a control signal" (claim 19)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 150

- "logic to arbitrate use of the first control bus, the logic to arbitrate use being operable to: determine whether the control bus is in use by the transmitting device, and if the first control bus is not in use by the transmitting device, conduct arbitration for control of the first control bus" (claim 19)

- "the logic to arbitrate use of the first control bus is further operable to allow the transmitting device to take control of the first control bus if the transmitting device and the receiving device arbitrate use of the first control bus at the same time" (claim 25)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

IX. THE ASSERTED CLAIMS OF THE '231 PATENT ARE INVALID

A. Identification of Prior Art

Defendant contends that the prior art references charted in Exhibits G-1 through G-10, discussed in any incorporated IPR petitions and institution decisions, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '231 Patent.

1. The '231 Patent Claims Are Anticipated by the Prior Art

Some or all of the Asserted Claims of the '231 Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit G-1 through G-10 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 151

In addition to references identified in any incorporated IPR petitions and institution decisions, Defendant identifies the following references as anticipating one or more of the Asserted Claims of the '231 Patent under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '231 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim, anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date/Filing Date	Short Name	Exhibit Number
U.S. Patent Pub. No. 2006/0280055	Filed: June 8, 2006 Pub'd: Dec. 14, 2006	Miller '055	G-1
U.S. Patent Pub. No. 2007/0036158	Filed: Aug. 11, 2006 Pub'd: Feb. 15, 2007	Hun-Kwon	G-2
U.S. Patent No. 8,203,325	Filed: Sep. 7, 2007 Issued: June 19, 2012	Miller '325	G-3
U.S. Patent Pub. No. 2004/0010730	Filed: Mar. 6, 2003 Pub'd: Jan. 15, 2004	Saito	G-4
Japanese Patent Pub. No. 2006/248149	Filed: Mar. 15, 2005 Pub'd: Sep. 21, 2006	Ozawa	G-5
U.S. Patent Pub. No. 2003/0132941	Filed: Jan. 14, 2003 Pub'd: July 17, 2003	Echizenya	G-6
U.S. Patent Pub. No. 2006/0076977	Filed: Sep. 20, 2004 Pub'd: Apr. 13, 2006	Zhu	G-8
U.S. Patent Pub. No. 2005/0114580 U.S. Patent Pub. No. 2007/0028127	Filed: Nov. 26, 2003 Pub'd: May 26, 2005 Filed: July 6, 2006 Pub'd: Feb. 1, 2007	Ede Kim	G-10

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 152

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Video Electronics Standards Association	DisplayPort Standard, Version 1[4]	May 1, 2006	DisplayPort 1.0	G-7
USB Implementers Forum, Inc.	On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a	June 24, 2003	USB OTG Supplement	G-9
Adhir Upadhyay et al. Rick Downs	A Novel Asynchronous Wrapper Using 1-of-4 Data Encoding and Single-Track Handshaking Using 1-Wire I/O for Distributed System Monitoring	June 23, 2004 Sep. 17, 1998	Upadhyay Downs	G-10

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the '231 Patent. Defendant's further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- DisplayPort 1.0 or earlier
- USB 2.0 or earlier and/or USB On-The-Go Revision 1.0a

[4] Although the DisplayPort standards discussed herein include a tag purporting to limit their distribution to "Members Only," the versions discussed herein and/or charted in the attached exhibits are available publicly via the Internet. See, e.g., https://glenwing.github.io/docs/DP-1.0.pdf and https://glenwing.github.io/docs/DP-1.2.pdf

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 153

- HDMI Version 1.3a or earlier
- Dallas One-Wire Bus

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the ’231 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

2. The ’231 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the asserted claims of the ’231 Patent are not explicitly disclosed by an item of prior art identified above, in Exhibits G-1 through G-10, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 154

Furthermore, it would have been obvious to combine any of the prior art in Exhibits G-1 through G-10 with each other, at least because all of these references relate to serial communication between a transmitting device and a receiving device using both a power bus and a control bus, and discovery of devices using those buses.

Furthermore, U.S. Patent Publication No. 2006/0280055 ("Miller '055") teaches "a communication link 100 between a standard source (graphic/video source) 101 and a sink (display/receiver) 102. Communication between the graphic/video source 101 and the display/receiver 102 enables bi-directional transfer of signals that send graphic data from a source to a receiver and additional signals that send and receive control information between the source and receiver." Miller '055, ¶ 5. That communication occurs using the HDMI standard, which uses "control signals [that] include signals related to the Data Display Channel (DDC), the Consumer Electronics Channel (CEC), and Hot Plug Detect (HPD)." *Id.* ¶ 6. As Miller explains, "the signals that are transmitted between a source and a sink will include, three differential channels (six wires), a clock channel (two wires), SDA, SCL, CEC, DDC/CEC ground, +5V and HPD." *Id.* ¶ 32.

Furthermore, U.S. Patent Publication No. 2007/0036158 ("Hun-Kwon") teaches that "a media source device (e.g., a STB) for reproducing predetermined media data and processing the reproduced media data is connected to a Media sink device (e.g., a DTV) for receiving media data from the media source device and outputting the received media data to an external part via a predetermined interface cable. In this case, the media source device may be connected to the Media sink device via an interface cable (e.g., a DVI or a HDMI)." Hun-Kwon, ¶ 5. Hun-Kwon further teaches that "the first port 406 a includes a first power pin 407 a for receiving the voltage of +5V from the first media source device 410, and a first HPD pin 408 a for generating the HPD signal." *Id.* ¶ 62.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 155

Furthermore, U.S. Patent No. 8,203,325 ("Miller '325") teaches that "[a]ctivation systems and methods initiate High-Definition Multimedia Interface (HDMI) communication between an HDMI source and an HDMI sink through an HDMI receptacle of the source. These systems and methods are especially suited for use with mobile sources that generally operate from a battery that cannot provide the +5V signal which the HDMI protocol requires sources to place on the +5V pin of their HDMI receptacles. These systems and methods automatically detect the insertion of an HDMI cable into the source's HDMI receptacle and subsequently generate and apply the required +5V signal to the +5V pin of the source's HDMI receptacle to initiate HDMI communication." Miller '325, Abstract. Miller '325 further teaches that "[e]ach of the three data channels (channels 0, 1 and 2) and the associated TMDS clock is formed by a signal pin (denoted as +), an inverse signal pin (denoted as −), and a ground pin. These pins are located at the center and the right side of the plug 25. CEC, DDC data and clock, HPD, +5V, and DDC/CEC ground are each carried on respective pins that are located at the left side of the plug 25." *Id.* at 4:4–11.

Furthermore, U.S. Patent Publication No. 2004/0010730 ("Saito") teaches that "a host is connected with a peripheral by a USB cable to which a Mini-A plug and a Mini-B plug are provided on opposite ends." Saito, ¶ 108. Saito further teaches that "In the USB standard, a host can be connected with a peripheral only by using VBUS (power supply), GND (ground), and two data signal lines (D+ and D−). VBUS is supplied from the host. The data signal lines D+ and D− are used as differential signal lines. In the OTG standard, a dual-role device to which a Mini-A plug is connected becomes an A-device, as shown in FIG. 1B. The A-device operates as the host at the start of a session and is capable of transferring the host function to a B-device under given conditions. A dual-role device to which a Mini-B plug is connected becomes a B-device. The B-

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 156

device operates as the peripheral at the start of a session and is allowed to operate as the host by the A-device. The A-device supplies VBUS." *Id.* ¶¶ 109–10.

Furthermore, Japanese Patent Publication No. 2006/248149 ("Ozawa") teaches that an "interface 200 communicates with an external device based on a communication method such as USB or IEEE (the Institute of Electrical Engineers) 1394, sends data acquired from the external device to the CPU 203, and transmits data acquired from the CPU 203 to the external device." Ozawa, ¶ 21. Ozawa further teaches that an "interrupt generation circuit 201 detects a change in the interface 200 from a state in which no external device is connected to the interface 200 to a state in which the external device is connected, and notifies the CPU 203 of the change. The interrupt generation circuit 201 is, for example, an edge-triggered flip-flop, and detects that an external device is connected to the interface 200 by detecting a change in the voltage of a predetermined signal line of the interface 200. In the present embodiment, when a predetermined signal line changes from a low voltage to a high voltage, the interrupt generation circuit 201 detects that an external device is connected to the interface 200 and notifies the CPU 203 accordingly." *Id.* ¶ 24.

Furthermore, U.S. Patent Publication No. 2003/0132941 ("Echizenya") teaches "a controller adapted to ascertain, when the host device and the monitoring device are connected with each other through optical extension cables each based on DVI standard, whether these host device and monitoring device have been exactly connected with each other through the optical extension cables or not as well as to ascertain whether a power from an external power source or supply has been supplied to attached circuits of the host device and the monitoring device or not." Echizenya, ¶ 2. More specifically, Echizenya teaches that "a video signal is digitally transmitted at high speed through the optical extension cables by use of T.M.D.S. transmission system, and (DDC+5V)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 157

signal, DDC clock, DDC data and HPD signal all of which are low speed signals for carrying out the plug and play of a display are transmitted through the metal extension cables." *Id.* ¶ 41.

Furthermore, Video Electronics Standards Association, *DisplayPort Standard, Version 1* ("DisplayPort 1.0") teaches a link consisting of "consists of Main Link, Auxiliary Channel (AUX CH), and Hot Plug Detect (HPD) signal line." DisplayPort 1.0 at 24. DisplayPort 1.0 further teaches that "DisplayPort connectors for detachable, box-to-box connections have one power pin and one return current pin. The power shall be provided by Source Device only. The voltage of the power pin shall be in the range of 5- to 12-V." *Id.* at 115. DisplayPort 1.0 further discloses that "The HPD signal is asserted by the DisplayPort Sink whenever the Sink is connected to its main power supply. . . . The voltage level of the HPD pin is monitored by Source Device. TTL level shall be used for the detection." *Id.* at 116.

Furthermore, U.S. Patent Publication No. 2006/0076977 ("Zhu") teaches "enabl[ing] a USB 1.1 device and a USB 1.1 host to communicate seamlessly with a USB OTG device. The invention complies with both USB 1.1 and OTG specifications. The invention includes the USB 1.1 host, USB 1.1 device and mixed signal circuits to implement USB OTG functions." Zhu, Abstract. Zhu further discloses that a "USB A-Device supplies power to the Vbus power line. It is host at the start of a transaction session. It will relinquish the role of host to a dual-role B-Device to which it is connected by a USB cable. This can occur only under the rules determined by the host negotiation protocol (HNP)." *Id.* ¶ 17.

Furthermore, USB Implementers Forum, *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a* ("USB OTG Supplement") teaches that "USB has become a popular interface for exchanging data between PC's and peripherals. An increasing number of portable peripherals are using the USB interface to communicate with the PC. Many of these portable

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 158

devices would benefit from being able to communicate to each other over the USB interface, yet certain aspects of USB make this difficult to achieve." USB OTG Supplement at 1. The USB OTG Supplement further teaches that "this supplement to the USB 2.0 specification was developed that allows a portable device to take on the role of a limited USB host, without the burden of supporting all the above functions of a PC." *Id.*

Furthermore, U.S. Patent Publication No. 2005/0114580 ("Ede") teaches that "[t]he USB On-The-Go (OTG) supplement to USB allows a device to be dual mode. A dual mode device has a mini A/B connector that allows it to be connected to a mini A-plug as an A-device or to be connected to a mini B-plug as a B-device. As a default a dual mode device when connected as an A-device operates as a default host and when connected as a B-device operates as a default peripheral. However, OTG will enable the role of the dual-role device to change without reversing the cable. Thus the OTG device will be able to operate as a host or peripheral whether to is connected as an A-device or a B-device." Ede, ¶ 5. Ede further discloses that "[t]he A/B interface 12 of the dual-mode device 2 comprises a USB transceiver 14 and five pin contacts. The first pin contact 40 (Vbus) is used to provide power from the A-device to the B-device. The second pin contact 42 (D+) and the third pin contact 44 (D−) are used as differential data lines for transmitting data between connected devices. The fourth pin contact 46 (GND) is used as an earth or ground. The fifth pin contact 48 (ID) is used to detect, in the dual mode device 2, whether it is connected to a mini A-plug or a mini B-plug. A mini A-plug connects, when inserted, the fourth pin contact 46 (ID) to the fifth pin contact (GND) via a resistor. A mini B-plug, when inserted, leaves the fourth pin contact 46 (ID) isolated." *Id.* ¶ 24.

Furthermore, Adhir Upadhyay et al., *A Novel Asynchronous Wrapper Using 1-of-4 Data Encoding and Single-Track Handshaking* ("Upadhyay"), teaches that "[t]he ST handshaking

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 159

shown in Fig.3 needs just one wire to signal both REQ and ACK. The sender pulls the ST line high to indicate a REQ. The receiver pulls the ST line low to signal an ACK. Since after an REQ transmission, the ACK signal returns the wire to its initial electrical state, the ST signaling essentially combines the common 2-phase and 4-phase protocols-to become a 2-phase, return-to-zero handshaking scheme." Upadhyay at 206.

Furthermore, Rick Downs, *Using 1-Wire I/O for Distributed System Monitoring* ("Downs"), teaches that "[o]ne popular serial bus used by integrated circuit manufacturers is the I2C bus from Philips, and its compatible 2-wire bus variants from several other manufacturers. This bus scheme uses a clock and a bidirectional data line, and defines 4-bit addresses for typical circuit functions." Downs at 161. Downs further discloses that "The Dallas One-Wire™ (DOW) [2] bus uses only a single wire to communicate data. Originally defined as a way to communicate with memory devices using a minimal contact count, the DOW has been extended to several different product families. Products available that use the DOW include EPROM memories, digital temperature sensors, and specialized battery management devices. The use of a single data line makes routing the bus on a board much simpler, or for extended systems, makes wiring simpler and less costly." *Id.* at 162.

Furthermore, U.S. Patent Publication No. 2007/0028127 ("Kim") teaches "a USB system comprises a host device, and at least one client device connected to the host device through a USB connection, in which the host interrupts a power supply to the client device through a power line when there is a deadlock condition and resumes the power supply to the client device after an initialization." Kim, ¶ 11. More specifically, Kim teaches that "[t]he host device comprises a first switch connected to the power line for regulating the power supply to the client device. The client device comprises a pull-up resistor connected to a data line of the USB connection, the pull-up

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 160

resistor being connected with a second switch. The second switch disconnects the data line from the pull-up resistor when the power supply through the power line is interrupted, and connects the data line with the pull-up resistor when the power supply resumes." *Id.* ¶¶ 12–14.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Furthermore, to the extent that it is determined that any of the above references do not disclose a "second state" for a "second type of transmitting device," it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Hun-Kwon, ¶ 87 ("In more detail, if the user selects the second media source device, the Media sink device recognizes the power received via the second power pin, and determines whether the recognized power is the voltage of +5V at step S612."); Miller '325, 5:9–14 (""Because the cell phone 40 operates on a battery voltage in the range of 2.5 to 4.5 volts, it cannot provide a voltage on the +5V line of the HDMI plug 28 that will be recognized by a sink. The activation system 50 of FIG. 5, however, modifies the cell phone so that it can successfully complete HDMI communications with an HDMI sink."); Echizenya, ¶ 50 ("In the monitoring device M, it is determined in a decision step 23 whether the transmitted (DDC+5V) signal is the proper (DDC+5V) signal or not. In case it is the proper (DDC+5V) signal, the decision step 23 generates "Yes" signal, and the process proceeds to a step 22 shown in FIG. 3. In the step 22, the HPD signal source 44 provided in the monitoring device M is driven to generate a HPD signal (a

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 161

return signal of the (DDC+5V) signal) therefrom, and the process proceeds to the next decision step 73. The decision step 73 decides whether the generated HPD signal is the proper HPD signal or not. When the decision step 73 decides that it is the proper HPD signal, "Yes" signal is outputted from the decision step 73, and the process proceeds to a step 74."); Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a transmitter that drives "a first signal value on the control bus periodically upon transitioning to the pending state," and a "second logic" for doing so, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, USB OTG Supplement at 51 ("The A-device detects the SE0 on the bus and recognizes this as a request from the B-device to become Host. The A-device responds by turning on its D+ pull-up within TA_BDIS_ACON max of first detecting the SE0 on the bus. . . . After waiting long enough to insure that the D+ line cannot be high due to the residual effect of the B-device pull-up, (see Section 5.1.9), the B-device sees that the D+ line is high and D- low, (i.e. J state). This indicates that the A-device has recognized the HNP request from the B-device. At this point, the B-device becomes Host and asserts bus reset to start using the bus."); Downs at 162 (""Data transfer is initiated by the bus master, which first resets the bus by pulling it low for at least 480ps. Within 60ps after the master releases the line, any slave devices present on the bus will respond to the reset by pulling the bus low for at least 60ps - this is known as a presence pulse. Once the master knows there is someone out there to talk to, data can be communicated between the master and a slave in timeslots which are 120ps long (Figure 1)."); Kim ¶ 78 ("In the USB system of FIG. 4, the data lines D+ and D− are also variable in accordance with the deadlock detection. If the switch SW2 of the bus-powered high-speed USB device 220 is turned off, the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 162

positive data line D+ transitions to the low level from the high level. When both the data lines D+ and D− have low levels for the predetermined time T1, the USB host 110 detects a state of disconnection with the bus-powered high-speed USB client 220. The USB host 110 turns the switch SW1 off and initializes its internal condition for the predetermined time T2."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose "a switchable pull up circuit on the control bus" and "the transmitting device to enable the pull up circuit in the discovered state" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Saito, ¶ 114 ("The dual- role device 10 includes a pull-up resistor R1 for pulling up the data signal line D+ and a pull-down resistor R2 for pulling down the data signal line D+ in order to operate as either the host or the peripheral. The pull-up resistor R1 is connected with a power supply voltage line through a switch circuit SW1 for turning the pull-up on/off. The pull-down resistor R2 is connected with a ground line through a switch circuit SW2 for turning the pull-down on/off. The switch circuits SW1 and SW2 are controlled exclusively so that one of the switch circuits SW1 and SW2 is turned off when the other is turned on."); USB OTG Supplement at 50 ("When the B-device has finished using the bus, it starts the process of returning control to the A-device simply by stopping all bus activity and turning on its D+ pull-up resistor when the bus is in FS idle. The A-device will detect this lack of activity and turn off its pull-up resistor. When the A-device detects the connection from the B-device, it will resume bus operation as Host."); Ede, ¶ 28 ("The B-interface 22 monitors Vbus and when the voltage on the line exceeds a predetermined threshold, a pull-up resistor 24 is connected to one of the data lines D+, D−. This is not described in detail as this is how a current peripheral USB device responds to a host initiating a session by switching

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 163

and keeping Vbus on. If the B-interface 22 is a high speed interface then the pull-up resistor is connected to the data line D+ using a switch. If the B-interface 22 is a low speed interface then the pull-up resistor is connected to the data line D− using a switch."); Kim, ¶¶ 13–14 ("The client device comprises a pull-up resistor connected to a data line of the USB connection, the pull-up resistor being connected with a second switch. The second switch disconnects the data line from the pull-up resistor when the power supply through the power line is interrupted, and connects the data line with the pull-up resistor when the power supply resumes."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose "wherein the transmitting device is a mobile device" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Miller '325, Figs. 5A–5C, 5:9–14 (""Because the cell phone 40 operates on a battery voltage in the range of 2.5 to 4.5 volts, it cannot provide a voltage on the +5V line of the HDMI plug 28 that will be recognized by a sink. The activation system 50 of FIG. 5, however, modifies the cell phone so that it can successfully complete HDMI communications with an HDMI sink."); Saito, ¶¶ 305–06, Fig. 1A; Ozawa, ¶¶ 7, 10, 16; USB OTG Supplement at 5, 14–16; Ede, ¶¶ 20–22; Downs at 165; Kim ¶¶ 5, 85. Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose a "switchable pull down circuit" on the control bus, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Saito, ¶ 115 ("The dual- role device 20 includes a pull-up resistor R3 for pulling up the data signal line D+ and a pull-down resistor R4 for pulling down the data signal line D+. The pull-

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 164

up resistor R3 is connected with a power supply voltage line through a switch circuit SW3 for turning the pull-up on/off. The pull-down resistor R4 is connected with a ground line through a switch circuit SW4 for turning the pull-down on/off. The switch circuits SW3 and SW4 are controlled exclusively so that one of the switch circuits SW3 and SW4 is turned off when the other is turned on."); USB OTG Supplement at 34 ("When an A-device is idle or acting as Host, it shall activate pull-down resistors on both the D+ and D- lines. These resistors shall be within the range of 14.25 kΩ to 24.8 kΩ (RPD). When an A-device is acting as a Peripheral, it shall disable the pull-down on the D+ line but shall not disable the pull-down on the D- line. The A-device is allowed to disable both pull-down resistors during the interval of a packet transmission, when acting as either Host or Peripheral."); Kim, ¶ 47 ("The downstream port transceiver 101 is connected with a pair of data lines D+ and D−, a power line Vbus, and a ground line GND. The data lines D+ and D− of the downstream port transceiver 101 are each connected to pull-down resistors R1 and R2. The pull-down resistors R1 and R2 have values of about 15 KΩ."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

Furthermore, to the extent that it is determined that any of the above references do not disclose "the first type of device is compatible with a modified protocol" (and related limitations) as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the following teachings: *See, e.g.*, Kim, ¶ 82 ("The USB OTG system shown in FIG. 13 is set by altering the functions of the host and device from the USB OTG system of FIG. 12 by means of HNP. When the functions of the USB host and client are changed by HNP while the USB OTG system is operating, a deadlock condition occurs to cut off connection between the two USB devices and the allocation of functions is re-established as the initial

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 165

configuration when the systems are reconnected."). Therefore, a person of ordinary skill in the art would be motivated to make such a combination.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to serial communications between a transmitting device and a receiving device that communicate via a power bus and a control bus.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards signal processing in microphone array systems, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 166

For example, a person skilled in the art would have been motivated to combine Zhu and/or the USB OTG Supplement with Kim, Saito, Ede and/or additional references discussed above and disclosed in Exhibits G-1 through G-10 for the reasons provided above. Moreover, the combination of references is no more than a combination of systems all directed to communication between devices using the USB 2.0 and USB On-The-Go standards. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, the addition of the deadlock detection logic disclosed in Kim would be a straightforward modification to the systems disclosed in Zhu and the USB OTG Supplement. Additionally, Kim discloses that it is possible to modify the functions of host and client devices that communicate using the USB OTG standard, and that such modifications are within the level of ordinary skill in the art. Further, combining features of Zhu and the USB OTG Supplement with the teachings of these references employs the use of known techniques to improve similar devices in the same way. For example, Zhu with Kim would use Kim's deadlock detection logic to enable seamless communication between USB devices, which is the problem disclosed in Zhu.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the Asserted Claims of the '231 Patent:

-
- Zhu in view of Kim
- Zhu in view Saito
- Zhu in view of Ede
- USB OTG Supplement in view of Kim
- USB OTG Supplement in view of Saito
- USB OTG Supplement in view of Ede

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 167

B. Invalidity of the ’231 Patent Based on 35 U.S.C. § 112, ¶ 1 (Enablement and Written Description)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’231 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that the Asserted Claims of the ’231 Patent are invalid for failure to provide a written description that enables the full scope of the Asserted Claims based on at least the following claim terms, phrases, or limitations:

- “disabling hot plug functionality” (claims 1 and 16)

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

The written description and enablement issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

C. Invalidity of the ’231 Patent Based on 35 U.S.C. § 112, ¶ 2 (Indefiniteness)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’231 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that the Asserted Claims of the ’231 Patent are invalid for reciting at least the following claim terms, phrases, or limitations:

- “the transmitter to transition from a disconnect state to a pending state when a predetermined voltage is detected on the power bus by the first logic” (claim 10)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 168

- "the transmitter to drive a first signal value on the control bus periodically upon transitioning to the pending state" (claim 10)
- "the transmitting device is to transition to the disconnect state when the first logic determines that the voltage value on the power bus is lost" (claim 11)
- "the transmitting device is to enable the pull up circuit in the discovered state" (claim 13)
- "the receiving device to enable a voltage potential of a predetermined value on the power bus and to drive a signal on the control bus at a first signal value in a disconnect state" (claim 16)
- "the receiving device to discover a first type of transmitting device and transition to a first state when the first signal is detected" (claim 16)
- "the receiving device to enable the switchable pull down circuit on the control bus and disable hot plug functionality upon discovering the first type of transmitting device" (claim 16)
- "the receiving device to discover a second type of transmitting device and transition to a second state when the power signal is detected" (claim 16)
- "the receiving device is compatible with both the first type of transmitting device and the second type of transmitting device" (claim 17)
- "the second type of transmitting device is compatible with a standard protocol, and wherein the first type of device is compatible with a modified protocol" (claim 18)

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

At least claims 11, 13, and 16 (and their dependent claims) of the '231 Patent are invalid under 35 U.S.C. § 112(2) because they are mixed method-apparatus claims under the doctrine of *IPXL Holdings L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). In particular, at least the following claim terms and phrases improperly recite a method of using the entire claimed apparatus and/or functionality not tied to the capability of any recited structural element:

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 169

- "the transmitting device is to transition to the disconnect state when the first logic determines that the voltage value on the power bus is lost" (claim 11)
- "the transmitting device is to enable the pull up circuit in the discovered state" (claim 13)
- "the receiving device to enable a voltage potential of a predetermined value on the power bus and to drive a signal on the control bus at a first signal value in a disconnect state" (claim 16)
- "the receiving device to discover a first type of transmitting device and transition to a first state when the first signal is detected" (claim 16)
- "the receiving device to enable the switchable pull down circuit on the control bus and disable hot plug functionality upon discovering the first type of transmitting device" (claim 16)
- "the receiving device to discover a second type of transmitting device and transition to a second state when the power signal is detected" (claim 16)

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, at least Claims 10 and 16 (and their dependent claims) of the '231 Patent are invalid under 35 U.S.C. §§ 112(2) and (6) because the '231 Patent does not disclose sufficient structure corresponding to the function recited in at least the following means-plus-function claim limitations:

- "logic to detect signals on the cable interface" (claim 10)
- "a first logic to detect a voltage value on the power bus" (claim 10)
- "a second logic to detect signals on the control bus" (claim 10)
- "logic to discover a transmitting device coupled with the receiving device" (claim 16)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 170

- "a first logic to detect a first signal on the control bus" (claim 16)
- "a second logic to detect a power signal from the receiving device" (claim 16)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

X. THE ASSERTED CLAIMS OF THE '103 PATENT ARE INVALID

A. Identification of Prior Art

1. The '103 Patent Claims Are Anticipated by the Prior Art

Defendant contends that the prior art references charted in Exhibits H-1 through H-39, discussed in any incorporated IPR petitions and institution decisions, discussed or cited in the prosecution history and/or any reexamination proceedings, and/or described below anticipate and/or render obvious, alone or in combination, one or more of the Asserted Claims of the '103 Patent. As stated above, UCT asserts claims 1, 2, 3, 11, 12, 13, 17, 20, 21, 22 of the ''103 Patent ("the '103 Asserted Claims").

Some or all of the'103 Patent Asserted Claims are invalid as anticipated under 35 U.S.C. § 102 in view of each of the prior art references identified in the claim charts included in Exhibit H-1 through H-39 and/or identified in any incorporated IPR petitions and institution decisions, which identify specific examples of where each limitation of the '103 Asserted Claims is found in the prior art references. As explained above, the cited portions of prior art references identified in the attached claim charts are exemplary in nature and representative of the content and teaching of the prior art references, and should be understood in the context of the reference as a whole and as they would be understood by a person of ordinary skill in the art.

In addition to references identified in the incorporated IPR petitions and institution decisions, the prosecution history, and any reexamination proceedings, Defendant identifies the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 171

following references as anticipating one or more of the '103 Patent Asserted Claims under 35 U.S.C. § 102. The table of anticipating references below is exemplary, and it does not constitute an admission that any reference not listed below does not also anticipate the claims of the '103 Patent. Further, Defendant contends that any prior art reference in the attached charts that is charted for each limitation of any given claim anticipates that claim, regardless of whether that prior art reference is listed in the following tables.

a) Prior Art Patents and Applications

Number	Published/Issued Date/Filing Date	Short Name	Exhibit Number
U.S. Patent No. 8,799,537	Filed: May 1, 2012 Issued: Aug. 5, 2014	Zhu 537	H-1
U.S. Patent No. 7,558,326	Filed: Sep. 12, 2001 Issued: Jul. 7, 2009	Lyle	H-2
U.S. Patent Publ. No. 2013/0080665 A1	Filed: Sept. 22, 2011 Pub'd: Mar. 28, 2013 Issued: Apr. 26, 2016	Park	H-3
U.S. Patent No. 8,090.030	Filed: Jan. 4, 2008 Pub'd: Jul. 9, 2009 Issued: Jan. 3, 2012	Kim 030	H-4
U.S. Patent Publ. No. 2007/0201492	Filed: Dec. 2, 2003 Pub'd: Aug. 30, 2007 Issued: Jun. 19, 2012	Kobayashi	H-5
U.S. Patent No. 7,746,798	Filed: Nov. 7, 2001 Pub'd: Nov. 21, 2002 Issued: Jun. 29, 2010	'798 Patent	H-6
U.S. Patent No. 8,565,337	Filed: Feb. 7, 2007 Pub'd: Aug. 7, 2008 Issued: Oct. 13, 2013	Lida 337	H-7
U.S. Patent No. 8,355,327	Filed: Aug. 17, 2008 Pub'd: Dec. 11, 2008 Issued: Jan. 15, 2013	Lida 327	H-8
U.S. Patent No. 4,486,739	Filed: Jun. 30, 1982 Issued: Dec. 4, 1984	Franaszek	H-9
U.S. Patent Publ. No. 2010/0157169	Filed: Mar. 30, 2009 Pub'd: Jun. 24, 2010 Issued: Oct. 2, 2012	Yoshida	H-10
U.S. Patent No. 6,738,417	Filed: Sep. 9, 1999 Issued: May 18, 2004	Kim 417	H-11

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 172

U.S. Patent No. 8,238,445	Filed: Mar. 14, 2007 Pub'd: Jun. 5, 2008 Issued: Aug. 7, 2012	Wang 445	H-12
U.S. Patent No. 6,535,505	Filed: Sep. 30, 1998 Issued: Mar. 18, 2003	Hwang	H-13
U.S. Patent No. 5,420,640	Filed: Dec. 3, 1993 Issued: May 30, 1995	Munich	H-14
U.S. Patent Publ. No. 2010/0128176	Filed: Nov. 7, 2007 Pub'd: May 27, 2010 Issued: May 14, 2013	Nakajima	H-15
US 2015/0280895	Prov.: Apr. 1, 2014 Filed: Apr. 1, 2015 Pub'd: Oct. 1, 2015 Issued: Jan. 1, 2035	Whitby-Strevens	H-16
EP 2172011 B1	Filed: Jul. 1, 2008 Issued: Oct. 2, 2013	Butcher	H-17
US 2014/0019653	Filed: Jul. 11, 2012 Issued: Jan. 16, 2014	Amchislavsky	H-18
U.S. Patent Publ. No. 2014/0004741	Filed: Jul. 18, 2013 Pub'd: Jan. 2, 2014 Issued: Mar. 17, 2015	Jol	H-19
U.S. Patent No. 8,332,518	Filed: Aug. 13, 2007 Pub'd: Feb. 14, 2008 Issued: Dec. 11, 2012	Bradshaw	H-20
U.S. Patetnt No. 8,019,905	Filed: Feb. 11, 2008 Pub'd: Aug. 13, 2009 Issued: Sep. 13, 2011	Wu	H-21
U.S. Patent No. 8,966,134	Filed: Feb. 23, 2012 Pub'd: Aug. 23, 2012 Issued: Feb. 24, 2015	Anderson 134	H-28
U.S. Patent Publ. No. 2013/0244491 (issued as U.S. Patent No. 9,112,327)	Filed: Sep. 7, 2012 Pub'd: Sep. 19, 2013 Issued: Aug. 18, 2015	Sarwar 491 Sarwar 327	H-28; H-24
U.S. Patent Publ. No. 2006/0076977	Filed: Sep. 10, 2004 Pub'd: Apr. 13, 2006 Issued: Mar. 20, 2007	Zhu 977	H-37
U.S. Patent Publ. No. 2008/0084834	Filed: Oct. 9, 2006 Issued: Apr. 10, 2008	Stanek	H-39

b) Prior Art Publications

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Video Electronics Standards Association (VESA)	DisplayPort Standard Version 1, Revision 2	Jan. 5, 2010	DisplayPort 1.2	H-23; H-24
Hitachi, Ltd. Matsushita Electric Industrial Co., Ltd. Philips Consumer Electronics, International B.V. Silicon Image, Inc. Sony Corporation Thomson Inc. Toshiba Corporation	High-Definition Multimedia Interface Specification Version 1.3a	Nov. 10, 2006	HDMI 1.3a	H-22
Digital Display Working Group	Digital Visual Interface Revision 1.0	Apr. 2, 1999	DVI 1.0	H-25
Craig Wiley	"Invited Paper: DisplayPort 1.2, Embedded DisplayPort, and Future Trends," Society for Information Display (SID) Symposium Digest of Technical Papers: Volume 42, Issue 1 (June 2011) at 551-554	Aug. 12, 2012	Wiley	H-24; H-31
Mats Erik Setterberg	DisplayPort Link training optimization, Master's Thesis, Department of Computer Science and Engineering, Chalmers University of Technology,	2017	Setterberg	H-24

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 174

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
	University of Gothenburg (Sweden, 2017)			
Alan Kobayashi	DisplayPort Ver. 1.2 Overview, DisplayPort Developer Conference (Taipei, Dec. 6, 2010)	Dec. 6, 2010	DisplayPort 1.2 Overview	H-24
Craig Wiley	DisplayPort Technical Overview, IEEE International Conference on Consumer Electronics (ICCE) (Las Vegas, Nevada, Jan. 10, 2011)	Jan. 10, 2011	DisplayPort Technical Overview	H-24
John Canosa	"Fundamentals of Firewire," Questra Consulting		Fundamentals of Firewire	H-27
Michael Johas Teener	Technical Introduction to IEEE 1394		Firewire Technical Introduction	H-27
Blessy C Simon	Thunderbolt Pinout (Thunderbolt, 2, 3, and 4)	Mar. 21, 2024		H-28
Intel	Thunderbolt Technology, The Fastest Connection to your PC	2012		H-28
Intel	How Thunderbolt Technology Works	2013		H-28
Intel	Thunderbolt Technology, The Fastest Connection To Your PC Experience	2013		H-28
Intel	Introducing Thunderbolt.			H-28

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 175

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V.	Universal Serial Bus Specification, Revision 2.0	April 27, 2000	USB 2.0	H-26; H-29
USB Implementers Forum, Inc.	On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a	June 24, 2003	USB OTG 1.0a	H-29
maxim integrated	USB On-the-Go Basics	Dec. 20, 2002	USB OTG Basics	H-29
Texas Instruments	USB On-the-Go Solutions	Mar. 7-9, 2007	USB OTG Solutions	H-29
YouTube (XperiaBlog)	"Sony Xperia S USB OTG demo" YouTube video	Mar. 8, 2012	Xperia S YouTube Video 1	H-29
YouTube (Inam Ghafoor)	"Sony Xperia S: USB OTG Increases Storage Space / Transfer Files Between Smartphones," YouTube video	July 29, 2012	Xperia S YouTube Video 2	H-29
Digital Spy	Sony Xperia S UK release date announced	Jan. 10, 2012	Xperia S Digital Spy Article	H-29
CNET	Sony Xperia S (unlocked) review: Sony Xperia S (unlocked)	July 25, 2012	Xperia S CNET Article	H-29

Author or Publisher	Title	Publication/Use Date	Short Name	Exhibit Number
The Verge	Sony Xperia S review	Mar. 5, 2012	Xperia S The Verge Article	H-29
Sony	User Guide, Xperia S LT261	2013	XperiaS User Guide	H-29
Texas Instruments	DisplayPort to TMDS Translator	2008	TI SN75DP129	H-30
USB Implementers Forum, Inc.	Universal Serial Bus Device Class Definition for Video Devices, Revision 1.5	Aug. 9, 2012	USB Video Class	H-36
Apple	MacBook Pro User Guide (2011)	2011		H-28
Apple	MacBook Air User Guide (2011)	2011		H-28
Apple	Mac mini User Guide (2011)	2011		H-28
Apple	iMac User Guide (2011)	2011		H-28
Apple	Mac Pro QuickStart Guide (2013)	2013		H-28
Apple	MacBook Pro QuickStart Guide (2013)	2013		H-28

c) Prior Art Systems

On information and belief, systems implementing the protocols identified below were in public use, on sale, or otherwise available to the public before the priority date of the ’103 Patent. Defendant’s further investigation and/or subsequent discovery from Plaintiff or third parties with knowledge regarding prior art systems may reveal additional relevant prior art systems and/or

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 177

further information regarding the systems identified below, or other relevant prior art systems. Defendant reserves the right to supplement these Invalidity and Eligibility Contentions, based on subsequent investigation and discovery, including from third parties.

- Thunderbolt (Ex. H-28), including the Apple MacBook Pro (early 2011 and later); MacBook Air (mid 2011 and later); Mac mini (Mid 2011 and later); iMac (mid 2011 and later); Mac Pro (late 2013); and MacBook Pro (Retina, late 2013 and later)
- Firewire (Ex. H-27)
- DisplayPort (Ex. H-24)
- High-Definition Multimedia Interface (HDMI) (*e.g.,* HDMI 1.3a, Ex. H-22)
- DVI (*e.g.,* DVI 1.0, Ex. H-25)
- Multimedia High-definition Link (MHL)
- USB 2.0 (Ex. H-26, H-29)
- USB OTG (*see, e.g.,* Ex. H-29)
- PCI Express

An example prior art system that anticipates and/or renders obvious the '103 Asserted Claims includes the Sony Xperia line of smartphones (including, e.g. the Xperia S) which, on information and belief, transmitted and received USB data and video data over a USB OTG connection. *See, e.g.,* Ex. H-29.

Other examples of prior art systems that anticipate and/or render obvious the '103 Asserted Claims include the Apple MacBook Pro, MacBook Air, Mac mini, iMac, and Mac Pro, all of which implemented Thunderbolt. *See, e.g.*, Ex. H-28.

Defendant additionally identifies and relies on any system, product, or public knowledge or use that embodies or otherwise incorporates any of the prior art patents and publications listed

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 178

above. Defendant reserves the right to identify and rely on systems that represent different versions or are otherwise related variations of the identified systems. Defendant also incorporates by reference any and all other prior art systems identified in any other case brought by Plaintiff and/or involving the Asserted Patents.

To the extent any item of prior art cited above is deemed not to disclose, explicitly or inherently, any limitation of an asserted claim of the '103 Patent, Defendant contends that any difference between that prior art and the corresponding patent claim would have been either inherent in the art or obvious to a person of ordinary skill in the art, even if Defendant has not specifically denoted that the art is to be combined with the knowledge of a person of ordinary skill in the art.

d) Other Relevant References

Defendant reserves the right to rely on the prior art references identified in connection with one of the other Asserted Patents in connection with the '103 patent. In addition, Defendant hereby cites the following additional references as being relevant to the subject matter claimed in the '103 patent. Defendant is producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Defendant reserves the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103, as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Plaintiff may take regarding the scope of the asserted claims, and/or based on the Court's claim construction (once issued), Defendant reserves the right to revise these contentions and to rely on these references to prove the invalidity

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 179

of the ’103 patent in a manner consistent with this Court’s Rules and with the Federal Rules of Civil Procedure.

(1) Prior Art Patents and Applications

Number	Published/Issued Date
EP 2023632	Filed: May 16, 2007 Issued: Oct. 2, 2013
EP 2091253	Filed: Nov. 7, 2007 Issued: Jul. 29, 2015
JP 4844230	Filed: May 16, 2006 Pub’d: Nov. 29, 1007 Issued: Dec. 28, 2011
US 8,539,628	Filed: Oct. 2, 2008 Pub’d: Apr. 9, 2009 Issued: Jan. 22, 2013
US 2009/0185637	Filed: Sep. 4, 2008 Pub’d: Jul. 23, 2009
US 8,749,285	Filed: Mar. 15, 2013 Issued: Jun. 10, 2014
U.S. Patent Publ. No. 2009/0046690	Filed: Aug. 16, 2007 Pub’d: Feb. 19, 2009 Issued: Oct. 19, 2010
US 8,429,713	Filed: Apr. 2, 2007 Pub’d: Oct. 2, 2008 Issued: Apr. 23, 2013
U.S. Patent Publ. No. 2013/0244492	Filed: Sep. 7, 2012 Pub’d: Sep. 19, 2013
Japanese Patent No. 4844230	Filed: May 16, 2006 Pub’d: Nov. 29, 2007 Issued: Dec. 28, 2011
U.S. Patent Publ. No. 2010/0066919	Filed: Nov. 7, 2007 Pub’d: Mar. 18, 2010
U.S. Patent Publ. No. 2010/0073574	Filed: Jan. 20, 2009 Pub’d: Mar. 25, 2010
U.S. Patent Publ. No. 2010/0269137	Filed: Nov. 7, 2007 Pub’d: Oct. 21, 2010
U.S. Patent Publ. No. 2010/0118188	Filed: Nov. 7, 2007 Pub’d: May 13, 2010

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 180

(2) Prior Art Publications

Author or Publisher	Title	Publication/Use Date
Daryl J. Eigen	ISDN Architecture: A Basis for New Services	1985
Garry Musgrave	An Overview of ISDN Technology	Jan. 2001
Thomas Doumas (Hewlett Packard)	Next Generation Telephony: A look at Session Initiation Protocol	Apr. 5, 1999
Wikipedia	8b/10b encoding	

2. The '103 Patent Claims Are Obvious Over the Prior Art

To the extent Plaintiff argues that any limitation of the '103 Asserted Claims is not explicitly disclosed by an item of prior art identified above, in Exhibits H-1 through H-39, or discussed in any incorporated IPR petitions and institution decisions, any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. The item of prior art would, therefore, render the relevant claims invalid as obvious under 35 U.S.C. § 103.

Furthermore, it would have been obvious to combine any of the prior art in Exhibits H-1 through H-39 with each other, at least because all of these references relate to methods and apparatuses for communicating both audio/visual data and other data (such as control data) between a source and a sink. The charted references may further disclose transmitting audio/visual data unidirectionally, while transmitting and receiving other data and/or control data bidirectionally. Moreover, the references may further disclosed that audio/visual and other data

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 181

are communicated on one physical channel while control data is communicated on a different physical channel.

For example, U.S. Patent No. 8,799,537 to Zhu and Mohanty ("Zhu 537") teaches a device "configured to transmit, on a DisplayPort link to [a] second device, a data flow comprising both USB protocol data and uncompressed high definition media data signals." Zhu 537 at Abstract. The USB protocol data and uncompressed high definition media data may be communicated between the devices using a modified version of the link timing defined in the DisplayPort 1.2 specification. *Id.* at 34:52-61. Zhu 537 discloses that the USB protocol data may be transmitted bidirectionally on the same physical channel as the uncompressed high definition media data. *Id.* at 34:11-51. In particular, Zhu 537 teaches reverse USB transmission may occur during blanking periods. *Id.* at Abstract. Zhu 537 further explains that a DisplayPort link includes a separate sideband channel (AUX) for bidirectional communication of control data. *Id.* at 1:42 – 2:3.

U.S. Patent No. 7,558,326 to Lyle et al. ("Lyle"), entitled "Method and Apparatus for Sending Auxiliary Data on a TMDS-Like Link," describes a "communication system including a transmitter, a receiver, and a TMDS-like link, in which video data and auxiliary data (typically including timing data associated with other auxiliary data) are transmitted from the transmitter to the receiver, or in which video data are transmitted over the link from the transmitter to the receiver, and auxiliary data (typically including timing data associated with other auxiliary data) are transmitted from the receiver to the transmitter." Lyle at Abstract. Lyle explains that USB data is a type of auxiliary data that could be transmitted. Lyle at 50:47-50. Lyle describes embodiments in which "the transmitter transmits video data and auxiliary data to the receiver over a video channel of the link" (*id.* at 8:46-48) and explains that auxiliary data may be sent in the opposite direction by "reversing one video data transmission channel, or two or more video data

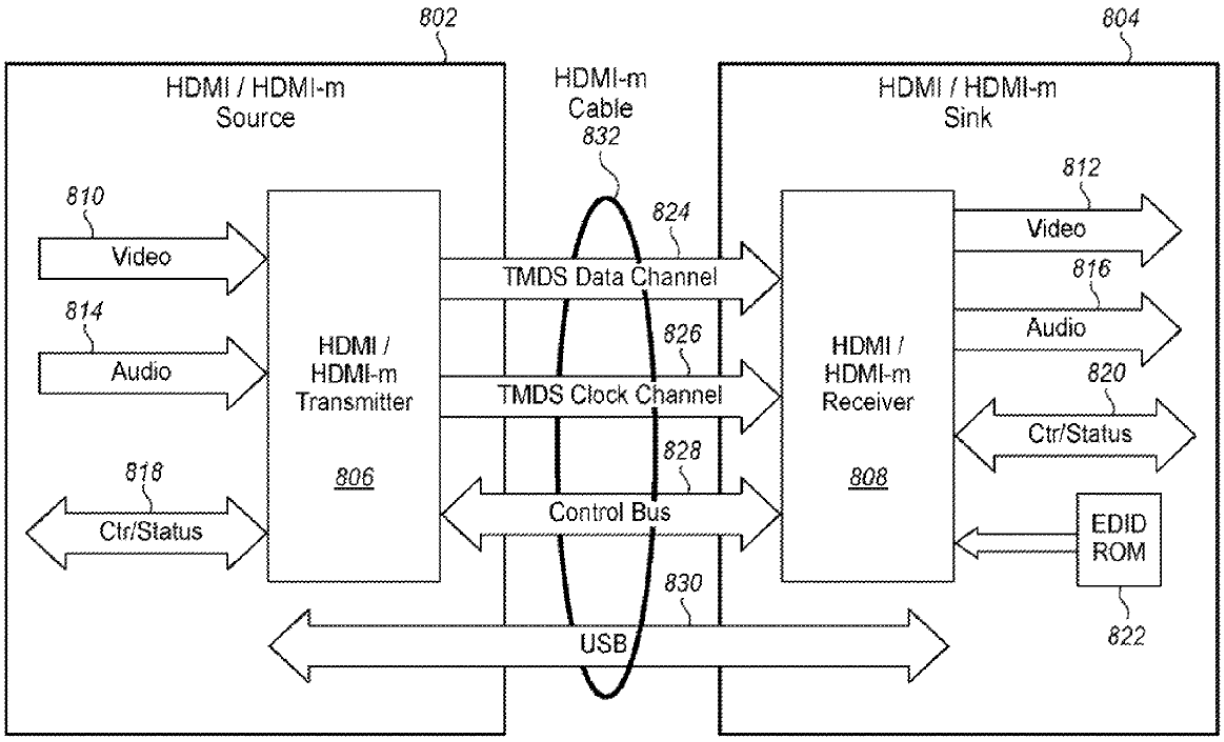
Universal Connectivity Technologies Inc.
Ex. 2005 - Page 182

transmission channels, during blanking periods (to send auxiliary data from the receiver of the video data to the transmitter of the video data)" (*id.* at 45:43-48). Further, embodiments include a Display Data Channel for bidirectional transmission of control data. *See id.* at 28:26-45.

Furthermore, US 2013/00800665 to Park and Shamarao ("Park") teaches a "data transmission system" including "a transmission link coupling the source device and the sink device. The transmission link includes a unidirectional main line having a plurality of main link channels, a bidirectional auxiliary line configured to transmit data between the source device and the sink device at a first data rate, and a unidirectional interrupt line. The transmission link is configured to transmit data from the source device to the sink device over one of the main link lines at a second data rate and to transmit data from the sink device to the source device over the auxiliary line at the second data rate. The transmission link may comply with the DisplayPort standard, and the data may be transmitted in accordance with the USB standard." Park at Abstract. In particular, Park discloses at least one embodiment in which USB data is transmitted bidirectionally over certain lines of the DisplayPort main link, while the remaining main link lines continue to transmit AV data. *Id.* at [0030] and Fig. 6.

U.S. Patent No. 8,090,030 to Kim et al. ("Kim 030"), issued Jan. 3, 2012 and published as US 2009/0178097 on July 9, 2009, discloses an "HDMI-M system architecture 800 includ[ing] a source 802 and a sink 804" connected by an HDMI-M cable that carries a TMDS data channel for video, audio and auxiliary data; a single-wire control bus; and a dedicated bidirectional USB connection. Kim 030 at 6:48 – 7:6. This is shown in Figure 8 of Kim 030:

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 183



Kim 030 was originally assigned to Silicon Image, Inc. and shares one or more inventors with the '103 Patent.

U.S. Patent Publ. No. 2007/0201492 to Kobayashi ("Kobayashi"), published Aug. 30, 2007, discloses a "compact packet based multimedia interface" including "a uni-directional main link having a single lane coupling the multimedia source to the multimedia sink arranged to carry a packetized multimedia data stream from the multimedia source to the multimedia display at a link rate that is independent of the native multimedia clock rate, a half duplex, bi-directional auxiliary channel connecting the multimedia source and the display that provides in concert with the uni-directional main link, a secondary communication link between the multimedia source and the display for transferring information between the multimedia source and the display, and a connector arrangement arranged to electrically connect the uni-directional main link and the half duplex, bi-directional auxiliary channel to the multimedia source and the display." Kobayashi at [0008]. Kobayashi was the basis for a rejection during prosecution of the '103 Patent. The

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 184

applicant overcame that objection by arguing that "Kobayashi describes sending video data over a first channel (e.g., main link 222), but only describes receiving USB data over a second, different channel (e.g., auxiliary channel, such as auxiliary channel 224 or auxiliary channel 524)" and thus "does not describe a single physical channel over which both video data is sent and data compliant with the first standard (e.g. USB data) is sent an received." Response to Office Action, July 12, 2017 at 8. The applicant did not argue, however, that any other limitation was missing from Kobayashi. In particular, the applicant did not dispute the examiner's mapping of Kobayashi's teachings regarding "link training" and reestablishing a link from the electrical idle state, and associated signals (such as training patterns and SYNC patterns), to the "synchronization signal" claim elements (see, e.g., claims 2, 3, 12, 13, and 17). Kobayashi's disclosure of these synchronization signals is very similar to the link training of the DisplayPort standards. As discussed below, a POSITA would have been motivated to combine Kobayashi with any reference teaching the unidirectional transmission of AV data and bidirectional transmission of USB or other data on the same physical channel.

U.S. Patent No. 8,565,337 to Lida et al. ("Lida 337"), published as US 2008/0187028 on Aug. 7, 2008, discloses methods and apparatuses for "transmitting data for different applications over a same communication network and in particular to transmitting high definition uncompressed multimedia audio/video (AV) streams and networking data such as appliance control data and Ethernet data over a same network." Lida 337 at 1:6-10. In particular, Lida 337 claims a "wired communication link" that includes a transceiver for transmitting a "multiplexed transmission comprising a first direction of a bidirectional data channel and lossless high definition digital video comprising pixel data, video clock related data, and video synchronization data" and receiving "a second transmission comprising a second direction of the bidirectional data channel."

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 185

Id. at 13:59 – 14:5. The bidirectional data may comprise "Digital Video Interfacing (DVI) control signal data, High Definition Multimedia Interface (HDMI) control signal data, or DisplayPort control signal data, I2C, Consumer Electronics Control (CEC), Hot Plug Detection (HPD), 5V indication, or a combination thereof." *Id.* at 18:6-13. The wired communication link of Lida 337 further includes a "second transceiver operative to receive the first multiplexed transmission and regenerate video timing based on the video clock related data, and order in which the video pixel data and the video synchronization data are received." *Id.* at 15:14-18.

U.S. Patent No. 8,355,327 to Lida et al. ("Lida 327"), published as US 2008/0304433 on Dec. 11, 2008, explains that "[c]urrent video, audio, or multimedia solutions transmit some or all of their standby and/or low power data types over dedicated wires. For example, a High-Definition Multimedia Interface (HDMI™) includes dedicated wires for DDC, HPD, and CEC controls. DisplayPort™ includes two wires for transmitting the auxiliary data." Lida 327 at 1:30-35. Lida 327 further discloses an apparatus and method for "transmitting in a first mode of operation bidirectional data between a source device and a sink device and unidirectional uncompressed high definition digital video from the source device to the sink device over at least a first subset of conductive wires comprised in a cable." *Id.* at 9:34-40; Figs. 11 and 17. In particular, Lida 327 lists several examples of different "data types" that may be transmitted: "video pixel data; audio data; video synchronization control data, such as horizontal and vertical video picture synchronizations; video system controls, such as CEC, HPD and DDC signals; or general data transmissions, such as Ethernet data, USB data, or RS232 data; or infra-red (IR) control data." *Id.* at 4:1-7. Lida 327 incorporates the disclosure of Lida 337 by reference. *See id.* at 1:7-9.

U.S. Patent Publ. No. 2010/0157169 to Yoshida and Sato ("Yoshida") describes a modification of an HDMI protocol to allow bidirectional high-speed data transmission over an

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 186

HDMI connector. In particular, Yoshida describes reassigning pins 14 (Reserved) and 19 (HPD) for bidirectional LAN communication. *See* Yoshida at Fig. 9 and corresponding description.

U.S. Patent No. 6,738,417 to Kim et al. ("Kim 417"), issued May 18, 2004, discloses and claims "[a]n apparatus for bidirectional data transfer between a computer and a display connected through cables having a first end at the computer and a second end at the display, the apparatus comprising: a transmitter located at the computer for transmitting a pixel clock and forward data aligned to the pixel clock to the receiver in a forward channel; [and] a receiver located at the display for receiving the pixel clock and the forward data from the transmitter, and for transmitting backward data to the transmitter in a backward channel, wherein the transmitter further comprises an oversampling circuit for generating a plurality of oversampling clocks for sampling the backward data received from the receiver, each clock being equally spaced in phase from its adjacent clock." Kim 417 at 5:32-47. Kim 417 further describes the use of synchronization signals. *Id.* at 5:10-23. Kim 417 was originally assigned to Silicon Image, Inc. and shares one or more inventors with the '103 Patent.

U.S. Patent Publ. No. 2010/0128176 to Nakajima et al. ("Nakajima") filed on November 7, 2007 and published on May 27, 2010, discloses "a receiving device that receives video and audio signals from an external apparatus to perform image displaying and audio outputting, a delay-information transmitting method of the receiving device, an audio output device, and a delay-control method of the audio output device." Nakajima at ¶ 0001. Specifically, Nakajima describes an "HDMI source [which] transmits a differential signal corresponding to pixel data of a non-compressed 1-screen image unidirectionally to the HDMI sink [] through a plurality of channels in an effective image period . . . i.e., a period obtained by removing a horizontal blanking period and a vertical blanking period from a period between one vertical synchronizing signal and

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 187

a subsequent vertical synchronizing signal. The HDMI source [] further transmits differential signals corresponding to the audio data and the control data which accompany at least the image, other auxiliary data, etc., unidirectionally to the HDMI sink [] through a plurality of channels in the horizontal blanking period or the vertical blanking period." Nakajima at ¶ 0122. The inventor of Nakajima is also named on several other patents and published applications, each of which includes similar disclosure, including:

- Japanese Patent No. 4844230
- U.S. Patent Publ. No. 2010/0066919
- U.S. Patent Publ. No. 2010/0073574
- U.S. Patent Publ. No. 2010/0269137
- U.S. Patent Publ. No. 2010/0118188

U.S. Patent No. 7,836,223 to Butcher ("Butcher") is another Silicon Image patent that discusses modifying HDMI to allow bidirectional data transfer. In particular, Butcher modifies HDMI so that Ethernet data can be communicated bidirectionally over the AV channels at times when those channels are not used to transmit unidirectional AV data.

U.S. Patent Publ. No. 2014/0019653 to Amchislavsky et al. ("Amchislavsky") is yet another Silicon Image patent relating to bidirectional communication of USB over an AV protocol link. In particular, just like the '103 patent, Amchislavsky describes bidirectional communication of USB over a Mobile High-definition Link (MHL) connection. Amchislavsky describes a link including a data channel for AV data and a separate bidirectional control channel. According to Amchislavsky, the MHL "specification allows for a connector to be utilized for transmission of both MHL data and USB™ (Universal Serial Bus) data, where USB data may be transmitted when the connector is not being utilized for the transmission of MHL data" but that "such use may be

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 188

limited to only one of such protocols at any time." Amchislavsky at [0002]-[0003]. Amchislavsky thus describes methods and apparatus allowing simultaneous bidirectional USB data transmission and unidirectional AV data transmission over an MHL link.

U.S. Patent Publ. No. 2014/0004741 to Jol ("Jol"), published Jan. 2, 2014, discloses a connector with "one pair of contacts for transmitting data and one pair of contacts for receiving data. All data transmitted and received using the plug connector is serialized/de-serialized to enable data transmission at a very high rate." Jol at Abstract. The serialized data includes video data (such as HDMI and DisplayPort data) and USB data. Jol further describes a "single wire" for control. Jol at [0020].

U.S. Patent Publication No. 2008/0084834 to Stanek ("Stanek"), published Apr. 10, 2008, discloses methods and apparatus for transmitting/receiving unidirectional HDMI video data and bidirectional USB data over the same multimedia link, and sending/receiving control data over a bidirectional control line (e.g. CEC line).

Furthermore, the Video Electronics Standards Association (VESA) DisplayPort Standard Version 1, Revision 2 ("DisplayPort 1.2") "define[s] a flexible system and apparatus capable of transporting video, audio and other data between a Source Device and a Sink Device over a digital communications interface." DisplayPort 1.2 at 1. A DisplayPort link as defined in DisplayPort 1.2 "consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line." *Id.* at 34. "[T]he Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device." *Id.* Moreover, DisplayPort 1.2

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 189

included a Fast AUX capability, which allowed bidirectional communication of USB 2.0 data over the AUX channel. *Id.* at 20.

Additional information about the operation of prior art systems implementing DisplayPort 1.2 can be found in Craig Raymond Wiley, "Invited Paper: DisplayPort 1.2, Embedded DisplayPort, and Future Trends," *Society for Information Display (SID) Symposium Digest of Technical Papers*: Volume 42, Issue 1 (June 2011) at 551-554 (Wiley) (published Aug. 12, 2012) ("Wiley"); Mats Erik Setterberg, DisplayPort Link training optimization, Master's Thesis, Department of Computer Science and Engineering, Chalmers University of Technology, University of Gothenburg (Sweden, 2017) ("Setterberg"); Alan Kobayashi, DisplayPort Ver. 1.2 Overview, DisplayPort Developer Conference (Taipei, Dec. 6, 2010) ("DisplayPort 1.2 Overview"); Craig Wiley, DisplayPort Technical Overview, IEEE International Conference on Consumer Electronics (ICCE) (Las Vegas, Nevada, Jan. 10, 2011) ("DisplayPort Technical Overview"); U.S. Patent Publ. No. 2013/0244491 to Sarwar and Terlizzi ("Sarwar 491).

Digital Visual Interface Revision 1.0 ("DVI 1.0") is a protocol specification for high-speed digital AV content. DVI 1.0 included a transition-minimized differential signaling (TMDS) link to send graphics data to a display. *See* DVI 1.0 at Section 2.1. DVI 1.0 also incorporates the VESA display data channel (DDC) and extended display identification data (EDID) for control signaling. DVI 1.0 discloses synchronization signals.

IEEE 1394-1995 ("Firewire") was a high-speed peer-to-peer serial interface standard. The Firewire connector included six wires, including two signal pairs and one power pair. Firewire included the use of tokens during configuration, arbitration, and data transmission.

"High-Definition Multimedia Interface Specification Version 1.3a" ("HDMI 1.3a"), published Nov. 10, 2006, by HDMI Licensing, LLC defines an interface "for transmitting digital

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 190

television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays" based on "Transition Minimized Differential Signaling (TMDS)." HDMI 1.3a at 1. "HDMI can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats [and] can also carry control and status information in both directions." *Id.* In particular, HDMI 1.3a describes an interface between an HDMI source and HDMI sink including "four differential pairs that make up the TMDS data and clock channels [that] are used to carry video, audio and auxiliary data" from source to sink, a bidirectional display data channel (DDC) line "used for configuration and status exchange between a single Source and a single Sink," and an optional bidirectional consumer electronics control (CEC) line that "provides high-level control functions between all of the various audiovisual products in a user's environment." *Id.* at 8. This is shown in Figure 3-1:

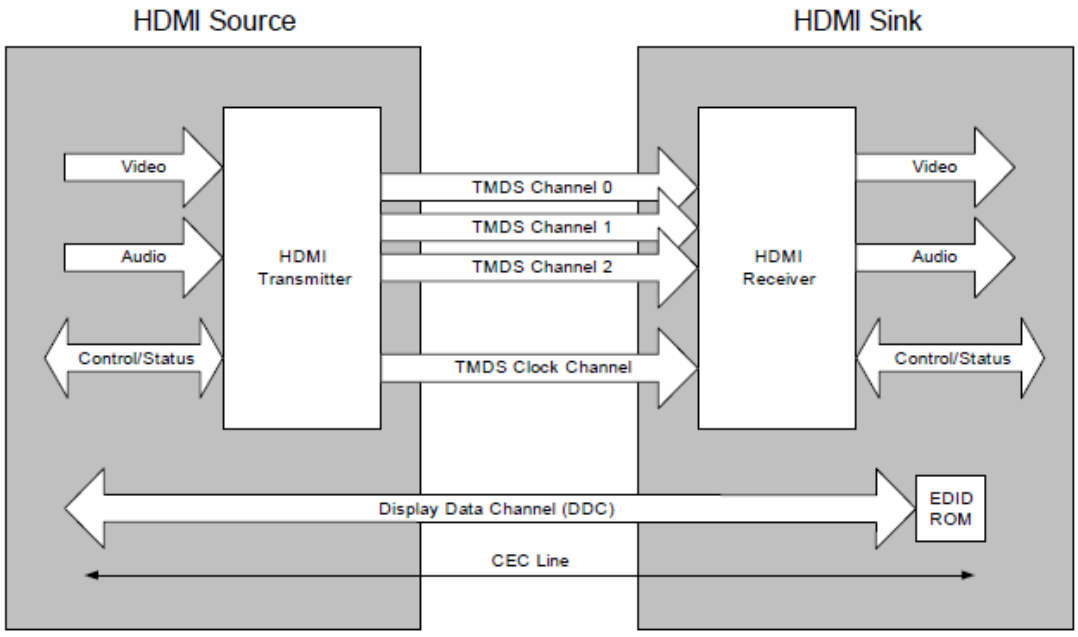
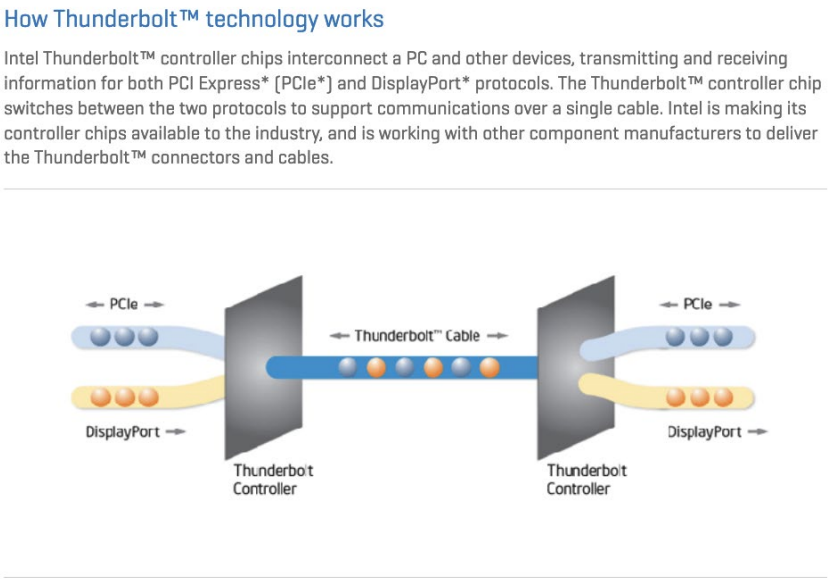


Figure 3-1 HDMI Block Diagram

Thunderbolt is a data communication protocol capable of transmitting bidirectional general data (e.g. PCI Express data) and unidirectional DisplayPort data over a single cable. The PCIe and

DisplayPort data are multiplexed and transmitted over the same Thunderbolt cable, as shown below:



U.S. Patent No. 7,746,798 to Shin et al. ("the '798 Patent"), issued June 29, 2010 and published as US 2002/0172200 on Nov. 21, 2002, describes a "serial communications architecture for communicating between hosts and data store devices." The '798 Patent discloses the use of "synchronization signals" in language nearly identical to the discussion of synchronization signals in the '103 Patent. For example, the '798 Patent states the following:

> A synchronization signal is typically used by the physical layer to help ensure correct alignment of symbols. A transmitting communications node periodically transmits synchronization primitives so that the receiving communications node can properly align with that synchronization primitive. When a communications node receives a synchronization primitive, it knows that the primitive is correctly aligned on a symbol boundary.

'798 Patent at 14:34-41; *compare* '103 Patent at claim 17 and 5:55-59. The '798 Patent was originally assigned to Silicon Image, Inc. and is asserted by UCT in this litigation.

U.S. Patent No. 4,486,739 to Franaszek ("Franaszek") describes an 8b/10b coding scheme, in which 8 bits are encoded into 10 bit code words. Franaszek discloses several special characters,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 192

including "comma" codes that are used for synchronization. The 8b/10b coding scheme developed by Franaszek is used in a variety of communication protocols, including DisplayPort.

U.S. Patent No. 8,238,445 to Wang ("Wang 445") discloses a video and audio data synchronization method for HDMI. In particular, Wang describes the transmission of synchronization signals and a method for determining and aligning symbol boundaries in HDMI data transmission.

U.S. Patent No. 6,535,505 to Hwang et al. ("Hwang") discloses the use of frame synchronization signals in time-division multiplex communications. U.S. Patent 5,420,640 to Munich et al. ("Munich") discloses a system for multiplexed communication of video, audio, and other data in which various synchronization signals are transmitted.

U.S. Patent No. 5,420,640 to Munich et al. ("Munich") discloses a receiver for receiving digital data frames including multiple lines of data, including video, audio, and other data. Munich at Abstract. Munich further discloses that the beginning of each frame of data is indicated with a frame synchronization word and the beginning of each line of data is indicated with a horizontal synchronization byte. *Id.*

U.S. Patent Publ. No. 2015/0280895 to Whitby-Strevens and Johnston ("Whitby-Strevens") describes modifications to DisplayPort standards. Whitby-Strevens explicitly lists several DisplayPort standards, including DisplayPort 1.2. *See* Whitby-Strevens at [0036]. It also explicitly discusses USB. *Id.* at [0033] and [0042]. In particular, Whitby-Strevens discusses the use of 8b/10b encoded control symbols in the DisplayPort standards, including control symbols used for synchronization during normal operation and link training.

Universal Serial Bus Specification, Revision 2.0, April 27, 2000 ("USB 2.0"). USB 2.0 provides for packet-based, half-duplex bidirectional data communication over a single differential

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 193

pair of wires. Although USB 2.0 is intended for communicating a range of different data types, one stated goal of USB 2.0 was to provide "[f]ull support for real-time data for voice, audio, and video." USB 2.0 at 11. Different classes of USB 2.0 devices are capable of different functions; one example is the video class (discussed in more detail below).

On-The-Go Supplement to the USB 2.0 Specification ("USB OTG") is a supplement that added new functionality to the protocol specified in the Universal Serial Bus Specification, Revision 2.0 ("USB 2.0"). USB OTG added the capability for USB devices to communicate via the GND and VBUS lines to negotiate roles. Mobile phones were one target (or anticipated) application of USB OTG. For example, the Sony Xperia line of smartphones (including, e.g. the Xperia S) had USB OTG capabilities. YouTube videos uploaded in 2012 show users streaming video files from USB flash drives to their phones over a USB OTG connection, and documents describe bidirectional data transfer to and from an Xperia 6 via USB OTG.

Universal Serial Bus Device Class Definition for Video Devices, Revision 1.5, August 9, 2012 ("USB Video Class") defines the capabilities and characteristics of a USB Video Class device. It explicitly refers to USB 2.0 (as well as the later USB 3.0).

U.S. Patent Publ. No. 2006/0076977 to Zhu ("Zhu 977") describes devices and methods to enable a USB 1.1 device to communicate with a USB OTG device. In particular, Zhu 977 explains the operation of USB OTG, including bidirectional transmission of control signals through VBUS pulsing as part of session request protocol (SRP) and the transmission of video and USB data.

U.S. Patent No. 8,019,905 ("Wu") discloses methods and apparatus for converting AV and control data between DisplayPort and a TMDS-based protocol such as DVI, for communication between one or more video sources and a video display. For example, Wu 905 describes converting image data from DisplayPort format to DVI format for communication to a video display. Wu 905

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 194

also explicitly describes converting control signals between DisplayPort AUX channel and DVI DDC lines for bidirectional communication of control information between the source and sink.

TI SN75DP129 is a chip for converting "a Dual-Mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output." The TMDS output may be compliant with DVI 1.0 or HDMI 1.3.

U.S. Patent No. 8,332,518 to Bradshaw et al. ("Bradshaw") filed on August 13, 2007 and issued on December 11, 2012, discloses methods and devices involving a "bidirectional communication protocol for data communication between a first device and a second device. The method includes: during a first time interval, transmitting data from the first device to the second device; and during a second time interval, (a) after the occurrence of a first event, (i) suspending data transmission from the first device to the second device; and (ii) transmitting control data from the second device to the first device; and (b) after the occurrence of a second event, transmitting control data from the first device to the second device." Bradshaw at Abst. The communication protocol disclosed in Bradshaw involves the use of various synchronization signals between the first and second devices. *See, e.g.*, Bradshaw at 3:64-4:16, FIGs. 2-5.

Accordingly, because each of the identified references are directed to similar devices in the similar field of endeavor, a person of ordinary skill in the art would be motivated to combine the teachings of two or more references together because the references disclose similar systems that solve the same problems in similar ways. Thus, it would have been obvious to one of ordinary skill in the art to combine any of the foregoing references and one of ordinary skill would have expected such a combination to be successful.

Thus, to the extent that it is determined that any of the above references do not disclose a particular claim element, it would have been obvious to modify the teachings of that reference to

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 195

include such element as taught in any other of the above references that discloses such element (as documented in the claim charts attached as Exhibits H-1 through H-39).

For example, to the extent that it is determined that any of the above references do not disclose "forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data" and/or "backward units of data comprising backward data compliant with the first standard" as claimed, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Butcher, Amchislavsky, Stanek, and Jol. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose a "over a second physical channel of the multimedia link distinct from the first physical channel: sending control data from the source device to the sink device" and/or "receiving control data from the sink device to the source device over the second physical channel of the multimedia link distinct from the first physical channel" as recited in claims 1, 10, 11, 20, 21, and/or 22, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB OTG, Thunderbolt, Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Butcher, Amchislavsky, Stanek, and Jol. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 196

As an additional example, to the extent that it is determined that any of the above references do not disclose the claimed "transmitter[s]," "receiver[s]," and "transceiver[s]" recited in claims 21 and 22, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB OTG, Thunderbolt, Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Butcher, Amchislavsky, Stanek, and Jol. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "sending a first synchronization signal of a first length after sending a first forward unit of data of the forward units of data, and before sending another forward unit of data from the source device" as recited in claims 2 and 12, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle, Kim 030, Kobayashi,'798 Patent, Lida 337, Franaszek, Yoshida, Kim 417, Wang, Hwang, Munich, Whitby-Strevens, DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB 2.0 (and thus USB OTG), and Thunderbolt. For example, as discussed in Craig Wiley, DisplayPort Technical Overview, IEEE International Conference on Consumer Electronics (ICCE) (Las Vegas, Nevada, Jan. 10, 2011) ("DisplayPort Technical Overview"), synchronization symbols have been in use since the first consumer video interface in 1941. DisplayPort Technical Overview at 6-7. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 197

As an additional example, to the extent that it is determined that any of the above references do not disclose "sending a second synchronization signal of a second length longer than the first synchronization to initialize communication over the first physical channel before sending the first forward unit of data" as recited in claims 3 and 13, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle, Kim 030, Kobayashi, '798 Patent, Lida 337, Franaszek, Yoshida, Kim 417, Wang, Hwang, Munich, Whitby-Strevens, DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB 2.0 (and thus USB OTG), and Thunderbolt. Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

As an additional example, to the extent that it is determined that any of the above references do not disclose "aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal." as recited in claim 17, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Kobayashi, '798 Patent, Franaszek, Yoshida, Kim 417, Wang, Hwang, Munich, Whitby-Strevens, DisplayPort 1.2, DisplayPort System, DVI 1.0, HDMI 1.3a, USB 2.0 (and thus USB OTG), and Thunderbolt. Aligning symbol boundaries was a well-known use for synchronization signals. *See, e.g.,* '798 patent at 15:17-21 ("The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers."). Therefore, a person of ordinary skill in the art would be motivated to make such a modification and/or combination.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 198

As an additional example, to the extent that it is determined that any of the above references do not disclose the basic concept of the independent claims—namely, over a first physical channel, communicating AV data in one direction and USB data bidirectionally and, over a second physical channel, communicating control information—it would have been obvious to modify any such reference in view of Zhu 537, Lyle, Park, Kim 030, Kobayashi, Lida 337, Lida 327, Yoshida, Kim 417, Nakajima, Butcher, Amchislavsky, Jol, DisplayPort 1.2, DisplayPort System, and USB OTG system (e.g. Sony Xperia S) to include this feature. As demonstrated in the attached claim charts for these references, each discloses transmitting AV data in one direction and transmitting and receiving bidirectional data. Although the references differ on how the unidirectional AV data and bidirectional data are assigned to various channels, collectively they demonstrated that various permutations were well known in the art at the time. For example, Zhu 537, Lyle, and Park each disclose communicating unidirectional AV data and bidirectional USB data on one channel (and in some cases, on the same wire pair) while communicating bidirectional control data on a separate channel. Lida 337 discloses communicating AV data, ethernet data, and control data in one direction on a first channel, and ethernet and control data in the opposite direction on a second channel. Lida 327 and Kobayashi disclose transmitting AV data unidirectionally on a first channel, while transmitting USB data and control signals bidirectionally on a second channel. Kim 030 discloses transmitting AV data unidirectionally on a first channel, USB data bidirectionally on a second channel, and control signals bidirectionally on a third channel. And Butcher describes transmitting AV data and other data in one direction on a first channel, receiving other data on a second channel, and communicating control signals bidirectionally on a third channel. Thus, a POSITA at the time would have known that it was possible to communicate unidirectional AV data, bidirectional USB data, and bidirectional control signals over a variety of channel

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 199

permutations and combinations, and it would have been obvious to try the specific permutation claimed in the '103 Patent—especially considering that multiple prior art references taught that same permutation.

As an additional example, to the extent that it is determined that any of the above references do not disclose "[a] non-transitory computer readable storage medium storing instructions thereon, the instructions representing a digital design of a circuit" as recited in claim 22, it would further have been obvious to modify the teachings of that reference to include this feature in view of the knowledge of a POSITA and the teachings of these features in at least the following references: *See, e.g.*, Zhu 537, Lyle, Kim 030, Lida 327, Butcher, and Amchislavsky.

A person skilled in the art would have been motivated to combine any of the above references. In particular, the combinations identified herein would merely have been (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of known technique to improve similar devices or methods in the same way; (d) application of a known technique to a known device or method ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art. Moreover, a person of ordinary skill in the art had a reason to combine these references because—at a minimum—they all pertain to communicating different forms of data over a multimedia link.

As discussed above, the motivation to combine the teachings of the patents and other prior art referenced above is found in the art as specified in the charts and in: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 200

knowledge of persons of ordinary skill in the art; and (4) the fact that the prior art is generally directed towards providing connectivity for communication of data including A/V data between, for example, computers, peripherals, and/or displays, and (5) the predictable results obtained in combining the different elements of the prior art. The Supreme Court has held that a showing of a motivation to combine within the references themselves is not required to prove obviousness. *See KSR*, 550 U.S. at 401 ("Any need or problem known in the field of endeavor at the time of invention may provide the motivation to combine.").

As illustrated in the claim charts attached as Exhibits H-1, H-23, H-24, and H32, Zhu 537, alone or in combination with a reference describing DisplayPort, including but not limited to DisplayPort 1.2, disclose or render obvious all elements of the '103 Asserted Claims. Specifically, Zhu 537 teaches methods and apparatuses for transmitting USB data and audio/visual data over a DisplayPort link. Zhu 537 teaches a "mixed mode" in which USB may be multiplexed with DisplayPort data for transmission in the forward direction, while USB data may also be transmitted in the backward direction during a video blanking period. Zhu 537 explains that DisplayPort includes one to four lanes for transmission of video data and a separate bidirectional side-band channel for control information. DisplayPort 1.2 further describes the transmission, reception, and use of numerous signals (including, e.g., control symbols and symbol patterns for link training) for purposes of initializing communication, synchronization, and alignment of symbol boundaries. A person skilled in the art would have been motivated to combine Zhu 537 with DisplayPort 1.2 for the reasons provided above. Both Zhu 537 and DisplayPort 1.2 relate to communication of A/V data and, in particular, data compliant with the DisplayPort 1.2 standard. Moreover, Zhu 537 explicitly references DisplayPort 1.2 (and other versions of the DisplayPort standard) and discloses embodiments that relate explicitly to the DisplayPort protocol. *See, e.g.,* Zhu 537 at Abstract; 1:42

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 201

– 2:14; 5:4-17; 17:3 – 18:20; Figs. 14-15; 33:20 – 36:24; Figs. 34-35, 41. Specifically, Zhu 537 describes a "system and corresponding method for selectively communicating data between a first device and a second device" in which "[t]he first device may be configured to transmit, on a DisplayPort link to the second device, a data flow comprising both USB protocol and uncompressed high definition media data signals." *Id.* at Abstract. Zhu 537 specifically describes embodiments that are built on modifications to various aspects of DisplayPort 1.2. *See id.* at 34:52 – 36:24. Moreover, Zhu 537 incorporates by reference the VESA DisplayPort standards and lists several example versions. *Id.* at 1:42-47; 34:52-65. A POSITA would have been specifically motivated to combine Zhu 537 with DisplayPort 1.2's teachings about the side-band channel, including the AUX and HPD lines. Zhu 537 explicitly references these concepts multiple times. *See id.* at 1:52-57; 5:6-11. Moreover, a POSITA would understand that Zhu 537's references to a "DisplayPort link" (*id.* at 33:26-29), "first media port" (*id.* at 33:34-38), and "second media port" (*id.* at 33:43-46) would inherently include the channels and links described in the DisplayPort standards available at the time, including the side-band channel (e.g. AUX), and would also include the various control symbols and symbol patterns for link training and other purposes. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, Zhu 537 teaches a simple substitution of a modified MST protocol for the one specified in DisplayPort 1.2.

Moreover, as illustrated in the claim charts attached as Exhibits H-3, H-23, and H-24, Park, alone or in combination with a reference describing DisplayPort, including but not limited to DisplayPort 1.2, disclose or render obvious all elements of the '103 Asserted Claims. Specifically, Park teaches methods and apparatuses for transmitting USB data and audio/visual data over a DisplayPort link. A person skilled in the art would have been motivated to combine Park with

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 202

DisplayPort 1.2 for many of the same reasons described above in connection with Zhu 537. Both Park and DisplayPort 1.2 relate to communication of A/V data and, in particular, data compliant with a DisplayPort standard. In fact, Park mentions DisplayPort in its title: "System and method for transmitting USB data over a DisplayPort transmission link." *See also* Park at Abstract ("The transmission link may comply with the DisplayPort standard"). The term "DisplayPort" appears at least 40 times in Park. A POSITA would thus have been specifically motivated to combine Park with DisplayPort 1.2's teachings about, for example, the side-band channel, including the AUX and HPD lines, and synchronization / control signals. Additionally, the combination reflects no more than a simple substitution of known elements for one another to obtain predictable results. For example, Park teaches a simple substitution of a modified version of a DisplayPort link.

A POSITA would have been further motivated to modify Kim 030 to communicate unidirectional AV data and bidirectional USB data over a single physical channel connected to a single transmitter and single receiver. As discussed above, Kim 030 teaches a multimedia link between source and sink for communicating unidirectional AV (HDMI) data, bidirectional USB data, and bidirectional control signals. Unlike the independent claims of the '103 Patent, in Kim 030, AV data is communicated over one set of channels while bidirectional USB data is communicated over "a dedicated USB connection differential pair." Kim 030 at 6:48 – 7:6. As discussed above, however, UCT applies a broad construction in its infringement contentions such that it alleges that multiple distinct differential pairs can form a single "physical channel." Thus, at least under UCT's own applied construction, there is no distinction between Kim 030 and at least the independent claims of the '030 Patent. Regardless, it would have been obvious to a POSITA in view of the knowledge at the time (including the teaching of, for example, references such as Zhu 537 and Park) that Kim 030 could be modified such that unidirectional AV data and

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 203

bidirectional USB data would be communicated over a single physical channel (and by the same transmitter and receiver) by, for example, multiplexing AV and USB data in the forward direction and using half-duplex communication to send USB data in the reverse direction during available time slots (such as a blanking period), as taught in Zhu 537. The teachings of Kim 030 itself would provide motivation to modify Kim 030. For example, Kim 030 is directed to a mobile version of HDMI and, as such, proposes to reduce the size of the HDMI connector for use with mobile devices. *See* Kim 030 at 4:31-37. To facilitate this, Kim 030 proposes multiplexing multiple HDMI channels to for communication on a single pair of wires. *See* Kim 030 at 4:38-54 and 5:26-38. And the claims of Kim 030 recite "merg[ing] multiple channels of a high-definition interface into a single channel." Kim 030 at claim 1. And at a high level, Kim 030 explicitly encourages further modification of connectors for use with HDMI. *See* Kim 030 at 1:29-37. Taken together, these teachings of Kim 030 would have motivated a POSITA to modify Kim 030 so as to multiplex AV and USB data together onto a single physical channel, as taught explicitly in Zhu 537. *See, e.g.,* Zhu 537 at 34:11-24. This motivation is further supported by Zhu 537's teaching that its principles are applicable to HDMI, which is the standard that is the focus of Kim 030. *Id.* at 20:58 – 21:5.

For similar reasons, a POSITA would have been motivated to modify Yoshida to communicate unidirectional AV data and bidirectional LAN data over a single physical channel connected to a single transmitter and single receiver. Moreover, a POSITA would have been motivated to modify Yoshida's teachings to substitute bidirectional transmission of USB data for bidirectional transmission of LAN data. Both LAN and USB were well-known packet-based protocols and a POSITA would have understood that a link for communicating one could be modified to allow communication of the other. Moreover, a POSITA would have been familiar with prior art (including references such as Zhu 537, Park, Lyle, and Kim 030) that explicitly

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 204

described the bidirectional transmission of USB data over a multimedia link, channel, and/or cable and would have been motivated and found it obvious to combine Yoshida with the teachings of any one or more of those references.

A POSITA would also have been motivated to and found it obvious to combine Lyle with (or modify Lyle in view of) the teachings of DVI 1.0. Lyle describes a "communication system including a transmitter, a receiver, and a TMDS-like link, in which video data and auxiliary data (typically including timing data associated with other auxiliary data) are transmitted from the transmitter to the receiver, or in which video data are transmitted over the link from the transmitter to the receiver, and auxiliary data (typically including timing data associated with other auxiliary data) are transmitted from the receiver to the transmitter." Lyle at Abstract. Lyle explains that USB data is a type of auxiliary data that could be transmitted. Lyle at 50:47-50. Lyle describes embodiments in which "the transmitter transmits video data and auxiliary data to the receiver over a video channel of the link" (*id.* at 8:46-48) and explains that auxiliary data may be sent in the opposite direction by "reversing one video data transmission channel, or two or more video data transmission channels, during blanking periods (to send auxiliary data from the receiver of the video data to the transmitter of the video data)" (*id.* at 45:43-48). Further, embodiments include a Display Data Channel for bidirectional transmission of control data. *See id.* at 28:26-45. Lyle explicitly describes modifications to a TMDS link according to the DVI protocol. A POSITA would therefore have found it obvious that the system described in Lyle would include features, such as synchronization signals, disclosed in DVI standards, such as DVI 1.0 (or at the very least, would have found it obvious to combine Lyle with such teachings in DVI 1.0).

A POSITA would also have been motivated to and found it obvious to combine Jol with the teachings of various refences, including USB 2.0, DisplayPort 1.2, and HDMI 1.3a. Jol

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 205

explicitly discusses transmitting and receiving data according to each of these protocols over a multimedia link. *See, e.g.,* Jol at Fig. 4, [0031], [0034]-[0036]. A POSITA would thus have been motivated to combine Jol with (or modify Jol in view of) the teachings in these other references of, for example, a dedicated bidirectional control channel and a synchronization signals. For example, Jol discusses the need to communicate control signals including via "[a] single wire, serial control chip." Jol at [0020]. A POSITA would have thus recognized the utility of a dedicated control channel as discussed in references such as USB 2.0, DisplayPort 1.2, and HDMI 1.3a when communicating data according to such protocols. Similarly, a POSITA would have recognized that the protocols described in USB 2.0, DisplayPort 1.2, and HDMI 1.3a include the synchronization symbols described in those references, and would have found it obvious that the system described in Jol would thus transmit such synchronization signals (or at the very least, would have found it obvious to use the system described in Jol to transmit such synchronization signals).

A POSITA would also have been motivated to and found it obvious to combine Stanek with the teachings of any HDMI specification, including HDMI 1.3a. Stanek explicitly references HDMI and, in particular, incorporates by reference the HDMI 1.3 specification. Stanek at [0036]. A POSITA would also have been motivated to combine Stanek with any USB standard, including USB 2.0, because Stanek explicitly references USB throughout its disclosure specifically cites to USB 2.0. Stanek at [0004]. A POSITA would also have been motivated to combine Stanek with DVI 1.0, because Stanek also mentions DVI. Stanek at [0005].

To the extent that any of Park, Kim 030, Kobayashi, Lida 327, Lida 337, Yoshida, Kim 417, Butcher, Amchislavsky, or Nakajima do not disclose sending forward units of data including video data and USB data over a first physical channel during first time periods and receiving USB data over the first physical channel during second time periods, a POSITA would have been

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 206

motivated and found it obvious to modify the teaching of such reference with, for example, the teachings in Zhu 537, Lyle, Stanek, and/or Jol to include such a feature. Each of Park, Kim 030, Kobayashi, Lida 327, Lida 337, Yoshida, Kim 417, Butcher, Amchislavsky, Nakajima, Zhu 537, Lyle, Stanek, and Jol disclose the transmission of AV data and bidirectional other data (including USB data) over one or more channels of a multimedia link. At least Zhu 537, Lyle, Stanek, and Jol explicitly disclose that AV data and bidirectional other data (including USB data) can be sent and received on the same channel at different times. As evident in the claim charts attached as Exhibits H, these references and others repeatedly emphasize that the principles of operation described in connection with one protocol or standard (e.g. DisplayPort, HDMI, DVI, MHL, USB) are applicable to other protocols and standards.

A POSITA would have been further motivated to combine Zhu 537, Park, Kim 030, Lyle, Butcher, Candalore, Anchislavsky, Lida 337, Lida 327, Yoshida, Nakajima, Jol, and/or Kim 417, either alone or in combination with other art, with Kobayashi. These references all disclose similar systems that solve the same problems (e.g. bidirectional transmission of USB data and unidirectional transmission of AV data in a multimedia link) in similar ways. Moreover, at least Zhu 537, Park, and DisplayPort 1.2 all relate to the DisplayPort standards. Zhu 537, Park, and DisplayPort 1.2 explicitly reference the DisplayPort standard. Although Kobayashi does not reference the DisplayPort standards explicitly, it was filed less than a year after the release of DisplayPort, version 1.0 and includes language and figures that seemingly reference DisplayPort concepts. *Compare, e.g.,* Kobayashi at Fig. 12 (discussing bidirectional "Aux. Ch." and unidirectional "Main Link") to DisplayPort, version 1.0 at Figure 1.2 (discussing bidirectional "AUX CH" and unidirectional "Main Link"); *see also* Kobayashi at [0071] (discussing "link training"). More fundamentally, Kobayashi explicitly discusses a multimedia interface for

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 207

audio/visual data. And although Kim 030 does not reference DisplayPort, as discussed below a POSITA would have found it obvious to combine a reference describing the transmission of data in connection with a HDMI standard (such as Kim 030) with a reference describing the transmission of data in connection with a DisplayPort standard (such as Kobayashi).

Moreover, as explained in further detail below, a POSITA would have been motivated and found it obvious to combine any one or more AV Link Plus Data References with any one or more AV Protocol and/or any one or more Sync Signal Reference.

The AV Link Plus Data References describe the transmission of non-AV data (including, for example, USB data) over a multimedia channel, link, or cable for transmission of AV data. The AV Link Plus Data References include at least the following:

- Zhu 537
- Park
- Lyle
- Kim 030
- Kim 417
- Lida 327
- Lida 337
- Kobayashi
- Yoshida
- Nakajima
- Butcher
- Amchislavsky
- Jol

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 208

- Stanek

Several AV link technologies were known at the time of the ’103 patent. For example, at least the following AV Protocols were known at the time:

- DisplayPort (including, for example, DisplayPort 1.2)
- Digital Video Interface (DVI) (including, for example, DVI 1.0)
- High-Definition Multimedia Intervace (HDMI) (including, for example, HDMI 1.3a)
- Mobile High-Definition Link (MHL) (including, for example, MHL Versions 1.0, 2.0, and 3.0)
- Whitby-Strevens

The ’103 Patent describes adding bidirectional USB data transmission over an MHL multimedia link (although the claims may not be limited to the MHL specification, specifically). Prior to the ’103 Patent, several references described adding the capability for bidirectional USB data transmission over a multimedia channel of an AV link in other known protocols at the time. For example, as discussed above, Zhu 537 and Park described bidirectional USB data transmission over the DisplayPort 1.2 main link. Lyle described bidirectional transmission of auxiliary data including, for example, USB data over a “video data transmission channel” in a DVI AV link. Kim 030 described bidirectional USB data transmission over a modified HDMI cable. Lida 327, Lida 337, Kim 417, and Kobayashi all disclose bidirectional data transmission (including, for example, USB data) over generic multimedia AV links.

A POSITA would have been motivated and found it obvious to combine any one or more AV Link Plus Data References with at least any one or more references describing the AV Protocol explicitly referenced in such AV Link Plus Data Reference (and any related AV Protocol, such as

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 209

an earlier or later version from the same protocol family). In addition to the motivations discussed above, such motivation would come from the teachings of the AV Link Plus Data Reference itself. For example, a POSITA would have been motivated and found it obvious to make any of the following exemplary combinations:

- Zhu 537 combined with DisplayPort 1.2 (or DisplayPort System)
- Zhu 537 combined with Whitby-Strevens
- Park combined with DisplayPort 1.2 (or DisplayPort System)
- Park combined with Whitby-Strevens
- Lyle combined with DVI 1.0
- Kim 030 combined with HDMI 1.3a
- Yoshida combined with HDMI 1.3a
- Nakajima combined with HDMI 1.3a
- Butcher combined with HDMI 1.3a
- Amchislavsky with MHL
- Jol with HDMI 1.3a
- Jol with DisplayPort 1.2 (or DisplayPort System)
- Stanek with HDMI 1.3a
- Stanek with DVI 1.0

Moreover, a POSITA would have been motivated and found it obvious to combine any one or more AV Link Plus Data References with any AV Protocol. Both the ’103 Patent and the prior art teach that the principles relevant to the alleged invention of the ’103 Patent can be applied across different AV Protocols. *See, e.g.,* ’103 Patent at 3:53-59 (“[T]he same principle can be applied to other standards such as High-Definition Multimedia Interface (HDMI) standard, a

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 210

Digital Visual Interface (DVI) standard, and a DisplayPort standard."); Zhu 537 at 20:58 – 21:5 ("Media connector 124 may be compatible with other media or multimedia standards besides DisplayPort such as but not limited to a Digital Video Interactive (DVI) or a high definition multimedia interface (HDMI) standard."); Lida 327 at 7:38-44 (discussing DVI, HDMI, DisplayPort, and DIVA standards); Lida 337 at 3:1-4 (discussing HDMI, DVI, UDI, and DisplayPort); and Butcher at [0029] (discussing HDMI, DisplayPort, and SCSI). For example, a POSITA would have been motivated and found it obvious to make any of the following combinations:

- Zhu 537 combined with DVI 1.0 or HDMI 1.3a
- Park combined with DVI 1.0 or HDMI 1.3a
- Lyle combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-Strevens) or HDMI 1.3a
- Kim 030 combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-Strevens) or DVI 1.0
- Yoshida combined with DisplayPort 1.2 (or DisplayPort System and/or Whitby-Strevens) or DVI 1.0
- Any of Lyle 327, Lyle 337, Kim 417, Nakajima, Butcher, and/or Kobayashi combined with any of DVI 1.0, HDMI 1.3a, DisplayPort 1.2, Whitby-Strevens, and/or DisplayPort System

A POSITA would also have been motivated and found it obvious to combine any one or more AV Link Plus Data References with any AV Protocol, alone or in combination with any one or more AV Protocol, with one or more references teaching synchronization signals ("Sync Signal References"). As evident from the teachings of the Sync Signal References themselves, the use of

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 211

synchronization signals was a well-known feature in data communication generally (and in the communication of USB data and AV data, specifically). A POSITA would therefore understand the benefits and uses of synchronization signals as described in the Sync Signal References. The Sync Signal References include at least the following references, which describe the transmission of one or more synchronization signals over an AV and/or non-AV data link, as well as any reference the claim chart for which cites disclosure from the reference in connection with, for example, claims 2, 3, 12, 13, and/or 17 of the '103 patent:

- '798 Patent
- Each of the AV Protocols (including, for example, DisplayPort 1.2, HDMI 1.3a, DVI 1.0)
- USB 2.0
- Kobayashi
- Hwang
- Munich
- Kim 417
- Franaszek
- Zhu 537
- Lyle
- Park
- Kim 030
- Lida 337
- Whitby-Strevens
- Wang 445

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 212

- Bradshaw
- The prior art to the ’798 Patent identified in Section V.A above.

The AV Protocols and most (if not all) of the AV Link Plus Data References also discuss the need for synchronization and the use of synchronization signals. Synchronization and synchronization signals were well-known concepts in the relevant art of data communication going back at least 30+ years before the filing of the ’103 patent. *See, e.g.,* Franaszek. Indeed, the predecessor to the original assignee of the ’103 patent, Silicon Image, described such synchronization signals in at least the prior art ’798 patent. A POSITA would therefore have been motivated to combine any AV Link Plus Data Reference or any combination of one or more AV Link Plus Data References with one or more AV Protocols (including the exemplary combinations listed above) with any one or more Sync Signal References.

A POSITA would have been further motivated to combine any reference discussing any AV Protocol with any reference discussing any other AV Protocol. Both the ’103 Patent and the prior art teach that the principles relevant to the alleged invention of the ’103 Patent can be applied across AV Protocols. *See, e.g.,* ’103 Patent at 3:53-59 (“[T]he same principle can be applied to other standards such as High-Definition Multimedia Interface (HDMI) standard, a Digital Visual Interface (DVI) standard, and a DisplayPort standard.”); Zhu 537 at 20:58 – 21:5 (“Media connector 124 may be compatible with other media or multimedia standards besides DisplayPort such as but not limited to a Digital Video Interactive (DVI) or a high definition multimedia interface (HDMI) standard.”); Lida 327 at 7:38-44 (discussing DVI, HDMI, DisplayPort, and DIVA standards); Lida 337 at 3:1-4 (discussing HDMI, DVI, UDI, and DisplayPort); and Butcher at [0029] (discussing HDMI, DisplayPort, and SCSI). Thus, a POSITA would have found it obvious to, and been motivated to, apply teachings regarding the communication of AV data, other

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 213

data, and control signals in a reference discussing one AV Protocol to any reference discussing any other AV Protocol.

For at least those same reasons, a POSITA would have been motivated to modify any reference teaching a multimedia link, including but not limited to any AV Protocol or any patent or publication related thereto, to include the capability for bidirectional communication of USB data on a physical channel, link, or cable used for transmission of AV data, as taught in at least AV Link Plus Data References, including by providing for a (or modifying a preexisting) transmitter, receiver, and/or transceiver on the AV data channel capable of transmitting and receiving USB data.

A POSITA would also have been motivated to combine any reference or combination of references relating to DisplayPort (or another non-TMDS video communication protocol) with an adapter that converts between DisplayPort and a TMDS protocol. Such adapters are taught, for example, in Wu 905 and TI SN75DP129. Motivation for such a combination can be found, for example, in the teachings of Wu 905, which discusses the value of and need for such adapters. *See* Wu 905 at 1:32 – 2:13.

Thus, in addition to the combinations discussed above, at least the following exemplary combinations render obvious some or all of the ’103 Asserted Claims:

- Zhu 537, alone or in combination with DisplayPort 1.2
- Zhu 537, alone or in combination with Whitby-Strevens
- Zhu 537, alone or in combination with DisplayPort System
- Zhu 537, alone or in combination with Kobayashi
- Zhu 537 in combination with Wu 905

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 214

- Zhu 537, alone or in combination with DisplayPort 1.2, in further combination with Wu 905, ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Zhu 537, alone or in combination with Whitby-Strevens, in further combination with Wu 905,’798 Patent, Kobayashi, Munich, Wang, and/or Franaszek
- Zhu 537, alone or in combination with DisplayPort System, in further combination with Wu 905, ’798 Patent, Kobayashi, Munich, Wang, and/or Franaszek
- Zhu 537, alone or in combination with Kobayashi, in further combination with Wu 905, ’798 Patent, Munich, Wang, and/or Franaszek
- Park, alone or in combination with DisplayPort 1.2
- Park, alone or in combination with Whitby-Strevens
- Park, alone or in combination with DisplayPort System
- Park, alone or in combination with Kobayashi
- Park in combination with Wu 905
- Park, alone or in combination with DisplayPort 1.2, in further combination with Wu 905, ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Park, alone or in combination with Whitby-Strevens, in further combination with Wu 905, ’798 Patent, Kobayashi, Munich, Wang, and/or Franaszek
- Park, alone or in combination with DisplayPort System, in further combination with Wu 905, ’798 Patent, Kobayashi, Munich, Wang, and/or Franaszek
- Park, alone or in combination with Kobayashi, in further combination with Wu 905, ’798 Patent, Munich, Wang, and/or Franaszek

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 215

- Lyle, alone or in combination with DVI 1.0
- Lyle, alone or in combination with DVI 1.0, in further combination with ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Lyle, alone or in combination with HDMI 1.3a
- Lyle, alone or in combination with HDMI 1.3a, in further combination with ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Kim 030, alone or in combination with HDMI 1.3a
- Kim 030, alone or in combination with HDMI 1.3a, in further combination with ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Yoshida, alone or in combination with HDMI 1.3a
- Yoshida, alone or in combination with HDMI 1.3a, in further combination with ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Jol, alone or in combination with HDMI 1.3a, USB 2.0, and/or DisplayPort 1.2
- Jol, alone or in combination with HDMI 1.3a, in further combination with USB 2.0, ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Jol, alone or in combination with DisplayPort 1.2 (or DisplayPort System), in further combination with Wu 905, USB 2.0, ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Amchislavsky, alone or in combination with MHL
- Butcher, alone or in combination with HDMI 1.3a
- Butcher, alone or in combination with HDMI 1.3a, in further combination with USB 2.0, ’798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 216

- Nakajima, alone or in combination with HDMI 1.3a
- Nakajima, alone or in combination with HDMI 1.3a, in further combination with USB 2.0, '798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens
- Stanek, alone or in combination with HDMI 1.3a
- Stanek, alone or in combination with HDMI 1.3a, in further combination with USB 2.0, '798 Patent, Kobayashi, Franaszek, Munich, Wang, and/or Whitby-Strevens

A POSITA would also have been motivated to combine the teachings of USB 2.0 with those of USB Video Class and/or USB OTG. Both USB Video Class and USB OTG explicitly refer to and expand upon USB 2.0. In fact, USB OTG is a supplement to USB 2.0. A POSITA would understand that these specifications are related and intended to interoperate, and that both USB Video Class and USB OTG describe additional features that may be used in conjunction with USB 2.0 and/or potential modifications to USB 2.0. Similarly, a POSITA would have been motivated to combine and/or modify the teachings of USB 2.0, USB Video Class, and/or USB OTG in view of Zhu 977, which explicitly cites (and describes, in detail, the operation of) USB OTG.

For purposes of illustration, the claim charts attached as Exhibits H-32 through H-36 demonstrate the collective disclosures of some exemplary combinations from the list above. Defendant's contentions on obviousness are not limited to those exemplary combinations, however. Defendant contends that for each combination discussed above, a POSITA would have been motivated (and known how) to combine the respective disclosures of each reference in the combination to obtain the claimed inventions of the '103 Asserted Claims.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 217

B. Invalidity of the ’103 Patent Based on 35 U.S.C. § 112(a) (Enablement and Written Description)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the claims of the ’103 Patent, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that one or more of the ’103 Asserted Claims are invalid for failure to provide a written description that enables the full scope of the ’103 Asserted Claims based on at least the following claim terms, phrases, or limitations:

- “aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal” (claim 17)

Based on Defendant’s present understanding of Plaintiff’s Infringement Contentions and apparent interpretation of the scope of the Asserted Claims, at least one or more of these claim terms, phrases, and limitations are not described in the specification of the Asserted Patent and do not enable a person of ordinary skill in the art to practice the claimed invention without undue experimentation or to distinguish all operative embodiments from all nonoperative embodiments without undue experimentation.

The written description and enablement issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

C. Invalidity of the ’103 Patent Based on 35 U.S.C. § 112(b) (Indefiniteness)

Based on Defendant’s present understanding of Plaintiff’s asserted scope of the ’103 Asserted Claims, to the extent such positions can be understood from Plaintiff’s Infringement Contentions, Defendant asserts that one or more of the ’103 Asserted Claims are invalid for reciting at least the following claim terms, phrases, or limitations:

- “The method of claim 11, further comprising aligning a boundary of a symbol in a first forward unit of data of the forward units of data using the first synchronization signal” (claim 17)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 218

These claim terms, phrases, limitations, and all dependent claims thereof, as apparently construed by Plaintiff, violate the definiteness requirements of 35 U.S.C. § 112 at least because they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

Based on Defendant's present understanding of Plaintiff's Infringement Contentions, at least one or more of these claim terms, phrases, and limitations are indefinite because they are inconsistent with and broader than the alleged invention disclosed in the specification and during prosecution, and given Plaintiff's apparent constructions of the claims, a person of ordinary skill in the art at the time of the invention would not understand what is claimed with reasonable certainty, even when the claims are read in light of the specification and prosecution history.

Additionally, Claims 21 and 22 of the '103 Patent are invalid under 35 U.S.C. §§ 112(b) and (f) because the '103 Patent does not disclose sufficient structure corresponding to the function recited in at least the following means-plus-function claim limitations:

- "a transmitter coupled to a first physical channel of the multimedia link and configured to send forward units of data from the source device to the sink device over the first physical channel during one or more first time periods, the forward units of data comprising video data and forward data compliant with a first standard comprising a universal serial bus (USB) standard and different from a standard of the video data" (claims 21 and 22)
- "a receiver coupled to the first physical channel and configured to receive backward units of data at the source device from the sink device over the first physical channel during one or more second time periods, the backward units of data comprising backward data compliant with the first standard" (claims 21 and 22)
- "a control signal transceiver coupled to a second physical channel of the multimedia link distinct from the first physical channel and configured to at least send control data from the source device to the sink device over the second physical channel" (claims 21 and 22)

The indefiniteness issues identified above apply to all claims that include the identified limitations, either explicitly or through claim dependency, and are not limited to the exemplary claims listed above.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 219

XI. UNENFORCEABILITY

Defendant reserves the right to assert, after obtaining discovery from the inventors and prosecuting attorneys, that the remaining Asserted Patents are unenforceable due to inequitable conduct at least on the grounds that material prior art, including but not limited to any of the references identified herein, were known to the applicants or their attorney(s), material and withheld with an intent to deceive the Patent Office.

Defendant also hereby incorporates by reference any allegation of unenforceability raised by any other Defendant in any Answer or Counterclaim filed in any case involving an Asserted Patent.

XII. SUBJECT-MATTER ELIGIBILITY CONTENTIONS

Pursuant to the Court's Standing Order Regarding Subject Matter Eligibility Contentions, Defendant hereby provides the bases for its contention that all Asserted Claims are patent ineligible and therefore invalid under 35 U.S.C. § 101.

Section 101 "defines the subject matter that may be patented under the Patent Act." *Bilski v. Kappos*, 561 U.S. 593, 601 (2010). Under § 101, the scope of patentable subject matter encompasses "any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof." *Id.* (quoting 35 U.S.C. § 101). These categories are not limitless, as § 101 contains three important exceptions—abstract ideas, laws of nature, and natural phenomena are not patentable. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 134 S. Ct. 2347, 2354 (2014). The determination of whether a claim recites patent-eligible subject matter under § 101 is guided by the two-step analytical framework set forth in *Alice*, *id.* at 2355. The first step requires determining whether the claims are directed to one of these three exceptions. *Id.* If so, the second step requires determining whether the claim elements, considered individually and as an ordered combination, "amount to significantly more" than the patent-ineligible concept. *Id.*

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 220

The first step is to examine the fundamental concept, or the "focus" of the claim and determine whether the claim as a whole is directed to an abstract idea, law of nature, and natural phenomenon. *See Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1346 (Fed. Cir. 2015) ("Under step one of Mayo/Alice, the claims are considered in their entirety to ascertain whether their character as a whole is directed to excluded subject matter."). While courts should be careful not to oversimplify the claims at this stage of the analysis, the analysis should not focus on excess verbiage or implementation details, but instead focus on the "concept embodied by the majority of the limitations." *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 715 (Fed. Cir. 2014); *see also Affinity Labs of Texas, LLC v. DirecTV, LLC*, 838 F.3d 1253, 1256 (Fed. Cir. 2016) (examining claim after being "stripped of excess verbiage"). Transformation into a patent-eligible claim requires "more than simply … adding the words 'apply it.'" *Id.* (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc., 132 S. Ct. 1289, 1294 (2012))*. Also, a claim is not meaningfully limited if it includes only token or insignificant pre- or post-solution activity—such as merely identifying a technological environment. *Mayo*, 132 S. Ct. at 1297–98, 1300–01. Finally, "simply appending conventional steps, specified at a high level of generality," to abstract ideas cannot make those ideas patentable. *Mayo*, 132 S. Ct. at 1300; *see also Fort Props., Inc. v. Am. Master Lease LLC*, 671 F.3d 1317, 1323 (Fed. Cir. 2012) ("Such a broad and general limitation does not impose meaningful limits on the claim's scope.").

With respect to abstract ideas, the Federal Circuit has clarified that a relevant inquiry at step one is to "ask whether the claims are directed to a specific improvement in the capabilities of computing devices, or, instead, 'a process that qualifies as an 'abstract idea' for which computers are invoked merely as a tool.'" *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 880 F.3d 1356, 1361-62 (Fed. Cir. 2018) (quoting *Enfish, LLC*, 822 F.3d at 1336). In *Core Wireless Licensing*, the

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 221

Federal Circuit noted that in *Enfish*, "unlike claims that merely 'add[ ] conventional computer components to well-known business practices,' the claimed self-referential table was 'a specific type of data structure designed to improve the way a computer stores and retrieves data in memory.'" *Id.* (quoting *Enfish*, 822 F.3d at 1338–39) (underlining added). The Federal Circuit further emphasized that claims directed to the improvement in the functioning of a computer must teach a specific and new method that enables a computer "to do things it could not do before." *Id.* For example, in *Finjan, Inc. v. Blue Coat Systems, Inc.*, the Federal Circuit "held claims directed to a behavior-based virus scanning method directed to patent eligible subject matter because they 'employ[ ] a new kind of file that enables a computer security system to do things it could not do before, ...'" *Id.* (citing *Finjan, Inc. v. Blue Coat Sys., Inc.*, 879 F.3d 1299 (Fed. Cir. 2018)).

With respect to laws of nature and natural phenomenon, the Federal Circuit has held that claims focused on detecting natural laws or phenomenon—even if new and useful—are patent-ineligible. *See, e.g.*, *Cleveland Clinic Found. v. True Health Diagnostics LLC*, 859 F.3d 1352, 1363 (Fed. Cir. 2017); *Ariosa Diagnostics, Inc. v. Sequenom, Inc*., 788 F.3d 1371, 1378 (Fed. Cir. 2015). For instance, in *Cleveland Clinic*, the claims recited a particular assay used to detect the protein MPO. 859 F.3d at 1357-58. In *Ariosa*, the claims recited a technique to amplify and detect DNA. 788 F.3d at 1377. The Federal Circuit emphasized that "the claims at issue, as informed by the specification, are generally directed to detecting the presence of a naturally occurring thing or a natural phenomenon" and amounted to nothing "more than simply stat[ing] the law of nature while adding the words 'apply it.'" *Id*. at 1376-77 (internal citations omitted).

The Asserted Patents are not patent eligible under § 101.

'905 Patent. The Asserted Claims of the '905 Patent are invalid under 35 U.S.C. § 101 because they are directed to ineligible subject matter. *See* Ex. A-7. In particular, under *Alice* Step

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 222

1, the ’905 Asserted Claims recite nothing more than the abstract idea of transmitting and/orreceiving packets. Specifically, the claims generically recite a technique for “transmitting packets,” or “receiving packets” such as the claimed “first packet” and “second packet;” transmitting or receiving indicators associated with the packets, such as the “preempt indicator” and the “continue indicator;” and using in-band symbols and out-of-band symbols. Such receiving and transmitting fail *Alice* Step 1. *See, e.g.*, *Prism Techs. LLC v. T-Mobile USA, Inc.*, 696 F. App’x 1014, 1017 (Fed. Cir. 2017) (generally finding claims to, *inter alia*, coordinating communication between transmitters to “provide restricted access” as ineligible under Section 101).

The ’905 Asserted Claims further fail *Alice* Step 2 because they do not contain any inventive concept that would transform the abstract idea into a patent-eligible invention. Rather, the claims recite purely function limitations with no structural elements at all (*e.g.*, claims 1, 8, and 15) or recite generic “components” combined in conventional ways to perform generic functions (*e.g.*, claim 21 reciting a “transmission component” for “transmitting the first packet”). *See Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 715-16 (Fed. Cir. 2014). Implementing an abstract idea using functional limitations or generic computer components does not constitute a patentable improvement in computer technology. *See Two-Way Media Ltd. v. Comcast Cable Commc’ns, LLC*, 874 F.3d 1329, 1337 (Fed. Cir. 2017). Further, the inclusion of well-known “in-band” or “out-of-band” symbols fails to produce “a result that overrides the routine and conventional” use of this known feature. *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245, 1258 (Fed. Cir. 2014). Instead, the use of “in-band” and “out-of-band” symbols is a conventional, well-known process for transmitting data, as shown by the accompanying prior art. Accordingly, the ’905 Asserted Claims fail *Alice* Step 2 because they do not contain any inventive concept that would transform the abstract idea into patent-eligible subject matter.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 223

’712 Patent. The Asserted Claims of the ’712 Patent are invalid under 35 U.S.C. § 101 because they are directed to ineligible subject matter. In particular, under *Alice* Step 1, the ’712 Asserted Claims recite nothing more than the abstract idea of delivering power to a device communicating that it is in need of power. Specifically, claim 1 recites a power delivery circuit for delivering power to a device, the circuit including a voltage source, a switch to convey voltage from the voltage source when closed, a signature resistor for detection, and a load detector for extracting information based on a device’s current, where the information includes whether the device is on, and whether it needs power. Independent claim 7 is even broader and claims a method of delivering power to a device, the method including detecting a load in the device, extracting information based on the load current, and relaying power based on that information, where the information includes whether the device is on, and whether it needs power. Such claims are plainly directed to an abstract idea and fail *Alice* step 1. *See, e.g., ChargePoint, Inc. v. SemaConnect, Inc*., 920 F.3d 759, 770 (Fed. Cir. 2019) (finding ineligible under § 101 claims directed to (a) an apparatus for charging an electric vehicle that receives communications from a remote server and adjusts charging based on those communications; and (b) a “network-controlled charge transfer system for electric vehicles” comprising a combination of generic components, including a charge transfer device, an electrical receptacle, a control device for switching the receptacle on and off, a current measuring device for measuring current through the receptacle, and a controller for monitoring output of the current measuring device and controlling the control device).

The ’712 Asserted Claims also fail *Alice* step 2 because they do not contain an inventive concept that would transform the abstract idea into a patent-eligible application. Instead, the claims either recite routine functional limitations with no structural elements (i.e., claims 7 and 9), or recite generic components combined in conventional ways (e.g., claim 1 reciting a voltage source,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 224

a power relay switch, a resistor, and a load detector). *Alice*, 573 U.S. at 223 ("the mere recitation of a generic computer cannot transform a patent-ineligible abstract idea into a patent-eligible invention"); *WhitServe LLC v. Dropbox, Inc*., 854 F. App'x 367, 372 (Fed. Cir. 2021) (finding claims reciting "generic computer components performing routine conventional functions" such as "sending and receiving information" not eligible under § 101). As the prior art cited and discussed in these contentions and the attached claim charts demonstrates, the concepts and components recited in the '712 Asserted Claims were all routine, conventional, and well-known at the time of invention. For example, the use of a current sensor and a signature resistor to determine a connected device's power requirements was well known in the art and widely used in PoE devices. Thus, at most, the '712 Asserted Claims merely recite an "abstract-idea-based solution implemented with generic technical components in a conventional way." *ChargePoint*, 920 F.3d at 775. Accordingly, the '712 Asserted Claims are invalid under § 101.

'103 Patent. The '103 Asserted Claims are directed to ineligible subject matter under 35 U.S.C. § 101. In particular, under *Alice* Step 1, the '103 Asserted Claims are directed to the abstract idea of transmitting and receiving two different types of data on one physical channel and control signals on a separate physical channel. *See, e.g., Hawk Tech. Sys., LLC v. Castle Retail, LLC*, 60 F.4th 1349 (Fed. Cir. 2023) (finding claims to receiving, transmitting, processing, storing, and displaying image data ineligible under Section 101). The patent ineligible nature of the '103 Asserted Claims is even more evident under the extremely broad construction applied by UCT in its infringement contentions. UCT reads the '103 Asserted Claims onto an implementation of DisplayPort tunneling over USB4. Such a read necessarily assumes broad constructions. For example, UCT interprets its claims so that they are not limited specifically to an audio/visual "multimedia link," but would apply also to a USB link and that they do not require a single bi-

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 225

directional, half-duplex first physical channel with time-division multiplexing or TMDS coding. The omission of these potential limitations exacerbates the fundamentally abstract nature of the '103 Asserted Claims.

The other elements of the claim do not contain any inventive concept that would transform the abstract idea into a patent-eligible invention under *Alice* Step 2. For example, as demonstrated in the contentions and claim charts for the '103 Patent, the limitations requiring a "multimedia link," "forward data compliant with . . . a universal serial bus (USB) standard," "video data" corresponding to "a standard of the video data," the first and second "synchronization signals," and the recited generic hardware (see below) are all conventional and, at most, attempt to limit the abstract idea to a particular technological environment, which is insufficient to convert the abstract idea into an inventive concept. *Alice Corp. v. CLS Bank Int'l*, 134 S.Ct. 2347, 2358 (2014). Further, the limitations "forward data compliant with . . . a universal serial bus (USB) standard" and "video data" corresponding to "a standard of the video data" recite printed matter, which is not patent-eligible subject matter and thus cannot transform the abstract concept into an eligible invention. Moreover, the recited hardware structures (including, for example, "source device," "sink device," "multimedia link," "physical channel," "transmitter," "receiver," and "transceiver") are all generic and functional. As the prior art cited and discussed in these contentions and the attached claim charts demonstrates, these concepts were all routine, conventional, and well-known at the time of invention.

When these conventional elements are assembled together in the Asserted Claims, they do not take on any transformative property that, considered as a whole, reflects an inventive concept. Instead, the conventional elements of the claim are used in an entirely conventional manner. For instance, the claims combine known data types (such as A/V data, USB data, and control signals)

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 226

and conventional data communication components (such as receivers, transmitters, transceivers, physical channels) and concepts (such as synchronization signals and time-division multiplexing for half-duplex communication) in predictable and conventional ways using known techniques. These components are also used for their conventional purposes—i.e., transmitting and receiving data between devices. These elements were well known in the art, and the Asserted Patents do no more than use the appropriate technique for their conventionally intended purpose.

Moreover, the prior art cited throughout Defendant's Invalidity and Eligibility Contentions (including the claim charts attached as Exhibits hereto), as well as the patents themselves and the prior art cited or admitted to therein, demonstrate that the claim elements are directed to well-understood, routine, and conventional techniques and components. Accordingly, the '103 Asserted Claims are invalid under § 101.

Additionally, at least claim 22 of the '103 Patent is directed to ineligible subject matter under Section 101 for the additional reason that it is directed to the abstract idea of a "digital design of a circuit." '103 Patent at claim 22 (preamble). The claim limitations thus recite printed matter – that is, the informational content of the "instructions" that make up the "digital design." Such limitations are not patentable subject matter and instead are more properly the subject of other intellectual property protections such as copyright.

Charts providing the information required by the Standing Order Regarding Subject Matter Eligibility are attached hereto as Exhibits A-7 , E-20, and H-38.

These Invalidity and Eligibility Contentions address only those claims that Plaintiff has asserted in its Infringement Contentions against Defendant. Defendant incorporates by reference any and all other subject matter eligibility contentions that have or will be served in this case or any other case brought by Plaintiff and/or involving the Asserted Patents. Defendant incorporates

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 227

by reference any and all other bases for invalidity identified during prosecution, reexamination, or any other proceeding before the United States Patent and Trademark Office regarding the Asserted Patents, or any other patents in the same family as any Asserted Patent.

XIII. DOCUMENT PRODUCTION

Pursuant to the Court's Patent Rules and Docket Control Order (Dkt. No. 27), Defendant is producing with these contentions (a) all prior art referenced in these contentions (DEFS_UCT_PA_00000001 – DEFS_UCT_PA_00016879) and (b) technical documents sufficient to show the operation of the accused products (LGL_UCT_00000001 – LGL_UCT_00059319).

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 228

Dated: July 24, 2024

Respectfully Submitted,

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Universal Connectivity Technologies Inc.
Ex. 2005 - Page 229

CERTIFICATE OF SERVICE

The undersigned certifies that a true and correct copy of the above and foregoing document has been served on July 24, 2024 to all counsel of record via electronic mail.

/s/ Debbie Kakanas

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 230

Exhibit B-7

Invalidity of the ’307 Patent in View of U.S. Patent application 2002/0159450 to Shin et al. (Shin ‘450)

This chart provides examples of where the prior art reference discloses, either expressly or inherently, the claim elements of asserted U.S. Patent No. 7,187,307 (“the ‘307 patent”). The citations herein are exemplary and are not exhaustive; Defendant has cited the most relevant portions of the identified prior art. For each citation, Defendant hereby incorporates by reference the entire cited prior art reference, and reserves the right to rely on uncited portions of each identified prior art reference. To provide context or identify the state of the art at the time of the alleged invention, Defendant reserves the right to rely on: (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art); (4) factual testimony from the inventors or authors of the prior art references, or purveyors of prior art devices; and (5) expert testimony.

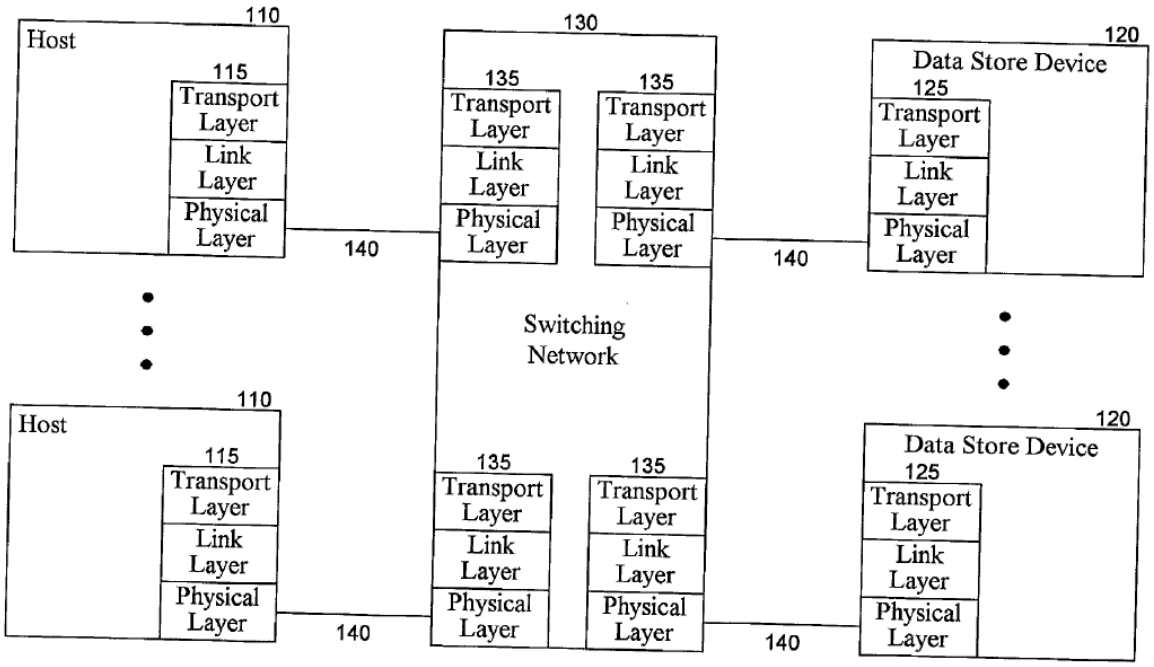
Where Defendant cites a figure, the citation includes any text associated with the figure. Where Defendant cites passages relating to a figure, the citation includes the associated figure any other text associated with that figure. Where Defendant cites particular prior art as disclosing a claim element, that citation equally applies to all identical or similar claim elements in this chart. Defendant reserves the right to further assert that a claim element is inherent, the element would have been obvious to a person of ordinary skill in the art, or the element is disclosed in other prior art that may be combined with the cited prior art. To establish the inherency of certain features of the prior art to invalidate the asserted claims, Defendant may rely on cited or uncited portions of the prior art, other documents, factual testimony, and expert testimony.

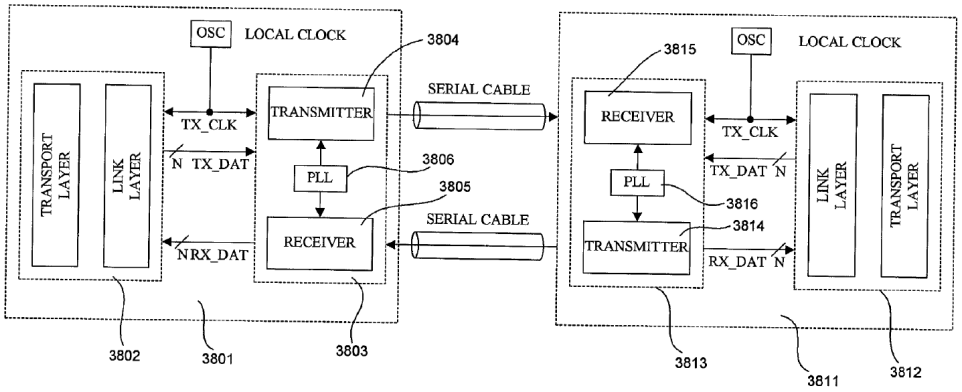
This invalidity chart is based on information presently available to Defendant, and the information herein is provided as a non-limiting example.

Shin ‘450 was filed on November 11, 2001, and published on October 31, 2002; therefore, Shin ‘450 is prior art under at least 35 U.S.C. § 102(e).

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 231

Claim Limitation		Shin '450
Claim 1		
1[p]	1. A communication system, including:	To the extent the preamble is limiting, Shin '450 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*: "A serial communications architecture for communicating between hosts and data store devices. The Storage Link architecture is specially adapted to support communications between multiple hosts and storage devices via a switch network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at Abstract. "In the following, aspects of the serial communications architecture are described using block diagrams and logic diagrams. One skilled in the art will appreciate that the serial communications architecture can be implemented using different combinations of logic circuits and/or firmware. In particular, the logic diagrams illustrate processing that may be performed in parallel using duplicate logic circuits (e.g., one for each communications link) or may be performed in serial using a single logic circuit. The particular logic designs can be tailored to meet the cost and performance objectives of the implementation of the serial communications architecture. One skilled in the art will be able to readily design logic circuits based on the following descriptions. 1. STORAGE LINKARCHITECTURE FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk

		drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer." Shin '450 at [0074-0076].  ***Fig. 1*** Shin '450 at Fig. 1.

		"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip." Shin '450 at [0164].  ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(a)	a first endpoint;	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "A serial communications architecture for communicating between hosts and data store devices. The Storage Link architecture is specially adapted to support communications between multiple

		hosts and storage devices via a switch network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at Abstract. "In the following, aspects of the serial communications architecture are described using block diagrams and logic diagrams. One skilled in the art will appreciate that the serial communications architecture can be implemented using different combinations of logic circuits and/or firmware. In particular, the logic diagrams illustrate processing that may be performed in parallel using duplicate logic circuits (e.g., one for each communications link) or may be performed in serial using a single logic circuit. The particular logic designs can be tailored to meet the cost and performance objectives of the implementation of the serial communications architecture. One skilled in the art will be able to readily design logic circuits based on the following descriptions. 1. STORAGE LINKARCHITECTURE FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer." Shin '450 at [0074-0076].

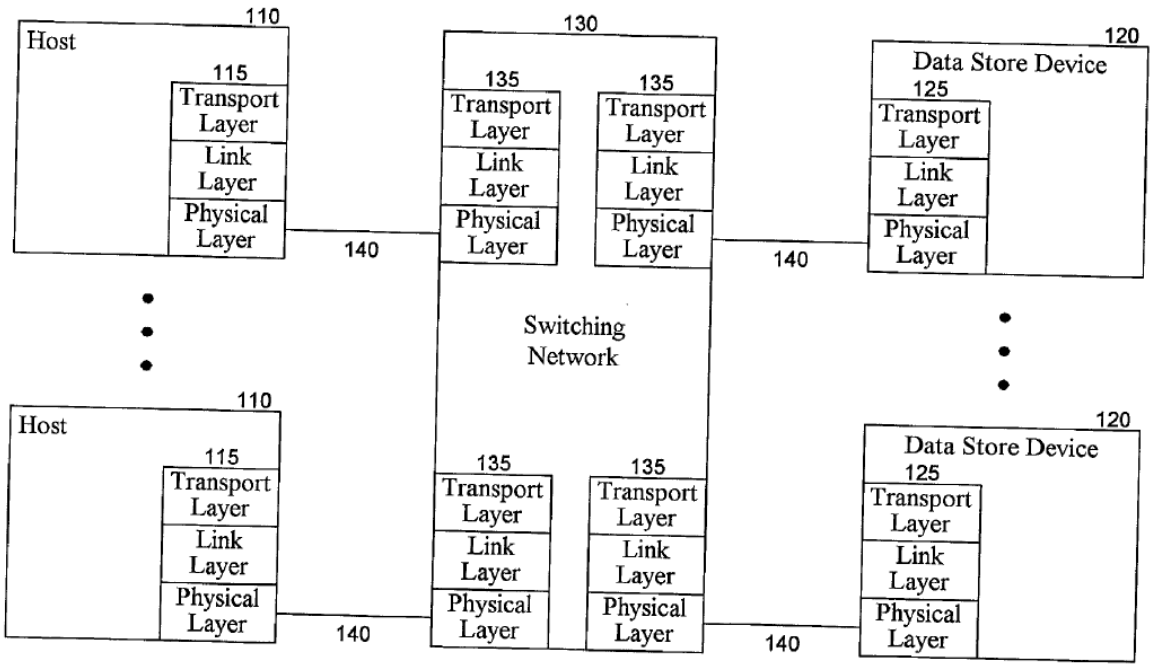


Fig. 1

Shin '450 at Fig. 1.

"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip."
Shin '450 at [0164].

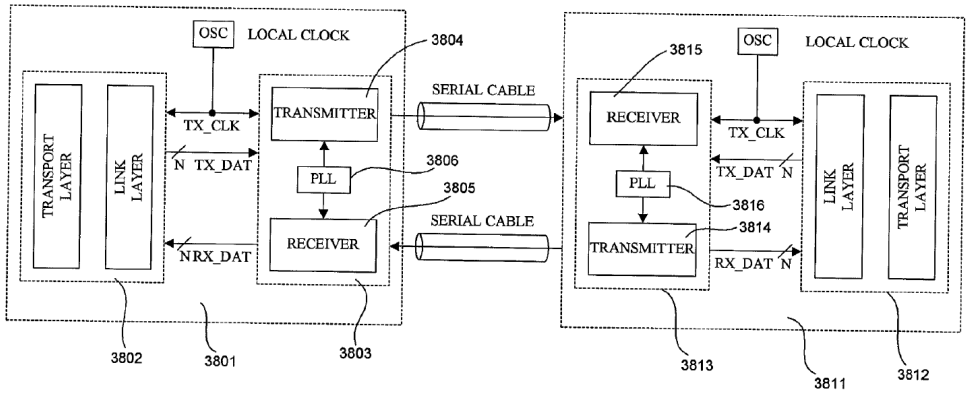


Fig. 38A

Shin ‘450 at Fig. 38A.

“FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers.”

Shin ‘450 at [0097].

		To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(b)	a second endpoint, including physical and link layer circuitry and higher level circuitry coupled to the physical and link layer circuitry; and	See exemplary disclosures and corresponding discussion for claim element 1[a]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(c)	a serial link between the first endpoint and the second endpoint,	See exemplary disclosures and corresponding discussion for claim element 1[a]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(d)	wherein the first endpoint is configured to generate encoded data in accordance with a line code, and to transmit the encoded data over the link to the second endpoint, and	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at [0071]. "FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk

		drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer. The hosts and data store devices have an upper layer that communicate to each other via transactions. When transmitting data, the upper layer provides the data for the transaction to the transport layer. The transport layer receives the data of the transaction and generates packets (i.e., packetizes the data) for transmission. The transport layer then provides each code (e.g., each byte) of the packets to the link layer for transmission to the destination. When receiving data, the transport layer receives the codes of transaction from the link layer and identifies the packets. The transport layer then combines the data of the packets of the transaction (i.e., depacketizes the data) and provides the data of the transaction to the upper layer. Each host and data store device may include an application upper layer that provides the data of a transaction to the transport layer to be transmitted to a destination and receives the data of a transaction from the transport layer that was transmitted by a source. Each packet includes a header section and a payload section. The header section identifies the source and destination and a packet type (e.g., data or command). Each switch may include a communications interface for each port of the switch. Each port may be connected to a serial communications link comprising a receive and transmit link. The switches and their interconnecting communications links form the switching network. The transport layer of a switch may not packetize and depacketize the data, rather it may direct packets received via one port to be transmitted via another port to affect the routing of the packets from the source to the destination as indicated in the header section. The link layer encodes the codes to be transmitted via its communications link into symbols and decodes symbols received via its communications link into codes. The link layer receives codes to be transmitted from the transport layer, encodes those codes into symbols, and provides those symbols to the physical layer. The link layer also receives symbols from the physical layer, decodes those symbols into codes, and provides those codes to the transport layer. The encoding may include mapping the codes to symbols to optimize bit transitions and to ensure DC-balance. The physical layer receives the symbols from the link layer, serializes the symbols, and transmits the serialized symbols via the communications link. The physical layer receives serialized

		symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. FIG. 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, Such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, Such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and Store the codes as packets in the receive memory. The link layer includes transmit components, such as an encoder 221, a data Selector 222, and a control Symbol generator 223, and receive components, Such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for receiving and identifying, control Symbols, Synchronization Symbols, timing Symbols, and So on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control Symbols and Synchronization Symbols. The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data. The data Selector Selects Symbols encoded from codes provided by the transport layer or Symbols generated by the control Symbol generator. The data Selector effectively inserts control Symbols and Synchronization Symbols into the Sequence of symbols that are to be transmitted. Various possible encoding techniques for the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate.

		The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the Serialized Symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode." Shin '450 at [0075-0081].

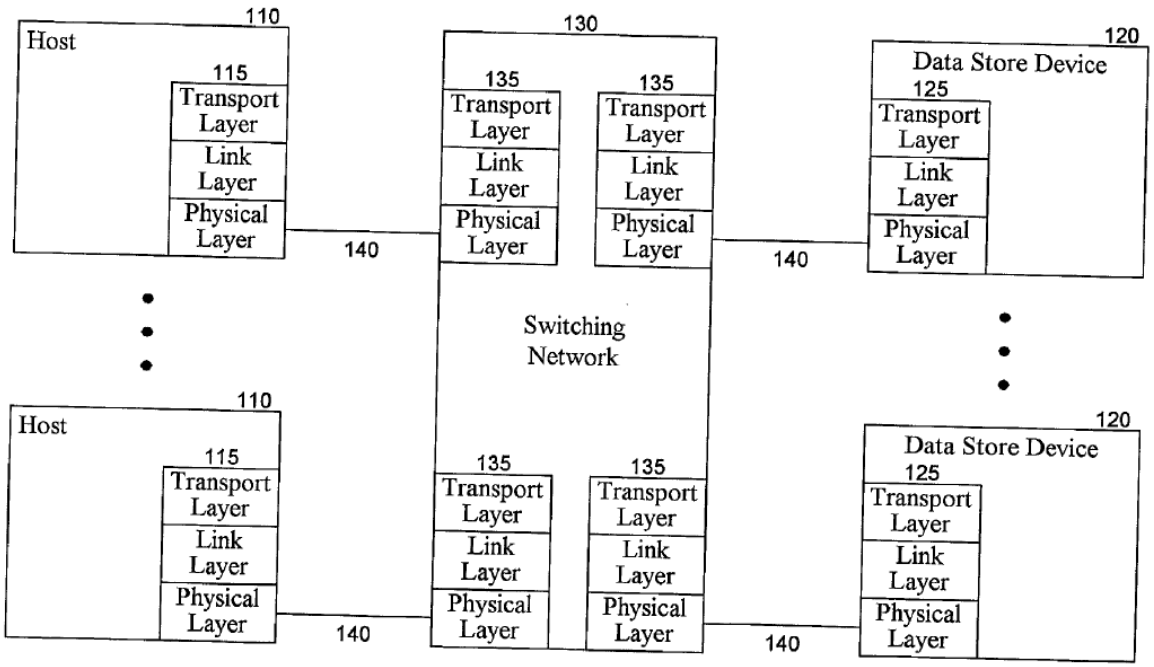


Fig. 1

Shin '450 at Fig. 1.

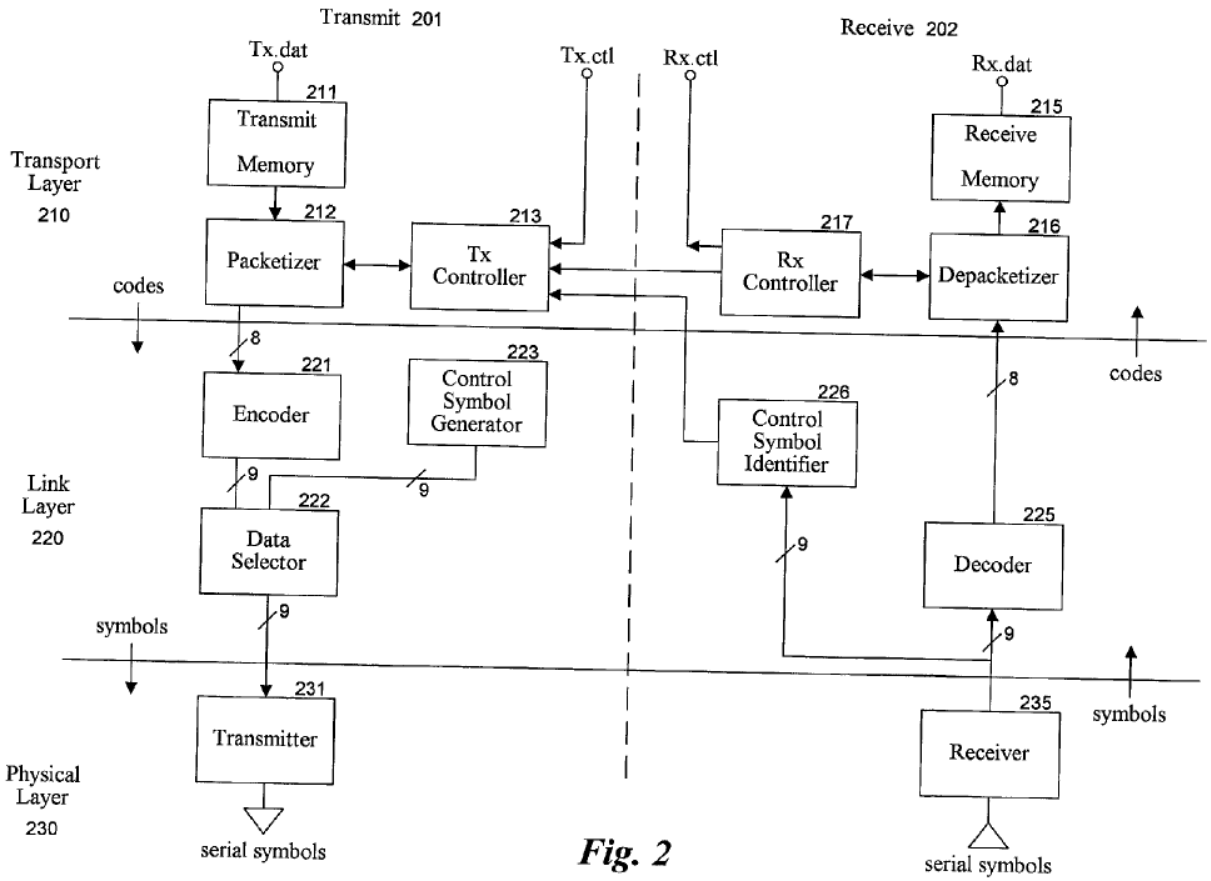
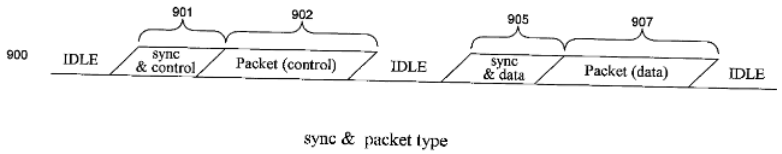
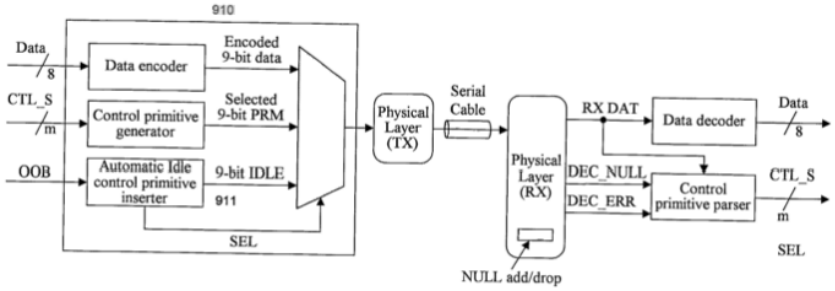


Fig. 2

Shin '450 at Fig. 2.

"FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not

		encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097].  *Fig. 9A* Shin '450 at Fig. 9A. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is

		Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105].  ***Fig. 9C*** Shin '450 at Fig. 9C. "In one embodiment, the link layer of a communications node encodes codes into symbols in order to optimize transition control and to ensure DC-balance. Transition control may be optimized to either maximize or minimize the number of transitions in symbols that are to be transmitted. A transition is defined as a bit value of 1 followed by a bit value of 0 or a bit value of 0 followed by a bit value of 1. When the number of transitions is maximized, clock information may be more accurately derived from the transmitted symbols. When the number of transitions is minimized, overall electromagnetic interference may be minimized. One skilled in the art will appreciate that the link layer may be designed to minimize or maximize transitions depending on the overall design objectives. In the following, the described encoding technique attempts to maximize the number of transitions in symbols to be transmitted. In an alternate embodiment, the

		transitions can be maximized at times and minimized at other times to balance the objectives of deriving a clock signal and reducing electromagnetic interference. The encoding technique in one embodiment encodes an 8-bit code based on the number of transitions in that code. The maximum possible number of transitions in an 8-bit code is seven and occurs when the bit values alternate between 0 and 1 (e.g., "10101010"). The minimum possible number of transitions in an 8-bit code is zero and occurs when all the bit values are the same (e.g., "11111111"). To maximize the number of transitions, the encoding technique inverts the bit value of alternate bits in each code with less than four transitions. This alternate bit inversion, also referred to as transition inversion, results in a code that previously had "n" transitions to now have |n- 7| transitions. For example, the result of alternate bit inversion of a code with zero transitions (e.g., "11111111") is a code with seven transitions (e.g., "01010101"), and the result of alternate bit inversion of the code with three transitions (e.g., "00010111") is a code with four transitions (e.g., "10111101"). The encoding technique adds a ninth bit (i.e., a transition inversion indicating bit) to the 8-bit code to indicate whether the alternate bits of the code were inverted, which results in a 9-bit symbol. For example, a bit value of 0 in the ninth bit indicates that the code did not have its alternate bits inverted, and a bit value of 1 in the ninth bit indicates that the code did have its alternate bits inverted. The symbol "010111101" has a bit value of 0 in its ninth bit, which indicates that alternate bits were not inverted. In contrast, the symbol "110111101" has a bit value of 1 in its ninth bit, which indicates that alternate bits were inverted. One skilled in the art will appreciate that the ninth bit can be stored at any bit position within the symbol. In this description, the ninth bit is represented as the most significant bit of the symbols. When a symbol is received at a communications node, the ninth bit is used to determine whether the symbol needs to have its alternate bits inverted to decode the symbol. Since the symbol "010111101" has a bit value of 0 in its ninth bit, its alternate bits were not inverted and the resulting decoded code is "10111101." Conversely, since the symbol "110111101" has a bit value of 1 in its ninth bit, its alternate bits were inverted and the resulting decoded code is "00010111." All the symbols generated by alternate bit inversion encoding are referred to as "in-band symbols" because they are 9-bit symbols with at least four transitions. All 9-bit symbols with three or less

		transitions are referred to as "out-of-band symbols." This alternate bit inversion encoding technique generates only in-band symbols. FIG. 20 illustrates an alternate bit inversion encoding technique in one embodiment. The left column represents the 8-bit codes, and the right column represents the 9-bit symbols. The alternate bit inversion encoding technique is referred to as an 8 b/9 b encoding, which is a more efficient encoding than standard 8 b/10 b encodings. Transition control encoding is described in U.S. Pat. No. 5,999,571, entitled "Transition-Controlled Digital Encoding and Signal Transmission System," which is hereby incorporated by reference. The encoding technique may also help ensure DC-balance by using selective block inversion encoding on symbols that have been transition optimized. Selective block inversion refers to an encoding technique that inverts certain bit values in a block of symbols to help ensure DC-balance is maintained. In one embodiment, selective block inversion may perform polarity inversion (i.e., inverting each bit of a symbol) on all but one symbol of a block to help ensure DC-balance and transition inversion on that one symbol in the block to indicate that the other symbols of the block have been polarity inverted. Although the encoding technique performs selective block inversion on blocks of four symbols, one skilled in the art will appreciate that a block can contain any number of symbols. Conventional encoding techniques, in contrast, typically process only one symbol at a time when attempting to ensure DC-balance. Because the selective block inversion encoding technique evaluates DC-balance over multiple symbols, DC-balance is more likely assured and there is essentially no bandwidth used to indicate whether a symbol has been inverted. The selective block inversion encoding technique tracks the running disparity on symbol boundaries of the symbols that have been transmitted so far. The running disparity represents the difference in the overall number of 1-bit values and 0-bit values of the symbols that have been transmitted on the communications link. For example, if 452 1-bit values and 448 0-bit values have been transmitted (e.g., 100 symbols), then the running disparity is +4 (e.g., in the 1−direction or positive). If 448 1-bit values and 452 0-bit values have been transmitted, then the running disparity is −4 (e.g., in the O-direction or negative). If the number of 1-bit values and 0-bit values are equal, then the running disparity is O (e.g., neutral). To determine whether to

		perform selective block inversion on a block of symbols, the encoding technique compares the running disparity of the symbols transmitted so far to the block disparity of that block. Block disparity is the difference between number of 1-bit values and 0-bit values of the symbols of a block. If the running disparity and the block disparity are both positive or both negative, then the encoding technique performs block inversion on that block. The encoding technique inverts a block by inverting alternate bits of the first symbol in the block (i.e., transition inversion) and inverting all the bits of the other symbols in the block (i.e., polarity inversion). The inverting of the alternate bits of the first symbol results in an out-of-band symbol that is used to indicate whether the following block has been block inverted. When a block of symbols is received, the receiving communications node can determine whether the block has been block inverted by checking the first symbol of the block. If the first symbol of the block is an in-band symbol, then the block has not been block inverted. If the first symbol of the block is an out-of-band symbol, then the block has been block inverted. If the block has been block inverted, then the decoding technique undoes the alternate bit inversion of the first symbol by inverting alternate bits of the first symbol and undoes the bit inversion of the other symbols by inverting all of the bits of the other symbols. One skilled in the art will appreciate that the symbol used to indicate whether the block is block inverted need not be the first symbol of the block, but rather can be any symbol of the block so long as the receiving communications node can identify which symbol indicates selective block inversion. FIG. 21A is a diagram illustrating the selective block inversion encoding technique in one embodiment. In this example, a block is defined as having four symbols. One skilled in the art will appreciate that a block can have any number of two or more symbols. In this example, the block disparity is +6, because there are 21 1-bit values and 15 0-bit values in the block. If the running disparity is positive, then the encoding technique performs block inversion. The first symbol of the block has its alternate bits inverted, and the remaining symbols of the block have all their bits inverted. The resulting symbols have a block disparity of −4. Thus, the DC-balance would be improved by transmitting the inverted block, rather than the noninverted block. The encoding technique may alternatively only perform block inversion when the running disparity is outside a certain range. For example, if the running disparity is between −100 and +100, then no selective block inversion is performed. If outside the range, then selective block inversion is

		performed. One skilled in the art will appreciate that this range can be selected based on various characteristics of the communications link such as transmission rate or maximum transmission distance. FIG. 21B is a block diagram illustrating selective block inversion with a programmable block size in one embodiment. In this example, the block size is represented by the variable "k." The selective block inversion encoding technique processes k sequential symbols at a time as indicated by blocks 2101 and 2102. The transition from block 2101 to 2102 illustrates selective block inversion for transmission, and the transition from block 2102 to 2101 illustrates the undoing of selective block inversion upon reception. To perform block inversion, the block header symbol Ci is transition inverted (TI) resulting in symbol Bi and the symbol Ci+1to symbol Ci+k−1 are polarity inverted (SI) resulting in symbol {overscore (Ci+1)} to symbol {overscore (Ci+k−1)}. To undo block inversion, the block header symbol Bi is transition inverted resulting in symbol Ci and the symbols {overscore (Ci+1)} to symbol {overscore (Ci+k−1)} are polarity inverted resulting in symbol Ci+1 and symbol Ci+k+1. FIG. 21C is a block diagram illustrating transition inversion and polarity inversion in one embodiment. In this example, 8-bit codes are inverted. The code 2110 may be transition inverted in two ways to generate codes 2111 and 2112. Code 2111 results from inverting alternate bits starting with the first bit, and code 2112 results from inverting alternate bits starting with the second bit. The code 2110 is polarity inverted by inverting each bit to generate code 2113. The same process is applied to codes 2111, 2112, and 2113 to generate code 2110. As discussed above, a primitive is a sequence of two out-of-band symbols. Thus, a receiving communications node can distinguish between a primitive and the first symbol of an inverted block because a primitive is a sequence of two out-of-band symbols and one out-of-band symbol by itself represents the first symbol of an inverted block. FIG. 22 is a diagram illustrating the format of a primitive in one embodiment. A primitive is defined as a sequence of two out-of-band symbols. The out-of-band symbols are preferably selected to have minimal impact on DC-balance. In particular, the disparity of a primitive is selected to be as close to 0 as possible. To achieve this disparity, one symbol of the primitive may have a negative disparity and the other symbol of the primitive may have any positive disparity.

		(A symbol with an odd number of bits cannot have a 0 disparity.) When the disparity of a primitive is 0, then the primitive can be transmitted at any time without affecting the running disparity and thus with minimal impact on the DC-balance. In one embodiment, the first symbol of a primitive has the negative disparity (i.e., negative polarity) and the second symbol has the positive disparity (i.e., positive polarity), or vice versa. The receiving communications node can detect a transmission error when a sequence of two out-of-band symbols has an improper ordering for their disparity or both symbols have either a positive or a negative disparity. When a primitive has minimal or no effect on DC-balance, then the complexity of the transmitting communications node may be reduced because the logic to calculate the running disparity need not include primitives in the calculation. FIGS. 23-28 are logic diagrams illustrating encoding and decoding techniques in one embodiment. FIG. 23 is a logic diagram illustrating transition control and selective block inversion encoding in one embodiment. A component of the link layer receives codes to be transmitted one code at a time from the transport layer. In block 2301, the component performs transition control optimization to generate a symbol from the code. In block 2302, the component buffers the symbols until a complete block of symbols has been buffered. In decision block 2303, if a complete block of symbols has been buffered, then the component continues at a block 2304, else the component waits to receive the next code. In decision block 2304, if the running disparity is equal to the block disparity, then the component continues at block 2305, else the component continues at block 2306. In block 2305, the component performs block inversion on the symbols of the block. In block 2306, the component provides the symbols of the buffer to the physical layer and then waits to receive the next code from the transport layer." Shin '450 at [0128-0140].

8b code	9 bit symbol
0000 0000	101010101
0000 0001	101010100
0000 0010	101010111
⋮	
0101 0101	001010101
⋮	
0111 0110	001110110
0111 0111	100100010
⋮	
1111 1111	110101010

Fig. 20

Shin ‘450 at Fig. 20.

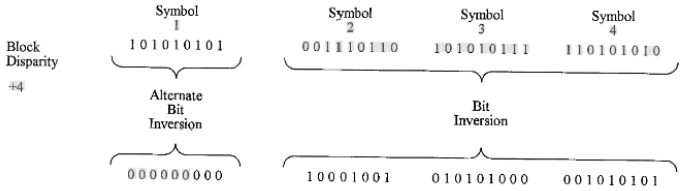


Fig. 21A

Shin ‘450 at Fig. 21A.

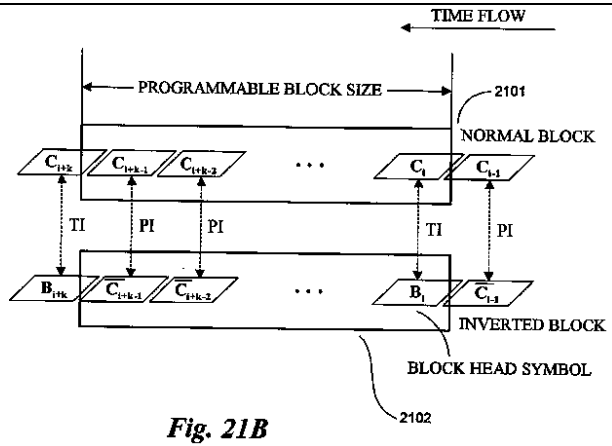


Fig. 21B

Shin ‘450 at Fig. 21B.

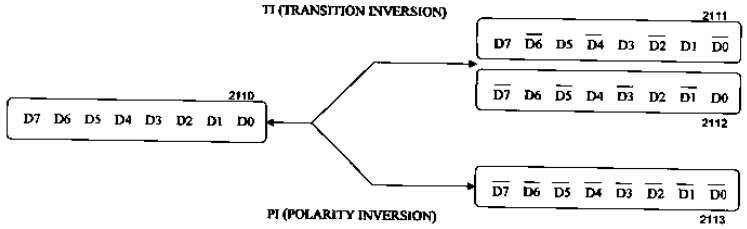
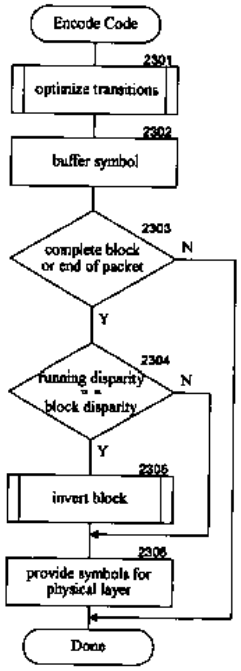


Fig. 21C

Shin ‘450 at Fig. 21C.

		 ***Fig. 23*** Shin '450 at Fig. 23.

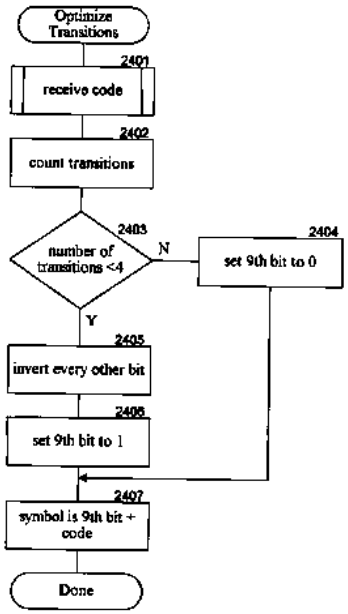
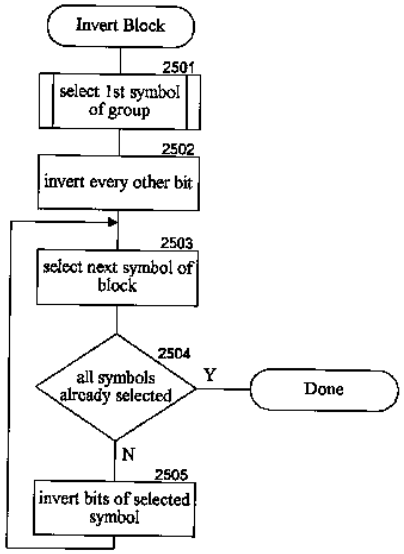
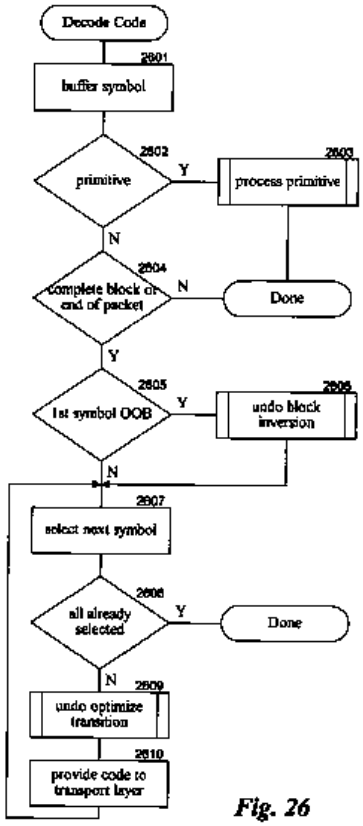
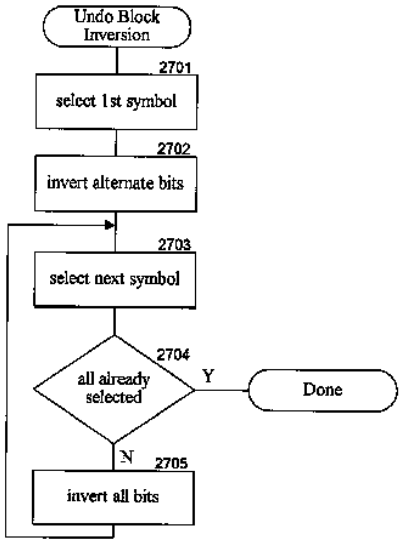


Fig. 24

Shin '450 at Fig. 24.

		 ***Fig. 25*** Shin '450 at Fig. 25.

		 ***Fig. 26*** Shin '450 at Fig. 26.

		 ***Fig. 27*** Shin '450 at Fig. 27.

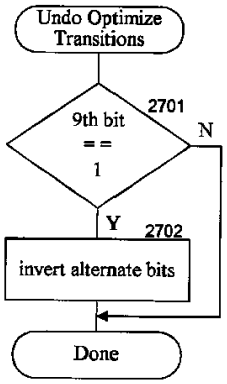
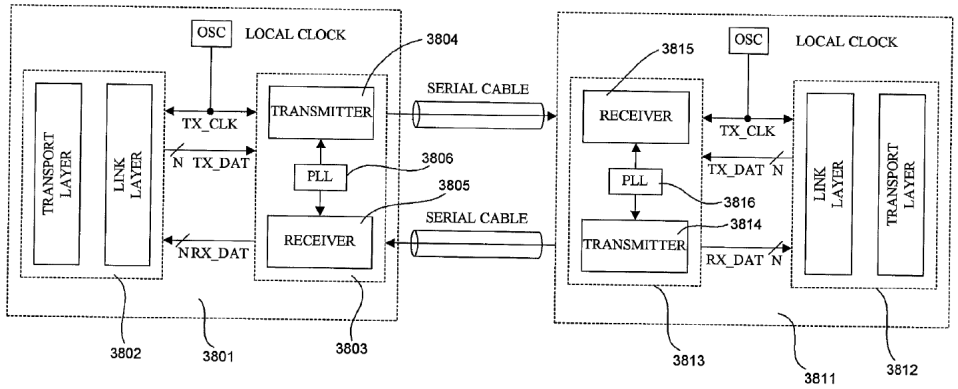


Fig. 28

Shin '450 at Fig. 28.

"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip.
The link layer provides symbols (i.e., N-bit encoded data) to be transmitted to the physical layer via TX_DAT lines."
Shin '450 at [0164-0165].

		 ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(e)	wherein the physical and link layer circuitry of the second endpoint is coupled to the link and configured to decode the encoded data	See exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(f)	to recover application data and control bits,	See exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more

		references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(g)	to perform at least one link level function in response to at least one of the control bits, and	Shin '450 discloses and/or renders obvious this limitation. See, e.g.: "In one embodiment, the serial communications architecture defines multiple primitives to operate as Synchronization signals. A Synchronization Signal is typically used by the physical layer to help ensure correct alignment of Symbols. A transmitting communications node periodically transmits Synchronization primitives So that the receiving communications node can properly align with that Synchronization primitive. When a communications node receives a Synchronization primitive, it knows that the primitive is correctly aligned on a Symbol boundary. The use of multiple Synchronization primitives allows for encoding packet type within a Synchronization primitive. In particular, the transport layer provides the packet type to the link layer. The link layer can then transmit a Synchronization primitive that indicates packet type immediately before the packet itself. The receiving communications node can take the appropriate action based on the packet type encoded in the Synchronization primitive without having to parse the packet header. Indeed, the packet header may not need to Separately include the packet type. The use of a Synchronization primitive with encoded packet type may be well adapted to use in an environment where the transmission time of a packet through the Switching network may be long relative to the time needed to Store the packet at the data Store device. For example, the time to transmit a packet through the Switching network may be longer than the time needed to Store the data of the packet in a memory-based data Store device. The rapid detection of packet type through a Synchronization primitive, rather than through a packet header, can reduce the processing time of a Switch. Also, when a Synchronization primitive encodes the packet type, then the link layer, rather than the transport layer, can detect packet type, which can enhance the Overall processing Speed." Shin '450 at [0096]. "After the packet has been transmitted, the link layer of the transmitting communications node Starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications

		node uses the Synchronization primitive encoded with packet type to align its Symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a Synchronization primitive encoded with the packet type. When the link layer detects a Synchronization primitive designating packet type, it Signals the transport layer So that the type of packet can be used when the packet is Stored in the receive memory, retrieved from the receive memory, Stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component Stores the packet in the data queue. The component then retrieves the next packet." Shin '450 at [0109]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(h)	to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry, and	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

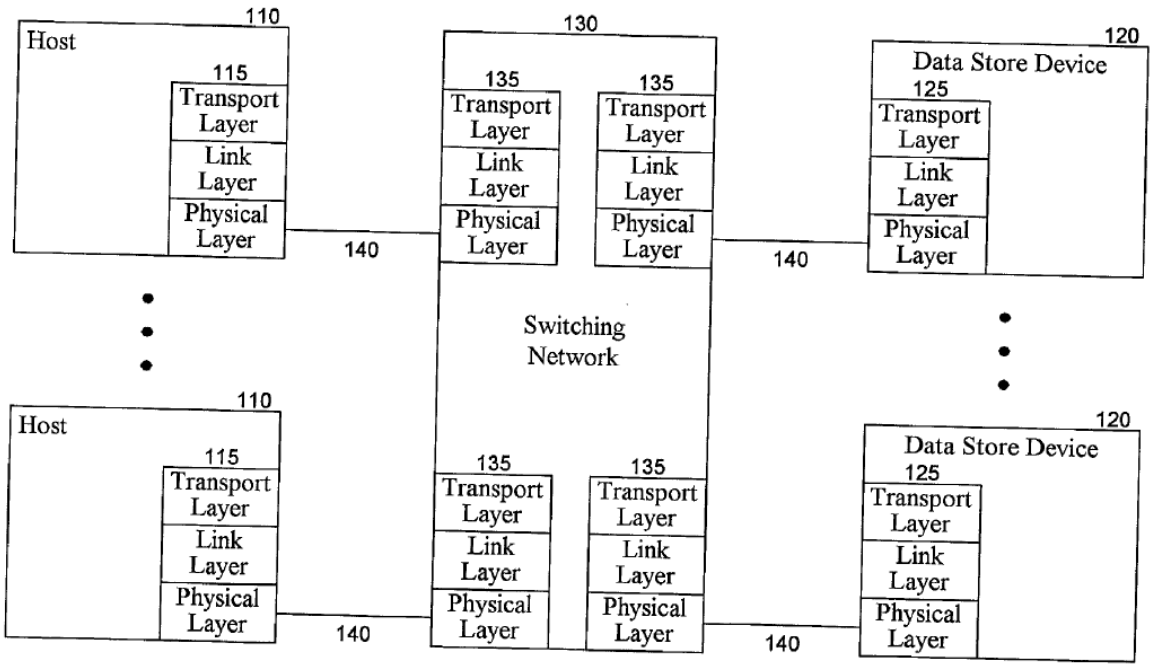


Fig. 1

Shin '450 at Fig. 1.

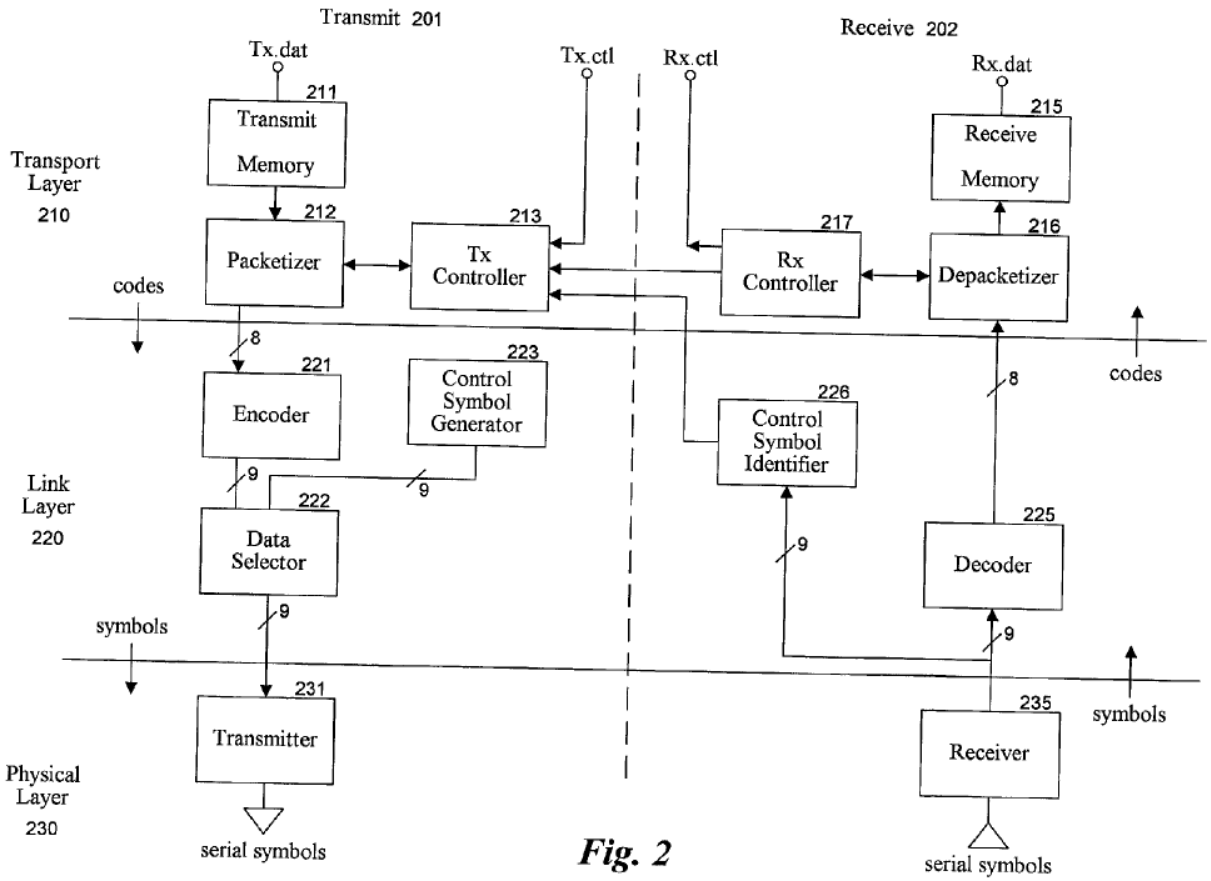


Fig. 2

Shin '450 at Fig. 2.

"The Storage Link architecture Specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture defines a hierarchy of transport, link, and physical layers Such that each layer in the hierarchy is aware of and can take advantage of characteristics of lower layers in the hierarchy. For example, the transport layer, which is responsible for handling packets, may

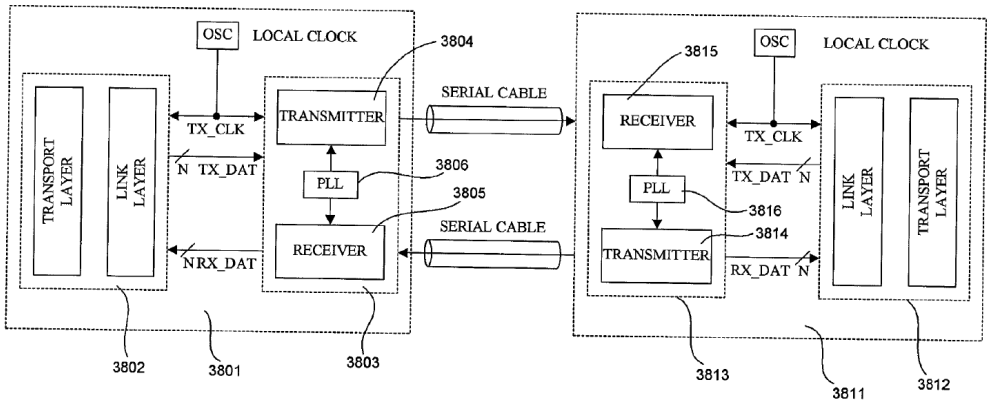
		receive Signals from the link layer that indicate when an end of packet is received. Traditional communications architectures prohibit a lower layer from being aware of the functions of a higher layer. The Storage Link architecture may provide packet ordering based on packet type, dynamic Segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band Symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at [0071]. "FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "The link layer encodes the codes to be transmitted via its communications link into Symbols and decodes Symbols received via its communications link into codes. The link layer receives codes to be transmitted from the transport layer, encodes those codes into Symbols, and provides those symbols to the physical layer. The link layer also receives Symbols from the physical layer, decodes those Symbols into codes, and provides those codes to the transport layer. The encoding

		may include mapping the codes to symbols to optimize bit transitions and to ensure DC balance. The physical layer receives the symbols from the link layer, Serializes the Symbols, and transmits the Serialized Symbols via the communications link. The physical layer receives Serialized Symbols via the communications link, deserializes the Symbols, and provides the Symbols to the link layer." Shin '450 at [0077]. "The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data… The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate." Shin '450 at [0079]. "The packet Segmentation is performed by the transport layer based on Signals provided by the link layer (e.g., in response to receiving an XOFF signal)." Shin '450 at [0089]. "FIG. 5 is a block diagram illustrating the organization of a data packet and a Segmented data packet in one embodiment. The payload Section of a data packet may include a target address and blocks of data to be Stored at the target address. For example, if the data Store device is a disk drive, then the target address may be a Sector address of the disk drive and the blocks of data may each correspond to a Sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF

		signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header Section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a Start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload Section is updated to reflect the Starting address at which the remaining blocks of the packet are to be Stored. For example, if packet 510 is segmented after block 504 and the Starting address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth." Shin '450 at [0090]. "In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a Synchronization primitive encoded with the packet type. When the link layer detects a Synchronization primitive designating packet type, it Signals the transport layer So that the type of packet can be used when the packet is Stored in the receive memory, retrieved from the receive memory, Stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component Stores the packet in the data queue. The component then retrieves the next packet." Shin '450 at [0109].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 266

		"FIG. 15 is a logic diagram illustrating processing of packet preemption by a receiving communications node in one embodiment. In block 1501, the component of the transport layer retrieves the next code from the link layer. In decision block 1502, if the link layer signals that a preempt primitive has been received, then the component continues at block 1504, else the component continues at block 1503. In block 1503, the component adds the code to the current packet and retrieves the next code in block 1501. In block 1504, the component Saves current packet information So that it can continue Storing codes in the packet after the preemption is complete. In block 1505, the component processes the preempting packet. The processing includes receiving each code and Storing the codes in a preempting packet until the link layer indicates that it received a continue primitive." Shin '450 at [0115]. "FIG. 38A is a block diagram of a plesiosynchronous communications System in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional Serial link. The transport layer and the link layer 3802, 3812 may be implemented in a Single digital ASIC chip with other interface logic Such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip." Shin '450 at [0164].

		 ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
1(i)	wherein the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data… The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate."

		Shin '450 at [0079]. "FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "The packet Segmentation is performed by the transport layer based on Signals provided by the link layer (e.g., in response to receiving an XOFF signal)." Shin '450 at [0089]. "FIG. 5 is a block diagram illustrating the organization of a data packet and a Segmented data packet in one embodiment. The payload Section of a data packet may include a target address and blocks of data to be Stored at the target address. For example, if the data Store device is a disk drive, then the target address may be a Sector address of the disk drive and the blocks of data may each correspond to a Sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF

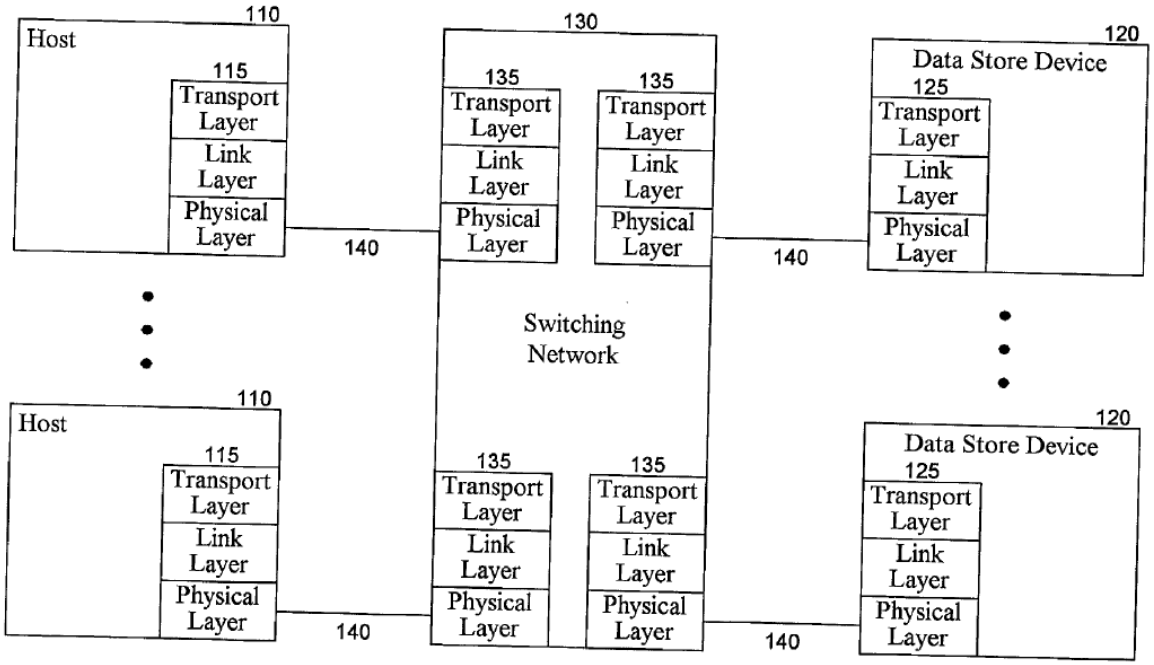
		signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header Section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a Start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload Section is updated to reflect the Starting address at which the remaining blocks of the packet are to be Stored. For example, if packet 510 is segmented after block 504 and the Starting address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth." Shin '450 at [0090]. "Because of the way memory is typically accessed, the physical layer, link layer, and transport layer might be Simplified as compared to the layers needed in a more general data Store device, Such as a disk drive. Each port of a multiport memory device is typically directly connected to a host. In Such a case, packets do not need to specify a Source and a destination and the headers are thus simplified. In addition, packet types can be encoded in Synchronization primitives to further simplify the packet header. The transport layer of a port in a multiport memory device can be Simplified or eliminated because (1) routing to another device is not needed, (2) minimal or no parsing of the header may be needed, and (3) preemption and priority ordering of packets may not be needed. In addition, the link layer may be simplified by the use of physical layer DC-balancing, rather than the use of the selective block inversion to achieve DC-balance. Physical layer DC-balancing can be used with a multiport memory device because the distance between the host and the multiport memory device is typically relatively short."

		Shin '450 at [0148]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 2		
2	The system of claim 1, wherein the line code specifies a block code and special characters, the first endpoint is configured to encode M-bit input words in accordance with the block code to generate a code word sequence of N-bit code words, where N>M, the code word sequence is indicative of at least one cell of the input words, and the encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.	Shin '450 discloses, expressly or inherently, the system of claim 1 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 1. "The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at [0071]. "FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer. The hosts and data store devices have an upper layer that communicate to each other via transactions. When transmitting data, the upper layer provides the data for the transaction to the transport layer. The transport layer receives the data of the transaction and generates packets (i.e., packetizes the data) for transmission. The transport layer then provides each code (e.g., each byte) of the packets to the link layer for transmission to the destination. When receiving data, the

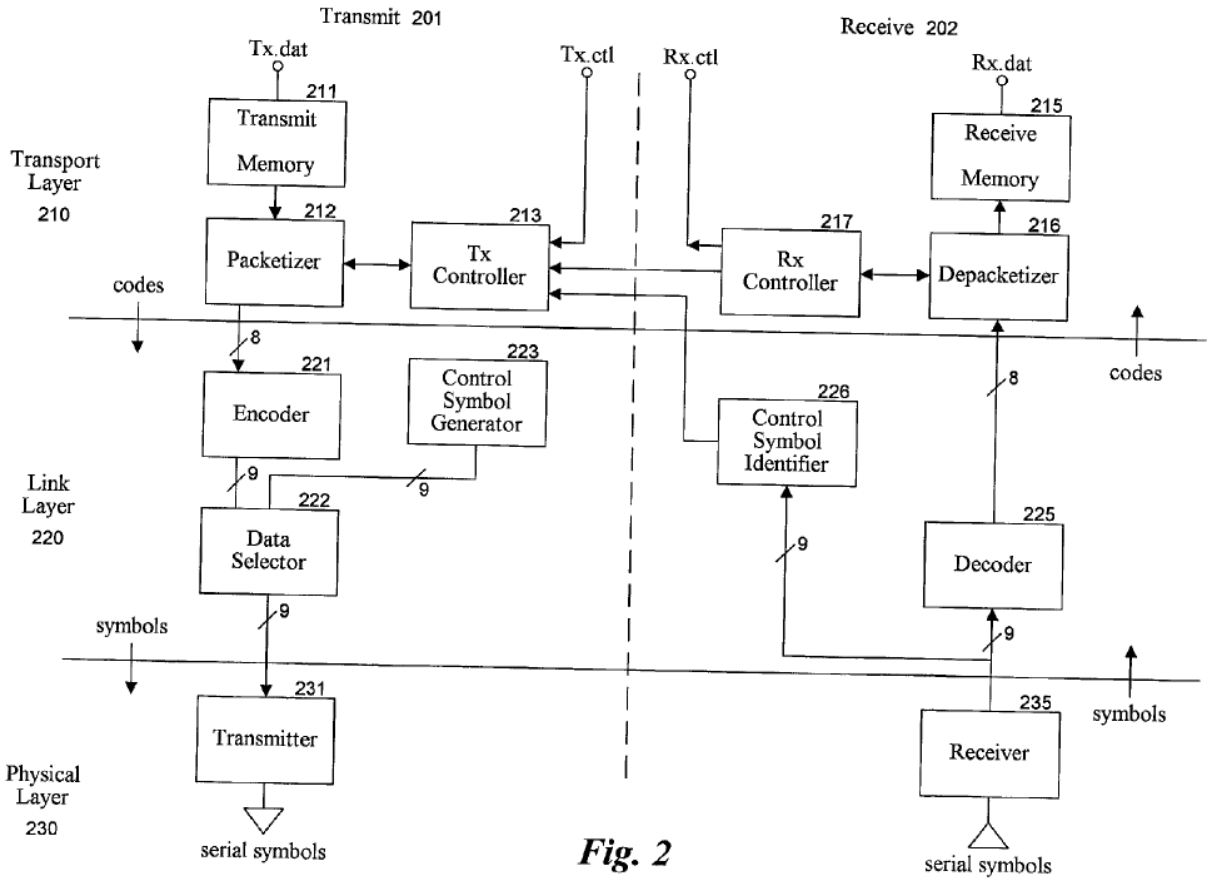
		transport layer receives the codes of transaction from the link layer and identifies the packets. The transport layer then combines the data of the packets of the transaction (i.e., depacketizes the data) and provides the data of the transaction to the upper layer. Each host and data store device may include an application upper layer that provides the data of a transaction to the transport layer to be transmitted to a destination and receives the data of a transaction from the transport layer that was transmitted by a source. Each packet includes a header section and a payload section. The header section identifies the source and destination and a packet type (e.g., data or command). Each switch may include a communications interface for each port of the switch. Each port may be connected to a serial communications link comprising a receive and transmit link. The switches and their interconnecting communications links form the switching network. The transport layer of a switch may not packetize and depacketize the data, rather it may direct packets received via one port to be transmitted via another port to affect the routing of the packets from the source to the destination as indicated in the header section. The link layer encodes the codes to be transmitted via its communications link into symbols and decodes symbols received via its communications link into codes. The link layer receives codes to be transmitted from the transport layer, encodes those codes into symbols, and provides those symbols to the physical layer. The link layer also receives symbols from the physical layer, decodes those symbols into codes, and provides those codes to the transport layer. The encoding may include mapping the codes to symbols to optimize bit transitions and to ensure DC-balance. The physical layer receives the symbols from the link layer, serializes the symbols, and transmits the serialized symbols via the communications link. The physical layer receives serialized symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. FIG. 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, Such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, Such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets

		to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and Store the codes as packets in the receive memory. The link layer includes transmit components, such as an encoder 221, a data Selector 222, and a control Symbol generator 223, and receive components, Such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for receiving and identifying, control Symbols, Synchronization Symbols, timing Symbols, and So on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control Symbols and Synchronization Symbols. The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data. The data Selector Selects Symbols encoded from codes provided by the transport layer or Symbols generated by the control Symbol generator. The data Selector effectively inserts control Symbols and Synchronization Symbols into the Sequence of symbols that are to be transmitted. Various possible encoding techniques for the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate. The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the Serialized Symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 273

		duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode." Shin '450 at [0075-0081].  ***Fig. 1***

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 274

		Shin ‘450 at Fig. 1.  ***Fig. 2*** Shin ‘450 at Fig. 2. “FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on

		a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers. As described above, the primitives are pairs of out-of-band symbols. (In the following, a symbol is assumed to have nine bits.) In one embodiment, when the in-band symbols are transition maximized, then the symbols of the control primitives have three transitions each and the symbols of the synchronization primitives have two transitions each. When the in-band symbols are transition minimized, then the symbols of the control primitives have five transitions each and the synchronization primitives have one symbol with five transitions and another symbol with seven transitions. Table 1 illustrates control primitives in one embodiment when the in-band symbols are transition maximized. Each control primitive comprises two symbols in which the first symbol is a polarity inversion of the second symbol. As a result, the disparity (described below) of each control primitive is 0. The control primitives such as XON, XOFF, preempt, and continue are selected from this table of control primitives. TABLE 1 Control primitives in transition maximization mode 0. 000010111-111101000

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 276

		1. 000011011-111100100 2. 000011101-111100010 3. 000100111-111011000 4. 000110011-111001100 5. 000111001-111000110 6. 001000111-110111000 7. 001100011-110011100 8. 001110001-110001110 9. 010000111-101111000 10. 011000011-100111100 11. 011100001-100011110 12. 100001110-011110001 13. 100011100-011100011 14. 100111000-011000111 15. 101110000-010001111 16. 110000110-001111001 17. 110001100-001110011 18. 110011000-001100111 19. 110110000-001001111 20. 111000010-000111101 21. 111000100-000111011

		22. 111001000-000110111 23. 111010000-000101111 Table 2 illustrates control primitives in one embodiment when the in-band symbols are transition minimized. TABLE 2 Control primitives in transition minimization mode 0. 000010101-111101010 1. 000100101-111011010 2. 000101001-111010110 3. 000101011-111010100 4. 000101101-111010010 5. 000110101-111001010 6. 001000101-110111010 7. 001001001-110110110 8. 001001011-110110100 9. 001001101-110110010 10. 001010001-110101110 11. 001010011-110101100 12. 001011001-110100110 13. 001100101-110011010 14. 001101001-110010110

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 278

		15. 010000101-101111010 16. 010001001-101110110 17. 010001011-101110100 18 010001101-101110010 19. 010010001-101101110 20. 010010011-101101100 21. 010011001-101100110 22. 010100001-101011110 23. 010100011-101011100 24. 010110001-101001110 25. 011000101-100111010 26. 011001001-100110110 27. 011010001-100101110 28. 100001010-011110101 29. 100010010-011101101 30. 100010100-011101011 31. 100010110-011101001 32. 100011010-011100101 33. 100100010-011011101 34. 100100100-011011011 35. 100100110-011011001

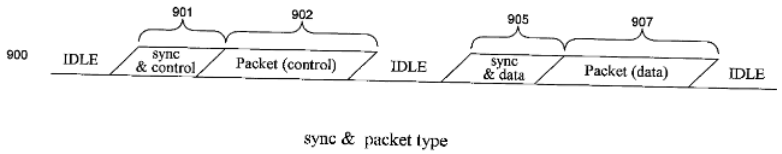
		36. 100101000-011010111 37. 100101100-011010011 38. 100110010-011001101 39. 1001101000-11001011 40. 101000010-010111101 41. 101000100-010111011 42. 101000110-010111001 43. 101001000-010110111 44. 101001100-010110011 45. 101010000-010101111 46. 101011000-010100111 47. 101100010-010011101 48. 101100100-010011011 49. 101101000-010010111 50. 110001010-001110101 51. 110010010-001101101 52. 110010100-001101011 53. 110100010-001011101 54. 110100100-001011011 55. 110101000-001010111

		The synchronization primitives are distinct from the control primitives. The synchronization primitives are selected to have the characteristic that when two synchronization primitives are transmitted sequentially the receiving device can unambiguously identify the synchronization primitives regardless of what is transmitted before or after the synchronization primitives. The synchronization primitives have a unique number of transitions that is not found in any control primitive or in-band symbol. In one embodiment, the synchronization primitive can be detected by looking for a sequence of symbols with that number of transitions. In one embodiment, the synchronization primitives are selected to start with a falling edge (i.e., "10"), a rising edge (i.e., "01"), a high level (i.e., "11"), or a low level (i.e., "00"). The selection of the start of the synchronization primitives is referred to as the "synchronization detection mode." Table 3 contains synchronization primitives in transition maximization mode that start with a falling edge and a rising edge. Each symbol in Table 3 contains two transitions resulting in synchronization primitives with four transitions. Table 4 contains synchronization primitives in transition minimization mode that start with a low level and a high level. Each synchronization primitive in Table 4 has 13 transitions. The high-level and low-level synchronization primitives have five transitions in one symbol, seven transitions in the other symbol, and one transition from their first to second symbol. TABLE 3 Falling Edge Rising Edge 0 100000001-100111111 011000000-011111110 1 100000011-100011111 011100000-011111100 2 100000111-100001111 011110000-011111000 3 100001111-100000111 011111000-011110000 4 100011111-100000011 011111100-011100000 5 100111111-100000001 011111110-011000000 TABLE 4

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 281

		High Level Low Level 0 110101000-110101010 001010101-001010111 1 110100010-110101010 001010101-001011101 2 110001010-110101010 001010101-001110101 3 110100100-110101010 001010101-001011011 4 110010100-110101010 001010101-001101011 5 110101010-110101000 001010111-001010101 6 110101010-110100010 001011101-001010101 7 110101010-110001010 001110101-001010101 8 110101010-110100100 001011011-001010101 9 110101010-110010100 001101011-001010101 Table 5 lists the transition distribution of the low and high polarity symbols onization primitives. TABLE 5 Total # of Transi-tions Sync Detect Mode / Transition Distribution in Low Polarity / Transition Distribution in High Polarity / in a Sync Primitive Falling edge (“10”) — one “10” and one “01” — one “10” and one “01” — 4 Risin edge — one “01” and one “10” — one “01” and one “10” — 4

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 282

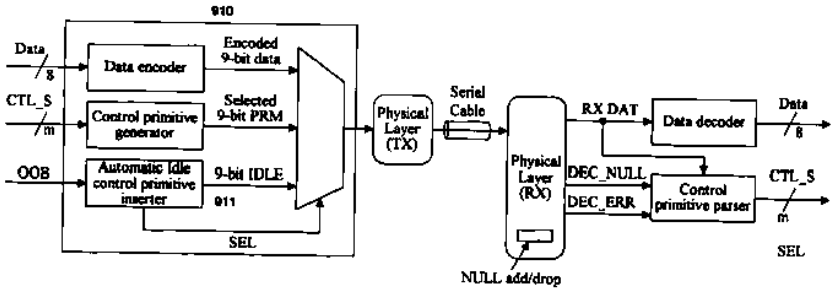
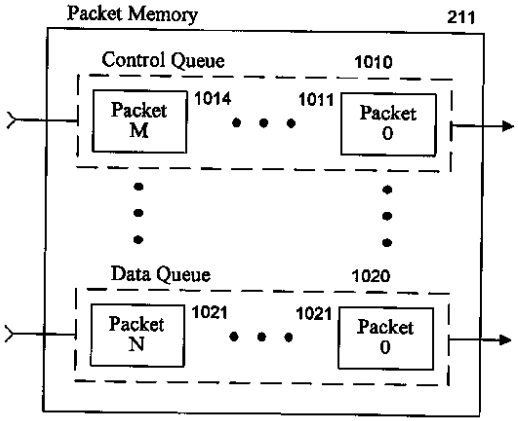
		(“01”) High level one “11” and two “00” one “11” and no “00” 13 (“11”) Low level one “00” and no “11” one “00” and two “11” 13 (“00”) In one embodiment, the synchronization primitives are detected by buffering three symbols (e.g., 27 bits). The synchronization primitives are selected so that any time the buffer has exactly three of the synchronization detection mode bits (e.g., “10” for falling edge) that are each 9 bits apart then the bits are at the beginning of a synchronization symbol. The bit buffer contains 27 bits, A[8:0], B[8:0], and C[8:0], in which bit A[8] was received first and bit C[0] was received last. In this example, the content of bits A[6]:B[7] represent synchronization symbol “100000001” and B[6]:C[7] represent synchronization symbol “100111111.” The starting points of the synchronization symbols (“synchronization markers”) are A[6], B[6], and C[6].” Shin ‘450 at [0097-0104].  *Fig. 9A* Shin ‘450 at Fig. 9A. “FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code (‘Data’) to be transmitted and with an indication of a control primitive (‘CTL-S’) to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g.,

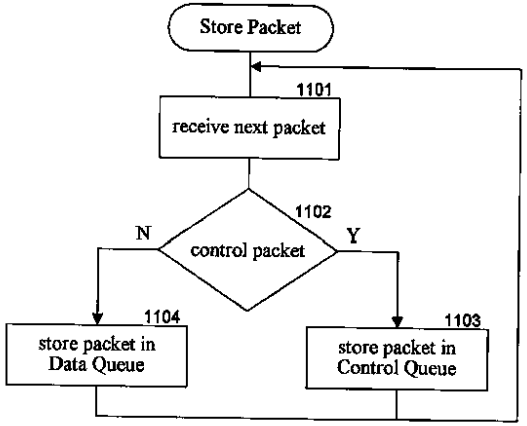
		Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer. 1.3 Transmission Order Based on Packet Type In one embodiment, a communications node transmits packets of certain types before packets of other types regardless of the order in which the packets are received or generated by the communications node. For example, a switch may transmit control packets (e.g., command packets, status packets, and message packets) before transmitting data packets. The transmitting of control packets before data packets may help ensure that the control packets are not unnecessarily delayed by data packets, which may have a tendency to be quite large. For example, a command packet requesting a read from a data store device may be transmitted before a data packet even through the control packet was received after the data packet. The data store device can thus start processing the read request without having to wait until the data packet is transmitted. A communications node may store control packets and data packets in separate areas of the packet memory and only select packets from the data packet area when the control packet area is empty. Alternatively, the communications node may use various algorithms to select control or data packets to be transmitted. For example, the algorithm may select a data packet that has been in the packet memory for certain amount of time even though there may be a control packet in the control area. In this way, a sequence of many control packets will not delay the data packet more than that certain amount of time. One skilled in the art will appreciate that there may be multiple packet types with different transmission orders. For example, a status packet might be transmitted before a command packet, and a command packet might be transmitted before a data packet.

		FIG. 10 is a block diagram illustrating an organization of a packet memory in one embodiment. The transmit packet memory 211 may include control queue 1010 and data queue 1020. The control queue contains the control packets 1011, and the data queue contains the data packets 1021. Packets to be transmitted are stored either in the control queue or the data queue based on packet type (which may be encoded in a synchronization primitive). When a transmitting communications node is ready to transmit the next packet, it retrieves the next packet from the control queue. If the control queue is empty, then the transmitting communications node retrieves the next packet from the data queue. FIG. 11 is a logic diagram illustrating a process of storing packets in a transmit memory in one embodiment. Similar logic can be used to store packets in the receive memory of a communications node. In block 1101, a component of the transport layer receives the next packet from an upper layer. In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a synchronization primitive encoded with the packet type. When the link layer detects a synchronization primitive designating packet type, it signals the transport layer so that the type of packet can be used when the packet is stored in the receive memory, retrieved from the receive memory, stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component stores the packet in the data queue. The component then retrieves the next packet. FIG. 12 is a logic diagram illustrating the transport layer processing of packets stored in the packet memory in one embodiment. In decision block 1201, if the control queue is empty, then the component continues to block 1203, else the component retrieves a control packet from the control queue in block 1202 and continues at block 1205. In decision block 1203, if the data queue is empty, then the component again checks for a packet in the control queue, else the component retrieves a packet from the data queue in block 1204 and continues at block 1205. In blocks 1205-1207, the component selects the codes of the retrieved packet. In block 1205, the component selects the next code of the retrieved packet. In decision block 1206, if all codes have already been selected, then the component continues at block 1201 to check for the next packet,

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 285

		else the component continues at block 1207. In block 1207, the component provides the selected code to the link layer and then continues at block 1205 to select the next code of the packet. 1.4 Packet Preemption In one embodiment, a communications node may preempt or interrupt the transmission of a packet when a packet with a higher priority is to be transmitted on the same communications link. Packet preemption helps ensure that data store devices receive control packets as soon as possible without being slowed by network congestion as a result of data packets. In particular, the transmission of a data packet, which may be large, may be preempted so that a control packet, which is typically small, may be transmitted. When a data packet is to be preempted, the transport layer of the communications node stops providing the codes of the data packet to the link layer, signals the link layer to transmit a preempt primitive, and then starts providing the code of the control packet to the link layer for transmission as a preempting packet. When the preempting packet is has been completely transmitted, the transport layer of the communications node signals the link layer to transmit a continue primitive and then resumes providing the remainder of the codes of the data packet to the link layer. The link layer of the receiving communications node detects the preempt primitive while it is receiving the codes of the data packet and signals its transport layer. The transport layer then starts storing the subsequent codes as a control packet. When the link layer detects the continue primitive, it signals the transport layer, which continues receiving the preempted data packet. The preempt and continue primitives, which are control primitives, serve to delimit transmission of a preempting packet. One skilled in the art will appreciate that packet preemption could be nested to any level. For example, a status packet might preempt a command packet that already preempted a data packet. FIG. 13 is a diagram illustrating the preemption of a packet in one embodiment. Serial link content diagram 1300 illustrates a data packet that is preempted by a control packet. Initially, the transmitting communications node transmits the first portion of data packet 1301. When the packet is to be preempted, the communications node then transmits the preempt primitive 1302. After transmitting the preempt primitive, the transmitting communications node transmits the preempting control packet 1303. After the control packet is transmitted, the communications node

		transmits the continue primitive 1304, and then resumes transmitting the remainder of the preempted data packet 1305." Shin '450 at [0105-0113].  *Fig. 9C* Shin '450 at Fig. 9C.  *Fig. 10*

		Shin ‘450 at Fig. 10.  ***Fig. 11*** Shin ‘450 at Fig. 11.

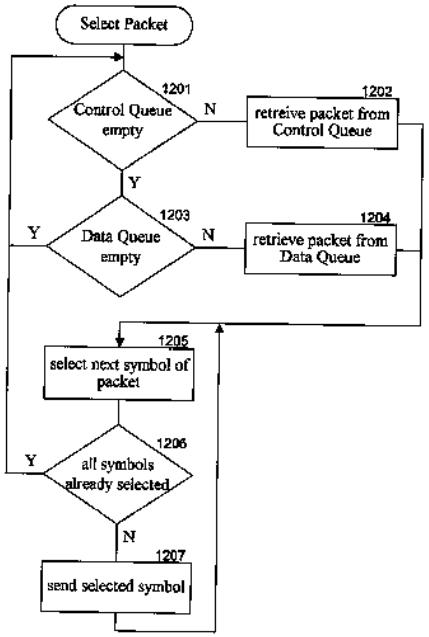


Fig. 12

Shin '450 at Fig. 12.

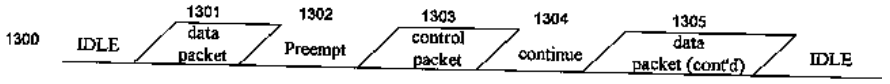


Fig. 13

Shin '450 at Fig. 13.

"In one embodiment, the link layer of a communications node encodes codes into symbols in order to optimize transition control and to ensure DC-balance. Transition control may be optimized to either maximize or minimize the number of transitions in symbols that are to be

		transmitted. A transition is defined as a bit value of 1 followed by a bit value of 0 or a bit value of 0 followed by a bit value of 1. When the number of transitions is maximized, clock information may be more accurately derived from the transmitted symbols. When the number of transitions is minimized, overall electromagnetic interference may be minimized. One skilled in the art will appreciate that the link layer may be designed to minimize or maximize transitions depending on the overall design objectives. In the following, the described encoding technique attempts to maximize the number of transitions in symbols to be transmitted. In an alternate embodiment, the transitions can be maximized at times and minimized at other times to balance the objectives of deriving a clock signal and reducing electromagnetic interference. The encoding technique in one embodiment encodes an 8-bit code based on the number of transitions in that code. The maximum possible number of transitions in an 8-bit code is seven and occurs when the bit values alternate between 0 and 1 (e.g., “10101010”). The minimum possible number of transitions in an 8-bit code is zero and occurs when all the bit values are the same (e.g., “11111111”). To maximize the number of transitions, the encoding technique inverts the bit value of alternate bits in each code with less than four transitions. This alternate bit inversion, also referred to as transition inversion, results in a code that previously had “n” transitions to now have |n- 7| transitions. For example, the result of alternate bit inversion of a code with zero transitions (e.g., “11111111”) is a code with seven transitions (e.g., “01010101”), and the result of alternate bit inversion of the code with three transitions (e.g., “00010111”) is a code with four transitions (e.g., “10111101”). The encoding technique adds a ninth bit (i.e., a transition inversion indicating bit) to the 8-bit code to indicate whether the alternate bits of the code were inverted, which results in a 9-bit symbol. For example, a bit value of 0 in the ninth bit indicates that the code did not have its alternate bits inverted, and a bit value of 1 in the ninth bit indicates that the code did have its alternate bits inverted. The symbol “010111101” has a bit value of 0 in its ninth bit, which indicates that alternate bits were not inverted. In contrast, the symbol “110111101” has a bit value of 1 in its ninth bit, which indicates that alternate bits were inverted. One skilled in the art will appreciate that the ninth bit can be stored at any bit position within the symbol. In this description, the ninth bit is represented as the most significant bit of the symbols.

		When a symbol is received at a communications node, the ninth bit is used to determine whether the symbol needs to have its alternate bits inverted to decode the symbol. Since the symbol "010111101" has a bit value of 0 in its ninth bit, its alternate bits were not inverted and the resulting decoded code is "10111101." Conversely, since the symbol "110111101" has a bit value of 1 in its ninth bit, its alternate bits were inverted and the resulting decoded code is "00010111." All the symbols generated by alternate bit inversion encoding are referred to as "in-band symbols" because they are 9-bit symbols with at least four transitions. All 9-bit symbols with three or less transitions are referred to as "out-of-band symbols." This alternate bit inversion encoding technique generates only in-band symbols. FIG. 20 illustrates an alternate bit inversion encoding technique in one embodiment. The left column represents the 8-bit codes, and the right column represents the 9-bit symbols. The alternate bit inversion encoding technique is referred to as an 8 b/9 b encoding, which is a more efficient encoding than standard 8 b/10 b encodings. Transition control encoding is described in U.S. Pat. No. 5,999,571, entitled "Transition-Controlled Digital Encoding and Signal Transmission System," which is hereby incorporated by reference. The encoding technique may also help ensure DC-balance by using selective block inversion encoding on symbols that have been transition optimized. Selective block inversion refers to an encoding technique that inverts certain bit values in a block of symbols to help ensure DC-balance is maintained. In one embodiment, selective block inversion may perform polarity inversion (i.e., inverting each bit of a symbol) on all but one symbol of a block to help ensure DC-balance and transition inversion on that one symbol in the block to indicate that the other symbols of the block have been polarity inverted. Although the encoding technique performs selective block inversion on blocks of four symbols, one skilled in the art will appreciate that a block can contain any number of symbols. Conventional encoding techniques, in contrast, typically process only one symbol at a time when attempting to ensure DC-balance. Because the selective block inversion encoding technique evaluates DC-balance over multiple symbols, DC-balance is more likely assured and there is essentially no bandwidth used to indicate whether a symbol has been inverted.

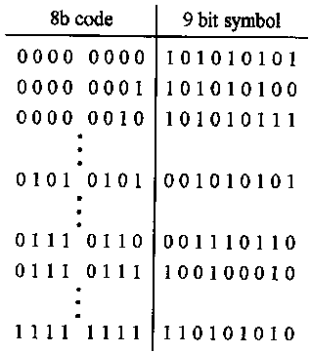
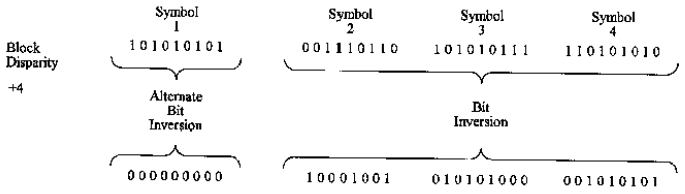
		The selective block inversion encoding technique tracks the running disparity on symbol boundaries of the symbols that have been transmitted so far. The running disparity represents the difference in the overall number of 1-bit values and 0-bit values of the symbols that have been transmitted on the communications link. For example, if 452 1-bit values and 448 0-bit values have been transmitted (e.g., 100 symbols), then the running disparity is +4 (e.g., in the 1−direction or positive). If 448 1-bit values and 452 0-bit values have been transmitted, then the running disparity is −4 (e.g., in the O-direction or negative). If the number of 1-bit values and 0-bit values are equal, then the running disparity is O (e.g., neutral). To determine whether to perform selective block inversion on a block of symbols, the encoding technique compares the running disparity of the symbols transmitted so far to the block disparity of that block. Block disparity is the difference between number of 1-bit values and 0-bit values of the symbols of a block. If the running disparity and the block disparity are both positive or both negative, then the encoding technique performs block inversion on that block. The encoding technique inverts a block by inverting alternate bits of the first symbol in the block (i.e., transition inversion) and inverting all the bits of the other symbols in the block (i.e., polarity inversion). The inverting of the alternate bits of the first symbol results in an out-of-band symbol that is used to indicate whether the following block has been block inverted. When a block of symbols is received, the receiving communications node can determine whether the block has been block inverted by checking the first symbol of the block. If the first symbol of the block is an in-band symbol, then the block has not been block inverted. If the first symbol of the block is an out-of-band symbol, then the block has been block inverted. If the block has been block inverted, then the decoding technique undoes the alternate bit inversion of the first symbol by inverting alternate bits of the first symbol and undoes the bit inversion of the other symbols by inverting all of the bits of the other symbols. One skilled in the art will appreciate that the symbol used to indicate whether the block is block inverted need not be the first symbol of the block, but rather can be any symbol of the block so long as the receiving communications node can identify which symbol indicates selective block inversion. FIG. 21A is a diagram illustrating the selective block inversion encoding technique in one embodiment. In this example, a block is defined as having four symbols. One skilled in the art will appreciate that a block can have any number of two or more symbols. In this example, the

		block disparity is +6, because there are 21 1-bit values and 15 0-bit values in the block. If the running disparity is positive, then the encoding technique performs block inversion. The first symbol of the block has its alternate bits inverted, and the remaining symbols of the block have all their bits inverted. The resulting symbols have a block disparity of −4. Thus, the DC-balance would be improved by transmitting the inverted block, rather than the noninverted block. The encoding technique may alternatively only perform block inversion when the running disparity is outside a certain range. For example, if the running disparity is between −100 and +100, then no selective block inversion is performed. If outside the range, then selective block inversion is performed. One skilled in the art will appreciate that this range can be selected based on various characteristics of the communications link such as transmission rate or maximum transmission distance. FIG. 21B is a block diagram illustrating selective block inversion with a programmable block size in one embodiment. In this example, the block size is represented by the variable "k." The selective block inversion encoding technique processes k sequential symbols at a time as indicated by blocks 2101 and 2102. The transition from block 2101 to 2102 illustrates selective block inversion for transmission, and the transition from block 2102 to 2101 illustrates the undoing of selective block inversion upon reception. To perform block inversion, the block header symbol Ci is transition inverted (TI) resulting in symbol Bi and the symbol Ci+1to symbol Ci+k−1 are polarity inverted (SI) resulting in symbol {overscore (Ci+1)} to symbol {overscore (Ci+k−1)}. To undo block inversion, the block header symbol Bi is transition inverted resulting in symbol Ci and the symbols {overscore (Ci+1)} to symbol {overscore (Ci+k−1)} are polarity inverted resulting in symbol Ci+1 and symbol Ci+k+1. FIG. 21C is a block diagram illustrating transition inversion and polarity inversion in one embodiment. In this example, 8-bit codes are inverted. The code 2110 may be transition inverted in two ways to generate codes 2111 and 2112. Code 2111 results from inverting alternate bits starting with the first bit, and code 2112 results from inverting alternate bits starting with the second bit. The code 2110 is polarity inverted by inverting each bit to generate code 2113. The same process is applied to codes 2111, 2112, and 2113 to generate code 2110.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 293

		As discussed above, a primitive is a sequence of two out-of-band symbols. Thus, a receiving communications node can distinguish between a primitive and the first symbol of an inverted block because a primitive is a sequence of two out-of-band symbols and one out-of-band symbol by itself represents the first symbol of an inverted block. FIG. 22 is a diagram illustrating the format of a primitive in one embodiment. A primitive is defined as a sequence of two out-of-band symbols. The out-of-band symbols are preferably selected to have minimal impact on DC-balance. In particular, the disparity of a primitive is selected to be as close to 0 as possible. To achieve this disparity, one symbol of the primitive may have a negative disparity and the other symbol of the primitive may have any positive disparity. (A symbol with an odd number of bits cannot have a 0 disparity.) When the disparity of a primitive is 0, then the primitive can be transmitted at any time without affecting the running disparity and thus with minimal impact on the DC-balance. In one embodiment, the first symbol of a primitive has the negative disparity (i.e., negative polarity) and the second symbol has the positive disparity (i.e., positive polarity), or vice versa. The receiving communications node can detect a transmission error when a sequence of two out-of-band symbols has an improper ordering for their disparity or both symbols have either a positive or a negative disparity. When a primitive has minimal or no effect on DC-balance, then the complexity of the transmitting communications node may be reduced because the logic to calculate the running disparity need not include primitives in the calculation. FIGS. 23-28 are logic diagrams illustrating encoding and decoding techniques in one embodiment. FIG. 23 is a logic diagram illustrating transition control and selective block inversion encoding in one embodiment. A component of the link layer receives codes to be transmitted one code at a time from the transport layer. In block 2301, the component performs transition control optimization to generate a symbol from the code. In block 2302, the component buffers the symbols until a complete block of symbols has been buffered. In decision block 2303, if a complete block of symbols has been buffered, then the component continues at a block 2304, else the component waits to receive the next code. In decision block 2304, if the running disparity is equal to the block disparity, then the component continues at block 2305, else the component continues at block 2306. In block 2305, the component performs block inversion on the symbols

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 294

		of the block. In block 2306, the component provides the symbols of the buffer to the physical layer and then waits to receive the next code from the transport layer." Shin '450 at [0128-0140].  ***Fig. 20*** Shin '450 at Fig. 20.  ***Fig. 21A*** Shin '450 at Fig. 21A.

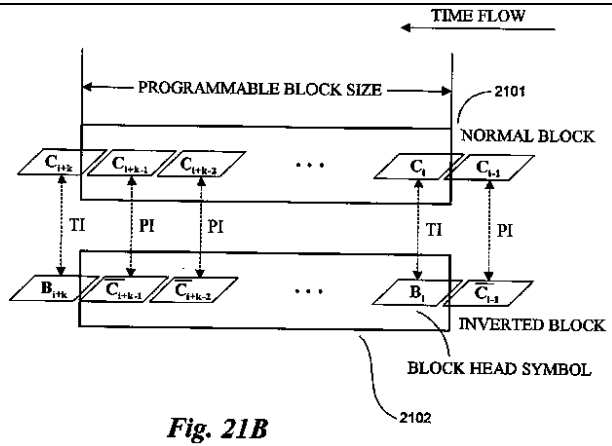


Fig. 21B

Shin ‘450 at Fig. 21B.

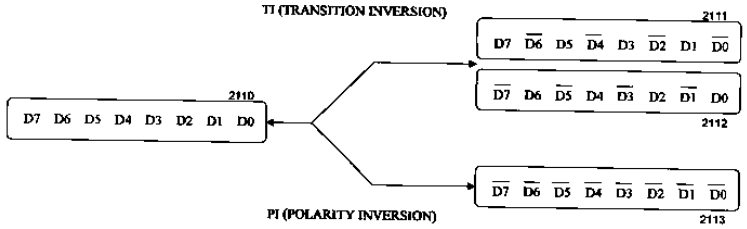
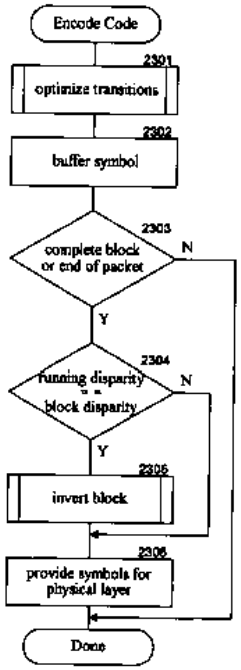
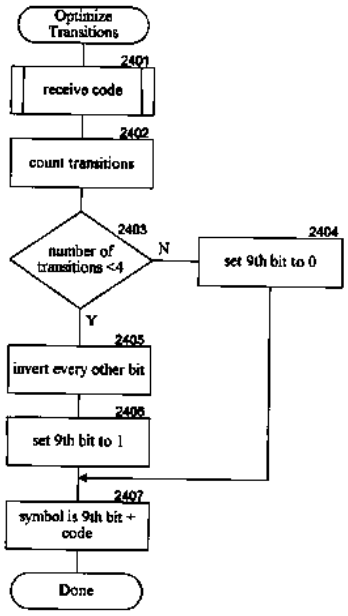
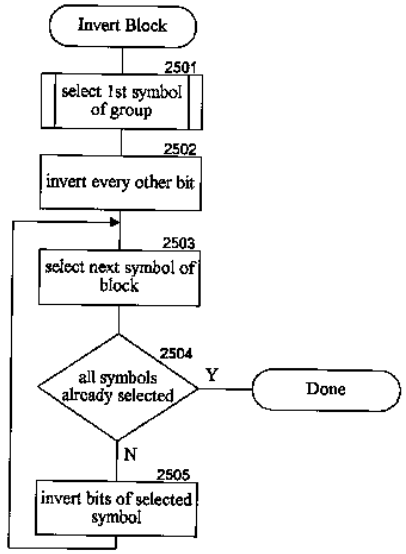


Fig. 21C

Shin ‘450 at Fig. 21C.

		 ***Fig. 23*** Shin '450 at Fig. 23.

		 ***Fig. 24*** Shin '450 at Fig. 24.

		 ***Fig. 25*** Shin '450 at Fig. 25.

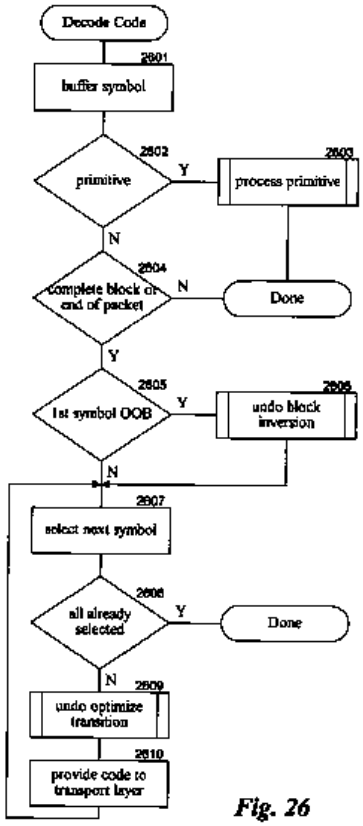
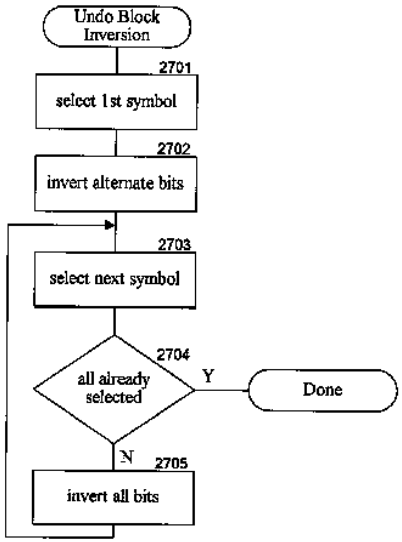


Fig. 26

Shin ‘450 at Fig. 26.

		 ***Fig. 27*** Shin '450 at Fig. 27.

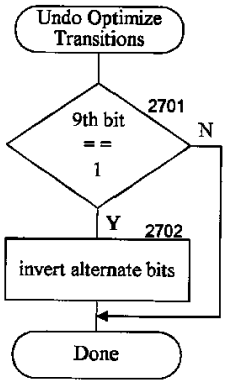
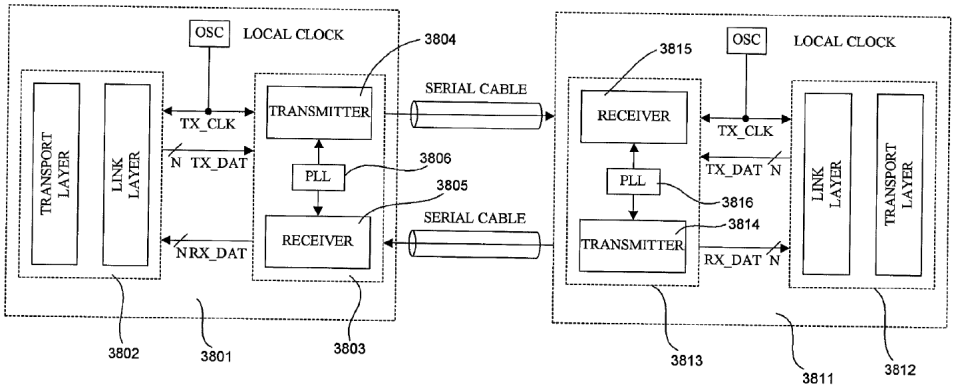


Fig. 28

Shin '450 at Fig. 28.

"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip.
The link layer provides symbols (i.e., N-bit encoded data) to be transmitted to the physical layer via TX_DAT lines."
Shin '450 at [0164-0165].

		 ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 6		
6	The system of claim 2, wherein said at least one of the special characters is an idle character.	Shin '450 discloses, expressly or inherently, the system of claim 2 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 2. "The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control Symbols can be inserted into a Sequence of Symbols generated

		from codes provided by the transport layer. Thus, a communications link can be Simultaneously transmitting and receiving data Symbols, and control Symbols can be inserted for link control." Shin '450 at [0081]. "FIG. 5 is a block diagram illustrating the organization of a data packet and a Segmented data packet in one embodiment. The payload Section of a data packet may include a target address and blocks of data to be Stored at the target address. For example, if the data Store device is a disk drive, then the target address may be a Sector address of the disk drive and the blocks of data may each correspond to a Sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header Section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a Start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload Section is updated to reflect the Starting address at which the remaining blocks of the packet are to be Stored. For example, if packet 510 is segmented after block 504 and the Starting address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth." Shin '450 at [0090].

		"FIG. 7 is a logic diagram illustrating the segmentation of a data packet by the transport layer in one embodiment. In block 701, a component of the transport layer waits for a block of data. In decision block 702, if an XOFF signal has been received, then the component waits for an XON signal in block 703, else the component continues at block 704. In block 704, the component sends the header to the link layer for transmission. In blocks 705-707, the component transmits Successive blocks of the packet and Segments the packet when an XOFF signal is received from the link layer. In block 705, the component transmits the next block of the packet. In decision block 706, if an XOFF signal is pending as indicated by the link layer, then the component continues to segment the packet at block 708, else the component continues at block 707. In decision block 707, if the next block is ready, then the component loops to block 705 to transmit the next block, else the component segments (or ends) the packet at block 708. In block 708, the component transmits the CRC to end the packet and waits for the next block in 701." Shin '450 at [0093].

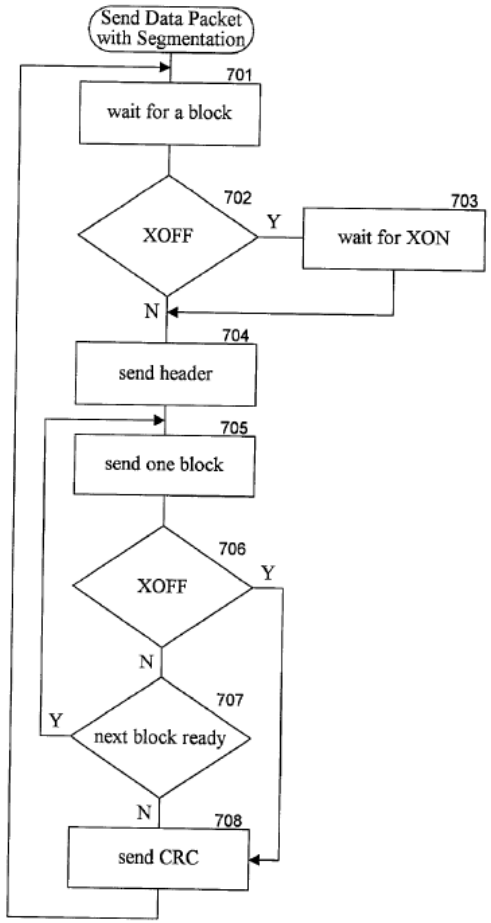
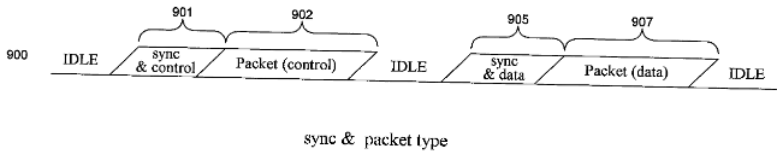
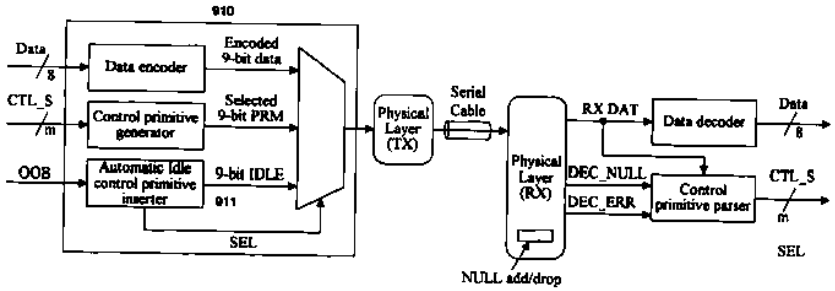


Fig. 7

Shin ‘450 at Fig. 7.

“FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the

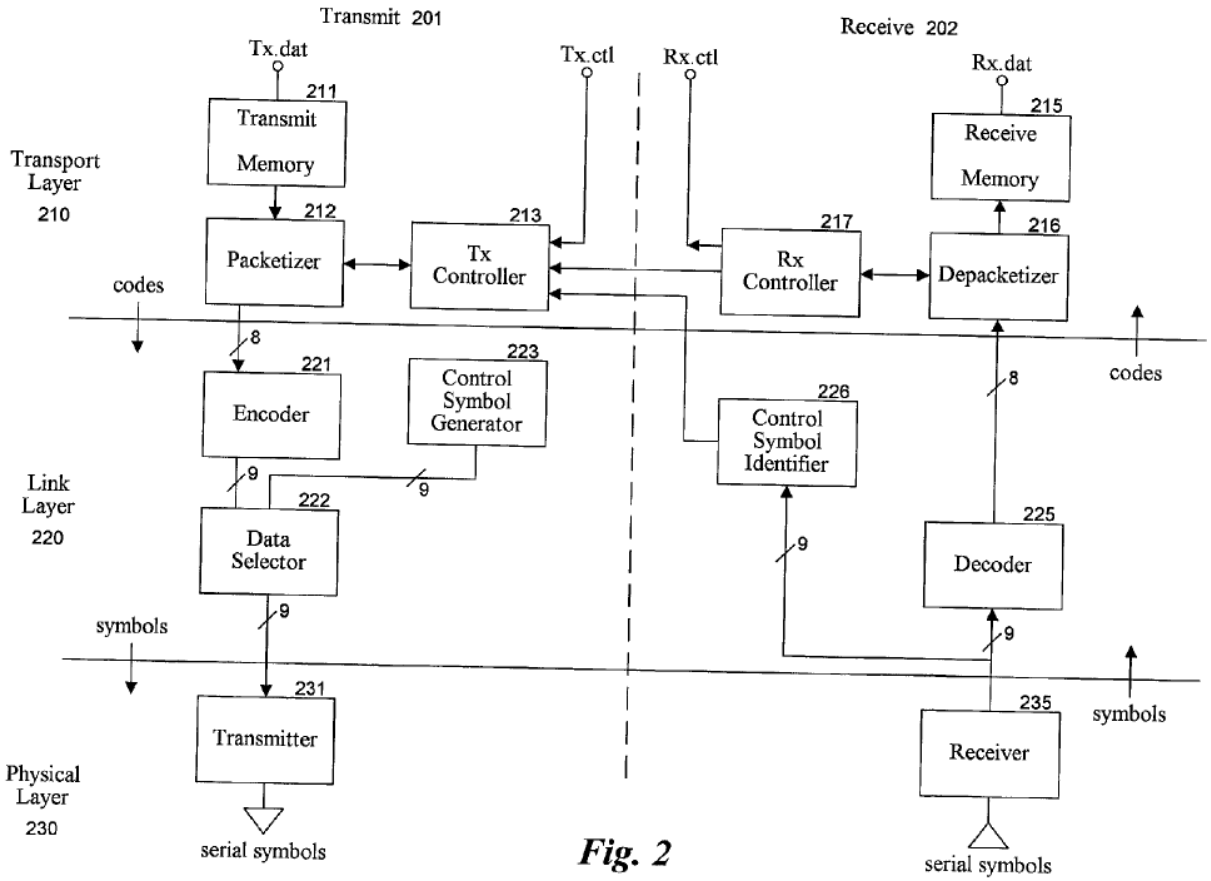
		communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097].  *Fig. 9A* Shin '450 at Fig. 9A. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can

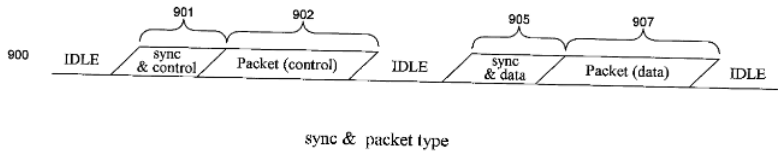
		periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105].  ***Fig. 9C*** Shin '450 at Fig. 9C. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 7		
7	The system of claim 6, wherein the physical and link layer circuitry is configured to perform simplex link flow control by inserting idle characters between Subsequences of	Shin '450 discloses, expressly or inherently, the system of claim 6 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 6. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more

	the code word sequence, where each of the Subsequences is indicative of a different cell of the input words.	references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 23		
23[p]	A communication system, including:	To the extent the preamble is limiting, Shin '450 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[p]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
23(a)	a first endpoint;	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[b]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
23(b)	a second endpoint; and	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[b]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

23(c)	a serial link between the first endpoint and the second endpoint,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[b]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
23(d)	wherein the first endpoint is configured to encode M-bit input words in accordance with a block code to generate a code word sequence of N-bit code words, where N>M,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
23(e)	the code word sequence is indicative of at least one cell of the input words, the input words of each said cell are indicative of application data and control bits,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "FIG. 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, Such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, Such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and Store the codes as packets in the receive memory. The link layer includes transmit components, such as an encoder 221, a data Selector 222, and a control Symbol generator 223, and receive components, Such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for

		receiving and identifying, control Symbols, Synchronization Symbols, timing Symbols, and So on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control Symbols and Synchronization Symbols. The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data. The data Selector Selects Symbols encoded from codes provided by the transport layer or Symbols generated by the control Symbol generator. The data Selector effectively inserts control Symbols and Synchronization Symbols into the Sequence of symbols that are to be transmitted. Various possible encoding techniques for the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate. The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the Serialized Symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link

		was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode." Shin '450 at [0078-0081].  *Fig. 2* Shin '450 at Fig. 2.

		"FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097].  ***Fig. 9A*** Shin '450 at Fig. 9A. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to

		transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer. 1.3 Transmission Order Based on Packet Type In one embodiment, a communications node transmits packets of certain types before packets of other types regardless of the order in which the packets are received or generated by the communications node. For example, a switch may transmit control packets (e.g., command packets, status packets, and message packets) before transmitting data packets. The transmitting of control packets before data packets may help ensure that the control packets are not unnecessarily delayed by data packets, which may have a tendency to be quite large. For example, a command packet requesting a read from a data store device may be transmitted before a data packet even through the control packet was received after the data packet. The data store device can thus start processing the read request without having to wait until the data packet is transmitted. A communications node may store control packets and data packets in separate areas of the packet memory and only select packets from the data packet area when the control packet area is empty. Alternatively, the communications node may use various algorithms to select control or data packets to be transmitted. For example, the algorithm may select a data packet that has been in the packet memory for certain amount of time even though there may be a control packet in the control area. In this way, a sequence of many control packets will not delay the data packet more than that certain amount of time. One skilled in the art will appreciate that there may be multiple packet types with different transmission orders. For example, a status packet might be transmitted before a command packet, and a command packet might be transmitted before a data packet.

		FIG. 10 is a block diagram illustrating an organization of a packet memory in one embodiment. The transmit packet memory 211 may include control queue 1010 and data queue 1020. The control queue contains the control packets 1011, and the data queue contains the data packets 1021. Packets to be transmitted are stored either in the control queue or the data queue based on packet type (which may be encoded in a synchronization primitive). When a transmitting communications node is ready to transmit the next packet, it retrieves the next packet from the control queue. If the control queue is empty, then the transmitting communications node retrieves the next packet from the data queue. FIG. 11 is a logic diagram illustrating a process of storing packets in a transmit memory in one embodiment. Similar logic can be used to store packets in the receive memory of a communications node. In block 1101, a component of the transport layer receives the next packet from an upper layer. In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a synchronization primitive encoded with the packet type. When the link layer detects a synchronization primitive designating packet type, it signals the transport layer so that the type of packet can be used when the packet is stored in the receive memory, retrieved from the receive memory, stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component stores the packet in the data queue. The component then retrieves the next packet. FIG. 12 is a logic diagram illustrating the transport layer processing of packets stored in the packet memory in one embodiment. In decision block 1201, if the control queue is empty, then the component continues to block 1203, else the component retrieves a control packet from the control queue in block 1202 and continues at block 1205. In decision block 1203, if the data queue is empty, then the component again checks for a packet in the control queue, else the component retrieves a packet from the data queue in block 1204 and continues at block 1205. In blocks 1205-1207, the component selects the codes of the retrieved packet. In block 1205, the component selects the next code of the retrieved packet. In decision block 1206, if all codes have already been selected, then the component continues at block 1201 to check for the next packet,

		else the component continues at block 1207. In block 1207, the component provides the selected code to the link layer and then continues at block 1205 to select the next code of the packet. 1.4 Packet Preemption In one embodiment, a communications node may preempt or interrupt the transmission of a packet when a packet with a higher priority is to be transmitted on the same communications link. Packet preemption helps ensure that data store devices receive control packets as soon as possible without being slowed by network congestion as a result of data packets. In particular, the transmission of a data packet, which may be large, may be preempted so that a control packet, which is typically small, may be transmitted. When a data packet is to be preempted, the transport layer of the communications node stops providing the codes of the data packet to the link layer, signals the link layer to transmit a preempt primitive, and then starts providing the code of the control packet to the link layer for transmission as a preempting packet. When the preempting packet is has been completely transmitted, the transport layer of the communications node signals the link layer to transmit a continue primitive and then resumes providing the remainder of the codes of the data packet to the link layer. The link layer of the receiving communications node detects the preempt primitive while it is receiving the codes of the data packet and signals its transport layer. The transport layer then starts storing the subsequent codes as a control packet. When the link layer detects the continue primitive, it signals the transport layer, which continues receiving the preempted data packet. The preempt and continue primitives, which are control primitives, serve to delimit transmission of a preempting packet. One skilled in the art will appreciate that packet preemption could be nested to any level. For example, a status packet might preempt a command packet that already preempted a data packet. FIG. 13 is a diagram illustrating the preemption of a packet in one embodiment. Serial link content diagram 1300 illustrates a data packet that is preempted by a control packet. Initially, the transmitting communications node transmits the first portion of data packet 1301. When the packet is to be preempted, the communications node then transmits the preempt primitive 1302. After transmitting the preempt primitive, the transmitting communications node transmits the preempting control packet 1303. After the control packet is transmitted, the communications node

transmits the continue primitive 1304, and then resumes transmitting the remainder of the preempted data packet 1305."

Shin '450 at [0105-0113].

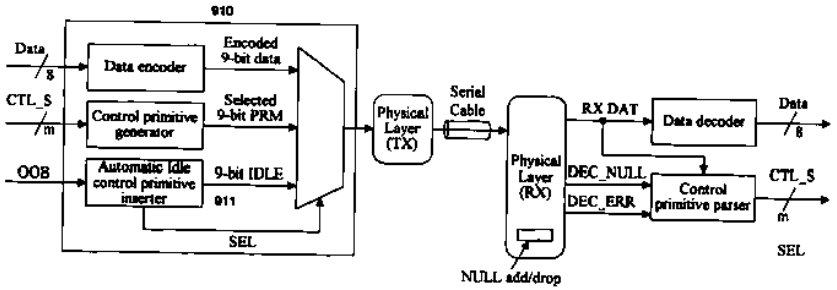


Fig. 9C

Shin '450 at Fig. 9C.

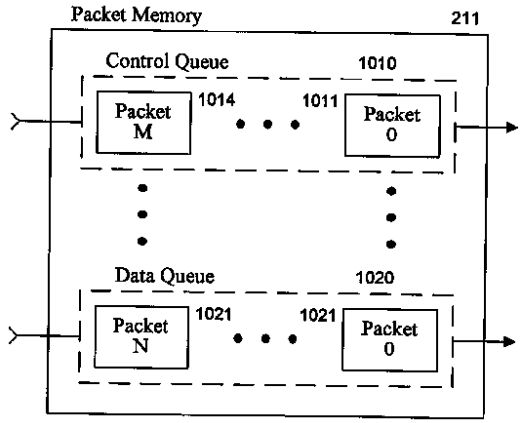
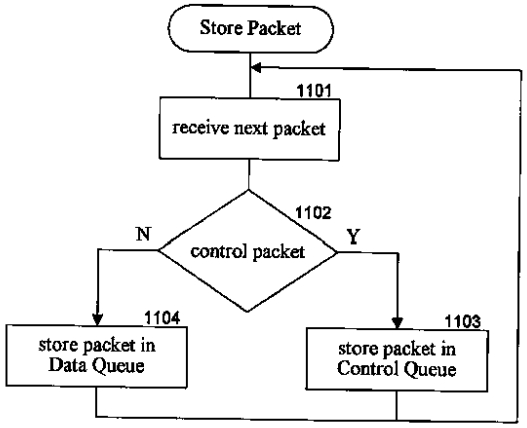


Fig. 10

Shin '450 at Fig. 10.

		 ***Fig. 11*** Shin '450 at Fig. 11.

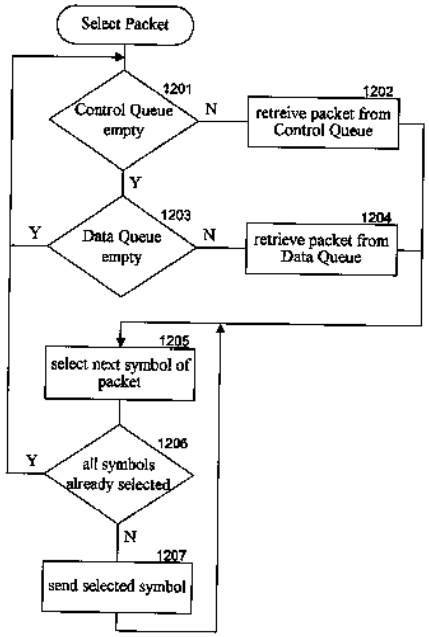


Fig. 12

Shin '450 at Fig. 12.

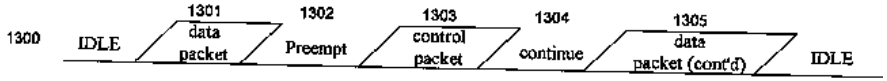


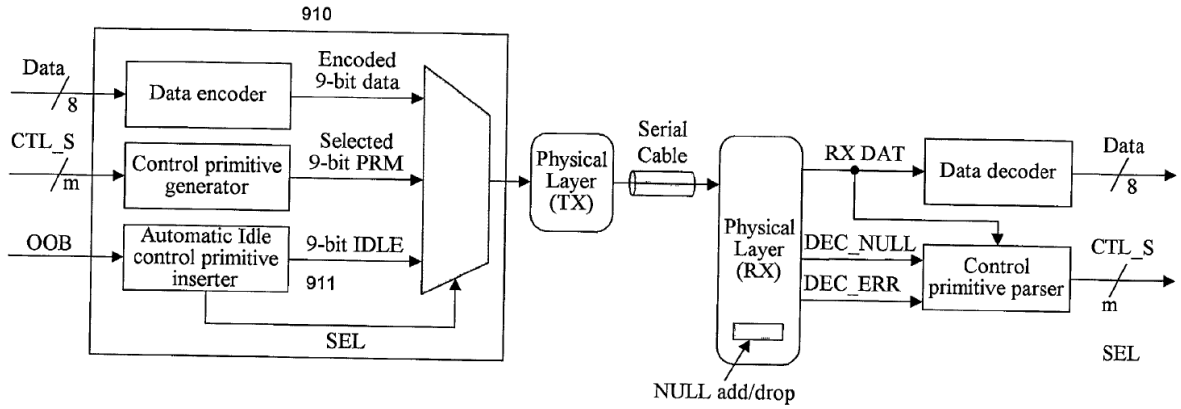
Fig. 13

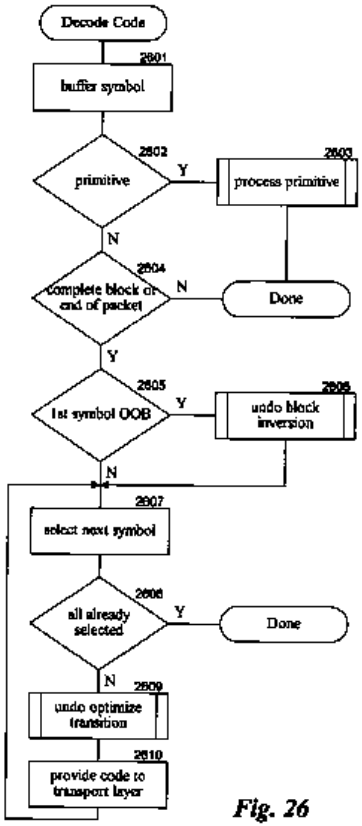
Shin '450 at Fig. 13.

To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

23(f)	the control bits have multiple levels of communication protocol functionality, and	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "In one embodiment, the serial communications architecture defines multiple primitives to operate as Synchronization signals. A Synchronization Signal is typically used by the physical layer to help ensure correct alignment of Symbols. A transmitting communications node periodically transmits Synchronization primitives So that the receiving communications node can properly align with that Synchronization primitive. When a communications node receives a Synchronization primitive, it knows that the primitive is correctly aligned on a Symbol boundary. The use of multiple Synchronization primitives allows for encoding packet type within a Synchronization primitive. In particular, the transport layer provides the packet type to the link layer. The link layer can then transmit a Synchronization primitive that indicates packet type immediately before the packet itself. The receiving communications node can take the appropriate action based on the packet type encoded in the Synchronization primitive without having to parse the packet header. Indeed, the packet header may not need to Separately include the packet type. The use of a Synchronization primitive with encoded packet type may be well adapted to use in an environment where the transmission time of a packet through the Switching network may be long relative to the time needed to Store the packet at the data Store device. For example, the time to transmit a packet through the Switching network may be longer than the time needed to Store the data of the packet in a memory-based data Store device. The rapid detection of packet type through a Synchronization primitive, rather than through a packet header, can reduce the processing time of a Switch. Also, when a Synchronization primitive encodes the packet type, then the link layer, rather than the transport layer, can detect packet type, which can enhance the Overall processing Speed." Shin '450 at [0096]. "FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals

		the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "After the packet has been transmitted, the link layer of the transmitting communications node Starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the Synchronization primitive encoded with packet type to align its Symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper

		Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105].  ***Fig. 9C*** Shin '450 at Fig. 9C. "FIG. 26 is a logic diagram illustrating transition control and Selective block inversion decoding in one embodiment. The component of the link layer is provided with one symbol at a time by the physical layer. In block 2601, the component stores the symbol in a buffer. In decision block 2602, if the buffer contains a primitive, then the component continues at block 2603 to process the primitive, else the component continues at block 2604. In block 2604, if the buffer contains a complete block, then the component continues at block 2605, else the component waits for the next symbol. In decision block 2605, if the first symbol in the buffer is an out-of-band symbol, then the transmitting communications node inverted the block and the component continues at

		block 2606, else the component continues at block 2607. In block 2606, the component undoes the block inversion of the block." Shin '450 at [0143].  *Fig. 26* Shin '450 at Fig. 26.

		"Because of the way memory is typically accessed, the physical layer, link layer, and transport layer might be Simplified as compared to the layers needed in a more general data Store device, Such as a disk drive. Each port of a multiport memory device is typically directly connected to a host. In Such a case, packets do not need to specify a Source and a destination and the headers are thus simplified. In addition, packet types can be encoded in Synchronization primitives to further simplify the packet header. The transport layer of a port in a multiport memory device can be Simplified or eliminated because (1) routing to another device is not needed, (2) minimal or no parsing of the header may be needed, and (3) preemption and priority ordering of packets may not be needed. In addition, the link layer may be simplified by the use of physical layer DC-balancing, rather than the use of the selective block inversion to achieve DC-balance. Physical layer DC-balancing can be used with a multiport memory device because the distance between the host and the multiport memory device is typically relatively short." Shin '450 at [0148]. "The handling of an underrun can also be costly and complex. These underrun and overrun conditions were typically handled at the link layer. These complexities and costs may, however, be avoided by the physical layer of a receiving communications node periodically inserting or removing NULL symbols or NULL primitives from the received Stream of Symbols at a rate Sufficient to compensate for variations in clock frequencies." Shin '450 at [0163]. "FIG. 39B is a block diagram illustrating resolution of an asynchronous clock boundary in the physical layer in one embodiment. The clock and data recover ('CDR') processing of the physical layer 3950 provides to the link layer RX DAT lines that are synchronized to the local clock. Thus, the asynchronous boundary at the link layer along with the needed logic to resolve the boundary is avoided in the link layer. The CDR processing also provides a 1-bit control signal (DET NULL) that indicates a NULL symbol is provided in RX DAT (i.e., to inform the link layer that a primitive has been received) and a 1-bit control signal (DER ERR) that indicates an error in the physical layer data recovery." Shin '450 at [0168].

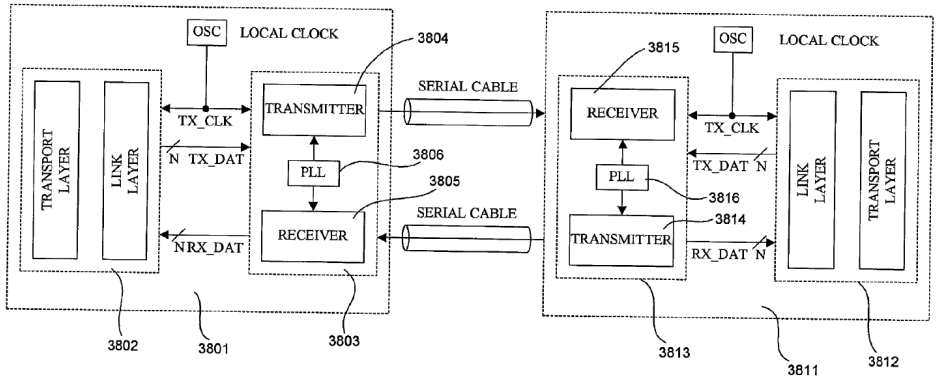


Fig. 38A

Shin '450 at Fig. 38A.

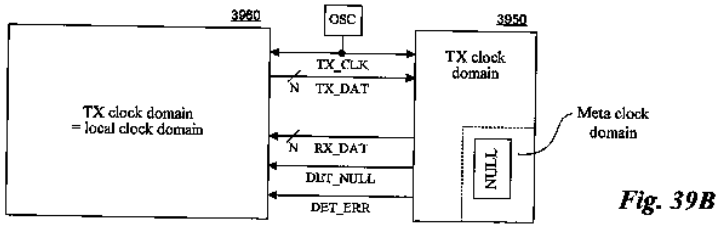
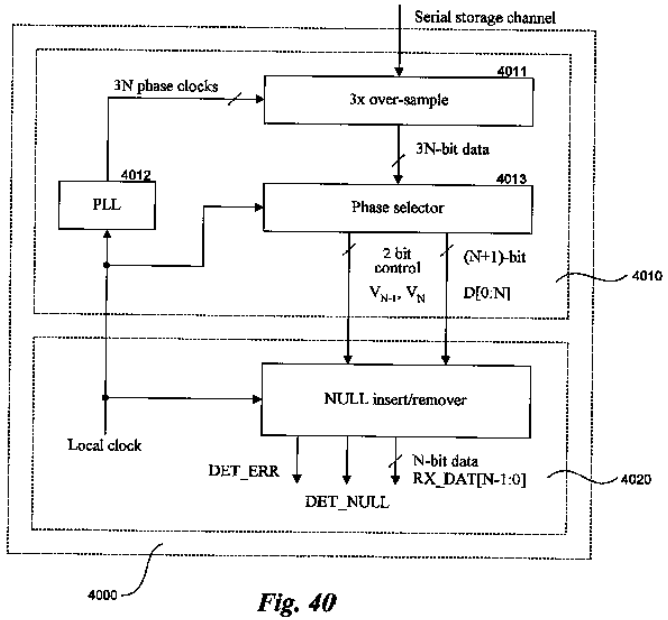


Fig. 39B

Shin '450 at Fig. 39B.

"FIG. 40 is a block diagram illustrating NULL insertion and deletion at the physical layer in one embodiment. Sampler 4010 in one embodiment corresponds to the over sampler 4011, digital phase lock loop 4012, and phase selector 4013 described in U.S. Pat. No. 6,229,859, entitled "System and Method for High-Speed, Synchronized Data Communication." The sampler outputs N+1 bits (where N is the number of bits in a symbol) of data lines DO:N) and two valid bits VN-1 and VIN). The sampler identifies a stream of data bits that are received and provides those data bits in data lines DO:N). The valid bits indicate whether DN-1 and DIN contain valid data (e.g., VIN-1=1 indicates that DN-1) is valid). The data bits provided by the sampler are not, however, frame (i.e., Symbol) aligned; that is, DO) is not necessarily (and more often than not would not

		be) the first bit in a symbol. The valid bits indicate whether an overrun or underrun condition has occurred. An overrun occurs as a result of the transmitter's clock frequency being faster than the receivers, and an underrun occurs as a result of the transmitter's clock frequency being slower than the receiver's. Nominally, N data bits are provided by the Sampler every Sample interval. In Such a case DN-1 is valid, but DN) is invalid. If, however, there is an overrun, then the sampler provides N+1 data bits; that is, DN-1 and DN) are both valid. If there is an underrun, then the sampler provides N-1 data bits; that is, DN-1 and DIN are both invalid. The data bits and the valid bits are supplied to a frame aligner 4020. The frame aligner not only aligns the frames, but also inserts and removes NULL symbols to adjust for variations in the transmitting and receiving clock frequencies." Shin '450 at [0169].  ***Fig. 40*** Shin '450 at Fig. 40.

		To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
23(g)	the first endpoint is configured to transmit encoded data including the code words of the code word sequence over the link to the second endpoint.	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: "FIG. 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, Such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, Such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and Store the codes as packets in the receive memory. The link layer includes transmit components, such as an encoder 221, a data Selector 222, and a control Symbol generator 223, and receive components, Such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for receiving and identifying, control Symbols, Synchronization Symbols, timing Symbols, and So on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control Symbols and Synchronization Symbols. The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data. The data Selector Selects Symbols encoded from codes provided by the transport layer or Symbols generated by the control Symbol generator. The data Selector effectively inserts control Symbols and Synchronization Symbols into the Sequence of symbols that are to be transmitted. Various possible encoding techniques for

		the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate. The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the Serialized Symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode." Shin '450 at [0078-0081].

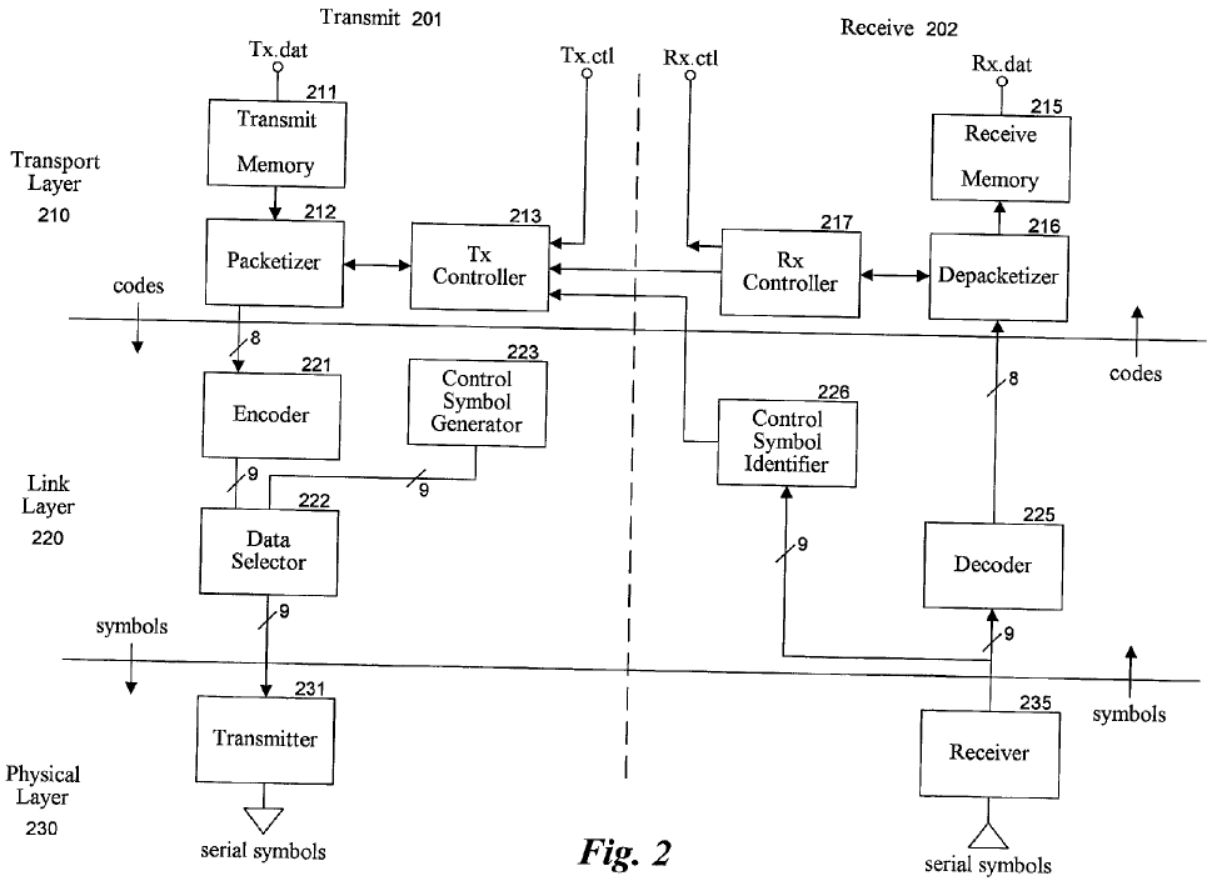
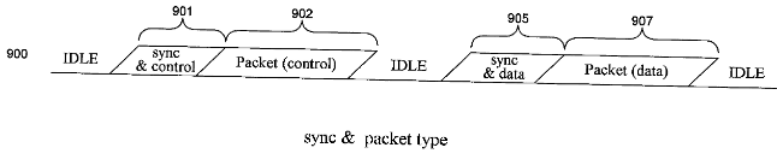


Fig. 2

Shin '450 at Fig. 2.

"FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command,

		status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097].  *Fig. 9A* Shin '450 at Fig. 9A. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper

		Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer. 1.3 Transmission Order Based on Packet Type In one embodiment, a communications node transmits packets of certain types before packets of other types regardless of the order in which the packets are received or generated by the communications node. For example, a switch may transmit control packets (e.g., command packets, status packets, and message packets) before transmitting data packets. The transmitting of control packets before data packets may help ensure that the control packets are not unnecessarily delayed by data packets, which may have a tendency to be quite large. For example, a command packet requesting a read from a data store device may be transmitted before a data packet even through the control packet was received after the data packet. The data store device can thus start processing the read request without having to wait until the data packet is transmitted. A communications node may store control packets and data packets in separate areas of the packet memory and only select packets from the data packet area when the control packet area is empty. Alternatively, the communications node may use various algorithms to select control or data packets to be transmitted. For example, the algorithm may select a data packet that has been in the packet memory for certain amount of time even though there may be a control packet in the control area. In this way, a sequence of many control packets will not delay the data packet more than that certain amount of time. One skilled in the art will appreciate that there may be multiple packet types with different transmission orders. For example, a status packet might be transmitted before a command packet, and a command packet might be transmitted before a data packet. FIG. 10 is a block diagram illustrating an organization of a packet memory in one embodiment. The transmit packet memory 211 may include control queue 1010 and data queue 1020. The control queue contains the control packets 1011, and the data queue contains the data packets 1021. Packets to be transmitted are stored either in the control queue or the data queue based on packet type (which may be encoded in a synchronization primitive). When a transmitting communications node is ready to transmit the next packet, it retrieves the next packet from the

		control queue. If the control queue is empty, then the transmitting communications node retrieves the next packet from the data queue. FIG. 11 is a logic diagram illustrating a process of storing packets in a transmit memory in one embodiment. Similar logic can be used to store packets in the receive memory of a communications node. In block 1101, a component of the transport layer receives the next packet from an upper layer. In decision block 1102, if the received packet is a control packet, then the component continues at block 1103, else the component continues at block 1104. The component may determine the type of the packet either from the type field of the packet header or, when the packet is received from another communications node, from a synchronization primitive encoded with the packet type. When the link layer detects a synchronization primitive designating packet type, it signals the transport layer so that the type of packet can be used when the packet is stored in the receive memory, retrieved from the receive memory, stored in the transmit memory, and retrieved from the transmit memory. In block 1103, the component stores the packet in the control queue. In block 1104, the component stores the packet in the data queue. The component then retrieves the next packet. FIG. 12 is a logic diagram illustrating the transport layer processing of packets stored in the packet memory in one embodiment. In decision block 1201, if the control queue is empty, then the component continues to block 1203, else the component retrieves a control packet from the control queue in block 1202 and continues at block 1205. In decision block 1203, if the data queue is empty, then the component again checks for a packet in the control queue, else the component retrieves a packet from the data queue in block 1204 and continues at block 1205. In blocks 1205-1207, the component selects the codes of the retrieved packet. In block 1205, the component selects the next code of the retrieved packet. In decision block 1206, if all codes have already been selected, then the component continues at block 1201 to check for the next packet, else the component continues at block 1207. In block 1207, the component provides the selected code to the link layer and then continues at block 1205 to select the next code of the packet. 1.4 Packet Preemption In one embodiment, a communications node may preempt or interrupt the transmission of a packet when a packet with a higher priority is to be transmitted on the same communications link.

		Packet preemption helps ensure that data store devices receive control packets as soon as possible without being slowed by network congestion as a result of data packets. In particular, the transmission of a data packet, which may be large, may be preempted so that a control packet, which is typically small, may be transmitted. When a data packet is to be preempted, the transport layer of the communications node stops providing the codes of the data packet to the link layer, signals the link layer to transmit a preempt primitive, and then starts providing the code of the control packet to the link layer for transmission as a preempting packet. When the preempting packet is has been completely transmitted, the transport layer of the communications node signals the link layer to transmit a continue primitive and then resumes providing the remainder of the codes of the data packet to the link layer. The link layer of the receiving communications node detects the preempt primitive while it is receiving the codes of the data packet and signals its transport layer. The transport layer then starts storing the subsequent codes as a control packet. When the link layer detects the continue primitive, it signals the transport layer, which continues receiving the preempted data packet. The preempt and continue primitives, which are control primitives, serve to delimit transmission of a preempting packet. One skilled in the art will appreciate that packet preemption could be nested to any level. For example, a status packet might preempt a command packet that already preempted a data packet. FIG. 13 is a diagram illustrating the preemption of a packet in one embodiment. Serial link content diagram 1300 illustrates a data packet that is preempted by a control packet. Initially, the transmitting communications node transmits the first portion of data packet 1301. When the packet is to be preempted, the communications node then transmits the preempt primitive 1302. After transmitting the preempt primitive, the transmitting communications node transmits the preempting control packet 1303. After the control packet is transmitted, the communications node transmits the continue primitive 1304, and then resumes transmitting the remainder of the preempted data packet 1305." Shin '450 at [0105-0113].

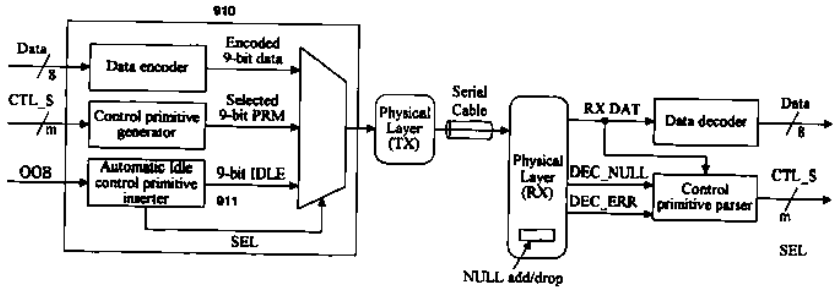


Fig. 9C

Shin ‘450 at Fig. 9C.

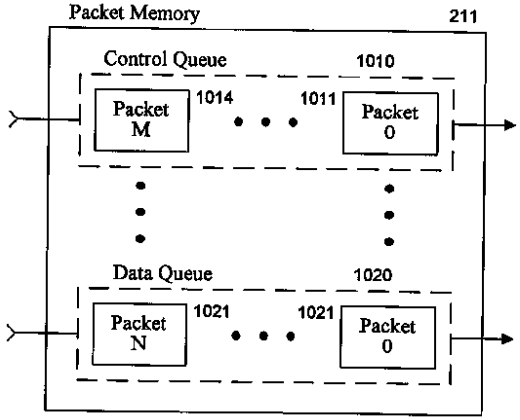
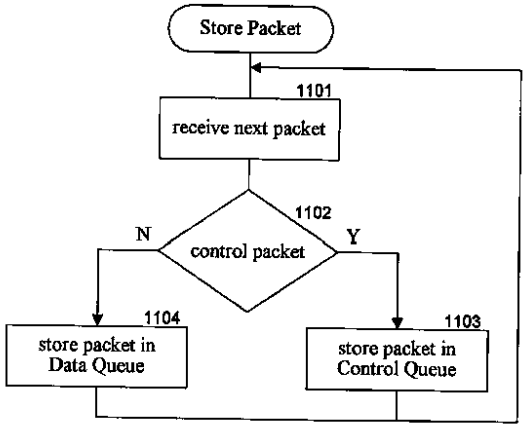


Fig. 10

Shin ‘450 at Fig. 10.

		 ***Fig. 11*** Shin '450 at Fig. 11.

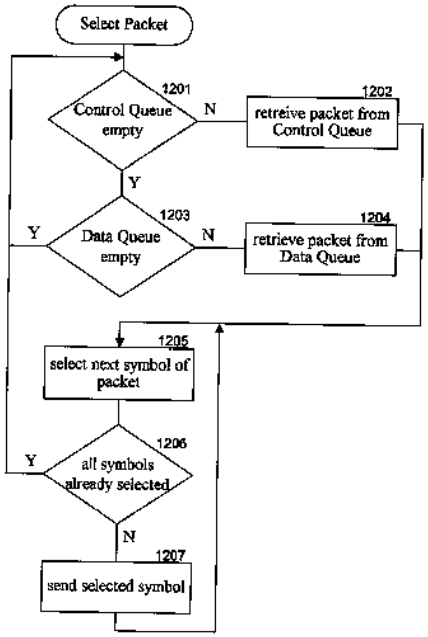


Fig. 12

Shin '450 at Fig. 12.

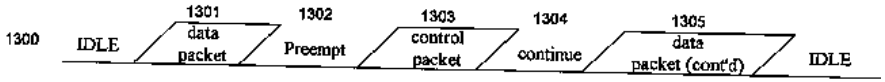
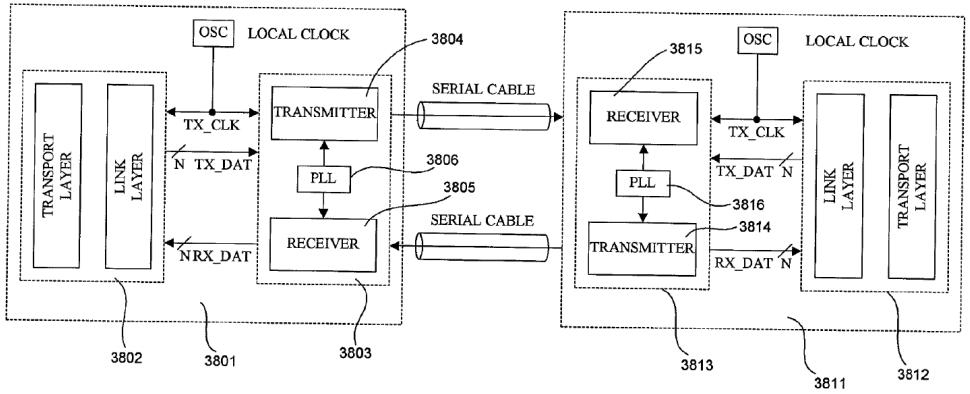


Fig. 13

Shin '450 at Fig. 13.

"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in

		a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip." Shin '450 at [0164].  ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 25		
25	The system of claim 23, wherein the block code is specified by a line code that also specifies special characters, the encoded data are a sequence of at least one of the special characters and the code	Shin '450 discloses, expressly or inherently, the system of claim 23 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 23. "FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not

	words of the code word sequence, and none of the special characters of the encoded data matches a bit sequence of the code word sequence.	encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command, status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers. As described above, the primitives are pairs of out-of-band symbols. (In the following, a symbol is assumed to have nine bits.) In one embodiment, when the in-band symbols are transition maximized, then the symbols of the control primitives have three transitions each and the symbols of the synchronization primitives have two transitions each. When the in-band symbols are transition minimized, then the symbols of the control primitives have five transitions each and the synchronization primitives have one symbol with five transitions and another symbol with seven transitions. Table 1 illustrates control primitives in one embodiment when the in-band symbols are transition maximized. Each control primitive comprises two symbols in which the first symbol is a polarity inversion of the second symbol. As a result, the disparity (described below) of each control primitive is 0. The control primitives such as XON, XOFF, preempt, and continue are selected from this table of control primitives. TABLE 1 Control primitives in transition maximization mode 0. 000010111-111101000 1. 000011011-111100100

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 338

		2. 000011101-111100010 3. 000100111-111011000 4. 000110011-111001100 5. 000111001-111000110 6. 001000111-110111000 7. 001100011-110011100 8. 001110001-110001110 9. 010000111-101111000 10. 011000011-100111100 11. 011100001-100011110 12. 100001110-011110001 13. 100011100-011100011 14. 100111000-011000111 15. 101110000-010001111 16. 110000110-001111001 17. 110001100-001110011 18. 110011000-001100111 19. 110110000-001001111 20. 111000010-000111101 21. 111000100-000111011 22. 111001000-000110111

		23. 111010000-000101111 Table 2 illustrates control primitives in one embodiment when the in-band symbols are transition minimized. TABLE 2 Control primitives in transition minimization mode 0. 000010101-111101010 1. 000100101-111011010 2. 000101001-111010110 3. 000101011-111010100 4. 000101101-111010010 5. 000110101-111001010 6. 001000101-110111010 7. 001001001-110110110 8. 001001011-110110100 9. 001001101-110110010 10. 001010001-110101110 11. 001010011-110101100 12. 001011001-110100110 13. 001100101-110011010 14. 001101001-110010110 15. 010000101-101111010

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 340

		16. 010001001-101110110 17. 010001011-101110100 18 010001101-101110010 19. 010010001-101101110 20. 010010011-101101100 21. 010011001-101100110 22. 010100001-101011110 23. 010100011-101011100 24. 010110001-101001110 25. 011000101-100111010 26. 011001001-100110110 27. 011010001-100101110 28. 100001010-011110101 29. 100010010-011101101 30. 100010100-011101011 31. 100010110-011101001 32. 100011010-011100101 33. 100100010-011011101 34. 100100100-011011011 35. 100100110-011011001 36. 100101000-011010111

		37. 100101100-011010011 38. 100110010-011001101 39. 1001101000-11001011 40. 101000010-010111101 41. 101000100-010111011 42. 101000110-010111001 43. 101001000-010110111 44. 101001100-010110011 45. 101010000-010101111 46. 101011000-010100111 47. 101100010-010011101 48. 101100100-010011011 49. 101101000-010010111 50. 110001010-001110101 51. 110010010-001101101 52. 110010100-001101011 53. 110100010-001011101 54. 110100100-001011011 55. 110101000-001010111 The synchronization primitives are distinct from the control primitives. The synchronization primitives are selected to have the characteristic that when two synchronization primitives are transmitted sequentially the receiving device can unambiguously identify the synchronization

		primitives regardless of what is transmitted before or after the synchronization primitives. The synchronization primitives have a unique number of transitions that is not found in any control primitive or in-band symbol. In one embodiment, the synchronization primitive can be detected by looking for a sequence of symbols with that number of transitions. In one embodiment, the synchronization primitives are selected to start with a falling edge (i.e., "10"), a rising edge (i.e., "01"), a high level (i.e., "11"), or a low level (i.e., "00"). The selection of the start of the synchronization primitives is referred to as the "synchronization detection mode." Table 3 contains synchronization primitives in transition maximization mode that start with a falling edge and a rising edge. Each symbol in Table 3 contains two transitions resulting in synchronization primitives with four transitions. Table 4 contains synchronization primitives in transition minimization mode that start with a low level and a high level. Each synchronization primitive in Table 4 has 13 transitions. The high-level and low-level synchronization primitives have five transitions in one symbol, seven transitions in the other symbol, and one transition from their first to second symbol. TABLE 3 Falling Edge Rising Edge 0 100000001-100111111 011000000-011111110 1 100000011-100011111 011100000-011111100 2 100000111-100001111 011110000-011111000 3 100001111-100000111 011111000-011110000 4 100011111-100000011 011111100-011100000 5 100111111-100000001 011111110-011000000 TABLE 4 High Level Low Level 0 110101000-110101010 001010101-001010111

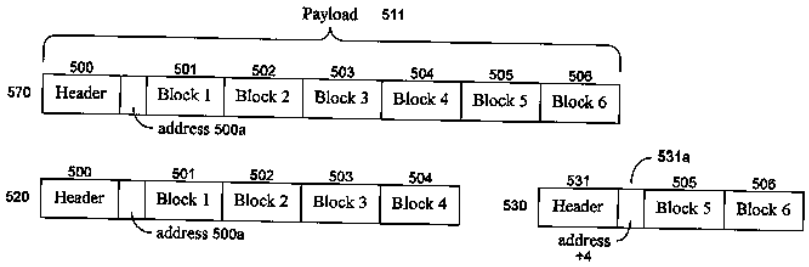
Universal Connectivity Technologies Inc.
Ex. 2005 - Page 343

		1 110100010-110101010 001010101-001011101 2 110001010-110101010 001010101-001110101 3 110100100-110101010 001010101-001011011 4 110010100-110101010 001010101-001101011 5 110101010-110101000 001010111-001010101 6 110101010-110100010 001011101-001010101 7 110101010-110001010 001110101-001010101 8 110101010-110100100 001011011-001010101 9 110101010-110010100 001101011-001010101 Table 5 lists the transition distribution of the low and high polarity symbols onization primitives. TABLE 5 Total # of Transi-tions Sync Detect Mode / Transition Distribution in Low Polarity / Transition Distribution in High Polarity / in a Sync Primitive Falling edge (“10”): one “10” and one “01” / one “10” and one “01” / 4 Risin edge (“01”): one “01” and one “10” / one “01” and one “10” / 4 High level: one “11” and two “00” / one “11” and no “00” / 13

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 344

		("11") Low level one "00" and no "11" one "00" and two "11" 13 ("00") In one embodiment, the synchronization primitives are detected by buffering three symbols (e.g., 27 bits). The synchronization primitives are selected so that any time the buffer has exactly three of the synchronization detection mode bits (e.g., "10" for falling edge) that are each 9 bits apart then the bits are at the beginning of a synchronization symbol. The bit buffer contains 27 bits, A[8:0], B[8:0], and C[8:0], in which bit A[8] was received first and bit C[0] was received last. In this example, the content of bits A[6]:B[7] represent synchronization symbol "100000001" and B[6]:C[7] represent synchronization symbol "100111111." The starting points of the synchronization symbols ("synchronization markers") are A[6], B[6], and C[6]." Shin '450 at [0097-0104]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 31		
31	The system of claim 23, wherein each of the first endpoint and the second endpoint is a transceiver, and the second endpoint is configured to generate additional encoded data in response to input words in accordance with the line code and to transmit the encoded data over the link to the first endpoint.	Shin '450 discloses, expressly or inherently, the system of claim 23 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 23. "The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control Symbols can be inserted into a Sequence of Symbols generated

		from codes provided by the transport layer. Thus, a communications link can be Simultaneously transmitting and receiving data Symbols, and control Symbols can be inserted for link control." Shin '450 at [0081]. "FIG. 5 is a block diagram illustrating the organization of a data packet and a Segmented data packet in one embodiment. The payload Section of a data packet may include a target address and blocks of data to be Stored at the target address. For example, if the data Store device is a disk drive, then the target address may be a Sector address of the disk drive and the blocks of data may each correspond to a Sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header Section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a Start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload Section is updated to reflect the Starting address at which the remaining blocks of the packet are to be Stored. For example, if packet 510 is segmented after block 504 and the Starting address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth." Shin '450 at [0090].

		 ***Fig. 5*** Shin '450 at Fig. 5. "FIG. 7 is a logic diagram illustrating the segmentation of a data packet by the transport layer in one embodiment. In block 701, a component of the transport layer waits for a block of data. In decision block 702, if an XOFF signal has been received, then the component waits for an XON signal in block 703, else the component continues at block 704. In block 704, the component sends the header to the link layer for transmission. In blocks 705-707, the component transmits Successive blocks of the packet and Segments the packet when an XOFF signal is received from the link layer. In block 705, the component transmits the next block of the packet. In decision block 706, if an XOFF signal is pending as indicated by the link layer, then the component continues to segment the packet at block 708, else the component continues at block 707. In decision block 707, if the next block is ready, then the component loops to block 705 to transmit the next block, else the component segments (or ends) the packet at block 708. In block 708, the component transmits the CRC to end the packet and waits for the next block in 701." Shin '450 at [0093].

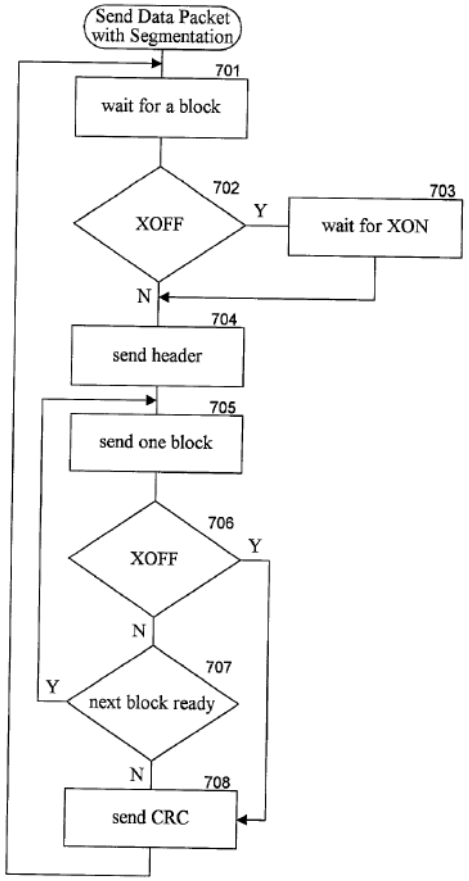


Fig. 7

Shin '450 at Fig. 7.

"After the packet has been transmitted, the link layer of the transmitting communications node Starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is

		transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the Synchronization primitive encoded with packet type to align its Symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 53		
53[p]	A receiver for receiving encoded data that have propagated over a serial link, the encoded data having been generated in accordance with a line code, said receiver including:	To the extent the preamble is limiting, Shin '450 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*: "A serial communications architecture for communicating between hosts and data store devices. The Storage Link architecture is specially adapted to support communications between multiple hosts and storage devices via a switch network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at Abstract. "The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at [0071].

		"FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer. The hosts and data store devices have an upper layer that communicate to each other via transactions. When transmitting data, the upper layer provides the data for the transaction to the transport layer. The transport layer receives the data of the transaction and generates packets (i.e., packetizes the data) for transmission. The transport layer then provides each code (e.g., each byte) of the packets to the link layer for transmission to the destination. When receiving data, the transport layer receives the codes of transaction from the link layer and identifies the packets. The transport layer then combines the data of the packets of the transaction (i.e., depacketizes the data) and provides the data of the transaction to the upper layer. Each host and data store device may include an application upper layer that provides the data of a transaction to the transport layer to be transmitted to a destination and receives the data of a transaction from the transport layer that was transmitted by a source. Each packet includes a header section and a payload section. The header section identifies the source and destination and a packet type (e.g., data or command). Each switch may include a communications interface for each port of the switch. Each port may be connected to a serial communications link comprising a receive and transmit link. The switches and their interconnecting communications links form the switching network. The transport layer of a switch may not packetize and depacketize the data, rather it may direct packets received via one port to be transmitted via another port to affect the routing of the packets from the source to the destination as indicated in the header section. The link layer encodes the codes to be transmitted via its communications link into symbols and decodes symbols received via its communications link into codes. The link layer receives codes to

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 350

		be transmitted from the transport layer, encodes those codes into symbols, and provides those symbols to the physical layer. The link layer also receives symbols from the physical layer, decodes those symbols into codes, and provides those codes to the transport layer. The encoding may include mapping the codes to symbols to optimize bit transitions and to ensure DC-balance. The physical layer receives the symbols from the link layer, serializes the symbols, and transmits the serialized symbols via the communications link. The physical layer receives serialized symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. FIG. 2 is a block diagram illustrating components of the transport layer, link layer, and physical layer in one embodiment. Each layer includes transmit components 201 and receive components 202. The transport layer includes transmit components, Such as a transmit memory 211, a packetizer 212, and a transmit controller 213, and receive components, Such as a receive memory 215, a depacketizer 216, and a receive controller 217. The data of the transaction to be transmitted is stored in the transmit memory. The transmit controller controls the packetizer to retrieve data of a transaction from the transmit memory, packetize the data, and provide each code of the packets to the link layer. The receive controller controls the depacketizer to receive codes provided by the link layer, identify the packets, and Store the codes as packets in the receive memory. The link layer includes transmit components, such as an encoder 221, a data Selector 222, and a control Symbol generator 223, and receive components, Such as a decoder 225 and a control symbol identifier 226. The link layer may be responsible for generating and transmitting and for receiving and identifying, control Symbols, Synchronization Symbols, timing Symbols, and So on, as described below in more detail. In one embodiment, however, the physical layer is responsible for detecting control Symbols and Synchronization Symbols. The transport layer may indicate to the link layer when to transmit control Symbols, and the link layer may indicate to the transport layer when control Symbols are received. For example, the transmit layer may notify the link layer when the receive memory is full. In Such a case, the link layer may transmit a control symbol (e.g., XOFF) notifying the other end of the communications link not to transmit any more data. When Such transmitted control symbol is received, the link layer of the other end may indicate to its transport layer to Stop transmitting data. The data Selector Selects Symbols encoded from codes provided by the transport layer or Symbols generated by the control Symbol

		generator. The data Selector effectively inserts control Symbols and Synchronization Symbols into the Sequence of symbols that are to be transmitted. Various possible encoding techniques for the codes are described below in detail. The data decoder receives symbols from the physical layer and decodes them into codes that are provided to the transport layer. The control symbol identifier identifies control Symbols and Signals the transport layer as appropriate. The physical layer includes a transmitter 231 and receiver 235. The transmitter serializes the symbols provided by the link layer and transmits the serialized symbols onto the communications link. The receiver receives the Serialized Symbols via the communications link, deserializes the symbols, and provides the symbols to the link layer. The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control symbols can be inserted into a sequence of symbols generated from codes provided by the transport layer. Thus, a communications link can be simultaneously transmitting and receiving data symbols, and control symbols can be inserted for link control. Prior transmission techniques typically transmitted in half-duplex mode because the receiving link was reserved for transmission of control information. Thus, the Storage Link architecture has a significant bandwidth advantage because of its full-duplex mode." Shin '450 at [0075-0081].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 352

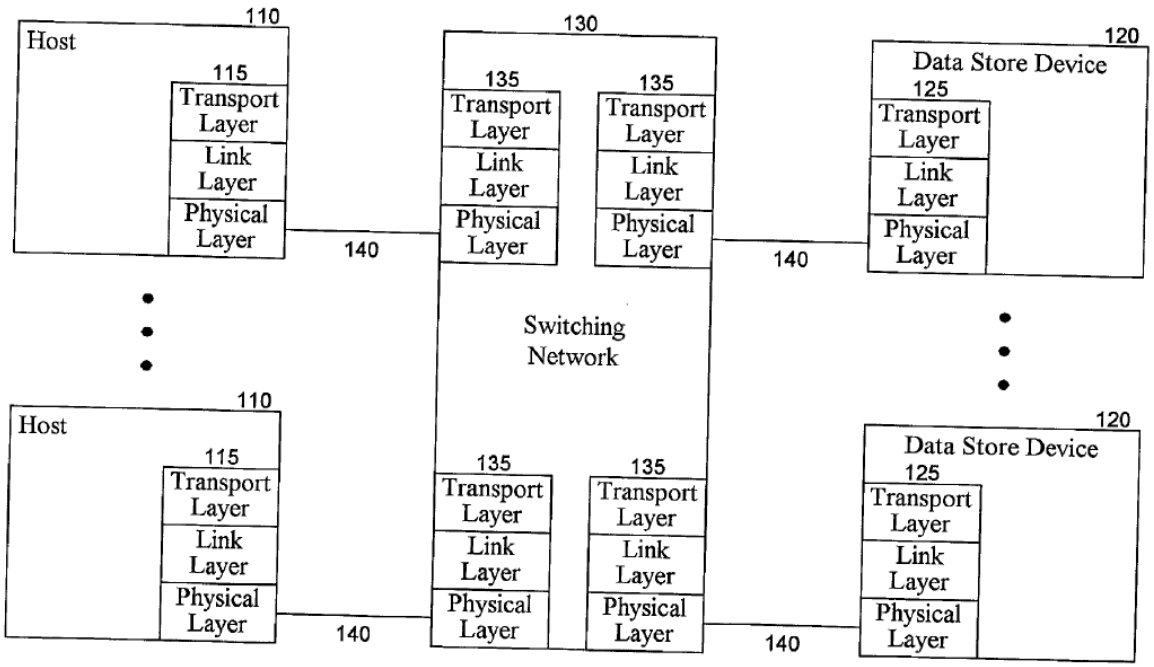


Fig. 1

Shin '450 at Fig. 1.

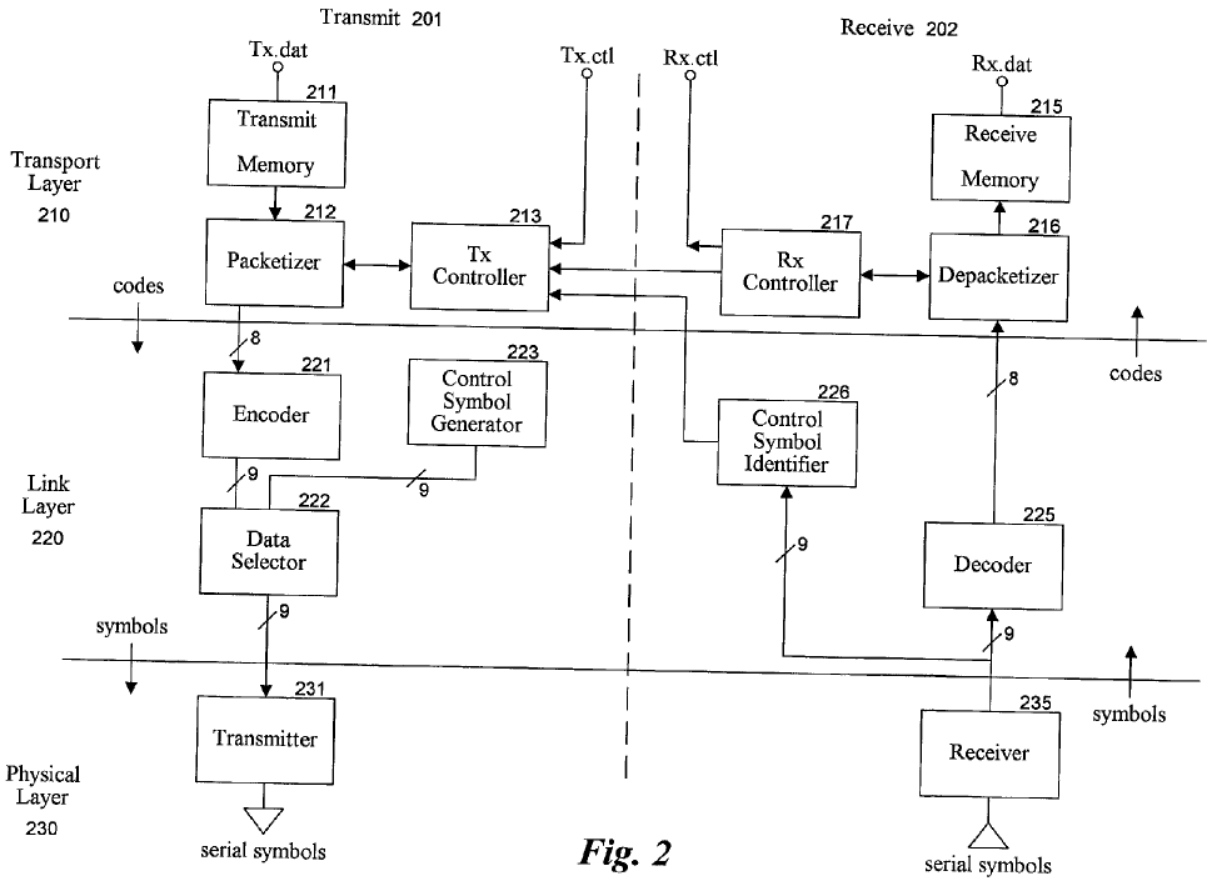
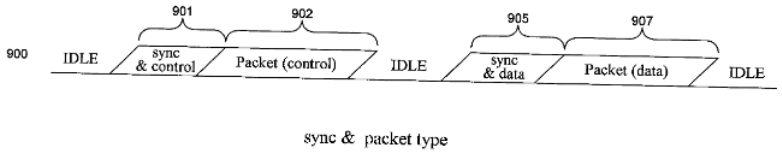
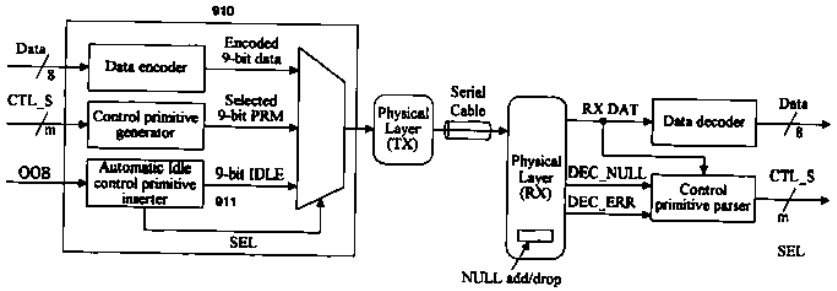


Fig. 2

Shin '450 at Fig. 2.

"FIG. 9A is a diagram illustrating the use of a synchronization primitive encoded with the packet type in one embodiment. Serial link content diagram 900 indicates the information transmitted on a serial link over a period of time. Initially, an IDLE primitive is transmitted onto the communications link. (An IDLE primitive may be a synchronization primitive that does not encode any packet type.) Immediately prior to transmitting control packet 902 (e.g., command,

		status, or message packets), the transport layer of the transmitting communications node signals the link layer that a control packet is to be transmitted next. The link layer then transmits a synchronization primitive 901 encoded with a packet type of control. After the packet has been transmitted, the link layer of the transmitting communications node starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the synchronization primitive encoded with packet type to align its symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097].  *Fig. 9A* Shin '450 at Fig. 9A. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper

		Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105].  ***Fig. 9C*** Shin '450 at Fig. 9C. "FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip." Shin '450 at [0164].

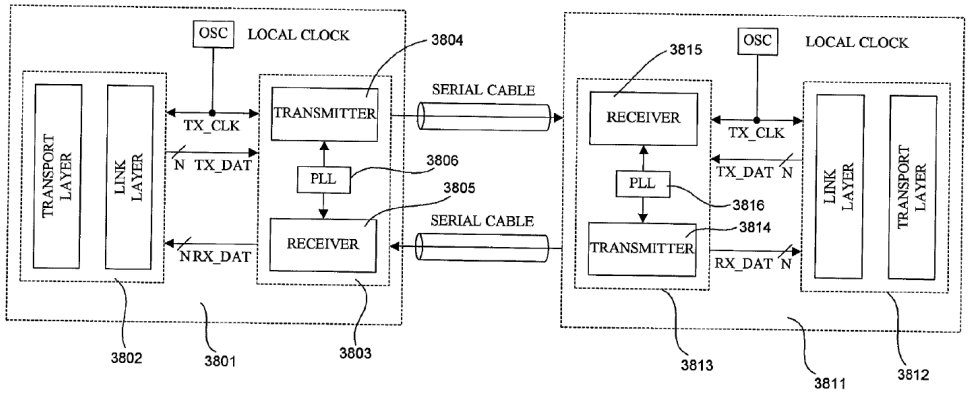


Fig. 38A

Shin ‘450 at Fig. 38A.

The encoding technique in one embodiment encodes an 8-bit code based on the number of transitions in that code. The maximum possible number of transitions in an 8-bit code is seven and occurs when the bit values alternate between 0 and 1 (e.g., “10101010”). The minimum possible number of transitions in an 8-bit code is zero and occurs when all the bit values are the same (e.g., “11111111”). To maximize the number of transitions, the encoding technique inverts the bit value of alternate bits in each code with less than four transitions. This alternate bit inversion, also referred to as transition inversion, results in a code that previously had “n” transitions to now have |n- 7| transitions. For example, the result of alternate bit inversion of a code with zero transitions (e.g., “11111111”) is a code with seven transitions (e.g., “01010101”), and the result of alternate bit inversion of the code with three transitions (e.g., “00010111”) is a code with four transitions (e.g., “10111101”). The encoding technique adds a ninth bit (i.e., a transition inversion indicating bit) to the 8-bit code to indicate whether the alternate bits of the code were inverted, which results in a 9-bit symbol. For example, a bit value of 0 in the ninth bit indicates that the code did not have its alternate bits inverted, and a bit value of 1 in the ninth bit indicates that the code did have its alternate bits inverted. The symbol “010111101” has a bit value of 0 in its ninth bit, which indicates that alternate bits were not inverted. In contrast, the

		symbol "110111101" has a bit value of 1 in its ninth bit, which indicates that alternate bits were inverted. One skilled in the art will appreciate that the ninth bit can be stored at any bit position within the symbol. In this description, the ninth bit is represented as the most significant bit of the symbols. Shin '450 at [0129]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
53(a)	physical and link layer circuitry, coupled and configured to receive and decode the encoded data	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
53(b)	to recover application data and control bits,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
53(c)	to perform at least one link level function in response	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[g].

	to at least one of the control bits; and	To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
53(d)	higher level circuitry coupled to the physical and link layer circuitry, wherein the physical and link layer circuitry is coupled and configured to assert at least one control signal indicative of at least another one of the control bits to the higher level circuitry,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[h]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
53(e)	and the higher level circuitry is configured to perform at least one higher level function in response to the at least one control signal.	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[i]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 68		
68[p]	A transmitter including physical and link layer circuitry, wherein the physical and link layer circuitry include:	To the extent the preamble is limiting, Shin '450 discloses this element and/or renders it obvious either alone or in combination with other references and/or the knowledge of one of ordinary skill in the art. *See, e.g.*: "A serial communications architecture for communicating between hosts and data store devices. The Storage Link architecture is specially adapted to support communications between multiple

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 359

		hosts and storage devices via a switch network, such as a storage area network. The Storage Link architecture specifies various communications techniques that can be combined to reduce the overall cost and increase the overall performance of communications. The Storage Link architecture may provide packet ordering based on packet type, dynamic segmentation of packets, asymmetric packet ordering, packet nesting, variable-sized packet headers, and use of out-of-band symbols to transmit control information as described below in more detail. The Storage Link architecture may also specify encoding techniques to optimize transitions and to ensure DC-balance." Shin '450 at Abstract. "In the following, aspects of the serial communications architecture are described using block diagrams and logic diagrams. One skilled in the art will appreciate that the serial communications architecture can be implemented using different combinations of logic circuits and/or firmware. In particular, the logic diagrams illustrate processing that may be performed in parallel using duplicate logic circuits (e.g., one for each communications link) or may be performed in serial using a single logic circuit. The particular logic designs can be tailored to meet the cost and performance objectives of the implementation of the serial communications architecture. One skilled in the art will be able to readily design logic circuits based on the following descriptions. 1. STORAGE LINKARCHITECTURE FIG. 1 is a block diagram illustrating components of the Storage Link architecture in one embodiment. The hosts 110 and data store devices 120 are interconnected to switching network 130 via serial communications links 140. The hosts may include computer systems that access the data store devices. The data store devices may include storage area network devices (e.g., disk drives), high-speed memory devices, and other devices for storing data. The Storage Link architecture, however, is designed to support block-oriented data store devices, such as disk drives. The switching network may include multiple switches that are interconnected so that communications paths, especially between hosts and data store devices, can be established. Each host, data store device, and switch is a communications node that includes one or more communications interfaces 115, 1257 and 135 with a transport layer, a link layer, and a physical layer." Shin '450 at [0074-0076].

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 360

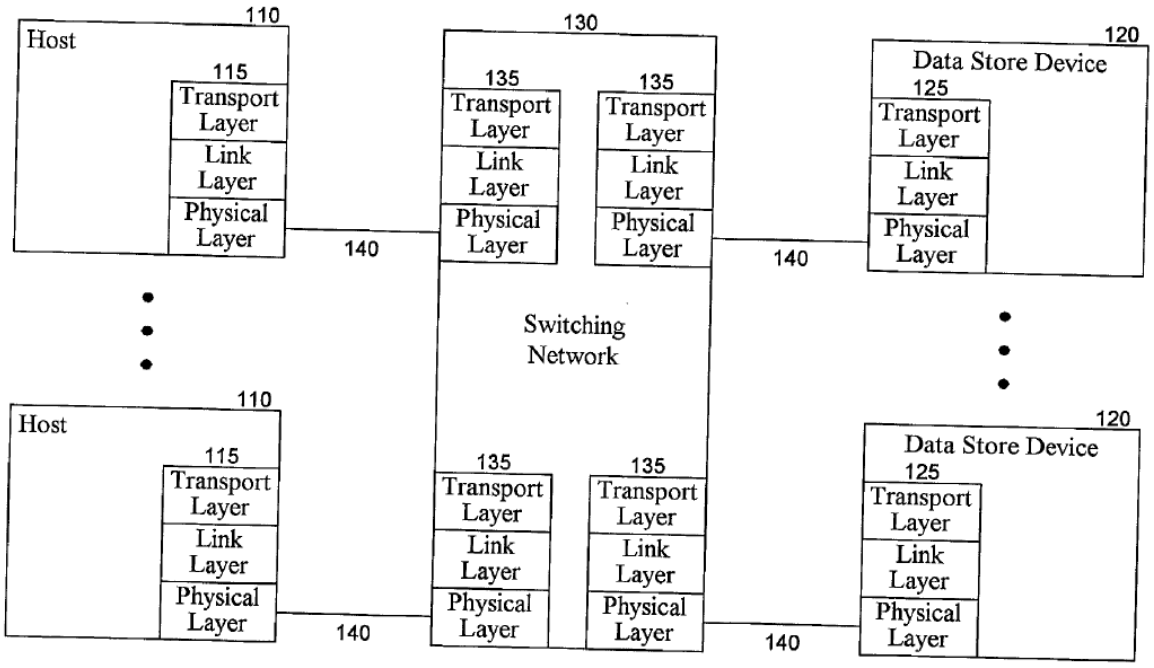
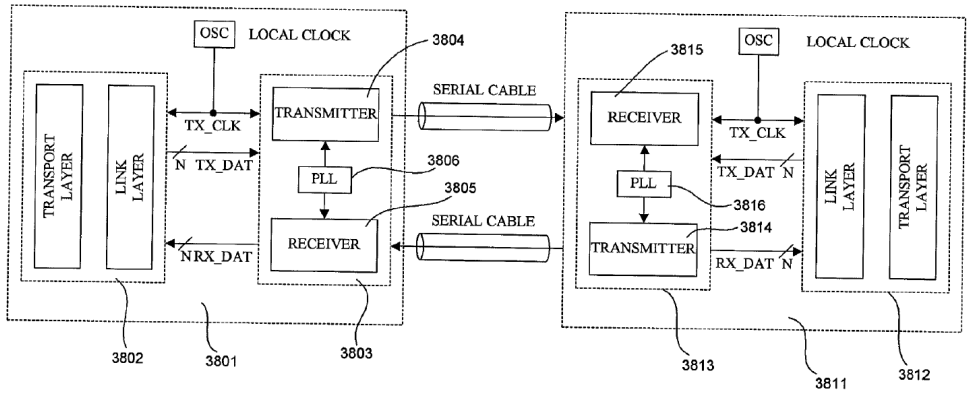


Fig. 1

Shin '450 at Fig. 1.

"FIG. 38A is a block diagram of a plesiosynchronous communications system in one embodiment. Communications node 3801 and communications node 3811 are connected via a bidirectional serial link. The transport layer and the link layer 3802, 3812 may be implemented in a single digital ASIC chip with other interface logic such as PCI bus interface logic. The physical layer 3803 and 3813 may be built in a separated custom analog chip."
Shin '450 at [0164].

		 ***Fig. 38A*** Shin '450 at Fig. 38A. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(a)	packetizing circuitry configured to generate M-bit input words,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(b)	wherein the input words are indicative of	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 23[e].

	application data and control bits; and	To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(c)	encoding and transmission circuitry coupled to the packetizing circuitry and configured to encode the input words in accordance with a block code to generate a code word sequence of N-bit code words, where N>M,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(d)	the code word sequence is indicative of at least one cell of the input words, the cell includes at least two of the control bits,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 23[e]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(e)	and said at least two of the control bits have multiple levels of communication protocol functionality,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 23[f]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

68(f)	wherein the encoding and transmission circuitry is configured to be coupled to a serial link and to transmit encoded data over the serial link,	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 1[a]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
68(g)	said encoded data including the code words of the code word sequence.	Shin '450 discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim element 23[g]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 70		
70	The transmitter of claim 68, wherein the block code is specified by a line code, the line code also specifies special characters, and the encoding and transmission circuitry is configured to generate the encoded data such that said encoded data are a sequence of at least one of the special characters and the code words of the code word sequence.	Shin '450 discloses, expressly or inherently, the transmitter of claim 68 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 68. *See also* exemplary disclosures and corresponding discussion for claim element 1[d]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.

Universal Connectivity Technologies Inc.
Ex. 2005 - Page 364

Claim 71		
71	The transmitter of claim 70, wherein none of the special characters of the encoded data matches a bit sequence of the code word sequence.	Shin '450 discloses, expressly or inherently, the transmitter of claim 70 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 70. *See also* exemplary disclosures and corresponding discussion for claim element 25. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 72		
72	The transmitter of claim 70, wherein said at least one of the special characters is a link training character.	Shin '450 discloses, expressly or inherently, the transmitter of claim 70 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 70. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ("Data') to be transmitted and with an indication of a control primitive ("CTL-S") to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105].

		"In one embodiment, the serial communications architecture defines multiple primitives to operate as Synchronization signals. A Synchronization Signal is typically used by the physical layer to help ensure correct alignment of Symbols. A transmitting communications node periodically transmits Synchronization primitives So that the receiving communications node can properly align with that Synchronization primitive. When a communications node receives a Synchronization primitive, it knows that the primitive is correctly aligned on a Symbol boundary. The use of multiple Synchronization primitives allows for encoding packet type within a Synchronization primitive. In particular, the transport layer provides the packet type to the link layer. The link layer can then transmit a Synchronization primitive that indicates packet type immediately before the packet itself. The receiving communications node can take the appropriate action based on the packet type encoded in the Synchronization primitive without having to parse the packet header. Indeed, the packet header may not need to Separately include the packet type. The use of a Synchronization primitive with encoded packet type may be well adapted to use in an environment where the transmission time of a packet through the Switching network may be long relative to the time needed to Store the packet at the data Store device. For example, the time to transmit a packet through the Switching network may be longer than the time needed to Store the data of the packet in a memory-based data Store device. The rapid detection of packet type through a Synchronization primitive, rather than through a packet header, can reduce the processing time of a Switch. Also, when a Synchronization primitive encodes the packet type, then the link layer, rather than the transport layer, can detect packet type, which can enhance the Overall processing Speed." Shin '450 at [0096]. "After the packet has been transmitted, the link layer of the transmitting communications node Starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the Synchronization primitive encoded with packet type to align its Symbol boundaries

		and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. "FIG. 9C is a block diagram illustrating a component of a link layer for inserting a Synchronization Symbol into a stream of symbols. The link layer 910 is provided with the bits of the code ('Data') to be transmitted and with an indication of a control primitive ('CTL-S') to transmit. The idle inserter 910 of the link layer automatically inserts an IDLE primitive (e.g., Synchronization primitive) to ensure that not too may data Symbols have been Sent without Sending a Synchronization primitive. In one embodiment, the transmitter may send an IDLE primitive after every block of a packet. If packets are short, the inter-packet gap ('IPG') is Sufficient for clock compensation. That is, the receiver will receive Synchronization primitives often enough to maintain proper Synchronization. If a packet is long, however, the link layer can periodically insert a Synchronization primitive to ensure that the receiver maintains proper Synchronization. The multiplexer of the link layer Selects the appropriate Symbol to Send to the physical layer." Shin '450 at [0105]. "FIG. 26 is a logic diagram illustrating transition control and Selective block inversion decoding in one embodiment. The component of the link layer is provided with one symbol at a time by the physical layer. In block 2601, the component stores the symbol in a buffer. In decision block 2602, if the buffer contains a primitive, then the component continues at block 2603 to process the primitive, else the component continues at block 2604. In block 2604, if the buffer contains a complete block, then the component continues at block 2605, else the component waits for the next symbol. In decision block 2605, if the first symbol in the buffer is an out-of-band symbol, then the transmitting communications node inverted the block and the component continues at block 2606, else the component continues at block 2607. In block 2606, the component undoes the block inversion of the block." Shin '450 at [0143].

		"Because of the way memory is typically accessed, the physical layer, link layer, and transport layer might be Simplified as compared to the layers needed in a more general data Store device, Such as a disk drive. Each port of a multiport memory device is typically directly connected to a host. In Such a case, packets do not need to specify a Source and a destination and the headers are thus simplified. In addition, packet types can be encoded in Synchronization primitives to further simplify the packet header. The transport layer of a port in a multiport memory device can be Simplified or eliminated because (1) routing to another device is not needed, (2) minimal or no parsing of the header may be needed, and (3) preemption and priority ordering of packets may not be needed. In addition, the link layer may be simplified by the use of physical layer DC-balancing, rather than the use of the selective block inversion to achieve DC-balance. Physical layer DC-balancing can be used with a multiport memory device because the distance between the host and the multiport memory device is typically relatively short." Shin '450 at [0148]. "FIG. 39B is a block diagram illustrating resolution of an asynchronous clock boundary in the physical layer in one embodiment. The clock and data recover ('CDR') processing of the physical layer 3950 provides to the link layer RX DAT lines that are synchronized to the local clock. Thus, the asynchronous boundary at the link layer along with the needed logic to resolve the boundary is avoided in the link layer. The CDR processing also provides a 1-bit control signal (DET NULL) that indicates a NULL symbol is provided in RX DAT (i.e., to inform the link layer that a primitive has been received) and a 1-bit control signal (DER ERR) that indicates an error in the physical layer data recovery." Shin '450 at [0168]. "The handling of an underrun can also be costly and complex. These underrun and overrun conditions were typically handled at the link layer. These complexities and costs may, however, be avoided by the physical layer of a receiving communications node periodically inserting or removing NULL symbols or NULL primitives from the received Stream of Symbols at a rate Sufficient to compensate for variations in clock frequencies." Shin '450 at [0163] "FIG. 40 is a block diagram illustrating NULL insertion and deletion at the physical layer in one embodiment. Sampler 4010 in one embodiment corresponds to the over sampler 4011, digital

		phase lock loop 4012, and phase selector 4013 described in U.S. Pat. No. 6,229,859, entitled "System and Method for High-Speed, Synchronized Data Communication." The sampler outputs N+1 bits (where N is the number of bits in a symbol) of data lines DO:N) and two valid bits VN-1 and VIN). The sampler identifies a stream of data bits that are received and provides those data bits in data lines DO:N). The valid bits indicate whether DN-1 and DIN contain valid data (e.g., VIN-1=1 indicates that DN-1) is valid). The data bits provided by the sampler are not, however, frame (i.e., Symbol) aligned; that is, DO) is not necessarily (and more often than not would not be) the first bit in a symbol. The valid bits indicate whether an overrun or underrun condition has occurred. An overrun occurs as a result of the transmitter's clock frequency being faster than the receivers, and an underrun occurs as a result of the transmitter's clock frequency being slower than the receiver's. Nominally, N data bits are provided by the Sampler every Sample interval. In Such a case DN-1 is valid, but DN) is invalid. If, however, there is an overrun, then the sampler provides N+1 data bits; that is, DN-1 and DN) are both valid. If there is an underrun, then the sampler provides N-1 data bits; that is, DN-1 and DIN are both invalid. The data bits and the valid bits are supplied to a frame aligner 4020. The frame aligner not only aligns the frames, but also inserts and removes NULL symbols to adjust for variations in the transmitting and receiving clock frequencies." Shin '450 at [0169].

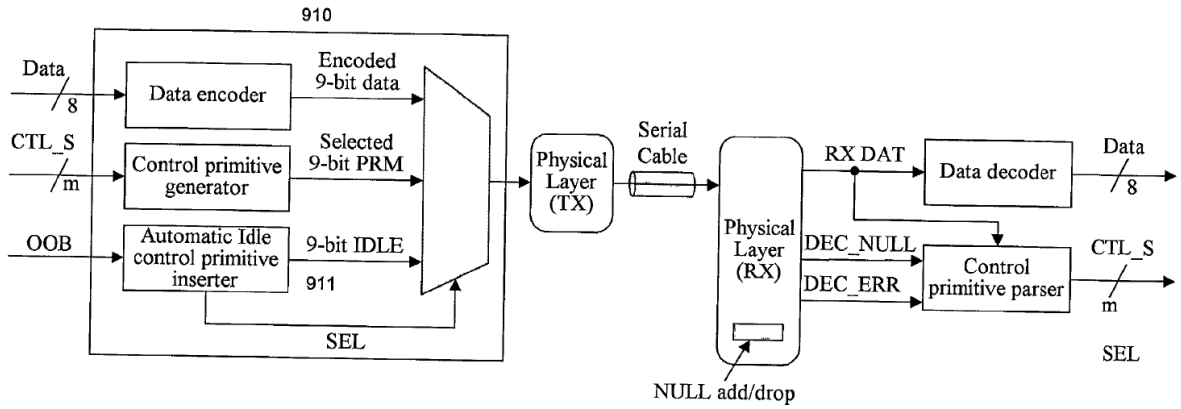


Fig. 9C

Shin '450 at Fig. 9C.

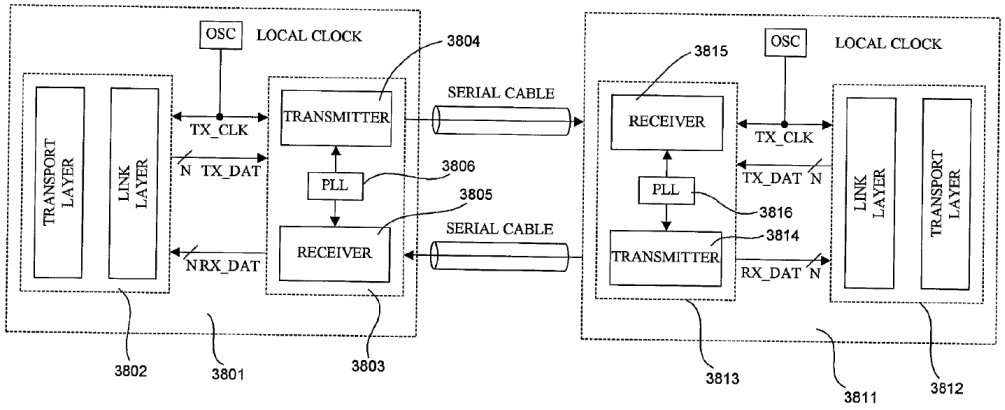


Fig. 38A

Shin '450 at Fig. 38A.

		To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 74		
74	The transmitter of claim 70, wherein said at least one of the special characters is an idle character.	Shin '450 discloses, expressly or inherently, the transmitter of claim 70 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 70. *See also* exemplary disclosures and corresponding discussion for claim element 6. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination with one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.
Claim 75		
75	The transmitter of claim 70, wherein said at least one of the special characters is a flow control character.	Shin '450 discloses, expressly or inherently, the transmitter of claim 70 under any proposed construction, and further discloses and/or renders obvious this limitation. *See, e.g.*: *See* exemplary disclosures and corresponding discussion for claim 70. "The transmit components and the receive components can transmit and receive packets in full duplex mode. That is, a packet received by the transport layer can be transmitted by the transmit components simultaneously with a packet being received by the receive components. As discussed below in detail, the encoding techniques enable transmitting of control symbols by the link layer for link control (e.g., flow control) even while packets are being transmitted in full duplex mode. That is, link control Symbols can be inserted into a Sequence of Symbols generated from codes provided by the transport layer. Thus, a communications link can be Simultaneously transmitting and receiving data Symbols, and control Symbols can be inserted for link control." Shin '450 at [0081].

		"FIG. 5 is a block diagram illustrating the organization of a data packet and a Segmented data packet in one embodiment. The payload Section of a data packet may include a target address and blocks of data to be Stored at the target address. For example, if the data Store device is a disk drive, then the target address may be a Sector address of the disk drive and the blocks of data may each correspond to a Sector of data. In one embodiment, the blocks have a fixed size (e.g., the sector size). Packet 510 includes a header section 500 and a payload section 511 that includes an address 500a and blocks 501-506. When a communications node is transmitting packet 510, it may transmit the header section and address 500a and blocks 501-503 of the payload section. During transmission of block 504, the transmitting communications node may receive an XOFF signal from the receiving communications node. (The receiving communications node may transmit an XOFF control primitive.) The transmitting communications node completes the transmission of block 504 and then stops transmitting the packet on that serial communications link. (The link layer then starts transmitting an IDLE symbol on the communications link.) When the transmitting communications node eventually receives an XON signal from the receiving communications node, it transmits a new header Section 531 plus a payload section indicating a new address 531a and blocks 505 and 506 to complete the transmitting of the packet. The new address may be represented by an offset that is added to a Start address to generate the new address. The new header may contain the same header information as the previously transmitted header, but the address (e.g., as an offset) of the payload Section is updated to reflect the Starting address at which the remaining blocks of the packet are to be Stored. For example, if packet 510 is segmented after block 504 and the Starting address for that packet is address 211, then the starting address for the packet containing blocks 505 and 506 is 215 (i.e., 211+4). Packet 510 is thus segmented into packets 520 and 530. When a packet is segmented, the transport layer may route the remaining packet on a different communications link to the destination. The use of different communications links helps to optimize the use of available bandwidth." Shin '450 at [0090]. "FIG. 7 is a logic diagram illustrating the segmentation of a data packet by the transport layer in one embodiment. In block 701, a component of the transport layer waits for a block of data. In decision block 702, if an XOFF signal has been received, then the component waits for an XON signal in block 703, else the component continues at block 704. In block 704, the component

		sends the header to the link layer for transmission. In blocks 705-707, the component transmits Successive blocks of the packet and Segments the packet when an XOFF signal is received from the link layer. In block 705, the component transmits the next block of the packet. In decision block 706, if an XOFF signal is pending as indicated by the link layer, then the component continues to segment the packet at block 708, else the component continues at block 707. In decision block 707, if the next block is ready, then the component loops to block 705 to transmit the next block, else the component segments (or ends) the packet at block 708. In block 708, the component transmits the CRC to end the packet and waits for the next block in 701." Shin '450 at [0093].

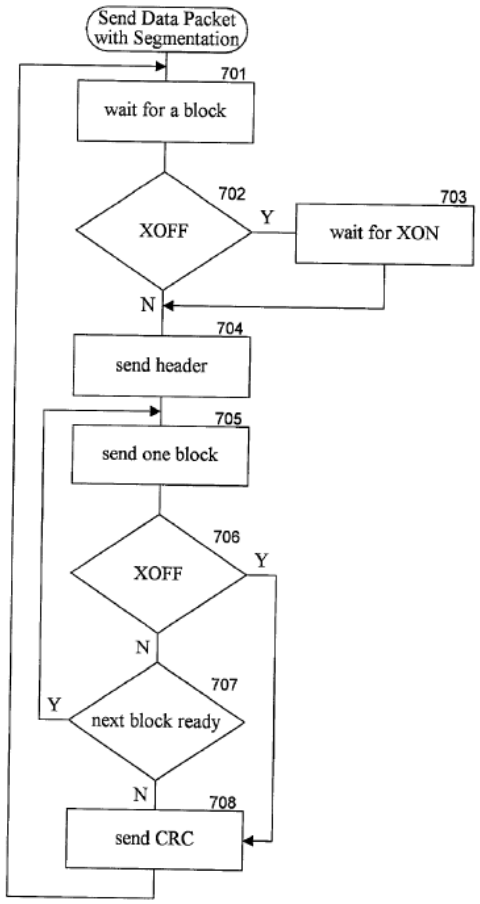


Fig. 7

Shin ‘450 at Fig. 7.

“After the packet has been transmitted, the link layer of the transmitting communications node Starts transmitting the idle primitive. Immediately before the transport layer transmits data packet 904, it notifies the link layer that a data packet is to be transmitted. The link layer transmits a

		synchronization primitive 903 encoded with a packet type of data. After the data packet is transmitted, the link layer starts transmitting the IDLE primitive. The receiving communications node uses the Synchronization primitive encoded with packet type to align its Symbol boundaries and to rapidly identify the packet type. This alignment and identification can occur in the physical and link layers." Shin '450 at [0097]. To the extent that Plaintiff contends that Shin '450 does not explicitly or inherently disclose this element, or render obvious this element, this element is obvious in combination of one or more references and/or with the knowledge of a person of ordinary skill in the art, as set forth in Defendant's Invalidity Contentions.