

Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1

Remove

Given Name

Middle Name

Family Name

City

State

Country i

Homayoon

Haddad

Beaverton

OR

US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Title of Invention

Shallow trench isolation-created backside textured optoelectronic device and associate methods

Attorney Docket Number (if applicable)

3035-060.PROV

Correspondence Address

Direct all correspondence to (select one):

☒ The address corresponding to Customer Number

☐ Firm or Individual Name

Customer Number

20551

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the invention was made by an agency of the United States Government. The U.S. Government agency name is:

☐ Yes, the invention was under a contract with an agency of the United States Government. The name of the U.S. Government agency and Government contract number are:

Entity Status

Applicant asserts small entity status under 37 CFR 1.27 or applicant certifies micro entity status under 37 CFR 1.29

- ☒ Applicant asserts small entity status under 37 CFR 1.27
- ☐ Applicant certifies micro entity status under 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
- ☐ No

Warning

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Todd B. Alder/			Date (YYYY-MM-DD)	2013-06-29
First Name	Todd B.	Last Name	Alder	Registration Number (If appropriate)	54598

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. This form can only be used when in conjunction with EFS-Web. If this form is mailed to the USPTO, it may cause delays in handling the provisional application.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that : (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SHALLOW TRENCH TEXTURED REGIONS AND ASSOCIATED METHODS

BACKGROUND

The interaction of light with semiconductor materials has been a significant
5 innovation. Silicon imaging devices are used in various technologies, such as digital
cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices
(CCDs) were widely used in digital imaging, and were later improved upon by
complementary metal-oxide-semiconductor (CMOS) imagers having improved
performance. Many traditional CMOS imagers utilize front side illumination (FSI). In
10 such cases, electromagnetic radiation is incident upon the semiconductor surface
containing the CMOS devices and circuits. Backside illumination CMOS imagers have
also been used, and in many designs electromagnetic radiation is incident on the
semiconductor surface opposite the CMOS devices and circuits. CMOS sensors are
typically manufactured from silicon and can convert visible incident light into a
15 photocurrent and ultimately into a digital image. Silicon-based technologies for detecting
infrared incident electromagnetic radiation have been problematic, however, because
silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the
absorption of electromagnetic radiation having wavelengths of greater than about 1100
nm is, therefore, very low in silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure,
reference is being made to the following detailed description of embodiments and in
connection with the accompanying drawings, in which:

25 FIG. 1 provides data showing the optical absorption of textured silicon compared
to standard silicon as a function of wavelength in accordance with an embodiment of the
present disclosure;

FIG. 2 is a cross-sectional view of an image sensor in accordance with another
embodiment of the present disclosure;

30 FIG. 3 is a cross-sectional view of an image sensor in accordance with another
embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a textured region associated with a silicon substrate in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a textured region associated with the silicon substrate in accordance with another embodiment of the present disclosure;

5 FIG. 6 is a cross-sectional view of a textured region associated with the silicon substrate in accordance with another embodiment of the present disclosure; and

FIG. 7 is a cross-sectional view of a textured region associated with the silicon substrate in accordance with another embodiment of the present disclosure.

10 **DETAILED DESCRIPTION**

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed
15 herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

20 It should be noted that, as used in this specification and the appended claims, the singular forms “a,” and, “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a dopant” includes one or more of such dopants and reference to “the layer” includes reference to one or more of such layers.

As used herein, the terms “light” and “electromagnetic radiation” can be used
25 interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term “light” is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in
30 the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm

and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately
5 1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as “infrared” portions of the electromagnetic spectrum unless otherwise noted.

As used herein, the term “detection” refers to the sensing, absorption, and/or
10 collection of electromagnetic radiation.

As used herein, the terms “disordered surface” and “textured surface” can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by a variety of known techniques, including chemical etching (e.g. anisotropic etching, isotropic etching), wet
15 or dry etching including masked or maskless etching, lithographic patterning, porous silicon etching, nanoimprinting, material deposition, selective epitaxial growth, reactive ion etching, plasma etching or any other technique that can be used to form such a topology except for laser ablation techniques, which, at least in one aspect, are specifically disclaimed. While the characteristics of such a surface can be variable
20 depending on the materials and techniques employed, in one aspect such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm . A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from
25 the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced at a distance of from about 50nm to about 50 μm . In another aspect, neighboring
30 structures can be spaced at a distance of from about 50nm to about 2 μm . Such spacing is intended to be from a center point of one structure to the center point of a neighboring

structure.

As used herein, the term “backside illumination” refers to a device architecture design whereby electromagnetic radiation is incident on a surface of a semiconductor material that is opposite a surface containing the device circuitry. In other words,
5 electromagnetic radiation is incident upon and passes through a semiconductor material prior to contacting the device circuitry.

As used herein, the term “frontside illumination” refers to a device architecture design whereby electromagnetic radiation is incident on a surface of a semiconductor material that contains the device circuitry. In other words, electromagnetic radiation is
10 incident upon and passes through the device circuitry prior to contacting the semiconductor material.

As used herein, the term “absorptance” refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term “target region” refers to an area of a semiconductor
15 material that is intended to be surface modified. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term “substantially” refers to the complete or nearly
20 complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is “substantially” enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have
25 the same overall result as if absolute and total completion were obtained. The use of “substantially” is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is “substantially free of” particles would either completely lack particles, or so nearly completely lack particles that the effect
30 would be the same as if it completely lacked particles. In other words, a composition that

is “substantially free of” an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term “about” is used to provide flexibility to a numerical range endpoint by providing that a given value may be “a little above” or “a little below” the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of “about 1 to about 5” should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, such silicon based detectors are mostly transparent to infrared light. While other expensive or exotic materials, such as InGaAs, can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm,

silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm — 800 nm). Traditional silicon materials require substantial optical path lengths and absorption depths to detect photons from electromagnetic radiation having wavelengths longer than
5 approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μ m) is poor if at all.

The devices of the present disclosure increase the absorption of semiconductor materials by increasing the effective optical path length for longer wavelengths of
10 electromagnetic radiation as compared to traditional materials. The absorption depth in conventional silicon detectors is the depth into silicon at which the radiation intensity is reduced to about 36% of the value at the surface of the semiconductor. The increased optical path length of the photons results in an apparent reduction in the absorption depth, or a reduced apparent or effective absorption depth. For example, the effective
15 absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μ m. In other words, by increasing the optical path length, these devices are able to absorb longer wavelengths (e.g. > 1000 nm for silicon) within a thin semiconductor material. In addition to absorbing light having longer wavelengths in thin silicon materials (e.g. less than 30 microns thick as
20 compared to 700 microns thick), the response rate or response speed can also be increased by using such thin materials.

Accordingly, photosensitive imager devices and associated methods are provided. It is noted that the present devices can be either frontside illuminated (FSI) or backside illuminated (BSI). Such devices provide, among other things, increased absorption and
25 enhanced response in the near infrared light portion of the optical spectrum, and enhanced response and quantum efficiency in converting electromagnetic radiation to electrical signals. In some aspects, for example, a quantum efficiency (QE) of over 60% can be obtained in the visible region.

The various devices according to aspects of the present disclosure can exhibit
30 increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex

structures can provide not only increased quantum efficiency but also good uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8 A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than $100 \mu\text{m}$ thick. In other
5 embodiment the responsivity can be greater than 0.5 A/W for wavelengths greater than 1100nm for semiconductor substrate that is less than $50 \mu\text{m}$ thick.

As has been described, photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light,
10 however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a
15 micro-lens. BSI imagers, on the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. It should also be understood that devices according to aspects of
20 the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

The present disclosure provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation,
25 including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. As is shown in FIG. 1, for example, a textured region can increase the optical absorption of silicon as compared to non-textured silicon
30 over an electromagnetic spectrum range of at least about 700 nm to about 1100 nm.

A photosensitive imager or pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, and a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In some aspects, the imager can include a passivation region positioned between the textured region and the at least one junction. The passivation region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. It is noted, that with or without the passivation region, the textured region can be located on the light incident side of the semiconductor material, on a side of the semiconductor material opposite the light incident side, or both on the light incident side and opposite the light incident side. Additionally, the photosensitive pixel can also include an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photo detecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As an example, a 4T configuration as is shown in FIG. 1 can additionally include, among other things, a transfer gate 2, a reset transistor 1, a source follower 3, a row select transistor 4, and a photodiode sensor 5. Additionally, devices having greater than 4 transistors are also within the present scope. Photosensor diode 5 can be a conventional pinned photodiode as used in current state of the art CMOS imagers.

In one aspect, as is shown in FIG. 2, a BSI photosensitive diode 200 can include a semiconductor substrate 202 having multiple doped regions 203, 204 forming at least one junction, and a textured region 206 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The multiple doped regions can have the same
5 doping profile or different doping profiles, depending on the device. While the device shown in FIG. 2 contains three doped regions, it should be noted that other aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. In some aspects, a passivation region 208 can be
10 optionally positioned between the textured region 206 and the at least one junction 203,204. The passivation region is positioned to isolate the at least one junction from the textured region, and the semiconductor substrate and the textured region are positioned such that incoming electromagnetic radiation passes through the semiconductor substrate before contacting the textured region. The photosensitive diode is BSI by
15 electromagnetic radiation 210 that is incident on the side of the semiconductor substrate 202 opposite the multiple doped regions 203,204. Additionally, present scope also includes FSI imagers where the incident light impinges on the junction side of the semiconductor material (not shown). Further details regarding both BSI and FSI photodiodes, pixels, imagers, and other optoelectronic devices can be found in US Patent
20 Application Serial Number 12/885,158, filed on September 17, 2010, and in US Patent Number 8,476,681, filed on March 17, 2011, both of which are incorporated herein by reference.

Turning to FIG. 3, an imager is provided having a silicon epi-layer having a textured region on one side, and a device layer opposite the textured region. In some
25 aspects, the textured region can be a pattern of shallow trench isolation features. Such shallow trench isolation features can function to increase the optical absorption of the device, thus enhancing QE. Additionally, the device can include deep trench isolation (DTI) to isolate the imager and to provide light trapping functionality. In addition, in some aspects such a device can include a silicon handle wafer to facilitate manipulation
30 of the device. One technique for coupling the silicon handle wafer to the silicon epi-layer includes oxide bonding. Accordingly, in one aspect shallow trench isolation features can

be formed on a surface of the silicon epi-layer, the silicon handle wafer can be attached to the silicon epi-layer, and the device layer can then be built on the silicon epi-layer while using the silicon handle wafer to manipulate the device. Further details regarding such a substrate, including additional substrate and an imager details can be found in US Patent
5 Application Serial Number 13/069,135, filed on March 22, 2011, which is incorporated herein by reference.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to thus increase the quantum efficiency of the device. In some cases, electromagnetic radiation passing through the semiconductor substrate can
10 contact the textured region. The textured region can include surface features to thus increase the effective optical path length of the photosensitive diode. Such surface features can be micron-sized and/or nano-sized, and can be any shape or configurations. Non-limiting examples of such shapes and configurations include cones, pillars, pyramids, inverted features, trenches, gratings, protrusions, and the like, including
15 combinations thereof. Additionally, factors such as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or
20 eliminated via filtering.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective optical path length, thus allowing the silicon material to
25 absorb light at thicknesses that are less than standard silicon. This increase in the effective optical path length of electromagnetic radiation in silicon increases the quantum efficiency of the device, thus leading to an improved signal to noise ratio.

The materials used for making the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be
30 utilized in the construction of a textured region is considered to be within the present scope. In one aspect, the textured region can be formed directly on the silicon epi-layer.

In another aspect, an additional material can be deposited onto the silicon epi-layer to support the formation of the textured region. Non-limiting examples of such materials include semiconductor materials, dielectric materials, silicon, polysilicon, amorphous silicon, transparent conductive oxides, and the like, including composites and combinations thereof. In one specific aspect, the textured layer can be a textured polysilicon layer. Thus a polysilicon layer can be deposited onto the silicon epi-layer, either directly or onto an intermediate passivation layer, and then textured to form the textured region. In another aspect, the textured layer is a textured dielectric layer. In this case the textured region can be a portion of a dielectric layer making up a passivation region disposed on the silicon epi-layer. In yet another aspect the textured layer can be a transparent conductive oxide or another semiconductor material. In the case of dielectric layers, the textured region can be a textured portion of a passivation region or the textured region can be formed from other dielectric material deposited over a passivation region. The texturing process can texture the entire substrate material or only a portion of the material.

Various methods can be utilized to form shallow trench isolation features, and any such shallow trench formation technique is considered to be within the present scope. Non-limiting examples can include chemical etching (e.g. anisotropic etching, isotropic etching), wet or dry etching including masked or maskless etching, lithographic patterning, porous silicon etching, nanoimprinting, material deposition, selective epitaxial growth, reactive ion etching, plasma etching or any other technique that can be used to form such a topology. It is noted that, in one aspect, texturing techniques that involve laser ablation are specifically disclaimed from the present scope.

In some cases, the textured region can be formed by using a patterned mask and photolithography, followed by etching to define a specific structure or pattern. In one aspect, shallow trench isolation techniques can be used to form the textured region. Various shallow trench isolation techniques are contemplated, and any such technique is considered to be within the present scope. In one non-limiting example, an oxide material is deposited on the substrate to be etched with shallow trenches. Upon the oxide material is deposited a uniform coating of a nitride material followed by a patterned coating of a resist material to be used as a mask. Thus the pattern of the mask will define

the future pattern of the textured region. Any of a number of etch processes can then be applied across the layered material. As a result regions of the layered material beneath the resist are protected from the edge, while regions of the layered material that are not located beneath the resist are etched by the etch process. This process is continued such that a shallow trench is etched in the unprotected regions between the resist material through the nitride material, the oxide material, and into the substrate. Following etching of the shallow trench, the resist material can be removed by any appropriate process. In some aspects where the shallow trenches can be left is open spaces. In other aspects, further processing can be performed to fill in the shallow trenches. For example, in oxide material can be grown along the sides and bottom of the trenches by a thermal oxide process or, by a direct deposition of an oxide material therein in order to create physical passivation. Once the shallow trenches are sufficiently filled, the nitride layer can be removed and the resulting surface can be further processed by techniques such as CMP processing.

In another aspect, once the trenches are formed in the substrate the sidewalls and possibly the bottoms can be highly doped with a dopant profile to create a back surface field. A back surface field can function to impede the movement of photo-generated carriers from the junction toward the silicon epi-layer, and as such the dopant profile should be designed accordingly. The use of the back surface field in the shallow trenches can thus be used to electrically passivate the regions around the shallow trenches.

In some aspects, the shallow trench isolation can be formed on a surface of the silicon epi-layer. In other aspects, a separate material can be applied to the silicon epi-layer, and the shallow trench isolation can subsequently be formed in the separate material. As is shown in FIG. 4, for example, a separate material, in this case amorphous silicon, can be deposited on the silicon epi-layer and subsequently processed to form shallow trench isolation features therein. It is noted, that the use of amorphous silicon is merely exemplary in this case, and that any suitable material is considered to be within the present scope. Additionally, in some aspects an oxide layer can optionally be disposed between the silicon epi-layer and the separate material in order to isolate the shallow trench isolation from the silicon epi-layer.

The shallow trench isolation can have a variety of configurations, structure and in size, depending on the desired characteristics of the resulting device. In one aspect, as is shown in FIG. 5 for example, the shallow trench isolation can be a uniform grid pattern comprised of trench is that form a series of spaces and lines or pillars. Various uniform
5 grid patterns are contemplated, and in one aspect the uniform pattern can include a uniformly spaced series pillars surrounded by spaces. In another aspect, the uniform grid pattern can include a series of lines surrounding a uniformly spaced series of spaces or holes cut between the lines. Additionally, the shallow trench isolation can form a pattern that is nonuniform. As is shown in FIG. 6, for example, the spaces are of approximately
10 the same size and shape and the lines or pillars vary in width. FIG. 7 shows a shallow trench isolation pattern were both spaces and the lines or pillars are varied. It should be noted that a variety of shallow trench isolation patterns are contemplated, and that the present scope should not be limited thereby. With respect to nonuniform patterns, in some aspects the patterns can be random, either for the liner pillar, the spaces, or both. In
15 other aspects, a shallow trench isolation pattern can be nonuniform but also nonrandom.

In addition to the pattern formed by the shallow trench isolation across a surface of the silicon epi-layer, the depth of the spaces between the features may also have an impact on optical absorption. In one aspect, for example, the shallow trench spaces can be cut into the silicon epi-layer to a uniform depth. In another aspect, the shallow trench
20 spaces can be cut into the silicon epi-layer to a nonuniform depth, with the depths of spaces can vary across the surface of the silicon material. Such variation in depth can be random in some cases, and nonrandom in other cases depending on the desired design of the device.

While the present disclosure has focused on silicon materials, it should be
25 understood that a variety of semiconductor materials are also contemplated for use and should be considered to be within the present scope. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary
30 group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can

include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

The silicon epi-layer can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of silicon material is considered to be within the present scope. In some aspects the textured region increases the efficiency of the device such that the silicon material can be thinner than has previously been possible. Decreasing the thickness of the silicon material reduces the amount of silicon required to make such a device. In one aspect, for example, the silicon material has a thickness of from about 500 nm to about 50 μm . In another aspect, the silicon material has a thickness of less than or equal to about 100 μm . In yet another aspect, the silicon material has a thickness of from about 1 μm to about 10 μm . In a further aspect, the silicon material can have a thickness of from about 5 μm to about 50 μm . In yet a further aspect, the silicon material can have a thickness of from about 5 μm to about 10 μm .

A variety of dopant materials are contemplated for both the formation of the multiple doped regions and to create a back surface field at the shallow trench regions, and any such dopant that can be used in such processes is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either charge donating or accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped. A highly doped region can also be formed on or near the doped region to create a pinned diode. In one non-limiting example, the semiconductor substrate can be negative in polarity, and a doped region and a highly doped region can be doped with p+

and n dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++), type doping of the regions can be used.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H₂S, SF₆, SO₂, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm². Non-limiting examples of fluorine-containing compounds can include ClF₃, PF₅, F₂ SF₆, BF₃, GeF₄, WF₆, SiF₄, HF, CF₄, CHF₃, CH₂F₂, CH₃F, C₂F₆, C₂HF₅, C₃F₈, C₄F₈, NF₃, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include B(CH₃)₃, BF₃, BCl₃, BN, C₂B₁₀H₁₂, borosilica, B₂H₆, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF₅, PH₃, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl₂, SiH₂Cl₂, HCl, SiCl₄, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH₃ and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one specific aspect, the dopant material can include Se, H₂S, SF₆, or mixtures thereof. In yet another specific aspect, the dopant can be SF₆ and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm³ to about 5.0×10^{-4} mol/cm³. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of

amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

ABSTRACT OF THE DISCLOSURE

Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a silicon substrate having multiple doped regions forming a least one junction, a textured region coupled to the
5 semiconductor substrate and positioned to interact with electromagnetic radiation. The textured region can be formed from a series of shallow trench isolation features.

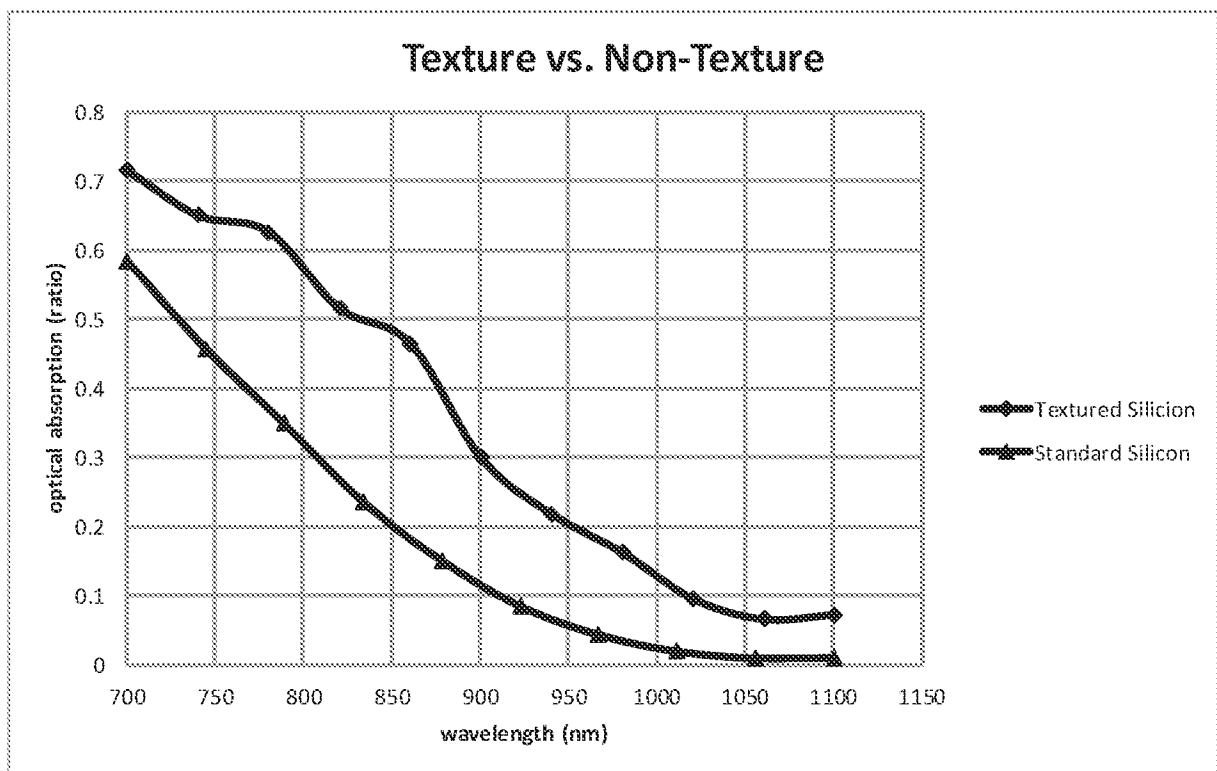


FIG. 1

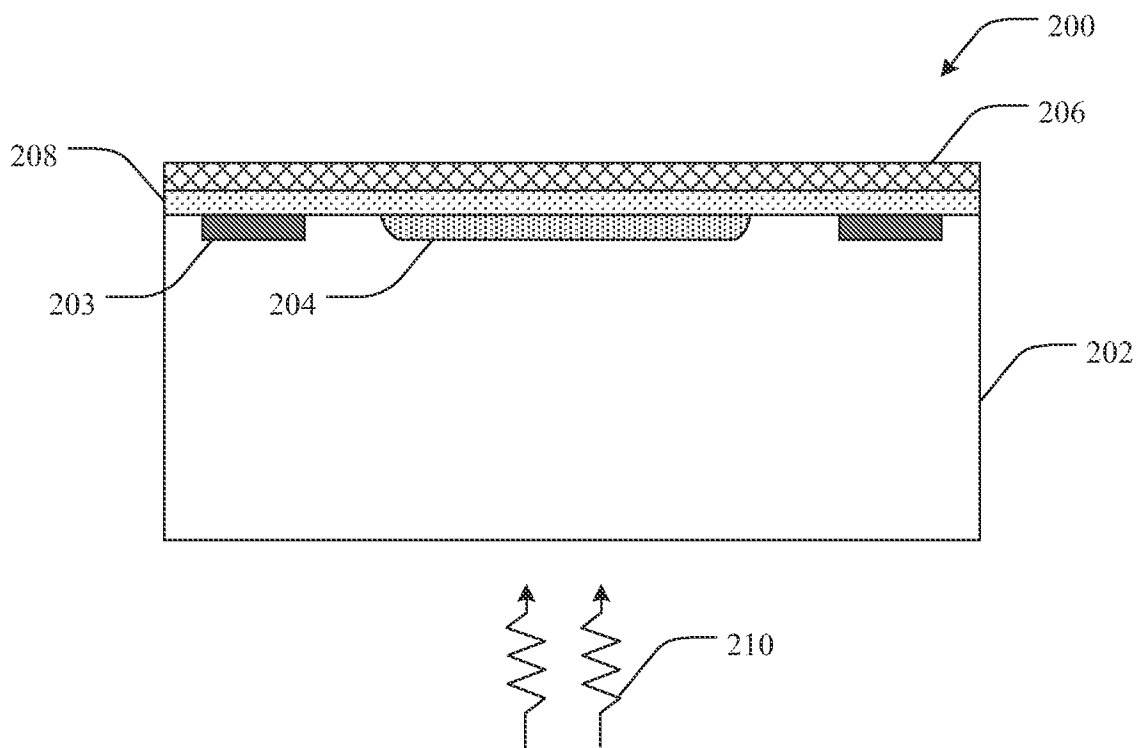


FIG. 2

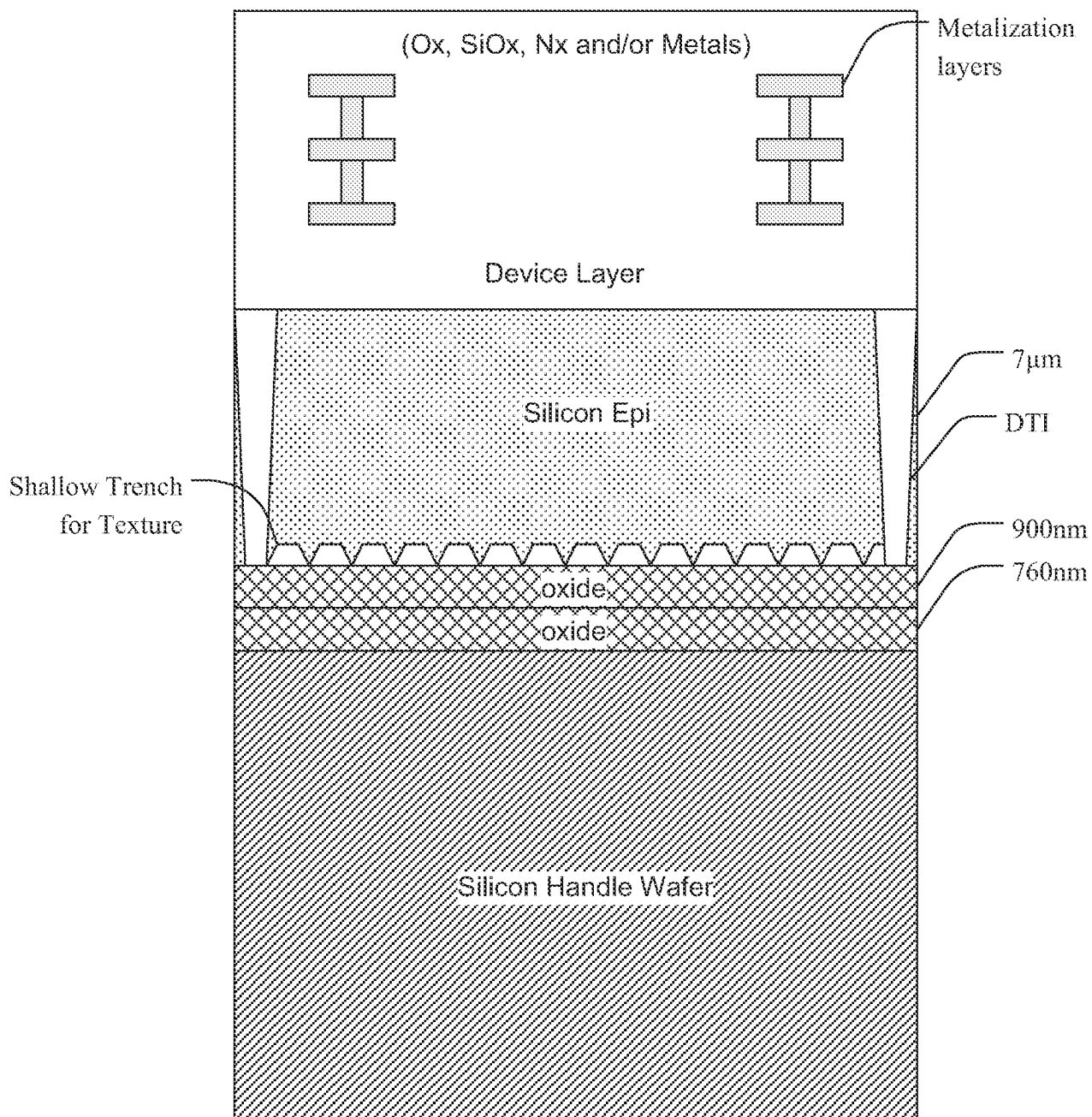


FIG. 3

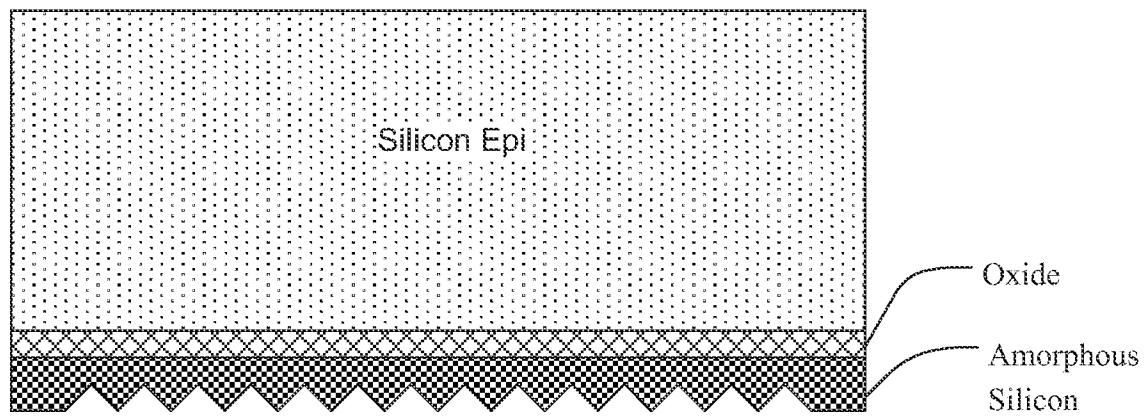


FIG. 4

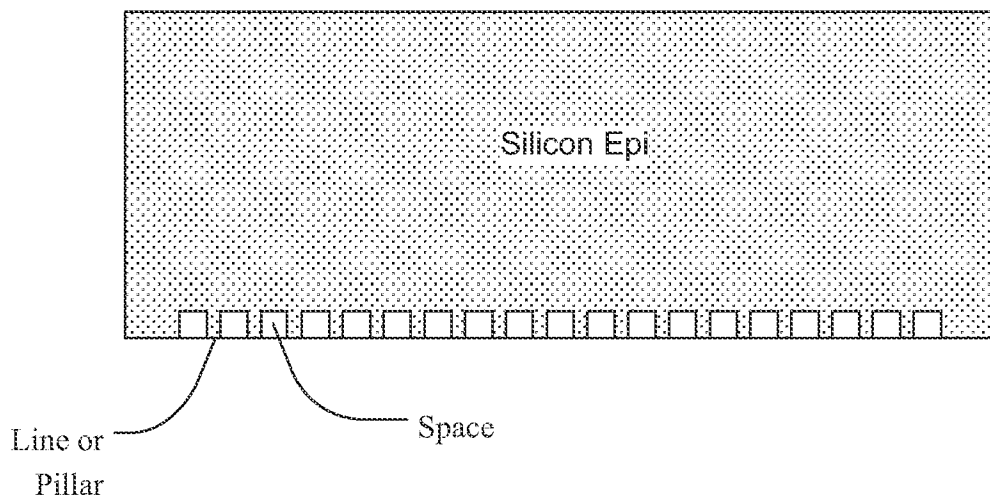
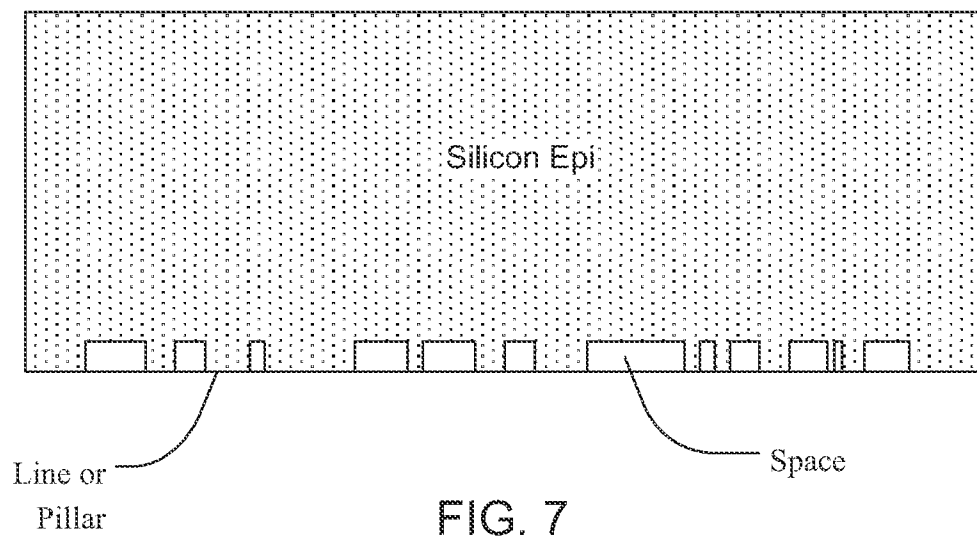
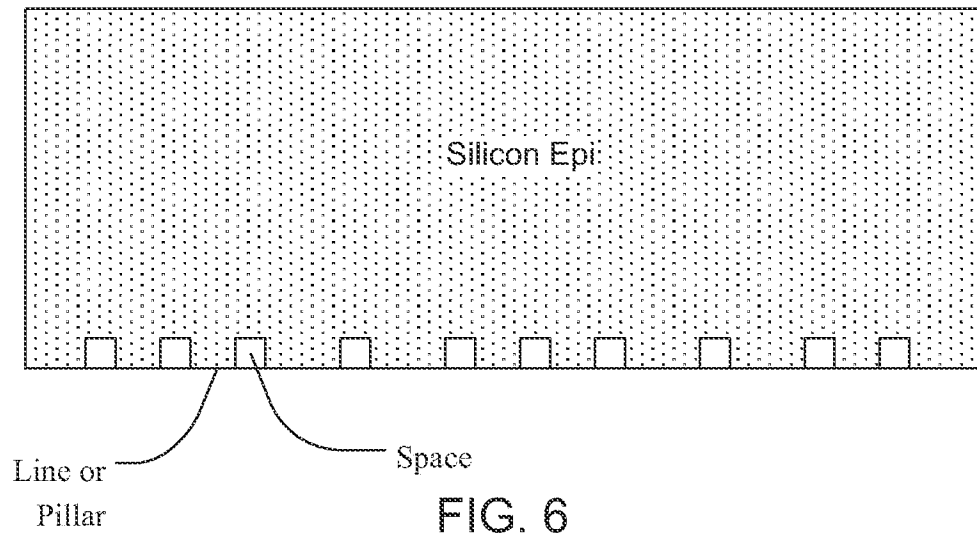


FIG. 5



Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	Shallow Trench Isolation-Created Backside Textured Optoelectronic Device and Associate Methods			
First Named Inventor/Applicant Name:	Homayoon Haddad			
Filer:	Todd Brent Alder			
Attorney Docket Number:	3035-060.PROV			
Filed as Small Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Provisional Application Filing Fee	2005	1	130	130
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				130

Electronic Acknowledgement Receipt

EFS ID:	16195797
Application Number:	61841326
International Application Number:	
Confirmation Number:	6239
Title of Invention:	Shallow Trench Isolation-Created Backside Textured Optoelectronic Device and Associate Methods
First Named Inventor/Applicant Name:	Homayoon Haddad
Customer Number:	20551
Filer:	Todd Brent Alder
Filer Authorized By:	
Attorney Docket Number:	3035-060.PROV
Receipt Date:	29-JUN-2013
Filing Date:	
Time Stamp:	20:40:18
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	\$ 130
RAM confirmation Number	10350
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Provisional Cover Sheet (SB16)	3035-060PROVcoversheet.pdf	1476824 565716231a9788c9a5f3e6beb8cbd30d5560fdec	no	3
Warnings:					
Information:					
2	Specification	3035-060PROVapplication.pdf	110099 2d692eb38f2a165c654e190f1110ec8545e1dc76	no	17
Warnings:					
Information:					
3	Drawings-only black and white line drawings	3035-060PROV_figures.pdf	46195 5c03d9bcf04d66c04f74085ebfbb7ecfa485a144	no	4
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	29588 4a5b638c5d4dbb556fc0861f79a83e1a983b4c06	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1662706		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
61/841,326	06/29/2013		130	3035-060.PROV		

CONFIRMATION NO. 6239

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FILING RECEIPT



Date Mailed: 07/16/2013

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Homayoon Haddad, Beaverton, OR;

Applicant(s)

Homayoon Haddad, Beaverton, OR;

Power of Attorney:

Todd Alder--54598

If Required, Foreign Filing License Granted: 07/12/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/841,326**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

Shallow trench isolation-created backside textured optoelectronic device and associate methods

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international

application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national

security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.