

Fundamentals of Semiconductor Fabrication

GARY S. MAY

*Motorola Foundation Professor
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, Georgia*

SIMON M. SZE

*UMC Chair Professor
National Chiao Tung University
National Nano Device Laboratories
Hsinchu, Taiwan*



WILEY
JOHN WILEY & SONS, INC.

Senior Acquisitions Editor *Bill Zobrist*
Production Editor *Sandra Dumas*
Senior Marketing Manager *Katherine Hepburn*
Senior Designer *Kevin Murphy*
Production Management Services *Argosy*

Photo Credit: Nicole Capello/Georgia Institute of Technology

Cover Description: An eight-inch silicon wafer containing Intel Pentium processors.

The paper in this book was manufactured by a mill whose forest management programs include sustained yield harvesting of its timberlands. Sustained yield harvesting principles ensure that the number of trees cut each year does not exceed the amount of new growth.

This book is printed on acid-free paper. 

Copyright © 2004 by John Wiley & Sons, Inc. All rights reserved.

No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning or otherwise, except as permitted under Sections 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4470. Request to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, (201) 748-6011, fax (201) 748-6008, e-mail: PERMREQ@WILEY.COM. To order books or for customer service call 1-800-CALL-WILEY (225-5945).

May, Gary, S., Simon M. Sze
Fundamentals of Semiconductor Fabrication

ISBN 0-471-23279-3
Wiley International Edition ISBN 0-471-45238-6

10 9 8 7 6 5 4 3 2 1

Etching

As discussed in the previous chapter, lithography is the process of transferring patterns to photoresist covering the surface of a semiconductor wafer. To produce circuit features, these resist patterns must be transferred into the underlying layers comprising the device. The pattern transfer is accomplished by an etching process that selectively removes unmasked portions of a layer.¹ A brief description of etching was given in Section 1.4.2. The present chapter covers the following topics:

- Mechanisms for wet chemical etching of semiconductors, insulators, and metal films
- Plasma-assisted etching (also called dry etching) for high-fidelity pattern transfer

► 5.1 WET CHEMICAL ETCHING

Wet chemical etching is used extensively in semiconductor processing. Starting from semiconductor wafers sliced from an ingot (Chapter 2), chemical etchants are used for lapping and polishing to give an optically flat, damage-free surface. Prior to thermal oxidation (Chapter 3) or epitaxial growth (Chapter 8), semiconductor wafers are chemically cleaned to remove contamination that results from handling and storing. Wet chemical etching is especially suitable for blanket etches (i.e., over the whole wafer surface) of polysilicon, oxide, nitride, metals, and III-V compounds.

The mechanisms for wet chemical etching involve three essential steps, as illustrated in Figure 5.1: The reactants are transported by diffusion to the reacting surface, chemical reactions occur at the surface, and the products from the surface are removed by diffusion. Both agitation and the temperature of the etchant solution influence the etch rate, which is the amount of film removed by etching per unit time. In IC processing, most wet chemical etches proceed by immersing the wafers in a chemical solution or by spraying the wafers with the etchant solution. For immersion etching, the wafer is immersed in the etch solution, and mechanical agitation is usually required to ensure etch uniformity and a consistent etch rate. Spray etching has gradually replaced immersion etching because it greatly increases the etch rate and uniformity by constantly supplying fresh etchant to the wafer surface.

For semiconductor production lines, highly uniform etch rates are important. Etch rates must be uniform across a wafer, from wafer to wafer, from run to run, and for any variations in feature sizes and pattern densities. Etch rate uniformity is given by the following equation:

$$\text{Etch rate uniformity (\%)} = \frac{(\text{Maximum etch rate} - \text{Minimum etch rate})}{(\text{Maximum etch rate} + \text{Minimum etch rate})} \times 100\% \quad (1)$$

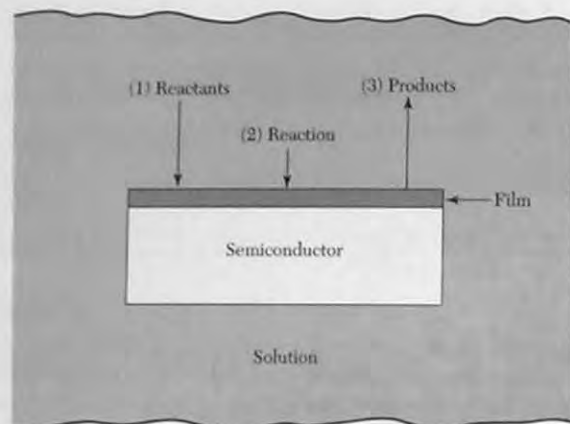


Figure 5.1 Basic mechanisms in wet chemical etching.

EXAMPLE 1

Calculate the Al average etch rate and etch rate uniformity on a 200-mm diameter silicon wafer, assuming the etch rates at the center, left, right, top, and bottom of the wafer are 750, 812, 765, 743, and 798 nm/min, respectively.

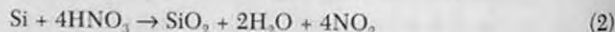
SOLUTION

$$\text{Al average etch rate} = (750 + 812 + 765 + 743 + 798) / 5 = 773.6 \text{ nm/min}$$

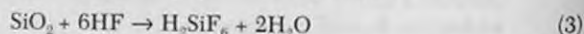
$$\text{Etch rate uniformity} = (812 - 743) / (812 + 743) \times 100\% = 4.4\%$$

5.1.1 Silicon Etching

For semiconductor materials, wet chemical etching usually proceeds by oxidation, followed by the dissolution of the oxide by a chemical reaction. For silicon, the most commonly used etchants are mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF) in water or acetic acid (CH_3COOH). Nitric acid oxidizes silicon to form a SiO_2 layer.² The oxidation reaction is



Hydrofluoric acid is used to dissolve the SiO_2 layer. The reaction is



Water can be used as a diluent for this etchant. However, acetic acid is preferred because it reduces the dissolution of the nitric acid.

Some etchants dissolve a given crystal plane of single-crystal silicon much faster than another plane; this results in orientation-dependent etching.³ For a silicon lattice, the (111) plane has more available bonds per unit area than the (110) and (100) planes; therefore, the etch rate is expected to be slower for the (111) plane. A commonly used orientation-dependent etch for silicon consists of a mixture of KOH in water and isopropyl alcohol.

For example, a solution with 19 wt % KOH in deionized (DI) water at about 80°C removes the (100) plane at a much higher rate than the (110) and (111) planes. The ratio of the etch rates for the (100), (110), and (111) planes is 100:16:1.

Orientation-dependent etching of <100>-oriented silicon through a patterned silicon dioxide mask creates precise V-shaped grooves,⁴ the edges being the (111) planes at an angle of 54.7° from the (111) surface, as shown at the left of Figure 5.2a. If the window in the mask is sufficiently large or if the etching time is short, a U-shaped groove will be formed, as shown at the right of Figure 5.2a. The width of the bottom surface is given by

$$W_b = W_0 - 2l \cot 54.7^\circ$$

or

$$W_b = W_0 - \sqrt{2}l \quad (4)$$

where W_0 is the width of the window on the wafer surface and l is the etched depth. If <110>-oriented silicon is used, essentially straight-walled grooves with sides of (111) planes can be formed, as shown in Figure 5.2b. We can use the large orientation dependence in the etch rates to fabricate device structures with submicron feature lengths.

5.1.2 Silicon Dioxide Etching

The wet etching of silicon dioxide is commonly achieved in a dilute solution of HF with or without the addition of ammonium fluoride (NH_4F). Adding NH_4F creates what is

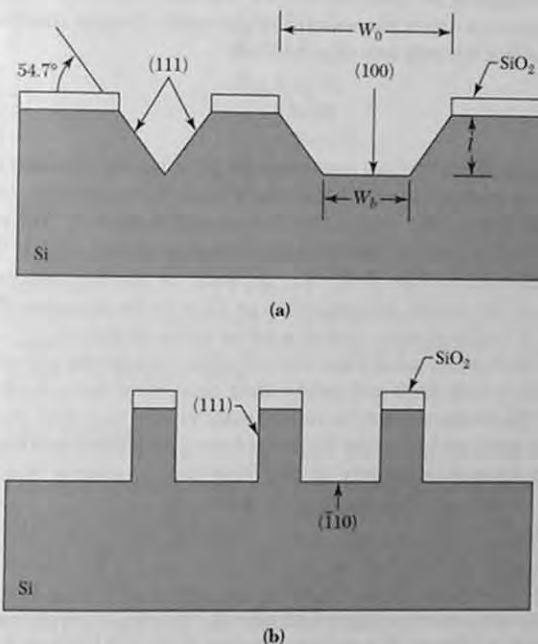


Figure 5.2 Orientation-dependent etching.⁴ (a) Through window patterns on <100>-oriented silicon. (b) Through window patterns on <110>-oriented silicon.

referred to as a *buffered HF solution* (BHF), also called *buffered oxide etch* (BOE). The addition of NH_4F to HF controls the pH value and replenishes the depletion of the fluoride ions, thus maintaining stable etching performance. The overall reaction for SiO_2 etching is the same as that in Eq. 3. The etch rate of SiO_2 etching depends on etchant solution, etchant concentration, agitation, and temperature. In addition, density, porosity, microstructure, and the presence of impurities in the oxide influence the etch rate. For example, a high concentration of phosphorus in the oxide results in a rapid increase in the etch rate, and a loosely structured oxide formed by chemical vapor deposition (CVD) or sputtering exhibits a faster etch rate than thermally grown oxide.

Silicon dioxide can also be etched in vapor-phase HF. Vapor-phase HF oxide etch technology has a potential for submicron feature etching because the process can be well controlled.

5.1.3 Silicon Nitride and Polysilicon Etching

Silicon nitride films are etchable at room temperature in concentrated HF or buffered HF and in a boiling H_3PO_4 solution. Selective etching of nitride to oxide is done with 85% H_3PO_4 at 180°C because this solution attacks silicon dioxide very slowly. The etch rate is typically 10 nm/min for silicon nitride, but less than 1 nm/min for silicon dioxide. However, photoresist adhesion problems are encountered when etching nitride with boiling H_3PO_4 solution. Better patterning can be achieved by depositing a thin oxide layer on top of the nitride film before resist coating. The resist pattern is transferred to the oxide layer, which then acts as a mask for subsequent nitride etching.

Etching polysilicon is similar to etching single-crystal silicon. However, the etch rate is considerably faster because of the grain boundaries. The etch solution is usually modified to ensure that it does not attack the underlying gate oxide. Dopant concentrations and temperature may affect the etch rate of polysilicon.

5.1.4 Aluminum Etching

Aluminum and aluminum alloy films are generally etched in heated solutions of phosphoric acid, nitric acid, acetic acid, and DI water. The typical etchant is a solution of 73% H_3PO_4 , 4% HNO_3 , 3.5% CH_3COOH , and 19.5% DI water at 30°C to 80°C . The wet etching of aluminum proceeds as follows: HNO_3 oxidizes aluminum, and H_3PO_4 then dissolves the oxidized aluminum. The etch rate depends on etchant concentration, temperature, agitation of the wafers, and impurities or alloys in the aluminum film. For example, the etch rate is reduced when copper is added to the aluminum.

Wet etching of insulating and metal films is usually done with similar chemicals that dissolve these materials in bulk form and involve their conversion into soluble salts or complexes. Generally, film materials will be etched more rapidly than their bulk counterparts. Also, the etch rates are higher for films that have a poor microstructure, built-in stress, or departure from stoichiometry, or that have been irradiated. Some useful etchants for insulating and metal films are listed in Table 5.1.

5.1.5 Gallium Arsenide Etching

A wide variety of etches have been investigated for gallium arsenide; however, few of them are truly isotropic.⁵ This is because the surface activities of the (111) Ga and (111) As faces are very different. Most etches give a polished surface on the arsenic face, but the gallium face tends to show crystallographic defects and etches more slowly. The most commonly used etchants are the $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2\text{-H}_2\text{O}$ and $\text{H}_3\text{PO}_4\text{-H}_2\text{O}_2\text{-H}_2\text{O}$ systems. For

TABLE 5.1 Etchants for Insulators and Conductors

Material	Etchant Composition	Etch Rate (nm/min)
SiO_2	28 ml HF	100
	170 ml HF	
	113 g NH_4F	
	15 ml HF	12
	10 ml HNO_3	
	300 ml H_2O	
Si_3N_4	Buffered HF	0.5
Al	H_3PO_4	10
	4 ml HNO_3	30
	3.5 ml CH_3COOH	
	73 ml H_3PO_4	
	19.5 ml H_2O	
Au	4 g KI	1000
Mo	1 g I_2	500
	40 ml H_2O	
	5 ml H_3PO_4	
	2 ml HNO_3	
	4 ml CH_3COOH	
Pt	150 ml H_2O	50
	1 ml HNO_3	
	7 ml HCl	
	8 ml H_2O	
	34 g KH_2PO_4	
W	13.4 g KOH	160
	33 g $\text{K}_3\text{Fe}(\text{CN})_6$	
	H_2O to make 1 liter	

an etchant with an 8:1:1 volume ratio of $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$, the etch rate is 0.8 $\mu\text{m}/\text{min}$ for the <111> Ga face and 1.5 $\mu\text{m}/\text{min}$ for all other faces. For an etchant with a 3:1:50 volume ratio of $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$, the etch rate is 0.4 $\mu\text{m}/\text{min}$ for the <111> Ga face and 0.8 μm for all other faces.

► 5.2 DRY ETCHING

In pattern transfer operations, a resist pattern is defined by a lithographic process to serve as a mask for etching of its underlying layer (Fig. 5.3a).⁶ Most of the layer materials (e.g., SiO_2 , Si_3N_4 , and deposited metals) are amorphous or polycrystalline thin films. If they are etched in a wet chemical etchant, the etch rate is generally isotropic (i.e., the lateral and vertical etch rates are the same), as illustrated in Figure 5.3b. If h_t is the thickness of the layer material and l the lateral distance etched underneath the resist mask, we can define the degree of anisotropy (A_t) by

$$A_t = 1 - \frac{l}{h_t} = 1 - \frac{R_t t}{R_v t} = 1 - \frac{R_t}{R_v} \quad (5)$$

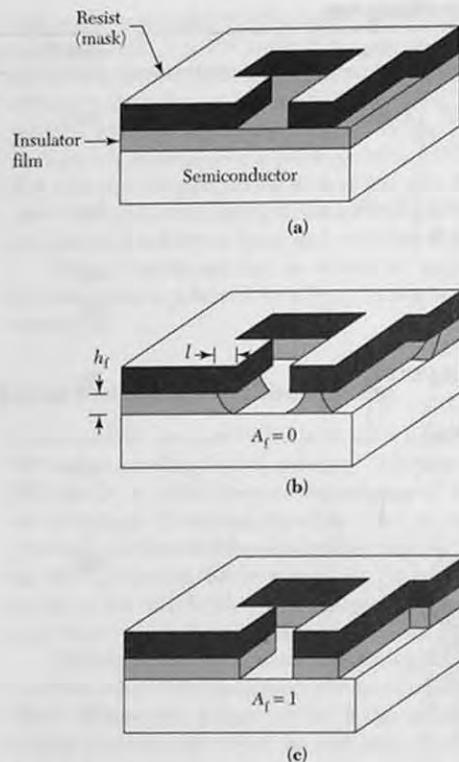


Figure 5.3 Comparison of wet chemical etching and dry etching for pattern transfer.⁶

where t is time and R_l and R_v are the lateral and vertical etch rates, respectively. For isotropic etching, $R_l = R_v$ and $A_t = 0$.

The major disadvantage of wet chemical etching in pattern transfer is the undercutting of the layer underneath the mask, resulting in a loss of resolution in the etched pattern. In practice, for isotropic etching, the film thickness should be about one-third or less of the resolution required. If patterns are required with resolutions much smaller than the film thickness, anisotropic etching (i.e., $1 \geq A_t > 0$) must be used. In practice, the value of A_t is chosen to be close to unity. Figure 5.3c shows the limiting case where $A_t = 1$, corresponding to $l = 0$ (or $R_l = 0$).

To achieve a high-fidelity transfer of the resist patterns required for ultralarge-scale integration processing, dry etching methods have been developed. Dry etching is synonymous with *plasma-assisted etching*, which denotes several techniques that use plasma in the form of low-pressure discharges. Dry etch methods include plasma etching, reactive ion etching (RIE), sputter etching, magnetically enhanced RIE (MERIE), reactive ion beam etching, and high-density plasma (HDP) etching.

5.2.1 Plasma Fundamentals

A plasma is a fully or partially ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules. A plasma is produced

when an electric field of sufficient magnitude is applied to a gas, causing the gas to break down and become ionized. The plasma is initiated by free electrons that are released by some means, such as field emission from a negatively biased electrode. The free electrons gain kinetic energy from the electric field. In the course of their travel through the gas, the electrons collide with gas molecules and lose their energy. The energy transferred in the collision causes the gas molecules to be ionized (i.e., to free electrons). The free electrons gain kinetic energy from the field, and the process continues. Therefore, when the applied voltage is larger than the breakdown potential, a sustained plasma is formed throughout the reaction chamber.

The electron concentrations in the plasma for dry etchings are relatively low, typically on the order of 10^9 to 10^{12} cm⁻³. At a pressure of 1 Torr, the concentrations of gas molecules are 10^4 to 10^7 times higher than the electron concentrations. This results in an average gas temperature in the range of 50°C to 100°C. Therefore, plasma-assisted dry etching is a low-temperature process.

EXAMPLE 2

The electron densities in RIE and HDP systems range from 10^9 to 10^{10} cm⁻³ and 10^{11} to 10^{12} cm⁻³, respectively. Assuming the RIE chamber pressure is 200 mTorr and HDP chamber pressure is 5 mTorr, calculate the ionization efficiency in RIE reactors and HDP reactors at room temperature. The ionization efficiency is the ratio of the electron density to the density of molecules.

SOLUTION

$$PV = nRT$$

where P is the pressure in atm (1 atm = 760,000 mTorr), V is the volume in liters, n is the number of moles, R is the gas constant (0.082 liter-atm/mol-K), and T is the absolute temperature in K, respectively.

For the RIE system,

$$\begin{aligned} n/V &= P/RT = (200/760,000)/(0.082 \times 300) = 1.06 \times 10^{-5} \text{ (mol/liter)} \\ &= 1.06 \times 10^{-5} \times 6.02 \times 10^{23} + 1000 \\ &= 6.38 \times 10^{15} \text{ (cm}^{-3}\text{)} \\ \text{Ionization efficiency} &= (10^9 - 10^{10})/(6.38 \times 10^{15}) \\ &= 1.56 \times 10^{-7} - 1.56 \times 10^{-8} \end{aligned}$$

For the HDP system,

$$\begin{aligned} n/V &= P/RT = (5/760,000)/(0.082 \times 300) = 2.66 \times 10^{-7} \text{ (mol/liter)} \\ &= 2.66 \times 10^{-7} \times 6.02 \times 10^{23} + 1000 \\ &= 1.6 \times 10^{14} \text{ (cm}^{-3}\text{)} \\ \text{Ionization efficiency} &= (10^{11} - 10^{12})/(1.6 \times 10^{14}) \\ &= 6.25 \times 10^{-4} - 6.25 \times 10^{-3} \end{aligned}$$

Therefore, HDP has much higher ionization efficiency than RIE.

5.2.2 Etch Mechanism, Plasma Diagnostics, and End-Point Control

Plasma etching is a process in which a solid film is removed by a chemical reaction with ground-state or excited-state neutral species. Plasma etching is often enhanced or induced

by energetic ions generated in a gaseous discharge. The basic etch mechanism, plasma diagnostics, and end-point control are introduced briefly in this section.

Etch Mechanism

Plasma etching proceeds in five steps, as illustrated in Figure 5.4. First, the etchant species is generated in the plasma. The reactant is then transported by diffusion through a stagnant gas layer to the surface. Next, the reactant is adsorbed on the surface. A chemical reaction (along with physical effects such as ion bombardment) follows to form volatile compounds. Finally, the compounds are desorbed from the surface, diffused into the bulk gas, and pumped out by the vacuum system.⁷

Plasma etching is based on the generation of plasma in a gas at low pressure. Two basic types of methods are used: physical methods and chemical methods. The former includes sputter etching, and the latter includes pure chemical etching. In physical etching, positive ions bombard the surface at high speed; small amounts of negative ions formed in the plasma cannot reach the wafer surface and therefore play no direct role in plasma etching. In chemical etching, neutral reactive species generated by the plasma interact with the material surface to form volatile products. Chemical and physical etch mechanisms have different characteristics. Chemical etching exhibits a high etch rate and good selectivity (i.e., the ratio of etch rates for different materials) and produces low ion bombardment-induced damage, but yields isotropic profiles. Physical etching can yield anisotropic profiles, but is associated with low etch selectivity and high bombardment-induced damage. Combinations of chemical and physical etching give anisotropic etch profiles, reasonably good selectivity, and moderate bombardment-induced damage. An example is the RIE process, which uses a physical method to assist chemical etching or creates reactive ions to participate in chemical etching.

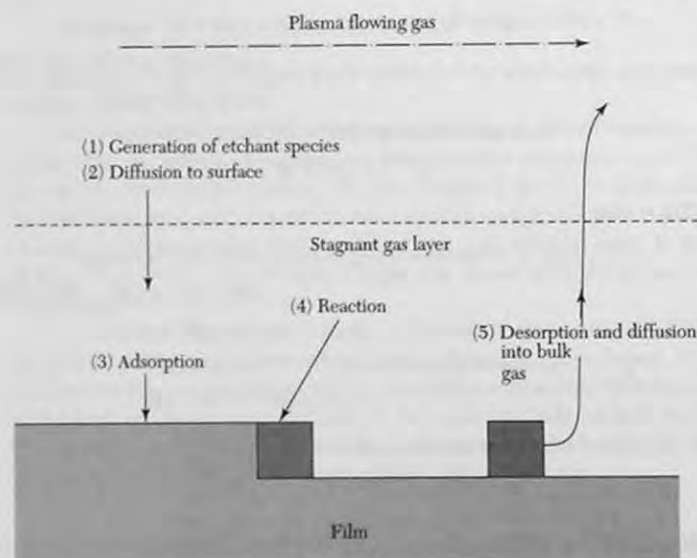


Figure 5.4 Basic steps in a dry etching process.⁷

Plasma Diagnostics

Most processing plasmas emit radiation in the range from infrared to ultraviolet. A simple analytical technique is to measure the intensity of these emissions versus wavelength with the aid of optical emission spectroscopy (OES). Using observed spectral peaks, it is usually possible to determine the presence of neutral and ionic species by correlating these emissions with previously determined spectral series. Relative concentrations of the species can be obtained by correlating changes in intensity with the plasma parameters. The emission signal derived from the primary etchant or by-product begins to rise or fall at the end of the etch cycle.

End-Point Control

Dry etching differs from wet chemical etching in that dry etching has less etch selectivity to the underlying layer. Therefore, the plasma reactor must be equipped with a monitor that indicates when the etching process is to be terminated (i.e., an *end-point detection system*). Laser interferometry of the wafer surface is used to continuously monitor etch rates and to determine the end point. During etching, the intensity of laser light reflected off a thin film surface oscillates. This oscillation occurs because of the phase interference between the light reflected from the outer and inner interfaces of the etching layer. This layer must therefore be optically transparent or semitransparent to observe the oscillation. Figure 5.5 shows a typical signal from a silicide/polycrystalline Si gate etch. The period of the oscillation is related to the change in film thickness by

$$\Delta d = \lambda / 2\bar{n} \quad (6)$$

where Δd is the change in film thickness for one period of reflected light, λ is the wavelength of the laser light, and $\bar{n}$ is the refractive index of the layer being etched. For example, Δd for polysilicon is 80 nm, measured by using a helium-neon laser source for which $\lambda = 632.8$ nm.

5.2.3 Reactive Plasma Etching Techniques and Equipment

Plasma reactor technology in the IC industry has changed dramatically since the first application of plasma processing to photoresist stripping. A reactor for plasma etching contains a vacuum chamber, pump system, power supply generators, pressure sensors, gas flow control units, and end-point detector. Table 5.2 shows the similarities and differences

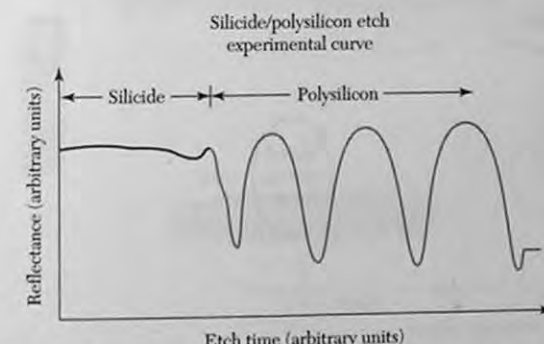


Figure 5.5 The relative reflectance of the etching surface of a composite silicide/poly-Si layer. The end point of the etch is indicated by the cessation of the oscillations.

TABLE 5.2 Etch Mechanisms and Pressure Ranges of Plasma Reactors

Etch Tool Configuration	Etch Mechanism	Pressure Range (Torr)
Barrel etching	Chemical	0.1–10
Downstream plasma etching	Chemical	0.1–10
Reactive ion etching (RIE)	Chemical and physical	0.01–1
Magnetic enhanced RIE	Chemical and physical	0.01–1
Magnetic confinement triode RIE	Chemical and physical	0.001–0.1
Electron cyclotron resonance plasma etch	Chemical and physical	0.001–0.1
Inductively coupled plasma or transformer-coupled plasma	Chemical and physical	0.001–0.1
Surface wave coupled plasma or helicon plasma etching	Chemical and physical	0.001–0.1

in the types of etching equipment that are commercially available. A comparison of pressure operating ranges and ion energies for different types of reactors is shown in Figure 5.6. Each etch tool is designed empirically and uses a particular combination of pressure, electrode configuration and type, and source frequency to control the two primary etch mechanisms—chemical and physical. Higher etch rates and tool automation are required for most etchers used in manufacturing.

Reactive Ion Etching

RIE has been extensively used in the microelectronics industry. In a parallel-plate diode system, a radio frequency capacitively coupled bottom electrode holds the wafer. This allows the grounded electrode to have a significantly larger area because it is, in fact, the chamber itself. The larger grounded area combined with the lower operating pressure (<500 mTorr) causes the wafers to be subjected to a heavy bombardment of energetic ions from the plasma as a result of the large negative self-bias at the wafer surface.

The etch selectivity of this system is relatively low compared with traditional barrel-etch systems because of strong physical sputtering. However, selectivity can be improved

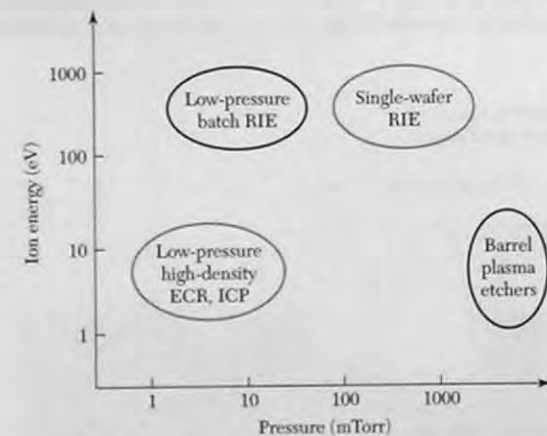


Figure 5.6 Comparison of ion energy and operating pressure ranges for different types of plasma reactors.

by choosing the proper etch chemistry, for example, by polymerizing the silicon surface with fluorocarbon polymers to obtain selectivity of SiO_2 over silicon. Alternatively, a triode-configuration RIE etch, as shown in Figure 5.7, can separate plasma generation from ion transport. Ion energy is controlled through a separate bias on the wafer electrode, thereby minimizing the loss of selectivity and the ion bombardment-induced damage observed in most traditional RIE systems.

Electron Cyclotron Resonance Plasma Etching

Most parallel-plate plasma etchers, except triode RIE, do not provide the ability to control plasma parameters such as electron energy, plasma density, and reactant density independently. As a result, ion bombardment-induced damage becomes a serious problem. The *electron cyclotron resonance* (ECR) reactor combines microwave power with a static magnetic field to force electrons to circulate around the magnetic field lines at an angular frequency. When this frequency equals the applied microwave frequency, a resonance coupling occurs between the electron energy and the applied electric field that results in a high degree of dissociation and ionization (10^{-2} for ECR compared with 10^{-6} for RIE). Figure 5.8 shows an ECR reaction chamber configuration. Microwave power is coupled through a microwave window into the ECR source region. The magnetic field is supplied from the magnetic coils. ECR plasma systems can also be used in thin film deposition. High efficiency in exciting the reactants in ECR plasmas allows the deposition of films at room temperature without the need for thermal activation.

Other High-Density Plasma Etchers

As feature sizes for ULSI continue to decrease, the limits of the conventional RIE system are being approached. In addition to the ECR system, other types of high-density plasma sources, such as the inductively coupled plasma (ICP) source, the transformer-coupled plasma (TCP) source, and surface wave-coupled plasma (SWP) sources, have been developed. These etchers have high plasma density (10^{11} – 10^{12} cm^{-3}) and low processing pressure (<20 mTorr). In addition, they allow the wafer platen to be powered independently of the source, providing significant decoupling between the ion energy (wafer bias) and the ion flux (plasma density, primarily driven by source power). The primary

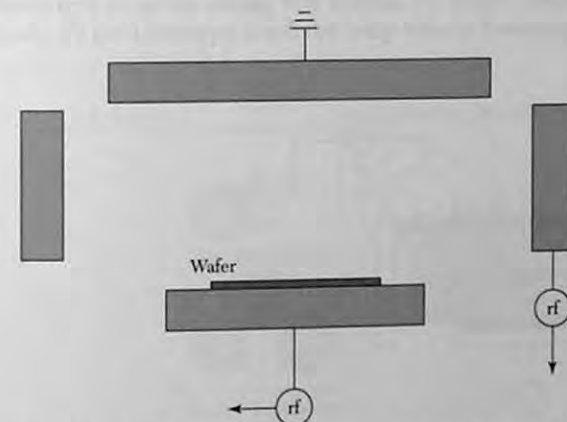


Figure 5.7 Schematic of a triode reactive ion etch reactor. The ion energy is separately controlled by a bias voltage on the bottom electrode. rf, radio frequency.

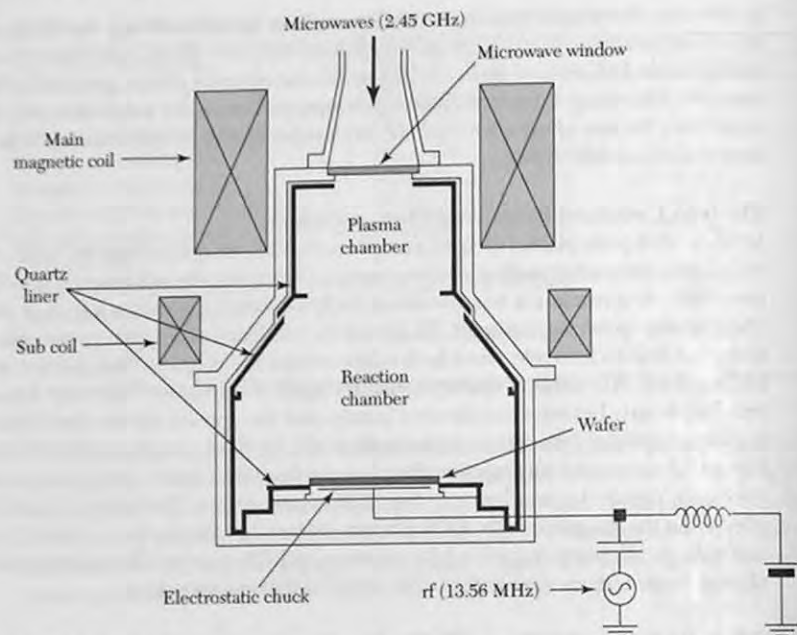


Figure 5.8 Schematic of an electron cyclotron resonance reactor.

processing advantages of HDP sources are better critical dimension (CD) control, higher etching rates, and better selectivity.

In addition, HDP sources provide low substrate damage (because of independent biasing of the substrate and the side electrode potentials) and high anisotropy (because of low pressure, yet high active species density). However, because of their complexity and higher cost, these systems may not be used for less critical applications, such as spacer etching or planarization.⁵ Figure 5.9 shows a TCP plasma reactor. A high-density, low pressure plasma is generated by a flat spiral coil that is separated from the plasma by a

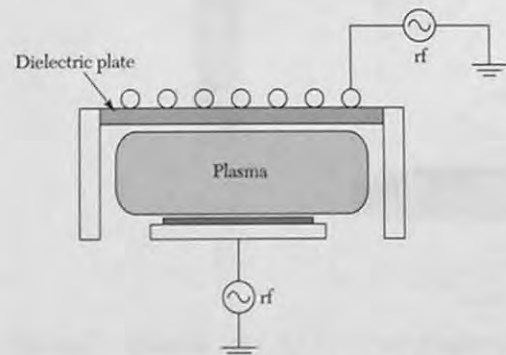


Figure 5.9 Schematic of a transformer-coupled plasma reactor.

dielectric plate on the top of the reactor. The wafer is located away from the coil, so it is not affected by the electromagnetic field generated by the coil. There is little plasma density loss because plasma is generated only a few mean free paths away from the wafer surface. Therefore, a high-density plasma and high etch rates are achieved.

Clustered Plasma Processing

Semiconductor wafers are processed in clean rooms to minimize exposure to ambient particulate contamination. As device dimensions shrink, particulate contamination becomes a more serious problem. To minimize particulate contamination, clustered plasma tools use a wafer handler to pass wafers from one process chamber to another in a vacuum environment. Clustered plasma processing tools can also increase throughput. Figure 5.10 shows the multilayer metal (TiW/AlCu/TiW) etching process with clustered tools in an AlCu etch chamber, a TiW etch chamber, and a strip passivation chamber. Clustered tools provide an economic advantage by having high chip yield because the wafer is exposed to less ambient contamination and is handled less.

5.2.4 Reactive Plasma Etching Applications

Plasma etching has rapidly evolved from simple batch resist stripping to large and single-wafer processing. Etching systems continue to be improved, from the conventional RIE tool to the high-density plasma tool for pattern transfer of deep-submicron devices. Aside from the etching tool, etch chemistry also plays a critical role in the performance of the etch process. Table 5.3 lists some etch chemistries for different etch processes. Developing an etch process usually means optimizing etch rate, selectivity, profile control, critical dimension, damage, and so forth by adjusting a large number of process parameters.

Silicon Trench Etching

As device feature size decreases, a corresponding decrease is needed in the wafer surface area occupied by the isolation between circuit elements and the storage capacitor

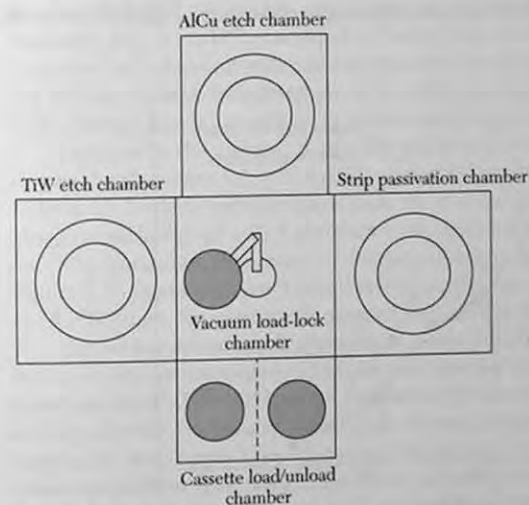


Figure 5.10 Cluster reactive ion etch tool for multilayer metal (TiW/AlCu/TiW) interconnect etching.²

TABLE 5.3 Etch Chemistries of Different Etch Processes

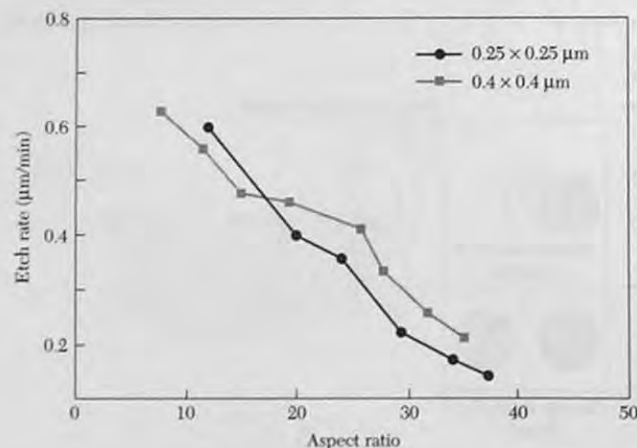
Material Being Etched	Etching Chemistry
Deep Si trench	HBr/NF ₃ /O ₂ /SF ₆
Shallow Si trench	HBr/Cl ₂ /O ₂
Poly Si	HBr/Cl ₂ /O ₂ , HBr/O ₂ , BCl ₃ /Cl ₂ , SF ₆
Al	BCl ₃ /Cl ₂ , SiCl ₄ /Cl ₂ , HBr/Cl ₂
AlSiCu	BCl ₃ /Cl ₂ /N ₂
W	SF ₆ only, NF ₃ /Cl ₂
TiW	SF ₆ only
WSi ₂ , TiSi ₂ , CoSi ₂	CCl ₂ F ₂ /NF ₃ , CF ₄ /Cl ₂ , Cl ₂ /N ₂ /C ₄ F ₈
SiO ₂	CF ₄ /CHF ₃ /Ar, C ₂ F ₆ , C ₃ F ₈ , C ₄ F ₈ /CO, C ₃ F ₈ , CH ₂ F ₂
Si ₃ N ₄	CHF ₃ /O ₂ , CH ₂ F ₂ , CH ₃ CHF ₂

of a DRAM cell. This surface area can be reduced by etching trenches into the silicon substrate and filling them with suitable dielectric or conductive materials. Deep trenches, usually with a depth greater than 5 μm , are used mainly for forming storage capacitors. Shallow trenches, usually with a depth less than 1 μm , are often used for isolation.

Chlorine-based and bromine-based chemistries have a high silicon etch rate and high etch selectivity to the silicon dioxide mask. The combination of HBr + NF₃ + SF₆ + O₂ gas mixtures is used to form a trench capacitor with a depth of approximately 7 μm . This combination is also used for shallow trench isolation etching. *Aspect ratio-dependent etching* (i.e., variation in etch rate with aspect ratio) is often observed in deep silicon trench etching, caused by limited ion and neutral transport within the trench. Figure 5.11 shows the dependence of average silicon trench etch rate on aspect ratio. Trenches with large aspect ratios are etched more slowly than trenches with small aspect ratios.

Polysilicon and Polycide Gate Etching

Polysilicon or polycide (i.e., low-resistance metal silicides over polysilicon) is usually used as a gate material for MOS devices. Anisotropic etching and high etch selectivity to the

Figure 5.11 Dependence of average silicon trench etch rate on aspect ratio.²

gate oxide are the most important requirements for gate etching. For example, the selectivity required in 1G DRAM is more than 150 (i.e., the ratio of etch rates for polycide and gate oxide is 150:1). Achieving high selectivity and etch anisotropy at the same time is difficult for most ion-enhanced etching processes. Therefore, multistep processing is used, in which different etch steps in the process are optimized for etch anisotropy and selectivity. On the other hand, the trend in plasma technology for anisotropic etching and high selectivity is to utilize a low-pressure, high-density plasma using a relatively low power. Most chlorine-based and bromine-based chemistries can be used for gate etching to achieve the required etch anisotropy and selectivity.

Dielectric Etching

The patterning of dielectrics, especially silicon dioxide and silicon nitride, is a key process in the manufacture of modern semiconductor devices. Because of their higher bonding energies, dielectric etching requires aggressive ion-enhanced, fluorine-based plasma chemistry. Vertical profiles are achieved by sidewall passivation, typically by introducing a carbon-containing fluorine species to the plasma (e.g., CF₄, CHF₃, C₄F₈). High ion-bombardment energies are required to remove this polymer layer from the oxide, as well as to mix the reactive species into the oxide surface to form SiF_x products.

A low-pressure, high-density plasma is advantageous for aspect ratio-dependent etching. However, the HDP generates high-temperature electrons and subsequently generates a high degree of dissociation of ions and radicals. It generates far more active radicals and ions than RIE or MERIE plasmas. In particular, a high F concentration worsens the selectivity to silicon. Various methods have been tried to enhance the selectivities in the high-density plasma. First, a parent gas with a high C/F ratio, such as C₂F₆, C₄F₈, or C₃F₈, was attempted. Other methods to scavenge F radicals have also been developed.⁹

Interconnect Metal Etching

Etching of a metallization layer is a very important step in IC fabrication. Aluminum, copper, and tungsten are the most popular materials used for interconnection. These materials usually require anisotropic etching. The reaction of aluminum with fluorine results in nonvolatile AlF₃, which has a vapor pressure of only 1 Torr at 1240°C. Chlorine-based chemistry (e.g., a Cl₂/BCl₃ mixture) has been widely used for aluminum etching. Chlorine has a very high chemical etch rate with aluminum and tends to produce an undercut during etching. Carbon-containing gas (e.g., CHF₃) or N₂ is added to form sidewall passivation during aluminum etching to obtain anisotropic etching.

Exposure to the ambient is another problem in aluminum etching. Residual chlorine on the aluminum sidewall and the photoresist tends to react with atmospheric water to form HCl, which corrodes aluminum. An *in situ* exposure of the wafer to a CF₄ discharge to exchange Cl with F and then to an oxygen discharge to remove the resist, followed by immediate immersion in deionized water, can eliminate aluminum corrosion. Figure 5.12 shows 0.35- μm TiN/Al/Ti lines and spaces on a wafer maintained at ambient for 72 hours. No corrosion is present even after prolonged exposure to the ambient.

Copper has drawn much attention as a new metallization material in ULSI circuits because of its low resistivity ($\sim 1.7 \Omega\text{-cm}$) and superior resistance to electromigration compared with Al or Al alloys. However, because of the low volatility of copper halides, plasma etching at room temperature is difficult. Process temperatures higher than 200°C are required to etch copper films. Therefore, the *damascene* process is used to form Cu interconnection without dry etching. Damascene processing involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench with metal, such as aluminum or copper. In dual damascene processing (Fig. 5.13), a second level is involved where a series of holes (vias) are etched and filled.

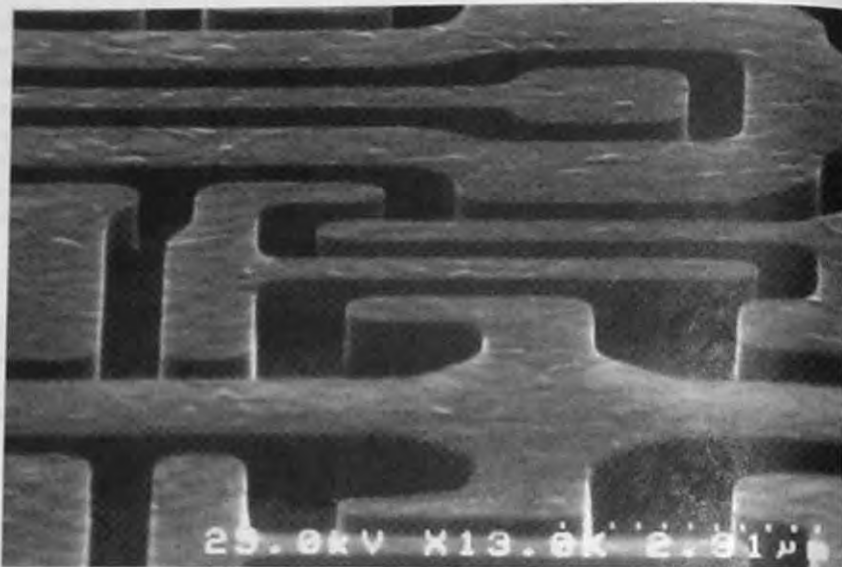


Figure 5.12 0.35- μm TiN/Al/TiN lines and spaces on a wafer maintained at ambient for 72 hours after a microwave strip are not corroded.

in addition to the trench. After filling, the metal and dielectric are planarized by *chemical mechanical polishing* (CMP, see Chapter 8). The advantage of damascene processing is that it eliminates the need for metal etch. This is an important concern as the industry moves from aluminum to copper interconnections.

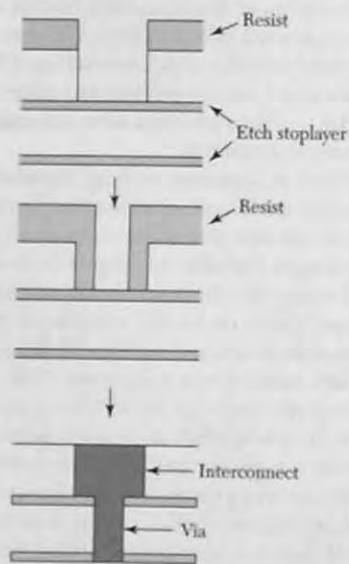


Figure 5.13 Process sequence for the dual damascene process.

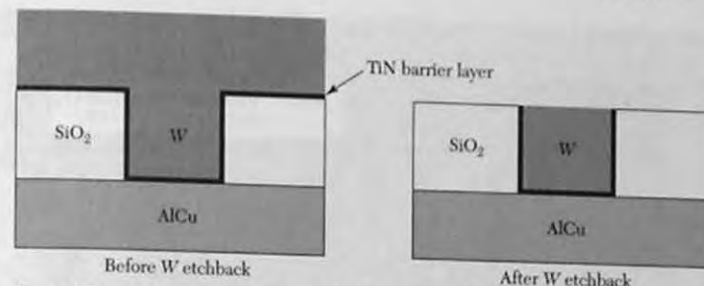


Figure 5.14 Formation of tungsten plug in a contact hole by depositing blanket low-pressure chemical vapor deposition W and then using reaction ion etching etchback.

Low-pressure CVD (LPCVD) tungsten (W) has been widely used for filling contact holes and first-level metallization because of its excellent deposition conformability. Both fluorine- and chlorine-based chemistries etch W and form volatile etch products. An important tungsten etch process is the blanket W etchback to form a W plug. The blanket LPCVD W is deposited on top of a TiN barrier layer, as shown in Figure 5.14. A two-step process is usually used. First, 90% of the W is etched at a high etch rate, and then the etch rate is reduced to remove the remaining W with an etchant that has a high W-to-TiN selectivity.

► 5.3 ETCH SIMULATION

SUPREM may be used to simulate the etching process. However, etch simulation using SUPREM is rudimentary at best. Simulation results may be achieved using the ETCH command, which allows the user to etch all or part of any given layer at the top of the current structure. If the material at the top of the structure is not the material specified, then no etching takes place. If the amount to be etched is not specified, then the entire layer is removed.

EXAMPLE 3

Suppose we want to simulate the etching of 0.3 μm of the oxide grown after the dry-wet-dry sequence in Example 3 of Chapter 3.

SOLUTION The SUPREM input listing is as follows:

TITLE	Etching Example
COMMENT	Initialize silicon substrate
INITIALIZE	<100> Silicon Phosphor Concentration=1e16
COMMENT	Ramp furnace up to 1100 C over 10 minutes in N2
DIFFUSION	Time=10 Temperature=900 Nitrogen T.rate=20
COMMENT	Oxidize the wafers for 5 minutes at 1100 C in dry O2
DIFFUSION	Time=5 Temperature=1100 DryO2
COMMENT	Oxidize the wafers for 120 minutes at 1100 C in wet O2
DIFFUSION	Time=120 Temperature=1100 WetO2
COMMENT	Oxidize the wafers for 5 minutes at 1000 C in dry O2
DIFFUSION	Time=5 Temperature=1100 DryO2
COMMENT	Ramp furnace down to 900 C over 10 minutes in N2
DIFFUSION	Time=10 Temperature=900 Nitrogen T.rate=20

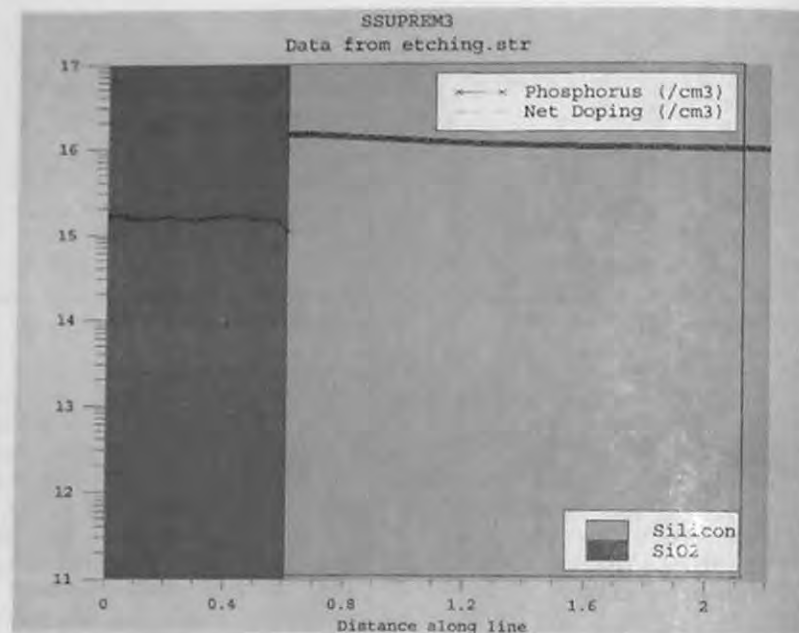


Figure 5.15 Plot of phosphorus concentration as a function of depth into the silicon substrate, using SUPREM.

```

ETCH      Oxide Thickness = 0.3
PRINT     Layers Chemical Concentration Phosphor
PLOT      Active Net Cmin=1e14
STOP      End etching example

```

After oxidation is complete, we print and plot the phosphorus concentration as a function of depth into the silicon substrate. The results are shown in Figure 5.15, which indicates a final oxide thickness of 0.609 μm and depicts the phosphorus incorporation in the oxide layer.

► 5.4 SUMMARY

The two major processes to transfer patterns in IC fabrication are photolithography and etching. Wet chemical etching is used extensively in semiconductor processing. It is particularly suitable for blanket etching. This chapter discussed wet chemical etching processes for silicon and gallium arsenide, insulators, and metal interconnections. Wet chemical etching was used for pattern transfer. However, undercutting of the layer underneath the mask resulted in loss of resolution in the etched pattern.

Dry etching methods are used to achieve high-fidelity pattern transfer. Dry etching is synonymous with plasma-assisted etching. This chapter considered plasma fundamentals and various dry etching systems, which have grown from relatively simple, parallel-plate configurations to complex chambers with multiple frequency generators and a variety of process-control sensors.

The challenges for future etching technology are high etch selectivity, better dimensioned control, low aspect ratio-dependent etching, and low plasma-induced damage. Low-pressure, high-density plasma reactors are necessary to meet these requirements.

As processing evolves from 200-mm to 300-mm and even larger diameter wafers, continued improvements are required for etch uniformity across the wafer. New gas chemistries must be developed to provide the improved selectivity necessary for advanced integration schemes.

► REFERENCES

1. For a more detailed discussion on etching, see Y. J. T. Liu, "Etching," in C. Y. Chang and S. M. Sze, Eds., *ULSI Technology*, McGraw-Hill, New York, 1996.
2. H. Robbins and B. Schwartz, "Chemical Etching of Silicon II, the System HF , HNO_3 , H_2O and $\text{HC}_2\text{H}_3\text{O}_2$," *J. Electrochem. Soc.*, **107**, 108 (1960).
3. K. E. Bean, "Anisotropic Etching in Silicon," *IEEE Trans. Electron Devices*, **ED-25**, 1185 (1978).
4. D. P. Kern, et al., "Practical Aspects of Microfabrication in the 100-nm Region," *Solid State Technol.*, **27**, 2, 127 (1984).
5. S. Iida and K. Ito, "Selective Etching of Gallium Arsenide Crystal in H_2SO_4 - H_2O_2 - H_2O System," *J. Electrochem. Soc.*, **118**, 768 (1971).
6. E. C. Douglas, "Advanced Process Technology for VLSI Circuits," *Solid State Technol.*, **24**, 5, 65 (1981).
7. J. A. Mucha and D. W. Hess, "Plasma Etching," in L. F. Thompson and C. G. Willson, Eds., *Microcircuit Processing: Lithography and Dry Etching*, American Chemical Society, Washington, DC, 1984.
8. M. Armacost, et al., "Plasma-Etching Processes for ULSI Semiconductor Circuits," *IBM J. Res. Dev.*, **43**, 39 (1999).
9. C. O. Jung, et al., "Advanced Plasma Technology in Microelectronics," *Thin Solid Films*, **341**, 112 (1999).

► PROBLEMS

Asterisks denote difficult problems.

SECTION 5.1: WET CHEMICAL ETCHING

1. If the mask and the substrate cannot be etched by a particular etchant, sketch the edge profile of an isotropically etched feature in a film of thickness h_i for (a) etching just to completion, (b) 100% overetch, and (c) 200% overetch.
2. A $\langle 100 \rangle$ -oriented silicon crystal is etched in a KOH solution through a $1.5 \mu\text{m} \times 1.5 \mu\text{m}$ window defined in silicon dioxide. The etch rate normal to $\langle 100 \rangle$ planes is $0.6 \mu\text{m}/\text{min}$. The etch rate ratios are 100:16:1 for the $\langle 100 \rangle$: $\langle 110 \rangle$: $\langle 111 \rangle$ planes. Show the etched profile after 20 seconds, 40 seconds, and 60 seconds.
3. Repeat the previous problem with a $\langle 110 \rangle$ -oriented silicon etched with a thin SiO_2 mask in KOH solution. Show the etched pattern profiles on $\langle 110 \rangle$ Si.
4. A $\langle 100 \rangle$ -oriented silicon wafer 150 mm in diameter is 625 μm thick. The wafer has 1000 $\mu\text{m} \times 1000 \mu\text{m}$ ICs on it. The IC chips are to be separated by orientation-dependent etching. Describe two methods for doing this and calculate the fraction of the surface area that is lost in these processes.

SECTION 5.2: DRY ETCHING

- *5. The average distance traveled by particles between collisions is called the mean free path (λ), $\lambda \approx 5 \times 10^{-3}/P$ (cm), where P is pressure in Torr. In typical plasmas of interest, the chamber pressure ranges from 1 Pa to 150 Pa. What are the corresponding density of gas molecules (cm^{-3}) and the mean free path?
6. Fluorine (F) atoms etch Si at a rate given by

$$\text{Etch rate (nm/min)} = 2.86 \times 10^{-3} \left(\frac{P}{\text{Torr}} \right)^{0.75} \left(\frac{C_{\text{F}}}{\text{cm}^{-3}} \right)^{0.75}$$

where n_F is the concentration of F atoms (cm^{-3}), T the temperature (K), and E_a and R the activation energy (2.48 kcal/mol) and gas constant (1.987 cal-K), respectively. If n_F is 3×10^{15} , calculate the etch rate of Si at room temperature.

7. SiO_2 etched by F atoms could also be expressed by

$$\text{Etch rate (nm/min)} = 0.614 \times 10^{-13} n_F \times T^{1/2} \exp(-E_a/RT)$$

where n_F is 3×10^{15} (cm^{-3}) and E_a is 3.76 kcal/mol. Calculate the etch rate of SiO_2 and etch selectivity of SiO_2 over Si at room temperature.

8. A multiple-step etch process is required for etching a polysilicon gate with thin gate oxide. How do you design an etch process that has no micromasking, has an anisotropic etch profile, and is selective to thin gate oxide?
9. Find the etch selectivity required to etch a 400-nm polysilicon layer without removing more than 1 nm of its underlying gate oxide, assuming that the polysilicon is etched with a process having a 10% etch-rate uniformity.
10. A 1- μm Al film is deposited over a flat field oxide region and patterned with photoresist. The metal is then etched with a mixture of BCl_3/Cl_2 gases at a temperature of 70°C in a Helicon etcher. The selectivity of Al over photoresist is maintained at 3. Assuming a 30% overetch, what is the minimum photoresist thickness required to ensure that the top metal surface is not attacked?
11. In an ECR plasma, a static magnetic field B forces electrons to circulate around the magnetic field lines at an angular frequency, ω_e , that is given by

$$\omega_e = qB/m_e$$

where q is the electronic charge and m_e the electron mass. If the microwave frequency is 2.45 GHz, what is the required magnetic field?

12. What are the major distinctions between traditional reactive ion etching and high-density plasma etching (ECR, ICP, etc.)?
13. Describe how to eliminate the corrosion issues in Al lines after etching with chlorine-based plasma.

Film Deposition

To fabricate discrete devices and integrated circuits, we use many different kinds of thin films. We can classify thin films into five groups: thermal oxides, dielectric layers, epitaxial layers, polycrystalline silicon, and metal films. The growth of thermal oxides was discussed in Chapter 3. This chapter deals with various other techniques for depositing thin films.

Epitaxial growth is closely related to the crystal growth concepts discussed in Chapter 2. It involves the growth of single-crystal semiconductor layers on a single-crystal semiconductor substrate. The word *epitaxy* is derived from the Greek words *epi* (meaning "on") and *taxis* (meaning "arrangement"). The epitaxial layer and the substrate materials may be the same, giving rise to *homoepitaxy*. For example, an *n*-type silicon can be grown epitaxially on an *n*-type silicon substrate. On the other hand, if the epitaxial layer and the substrate are chemically and often crystallographically different, we have *heteroepitaxy*, such as the epitaxial growth of $\text{AlGa}_{1-x}\text{As}$ on GaAs.

Dielectric layers such as silicon dioxide and silicon nitride are used for insulation between conducting layers, for diffusion and ion implantation masks, for capping doped films to prevent the loss of dopants, and for passivation. Polycrystalline silicon, usually referred to as *polysilicon*, is used as a gate electrode material in MOS devices, a conductive material for multilevel metallization, and a contact material for devices with shallow junctions. Metal films such as aluminum and silicides are used to form low-resistance interconnections, ohmic contacts, and rectifying metal-semiconductor barriers.

This chapter covers the following topics:

- Basic techniques of epitaxy, that is, growing a single-crystal layer on a single-crystal substrate
- Structures and defects of lattice-matched and strained-layer epitaxial growth
- Deposition techniques to form low-dielectric-constant and high-dielectric-constant films, as well as polysilicon films
- Deposition techniques to form aluminum and copper interconnections, as well as the related global planarization process
- Characteristics of these thin films and their compatibility with integrated circuit processing

8.1 EPITAXIAL GROWTH TECHNIQUES

In an epitaxial process, the substrate wafer acts as the seed crystal. Epitaxial processes are differentiated from the melt-growth processes described in Chapter 2 in that the epitaxial layer can be grown at a temperature substantially below the melting point, typically

30% to 50% lower. The common techniques for epitaxial growth are *chemical vapor deposition* (CVD) and *molecular beam epitaxy* (MBE).

8.1.1 Chemical Vapor Deposition

CVD is also known as *vapor-phase epitaxy* (VPE). CVD is a process whereby an epitaxial layer is formed by a chemical reaction between gaseous compounds. CVD can be performed at atmospheric pressure (APCVD) or at low pressure (LPCVD).

Figure 8.1 shows three common susceptors for epitaxial growth. Note that the geometric shape of the susceptor provides the name for the reactor: horizontal, pancake, and barrel. All are made from graphite blocks. Susceptors in epitaxial reactors are analogous to crucibles in the crystal growing furnaces. Not only do they mechanically support the wafer, but in induction-heated reactors, they also serve as the source of thermal energy for the reaction. The mechanism of CVD involves a number of steps: (a) the reactants (gases and dopants) are transported to the substrate region; (b) they are transferred to the substrate surface, where they are adsorbed; (c) a chemical reaction occurs, catalyzed at the surface, followed by growth of the epitaxial layer; (d) the gaseous products are desorbed into the main gas stream; and (e) the reaction products are transported out of the reaction chamber.

CVD for Silicon

Four silicon sources have been used for VPE growth. They are silicon tetrachloride (SiCl_4), dichlorosilane (SiH_2Cl_2), trichlorosilane (SiHCl_3), and silane (SiH_4). Silicon tetrachloride has been studied the most and has the widest industrial use. The typical reaction temperature is 1200°C . Other silicon sources are used because of lower reaction temperatures. The

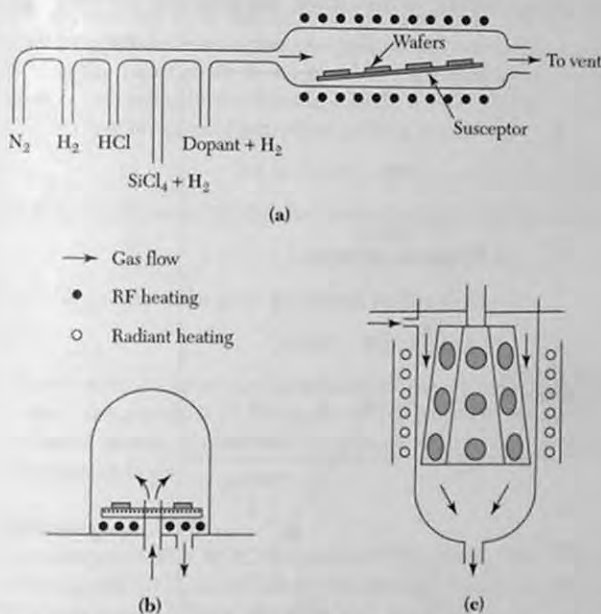
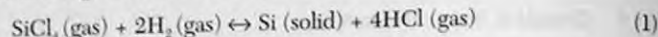
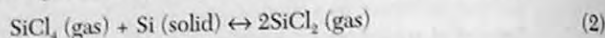


Figure 8.1 Three common susceptors for chemical vapor deposition: (a) horizontal, (b) pancake, and (c) barrel susceptors.

substitution of a hydrogen atom for each chlorine atom from silicon tetrachloride permits about a 50°C reduction in the reaction temperature. The overall reaction of silicon tetrachloride that results in the growth of silicon layers is



An additional competing reaction takes place along with that given in Eq. 1:



As a result, if the silicon tetrachloride concentration is too high, etching, rather than growth of silicon, will take place. Figure 8.2 shows the effect of the concentration of silicon tetrachloride in the gas on the reaction, where the mole fraction is defined as the ratio of the number of molecules of a given species to the total number of molecules.¹ Note that initially the growth rate increases linearly with an increasing concentration of silicon tetrachloride. As the concentration of silicon tetrachloride is increased, a maximum growth rate is reached. Beyond that, the growth rate starts to decrease, and eventually etching of the silicon will occur. Silicon is usually grown in the low-concentration region, as indicated in Figure 8.2.

The reaction of Eq. 1 is reversible; that is, it can take place in either direction. If the carrier gas entering the reactor contains hydrochloric acid, removal or etching will take place. Actually, this etching operation is used for in situ cleaning of the silicon wafer prior to epitaxial growth.

The dopant is introduced at the same time as the silicon tetrachloride during epitaxial growth (Fig. 8.1a). Gaseous diborane (B_2H_6) is used as the *p*-type dopant, whereas phosphine (PH_3) and arsine (AsH_3) are used as *n*-type dopants. Gas mixtures are ordinarily used with hydrogen as the diluent to allow reasonable control of flow rates for the desired doping concentration. The dopant chemistry for arsine is illustrated in Figure 8.3, which shows arsine being adsorbed on the surface, decomposing, and being incorporated

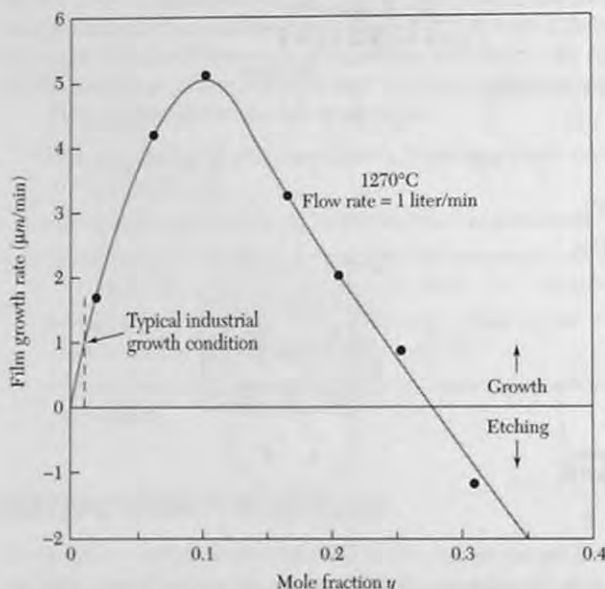


Figure 8.2 Effect of SiCl_4 concentration on silicon epitaxial growth.¹

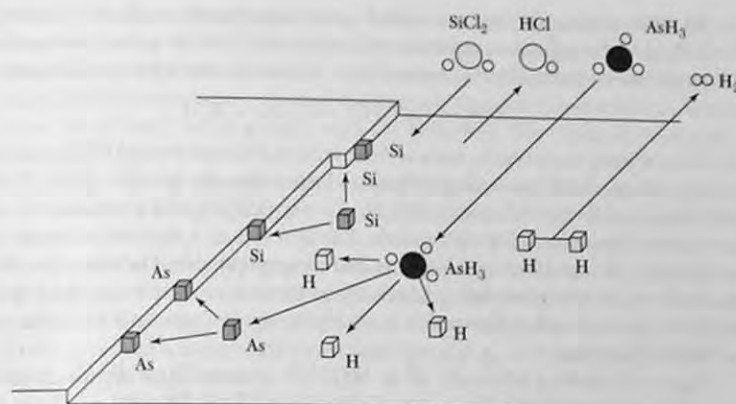
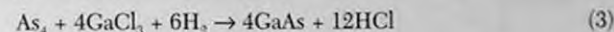


Figure 8.3 Schematic representation of arsenic doping and the growing processes.²

into the growing layer. Figure 8.3 also shows the growth mechanisms at the surface, which are based on the surface adsorption of host atoms (silicon) as well as the dopant atoms (e.g., arsenic) and the movement of these atoms toward the ledge sites.² To give these adsorbed atoms sufficient mobility for finding their proper positions within the crystal lattice, epitaxial growth requires relatively high temperatures.

CVD for Gallium Arsenide

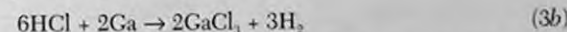
For gallium arsenide, the basic setup is similar to that shown in Figure 8.1a. Because gallium arsenide decomposes into gallium and arsenic upon evaporation, its direct transport in the vapor phase is not possible. One approach is the use of As_4 for the arsenic component and gallium chloride (GaCl_3) for the gallium component. The overall reaction leading to epitaxial growth of gallium arsenide is



The As_4 is generated by thermal decomposition of arsine (AsH_3):



and the gallium chloride is generated by the reaction

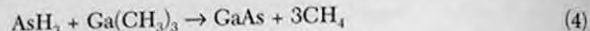


The reactants are introduced into a reactor with a carrier gas (e.g., H_2). The gallium arsenide wafers are typically held within the 650°C to 850°C temperature range. There must be sufficient arsenic overpressure to prevent thermal decomposition of the substrate and the growing layer.

Metalorganic CVD

Metalorganic CVD (MOCVD) is also a VPE process based on pyrolytic reactions. Unlike conventional CVD, MOCVD is distinguished by the chemical nature of the precursor. It is important for those elements that do not form stable hydrides or halides, but that do form stable metalorganic compounds with reasonable vapor pressure. MOCVD has been extensively applied in the heteroepitaxial growth of III-V and II-VI compounds.

To grow GaAs, we can use metalorganic compounds such as trimethylgallium $[\text{Ga}(\text{CH}_3)_3]$ for the gallium component and arsine (AsH_3) for the arsenic component. Both chemicals can be transported in vapor form into the reactor. The overall reaction is



For Al-containing compounds, such as AlAs, trimethylaluminum $[\text{Al}(\text{CH}_3)_3]$ can be used. During epitaxy, the GaAs is doped by introducing dopants in vapor form. Diethylzinc $[\text{Zn}(\text{C}_2\text{H}_5)_2]$ and diethylcadmium $[\text{Cd}(\text{C}_2\text{H}_5)_2]$ are typical *p*-type dopants, and silane (SiH_4) is an *n*-type dopant for III-V compounds. The hydrides of sulfur and selenium or tetramethyltin are also used for *n*-type dopants, and chromyl chloride is used to dope chromium into GaAs to form semiinsulating layers. Since these compounds are highly poisonous and often spontaneously inflammable in air, rigorous safety precautions are necessary in the MOCVD process.

Figure 8.4 shows a schematic of an MOCVD reactor.³ Typically, the metalorganic compound is transported to the quartz reaction vessel by hydrogen carrier gas, where it is mixed with AsH_3 in the case of GaAs growth. The chemical reaction is induced by heating the gases to 600°C to 800°C above a substrate placed on a graphite susceptor using radio frequency heating. A pyrolytic reaction forms the GaAs layer. The advantages of using metalorganics are that they are volatile at moderately low temperatures and that there are no troublesome liquid Ga or In sources in the reactor.

8.1.2 Molecular Beam Epitaxy

MBE is an epitaxial process involving the reaction of one or more thermal beams of atoms or molecules with a crystalline surface under ultrahigh-vacuum conditions ($\sim 10^{-8}$ Pa).⁴

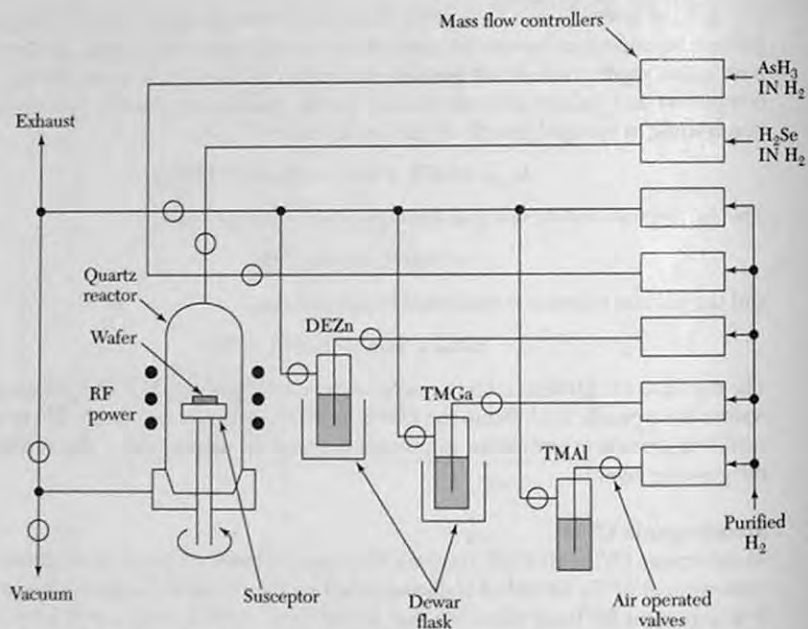


Figure 8.4 Schematic diagram of a vertical atmospheric-pressure MOCVD reactor.³ DEZn, diethylzinc $[\text{Zn}(\text{C}_2\text{H}_5)_2]$; TMGa, trimethylgallium $[\text{Ga}(\text{CH}_3)_3]$; TMAI, trimethylaluminum $[\text{Al}(\text{CH}_3)_3]$.

MBE can achieve precise control of both chemical compositions and doping profiles. Single-crystal, multilayer structures with dimensions on the order of atomic layers can be grown using MBE. Thus, the MBE method enables the precise fabrication of semiconductor heterostructures having thin layers from a fraction of a micron down to a monolayer. In general, MBE growth rates are quite low. For GaAs, for example, a value of 1 $\mu\text{m/hr}$ is typical.

Figure 8.5 shows a schematic of an MBE system for gallium arsenide and related III-V compounds, such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$. The system represents the ultimate in film deposition control, cleanliness, and in situ chemical characterization capability. Separate effusion ovens made of pyrolytic boron nitride are used for Ga, As, and the dopants. All the effusion ovens are housed in an ultrahigh-vacuum chamber ($\sim 10^{-8}$ Pa). The temperature of each oven is adjusted to give the desired evaporation rate. The substrate holder rotates continuously to achieve uniform epitaxial layers (e.g., $\pm 1\%$ in doping variations and $\pm 0.5\%$ in thickness variations).

To grow GaAs, an overpressure of As is maintained, since the sticking coefficient of Ga to GaAs is unity, whereas that for As is zero, unless there is a previously deposited Ga layer. For a silicon MBE system, an electron gun is used to evaporate silicon. One or more effusion ovens are used for the dopants. Effusion ovens behave like small-area sources and exhibit a $\cos\theta$ emission, where θ is the angle between the direction of the source and the normal to the substrate surface.

MBE uses an evaporation method in a vacuum system. An important parameter for vacuum technology is the molecular impingement rate; that is, how many molecules impinge on a unit area of the substrate per unit time. The impingement rate (ϕ) is a function of the molecular weight, temperature, and pressure. The rate is derived in Appendix H and can be expressed as⁵

$$\phi = P(2\pi mkT)^{-1/2} \quad (5)$$

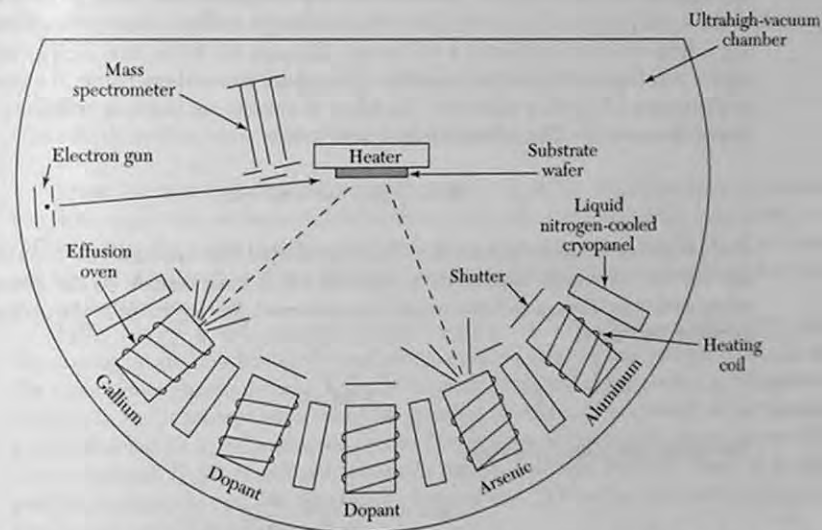


Figure 8.5 Arrangement of the sources and substrate in a conventional molecular beam epitaxy (MBE) system. (Courtesy of M. B. Panish, Bell Laboratories.)

or

$$\phi = 2.64 \times 10^{20} \left(\frac{P}{\sqrt{MT}} \right) \text{ molecules/cm}^2\text{-s} \quad (5a)$$

where P is the pressure in Pa, m is the mass of a molecule in kg, k is Boltzmann's constant in J/K, T is the temperature in degrees Kelvin, and M is the molecular weight. Therefore, at 300 K and 10^{-4} Pa pressure, the impingement rate is 2.7×10^{14} molecules/cm²-s for oxygen ($M = 32$).

EXAMPLE 1

At 300 K, the molecular diameter of oxygen is 3.64 Å, and the number of molecules per unit area N_i is 7.54×10^{14} cm⁻². Find the time required to form a monolayer of oxygen at pressures of 1, 10^{-4} , and 10^{-8} Pa.

SOLUTION The time required to form a monolayer (assuming 100% sticking) is obtained from the impingement rate:

$$t = \frac{N_i}{\phi} = \frac{N_i \sqrt{MT}}{2.64 \times 10^{20} P}$$

Therefore,

$$\begin{aligned} t &= 2.8 \times 10^{-4} = 0.28 \text{ ms} \quad \text{at } 1 \text{ Pa} \\ &= 2.8 \text{ s} \quad \text{at } 10^{-4} \text{ Pa} \\ &= 7.7 \text{ hr} \quad \text{at } 10^{-8} \text{ Pa} \end{aligned}$$

To avoid contamination of the epitaxial layer, it is of paramount importance to maintain ultrahigh-vacuum conditions ($\sim 10^{-8}$ Pa) for the MBE process. ◀

During molecular motion, molecules will collide with one another. The average distance traversed by all the molecules between successive collisions with each other is defined as the *mean free path*. It can be derived from a simple collision theory. A molecule having a diameter d and a velocity v will move a distance $v\delta t$ in the time δt . The molecule suffers a collision with another molecule if its center is anywhere within the distance d of the center of another molecule. Therefore, it sweeps out (without collision) a cylinder of diameter $2d$. The volume of the cylinder is

$$\delta V = \frac{\pi}{4} (2d)^2 v \delta t = \pi d^2 v \delta t \quad (6)$$

Since there are n molecules/cm³, the volume associated with one molecule is on the average $1/n$ cm³. When the volume δV is equal to $1/n$, it must contain on the average one other molecule. Thus, a collision would have occurred. Setting $\tau = \delta t$ as the average time between collisions,

$$\frac{1}{n} = \pi d^2 v \tau \quad (7)$$

The mean free path (λ) is then

$$\lambda = v\tau = \frac{1}{\pi n d^2} = \frac{kT}{\pi P d^2} \quad (8)$$

A more rigorous derivation gives

$$\lambda = \frac{kT}{\sqrt{2} \pi P d^2} \quad (9)$$

and

$$\lambda = \frac{0.66}{P(\text{in Pa})} \text{ cm} \quad (10)$$

for air molecules (equivalent molecular diameter of 3.7 Å) at room temperature. Therefore, at a system pressure of 10^{-8} Pa, λ would be 660 km.

EXAMPLE 2

Assume an effusion oven geometry of area $A = 5$ cm² and a distance L between the top of the oven and the gallium arsenide substrate of 10 cm. Calculate the MBE growth rate for the effusion oven filled with gallium arsenide at 900°C. The surface density of gallium atoms is 6×10^{14} cm⁻², and the average thickness of a monolayer is 2.8 Å.

SOLUTION On heating gallium arsenide, the volatile arsenic vaporizes first, leaving a gallium-rich solution. Therefore, only the pressures marked "Ga-rich" in Figure 2.11 are of interest. The pressure at 900°C is 5.5×10^{-3} Pa for gallium and 1.1 Pa for arsenic (As₂). The arrival rate can be obtained from the impingement rate (Eq. 5a) by multiplying it by $A/\pi L^2$:

$$\text{Arrival rate} = 2.64 \times 10^{20} \left(\frac{P}{\sqrt{MT}} \right) \left(\frac{A}{\pi L^2} \right) \text{ molecules/cm}^2\text{-s}$$

The molecular weight (M) is 69.72 for Ga and 74.92×2 for As₂. Substituting values of P , M , and T (1173 K) into the above equation gives

$$\begin{aligned} \text{Arrival rate} &= 8.2 \times 10^{14} / \text{cm}^2\text{-s for Ga} \\ &= 1.1 \times 10^{16} / \text{cm}^2\text{-s for As}_2 \end{aligned}$$

The growth rate of gallium arsenide is governed by the arrival rate of gallium. The growth rate is

$$\frac{8.2 \times 10^{14} \times 2.8}{6 \times 10^{14}} = 3.8 \text{ Å/s} = 23 \text{ nm/min}$$

Note that the growth rate is relatively low compared with that of VPE. ◀

There are two ways to clean a surface in situ for MBE. High-temperature baking can decompose the native oxide and remove other adsorbed species by evaporation or diffusion into the wafer. Another approach is to use a low-energy ion beam of an inert gas to sputter-clean the surface, followed by a low-temperature annealing to reorder the surface lattice structure.

MBE can use a wide variety of dopants (compared with CVD and MOCVD), and the doping profile can be exactly controlled. However, the doping process is similar to the vapor-phase growth process: A flux of evaporated dopant atoms arrives at a favorable lattice site and is incorporated along the growing interface. Fine control of the doping profile is achieved by adjusting the dopant flux relative to the flux of silicon atoms (for silicon epitaxial films) or gallium atoms (for gallium arsenide epitaxial films). It is also possible to dope the epitaxial film using a low-current, low-energy ion beam to implant the dopant (see Chapter 7).

The substrate temperatures for MBE range from 400°C to 900°C, and the growth rates range from 0.001 to 0.3 $\mu\text{m}/\text{min}$. Because of low-temperature processing and the low growth rate, many unique doping profiles and alloy compositions not obtainable from conventional CVD can be produced in MBE. Many novel structures have been made using MBE. These include the *superlattice*, which is a periodic structure consisting of alternating ultrathin layers with a period less than the electron mean free path (e.g., GaAs/Al_xGa_{1-x}As, with each layer 10 nm or less in thickness), and heterojunction field-effect transistors.

A further development in MBE has replaced the group III elemental sources by metalorganic compounds such as trimethylgallium (TMG) or triethylgallium (TEG). This approach is called *metalorganic molecular beam epitaxy* (MOMBE) and is also referred to as *chemical beam epitaxy* (CBE). Although closely related to MOCVD, it is considered a special form of MBE. The metalorganics are sufficiently volatile that they can be admitted directly into the MBE growth chamber as a beam and are not decomposed before forming the beam. The dopants are generally elemental sources, typically Be for *p*-type and Si or Sn for *n*-type GaAs epitaxial layers.

8.2 STRUCTURES AND DEFECTS IN EPITAXIAL LAYERS

8.2.1 Lattice-Matched and Strained-Layer Epitaxy

For conventional homoepitaxial growth, a single-crystal semiconductor layer is grown on a single-crystal semiconductor substrate. The semiconductor layer and the substrate are the same material having the same lattice constant. Therefore, homoepitaxy is, by definition, a lattice-matched epitaxial process. The homoepitaxial process offers one important means of controlling the doping profiles so that device and circuit performance can be optimized. For example, an *n*-type silicon layer with a relatively low doping concentration can be grown epitaxially on an *n*⁺ silicon substrate. This structure substantially reduces the series resistance associated with the substrate.

For heteroepitaxy, the epitaxial layer and the substrate are two different semiconductors, and the epitaxial layer must be grown in such a way that an idealized interfacial structure is maintained. This implies that atomic bonding across the interface must be continuous. Therefore, the two semiconductors must either have the same lattice spacing or be able to deform to adopt a common spacing. These two cases are referred to as *lattice-matched epitaxy* and *strained-layer epitaxy*, respectively.

Figure 8.6a shows a lattice-matched epitaxy where the substrate and the film have the same lattice constant. An important example is the epitaxial growth of Al_xGa_{1-x}As on a GaAs substrate where for any *x* between 0 and 1, the lattice constant of Al_xGa_{1-x}As differs from that of GaAs by less than 0.13%.

For the lattice-mismatched case, if the epitaxial layer has a larger lattice constant and is flexible, it will be compressed in the plane of growth to conform to the substrate spacing. Elastic forces then compel it to dilate in a direction perpendicular to the interface. This type of structure is called *strained-layer epitaxy* and is illustrated in Figure 8.6b. On the other hand, if the epitaxial layer has a smaller lattice constant, it will be dilated in the plane of growth and compressed in a direction perpendicular to the interface. In the above strained-layer epitaxy, as the strained-layer thickness increases, the total number of atoms under strain of the distorted atomic bonds grows, and at some point, misfit dislocations are nucleated to relieve the homogeneous strain energy. This thickness is referred to as the *critical layer thickness* for the system. Figure 8.6c shows the case in which there are edge dislocations at the interface.

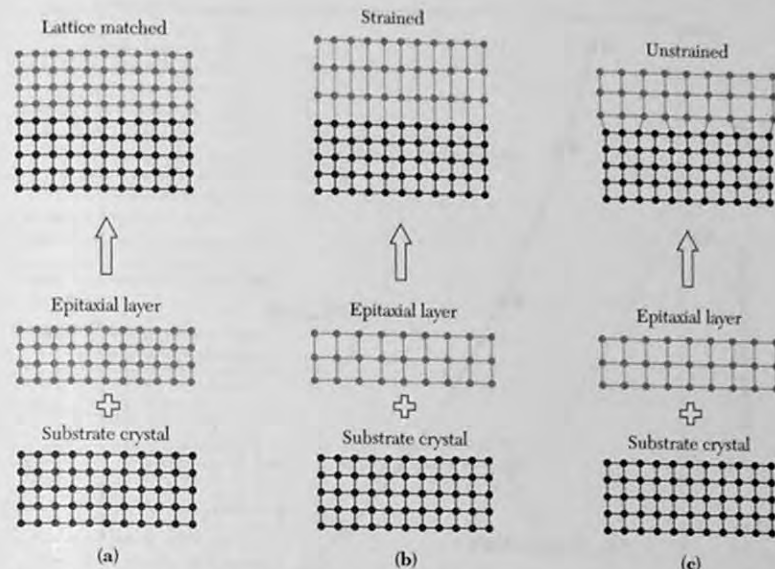


Figure 8.6 Schematic illustration of (a) lattice-matched, (b) strained,⁶ and (c) relaxed heteroepitaxial structures. Homoepitaxy is structurally identical to the lattice-matched heteroepitaxy.

The critical layer thicknesses for two material systems are shown in Figure 8.7.⁷ The upper curve is for the strained-layer epitaxy of a Ge_{0.3}Si_{0.7} layer on a silicon substrate, and the lower curve is for a Ga_{1-x}In_xAs layer on a GaAs substrate. For example, for Ge_{0.3}Si_{0.7} on silicon, the maximum epitaxial thickness is about 70 nm. For thicker films, edge dislocations will occur.

A related heteroepitaxial structure is the *strained-layer superlattice* (SLS). A superlattice is an artificial one-dimensional periodic structure constituted by different materials with a period of about 10 nm. Figure 8.8 shows⁴ an SLS having two semiconductors with different equilibrium lattice constants $a_1 > a_2$, grown in a structure with a common inplane lattice constant b , where $a_1 > b > a_2$. For sufficiently thin layers, the lattice mismatch is accommodated by uniform strains in the layers. Under these conditions, no misfit dislocations are generated at the interfaces, so high-quality crystalline materials can be obtained. These artificially structured materials can be grown by MBE. These materials provide a new area in semiconductor research and permit new solid-state devices, especially for high-speed and photonic applications.

8.2.2 Defects in Epitaxial Layers

Defects in epitaxial layers will degrade device properties. For example, defects can result in reduced mobility or increased leakage current. The defects in epitaxial layers can be categorized into five groups:

1. *Defects from the substrates.* These defects may propagate from the substrate into the epitaxial layer. To avoid these defects, dislocation-free semiconductor substrates are required.

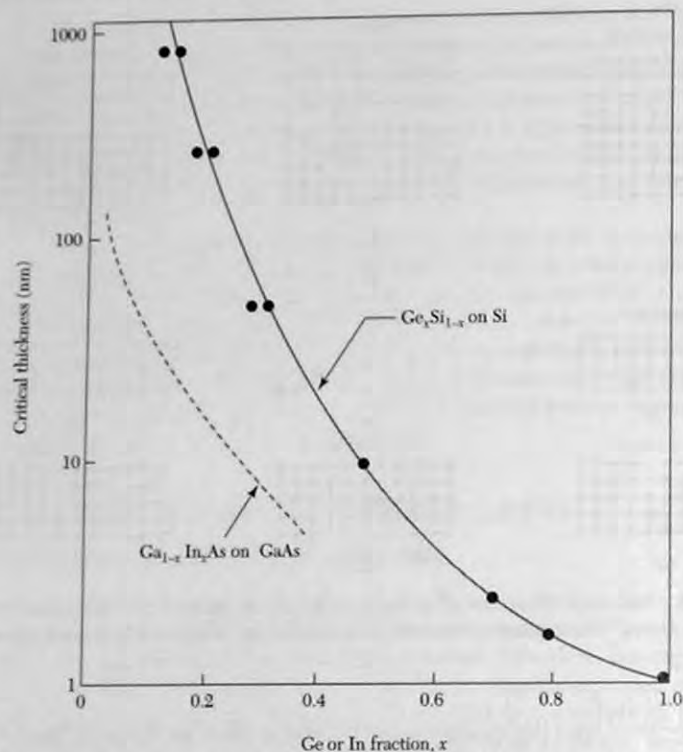


Figure 8.7 Experimentally determined critical layer thickness for defect-free, strained-layer epitaxy of $\text{Ge}_x\text{Si}_{1-x}$ on Si, and $\text{Ga}_{1-x}\text{In}_x\text{As}$ on GaAs.⁷

2. *Defects from the interface.* Oxide precipitates or any contamination at the interface of the epitaxial layer and substrate may cause the formation of mis-oriented clusters or nuclei containing stacking faults. These clusters and stacking faults may coalesce with normal nuclei and grow into the film in the shape of an inverted pyramid. To avoid these defects, the surface of the substrate must be thoroughly cleaned. In addition, an in situ etchback may be used, such as the reversible reaction of Eq. 1.
3. *Precipitates or dislocation loops.* Their formation is due to supersaturation of impurities or dopants. Epitaxial layers containing very high intentional or unintentional dopants or impurity concentrations are susceptible to such defects.
4. *Low-angle grain boundaries and twins.* Any misoriented areas of an epitaxial film during growth may meet and coalesce to form these defects.
5. *Edge dislocations.* These are formed in the heteroepitaxy of two lattice-mismatched semiconductors. If both lattices are rigid, they will retain their fundamental lattice spacings, and the interface will contain rows of misbonded atoms described as misfit or edge dislocations. The edge dislocations can also form in a strained layer when the layer thickness becomes larger than the critical layer thickness.

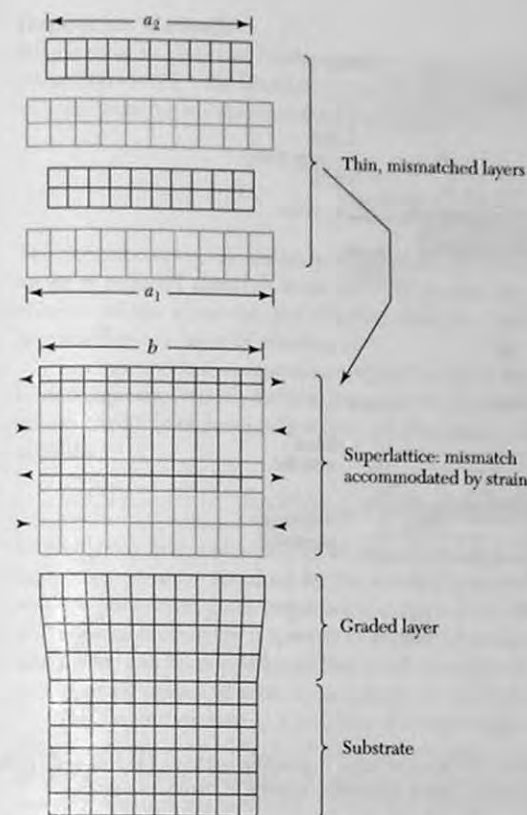


Figure 8.8 Illustration of the elements and formation of a strained-layer superlattice.⁴ Arrows show the direction of the strain.

► 8.3 DIELECTRIC DEPOSITION

Deposited dielectric films are used mainly for insulation and passivation of discrete devices and integrated circuits. There are three commonly used deposition methods: atmospheric-pressure CVD, low-pressure CVD (LPCVD), and plasma-enhanced chemical vapor deposition (PECVD, or plasma deposition). PECVD is an energy-enhanced CVD method in which plasma energy is added to the thermal energy of a conventional CVD system. Considerations in selecting a deposition process are the substrate temperature, the deposition rate and film uniformity, the morphology, the electrical and mechanical properties, and the chemical composition of the dielectric films.

The reactor for atmospheric-pressure CVD is similar to the one shown in Figure 3.2, except that different gases are used at the gas inlet. In a hot-wall, reduced-pressure reactor like the one shown in Figure 8.9a, the quartz-tube is heated by a three-zone furnace, and gas is introduced at one end and pumped out at the opposite end. The semiconductor wafers are held vertically in a slotted quartz boat.⁸ The quartz-tube wall is hot because it is adjacent to the furnace, in contrast to a cold-wall reactor such as the horizontal epitaxial reactor that uses radio frequency (rf) heating.

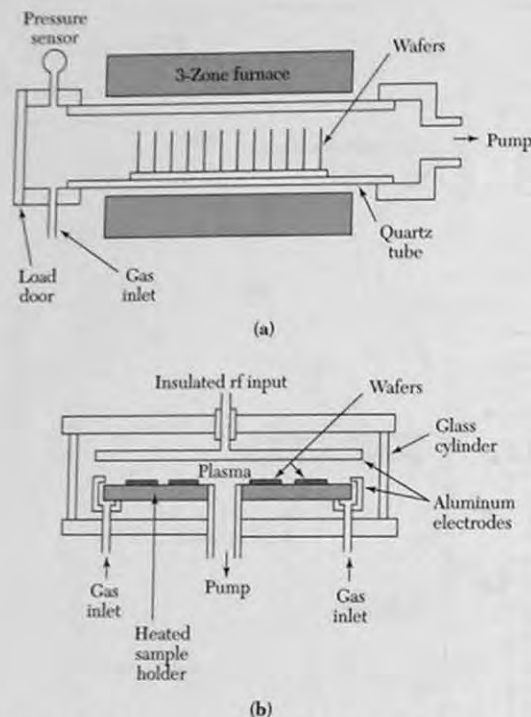


Figure 8.9 Schematic diagrams of chemical vapor deposition reactors. (a) Hot-wall, reduced-pressure reactor. (b) Parallel-plate plasma deposition reactor. rf, radio frequency.

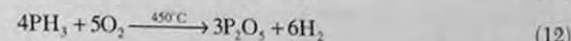
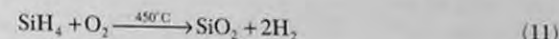
The parallel-plate, radial-flow PECVD reactor shown in Figure 8.9b consists of a cylindrical glass or aluminum chamber sealed with aluminum endplates. Inside are two parallel aluminum electrodes. An rf voltage is applied to the upper electrode, whereas the lower electrode is grounded. The rf voltage causes a plasma discharge between the electrodes. Wafers are placed on the lower electrode, which is heated between 100°C and 400°C by resistance heaters. The reaction gases flow through the discharge from outlets located along the circumference of the lower electrode. The main advantage of this reactor is its low deposition temperature. However, its capacity is limited, especially for large-diameter wafers, and the wafers may become contaminated if loosely adhering deposits fall on them.

8.3.1 Silicon Dioxide

CVD silicon dioxide cannot replace thermally grown oxides, because the best electrical properties are obtained with thermally grown films. CVD oxides are used instead to complement thermal oxides. A layer of undoped silicon dioxide is used to insulate multilevel metallization, to mask ion implantation and diffusion, and to increase the thickness of thermally grown field oxides. Phosphorus-doped silicon dioxide is used both as an insulator between metal layers and as a final passivation layer over devices. Oxides doped with phosphorus, arsenic, or boron are used occasionally as diffusion sources.

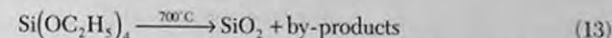
Deposition Methods

Silicon dioxide films can be deposited by several methods. For low-temperature deposition (300–500°C), the films are formed by reacting silane, dopant, and oxygen. The chemical reactions for phosphorus-doped oxides are



The deposition process can be performed either at atmospheric pressure in a CVD reactor or at reduced pressure in an LPCVD reactor (Fig. 8.9a). The low deposition temperature of the silane–oxygen reaction makes it a suitable process when films must be deposited over a layer of aluminum.

For intermediate-temperature deposition (500–800°C), silicon dioxide can be formed by decomposing tetraethylorthosilicate, $\text{Si}(\text{OC}_2\text{H}_5)_4$, in an LPCVD reactor. The compound, abbreviated TEOS, is vaporized from a liquid source. The TEOS compound decomposes as follows:

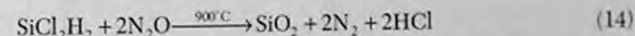


forming both SiO_2 and a mixture of organic and organosilicon by-products. Although the higher temperature required for the reaction prevents its use over aluminum, it is suitable for polysilicon gates requiring a uniform insulating layer with good step coverage. The good step coverage is a result of enhanced surface mobility at higher temperatures. The oxides can be doped by adding small amounts of the dopant hydrides (phosphines, arsine, or diborane), similar to the process in epitaxial growth.

The deposition rate as a function of temperature varies as $\exp(-E_a/kT)$, where E_a is the activation energy. The E_a of the silane–oxygen reaction is quite low: about 0.6 eV for undoped oxides and almost zero for phosphorus-doped oxide. In contrast, E_a for the TEOS reaction is much higher: about 1.9 eV for undoped oxide and 1.4 eV when phosphorus doping compounds are present. The dependence of the deposition rate on TEOS partial pressure is proportional to $(1 - e^{-P/P_0})$, where P is the TEOS partial pressure and P_0 is about 30 Pa. At low TEOS partial pressures, the deposition rate is determined by the rate of the surface reaction. At high partial pressures, the surface becomes nearly saturated with adsorbed TEOS, and the deposition rate becomes essentially independent of TEOS pressure.⁸

Recently, atmospheric-pressure and low-temperature CVD processes using TEOS and ozone (O_3) have been proposed,⁹ as shown in Figure 8.10. This CVD technology produces oxide films with high conformality and low viscosity under low deposition temperature. The shrinkage of oxide film during annealing is also a function of ozone concentration, as shown in Figure 8.11. Because of their porosity, O_3 –TEOS CVD oxides are often accompanied by plasma-assisted oxides to permit planarization in ULSI processing.

For high-temperature deposition (900°C), silicon dioxide is formed by reacting dichlorosilane, SiCl_2H_2 , with nitrous oxide at reduced pressure:



This deposition gives excellent film uniformity and is sometimes used to deposit insulating layers over polysilicon.

Properties of Silicon Dioxide

Table 8.1 lists deposition methods and properties of silicon dioxide films.⁸ In general, there is a direct correlation between deposition temperature and film quality. At higher

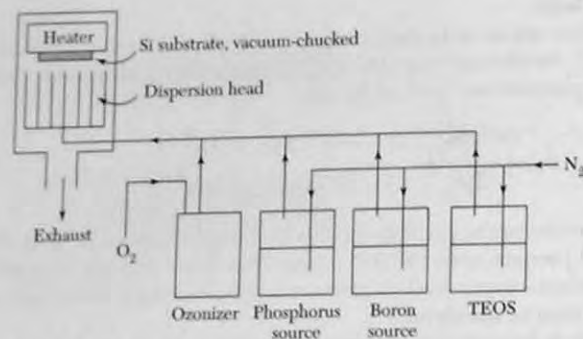


Figure 8.10 Experimental apparatus for the O_3 -TEOS chemical vapor deposition system.

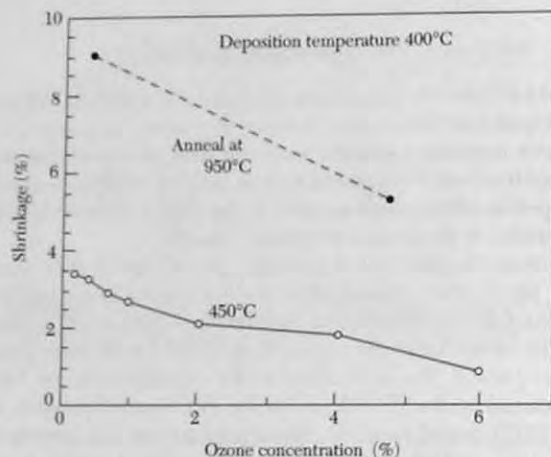


Figure 8.11 Dependence of the shrinkage of the O_3 -TEOS CVD film on ozone concentration using annealing. (Courtesy of SAMCO Company, Japan.)

TABLE 8.1 Properties of Silicon Dioxide Films

Property	Thermally Grown at 1000°C	$SiH_4 + O_2$ at 450°C	TEOS at 700°C	$SiCl_2H_2 + N_2O$ at 900°C
Composition	SiO_2	$SiO_2 (H)$	SiO_2	$SiO_2(Cl)$
Density (g/cm^3)	2.2	2.1	2.2	2.2
Refractive index	1.46	1.44	1.46	1.46
Dielectric strength (10^6 V/cm)	>10	8	10	10
Etch rate ($\text{\AA}/min$) (100:1 $H_2O:HF$)	30	60	30	30
Etch rate ($\text{\AA}/min$) (buffered HF)	440	1200	450	450
Step coverage	—	Nonconformal	Conformal	Conformal

temperatures, deposited oxide films are structurally similar to silicon dioxide that has been thermally grown.

The lower densities occur in films deposited below 500°C. Heating deposited silicon dioxide at temperatures between 600°C and 1000°C causes densification, during which the oxide thickness decreases, whereas the density increases to 2.2 g/cm^3 . The refractive index of silicon dioxide is 1.46 at a wavelength of 0.6328 μm . Oxides with lower indices are porous, such as the oxide resulting from silane-oxygen deposition, which has a refractive index of 1.44. The porous nature of the oxide also is responsible for the lower dielectric strength, which is the applied electric field that will cause a high current to flow in the oxide film. The etch rates of oxides in a hydrofluoric acid solution depend on deposition temperature, annealing history, and dopant concentration. Usually, higher-quality oxides are etched at lower rates.

Step Coverage

Step coverage relates the surface topography of a deposited film to the various steps on the semiconductor substrate. In the illustration of ideal, or *conformal*, step coverage shown in Figure 8.12a, film thickness is uniform along all surfaces of the step. The uniformity of the film thickness, regardless of topography, is due to the rapid migration of reactants after adsorption on the step surfaces.¹⁰

Figure 8.12b shows an example of nonconformal step coverage, which results when the reactants adsorb and react without significant surface migration. In this instance, the

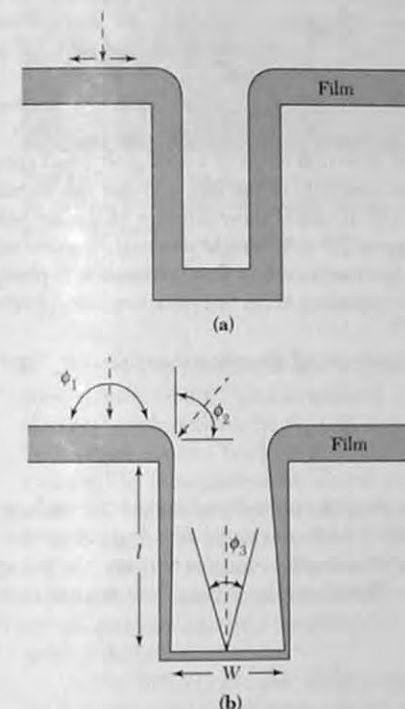


Figure 8.12 Step coverage of deposited films.¹⁰ (a) Conformal step coverage. (b) Nonconformal step coverage.

deposition rate is proportional to the arrival angle of the gas molecules. Reactants arriving along the top horizontal surface come from many different angles, and ϕ_1 , the arrival angle, varies in two dimensions, from 0° to 180° , whereas reactants arriving at the top of a vertical wall have an arrival angle (ϕ_2) that varies from 0° to 90° . Thus, the film thickness on the top surface is double that of a wall surface. Further down the wall, ϕ_3 is related to the width of the opening, and the film thickness is proportional to

$$\phi_3 \equiv \arctan \frac{W}{l} \quad (15)$$

where l is the distance from the top surface and W is the width of the opening. This type of step coverage is thin along the vertical walls, with a possible crack at the bottom of the step caused by self-shadowing.

Silicon dioxide formed by TEOS decomposition at reduced pressure gives a nearly conformal coverage due to rapid surface migration. Similarly, the high-temperature dichlorosilane-nitrous oxide reaction also results in conformal coverage. However, during silane-oxygen deposition, no surface migration takes place, and the step coverage is determined by the arrival angle. Most evaporated or sputtered materials have a step coverage similar to that in Figure 8.12b.

P-Glass Flow

A smooth topography is usually required for the deposited silicon dioxide used as an insulator between metal layers. If the oxide used to cover the lower metal layer is concave, circuit failure may result from an opening that may occur in the upper metal layer during deposition. Because phosphorus-doped silicon dioxide (P-glass) deposited at low temperatures becomes soft and flows upon heating, it provides a smooth surface and is often used to insulate adjacent metal layers. This process is called *P-glass flow*.

Figure 8.13 shows four cross sections of scanning electron microscope photographs of P-glass covering a polysilicon step.¹⁰ All samples are heated in steam at 1100°C for 20 minutes. Figure 8.13a shows a sample of glass that contains a negligibly small amount of phosphorus and does not flow. Note the concavity of the film and that the corresponding angle (θ) is about 120° . Figures 8.13b, c, and d show samples of P-glass with progressively higher phosphorus contents, up to 7.2 wt% (weight percent). In these samples, the decreasing step angles of the P-glass layer indicate how flow increases with phosphorus concentration. P-glass flow depends on annealing time, temperature, phosphorus concentration, and the annealing ambient.¹⁰

The angle θ as a function of weight percent of phosphorus as shown in Figure 8.13 can be approximated by

$$\theta \cong 120^\circ \left(\frac{10 - \text{wt}\%}{10} \right) \quad (16)$$

If we want an angle smaller than 45° , we require a phosphorus concentration larger than 6 wt%. However, at concentrations above 8 wt%, the metal film (e.g., aluminum) may be corroded by the acid products formed during the reaction between the phosphorus in the oxide and atmospheric moisture. Therefore, the P-glass flow process uses phosphorus concentrations of 6 to 8 wt%.

8.3.2 Silicon Nitride

It is difficult to grow silicon nitride by thermal nitridation (e.g., with ammonia, NH_3) because of its slow growth rate and high growth temperature. However, silicon nitride

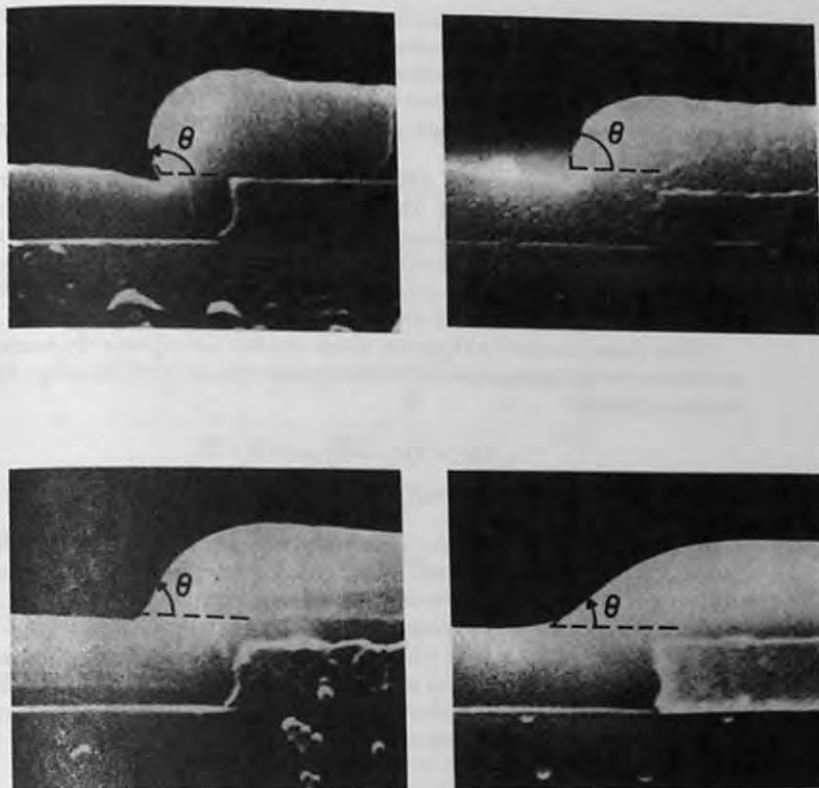
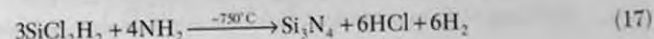


Figure 8.13 Scanning electron micrographs ($10,000\times$) of samples annealed in steam at 1100°C for 20 minutes for the following weight percent of phosphorus:¹⁰ (a) 0 wt%, (b) 2.2 wt%, (c) 4.6 wt%, and (d) 7.2 wt%.

films can be deposited by an intermediate-temperature (750°C) LPCVD process or a low-temperature (300°C) plasma-assisted CVD process.^{11,12} The LPCVD films are of stoichiometric composition (Si_3N_4) with high density ($2.9\text{--}3.1\text{ g/cm}^3$). These films can be used to passivate devices because they serve as good barriers to the diffusion of water and sodium. The films also can be used as masks for the selective oxidation of silicon because silicon nitride oxidizes very slowly and prevents the underlying silicon from oxidizing. The films deposited by plasma-assisted CVD are not stoichiometric and have a lower density ($2.4\text{--}2.8\text{ g/cm}^3$). Because of the low deposition temperature, silicon nitride films can be deposited over fabricated devices and serve as their final passivation. Plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion.

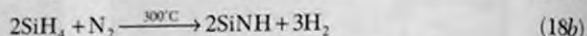
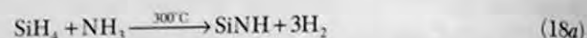
In the LPCVD process, dichlorosilane and ammonia react at reduced pressure to deposit silicon nitride at temperatures between 700°C and 800°C . The reaction is



Good film uniformity and high wafer throughput (i.e., wafers processed per hour) are advantages of the reduced-pressure process. As in the case of oxide deposition, silicon nitride deposition is controlled by temperature, pressure, and reactant concentration. The activation energy for deposition is about 1.8 eV. The deposition rate increases with increasing total pressure or dichlorosilane partial pressure and decreases with an increasing ammonia-to-dichlorosilane ratio.

Silicon nitride deposited by LPCVD is an amorphous dielectric containing up to 8 atomic percent (at%) hydrogen. The etch rate in buffered HF is less than 1 nm/min. The film has a very high tensile stress of approximately 10^{10} dynes/cm², which is nearly 10 times that of TEOS-deposited SiO₂. Films thicker than 200 nm may crack because of the very high stress. The resistivity of silicon nitride at room temperature is about 10^{16} Ω-cm. Its dielectric constant is 7, and its dielectric strength is 10^7 V/cm.

In the plasma-assisted CVD process, silicon nitride is formed either by reacting silane and ammonia in an argon plasma or by reacting silane in a nitrogen discharge. The reactions are as follows:



The products depend strongly on deposition conditions. The radial-flow, parallel-plate reactor (Fig. 8.9b) is used to deposit the films. The deposition rate generally increases with increasing temperature, power input, and reactant gas pressure.

Large concentrations of hydrogen are contained in plasma-deposited films. The plasma nitride (also referred to as SiN) used in semiconductor processing generally contains 20 to 25 at% hydrogen. Films with low tensile stress ($\sim 2 \times 10^9$ dynes/cm²) can be prepared by plasma deposition. Film resistivities range from 10^5 to 10^{21} Ω-cm, depending on silicon-to-nitrogen ratio, whereas dielectric strengths are between 1×10^6 and 6×10^6 V/cm.

8.3.3 Low-Dielectric-Constant Materials

As device sizes continue to shrink down to the deep submicron region, they require a multilevel interconnection architecture to minimize the time delay due to parasitic resistance (R) and capacitance (C). The gain in device speed at the gate level is offset by the propagation delay at the metal interconnects because of the increased RC time constant, as shown in Figure 8.14. For example, in devices with gate length of 250 nm or less, up to 50% of the time delay is due to the RC delay of long interconnections.¹³ Therefore, the device interconnection network becomes a limiting factor in determining chip performance metrics such as device speed, cross talk, and power consumption of ULSI circuits.

Reducing the RC time constant of ULSI circuits requires interconnection materials with low resistivity and interlayer films with low capacitance. Note that $C = \epsilon A/d$, where ϵ is the dielectric permittivity, A is the area, and d is the thickness of the dielectric film. Regarding the low-capacitance issue, it is not easy to lower the parasitic capacitance by increasing thickness of the interlayer dielectric (which makes gap filling more difficult) or decreasing wiring height and area (which results in the increase of interconnect resistance). Therefore, materials with low dielectric constant (low k) are required. The dielectric permittivity is equal to the product of k and ϵ_0 , where k and ϵ_0 are the dielectric constant and permittivity of free space, respectively.

The properties of the interlayer dielectric film and how it is formed have to meet the following requirements: low dielectric constant, low residual stress, high planarization

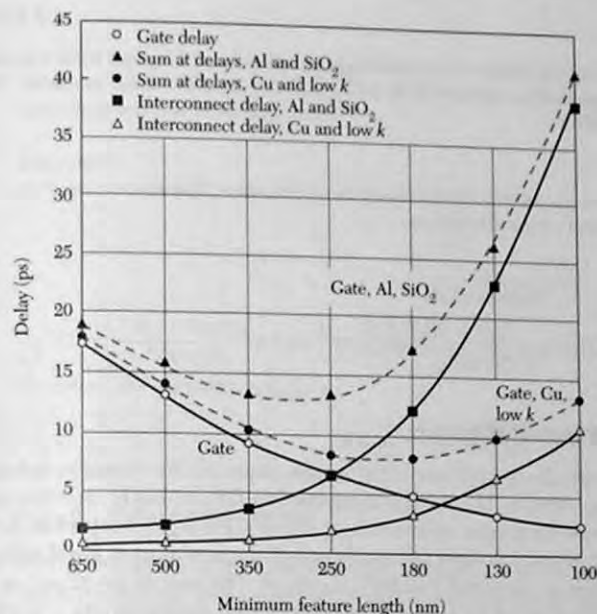


Figure 8.14 Calculated gate and interconnect delay versus technology generation. The dielectric constant for the low- k material is 2.0. Both Al and Cu interconnects are 0.8 μm thick and 43 μm long.

capability, high capability for gap filling, low deposition temperature, simplicity of process, and ease of integration. A substantial number of low- k materials have been synthesized for the intermetal dielectric in ULSI circuits. Some of the promising low- k materials are shown in Table 8.2. These materials can be either inorganic or organic and can be deposited by either CVD or spin-on techniques.¹³

TABLE 8.2 Low- k Materials

Determinant	Materials	Dielectric Constant
Vapor-phase deposition polymers	Fluorosilicate glass (FSG)	3.5–4.0
	Parylene N	2.6
	Parylene F	2.4–2.5
	Black diamond (C-doped oxide)	2.7–3.0
	Fluorinated hydrocarbon	2.0–2.4
	Teflon-AF	1.93
Spin-on polymers	HSQ/MSQ	2.8–3.0
	Polyimide	2.7–2.9
	SiLK (aromatic hydrocarbon polymer)	2.7
	PAE [poly(arylene ethers)]	2.6
	Fluorinated amorphous carbon	2.1
	Xerogels (porous silica)	1.1–2.0

EXAMPLE 3

Estimate the intrinsic RC value of two parallel Al wires $0.5 \mu\text{m} \times 0.5 \mu\text{m}$ in cross section, 1 mm in length, and separated by a polyimide ($k \sim 2.7$) dielectric layer that is $0.5 \mu\text{m}$ thick. The resistivity of Al is $2.7 \mu\Omega\text{-cm}$.

SOLUTION Let t_w be the cross-sectional dimension of the wires. Resistance is equal to ρl divided by the cross-sectional area of the wire, so

$$RC = \left(\rho \frac{l}{t_w^2} \right) \times \left(\epsilon \frac{A}{\text{Spacing width}} \right)$$

$$= \left(2.7 \times 10^{-6} \times \frac{10^{-1}}{0.25 \times 10^{-8}} \right) \times \left(8.85 \times 10^{-14} \times 2.7 \times \frac{0.5 \times 10^{-4} \times 10^{-1}}{0.5 \times 10^{-4}} \right) = 2.57 \text{ ps}$$

8.3.4 High-Dielectric-Constant Materials

High- k materials are also required for ULSI circuits, especially for dynamic random access memory (DRAM) circuits. The storage capacitor in a DRAM has to maintain a certain value of capacitance for proper operation (e.g., 40 fF). For a given capacitance, a minimum d is usually selected to meet the conditions of the maximum allowed leakage current and the minimum required breakdown voltage. The area of the capacitor can be increased by using stacked or trench structures. These structures are considered in Chapter 9. However, for a planar structure, area is reduced with increasing DRAM density. Therefore, the dielectric constant of the film must be increased.

Several high- k materials have been proposed, such as barium strontium titanate (BST) and lead zirconium titanate (PZT). These materials are shown in Table 8.3. In addition, there are titanates doped with one or more acceptors, such as alkaline earth metals, or doped with one or more donors, such as rare earth elements. Tantalum oxide (Ta_2O_5) has a dielectric constant in the range of 20 to 30. As a reference, the dielectric constant of Si_3N_4 is in the range of 6 to 7, and that for SiO_2 is 3.9. A Ta_2O_5 film can be deposited by a CVD process using gaseous TaCl_5 and O_3 as the starting materials.

TABLE 8.3 High- k Materials

	Materials	Dielectric Constant
Binary	Ta_2O_5	25
	TiO_2	40
	Y_2O_3	17
	Si_3N_4	7
Paraelectric perovskite	SrTiO_3 (STO)	140
	$(\text{Ba}_{1-x}\text{Sr}_x)\text{TiO}_3$ (BST)	300–500
	$\text{Ba}(\text{Ti}_{1-x}\text{Zr}_x)\text{O}_3$ (BZT)	300
	$(\text{Pb}_{1-x}\text{La}_x)(\text{Zr}_{1-y}\text{Ti}_y)\text{O}_3$ (PLZT)	800–1000
	$\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3$ (PMN)	1000–2000
Ferroelectric perovskite	$\text{Pb}(\text{Zr}_{0.47}\text{Ti}_{0.53})\text{O}_3$ (PZT)	>1000

EXAMPLE 4

A DRAM capacitor has the following parameters: $C = 40 \text{ fF}$, cell size (A) = $1.28 \mu\text{m}^2$, and $k = 3.9$ for silicon dioxide. If we replace SiO_2 with Ta_2O_5 ($k = 25$) without changing thickness, what is the equivalent cell area of the capacitor?

SOLUTION

$$C = \frac{\epsilon A}{d}$$

so

$$\frac{3.9 \times 1.28}{d} = \frac{25 \times A}{d}$$

Therefore, the equivalent cell size is

$$A = \frac{3.9}{25} \times 1.28 = 0.2 \mu\text{m}^2$$

► 8.4 POLYSILICON DEPOSITION

Using polysilicon as the gate electrode in MOS devices is a significant development in MOS technology. One important reason is that polysilicon surpasses aluminum for electrode reliability. Figure 8.15 shows the maximum time to breakdown for capacitors with both polysilicon and aluminum electrodes.¹⁴ Polysilicon is clearly superior, especially for

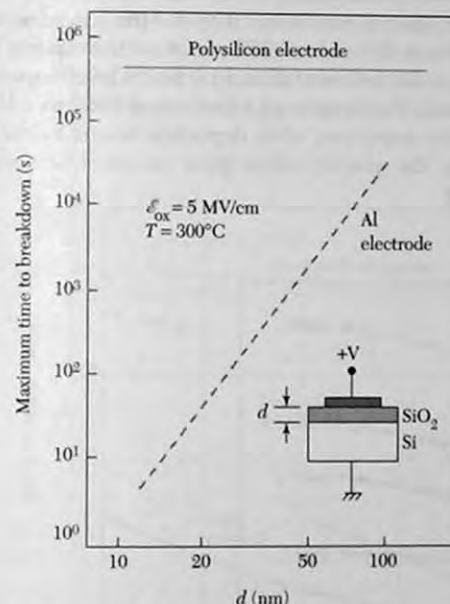


Figure 8.15 Maximum time to breakdown versus oxide thickness for a polysilicon electrode and an aluminum electrode.¹⁴

thinner gate oxides. The inferior time to breakdown of aluminum electrodes is due to the migration of aluminum atoms into the thin oxide under an electrical field. Polysilicon is also used as a diffusion source to create shallow junctions and to ensure ohmic contact to crystalline silicon. Additional uses include the manufacture of conductors and high-value resistors.

A low-pressure reactor (Fig. 8.9a) operated between 600°C and 650°C is used to deposit polysilicon by pyrolyzing silane according to the reaction



Of the two most common low-pressure processes, one operates at a pressure of 25 to 130 Pa using 100% silane, whereas the other involves a diluted mixture of 20% to 30% silane in nitrogen at the same total pressure. Both processes can deposit polysilicon on hundreds of wafers per run with good uniformity (i.e., thicknesses within $\pm 5\%$).

Figure 8.16 shows the deposition rate at four deposition temperatures. At low silane partial pressure, the deposition rate is proportional to the silane pressure.⁸ At higher silane concentrations, saturation of the deposition rate occurs. Deposition at reduced pressure is generally limited to temperatures between 600°C and 650°C. In this temperature range, the deposition rate varies as $\exp(-E_a/kT)$, where E_a is 1.7 eV, which is essentially independent of the total pressure in the reactor. At higher temperatures, gas-phase reactions that result in a rough, loosely adhering deposit become significant, and silane depletion occurs, causing poor uniformity. At temperatures much lower than 600°C, the deposition rate is too slow to be practical.

Process parameters that affect the polysilicon structure are deposition temperature, dopants, and the heat cycle applied following the deposition step. A columnar structure results when polysilicon is deposited at a temperature of 600°C to 650°C. This structure consists of polycrystalline grains ranging in size from 0.03 to 0.3 μm at a preferred orientation of (110). When phosphorus is diffused at 950°C, the structure changes to crystallite, and grain size increases to a size between 0.5 and 1.0 μm . When temperature is increased to 1050°C during oxidation, the grains reach a final size of 1 to 3 μm . Although the initially deposited film appears amorphous when deposition occurs below 600°C, growth characteristics similar to the polycrystalline-grain columnar structure are observed after doping and heating.

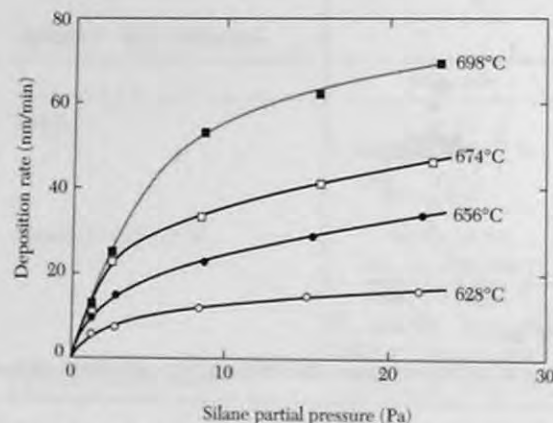


Figure 8.16 Effect of silane concentration on the polysilicon deposition rate.⁸

Polysilicon can be doped by diffusion, ion implantation, or the addition of dopant gases during deposition, referred to as *in situ doping*. The implantation method is most commonly used because of its lower processing temperatures. Figure 8.17 shows the sheet resistance of single-crystal silicon and of 500-nm polysilicon doped with phosphorus and antimony using ion implantation.¹⁵ The ion implantation process was considered in Chapter 7. Implant dose, annealing temperature, and annealing time all influence the sheet resistance of implanted polysilicon. Carrier traps at the grain boundaries cause a very high resistance in the lightly implanted polysilicon. As Figure 8.17 illustrates, resistance drops rapidly, approaching that of implanted single-crystal silicon, as the carrier traps become saturated with dopants.

► 8.5 METALLIZATION

8.5.1 Physical Vapor Deposition

The most common methods of physical vapor deposition (PVD) of metals are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. Metals and metal compounds such as Ti, Al, Cu, TiN, and TaN can be deposited by PVD. Evaporation occurs when a source material is heated above its melting point in an evacuated chamber. The evaporated atoms then travel at high velocity in straight-line trajectories. The source can be melted by resistance heating, by rf heating, or with a focused electron beam. Evaporation and e-beam evaporation were used extensively in earlier generations of integrated circuits, but they have been replaced by sputtering for ULSI circuits.

In ion beam sputtering, a source of ions is accelerated toward the target and impinges on its surface. Figure 8.18a shows a standard sputtering system. The sputtered material deposits on a wafer that is placed facing the target. The ion current and energy can be independently adjusted. Since the target and wafer are placed in a chamber that has lower pressure, more target material and less contamination are transferred to the wafer.

One method to increase the ion density and, hence, the sputter-deposition rate is to use a third electrode that provides more electrons for ionization. Another method is to use

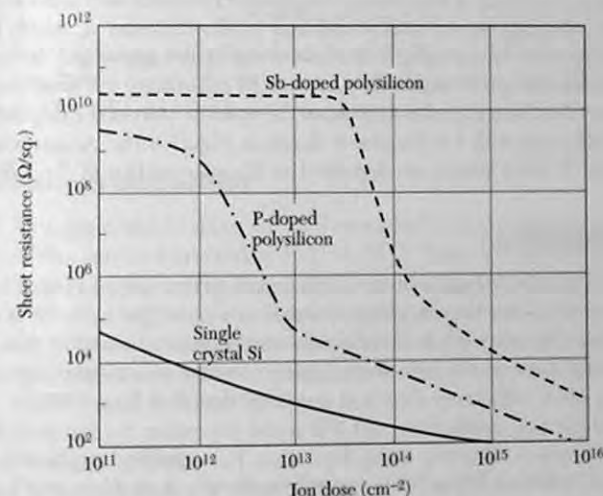


Figure 8.17 Sheet resistance versus ion dose into 500-nm polysilicon at 30 keV.¹⁵

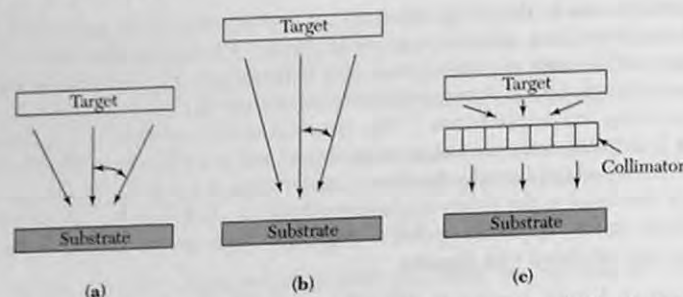


Figure 8.18 (a) Standard sputtering. (b) Long-throw sputtering. (c) Sputtering with a collimator.

a magnetic field, such as *electron cyclotron resonance* (ECR), to capture and spiral electrons, increasing their ionizing efficiency in the vicinity of the sputtering target. This technique, referred to as *magnetron sputtering*, has found widespread applications for the deposition of aluminum and its alloys at a rate that can approach 1 $\mu\text{m}/\text{min}$.

Long-throw sputtering is another technique used to control the angular distribution. Figure 8.18b shows a long-throw sputtering system. In standard sputtering configurations, there are two primary reasons for a wide angular distribution of incident flux at the surface: the use of a small target-to-substrate separation, d_{ts} ; and scattering of the flux by the working gas as the flux travels from the target to the substrate. These two factors are linked because a small d_{ts} is needed to achieve good throughput, uniformity, and film properties when there is substantial gas scattering. A solution to this problem is to sputter at very low pressures, a capability that has been developed using a variety of systems that can sustain the magnetron plasma under more rarefied conditions. These systems allow for sputtering at working pressures of less than 0.1 Pa. At these pressures, gas scattering is less important, and the target-to-substrate distance can be greatly increased. From a simple geometrical argument, this allows the angular distribution to be greatly narrowed, which permits more deposition at the bottom of high-aspect features such as contact holes.

Contact holes with large aspect ratio are difficult to fill with material, mainly because scattering events cause the top opening of the hole to seal before appreciable material has deposited on its floor. This problem can be overcome by collimating the sputtered atoms by placing an array of collimating tubes just above the wafer to restrict the depositing flux to normal $\pm 5^\circ$. Sputtering with a collimator is shown in Figure 8.18c. Atoms whose trajectory is more than 5° from normal are deposited on the inner surface of the collimators.

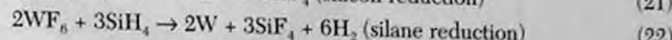
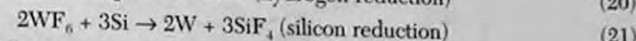
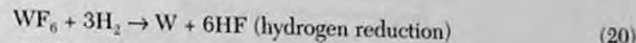
8.5.2 Chemical Vapor Deposition

CVD is attractive for metallization because it offers coatings that are conformal, has good step coverage, and can coat a large number of wafers at a time. The basic CVD setup is the same as that used for deposition of dielectrics and polysilicon (see Fig. 8.9a). Low-pressure CVD is capable of producing conformal step coverage over a wide range of topographical profiles, often with lower electrical resistivity than that from PVD.

One of the major new applications of CVD metal deposition for integrated circuit production is in the area of refractory metal deposition. For example, tungsten's low electrical resistivity (5.3 $\mu\Omega\text{-cm}$) and refractory nature make it a desirable metal for use in integrated circuit fabrication.

CVD Tungsten

Tungsten is used both as a contact plug and as a first-level metal. Tungsten can be deposited by using WF_6 as the source gas, since it is a liquid that boils at room temperature. WF_6 can be reduced by silicon, hydrogen, or silane. The basic chemistry for CVD W is as follows:

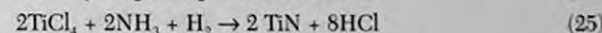
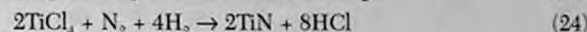
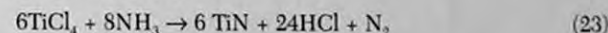


On a Si contact, the selective process starts from a silicon reduction process. This process provides a nucleation layer of W grown on Si but not on SiO_2 . The hydrogen reduction process can deposit W rapidly on the nucleation layer, forming the plug. The hydrogen reduction process provides excellent conformal coverage of the topography. This process, however, does not have perfect selectivity, and the HF gas by-product of the reaction is responsible for the encroachment of the oxide, as well as for the rough surface of deposited W films.

The silane reduction process gives a high deposition rate and much smaller W grain size than that obtained with the hydrogen reduction process. In addition, the problems of encroachment and a rough W surface are eliminated because there is no HF by-product generation. Usually, a silane reduction process is used as the first step in blanket W deposition to serve as a nucleation layer and to reduce junction damage. After the silane reduction, hydrogen reduction is used to grow the blanket W layer.

CVD TiN

TiN is widely used as a diffusion barrier metal layer in metallization and can be deposited by sputtering from a compound target or by CVD. CVD TiN can provide better step coverage than PVD methods in deep submicron technology. CVD TiN can be deposited¹⁶⁻¹⁸ using TiCl_4 with NH_3 , H_2/N_2 , or NH_3/H_2 :



The deposition temperature is about 400°C to 700°C for NH_3 reduction and is higher than 700°C for the N_2/H_2 reaction. The higher the deposition temperature, the better the TiN film, and the less Cl incorporated in TiN (~5%).

8.5.3 Aluminum Metallization

Aluminum and its alloys are used extensively for metallization in integrated circuits. The Al film can be deposited by PVD or CVD. Since aluminum and its alloys have low resistivities (2.7 $\mu\Omega\text{-cm}$ for Al and up to 3.5 $\mu\Omega\text{-cm}$ for its alloys), these metals satisfy the low-resistance requirements. Aluminum also adheres well to silicon dioxide. However, the use of aluminum in integrated circuits with shallow junctions often creates problems, such as spiking and electromigration. This section considers the problems of aluminum metallization and their solutions.

Junction Spiking

Figure 8.19 shows the phase diagram of the Al-Si system at 1 atm.¹⁹ The phase diagram relates these two components as a function of temperature. The Al-Si system exhibits

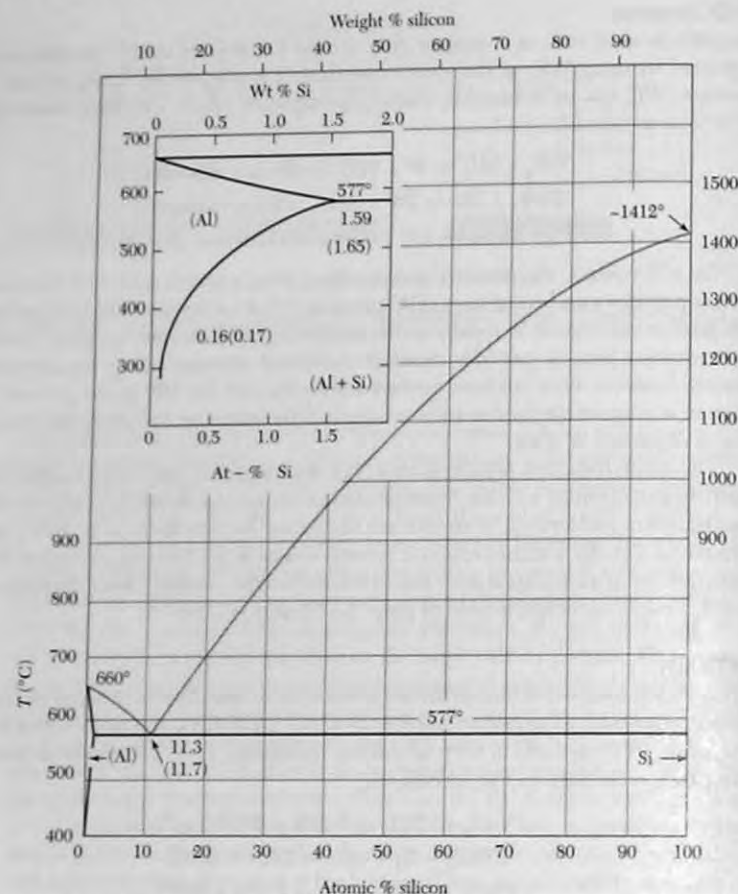


Figure 8.19 Phase diagram of the aluminum-silicon system.¹⁹

eutectic characteristics; that is, the addition of either component lowers the system's melting point below that of either metal. Here, the minimum melting temperature, called *eutectic temperature*, is 577°C, corresponding to a 11.3% Si and 88.7% Al composition. The melting points of pure aluminum and pure silicon are 660°C and 1412°C, respectively. Because of the eutectic characteristics, during aluminum deposition the temperature on the silicon substrate must be limited to less than 577°C.

The inset of Figure 8.19 shows the solid solubility of silicon in aluminum. For example, the solubility of silicon in aluminum is 0.25 wt% at 400°C, 0.5 wt% at 450°C, and 0.8 wt% at 500°C. Therefore, wherever aluminum contacts silicon, the silicon will dissolve into the aluminum during annealing. The amount of silicon dissolved will depend not only on the solubility at the annealing temperature, but also on the volume of aluminum to be saturated with silicon. Consider a long aluminum metal line in contact with an area ZL of silicon, as shown in Figure 8.20. After an annealing time t , the silicon will diffuse a distance of approximately $\sqrt{Dt}$ along the aluminum line from the edge of the contact, where D is the diffusion coefficient given by $4 \times 10^{-2} \exp(-0.92/kT)$ for silicon

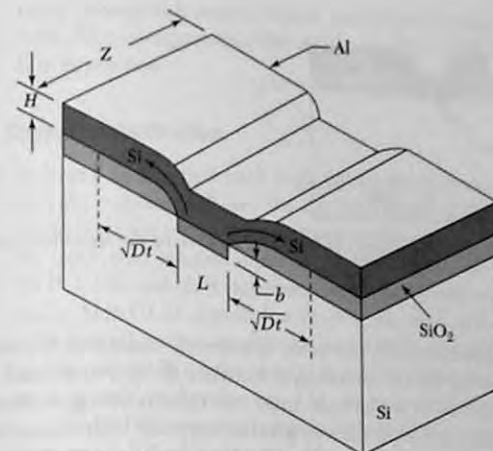


Figure 8.20 Diffusion of silicon in aluminum metallization.²⁰

diffusion in deposited aluminum films. Assuming that this length of aluminum is completely saturated with silicon, the volume of silicon consumed is then

$$\text{Vol} \cong 2\sqrt{Dt}(HZ)S\left(\frac{\rho_{\text{Al}}}{\rho_{\text{Si}}}\right) \quad (26)$$

where ρ_{Al} and ρ_{Si} are the densities of aluminum and silicon, respectively, and S is the solubility of silicon in aluminum at the annealing temperature.²⁰ If the consumption takes place uniformly over the contact area A (where $A = ZL$ for uniform dissolution), the depth to which silicon would be consumed is

$$b \cong 2\sqrt{Dt}\left(\frac{HZ}{A}\right)S\left(\frac{\rho_{\text{Al}}}{\rho_{\text{Si}}}\right) \quad (27)$$

EXAMPLE 5

Let $T = 500^\circ\text{C}$, $t = 30$ min, $ZL = 16 \mu\text{m}^2$, $Z = 5 \mu\text{m}$, and $H = 1 \mu\text{m}$. Find the depth b , assuming uniform dissolution.

SOLUTION The diffusion coefficient of silicon in aluminum at 500°C is about $2 \times 10^{-8} \text{ cm}^2/\text{s}$; thus, $\sqrt{Dt}$ is 60 μm . The density ratio is $2.7/2.33 = 1.16$. At 500°C, S is 0.8 wt%. From Eq. 27, we have

$$b = 2 \times 60 \left(\frac{1 \times 5}{16}\right) 0.8\% \times 1.16 = 0.35 \mu\text{m}$$

Aluminum will fill a depth of $b = 0.35 \mu\text{m}$ from which silicon is consumed. If at the contact point there is a shallow junction whose depth is less than b , the diffusion of silicon into aluminum can short-circuit the junction. ◀

In a practical situation, the dissolution of silicon does not take place uniformly, but rather at only a few points. The effective area in Eq. 27 is less than the actual contact area; hence, b is much larger. Figure 8.21 illustrates the actual situation in the p - n junction area of aluminum penetrating the silicon at only the few points where spikes are formed. One way to minimize aluminum spiking is to add silicon to the aluminum by co-evaporation

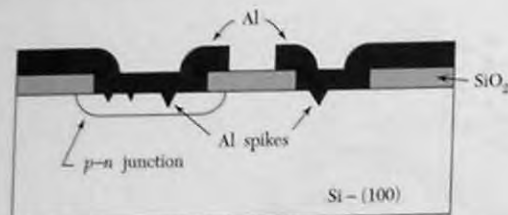


Figure 8.21 Schematic view of aluminum films contacting silicon. Note the aluminum spiking in the silicon.

until the amount of silicon contained by the alloy satisfies the solubility requirement. Another method is to introduce a barrier metal layer between the aluminum and the silicon substrate (Fig. 8.22). This barrier metal layer must meet the following requirements: It must form low contact resistance with silicon, it must not react with aluminum, and its deposition and formation must be compatible with the overall process. Barrier metals such as titanium nitride (TiN) have been evaluated and found to be stable for contact annealing temperatures of up to 550°C for 30 minutes.

Electromigration

As devices become smaller, the corresponding current density becomes larger. High current densities can cause device failure due to electromigration. The term *electromigration* refers to the transport of mass (i.e., atoms) in metals under the influence of current. It occurs by the transfer of momentum from the electrons to the positive metal ions. When a high current passes through thin metal conductors in integrated circuits, metal ions in some regions will pile up, and voids will form in other regions. This pileup can short-circuit adjacent conductors, whereas the voids can result in an open circuit.

The mean time to failure (MTF) of a conductor due to electromigration can be related to the current density (J) and the activation energy by

$$\text{MTF} \sim \frac{1}{J^2} \exp\left(\frac{E_a}{kT}\right) \quad (28)$$

Experimentally, a value of $E_a \approx 0.5$ eV is obtained for deposited aluminum. This indicates that low-temperature grain-boundary diffusion is the primary vehicle of material transport, since an $E_a \approx 1.4$ eV would characterize the self-diffusion of single-crystal aluminum. The electromigration resistance of aluminum conductors can be increased by

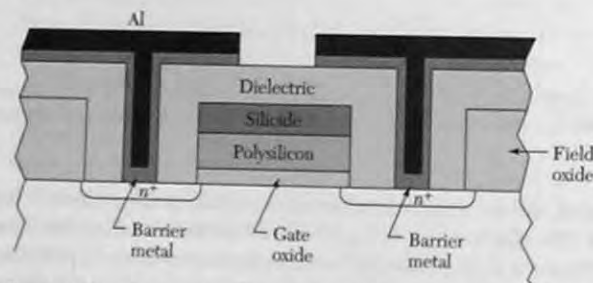


Figure 8.22 Cross-sectional view of a MOSFET with a barrier metal between the aluminum and silicon and a composite gate electrode of silicide and polysilicon.

using several techniques. These techniques include alloying with copper (e.g., Al with 0.5% Cu), encapsulating the conductor in a dielectric, or incorporating oxygen during film deposition.

8.5.4 Copper Metallization

It is well known that both high-conductivity wiring and low-dielectric-constant insulators are required to lower the RC time delay of the interconnect network. Copper is the obvious choice for a new interconnection metallization because it has higher conductivity and higher electromigration resistance than aluminum. Copper can be deposited by PVD, CVD, and electrochemical methods. However, the use of Cu as an alternative material to Al in ULSI circuits has drawbacks, such as its tendency to corrode under standard chip manufacturing conditions, its lack of a feasible dry etching method or a stable self-passivating oxide similar to Al_2O_3 on Al, and its poor adhesion to dielectric materials, such as SiO_2 and low- k polymers. This section discusses copper metallization techniques.

Several different techniques for fabrication of multilevel Cu interconnects have been reported.^{21, 22} The first method is a conventional method to pattern the metal lines, followed by dielectric deposition. The second method is to pattern the dielectric layer first and fill copper metal into trenches. This step is followed by *chemical mechanical polishing*, discussed later, to remove the excess metal on the top surface of the dielectric and leave Cu material in the holes and trenches. This method is also known as a *damascene* process.

Damascene Technology

The approach for fabricating a copper/low- k dielectric interconnect structure is by the damascene or dual damascene process. Figure 8.23 shows the dual damascene sequence for an advanced Cu interconnection structure. For a typical damascene structure, trenches for metal lines are defined and etched in the interlayer dielectric (ILD), followed by metal deposition of TaN/Cu. The TaN layer serves as a diffusion barrier layer and prevents copper from penetrating the low- k dielectric. The excess copper metal on the surface is removed to obtain a planar structure with metal inlays in the dielectric.

For the dual damascene process, the vias and trenches in the dielectric are defined using two lithography and reactive ion etching (RIE) steps before depositing the Cu metal (Figs. 8.23a-c). Then a Cu chemical mechanical polishing process is used to remove the metal on the top surface, leaving the planarized wiring and via imbedded in the insulator.²³ One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced.

EXAMPLE 6

If we replace Al with Cu wire associated with some low- k dielectric ($k = 2.6$) instead of a SiO_2 layer, what percentage of reduction in the RC time constant will be achieved? The resistivity of Al is $2.7 \mu\Omega\text{-cm}$, and the resistivity of Cu is $1.7 \mu\Omega\text{-cm}$.

SOLUTION

$$\frac{1.7}{2.7} \times \frac{2.6}{3.9} \times 100\% = 42\%$$

Chemical Mechanical Polishing

In recent years, the development of chemical mechanical polishing (CMP) has become increasingly important for multilevel interconnection because it is the only technology

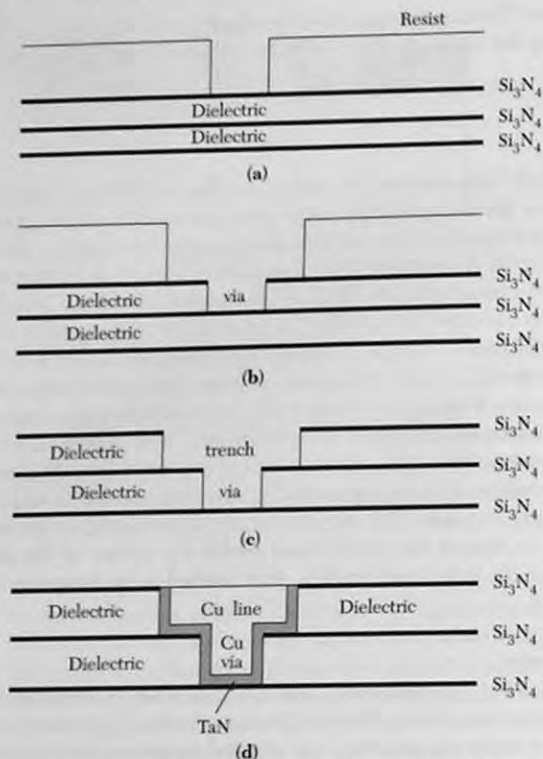


Figure 8.23 Process sequence used to fabricate a Cu line-stud structure using dual damascene. (a) Resist stencil applied. (b) Reactive ion etching dielectric and resist patterning. (c) Trench and via definition. (d) Cu depositions followed by chemical mechanical polishing.

that allows global planarization (i.e., makes a flat surface across the whole wafer). It offers many advantages over other types of technologies, including better global planarization over large or small structures, reduced defect density, and the avoidance of plasma damage. Three CMP approaches are summarized in Table 8.4.

The CMP process consists of moving the sample surface against a pad that carries slurry between the sample surface and the pad. Abrasive particles in the slurry cause mechanical damage on the sample surface, loosening the material for enhanced chemical attack or fracturing off the pieces of surface into a slurry where they dissolve or are swept away. The process is tailored to provide an enhanced material removal rate from high points on surfaces, thus affecting the planarization because most chemical actions are isotropic. Mechanical grinding alone may theoretically achieve the desired planarization,

TABLE 8.4 Three Methods of Chemical Mechanical Polishing (CMP)

Method	Wafer Facing	Platen Movement	Slurry Feeding
Rotary CMP	Down	Rotary against rotating wafer carrier	Dripping to pad surface
Orbital CMP	Down	Orbital against rotating wafer carrier	Through the pad surface
Linear CMP	Down	Linear against rotating wafer carrier	Dripping to pad surface

but is not desirable because of extensive associated damage to the material surfaces. There are three main parts of the process: (a) the surface to be polished; (b) the pad, which is the key medium enabling the transfer of mechanical action to the surface being polished; and (c) the slurry, which provides both chemical and mechanical effects. Figure 8.24 shows the CMP setup.²⁴

EXAMPLE 7

The oxide removal rate and the removal rate of a layer underneath the oxide (called a stop layer) are $1r$ and $0.1r$, respectively. To remove $1\text{ }\mu\text{m}$ of oxide and a $0.01\text{ }\mu\text{m}$ stop layer, the total removal time is 5.5 minutes. Find the oxide removal rate.

SOLUTION

$$\frac{1}{1r} + \frac{0.01}{0.1r} = 5.5$$

$$r = 0.2\text{ }\mu\text{m/min}$$

8.5.5 Silicide

Silicon forms many stable metallic and semiconducting compounds with metals. Several metal silicides show low resistivity and high thermal stability, making them suitable for ULSI application. Silicides such as TiSi_2 and CoSi_2 have reasonably low resistivities and are generally compatible with integrated circuit processing. Silicides become important metallization materials as devices become smaller. One important application of silicide is for the MOSFET gate electrode, either alone or with doped polysilicon (polycide) above the gate oxide. Table 8.5 shows a comparison of titanium silicide and cobalt silicide.

Metal silicides have been used to reduce the contact resistance of the source and drain, the gate electrodes, and interconnections. Self-aligned metal silicide technology

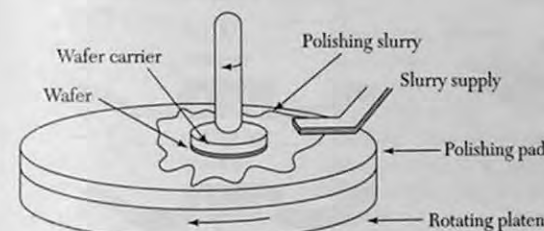


Figure 8.24 Schematic of a CMP polisher.

TABLE 8.5 A Comparison of TiSi_2 and CoSi_2 Films

Properties	TiSi_2	CoSi_2
Resistivity	13–16	22–28
Silicide/metal ratio	2.37	3.56
Silicide/Si ratio	1.04	0.97
Reactive to native oxide	Yes	No
Silicidation temperature ($^{\circ}\text{C}$)	800–850	550–900
Film stress (dyne/cm ²)	1.5×10^{10}	1.2×10^{10}

(salicide) has been proven to be a highly attractive technique for improving the performance of submicron devices and circuits. The self-aligned process uses the silicide gate electrode as the mask to form the source and drain electrodes of a MOSFET (e.g., by ion implantation, considered in Chapter 7). This process can minimize the overlap of these electrodes and thus reduce parasitic capacitances.

Figure 8.25 shows the polycide and salicide processes. A typical polycide formation sequence is shown in Figure 8.25a. For sputter deposition, a high-temperature, high-purity compound target is used to ensure the quality of the silicide. The most commonly used silicides for the polycide process are WSi_2 , TaSi_2 , and MoSi_2 . They are all refractory, thermally stable, and resistant to processing chemicals. A self-aligned silicide process is illustrated in Figure 8.25b. In the process, the polysilicon gate is patterned without any silicide, and a sidewall spacer (silicon oxide or silicon nitride) is formed to prevent shorting the gate to the source and drain during the silicidation process. A metal layer, either Ti or Co, is blanket-sputtered on the entire structure, followed by silicide sintering. Silicide is formed, in principle, only where the metal is in contact with Si. A wet chemical wash then rinses off the unreacted metal, leaving only the silicide. This technique eliminates the need to pattern the composite polycide gate structure and adds silicide to the source/drain area to reduce the contact resistance.

Silicides are promising materials for ULSI circuits because of their low resistivity and excellent thermal stability. Cobalt silicide has been widely investigated because of its low resistivity and high-temperature thermal stability. However, cobalt is sensitive to native oxides as well as an oxygen-containing environment, and a large amount of silicon is consumed during silicidation.

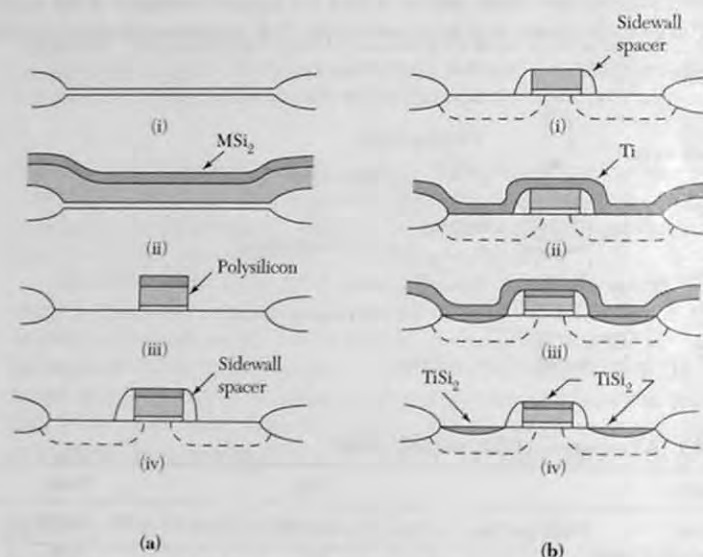


Figure 8.25 Polycide and salicide processes. (a) Polycide structure: (i) gate oxide, (ii) polysilicon and silicide deposition, (iii) pattern polycide, and (iv) lightly doped drain (LDD) implant, sidewall formation, and source/drain implant. (b) Salicide structure: (i) gate patterning (polysilicon only), LDD, sidewall, and source/drain implant; (ii) metal (Ti, Co) deposition; (iii) anneal to form silicide; and (iv) selective (wet) etch to remove unreacted metal.

EXAMPLE 8

Calculate the thickness of cobalt silicide for a desired sheet resistance of $0.6 \Omega/\square$. The resistivity is $18 \mu\Omega\text{-cm}$.

SOLUTION The resistivity is equal to the product of the sheet resistance and the film thickness:

$$\rho = R_s \times t$$

Then

$$t = \frac{\rho}{R_s} = \frac{18 \times 10^{-6}}{0.6} = 3 \times 10^{-5} \text{ cm} = 300 \text{ nm}$$

8.6 DEPOSITION SIMULATION

SUPREM may be used to simulate the deposition process. Like etch simulation, deposition modeling is very straightforward. Simulation is executed using the **DEPOSITION** command, which deposits a given amount of user-specified material on top of the current structure. The material deposited may be either undoped or uniformly doped. If single-crystal silicon is deposited, then the crystal orientation must also be specified. If polysilicon is deposited, the temperature must be specified for SUPREM to determine the proper polysilicon grain size.

EXAMPLE 9

Suppose we want to simulate the deposition of 800Å CVD silicon nitride on top of a dry oxide layer approximately 400Å thick. If the *p*-type silicon substrate is doped with boron at a level of 10^{15} cm^{-3} , use SUPREM to determine the final oxide and nitride layer thicknesses, as well as the boron doping profile in the oxide and nitride layers.

SOLUTION The SUPREM input listing is as follows:

TITLE	Deposition Example
COMMENT	Initialize silicon substrate
INITIALIZE	<100> Silicon Boron Concentration=1e15
COMMENT	Grow 400Å oxide
DIFFUSION	Time=40 Temperature=1000 DryO2
COMMENT	Deposit 800Å CVD nitride
DEPOSITION	Nitride Thickness=0.08
PRINT	Layers
PLOT	Chemical Boron Net
STOP	End Deposition Example

After simulation is complete, the results are shown in Figure 8.26, which indicates final oxide and nitride layer thicknesses of 379 and 800Å, respectively, and depicts the boron incorporation in the oxide layer.

8.7 SUMMARY

Modern semiconductor device fabrication requires the use of thin films. In the epitaxial growth process, the substrate wafer is the seed. High-quality, single-crystal films can be grown at a temperature 30% to 50% lower than the melting point. The common techniques for epitaxial growth are chemical vapor deposition, metalorganic CVD, and molecular beam

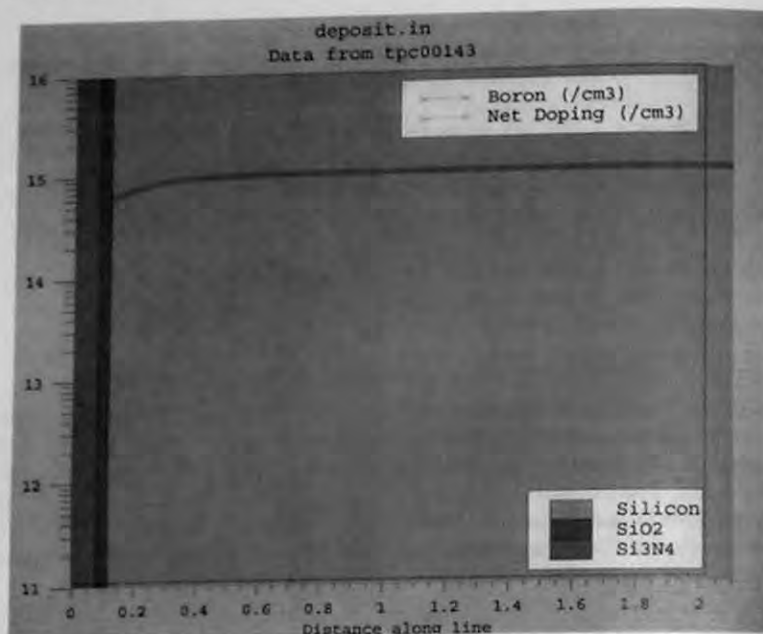


Figure 8.26 Plot of boron incorporation into the oxide layer, using SUPREM.

epitaxy. CVD and MOCVD are chemical deposition processes. Gases and dopants are transported in vapor form to the substrate, where a chemical reaction occurs that results in the deposition of the epitaxial layer. Inorganic compounds are used for CVD, whereas metalorganic compounds are used for MOCVD. MBE, on the other hand, is a physical deposition process. It is done by the evaporation of a species in an ultrahigh-vacuum system. Because it is a low-temperature process that has a low growth rate, MBE can grow single-crystal, multilayer structures with dimensions on the order of atomic layers.

In addition to conventional homoepitaxy, such as *n*-type silicon on an *n*⁺ silicon substrate, this chapter also considered heteroepitaxy, which includes lattice-matched and strained-layer structures. For strained-layer epitaxy, there is a critical layer thickness above which edge dislocations will nucleate to relieve the strain energy.

Besides the edge dislocations in an epitaxial layer, defects from the substrate, defects from the interface, precipitates, and low-angle grain boundaries and twins exist. These defects degrade device performance. Various means have been presented to minimize, or even eliminate, these defects so that a defect-free semiconductor layer can be grown either homoepitaxially or heteroepitaxially.

Aside from epitaxial layers, there are four other important types of films: thermal oxides, dielectric layers, polycrystalline silicon, and metal films. The major issues related to film formation are low-temperature processing, step coverage, selective deposition, uniformity, film quality, planarization, throughput, and large wafer capacity.

Thermal oxidation offers the best quality for the Si-SiO₂ interface and has the lowest interface trap density (see Chapter 3). Therefore, it is used to form gate and field oxides. LPCVD of dielectrics and polysilicon offers conformal step coverage. In contrast, PVD and atmospheric-pressure CVD generally result in nonconformal step coverage. CMP offers global planarization and reduces defect density. Conformal step coverage and planarization are also required for precise pattern transfer at the deep-submicron lithography level.

To minimize the RC time delay due to parasitic resistance and capacitance, the silicide process for ohmic contacts, copper metallization for interconnects, and low-dielectric-constant materials for interlayer films are extensively used to meet the requirements of the multilevel interconnect structures of ULSI circuits. In addition, this chapter discussed high-dielectric-constant materials to improve the gate insulator performance and to increase the capacitance per unit area for DRAM.

REFERENCES

1. A. S. Grove, *Physics and Technology of Semiconductor Devices*, Wiley, New York, 1967.
2. R. Reif, T. I. Kamins, and K. C. Saraswat, "A Model for Dopant Incorporation into Growing Silicon Epitaxial Films," *J. Electrochem. Soc.*, **126**, 644, 653 (1979).
3. R. D. Dupuis, "Metalorganic Chemical Vapor Deposition of III-V Semiconductors," *Science*, **226**, 623 (1984).
4. M. A. Herman and H. Sitter, *Molecular Beam Epitaxy*, Springer-Verlag, Berlin, 1996.
5. A. Roth, *Vacuum Technology*, North-Holland, Amsterdam, 1976.
6. M. Ohring, *The Materials Science of Thin Films*, Academic Press, New York, 1992.
7. J. C. Bean, "The Growth of Novel Silicon Materials," *Physics Today*, **39**, 10, 36 (1986).
8. For a discussion on film deposition, see, for example, A. C. Adams, "Dielectric and Polysilicon Film Deposition," in S. M. Sze, Ed., *VLSI Technology*, McGraw-Hill, New York, 1983.
9. K. Eujino, et al., "Doped Silicon Oxide Deposition by Atmospheric Pressure and Low Temperature Chemical Vapor Deposition Using Tetraethoxysilane and Ozone," *J. Electrochem. Soc.*, **138**, 3019 (1991).
10. A. C. Adams and C. D. Capio, "Planarization of Phosphorus-Doped Silicon Dioxide," *J. Electrochem. Soc.*, **127**, 2222 (1980).
11. T. Yamamoto, et al., "An Advanced 2.5nm Oxidized Nitride Gate Dielectric for Highly Reliable 0.25 μ m MOSFETs," *Symp. VLSI Technol. Dig. Tech. Pap.*, p. 45 (1997).
12. K. Kumar, et al., "Optimization of Some 3 nm Gate Dielectrics Grown by Rapid Thermal Oxidation in a Nitric Oxide Ambient," *Appl. Phys. Lett.*, **70**, 384 (1997).
13. T. Homma, "Low Dielectric Constant Materials and Methods for Interlayer Dielectric Films in Ultralarge-Scale Integrated Circuit Multilevel Interconnects," *Mater. Sci. Eng.*, **23**, 243 (1995).
14. H. N. Yu, et al., "1 μ m MOSFET VLSI Technology: Part I—An Overview," *IEEE Trans. Electron Devices*, **ED-26**, 318 (1979).
15. J. M. Andrews, "Electrical Conduction in Implanted Polycrystalline Silicon," *J. Electron. Mater.*, **8**, 3, 227 (1979).
16. M. J. Buiting, A. F. Otterloo, and A. H. Montree, "Kinetic Aspects of the LPCVD of Titanium Nitride from Titanium Tetrachloride and Ammonia," *J. Electrochem. Soc.*, **138**, 500 (1991).
17. R. Tobe, et al., "Plasma-Enhanced CVD of TiN and Ti Using Low-Pressure and High-Density Helicon Plasma," *Thin Solid Film*, **281-282**, 155 (1996).
18. J. Hu, et al., "Electrical Properties of Ti/TiN Films Prepared by Chemical Vapor Deposition and Their Applications in Submicron Structures as Contact and Barrier Materials," *Thin Solid Film*, **308**, 589 (1997).
19. M. Hansen and A. Anderko, *Constitution of Binary Alloys*, McGraw-Hill, New York, 1958.
20. D. Pramanik and A. N. Saxena, "VLSI Metallization Using Aluminum and Its Alloys," *Solid State Tech.*, **26**(1), 127 (1983); **26**(3), 131 (1983).
21. C. L. Hu and J. M. E. Harper, "Copper Interconnections and Reliability," *Mater. Chem. Phys.*, **52**, 5 (1998).
22. P. C. Andricacos, et al., "Damascene Copper Electroplating for Chip Interconnects," *193rd Meet. Electrochem. Soc.*, p. 3 (1998).
23. J. M. Steigerwald, et al., *Chemical Mechanical Planarization of Microelectronic Materials*, Wiley, New York, 1997.
24. L. M. Cook, et al., "Theoretical and Practical Aspects of Dielectric and Metal CMP," *Semicond. Int.*, p. 141 (1995).

PROBLEMS

Asterisks denote difficult problems.

SECTION 8.1: EPITAXIAL GROWTH TECHNIQUES

- *1. Find the average molecular velocity of air at 300 K (the molecular weight for air is 29).
2. The distance between source and wafer in a deposition chamber is 15 cm. Estimate the pressure at which this distance become 10% of the mean free path of source molecules.
- *3. Find the number of atoms per unit area, N_s , needed to form a monolayer under close-packing condition (i.e., each atom is in contact with its six neighboring atoms), assuming the diameter d of the atom is 4.68 Å.
- *4. Assume an effusion oven geometry of $A = 5 \text{ cm}^2$ and $L = 12 \text{ cm}$. (a) Calculate the arrival rate of gallium and the MBE growth rate for the effusion oven filled with gallium arsenide at 970°C. (b) For a tin effusion oven operated at 700°C under the same geometry, calculate the doping concentration (assuming tin atoms are fully incorporated in the gallium arsenide grown at the aforementioned rate). The molecular weight for tin is 118.69, and the pressure at 700°C for tin is $2.66 \times 10^{-6} \text{ Pa}$.

SECTION 8.2: STRUCTURES AND DEFECTS IN EPITAXIAL LAYERS

5. Find the maximum percentage of In (i.e., the x value for $\text{Ga}_{1-x}\text{In}_x\text{As}$) film grown on GaAs substrate without formation of misfit dislocation, if the final film thickness is 10 nm.
6. The lattice misfit, f , of a film is defined as $f = [a_0(s) - a_0(f)]/a_0(f) = \Delta a_0/a_0$ where $a_0(s)$ and $a_0(f)$ are the unstrained lattice constants of the substrate and the film, respectively. Find the f values for InAs–GaAs and Ge–Si systems.

SECTION 8.3: DIELECTRIC DEPOSITION

7. (a) In a plasma-deposited silicon nitride that contains 20 at% hydrogen and has a silicon-to-nitrogen ratio (Si/N) of 1.2, find x and y in the empirical formula of $\text{Si}_x\text{H}_y\text{N}_y$. (b) If the variation of film resistivity with Si/N ratio is given by $5 \times 10^{25} \exp(-33.3\gamma)$ for $2 > \gamma > 0.8$, where γ is the ratio, find the resistivity of the film in (a).
8. The dielectric constants of SiO_2 , Si_3N_4 , and Ta_2O_5 are about 3.9, 7.6, and 25, respectively. What is the capacitance ratio for the capacitors with the Ta_2O_5 and oxide/nitride/oxide dielectrics for the same dielectric thickness, provided the oxide/nitride/oxide has thickness ratio 1:1:1 for the oxide to the nitride?
9. In Problem 8, if BST with a dielectric constant of 500 is chosen to replace Ta_2O_5 , calculate the area reduction ratio to maintain the same capacitance if the two films have the same thickness.
10. In Problem 8, calculate the equivalent thickness of the Ta_2O_5 in terms of SiO_2 thickness if both have the same capacitance. Assume the actual thickness of Ta_2O_5 is 3 μm .
11. In a silane-oxygen reaction to deposit undoped SiO_2 film, the deposition rate is 15 nm/min at 425°C. What temperature is required to double the deposition rate?
12. The P-glass flow process requires temperatures above 1000°C. As device dimensions become smaller in ULSI, we must use lower temperatures. Suggest methods to obtain a smooth topography at < 900°C for deposited silicon dioxide that can be used as an insulator between metal layers.

SECTION 8.4: POLYSILICON DEPOSITION

13. Why is silane more often used for polysilicon deposition than silicon chloride?
14. Explain why the deposition temperature for polysilicon films is moderately low, usually between 600°C and 650°C.

SECTION 8.5: METALLIZATION

15. An e-beam evaporation system is used to deposit aluminum to form MOS capacitors. If the flatband voltage of the capacitance is shifted by 0.5 V because of e-beam radiation, find the number of fixed oxide charges (the silicon dioxide thickness is 50 nm). How can these charges be removed?
16. A metal line ($L = 20 \mu\text{m}$, $W = 0.25 \mu\text{m}$) has a sheet resistance of $5 \Omega/\square$. Calculate the resistance of the metal line.
17. Calculate the thicknesses of the TiSi_2 and CoSi_2 , where the initial Ti and Co film thicknesses are 30 nm.
18. Compare the advantages and disadvantages of TiSi_2 and CoSi_2 for salicide applications.
19. A dielectric material is placed between the two parallel metal lines. The length $L = 1 \text{ cm}$, width $W = 0.28 \mu\text{m}$, thickness $T = 0.3 \mu\text{m}$, and spacing $S = 0.36 \mu\text{m}$. (a) Calculate the RC time delay. The metal is Al with a resistivity of $2.67 \mu\Omega\text{-cm}$, and the dielectric is oxide with dielectric constant 3.9. (b) Calculate the RC time delay. The metal is Cu with a resistivity of $1.7 \mu\Omega\text{-cm}$, and the dielectric is organic polymer with dielectric constant 2.8. (c) Compare the results in (a) and (b). How much can we decrease the RC time delay?
20. Repeat Problems 19 (a) and (b) if the fringing factor for the capacitors is 3. The fringing factor is due to the spreading of the electric-field lines beyond the length and the width of the metal lines.
- *21. To avoid electromigration problems, the maximum allowed current density in an aluminum runner is about $5 \times 10^5 \text{ A/cm}^2$. If the runner is 2 mm long, 1 μm wide, and nominally 1 μm thick, and if 20% of the runner length passes over steps and is only 0.5 μm thick there, find the total resistance of the runner if the resistivity is $3 \times 10^{-6} \Omega\text{-cm}$. Find the maximum voltage that can be applied across the runner.
- *22. To use Cu for wiring, one must overcome several obstacles: the diffusion of Cu through SiO_2 , adhesion of Cu to SiO_2 , and corrosion of Cu. One way to overcome these obstacles is to use a cladding/adhesion layer (e.g., Ta or TiN) to protect the Cu wires. Consider a cladded Cu wire with a square cross section of $0.5 \mu\text{m} \times 0.5 \mu\text{m}$ and compare it with a layered TiN/Al/TiN wire of the same size, with the top and bottom TiN layers 40 nm and 60 nm thick, respectively. What is the maximum thickness of the cladding layer if the resistances of the cladded Cu wire and the TiN/Al/TiN wire are the same?